High-performance normally-off tri-gate GaN power MOSFETs

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***Abstract*— In this work, we present the investigation of the combination of gate recess and tri-gate structures to achieve high performance normally-off GaN-on-Si MOSFETs with high positive threshold voltage (V_{TH}), low specific on resistance ($R_{ON,SP}$) and high output current (I_D^{max}). The excellent channel control capability offered by tri-gate structure led to a reduced OFF-state leakage current (I_{OFF}), higher ON/OFF ratio, smaller sub-threshold slope (*SS*) compared to similar planar and recessed-gate devices. With gate to drain length (L_{GD}) of 20 µm, a soft V_{BR} of 1800 V at 1 µA/mm and hard V_{BR} of 2050 V at 9 µA/mm were observed, along with a low $R_{ON,SP}$ of 2.42 mΩ·cm², which corresponds to a state-of-the-art figure of merit (FOM) of 1.73 GW/cm². These results unveil the extraordinary prospects of tri-gate technology for future power electronics applications.**

***Keywords*— Gallium Nitride, normally-off, MOSFET, tri-gate, recess, high breakdown, low leakage**

I. Introduction

GaN transistors are very promising for future high-frequency power electronics converters with low conduction and switching losses and high blocking voltages [1]–[3]. Due to the presence of a polarization-induced two-dimensional electron gas (2DEG) [4], it is currently challenging to demonstrate concurrently a sufficiently positive V_{TH} with low R_{ON}, along with high breakdown voltage in GaN (MOS)HEMTs for normally-off (E-mode) operation, which is highly demanded by most power electronics applications [5]–[7].

Several techniques were reported in the literature to achieve normally-off operation, such as p-GaN gate [8], fluorine-based plasma treatment [9], [10], and recessing the barrier [11]–[14] under the gate region, either fully or partially [18], however these methods typically degrade R_{ON} and lower the I_D^{max}. Tri-gate structure can offer a way to control the V_{TH}, to enhance gate control [15]–[17] and to yield large V_{BR} [18]–[20]. Nonetheless, only a relatively limited positive V_{TH} can be achieved by relying solely on tri-gates, as shown in [21]. Much larger V_{TH} can be achieved by combining gate recess with tri-gate structures, however, to this date, only mild positive V_{TH} of 0.5 V has been demonstrated [15].

In this work, high performance normally-off GaN MOSFETs are demonstrated with high V_{BR}. A short gate recess was integrated with an optimized tri-gate geometry, fabricated with low-damage etching and a judicious surface treatment to minimize electron scattering in the channel. These devices presented V_{TH} of 1.4 V (defined at 1 µA/mm), high I_D^{max} of 622 mA/mm, improved *SS* of 95 mV/dec and large ON/OFF ratio beyond 10^9. In addition, the tri-gate region converts part of the gate electrode into a gate-connected FP (Fig. 1(a)), which resulted in an exceptional V_{BR} of up to 2050 V for L_{GD} of 20 µm with I_{OFF} below 9 µA/mm.

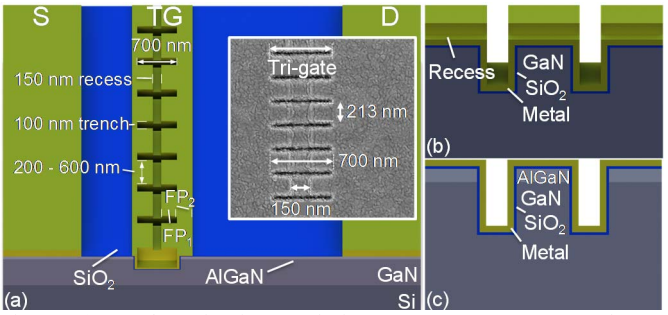

Fig. 1. (a) 3D schematic of recessed tri-gate MOSFET. Inset: zoomed SEM images of tri-gate regions. Cross-sectional views of recessed tri-gate MOSFET of (b) recessed regions and (c) tri-gate regions.

II. Device Structure and Fabrication

Fig.1 depicts the 3D schematic (Fig. 1(a)) and cross-sectional schematics (Fig. 1(b-c)) of the fabricated normally-off tri-gate GaN MOSFETs based on GaN-on-Si wafers. The wafer structure consisted of 4.2 µm buffer, 420 nm un-doped GaN channel, 20 nm $Al_{0.25}Ga_{0.75}N$ barrier and 2.5 nm GaN cap layer. The device fabrication started with mesa and tri-gate regions definition by e-beam lithography, and followed by Cl_2-based ICP etch. A 150 nm-wide gate recess (Fig. 1 (a)) was defined by e-beam lithography, followed by a 20 nm-deep low-damage slow-etch-rate Cl_2-based ICP etch, which resulted in a very precise control of the etch depth. The etched surfaces were treated with 5 cycles of O_2 plasma/HCl (37%) for 1 min each, followed by a 500°C annealing for 5 min. The low-damage slow-rate gate recess combined with cycled O_2 plasma/HCl treatment is a critical process for smoother etched surface, which minimizes electron scattering in the short recessed channel and results in E-mode transistors with reproducible V_{TH} and low R_{ON}. A metal stack composed of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/ Ni (60 nm)/ Au (50 nm) was deposited in both source and drain regions, followed by rapid thermal annealing

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(RTA) at 780°C under N_2 atmosphere. The 25 nm-thick SiO_2 gate dielectric was deposited by atomic layer deposition (ALD) at 300°C, immediately after a surface treatment in 37% HCl for 1 min and 500°C bake for 5 min. Finally, gate metal was formed by 50 nm Ni/ 150 nm Au. All device characteristics, such as I_D, R_{ON}, I_{OFF}, were normalized by the device width of 80 µm, and the standard deviation was determined from about 8 separate devices of the same kind.

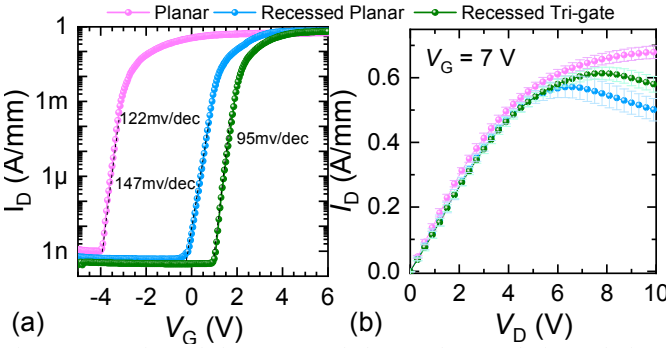

Fig. 2. Comparison of planar, recessed planar and recessed tri-gate devices. (a) Transfer at V_{DS} = 5 V and (b) Output characters of the three device with V_G = 7 V. The L_{GS}, L_G and L_{GD} were 1.5, 2 and 15 µm, respectively, and *FF* was 0.66.

III. Results and Discussion

The comparison of the DC transfer and output characteristics of planar, recessed and recessed tri-gate devices is shown in Fig. 2(a) and (b). A noteworthy shift of V_{TH} was observed from –3.6 V for the planar, to +0.3 V for the recessed and +1.4 V for the recessed tri-gate (V_{TH} was defined at 1 µA/mm) (Fig. 2(a)). The normally-off tri-gate MOSFET presented a steeper *SS* and a lower I_{OFF} compared with recessed planar devices, revealing a better gate control by the tri-gate. The recessed tri-gate exhibited an ON/OFF ratio beyond 10^9, an improved *SS* of 95 ± 3.2 mV/dec and I_{OFF} as small as 300 pA/mm at V_G = 0, compared to 30 nA/mm for the recessed device. Moreover, these devices presented high I_D^{max} (at V_G = 7 V) of 622 ± 16 mA/mm compared to 581 ± 34 mA/mm for the recessed, which was only slightly smaller than that of the normally-on planar device (672 ± 19 mA/mm) (Fig. 2(b)). The R_{ON} of planar, recessed and recessed tri-gate, extracted from I_D-V_D sweeps in the linear region, were 6.82 ± 0.29 Ω·mm, 7.37 ± 0.45 Ω· mm, and 7.32 ± 0.26 Ω·mm at V_G = 7 V, respectively (Fig. 2(b)).

The V_{TH} and *SS* for the recessed planar devices shifted with the variation of V_D, as observed in Fig. 3(a), which was not the case in planar and recessed tri-gate devices. This was mainly due to short-channel effects on the narrow recessed regions (100 to 150 nm) of the recessed gate transistors, which lacks effective gate control. The improved channel control of the tri-gate structure was effective in reducing the short-channel effects of the narrow recessed-gate MOSFETs [15], which makes possible to increase the I_D^{max} and reduce R_{ON} without increasing the recess length. Fig. 3(b) shows transfer characteristics of recessed tri-gate devices with different recess length (100 nm to 600 nm). We observed

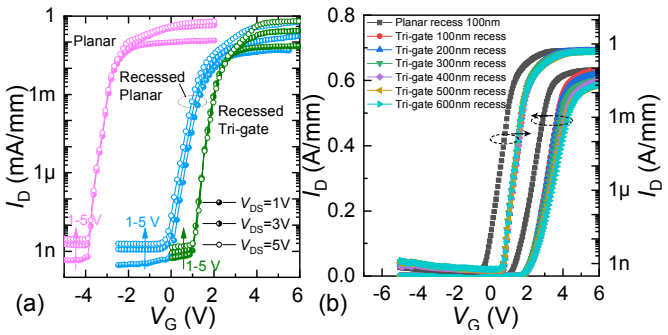

Fig. 3. (a) Comparison of the normally-off recessed tri-gate with planar and recessed devices under different V_{DS} (1V to 5V). (b) Comparison of planar recessed transistors with recessed tri-gate under different recess length (100nm to 600 nm).

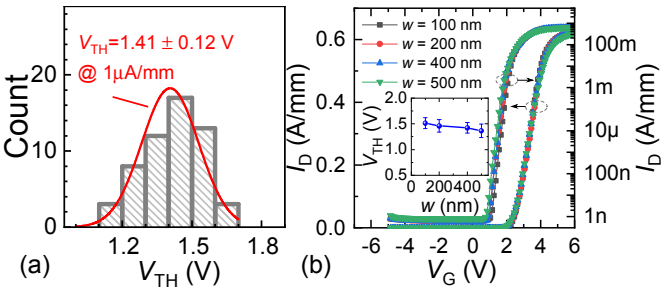

Fig. 4. (a) Distribution of V_{TH} of 56 recessed tri-gate devices. (b) Transfer characteristics of recessed tri-gate with different nanowire width. Inset: The extracted V_{TH} dependence with tri-gate nanowire width (*w*).

that the 100 nm-wide recessed planar device showed near normally-off behavior, but when combining the 100 nm-wide recess with tri-gate structures led to a much higher V_{TH} compared to planar devices. Moreover, the threshold voltage of recessed tri-gate devices remained unchanged with the variation of recess length up to 600 nm. Nevertheless, the maximum saturation current decreased with increasing recess length. Therefore, the enhanced gate control of recessed tri-gate allows to significantly reduce the gate recess length to minimize current degradation, without any detriment from short channel effects.

Fig. 4(a) shows the narrow V_{TH} distribution among measured 56 recessed tri-gate devices, with a V_{TH} of +1.41 ± 0.12V, confirming the excellent process uniformity. To optimize the tri-gate geometry, we fabricated devices with tri-gate width *w* of 200, 400, 500, and 600 nm and fixed spacing *s* of 100nm, corresponding to a number of tri-gate fins per mm N_{NW} of 3333, 2000, 1666, and 1333, respectively. The transfer characteristics of recessed tri-gate transistors with different *w* is shown in Fig. 4(b). The inset of Fig. 4(b) revealed that V_{TH} is not strongly dependent on the tri-gate width, which indicates the absence of 2DEG in the recessed region. A reduction of R_{ON} and an increase in I_D^{max} were observed when reducing the filling factor (*FF*) (Fig. 5(a)). The equivalent circuit (Fig. 5(b)) of the recessed tri-gate MOSFETs included 2 parallel parts: top (recessed + planar) and trench portions (sidewall and bottom portions). For small *FF*, the main conduction contribution is from the sidewall region, whereas by increasing *FF*, N_{NW} is reduced and the contribution from the top regions become

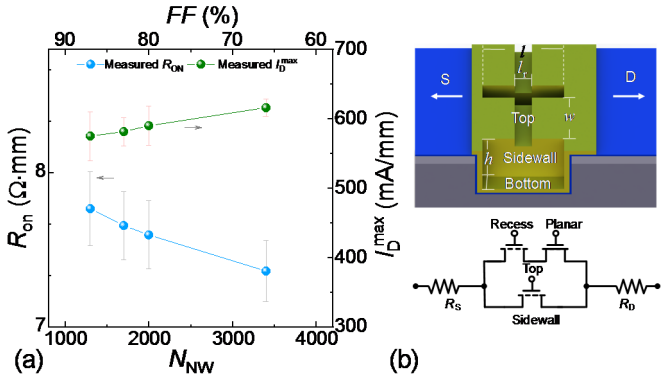

Fig. 5. (a) R_{ON} and I_D^{max} of the recessed tri-gate versus N_{NW} and FF. (b) Schematic and equivalent circuit of the recessed tri-gate region.

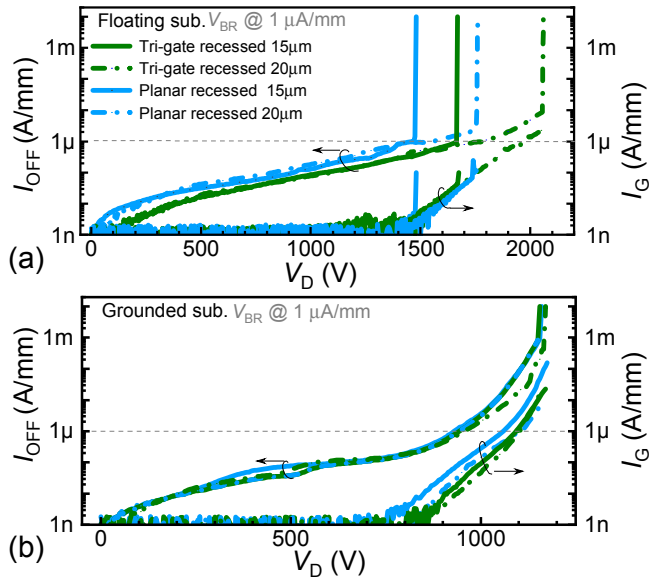

Fig. 6. Three terminal breakdown characteristics of recessed tri-gate (V_G = 0 V) and recessed planar (V_G = -1 V) MOSFETs with L_{GD} = 15 μm and 20 μm, for (a) floating and (b) grounded substrate.

dominant.

The three terminal breakdown voltage of the devices was measured with floating (Fig. 6(a)) and grounded substrate (Fig. 6(b)), with V_G = 0 V for the recessed tri-gate transistors and V_G=-1 V for the recessed planar devices. With floating substrate, the hard V_{BR} of the recessed tri-gate with L_{GD} of 15 μm and 20 μm were 1650 V (at 1 μA/mm) and 2050 V (at 9 μA/mm), respectively, compared with 1480 V and 1750 V, respectively, in recessed planar devices. The soft V_{BR} at I_{OFF} of 1μA/mm of the recessed tri-gate with L_{GD} of 20 μm was 1800 V compared with 1600 V of the recessed planar devices. The improvement in V_{BR} of recessed tri-gate devices was mainly due to the integrated FP_1 and FP_2 in the tri-gate regions (Fig.1(a)) [17]. Moreover, the OFF-state gate leakage of recessed tri-gate was also much smaller than recessed planar devices, leading to a higher soft V_{BR}. A large V_{BR} of 960 V at 1 μA/mm was also observed with grounded substrate, for both recessed and recessed tri-gate with L_{GD}= 15 μm or 20 μm, which was mainly limited by the 4.2 μm buffer thickness. The hard V_{BR} of the grounded substrate can be as high as 1100 V.

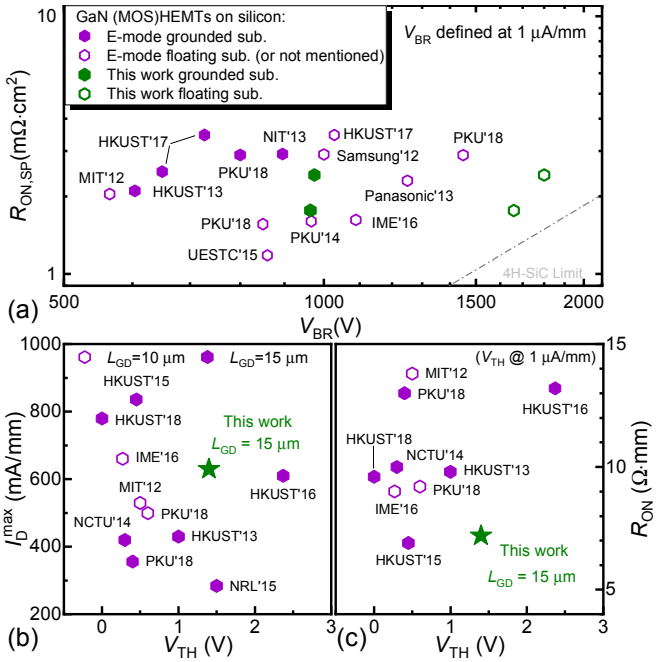

Fig. 7. Benchmarking of (a) $R_{ON,SP}$ versus V_{BR} of the recessed tri-gate against E-mode GaN-on-Si transistors, by defining V_{BR} at I_{OFF}< 1μA/mm with floating and grounded substrates. (b) $I_D^{max}$and (c) R_{ON} versus V_{TH} (defined at 1μA/mm). For fair comparison, L_{GD} smaller than 10 μm, and literature results with unspecified $R_{ON,SP}$ or I_{OFF} were not included.

Fig. 7 shows the performance of our recessed tri-gate normally-off transistors benchmarked against state-of-the-art E-mode GaN-on-Si transistors in the literature. Fig. 7(a) was benchmarked with both floating and grounded substrate of $R_{ON,SP}$ versus V_{BR}, which outperform other device with both methods. We also benchmarked with I_D^{max} versus V_{TH} (Fig. 7(b)) and R_{ON} versus V_{TH} (Fig. 7(c)), our device exhibited high I_D^{max}, low R_{ON} and large V_{TH} of 1.4 V (Fig. 7(b-c)), with $R_{ON,SP}$ of 1.76 and 2.42 mΩ·cm² for L_{GD} of 15 μm and 20 μm, respectively.

IV. Conclusion

In this work, we have demonstrated state-of-the-art normally-off recessed tri-gate GaN-on-Si MOSFETs presenting V_{TH} of 1.4 V at 1μA/mm, high I_D^{max}, low $R_{ON,SP}$ of 2.42 mΩ·cm² and high V_{BR} of 2050 V, corresponding to a record FOM of 1.73 GW/cm². These results unveil the excellent prospect of recessed tri-gate for power applications.

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