Record Efficiency N-type and High-efficiency P-type Mono-like Silicon Heterojunction Solar Cells with High Temperature Gettering Process

Maulid M. Kivambe[†], Jan Haschke[‡], Jörg Horzel[§], Brahim Aïssa[†], Amir A. Abdallah[†], Abdelhak Belaidi[†], Raphaël Monnard[‡], Loris Barraud[§], Antoine Descoeudres[§], Fabien Debrot[§], Matthieu Despeisse[§], Mathieu Boccard[‡], Christophe Ballif[‡] and Nouar Tabet[†]*

[†]*Qatar Environment and Energy Research Institute (QEERI), Hamad bin Khalifa University, Qatar Foundation, P.O. Box 5825, Doha, Qatar*

[‡]*Photovoltaics and Thin-Film Electronics Laboratory (PV-lab), Institute of Microengineering, Ecole Polytechnique Fédérale de Lausanne (EPFL), Rue de la Maladière 71B, CH-2002 Neuchâtel, Switzerland*

[§]*Swiss Center for Electronics and Microtechnology (CSEM), PV-center, Rue Jaquet Droz 1, CH-2002 Neuchâtel, Switzerland*

*Email: mkivambe@hbku.edu.qa, Tel +97444548114

ABSTRACT: We report independently confirmed 22.15% and record 22.58% power conversion efficiencies, for thin (130 μm – 140 μm) p- and n-type mono-like Si solar cells, respectively. We comparatively assessed advanced n-type and p-type mono-like silicon wafers for potential use in low-cost high-efficiency solar cell applications by using phosphorus diffusion gettering for material-quality improvement and silicon heterojunction solar cell fabrication for assessment of performance in high-efficiency photovoltaic device architecture. We show that gettering improves material quality and device properties significantly, depending on the type of doping (n-type or p-type), wafer position in the ingot, drive-in temperature and cooling profile. Owing to the high open circuit voltage (725 mV), the record n-type solar cell also represents the highest reported solar cell efficiency for cast silicon to date.

KEY WORDS: mono-like Si, cast-mono Si, quasi-mono Si, silicon heterojunction solar cell, high efficiency, phosphorus diffusion gettering

INTRODUCTION

Improvement in the power conversion efficiency and reduction in the cost of wafers are important paths for further reduction in the cost of silicon photovoltaics [1]. Therefore, manufacturing high quality wafers at low cost is of paramount importance to reduce the levelized cost of solar electricity. Currently, the record solar cell efficiency for industrial-standard low-cost substrates, i.e. multicrystalline silicon is 22.3% for lab-scale device (4-cm^2 area, n-type) [2, 3] and 22.0% for

large area device (246-cm^2 area, p-type) [3]. Low-cost substrates with higher efficiency potential than multicrystalline silicon include kerfless epitaxial silicon [4, 5] and Mono-like silicon, which is the subject of this study. Mono-like silicon, quasi-mono or cast-mono silicon is produced by directional solidification of feedstock melt on top of partially melted single crystal silicon seeds in a crucible [6]. It gained significant interest in PV industry following demonstration of casting of high quality large-scale ingots by BP Solar in 2008 [7, 8]. Being mostly monocrystalline yet cast, mono-like silicon offers simultaneously the advantages of monocrystalline silicon such as compatibility with alkaline texturization and the high throughput and yield of standard multi-crystalline silicon growth [6]. However, today's share of mono-like Si in the photovoltaics (PV) market is negligible [9]. This is mainly due to the emergence of high performance multi-crystalline silicon (HPMC) [10-12] which contains lower intra-granular dislocation density [13], has higher throughput and narrower efficiency distribution [12, 14] than mono-like silicon. Growth of mono-like silicon requires additional temperature control to preserve the seeds from melting with the feedstock leading to slight increase in the processing time [6]. In addition, mono-like silicon ingots contain a significant fraction of parasitic multicrystalline silicon resulting from grain nucleation on crucible sides [15-17] and dislocations can easily be generated from sources such as seed joints, easily propagate with the growing crystal and multiply into clusters of high density [15, 18-21]. Significant efforts in addressing the overall quality of mono-like silicon material through growth process optimization [21-24], gettering, and bulk passivation [25, 26], have been conducted in recent years. Very high minority carrier lifetimes (>3 ms) [21], and high efficiency (>21.5%) large area (~104 cm^2) mono-like silicon heterojunction (SHJ) solar cells have been reported [25], maintaining the potential and continued interest in this material. In fact, a record 22.28% efficiency large area (246-cm^2 area) p-type cast-mono silicon has been recently reported [27].

Despite the fact that the most efficient silicon solar cells of monocrystalline silicon, high performance multi-crystalline silicon [3], and mono-like silicon [25], are n-type, the current PV market is ~ 95% p-type [9]. Preference of p-type Si by commercial manufacturers is partly historical, stemming from superior radiation resistance of p-type solar cells and their application in space and spacecraft industry [28]. Currently, the main reasons are cheaper wafers and simplicity of fabrication processes [29], facilitated by uniformity in the resistivity (the effective segregation coefficient of boron dopant in silicon is near unit), lower-temperature phosphorus diffusion process for junction formation and for gettering of deleterious metallic impurities compared to temperature and additional steps required for boron diffusion. Progress in the identification of the impurities and their detrimental impact on diffusion length as well as in the development of methods for their removal or engineering their distribution in wafers [30, 31] is also a significant advantage for p-type. However, there has been significant progress in understanding and overcoming the challenges of crystallization and processing of n-type Si for commercial applications in PV. In fact, un-compensated n-type Si does not suffer from boron-oxygen defect [32] and the capture cross-section of most metal contaminants such as Fe, Ni and Cr, are much lower in n-type Si than in p-type Si [33, 34]. In addition, the non-uniformity in distribution of dopants can be overcome by replenishment of un-doped Si in a continuous Czochralski (Cz) Si crystallization system [35, 36]. It must be mentioned however, that in this technique, the melt and therefore the subsequent crystal are expected to get richer in impurity content due to the segregation coefficient of most of the metallic contaminants in silicon being much less than unit [37]. Nevertheless, further improvements in material quality, particularly of low-cost substrates and reduction in the device processing cost are still necessary. In this work, we have carried-out phosphorus diffusion gettering experiments to compare gettering efficacy of n-type and p-type mono-like silicon for solar cells by using 811 °C

and 900 °C plateau temperatures. We observe significant differences in the gettering response: the 900 °C process temperature resulted in higher gettering efficacy for n-type silicon, whereas the 811 °C process temperature gave the best results for p-type silicon. We report independently certified record power conversion efficiencies of 22.15% (p-type) and 22.58% (n-type) SHJ solar cells on wafers gettered with 811°C and 900°C plateau temperatures, respectively.

MATERIALS AND METHODS

The wafers used in this study were supplied by ECM Greentech (Grenoble, France). The mono-like silicon wafers with starting size of 156 mm × 156 mm × 190 μm and a resistivity of 1-2 **Ω**-cm for p-type Si and 2-5 **Ω**-cm for n-type, were selected from ~ 60-80 mm, 100-120 mm, 140 – 160 mm, 180 – 200 mm and 200 – 220 mm block-heights of ~270 mm high, 6th generation ingots. Material and device processing sequence are depicted in **Figure 1**. Wafers for as-grown property assessment received only saw-damage removal of the steps listed in **Figure 1(a)**, but the full sequence of the solar cell process listed in **Figure 1(b)**. For easier cell processing and characterization, the wafers were laser-cut into 4”-diameter circular shape. Five solar cells, sized 2 cm × 2 cm were fabricated per wafer, as shown in **Figure 1(d)**. The final thickness of the solar cells was 130 μm – 140 μm.

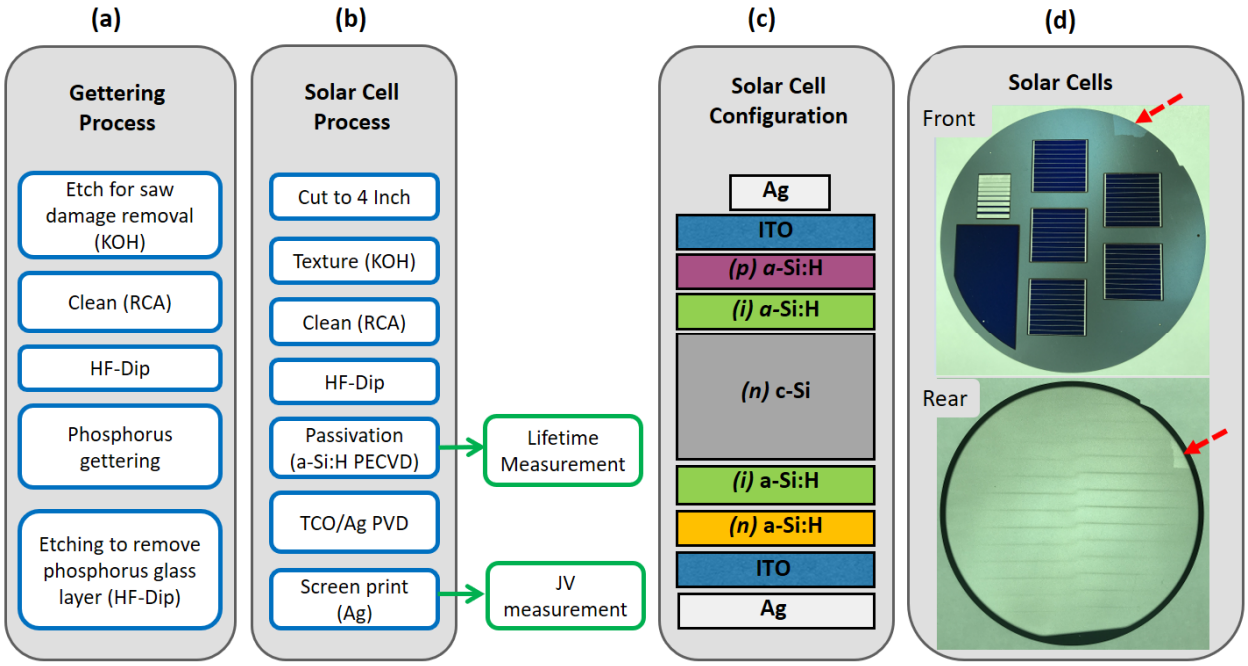

Figure 1. (a) Sequence for the gettering process. (b) Sequence for solar cell fabrication. (c) Device configuration for the n-type solar cells. (d) A photograph showing the front and the rear of the typical fabricated solar cells. Some multicrystalline grains can be visually observed wafers and in solar cells, as shown by the arrows in (d).

Three phosphorus diffusion gettering schemes, namely 811 °C, 900 °C and 900 °C + R (R stands for ramping) were used. The time-temperature profiles are depicted in **Figure 2(a)**. After $POCl_3$ deposition at 804 °C, the temperature was raised to 811 °C or 900 °C, and held for 20 minutes to drive-in phosphorus, then cooled at a rate of 4.6 °C/min to 800 °C and un-loaded. One of the recipes (900 °C + R) involved steady slow cooling (at a rate of 2.0 °C/min) from 900 °C to 600 °C before un-loading. The resulting profiles of electrically active phosphorus concentration as a function of doping depth for each gettering regime were obtained by electrochemical capacitance-

voltage (ECV) method [38, 39] (WEP wafer profiler CVP21) and are presented in **Figure 2(b)**. The 900 °C regime results in the highest surface concentration of active phosphorus while the 900 °C + R regime results in the deepest dopant diffusion.

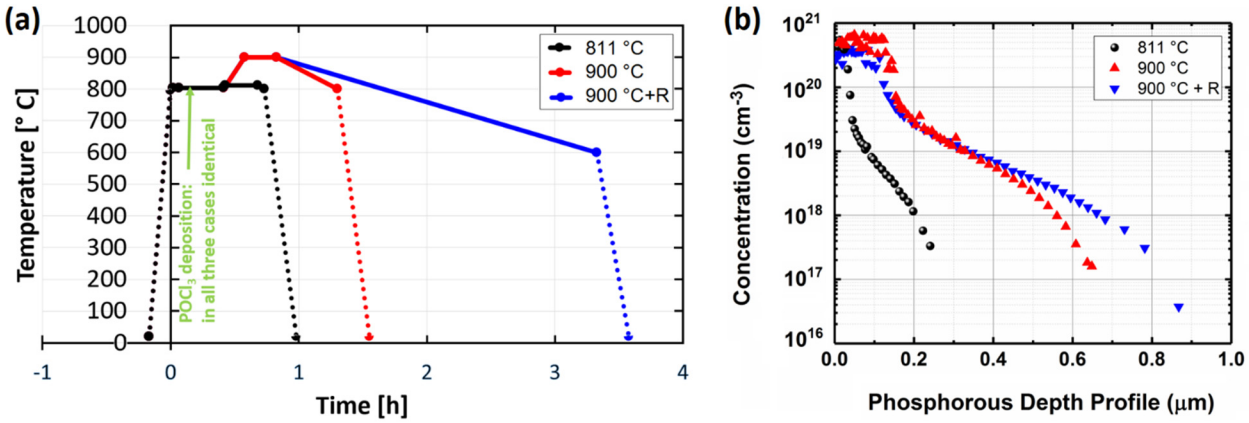

Figure 2. (a) Schematic time-temperature profiles, and (b) depth profiles of concentration of electrically-active phosphorus measured by ECV method for the 811 °C, 900 °C and 900 °C with slow cooling (900 °C + R) gettering schemes.

RESULTS AND DISCUSSION

All lifetime values reported here-in are effective minority carrier lifetimes at an injection level of 1×10^{15} cm^{-3}, measured by photoconductivity method [40] (Sinton WCT-120TS lifetime tester) . **Figure 3** shows lifetimes and implied open circuit voltage (iV_{OC}) measured on as-grown and on respective gettered sister wafers taken from various ingot-height positions after passivation with amorphous silicon layers (KAI-M PECVD tool). Lifetimes for the passivated as-grown wafers are

below 600 µs in all cases. Significant lifetime and iV_{OC} enhancements are observed with gettering. Gettering at 811 °C leads to the highest lifetime and iV_{OC} improvement for p-type Si, whereas n-type Si benefits most from gettering at 900 °C. For instance, gettering the edge-block p-type wafers from 100 – 120 mm ingot-height position at 811 °C improves lifetime from 310 µs to 900 µs, while gettering at 900 °C improves the lifetime to only 410 µs. Conversely, for the same ingot height, gettering n-type wafers at 811 °C improves their lifetime from 540 µs to ~1.2 ms, while gettering at 900 °C improves their lifetime up to 3.6 ms. Slow cooling treatment after high temperature plateau (i.e. gettering with 900 °C + R) lead to lower lifetime than gettering with the 900 °C profile in all cases.

In this batch of experiments, the maximum lifetime and iV_{OC} for p-type wafers were 1.3 ms and 745 mV respectively, on a sample from 140 mm ingot height, gettered at 811 °C and having resistivity of 1.52 Ω-cm. For the n-type wafers, the maximum lifetime and iV_{OC} were 3.8 ms and 737 mV, respectively, on a sample from 72 mm ingot height, gettered at 900 °C and having resistivity of 3.85 Ω-cm. The impact of the different responses to these various treatments on device performance are discussed below.

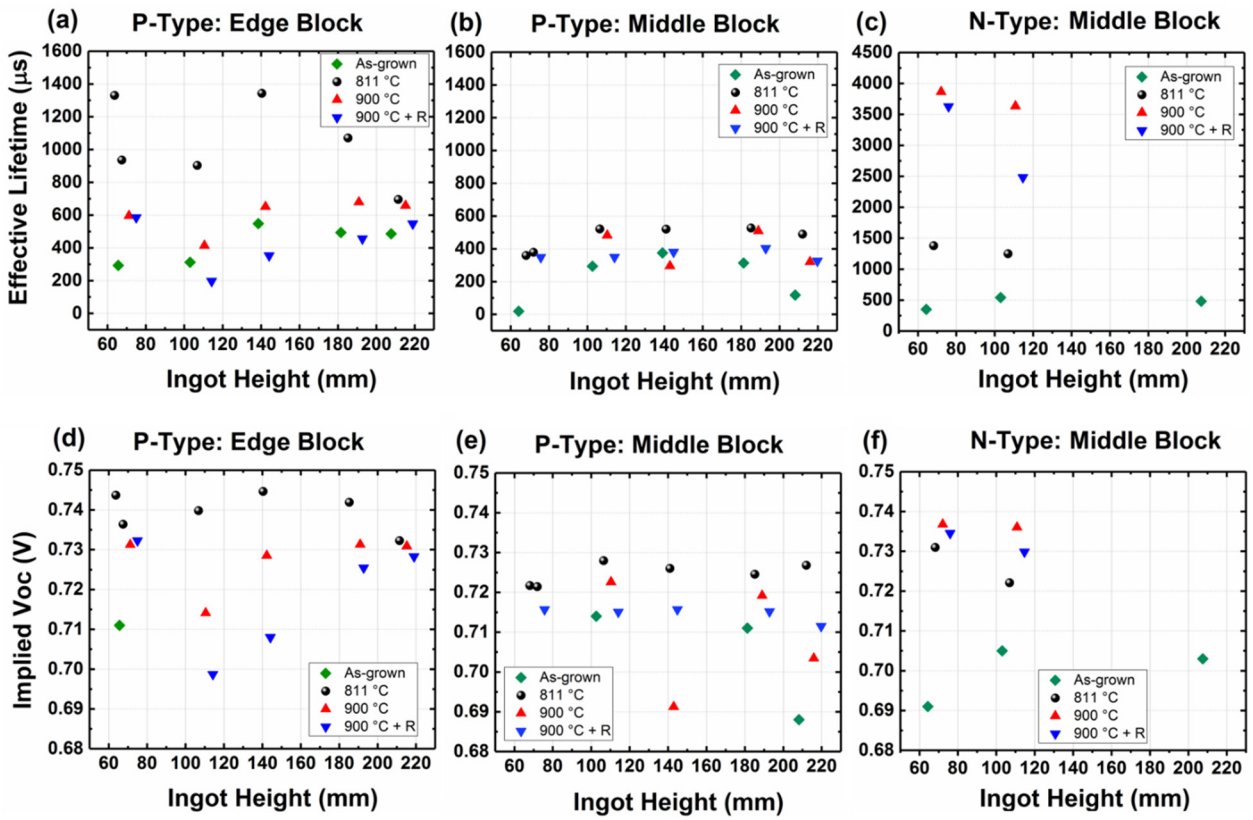

Figure 3. Effective minority carrier lifetime and iV_{OC} at different ingot height positions for p-type edge-block (a, d), p-type middle-block (b, e) and n-type middle-block wafers (c, f). Note the difference in vertical scale for the lifetime of n-type and p-type wafers.

Minority carrier lifetime and diffusion length in p-type Si are mostly governed by iron, where both Fe_i and FeB pairs show strong recombination activity [41, 42]. Cu_i, CuB pairs [43], Cr_i and CrB pairs [44] and silicide precipitates of Cu and Ni [41], have also been observed to cause significant lifetime degradation in p-type Si. In addition to the lower capture cross-section for holes than for electrons for most transition metal impurities in silicon [33, 34], there is no defect complex similar to metal-boron pairs associated with phosphorus doping. The electronic properties of n-type Si are therefore expected to generally be superior to those of p-type Si. On the difference in gettering response and

performance of n-type and p-type wafers upon high and low temperature gettering, Morishige [45], reported significant differences in the impact of precipitate size on the diffusion length of charge carriers in n-type and p-type Si wafers. It was observed that smaller precipitate fraction (larger precipitate size) was more detrimental to n-type Si and larger precipitate fraction (smaller precipitate size) to p-type Si. Since higher processing temperature results in smaller precipitate density [31], it is conceivable that the 900 °C gettering profile would result in larger fraction of the remaining precipitates than the 811 °C profile, making the latter more beneficial to p-type Si and the former to n-type Si.

Figure 4 shows photoluminescence (PL) intensity images [46, 47] of solar cells fabricated on the gettered wafers from 100 – 120 mm ingot height **(Figures 4a-f)** and from 200 – 220 mm ingot height **(Figures 4g-i)** for which lifetime values are shown in **Figure 3**. Areas of low PL signal are observed in areas with extended defects such as dislocation clusters and grain boundaries. For example, the recombination activity of multi-crystalline silicon grains marked by arrows in **Figures 4a-c** remains strong with all the three gettering profiles. Dislocation density in cast silicon is expected to increase with the ingot height [15, 48, 49], which is indeed observed here. Large areas of low PL count characteristic of large dislocation clusters are observed in all gettering schemes, for wafers from 200 – 220 mm ingot height, i.e. near the ingot top (Figures 4g-i). Note that the dark cell lines in the image are the front silver metal contacts. These results suggest that further improvement in the quality of the material, through growth process optimization to reduce dislocation density and the fraction of multicrystalline grains as well as post-growth defect

engineering to further reduce the impact of the dislocations and impurities on minority carrier lifetime are still necessary and possible.

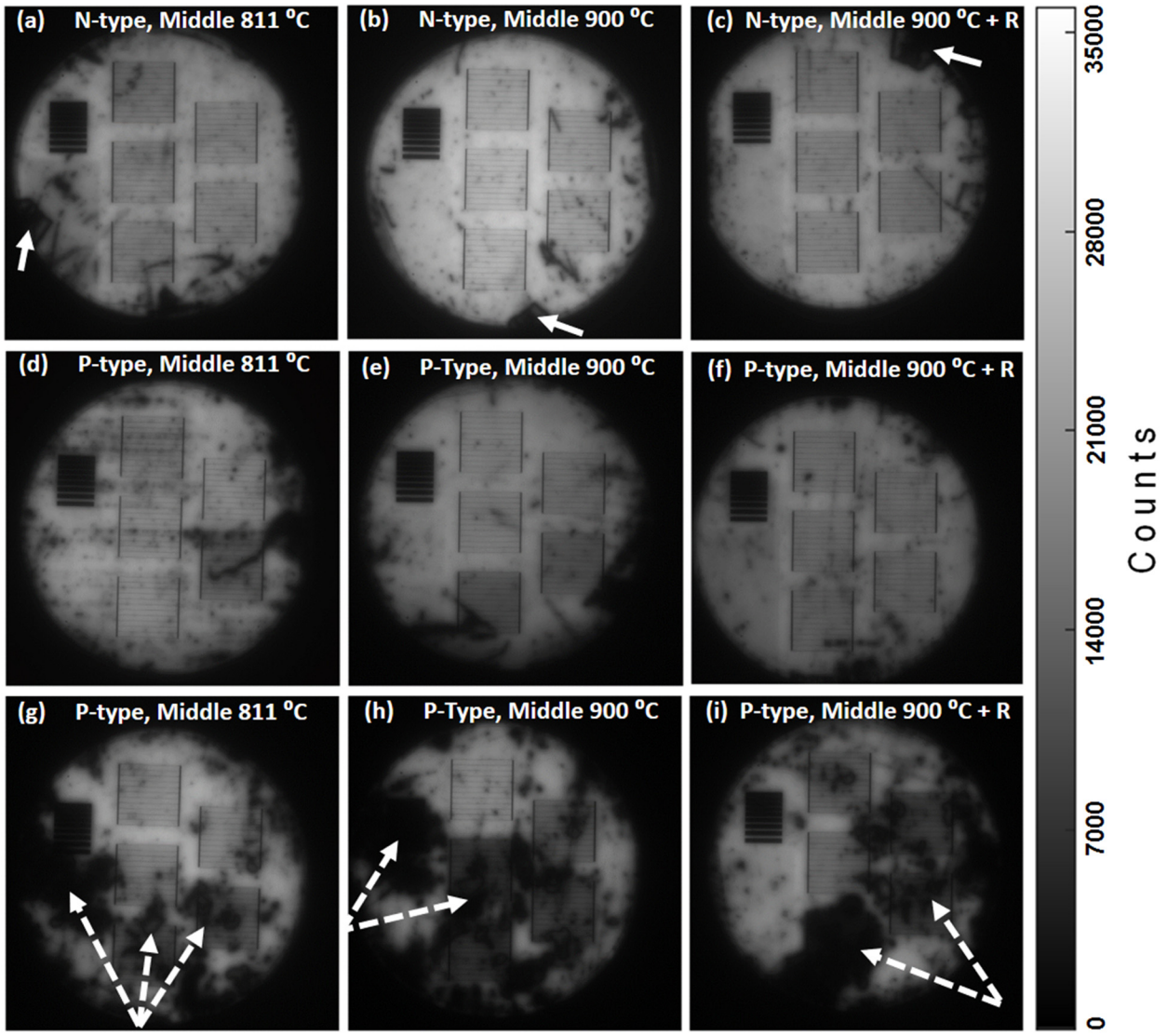

Figure 4. PL intensity images of solar cell devices fabricated on gettered n-type wafers from ~100 – 120 mm ingot heights (a-c), and p-type wafers from 100 – 120 mm (d-f) and from 200 – 220 mm (g-i), ingot heights for the three gettering profiles.

Figure 5 shows the n-type solar cell device characteristics for the wafers whose lifetime and iV_{OC} values are shown in **Figures 3c** and **3f**, respectively. Most of the n-type solar cells show significant improvement in all device properties, in comparison to the as-grown state. As could be expected from the lifetime and iV_{OC} data, gettering at 900 °C gives the best solar cell results for open circuit voltage (V_{OC}) and fill factor (FF), and thus efficiency. Indeed, the most efficient solar cell in this batch was achieved with the 900 °C scheme and was 21.93% efficient. The solar cell was from 111 mm ingot height position and had V_{OC} of 721 mV and resistivity of 3.5 Ω-cm. Some of the solar cells particularly those fabricated on wafers from 60 – 80 mm ingot height position and gettered at 811 °C deteriorated in solar cell efficiency, V_{OC} and FF. This can be attributed to the proximity of the wafer's position to the seeds, where the concentration of impurities is usually high [16, 50], together with the existence of multicrystalline grains (**Figure 4**). Low temperature gettering (820 °C) has been reported to be less effective in removing precipitated impurities in multicrystalline silicon than high temperature gettering (880–920 °C) [51].

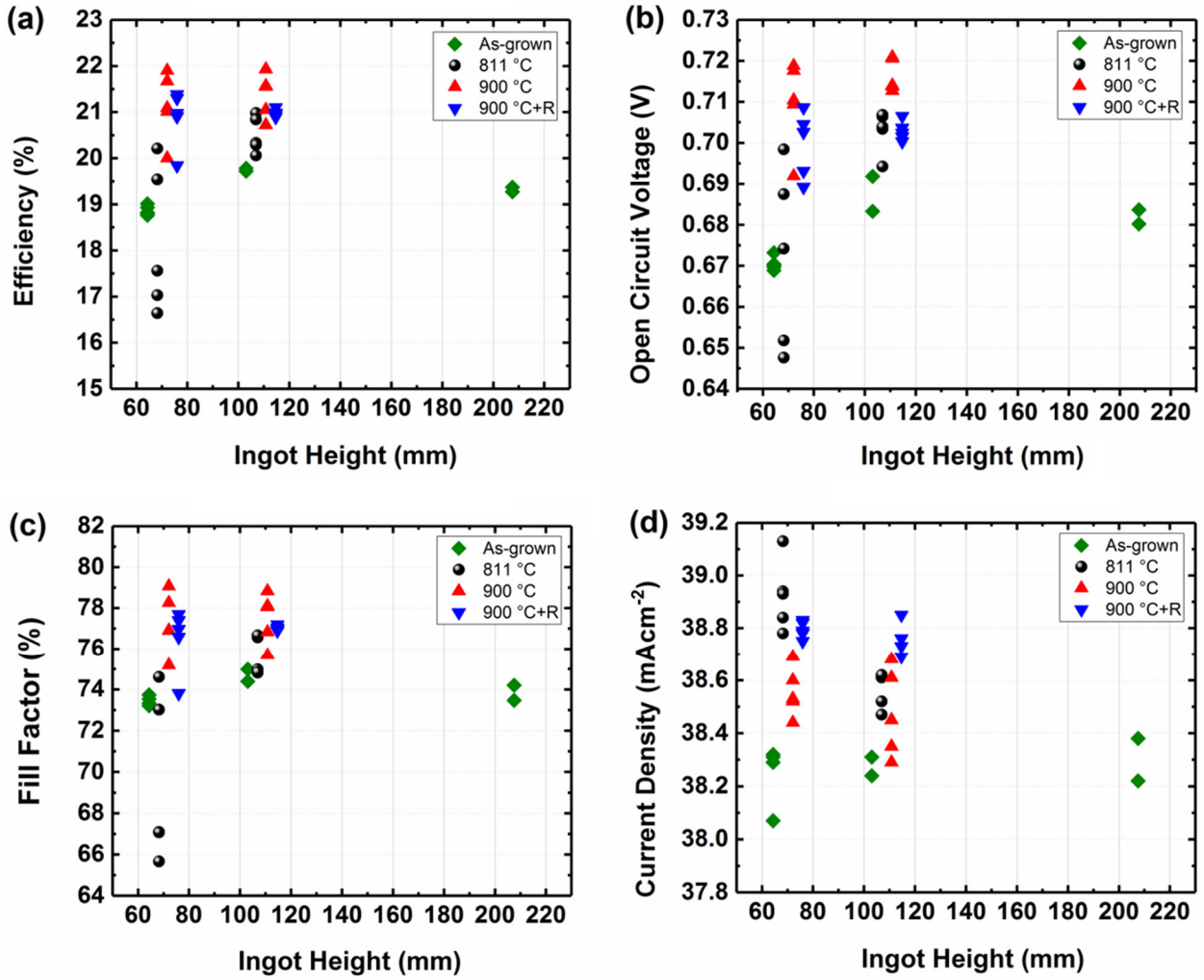

Figure 5. N-type Si solar cell device properties under different gettering profiles. (a) Efficiency, (b) open circuit voltage, (c) fill factor, (d) short circuit current density.

In line with the lifetime and iV_{OC} results (**Figures 3a**, **3b, 3d**, **3e**), device characteristics for the p-type solar cells is expected to show greater efficiency improvement with the 811 °C gettering profile. Thus, 811 °C and 900 °C gettering profiles were used for fabrication of high-efficiency p-type and n-type solar cells respectively, using an optimized SHJ solar cell process and an additional MgF2 layer at the front to form a dual-layer antireflection coating. A 22.15%-efficient p-type solar

cell (**Figure 6a**) and a 22.58%-efficient n-type solar cell (**Figure 6b**), designated area 2 cm × 2 cm were achieved, and independently certified by ISFH CalTeC. To the best of our knowledge, the n-type solar cell efficiency is the highest solar cell efficiency for cast silicon reported to date, and is ~0.3% absolute higher than the record high performance multicrystalline silicon (HPMS) efficiency for the same designated area [2, 3]. It is worth noting that for the results presented here, an industry-like texturing process and screen-printed front-grid metallization was used, whereas the highest efficiency HPMS device was obtained with a front-grid structured by photolithography and black-silicon texturing. This accounts for part of the difference in current density, although the use of a heterojunction architecture in the present case also leads to the more modest current density values. Also, for both material types, the highest-efficiency result only reflects the best 2×2 cm^2 area probed on the wafer. Lower values for full-wafer devices are to be expected.

Despite the excellent results presented in this paper, many challenges mentioned above persist. Increased processing time would lower throughput, and variation in wafer properties and the high density of structural defects would lead to spread in the individual co-processed cell results as observed in the present study and reported in [25] and in [52]. It can therefore be speculated that upscaling the present mono-like silicon results to large area (i.e. 156 mm × 156 mm) solar cells might be more challenging than for HPMS, making it an obstacle for wider adoption of the mono-like Si technology.

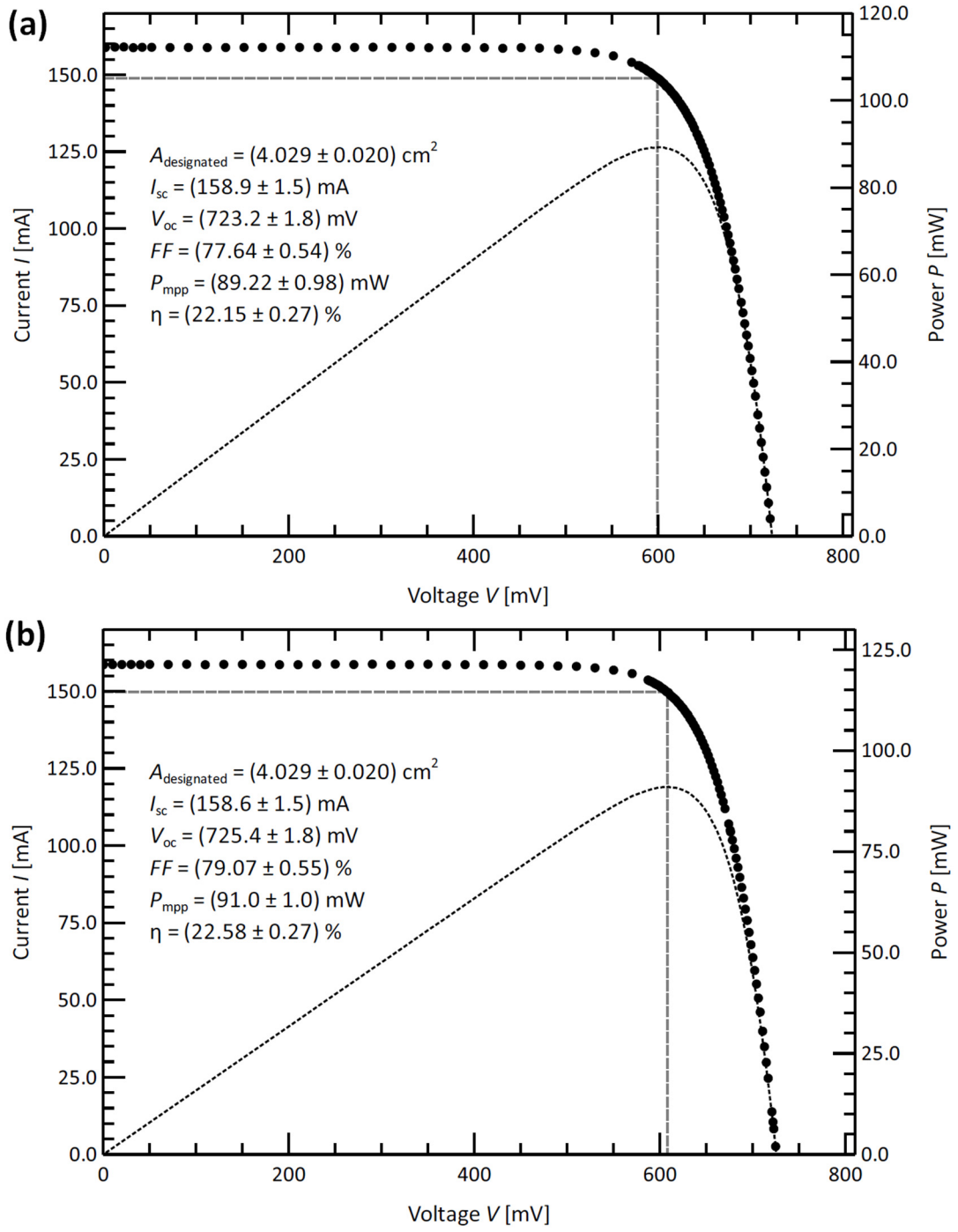

Figure 6. Most efficient mono-like Si solar cells manufactured at CSEM and certified by ISFH CalTeC for (a) p-type solar cell gettered at 811 °C and (b) n-type solar cell gettered at 900 °C.

CONCLUSIONS

In summary, we investigated the potential use of industrial-scale n-type and p-type mono-like silicon wafers in high efficiency silicon heterojunction (SHJ) solar cells. We applied phosphorus diffusion gettering at low (811 °C) and high (900 °C) temperature, and subsequently fabricated SHJ solar cells. Both n-type and p-type wafers can be considerably enhanced by gettering with significant differences: Gettering at 811 °C was more effective in improving the minority carrier lifetime of p–type wafers, whereas the 900 °C profile yielded strongest improvement for n–type wafers. Using tailored gettering process, we report certified efficiencies (ISFH CalTeC) for mono-like SHJ solar cells of 22.15% for p-type solar cell and 22.58% for n-type solar cells, the latter being also the highest solar cell efficiency for cast silicon growth reported to date.

Notes

The authors declare no competing financial interest

ACKNOWLEDGMENT

The authors are grateful to ECM Greentech for support and providing the wafers. This work was supported by Qatar Environment and Energy Research Institute, Qatar Foundation.

REFERENCES

(1) Powell, D.M.; Winkler, M. T.; Choi, H. J.; Simmons, C. B.; Needleman, D. B. and Buonassisi, T. "Crystalline silicon photovoltaics: a cost analysis framework for determining technology pathways to reach baseload electricity costs," *Energy & Environmental Science,* vol. 5, p. 5874, 2012.

(2) Benick, J.; Müller, R.; Schindler, F.; Richter, A; Hauser, H.; Feldmann, F. Krenckel, P.; Riepe, S.; Schubert, M.C. and Hermle, M."Approaching 22% Efficiency with Multicrystalline n-Type Silicon Solar Cells," *33rd European Photovoltaic Solar Energy Conference and Exhibition, Session: 2DO.3.1, Amsterdam, The Netherlands,* pp. 460 - 464, 2017.

(3) Green, M. A.; Hishikawa, Y.; Dunlop, E. D.; Levi, D. H.; Hohl-Ebinger, J.; Yoshita, M. and Ho-Baillie, A.W.Y., "Solar cell efficiency tables (Version 53)," *Progress in Photovoltaics: Research and Applications,* vol. 27, pp. 3-12, 2019.

(4) Kobayashi, E.; Watabe, Y.; Hao, R.; and Ravi, T. S. "High efficiency heterojunction solar cells on n-type kerfless mono crystalline silicon wafers by epitaxial growth," *Applied Physics Letters,* vol. 106, p. 223504, 2015.

(5) Kobayashi, E.; Watabe, Y.; Hao, R. and Ravi, T. S. "Heterojunction solar cells with 23% efficiency on n-type epitaxial kerfless silicon wafers," *Progress in Photovoltaics: Research and Applications,* vol. 24, pp. 1295-1303, 2016.

(6) Kutsukake, K. "Growth of Crystalline Silicon for Solar Cells: Mono-Like Method," in *Handbook of Photovoltaic Silicon*, D. Yang, Ed., ed Berlin, Heidelberg: Springer Berlin Heidelberg, 2018, pp. 1-20.

(7) Stoddard, N.; Wu, B.; Witting, I.; Wagener, M. C.; Park, Y.; Rozgonyi, G. A. and Clark, R., "Casting single crystal silicon: novel defect profiles from BP Solar's mono2 ™ wafers," in *Solid State Phenomena*, 2008, pp. 1-8.

(8) Stoddard, N.; Sidhu, R.; Creager, J.; Dey, S.; Kinsey, B.; Maisano, L.; Phillips, C.; Clark, R.; Zahler, J. and Xie, X., "Evaluating BP Solar's Mono 2™ material: Lifetime and cell electrical data," in *Photovoltaic Specialists Conference (PVSC), 2009 34th IEEE*, 2009, pp. 001163-001168.

(9) ITRPV, "International Technology Roadmap for Photovoltaic (ITRPV), 2018 Results,10th Edition, https://itrpv.vdma.org/," 2019.

(10) Lan, C. W.;. Lan, W. C.; Lee, T. F.; Yu, A.; Yang, Y. M.; Hsu, W. C. Hsu. B. and Yang, A., "Grain control in directional solidification of photovoltaic silicon," *Journal of Crystal Growth,* vol. 360, pp. 68-75, 2012/12/01/ 2012.

(11) Yang, Y. M.; Yu, A.;. Hsu, B; Hsu, W. C.;. Yang, A; and Lan, C. W. "Development of high-performance multicrystalline silicon for photovoltaic industry," *Progress in Photovoltaics: Research and Applications,* vol. 23, pp. 340-351, 2015.

(12) Lan, C. W.; Lan, A.; Yang, C. F.;. Hsu, H. P; Yang, M.; Yu, A.; Hsu, B.; Hsu, W. C. and Yang, A.,"The emergence of high-performance multi-crystalline silicon in photovoltaics," *Journal of Crystal Growth,* vol. 468, pp. 17-23, 2017/06/15/ 2017.

(13) Autruffe, A.; M'hamdi, M.; Schindler, F.; Heinz, F. D.; Ekstrøm, K. E.; Schubert, M. C. Di Sabatino, M. and Stokkan, G., "High performance multicrystalline silicon: Grain structure and iron precipitation," *Journal of Applied Physics,* vol. 122, p. 135103, 2017.

(14) Lan, C.-w.; Hsu, C. and Nakajima, K.; "Multicrystalline Silicon Crystal Growth for Photovoltaic Applications," in *Handbook of Crystal Growth: Bulk Crystal Growth*, ed: Elsevier, 2015, pp. 373-411.
(15) Gu, X.; Yu, X.; Guo, K.; Chen, L. Wang, D. and Yang, D. "Seed-assisted cast quasi-single crystalline silicon for photovoltaic application: Towards high efficiency and low cost silicon solar cells," *Solar Energy Materials and Solar Cells,* vol. 101, pp. 95-101, 6// 2012.
(16) Jouini, A.; Ponthenier, D.; Lignier, H. Enjalbert, N. Marie, B.; Drevet, B.; Pihan, E.; Cayron, C.; Lafford, T. and Camel, D., "Improved multicrystalline silicon ingot crystal quality through seed growth for high efficiency solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 20, pp. 735-746, 2012.
(17) Marie, B.; Bailly, S.; Jouini, A.; Ponthenier, D.; Plassat, N. Dubost, L.; Pihan, E.; Enjalbert, N.; Garandet, J.P and Camel, D., "Seeded grown mono-like Si ingots: effect on recombination activity of dislocations," in *Proceedings 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany*, 2011, pp. 1910-1914.
(18) Guerrero, I.; Parra, V.; Carballo, T.; Black, A.; Miranda, M.; Cancillo, D.; Moralejo, B.; Jiménez, J.; Lelièvre, J. and Del Cañizo, C., "About the origin of low wafer performance and crystal defect generation on seed-cast growth of industrial mono-like silicon ingots," *Progress in Photovoltaics: Research and Applications,* vol. 22, pp. 923-932, 2014.
(19) Ervik, T.; Stokkan, G.; Buonassisi, T.; Mjøs, Ø. and Lohne, O. "Dislocation formation in seeds for quasi-monocrystalline silicon for solar cells," *Acta Materialia,* vol. 67, pp. 199-206, 2014.
(20) Trempa, M.; Reimann, C.; Friedrich, J.; Müller, G.; Krause, A.; Sylla, L. and , Richter, T., "Defect formation induced by seed-joints during directional solidification of quasi-mono-crystalline silicon ingots," *Journal of Crystal Growth,* vol. 405, pp. 131-141, 2014.
(21) Wu, Y. C.;Lan, A.; Yang, C. F.; Hsu, C. W;. Lu, C. M.; Yang, A. and Lan, C. W., "Effect of Seed Arrangements on the Quality of n-Type Monolike Silicon Grown by Directional Solidification," *Crystal Growth & Design,* vol. 16, pp. 6641-6647, 2016/11/02 2016.
(22) Hu, D. Yuan, S. L. He, S. Chen, H. Wan, Y.; Yu, X. and Yang, D., "Higher quality mono-like cast silicon with induced grain boundaries," *Solar Energy Materials and Solar Cells,* vol. 140, pp. 121-125, 9// 2015.
(23) Lan, C. Y.; Wu, Y. C.; Lan, A.; Yang, C. F;. Hsu, C.; Lu, C. M. Yang, A. and Lan C. W., "Control of ingot quality and solar cell appearance of cast mono-like silicon by using seed partitions," *Journal of Crystal Growth,* vol. 475, pp. 136-143, 2017/10/01/ 2017.
(24) Kutsukake, K.; Usami, N.; Ohno, Y.; Tokumoto, Y.; and Yonenaga, I. "Mono-Like Silicon Growth Using Functional Grain Boundaries to Limit Area of Multicrystalline Grains," *IEEE Journal of Photovoltaics,* vol. 4, pp. 84-87, 2014.
(25) Jay, F.; Muñoz, D.; Desrues, T.; Pihan, E.; Amaral de Oliveira, V.; Enjalbert, N. and Jouini, A., "Advanced process for n-type mono-like silicon a-Si:H/c-Si heterojunction solar cells with 21.5% efficiency," *Solar Energy Materials and Solar Cells,* vol. 130, pp. 690-695, 2014.
(26) Wenham, A.; Song, L.; Abbott, M.; Zafirovska, I.; Wang, S.; Hallam, B.; Chan, C.; Barnett, A. and Wenham, S., "Defect passivation on cast-mono crystalline screen-printed cells," *Frontiers in Energy,* vol. 11, pp. 60-66, 2017.

(27) CanadianSolar, "http://investors.canadiansolar.com/news-releases/news-release-details/canadian-solar-set-world-record-2228-multi-crystalline-cell, accessed on 29 May 2019," 2019.
(28) Green, M.A.; *Silicon Solar Cells: Advanced Principles & Practice*: Centre for Photovoltaic Devices and Systems, University of New South Wales, 1995.
(29) Hallam, B.; Chen, D.; Kim, M.; Stefani, B.; Hoex, B.; Abbott, M. and Wenham, S., "The role of hydrogenation and gettering in enhancing the efficiency of next-generation Si solar cells: An industrial perspective," *physica status solidi (a),* vol. 214, p. 1700305, 2017.
(30) Buonassisi,T.; Istratov, A.A.; Marcus, M.A.; Lai, B.; Cai, Z.; Heald, S.M and Weber, E.R., "Engineering metal-impurity nanodefects for low-cost solar cells," *Nat Mater,* vol. 4, pp. 676-9, Sep 2005.
(31) Fenning, D. P.; Zuschlag, A. S.; Bertoni, M. I.; Lai, B.; Hahn, G.; and Buonassisi, T.; "Improved iron gettering of contaminated multicrystalline silicon by high-temperature phosphorus diffusion," *Journal of Applied Physics,* vol. 113, p. 214504, 2013.
(32) Schmidt, J.; and Bothe, K.; "Structure and transformation of the metastable boron- and oxygen-related defect center in crystalline silicon," *Physical Review B,* vol. 69, 2004.
(33) Martinuzzi, S.; Palais,O.; Pasquinelli; M.; Barakel; D.; and Ferrazza; F.; "N-type multicrystalline silicon wafers for solar cells," in *Conference Record of the Thirty-first IEEE Photovoltaic Specialists Conference, 2005.*, 2005, pp. 919-922.
(34) Macdonald, D.; and Geerligs, L. J.; "Recombination activity of interstitial iron and other transition metal point defects in p- and n-type crystalline silicon," *Applied Physics Letters,* vol. 85, p. 4061, 2004.
(35) Friedrich, J.; Von Ammon, W.; and Müller, G.; "Czochralski Growth of Silicon Crystals," in *Handbook of Crystal Growth (Second Edition)*, P. Rudolph, Ed., ed Boston: Elsevier, 2015, pp. 45-104.
(36) Kurinec, S. K.; Bopp, C.; and Xu, H.; "Emergence of Continuous Czochralski (CCZ) Growth for Monocrystalline Silicon Photovoltaics," in *Emerging Photovoltaic Materials*, S. K. Kurinec, Ed., ed, 2018.
(37) Davis, J. R.; Rohatgi, A.; Hopkins, R. H.; Blais, P. D.; Rai-Choudhury, P.; McCormick, J. R.and Mollenkopf, H. C., "Impurities in silicon solar cells," *IEEE Transactions on Electron Devices,* vol. 27, pp. 677-687, 1980.
(38) Peiner, E.; Schlachetzki, A.; and Krüger, D.; "Doping profile analysis in Si by electrochemical capacitance-voltage measurements," *Journal of the Electrochemical Society,* vol. 142, pp. 576-580, 1995.
(39) Bock, R.; Altermatt, P. P.; and Schmidt, J.; "Accurate extraction of doping profiles from electrochemical capacitance voltage measurements," in *Proc. 23rd Eur. Photovolt. Sol. Energy Conf. Exhib., Valencia, Spain*, 2008, pp. 1510-1513.
(40) Sinton, R. A.; and Cuevas, A.; "Contactless determination of current–voltage characteristics and minority carrier lifetimes in semiconductors from quasi steady state photoconductance data," *Applied Physics Letters,* vol. 69, pp. 2510-2512, 1996.
(41) Istratov, A. A.; and Weber, E. R; "Electrical properties and recombination activity of copper, nickel and cobalt in silicon," *Applied Physics A,* vol. 66, pp. 123-136, February 01 1998.

(42) Fenning, D. P.; Hofstetter, J.; Bertoni, M. I; Coletti, G.; Lai, B.; del Cañizo, C.and Buonassisi, T., "Precipitated iron: A limit on gettering efficacy in multicrystalline silicon," *Journal of Applied Physics,* vol. 113, p. 044521, 2013.
(43) Inglese, A.; Lindroos, J.; Vahlman, H.; and Savin, H.; "Recombination activity of light-activated copper defects in p-type silicon studied by injection- and temperature-dependent lifetime spectroscopy," *Journal of Applied Physics,* vol. 120, p. 125703, 2016.
(44) Schmidt, J.; Lim, B.; Walter, D.; Bothe, K.; Gatz, S.; Dullweber, T and Altermatt, P. P., "Impurity-Related Limitations of Next-Generation Industrial Silicon Solar Cells," *IEEE Journal of Photovoltaics,* vol. 3, pp. 114-118, 2013.
(45) Morishige, A. E.; "Metal impurities in n-type crystalline silicon for photovoltaics: Simulation, synchrotron-based characterization, and mitigation," Massachusetts Institute of Technology, 2016.
(46) Trupke, T.; Bardos, R. A.; Schubert, M. C.; and Warta, W.; "Photoluminescence imaging of silicon wafers," *Applied Physics Letters,* vol. 89, p. 044107, 2006.
(47) Trupke, T.; Mitchell, B.; Weber, J. W.; McMillan, W.; Bardos, R. A.; and Kroeze, R.; "Photoluminescence Imaging for Photovoltaic Applications," *Energy Procedia,* vol. 15, pp. 135-146, 2012/01/01/ 2012.
(48) Ryningen, B.; Stokkan, G.; Kivambe, M.M.; Ervik, T.; and Lohne, O.; "Growth of dislocation clusters during directional solidification of multicrystalline silicon ingots," *Acta Materialia,* vol. 59, pp. 7703-7710, 2011.
(49) Lan, C.W.; Yang, C.F.; Lan, A.; Yang, M.; Yu; A.; Hsu, H.P.Hsu, B and Hsu, C., "Engineering silicon crystals for photovoltaics," *CrystEngComm,* vol. 18, pp. 1474-1485, 2016.
(50) Liu, Z.; Vähänissi, V.; Laine, H.S.; Lindeberg, M.; Yli-Koski; M.; and Savin; H.; "Electronic Quality Improvement of Highly Defective Quasi-Mono Silicon Material by Phosphorus Diffusion Gettering," *Advanced Electronic Materials,* vol. 3, pp. 1600435-n/a, 2017.
(51) Morishige, A.E.; Jensen, M.A.; Hofstetter, J.; Yen, P.X.T.; Wang, C.; Lai; B. Fenning, D. P. and Buonassisi, T., "Synchrotron-based investigation of transition-metal getterability in n-type multicrystalline silicon," *Applied Physics Letters,* vol. 108, p. 202104, 2016.
(52) Haschke, J.; Kivambe, M.M.; Horzel, J.; Monnard, R.; Barraud, L.; Descoeudres, A Debrot, F.; Abdallah, A.; Aïssa, B.; Tabet, N; Despeisse M.; Boccard M and Ballif, C., "Silicon Heterojunction Solar Cells on Quasi-mono Wafers," in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC) (A Joint Conference of 45th IEEE PVSC, 28th PVSEC & 34th EU PVSEC)*, 2018, pp. 314-316.

TOC GRAPHICS