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Gate-Tunable Tunneling Transistor Based on a Thin Black Phosphorus−$SnSe_2$ Heterostructure

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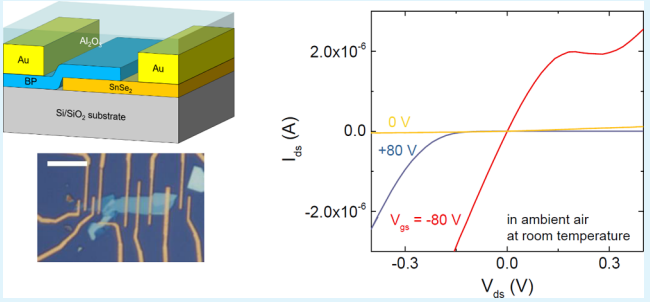
Supporting Information

ABSTRACT: Tunneling field-effect transistors (TFETs) are of considerable interest owing to their capability of low-power operation. Here, we demonstrate a novel type of TFET which is composed of a thin black phosphorus−tin diselenide (BP−$SnSe_2$) heterostructure. This combination of 2D semiconductor thin sheets enables device operation either as an Esaki diode featuring negative differential resistance (NDR) in the negative gate voltage regime or as a backward diode in the positive gate bias regime. Such tuning possibility is imparted by the fact that only the carrier concentration in the BP component can be effectively modulated by electrostatic gating, while the relatively high carrier concentration in the $SnSe_2$ sheet renders it insensitive against gating. Scanning photocurrent microscopy maps indicate the presence of a staggered (type II) band alignment at the heterojunction. The temperature-dependent NDR behavior of the devices is explainable by an additional series resistance contribution from the individual BP and $SnSe_2$ sheets connected in series. Moreover, the backward rectification behavior can be consistently described by the thermionic emission theory, pointing toward the gating-induced formation of a potential barrier at the heterojunction. It furthermore turned out that for effective Esaki diode operation, care has to be taken to avoid the formation of positive charges trapped in the alumina passivation layer.



KEYWORDS: *negative differential resistance, tunneling transistor, black phosphorus, tin diselenide, 2D van der Waals heterostructure*

INTRODUCTION

Modern electronic applications require integrated circuits of substantially reduced dynamic and static power consumption. However, the ultimate device scaling of conventional metal−oxide field-effect transistors faces its limits. As an alternative, tunneling field-effect transistors (TFETs) are receiving increasing attention in particular because of their potential low-power operation.[1−3] Recent research on TFETs has focused on p−n homo- and heterojunctions based on Si, Ge, and III−V materials.[4−8] In general, the device performance of heterojunction-based TFETs has been proven to be superior to that of homojunction-based TFETs, as the former typically exhibits a steep band edge at the junction and furthermore allows selecting high mobility channel materials.[1,9] However, further progress along this direction is slowed down by the significant lattice mismatch that often occurs in heterojunctions.

Promising candidates for overcoming the lattice mismatch problem are two-dimensional (2D) van der Waals (vdW) materials which lack dangling bonds on their surface.[10−12] In addition, the great diversity of available 2D vdW materials enables efficient tailoring of the device properties of TFETs.[13] However, the realization of high-performance TFETs is still challenging due to the low current density and device stability as limiting factors in particular for vertical TFETs.[14] Another relevant goal is to achieve an efficient and reliable gate-tuning capability of the devices. To this end, a promising device component is the 2D vdW material black phosphorus (BP) which features a high carrier mobility in comparison to most transition-metal dichalcogenides such as MoS_2.[15−19] One suitable counterpart to BP is the 2D vdW semiconductor tin diselenide ($SnSe_2$), which displays a relatively high electron affinity as one of the prerequisites for high device performance of TFETs.[20−24] In both its bulk and few-layer forms, $SnSe_2$ is (unintentionally) highly n-doped, thereby rendering it difficult to deplete charge carriers by electrostatic gating.[20,25,26] By contrast, BP is only slightly p-doped, such that its carriers can be readily tuned by electrostatic gating and/or dielectric passivation in case of the few-layer form.[17,27,28] Thus far, BP−$SnSe_2$ heterostructure diodes displaying negative differential resistance (NDR) behavior have only been realized in the bulk form.[29]

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Here, we demonstrate that stacking of a gate-tunable thin BP sheet onto a thin $SnSe_2$ sheet of high carrier density provides access to vertical TFETs whose operation can be tuned via electrostatic gating between a NDR and a backward diode mode, which at the same time exhibit a NDR peak current of unprecedented magnitude. Furthermore, by combining temperature-dependent charge transport experiments with scanning photocurrent microscopy (SPCM), we are able to unravel the presence of a gate-tunable type II staggered band alignment at the BP−$SnSe_2$ heterojunction.

RESULTS AND DISCUSSION

In Figure 1a, three subsequent stages of device fabrication are shown, starting with a mechanically exfoliated $SnSe_2$ sheet (top panel), the same $SnSe_2$ sheet after deterministic transfer of a BP sheet on top (middle panel), and the final BP−$SnSe_2$ heterostructure device with metal electrodes and a Al_2O_3 passivation deposited on top (bottom panel). The passivation layer is needed to preserve the original structure and electronic properties of the BP and $SnSe_2$ sheets, as both slowly degrade in ambient air.[28,30] In general, the exposure of the BP and $SnSe_2$ sheets to ambient air was limited to several minutes before final device passivation. As determined by atomic force microscopy (AFM), the thickness of the BP and $SnSe_2$ sheet is ∼8.5 and ∼12 nm, respectively (Figure S1). Details of the device fabrication process are provided in the Methods section. The BP−$SnSe_2$ heterostructure device is schematically illustrated in Figure 1b. The corresponding output curves recorded under ambient conditions at different gate voltages (−80, 0, and +80 V), shown in Figure 1c, signify a global back-gating effect on the device. The output curve at V_{gs} = −80 V (red line) clearly features NDR, which is indicative of band-to-band tunneling. In comparison, application of the opposite gate bias (V_{gs} = +80 V) resulted in a strongly different behavior, which is characteristic of a backward diode (blue line). More I_{ds}−V_{ds} and I_{ds}−V_{gs} data at different gate voltages and drain−source voltages are offered in the Supporting Information. Hysteresis induced by charge trapping/detrapping at the trap sites between the heterostructure and gate oxide are observed in Figure S2, but this could not affect the main result associated with the heterojunction.

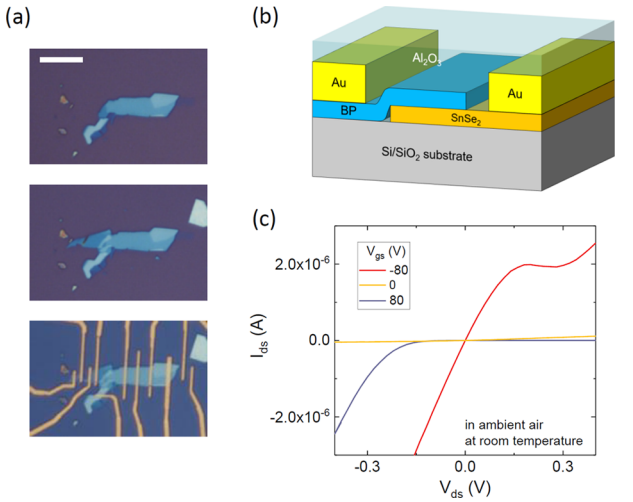

Figure 1. (a) Optical images showing the fabrication of a heterostructure device, starting from a thin $SnSe_2$ sheet (top), followed by deterministic transfer of a thin BP sheet on top (middle), then defining electrodes by e-beam lithography and metal evaporation, and finally deposition of an alumina layer by ALD (bottom). The scale bar is 10 μm. (b) Schematic illustration of a finished thin BP−$SnSe_2$ heterostructure device. (c) Output characteristics of the device at V_{gs} = −80, 0, and +80 V, recorded under ambient conditions.

To determine the type of band alignment at the BP−$SnSe_2$ heterojunction, we used SPCM. This technique involves raster scanning of the sample through a confocal laser spot, while the photocurrent is recorded as a function of illumination position.[31] In Figure 2a, three SPCM maps of the device in Figure 1, obtained using different gate voltages, are displayed. At zero drain-source and gate voltage (middle panel of Figure 2a), a negative photocurrent of approximately −17 nA is observed near the BP−$SnSe_2$ heterojunction, pointing toward an energy band bending of type II (staggered), as shown in the corresponding diagram of Figure 2b. The formation of a tunneling barrier between the two types of layers (represented by the two vertical black lines) is most likely due to native oxide layers and/or organic residues from the mechanical transfer process. That the band alignment is indeed of type II (staggered) rather than type III (broken-gap) and is further supported by the negative photocurrent observed at zero bias in the output curves (plot in the middle of Figure 2c). By contrast, in close correspondence to a previous report on a bulk BP−$SnSe_2$ heterojunction,[29] we observed NDR behavior and positive photocurrent for a bulk BP−$SnSe_2$ heterojunction device, implying type III (broken-gap) band alignment in this case (see the Supporting Information for further details). First of all, this difference between the bulk and few-layer heterostructure likely originates from a thickness-dependent carrier density of BP, that is, a decreased doping concentration with decreasing BP thickness.[32] In the device comprising bulk BP, while the high carrier concentration principally favors the TFET operation, the resulting poor gate controllability is a significant drawback. Another plausible explanation of the difference between the bulk and few-layer heterostructure is possible fixed charges in the tunneling barrier. Note that in a III−V heterostructure the band alignment change induced by the fixed charges at the heterojunction has been reported.[33]

Owing to the weak p-type doping of the thin BP sheet, the SPCM response is influenced by the applied back-gate voltage, as apparent from the photocurrent maps at the top and bottom of Figure 2a. Under zero drain−source voltage and application of V_{gs} = −40 V (top map), an increased negative photocurrent emerges near the heterojunction in the SPCM map. Such behavior indicates an upward energy band bending of the BP induced by the highly p-doped BP channel, as illustrated by the top diagram in Figure 2b. Under this condition, NDR behavior is observed in the forward bias regime of the output curve (top panel of Figure 2c). That only the BP channel part is tunable by the gate is confirmed by the observation that the heavily n-doped $SnSe_2$ channel, in contrast to the BP, cannot be turned off by the gate voltage (see Figure S4 in the Supporting Information). The electron concentration in the $SnSe_2$ sheet can be estimated from the simple equation, $n = \sigma/(\mu q)$, where n, σ, μ, and q are carrier concentration, conductivity, carrier mobility, and electronic charge, respectively. Thus, using the field-effect mobility in the $SnSe_2$ sheet extracted from the transfer curve, as described in the Supporting Information, an electron concentration on the order of 10^{13} cm^{-2} is obtained at zero gate voltage. Such high electron concentration is indeed expected to hinder effective gating. Correspondingly, when a positive gate bias of V_{gs} = +40 V is applied, a strong positive photocurrent at the heterojunction appears (see bottom panel of Figure 2a), which is consistent

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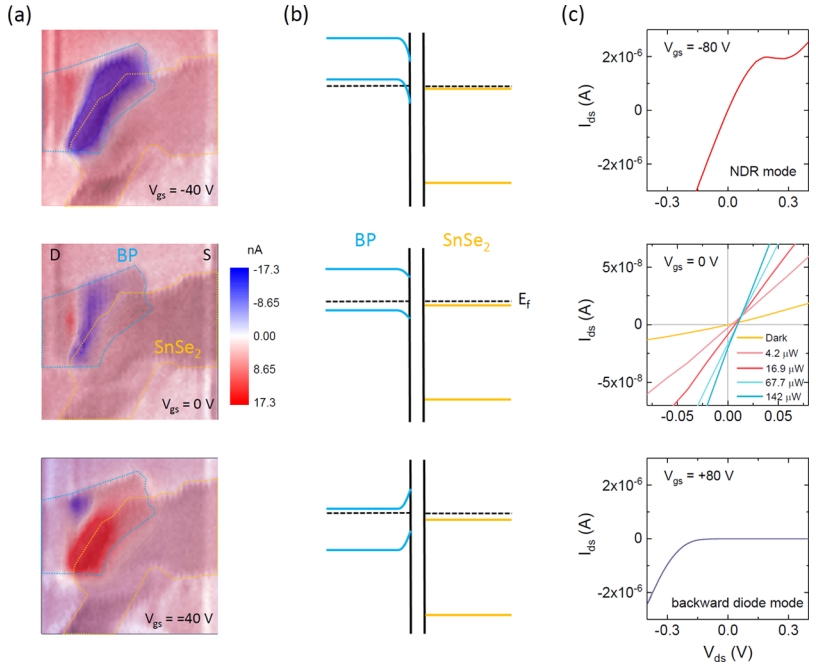

Figure 2. (a) SPCM maps of the BP−$SnSe_2$ heterostructure device in Figure 1, acquired at room temperature with λ = 514 nm. The maps were recorded at V_{ds} = 0 V and V_{gs} = −40 (top), 0 (middle), and +40 V (bottom). In each case, the corresponding optical image of the device is overlaid. The blue and yellow dotted lines mark the contours of the BP and $SnSe_2$ sheet, while "D" and "S" denote the drain and source electrode, respectively. The size of each SPCM map is 7 μm × 7 μm. (b) Band diagrams corresponding to the gating conditions in panel (a). (c) Measured output characteristics at high negative gate voltage (top), zero gate voltage (middle), and high positive gate voltage (bottom). E_f denotes the Fermi level position. For the zero gate voltage case (middle plot), I_{ds}−V_{ds} curves were acquired in the dark and under illumination with different laser powers of 4.2, 16.9, 67.7, and 142 μW, respectively.

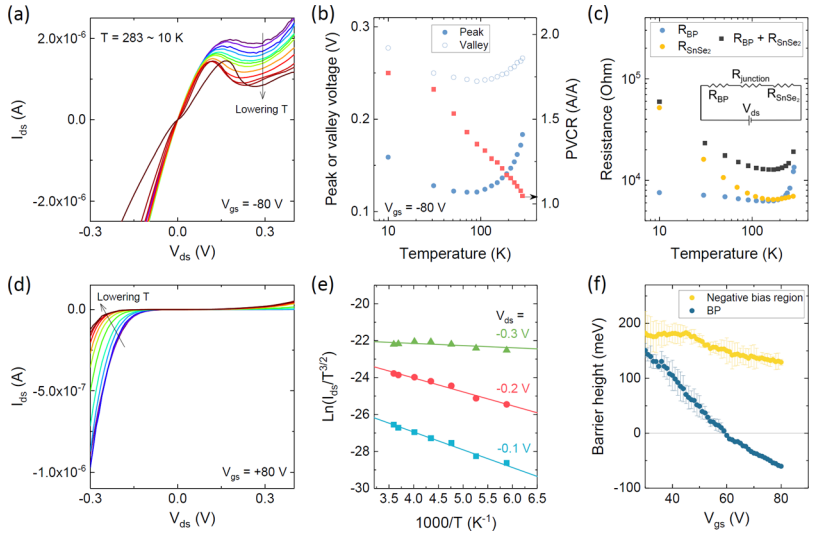

Figure 3. Temperature-dependent characteristics of the BP−$SnSe_2$ heterostructure device. (a) I_{ds}−V_{ds} curves at V_{gs} = −80 V, recorded at various temperatures between 283 and 10 K. (b) Peak/valley voltages and PVCR as a function of temperature, as extracted from the NDR features in panel (a). (c) Two-probe resistances of the BP (R_{BP}) and $SnSe_2$ (R_{SnSe_2}) sheets and their sum (R_{BP} + R_{SnSe_2}) as a function of temperature. The inset shows a simplified equivalent circuit of the device, comprising R_{BP}, R_{SnSe_2}, and a resistance at the BP−$SnSe_2$ junction ($R_{junction}$). (d) I_{ds}−V_{ds} curves at V_{gs} = +80 V for various temperatures between 283 and 10 K [analogous to panel (a)]. (e) Arrhenius plots of $\ln(I_{ds}/T^{3/2})$ vs $1000/T$, at V_{gs} = +80 V and in the negative bias regime (V_{ds} = −0.1, −0.2, and −0.3 V). The straight lines represent linear fits. (f) Extracted Schottky barrier heights for the BP−$SnSe_2$ heterostructure device in the negative bias regime and the BP device, both as a function of gate voltage.

with the resulting downward band bending in the BP channel, as depicted in the bottom diagram in Figure 2b. Under this condition, a conventional Schottky barrier is formed near the heterojunction, which in turn is responsible for the backward diode behavior (bottom plot of Figure 2c).

To evaluate the mechanism of charge transport across the BP−$SnSe_2$ p−n heterojunction, we performed temperature-dependent electrical measurements at high negative and positive gate voltages. The behavior in the NDR regime at V_{gs} = −80 V is shown in Figure 3a for the temperature range between 10 and

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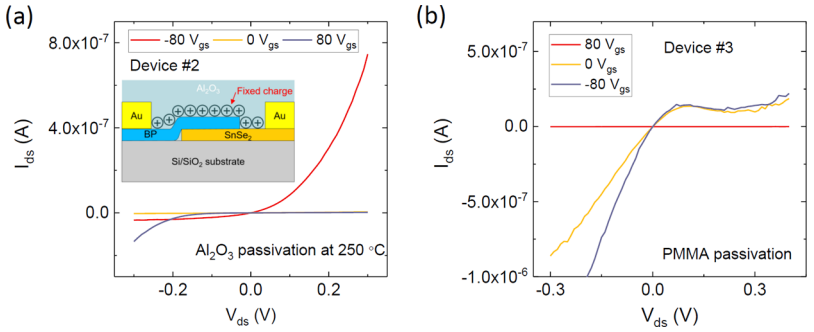

Figure 4. Effect of the nature of the passivation layer in the BP−$SnSe_2$ heterostructure devices. Output characteristics for the case of (a) an Al_2O_3 passivation layer deposited at 250 °C and (b) a PMMA passivation layer, in both cases for V_{gs} = −80, 0, and +80 V, respectively. The inset in panel (a) shows a schematic diagram of the device, with fixed charges in the Al_2O_3 passivation layer.

283 K. It is apparent that the peak current decreases upon cooling, which is unexpected at first sight because of the reduced tail of the Fermi−Dirac distribution function.[29,34] This temperature dependence of the peak current may be explained by a sizable excess current associated with a two-step process involving Shockley−Read−Hall (SRH) generation/recombination and trap-assisted tunneling.[35,36] It is noteworthy that for other materials such a decrease has been attributed to an increase of the energy band gap with decreasing temperature.[37,38] However, the present BP displays an anomalous temperature dependence of the band gap,[39] thus favoring the aforementioned alternative explanation.

The corresponding peak and valley voltages, along with the peak-to-valley current ratio (PVCR), are plotted in Figure 3b as a function of temperature. One plausible explanation for the observed overall trend of the peak and valley voltage positions is the contribution of a series resistance comprising an intrinsic and a contact-related component for each of the two sheets. To test this hypothesis, we measured the individual sheets' two-probe resistance with the aid of additional electrodes as shown at the bottom of Figure 1a (see the Supporting Information for more details). In Figure 3c, thus obtained temperature-dependent resistances (blue and yellow data points, respectively) are plotted together with their sum (black data points) at V_{gs} = −80 V. Based on the equivalent circuit in the inset of Figure 3c and assumption that the resistance of the heterojunction ($R_{junction}$) is insensitive to temperature at low drain−source bias (because the carrier injection is mostly the band-to-band tunneling process), the temperature dependence of the effective voltage drop across the heterojunction should be dominated by the temperature dependence of the series resistance. The decrease of both peak and valley voltages upon cooling from 300 to ∼100 K, as observed in Figure 3b, can then be attributed to the decrease of the series resistance within this temperature range. The subsequent increase of the peak/valley voltage upon further cooling below ∼100 K is consistent with the increase of the series resistance in this range. Likewise, the increase of PVCR with decreasing temperature, reaching ∼1.75 at 10 K (Figure 3b), can be related to the reduced excess current at lower temperatures. In general, the relatively small PVCR magnitude indicates considerable excess current, similar to other tunneling devices.[37,40] It may be possible to reduce the latter through mechanical transfer of the sheets under inert atmosphere, to ensure a cleaner interface.

For the backward diode operation regime at V_{gs} = +80 V, the temperature-dependent I_{ds}−V_{ds} curves are shown in Figure 3d. The current decrease in the negative bias regime upon cooling should be, according the bottom band diagram in Figure 2b, attributable to the forward bias regime of a Schottky diode. To confirm this assumption, we analyzed the data in the framework of classical thermionic emission theory (see the Supporting Information).[41,42] The Arrhenius plots of $\ln(I_{ds}/T^{3/2})$ as a function of T^{-1}, shown in Figure 3e, are linear for the three drain−source voltages of −0.1, −0.2, and −0.3 V. The extracted Schottky barrier height is plotted as a function of gate voltage in Figure 3f, along with the value for the individual BP sheet. The Schottky barrier height determined for the heterostructure is positive over the entire gate voltage regime, with a reasonable value on the order of 150 meV. This observation confirms the validity of the thermionic emission theory for the heterojunction in the negative bias regime. On the other hand, the appearance of a negative Schottky barrier height for the BP device above V_{gs} = +60 V shows that the thermionic emission theory is invalid in the high gate voltage regime.[42]

A major parameter governing the device performance of TFETs is the subthreshold slope (SS). A comparison between the SS of the present devices and values previously reported for other 2D material-based TFETs can be found in Table S1, which includes also further device parameters. Although in the hole regime, the SS of the present heterostructure devices falls below that of the BP-only device (see Figure S8), it remains above ∼4000 mV/dec. These relatively large values can be attributed to the thick gate insulator (300 nm SiO_2), along with a sizable trap density at the interface between the 2D sheets and gate insulator, which determine the SS according to the equation SS = $(1 + C_{it}/C_{ox}) \times k \times T/q \times \ln 10$, where C_{it}, C_{ox}, k, T, and q are the interface trap capacitance, gate oxide capacitance, Boltzmann constant, temperature, and electronic charge, respectively. One option to further decrease the SS would be to implement an ultrathin, high-κ gate insulator with a high quality interface to the 2D sheets.

As a further observation of practical relevance, because of the small thickness of the BP and $SnSe_2$ sheets, the electrical behavior of the heterostructure devices is influenced by the nature of the passivation layer. Figure 4a shows gate-dependent I_{ds}−V_{ds} curves of another BP−$SnSe_2$ heterostructure (device #2, see the Supporting Information for details), whose Al_2O_3 passivation layer was grown at the higher temperature of 250 °C. In contrast to the above described device (Figure 1) with the Al_2O_3 passivation layer grown at 100 °C, no NDR behavior is observed in the present device, as apparent from Figure 4a. The Ohmic-like I_{ds}−V_{ds} curves, that are obtained by separate measurements on the BP and $SnSe_2$ sheets (see the Supporting Information), indicate that the non-Ohmic behavior detected

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for the heterostructure arises due to the heterojunction. One possible reason for the absence of NDR is that positive fixed charges induced by oxygen vacancies in the Al_2O_3 layer (as depicted in the figure inset) hinder back gating, especially close to the heterojunction. In fact, it has been documented that sizeable oxygen vacancy densities can be induced with increasing growth temperature of the Al_2O_3 layer, which could in turn result in a larger density of fixed positive charge.[43,44] In comparison, when a PMMA layer is used for passivation, NDR behavior is again observed in the negative gate voltage regime (see Figure 4b), like for the device with the Al_2O_3 layer grown at 100 °C. This finding is in accord with the absence of fixed surface charges on PMMA, underlining the importance of properly choosing the passivation layer and its fabrication conditions.

CONCLUSIONS

In summary, we have successfully fabricated thin BP−$SnSe_2$ p−n heterostructure devices whose operation mode is tunable by electrostatic gating between the NDR and backward diode regime. This tuning is enabled by the fact that application of a global back-gate predominantly affects the thin BP sheet because if its lower charge carrier density in comparison to the $SnSe_2$ sheets. Based on spatially resolved photocurrent data, we conclude that the band alignment at the heterojunction is of type II staggered. Furthermore, temperature-dependent electrical measurements on the devices revealed that the charge transport across the heterojunction occurs via a two-step process involving SRH generation/recombination and trap-assisted tunneling in the high negative gate voltage regime, and via thermionic emission in the high positive gate voltage regime. In addition, growth of the required Al_2O_3 passivation layer at elevated temperature was found to suppress the NDR behavior, presumably because of fixed positive charges introduced at the interface. Taken together, our observations provide several clues for the further improvement of 2D vdW material-based tunneling devices.

METHODS

The thin $SnSe_2$ and BP sheets were mechanically exfoliated from bulk crystals by the Scotch tape method onto n^+-doped silicon substrates deposited with a thermally grown, 300 nm thick SiO_2 layer and onto PDMS-based gel (Gel-Pak), respectively.[45] A carefully selected BP sheet on the PDMS-based gel was transferred by a deterministic transfer method onto the $SnSe_2$ sheet on the Si/SiO_2 substrate. Contact electrodes were patterned by standard e-beam lithography, followed by an in situ Ar plasma treatment, thermal evaporation of the Ti/Au (2 nm/70 nm), and lift-off process. Atomic layer deposition (ALD) (Cambridge Nanotech ALD system) was performed with $Al(CH_3)_3$ and H_2O as precursors at 100 or 250 °C and a base pressure of 10 mTorr, to obtain a 20 nm thick Al_2O_3 passivation layer. Alternatively, a 200 nm thick PMMA bilayer was spin-coated on the heterostructure.

AFM was used to determine the thickness of the sheets. The electrical transport and photocurrent measurements in Figures 1, 2, and 4 were carried out under ambient conditions. The temperature-dependent charge transport experiments were performed inside an Oxford cryostat. All of the electrical measurements were performed in dc configuration using two Keithley 2400 source meters and a Keithley 2000 multimeter. A confocal microscope (Leica TCS SP2, 50× objective lens with NA = 0.8) was used for the SPCM experiments, in which the samples were raster-scanned (lateral step size of ∼100 nm) through the approximately 500 nm wide laser spot (linearly polarized light with λ = 514 nm).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.9b02589.

Thickness information of the BP−$SnSe_2$ heterostructure, double-sweep output and transfer characteristics, electrical properties of the individual BP and $SnSe_2$ devices, and so forth (PDF)

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Notes

The authors declare no competing financial interest.

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