On the Dynamic Performance of Laterally-Gated Transistors

Mohammad Samizadeh Nikoo, Giovanni Santoruvo, Catherine Erine, Armin Jafari, and Elison Matioli

***Abstract*—Laterally-gated transistors have been proposed as an innovative device architecture in which a semiconducting channel is controlled by side gates. In this sense, the gate can either be in contact with the sidewalls or be separated by a gap. In the latter case, the relatively large transconductance together with the small gate capacitance offers a promising potential for future RF devices. The DC performance of these transistors has been studied in the literature, however, there is a lack of investigation on their dynamic performance. Here we show that the channel control in a laterally-gated transistor with gate-channel separation can come from either the gate electric field or the trapped carriers in the surface or bulk. The latter effect results in very slow time responses. We also show that trap states can be more dominant in degrading the dynamic performance of these devices than in planar-gate transistors. The measurement method employed in this letter can be used to determine whether the control is from the gate electric-field or trapped carriers. This study aims to clarify the related studies in the literature, and opens a way to understand and optimize and laterally-gated transistors.**

***Index Terms*—HEMTs, GaN, laterally-gated, dynamic performance, trapped carriers.**

I. Introduction

CONTROLING a two-dimensional electron gas (2DEG) channel by lateral gates instead of a top gate, offers promising prospects for improving the device performance [1]. For instance, side-gate depletion makes it possible to control a multi-channel 2DEG formed by a stack of heterostructures, resulting in a considerable improvement in current capability [2], [3]. Figures 1a, 1b, and 1c show three potential implementations of laterally-gated high electron mobility transistors (HEMTs). The side gate depletion in the structure shown in Figure 1a reduces the OFF current and subthreshold slope [4]-[6]. One can remove the top gate and use just the side-gates to control the channel (Figure 1b). Tri-gates [7] and super-lattice castellated field-effect transistors (SLCFETs) [8] are examples of Figure 1a, and buried dual gates (BRIDGE) [9] is example of Figure 1b. In Figure 1c, a laterally-gated transistor with a gate-channel separation is shown. This architecture could lead to a considerable reduction in the gate capacitance, while presenting a relatively large transconductance [10]. This shows the potential of these devices to operate at very high-frequencies. In-plane-gate transistors are examples of this type of devices [10]-[13],

The authors are with the Power and Wide-band-gap Electronics Research Laboratory (POWERlab), École polytechnique fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland (e-mail: elison.matioli@epfl.ch).

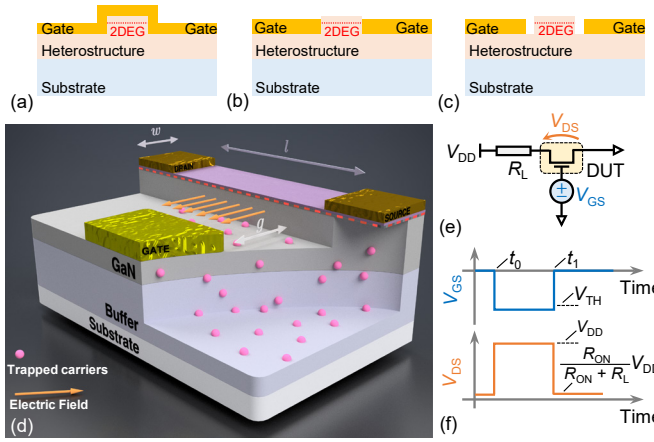

Fig. 1. Cross section of laterally-gated transistors, where (a) gate covers the channel, (b) gate is in contact with the side-wall, and (c) there is gate-channel separation. (d) The 3D view of a laterally-gated transistor with gate-channel separation. The gate can be formed by metal or by 2DEG. (e) Circuit model of the experimental set-up together with the (f) ideal switching waveforms.

where the 2DEG itself serves as the gate. Based on an estimation of the gate capacitance and the DC transconductance measurements, a cutoff frequency of 10 THz has been predicted [11]. In fact, DC characterization and capacitance measurement of laterally-gated transistors with gate-channel separation were the subjects of several reports [13]-[18], however, there is a lack of investigation on the RF and dynamic performance of these devices. Time-domain measurements of laterally-gated transistors with a gate-channel separation, designed for logic applications, have been reported in the literature, although the time scales are either in the range of 10 s [19]-[21], or presented in arbitrary units [22], [23]. The lack of report on the dynamic performance is also present in RF devices. Although SLCFETs and BRIDGE transistors have been fully characterized in RF [8], [9], the potentially outstanding RF performance of laterally-gated transistors with gate-channel separation has not been shown.

There is clearly a lack of investigation on the limiting factors hindering the dynamic performance of these laterally-gated devices. Here, we demonstrate that the channel control in these transistors can come from trapped carriers, in which the devices may present normal transistor behavior under DC characterization, with a large transconductance, however, with a very slow time response. The measurement technique used in this study allows to separately measure the control from the gate electric-field and from the trapped carriers. We also discuss that the degradation in dynamic performance, as a general issue in planar HEMTs, can be more serious in laterally-gated transistors with gate-channel separation.

II. Experimental Discussion

Figure 1d illustrates a 3D view of an AlGaN/GaN laterally-gated transistor with its cross section. The channel width, channel length, and gate-to-channel distance of the device are represented by w, l, and g, respectively. The lateral gate modulates the channel carrier density through the gate electric-field, however trapped carriers can potentially affect the channel conductivity, as well. The schematic of the circuit model and measurement set-up are shown in Figure 1e. The ideal switching waveforms of the transistor are shown in Figure 1f. For $t < t_0$, the device is ON, which results in a voltage drop of $V_{DD}R_{ON}/(R_{ON} + R_L)$ over drain-source ports (where R_L and R_{ON} are the load and transistor ON-state resistances, respectively). At $t = t_0$, a negative pulse is applied to the gate to switch OFF the transistor. Then, at $t = t_1$, the gate voltage is switched back to zero to turn ON the device. We studied the dynamic performance of devices with different dimensions based on AlGaN/GaN epitaxy with no passivation, on different substrates: Si, SiC, and Sapphire. In all of the devices, the distance from the epitaxial surface to the 2DEG was about 23 nm and the mesa isolation etching depth was 200 nm. We present the comparison of single gate transistors, however, double gate devices have shown similar behavior. We employed R_L = 100 kΩ for all of the experiments.

Figure 2a shows the transfer characteristics of a transistor with w = 150 nm, l = 250 nm, and g = 60 nm on a SiC substrate, showing a threshold voltage of −6.2 V. The output characteristics and switching waveforms of this device are shown in Figures 2b and 2c, respectively. For t < 3 ms, the gate was grounded and the transistor was ON with R_{ON} = 3.5 kΩ (Figure 2d). The gate signal (V_{GS} = −7 V) was applied to turn OFF the device at t = 3 ms. Based on the DC measured transfer characteristics, the device should be completely turned OFF by this gate signal. However, although there is a fast transition in the drain voltage, the device is not completely switched OFF at this moment. There is another slower transition that switches OFF the transistor at around t = 5 ms, [17], [24]. The device maintains its OFF state till t = 8 ms which comes from trapped carriers, not the gate electric-field when the gate is grounded. The ON resistance is considerably degraded to 700 kΩ showing another evidence that there are many trapped carriers either in the surface or in the bulk. The comparison of this switching waveform with the one measured for a planar HEMT (Figure 2c) shows that the channel control in these transistors comes from a combination of gate electric-field (fast response) and trapped carriers (slow response).

The degradation of the dynamic ON resistance is a general issue in planar transistors [25] and diodes [26], and can be even more serious in laterally-gated transistors. For instance, at the relatively small drain voltage of 5 V, there is 200 times R_{ON} degradation, as shown in Figure 2d. While the gate control in a laterally-gated device with zero gate-channel separation can be quite strong and the devices are less sensitive to traps [9], by increasing the gate-channel distance to decrease the input capacitance, the relative influence of trapped carriers becomes potentially more dominant on the channel.

Figure 3a shows the measured DC transfer characteristics of laterally-gated transistor on sapphire substrate with a 60-nm-wide channel and 80-nm gate-to-channel separation, showing a threshold voltage of −8 V. The output characteristics of the device is shown in Figure 3b. The switching waveforms of the transistor with different pulse amplitudes applied to the gate reveal both the fast field-effect and slow trap-assisted controls (Figure 3c). Figure 3d illustrates the device switching waveforms with smaller time scale to focus on the field-effect transition, showing a field-effect threshold voltage of −10 V. However, Figure 3c shows that the threshold voltage from trap-assisted switching is in agreement with that from DC measurement as the device reaches OFF-state with V_{GS} of −8 V, 1 ms after the gate signal. The magnitude of the DC-measured threshold voltage of the device is smaller than the field-effect threshold voltage, illustrating the effect of trapped carriers in depleting the channel. The observed rise time of ~ 2

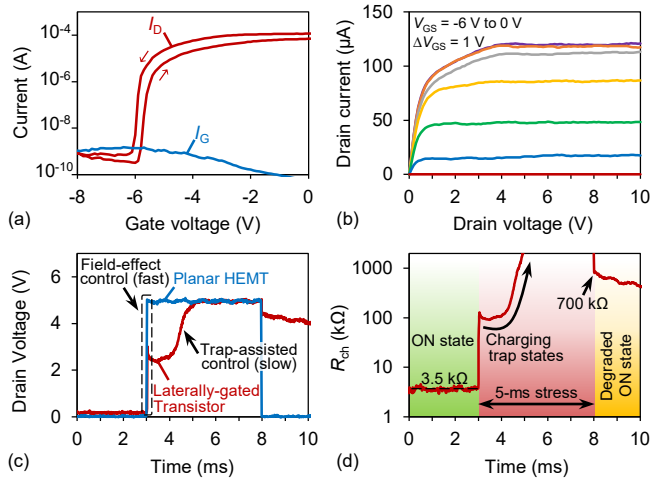

Fig. 2. (a) Double sweep transfer and (b) output characteristics of a 150-nm-wide 250-nm-long channel laterally-gated transistor with 60-nm gate-channel seperation on SiC substrate. (c) Voltage switching waveforms of the laterally-gated transistor and a planar HEMT as a reference. (d) The channel resistance of the laterally-gated transistor.

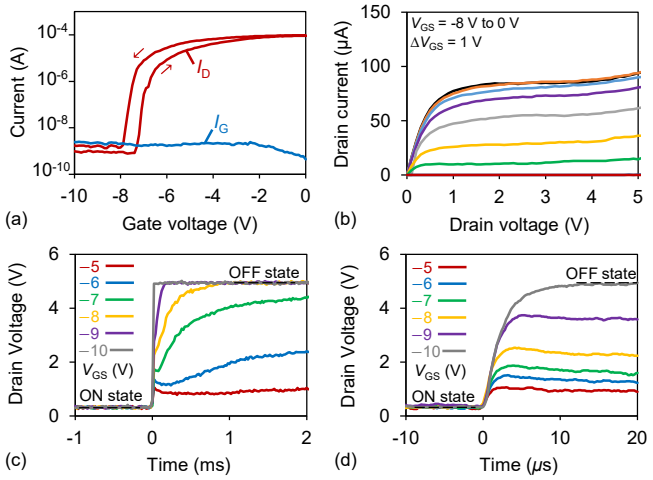

Fig. 3. (a) Double sweep transfer and (b) output characteristics of a 60-nm-wide channel laterally-gated transistor with 80-nm gate-channel seperation on sapphire substrate. (c) Switching waveforms of the device with different gate voltage levels. (b) The zoomed-in waveforms to show the field-effect control.

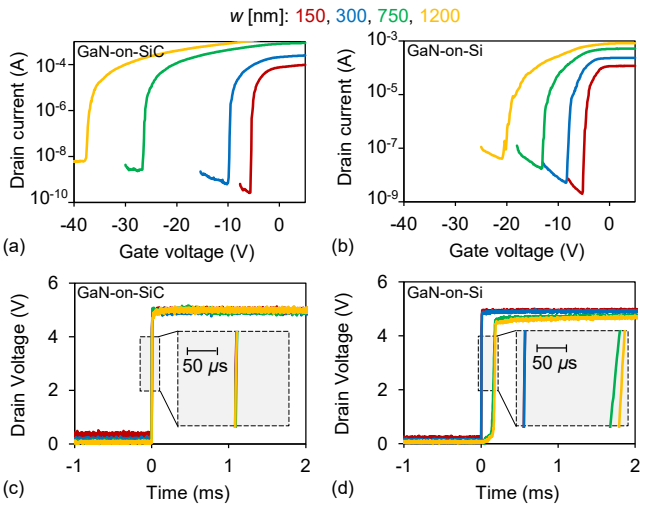

Fig. 4. Effect of substrate on the functionality of laterally-gated transistors. Transfer characterisitcs of 250-nm-long channel devices with gate-channel distance of 80 nm and different channel widths on (a) SiC and (b) HR Si substrates. The switching waveforms of the laterally-gated devices on (c) SiC and (d) HR Si susbstrates.

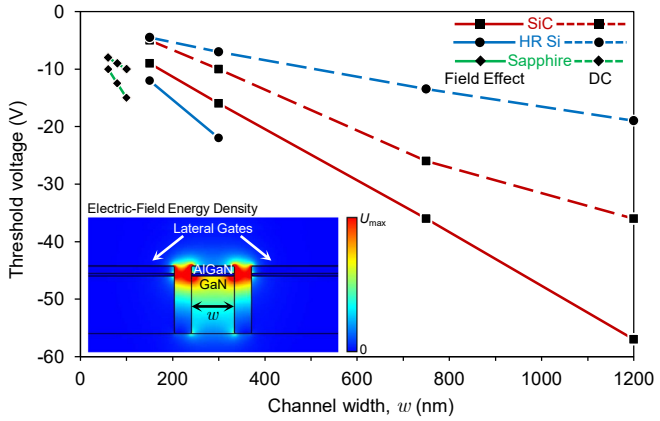

Fig. 5. Field-effect and trap-assisted threshold voltages of devices with different channel widths on SiC, HR Si, and Sapphire substrates. The inset illustrates the device cross section, where the electric-field energy density shows the field-effect control in latterally-gated transistor.

μs from the switching waveforms shown in Figure 3d are due the parasitics of connections in our measurement set-up, and the same rise time was observed for a reference planar HEMT.

Figures 4a and 4b present the measured DC transfer characteristics of transistors with different channel widths on SiC and HR Si substrates, respectively. As expected, devices with wider channels have more negative threshold voltages. The time-domain switching behaviors of the transistors on SiC and Si substrates are shown in Figures 4c and 4d, respectively. The fast transitions in the inset of Figure 4c reveals that all the transistors on SiC substrate could be switched OFF with the gate electric field. The applied voltages to the gate were V_G = −9, −16, −36, and −57 V for devices with w = 150, 300, 750, and 1200 nm, respectively. Figure 4d, however, shows the fast electric-field control just for the devices with w = 150 and 300 nm, for which V_G = −12 and −22 V were applied, respectively. Larger devices with w = 750 nm and 1200 nm presented a delay between the application of the gate signal (with V_G = −30 and −56 V, respectively) and the switching OFF of the device, corresponding to a slow channel control which is from trapped carriers. The devices could not be switched OFF with a fast transition, even by applying more negative voltages to the gate, until the device breakdown.

These results show that the conductivity of the substrate has a strong effect on performance of laterally-gated transistors. Substrates like Si or even high-resistivity (HR) Si [27], act as a ground plane and may suppress the lateral gate electric field in large gate-channel distances. Taking into account the dimensions of the device (w and g) with the substrate-channel distance d, for small-scale devices when w and g are much smaller than d, the effect of substrate ground plane is not dominant. However, for large-scale devices, one should apply much larger gate voltage to switch OFF the device with the gate electric field. This voltage can be larger than the gate breakdown voltage, hindering the use of the device as a field-effect transistor. Another important point is the smaller magnitude of measured DC threshold voltages in GaN-on-Si devices, than those on SiC substrate. This shows the potential of Si substrate to charge buffer traps [27] which helps the device to be switched OFF at a less negative gate voltage.

Figure 5 shows the DC and field-effect threshold voltages (from switching measurements) of devices with different channel widths, fabricated on three different epitaxies, showing the field-effect threshold voltage is always larger than the measured DC threshold voltage, however, the difference is much smaller for small-scale devices on insulating substrates. For example, this difference is only of 10% in 60-nm-wide channel devices on sapphire substrate showing that the gate electric field is more dominant in this case (inset of Figure 5). In contrast, large scale devices especially those on HR Si substrate display a relatively small DC threshold voltage that seems promising at first glance, however, their slow time responses drastically limit their applications. In this sense, the larger DC transconductance measured in large-scale laterally-gated transistors may not necessarily reflect a promising RF performance, thus requiring a more careful analysis. On the other hand, employing small-scale devices with small threshold voltage and large normalized transconductance, together with proper scaling-up methods, could result in promising RF performances.

III. Conclusion

We studied the dynamic performance of laterally-gated transistors with gate-channel separation. We demonstrated that the channel control in these devices can come from either gate electric-field or trapped carriers. Our results suggest that the DC characterization of these transistors, especially in wide-channel devices on conductive substrates could lead to a wrong estimation of their performance in RF or switching regimes. Thus a careful investigation of the dynamic performance of the devices is necessary. We compared the measured threshold voltage from DC and dynamic tests of the devices. The minor difference between these threshold voltages for small-scale devices, especially those on insulating substrate, show the more effective lateral gate control in these transistors. It was demonstrated that large-scale laterally-gated transistors can be considerably more sensitive to the traps.

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