Polarity-Controllable Devices and Circuits for Doping-Free 2D Electronics

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Love with your heart,
use your head for everything else.

— Alan Melikdjanian
a.k.a. Captain Disillusion

To my Family... To my Friends... To Mish.

Acknowledgements

It is a common conception that scientists suffer for their art. Like many such impressions, there is some truth behind this one also. Several studies conducted by academic institutions as well as by independent organizations have found that a high percentage of PhD students are at risk of developing depression. While it is difficult to make conclusive claims, and conditions vary considerably between different universities, some of the statistics reported are alarming at best. I was recently reading that a 2014 study at University of California, Berkeley (see http://go.nature.com/2HwlL4v) found that up to 47% of PhD students (out of the 790 in the survey) met the criteria to be classified as depressed. A Nature survey in 2017 (see go.nature.com/2kzo89o) showed that among the 1574 students that participated 45% had sought professional help for anxiety or depression caused by their PhD studies.

I then started to think about my own experiences in research and reflect on how fortunate I have been over the course of my PhD at LSI. Like any PhD student, I have gone through some stressful times, and I realize that it is mainly thanks to the people that have been around me that they never got the better of me.

First, I wish to thank my advisor Prof. Giovanni De Micheli (Nanni) and my co-advisor Prof. Pierre-Emmanuel Gaillardon for their guidance and support during this PhD thesis. While the current mentality in the research world often puts the need to publish ahead of the quality of the scientific work, I always felt that both Nanni and Pierre-Emmanuel focused on the soundness and cohesiveness of my research and never pressured me to over-publish. They always made me feel appreciated and respected, both as a person and a scientist. I still remember one of the first conversations I had with Nanni when he said that his hope for his PhD students is that they become more successful that he has been (quite a hard task!).

A special thanks goes to Prof. Francky Catthoor, Dr. Iuliana Radu and Dr. Dennis Lin for supporting my PhD at IMEC and for all their invaluable feedback throughout my research. I extend my gratitude to the members of my oral committee Prof. M.A. Ionescu and Prof A. Kis from EPFL, and Prof S. Mitra from Stanford.

EPFL is a great place to do a PhD, and these 4 years spent at LSI have been

amazing. I want to thank for the bottom of my heart Eleonora, Francesca C., Francesca S., Giulia, Ivan, Nadja, Aya and all the other members of the LSI lab. We have always been supportive to each other, shared the joy for each other achievements as you do in a family and not in a competitive work environment. These guys always made the office feel like another home, a place where you are happy to go every morning. More than just coworkers, they have become lifelong friends. I will always hold dear the memories of our years together! I also want to acknowledge few friends that stopped by the lab for a little while, bringing fresh energy and enthusiasm. Diego, Marcello, Eleonora, Matilda, Kate, Lucia, Sofia and Simone, it was such a pleasure meeting all of you. I would also not forget about Peanut, one of the newest addition to my life, who aside from bringing much joy, has made the lab slightly less safe on many Fridays (sorry Nanni!). A special thanks goes to Christina and Carole for their invaluable help in the daily life of the LSI lab.

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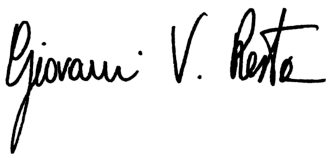
Last, but surely not least, Mish, my partner in life. No obstacle is too big with you on my side. Thank you.

April 26, 2019



Abstract

The growth of information technology in recent decades has been sustained by the miniaturization of *Complementary Metal-Oxide-Semiconductor* (CMOS) *Field-Effect Transistors* (FETs), with the number of devices per unit area constantly increasing, as exemplified by Moore's law. Modern digital *Integrated Circuits* (ICs) contain billions of transistors and logic gates, fabricated with CMOS technology. As scaling of conventional silicon-based electronics is reaching its ultimate limit, considerable effort has been devoted to find new materials and new device concepts that could ultimately outperform standard silicon transistors. Among the materials that are studied for charge-based devices, *Two-Dimensional* (2D) materials of the *Transition Metal Di-Chalcogenides* (TMDCs) family show promising opportunities, thanks to their electrical and physical properties. In order to enable 2D electronics to be integrated in the *Back-End-Of-the-Line* (BEOL) with conventional CMOS it is essential to achieve complementary operation of the transistors, in order to benefit from the low standby power consumption enabled by CMOS logic. In CMOS, silicon is physically doped during the fabrication process with ion implantation to create unipolar devices with Ohmic contacts. Ion implantation requires high temperature annealing to repair damages in the silicon and achieve proper dopant activation, and this high temperature process is not compatible with the process for monolithic 3D CMOS, which requires a low thermal budget. Physical doping, through ion-implantation, of 2D material has not proven to be successful due to extreme thinness of the 2D semiconductors. The possibility of introducing dopant atoms during growth of the 2D material has been reported, but lacks selectivity and does not allow for any control of the doping profile. Several chemical and molecular doping techniques have been developed, but are often non-stable and non-CMOS compatible. A device concept that does not rely on any physical or chemical doping, and use instead un-doped materials, would be of great interest in this regard.

In this thesis, we report the first experimental demonstration of a doping-free, polarity-controllable device fabricated on few-layer *tungsten di-selenide* (WSe_2). We show how modulation of the Schottky barriers at drain and source by a separate gate, named polarity gate, can enable the selection of the carriers injected in the channel, and achieve controllable polarity behaviour with ON/OFF current ratios $> 10^6$ for both electrons

and holes conduction. Following this demonstration, we fabricate and characterize a variety of polarity-controllable logic gates such as *Inverter* (INV), *NOT-AND* (NAND), *NOT-OR* (NOR), that are the building primitives used in the logic synthesis frameworks for conventional CMOS logic. Moreover, we experimentally show *2-Input Exclusive OR* (XOR-2), *3-Input Exclusive OR* (XOR-3) and *Majority* (MAJ) gates that, thanks to the polarity-controllable devices, can be realized with fewer transistors as compared to what is achievable in conventional CMOS. We demonstrate a complete standard cell library with the possibility of fabricating compact, highly-expressive logic gates that can be exploited to gain advantages at circuit level, using XOR and MAJ functions as logic primitives. Moreover, for the first time, we study scaling trends and evaluate the performances of polarity-controllable devices realized with undoped mono- and bi-layer 2D materials. Using ballistic self-consistent quantum simulations, combined with TCAD simulations, it is shown that, with the suitable channel material, such polarity-controllable technology can scale down to sub-10 nm gate lengths, while showing performances comparable to the ones of unipolar, physically-doped 2D electronic devices.

Keywords: nanotechnology, scaling, CMOS, beyond-CMOS, novel materials, 2D semiconductors, transition-metal-dichalcogenides, WSe_2, doping-free, electrostatic-doping, Schottky-barrier, polarity-control, 2D logic gates, fabrication, testing, simulations.

Sommario

La crescita della tecnologia dell'informazione nei decenni passati è stata resa possibile dalla miniaturizzazione dei transistor *Complementary Metal-Oxide-Semiconductor* (CMOS), con il numero di dispositivi per unità di area che ha continuato a raddoppiare ogni circa 2 anni, come predetto dalla legge di Moore. I circuiti integrati moderni contengono miliardi di transistor e porte logiche, fabbricati in tecnologia CMOS. La miniaturizzazione dei tradizionali dispositivi basati sul silicio sta raggiungendo i suoi limiti, e nella comunità scientifica vi è un notevole interesse nello scoprire nuovi materiali e nuovi tipi di dispositivi che potrebbero dimostrare prestazioni superiori ai transistor in silicio. Tra i nuovi materiali che sono studiati come canale semiconduttore per dispositivi a base di carica elettrica, i materiali *Two-Dimensional* (2D) della famiglia dei *Transition Metal Di-Chalcogenides* (TMDCs) sono tra i più promettenti, grazie alle loro proprietà elettriche e fisiche.

Nella tecnologia CMOS, il silicio viene drogato tramite impiantazione ionica durante la fabbricazione, per creare dispositivi unipolari con contatti omici. L'impiantazione ionica richiede però alte temperature di tempratura, necessarie per riparare i danni provocati alla struttura cristallina del silicio e per attivare gli atomi droganti. Queste alte temperature non sono compatibili con i processi di integrazione monolitica per 3D CMOS, che richiedono un budget di temperatura basso, per non danneggiare i dispositvi già construiti. Inoltre con le lunghezze dei canali che si avvicinano ai 20 nm, l'impiantazione ionica è diventata sempre più difficile da controllare. L' impiantazione ionica non si è dimostrata possibile per i materiali 2D, ed altre tecniche di doping che utilizzano drogaggio chimico o molecolare sono state sviluppate. Tutavia queste tecniche risultano essere non stabili e non sono compatibili con i processi CMOS tradizionali, non permettendo quindi l'integrazione dei dispositivi nel *Back-End-Of-the-Line* (BEOL). Un dispositivo che non richieda alcuna impiantazione ionica o drogaggio chimico, e si basi su materiali non drogati sarebbe di grande interesse in questo campo.

In questa tesi, presentiamo la prima dimostrazione sperimentale di un dispositivo senza drogaggio fisico o chimico, la cui polarità può essere controllata dinamicamente, realizzato su *tungsten di-selenide* (WSe_2). Dimostriamo come la modulazione delle barriere Schottky presenti ai contatti di source e drain da parte di un terminale aggiuntivo,

chiamato terminale di polarità, permetta di selezionare i di portatori di carica (elettroni o lacune) che vengono iniettati nel canale. Grazie a questa struttura, otteniamo il controllo della polarità del dispositivo, con un rapporto tra corrente di ON e OFF $> 10^6$ sia per la conduzione di elettroni che di lacune, sullo stesso dispositivo. I dispositivi con controllo della polarità realizzati su WSe_2 permettono di realizzare porte logiche compatte, in grado di aumentare la densità computazionale dell'elettronica 2D. Riportiamo sulla fabbricazione e caratterizzazione di una varietà di porte logiche fabbricate con transistor a controllo di polarità, come *Inverter* (INV), *NOT-AND* (NAND), *NOT-OR* (NOR) che sono i blocchi fondamentali usati per la sintesi di funzioni logiche in CMOS. Inoltre, dimostriamo sperimentalmente porte XOR a 2 ingressi, XOR a 3 ingressi e porte di maggioranza a 3 ingressi, che possono essere realizzate con un numero di transistor minore rispetto a quanto possibile in logica CMOS tradizionale. Per la prima volta, studiamo l'andamento delle prestazioni dei dispositivi a controllo di polarità realizzati su 1 o 2 layer di WSe_2, rispetto alla loro miniaturizzazione. Usando delle simulazioni quantistiche balistiche e autoconsistenti dimostriamo come, con il materiale di canale appropriato, i dispositivi a controllo di polarità possano essere miniaturizzati sino a lunghezze di canale di 5 nm, mantenendo prestazioni comparabili a quelle dei dispositivi unipolari, realizzati su materiali 2D drogati fisicamente.

Parole Chiave: nanotecnologie, miniaturizzazione, CMOS, oltre CMOS, nuovi materiali, semiconduttori 2D, transition-metal-dichalcogenides, WSe_2, assenza di drogaggio, drogaggio elettrostatico, barriere Schottky, controllo di polarità, porte logiche 2D, fabbricazione, misure, simulazioni.

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List of Acronyms

GND	*Ground*
I_{OFF}	*OFF-current*
I_{ON}	*ON-current*
V_{DD}	*Supply Voltage*
V_{TH}	*Threshold Voltage*
ϕ_{SB}	*Schottky-barrier height*
1L	*Mono-Layer*
2D	*Two-Dimensional*
2L	*Bi-Layer*
3D	*Three-Dimensional*
AFM	*Atomic Force Microscope*
Al_2O_3	*aluminium oxide*
ALD	*Atomic Layer Deposition*
Ar	*argon*
As	*arsenic*
Au	*gold*
BCB	*Beyond-CMOS Benchmark*
BEOL	*Back-End-Of-the-Line*
BJT	*Bipolar-Junction Transistor*
BTBT	*Band-to-Band Tunneling*

CG . . . . . *Control Gate*

CMOS . . . . . *Complementary Metal-Oxide-Semiconductor*

CMP . . . . . *Chemical Mechanical Polishing*

CNTs . . . . . *Carbon Nano-Tubes*

CVD . . . . . *Chemical Vapor Deposition*

D_{it} . . . . . *Interface-Trap Density*

DAC . . . . . *Design Automation Conference*

DCM . . . . . *di-chloro-methane*

DG . . . . . *Double-Gate*

DIBL . . . . . *Drain-Induced Barrier Lowering*

DIG . . . . . *Double-Independent-Gate*

DOS . . . . . *Density Of States*

DTCO . . . . . *Design Technology Co-Optimization*

EDLT . . . . . *Electric Double-Layer Transistors*

EDP . . . . . *Energy-Delay Product*

EDX . . . . . *Energy-Disperse X-ray*

EOT . . . . . *Equivalent Oxide Thickness*

EUV . . . . . *Extreme Ultra-Violet*

FEOL . . . . . *Front-End-Of-the-Line*

FET . . . . . *Field-Effect Transistor*

FETs . . . . . *Field-Effect Transistors*

FO4 . . . . . *Fan-Out of 4*

GAA . . . . . *Gate-All-Around*

H_2O . . . . . *water*

Hf . . . . . *hafnium*

HfO_2 . . . . . *hafnium di-oxide*

HRTEM . . . . . *High-Resolution Trasmission Electron Microscope*

ICs . . . . . *Integrated Circuits*

INV . . . . . *Inverter*

IPA . . . . . *isopropyl alcohol*

LOR1A . . . . . *Lift-Off Resist 1A*

MAJ . . . . . *Majority*

MAJ-3 . . . . . *3-Input Majority*

MIBK . . . . . *methyl-isobutyl ketone*

MIG . . . . . *Multiple-Independent-Gate*

Mo . . . . . *molybdenum*

MOCVD . . . . . *Metal-Organic Chemical Vapor Deposition*

MoS_2 . . . . . *molybdenum di-sulphide*

$MoSe_2$ . . . . . *molybdenum di-selenide*

MOSFET . . . . . *Metal-Oxide-Semiconductor Field-Effect-Transistor*

$MoTe_2$ . . . . . *molybdenum di-telluride*

N_2 . . . . . *nitrogen*

NAND . . . . . *NOT-AND*

Nb . . . . . *niobium*

NCFETs . . . . . *Negative-Capacitance Field-Effect Transistors*

NEGF . . . . . *Non-Equilibrium Green Function*

NOR . . . . . *NOT-OR*

OPD5262 . . . . . *tetramethylammonium hydroxide*

P . . . . . *phosphorus*

Pd . . . . . *palladium*

PECVD . . . . . *Plasma-Enhanced Chemical Vapor Deposition*

PG . . . . . *Polarity Gate*

PMMA . . . . . *polymethyl methacrylate*

Pt . . . . . *platinum*

PTW . . . . . *Partner Technical Week*

Re . . . . . *rhenium*

RFET . . . . . *Reconfigurable FET*

S . . . . . *sulfur*

SB . . . . . *Schottky-Barrier*

SB-FETs . . . . . *Schottky-Barrier Field Effect Transistors*

SCE . . . . . *Short-Channel Effects*

SCS . . . . . *Semiconductor Characterization System*

Se . . . . . *selenium*

SEM . . . . . *Scanning Electron Microscope*

Si . . . . . *silicon*

SiO_2 . . . . . *silicon di-oxide*

SS . . . . . *Sub-threshold Slope*

STCO . . . . . *System Technology Co-Optimization*

Ta . . . . . *tantalum*

TB . . . . . *Tight-Binding*

TCAD . . . . . *Technology Computer-Aided Design*

Te . . . . . *tellurium*

TEMAZ . . . . . *tetrakis(ethylmethylamino)zirconium*

TFETs . . . . . *Tunnel Field-Effect Transistors*

TG . . . . . *Top-Gate*

Ti . . . . . *titanium*

TIG . . . . . *Triple-Independent-Gate*

TMA . . . . . *trimethylaluminium*

TMAH . . . . . *trimethylammonium hydroxide*

TMDCs . . . . . *Transition Metal Di-Chalcogenides*

TSMC . . . . . *Taiwan Semiconductor Manufacturing Company*

UL . . . . . *Under-Lap*

W . . . . . *tungsten*

WS_2 . . . . . *tungsten di-sulfide*

WSe_2 . . . . . *tungsten di-selenide*

XOR-2 . . . . . *2-Input Exclusive OR*

XOR-3 . . . . . *3-Input Exclusive OR*

ZrO_2 . . . . . *zirconium di-oxide*

1 Introduction

Se vogliamo che tutto rimanga com'è,
bisogna che tutto cambi.

— Il Gattopardo,
Giuseppe Tomasi di Lampedusa

Electronics is ubiquitous in our daily activities, pervades our lives and shapes the way we communicate and interact with the world. What we have experienced in the last 70 years, in terms of technological advances, is almost unprecedented in human history, and it has all been enabled by the invention and constant advances in the performances of *Integrated Circuits* (ICs). To understand the magnitude of this technological revolution we can consider what a modern IC would look like if it had to be realized with vacuum tubes, the technology that preceded the invention of the integrated circuit. A system like ENIAC, Electronic Numerical Integrator and Compute, built in 1945 by John Mauchly and J. Presper Eckert at Univeristy of Pennsylvania under commission of the US Army, consisted of 20000 vacuum tubes, occupied 167 m^2 and consumed 150 kW to work at a clock cycle of 200 µs. The cost (corrected to match 2018) was 7 million dollars. If we consider each vacuum tube as a transistor and scale up to the size of today systems we have that in order to fit 10 billion devices (as are today in our phones) we would need 83.5 km^2 and 75 GW of power at a whopping cost of 3.5 trillion dollars (as a reference the US GDP in 2017 was 19 trillion dollars, Manhattan occupies 59 km^2 and a nuclear power plant produces roughly 4 GW.

This is of course an extreme example, but such is the advancement that modern ICs have enabled and still providing nowadays. ICs have themselves seen a tremendous improvements in performances, with the computational power of a 20 years old supercomputer being now provided by the processor in our new phone. The increase in performances has been enabled by the constant miniaturization of modern transistor, with an exponential increase in the number of devices that fit in a die (as shown in Fig. 1.1). This trend was first predicted in 1965 by Intel co-founder Gordon Moore, who stated that the number of devices in integrated circuits would double every two year,

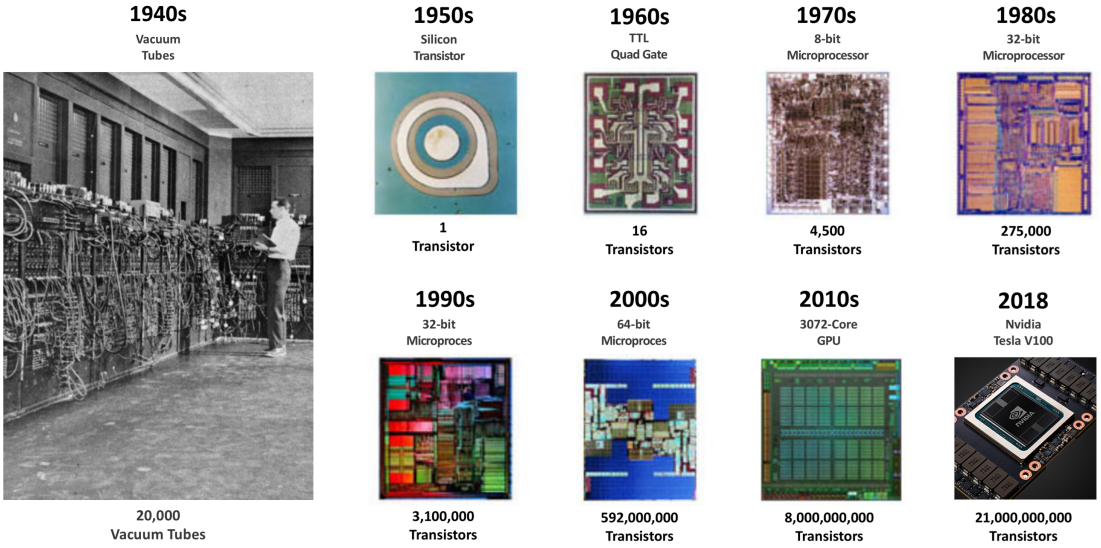


Figure 1.1 – Evolution of modern ICs and comparison with vacuum tube technology. Adapted from [1] and [2].

a prediction now commonly referred to as Moore's law [3]. In 1974 Robert Dennard formalized the guidelines that effectively enabled conventional geometrical scaling to stand until the early 2000s [4] (see Fig. 1.2). Dennard rules are based on the concept constant field scaling, *i.e.* reducing the critical dimension while keeping the electrical field constant yields higher speed and a reduced power consumption of a digital MOS device. Using a typical scaling factor of 0.7× per technology node, results in a doubling of transistor in a given area, with the power density remaining constant and the device and circuit speed inceasing by 1.4×. As stated by former Intel chief architect for the Pentium microprocessors Bob Colwell at the *Design Automation Conference* (DAC) in 2013 "*...Moore's law gives us more transistors...Dennard scaling made them useful*".

It is remarkable to appreciate that between 1975 and 2004, a time known as geometric scaling era, the core building block of modern ICs, the *Metal-Oxide-Semiconductor Field-Effect-Transistor* (MOSFET), remained virtually unchanged from his first experimental demonstration in 1959 at Bell lab by John Atalla and Dawon Khang. Until 2004, the miniaturization of devices had in fact been solely enabled by advancements in the lithographic process that allowed the definition of smaller features. It is equally staggering to realize that virtually every modern digital IC is based on *Complementary Metal-Oxide-Semiconductor* (CMOS) logic, that was originally developed by Frank Wanlass in 1963. Starting in 2005 with the 90 nm node technology boosters needed to be introduced, first at a material level, and then at a device level, in order to enable scaling to continue (equivalent (effective) scaling era in Fig. 1.2). These boosters include the use of strained Si and SiGe, the introduction of high-κ dielectric, metal gates and ultimately the development of the first 3D device structure (Fin-*Field-Effect Transistor* (FET)) at the 22 nm node. The next era of scaling (defined in Fig. 1.2 as hyper-scaling) will be

enabled by innovations at different technological level, starting from *Design Technology Co-Optimization* (DTCO) and up to *System Technology Co-Optimization* (STCO), where heterogeneous integration of functionally diverse integrated circuits and novel materials is envisioned. Using the words of Shekhar Borkar, former head of Intel's microprocessor technology research: "*Moore's law simply states that user value doubles every two years*", and in this form, the law will continue as long as the industry will be able to keep increasing the device functionality [5].

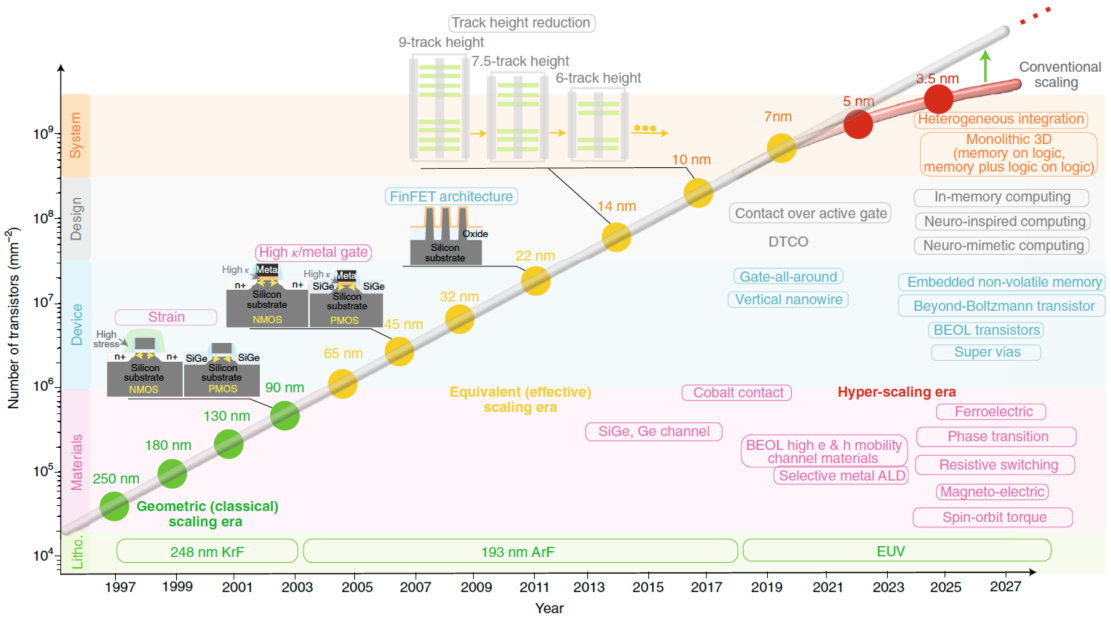


Figure 1.2 – Three eras of CMOS technology scaling. Past, present and future trend of transistor density scaling, depicting three distinct eras of scaling: geometric (or classical) scaling, equivalent (or effective) scaling, and hyper-scaling (or functional diversification). Proportional scaling of the various aspects of the transistor such as gate oxide, junctions, channel doping and physical gate length characterized the era of geometric scaling. The equivalent scaling era saw the introduction of unconventional materials such as silicon–germanium, hafnium-based high-κ dielectric and non-planar device structures such as FinFETs that scaled the effective mobility, the electrical gate oxide thickness and the effective transistor width, respectively. In the future, innovations in materials, devices with both logic and memory functions and heterogeneous integration technologies will enable the era of hyper-scaling in advanced electronics. Reproduced with permission from [6]. Copyright 2018 Springer Nature.

1.1 Thesis Motivation

The main motivation behind this thesis is the growing interest of the electronics industry and research institutions in novel device concepts and in new semiconducting materials for next-generation beyond-CMOS electronics. More specifically we are motivated by the

need to develop a device that could easily be monolithically integrated in the *Back-End-Of-the-Line* (BEOL) with conventional CMOS electronics. Dimensional scaling has been the main drive of the silicon industry in the last decades, with the exponential growth of information technology being sustained by the miniaturization of CMOS *Field-Effect Transistors* (FETs) [4], with the number of devices per unit area constantly increasing, as exemplified by Moore's law [3].

Nowadays, scaling of silicon devices is reaching its ultimate limit, as shown is Fig. 1.2, and the exploration of novel semiconducting materials, that could be heterogeneously integrated with silicon, is an open and exciting research field, with *Two-Dimensional* (2D) *Transition Metal Di-Chalcogenides* (TMDCs) materials being one of the key players in this field. In order to enable 2D electronics to be integrated with conventional CMOS it is essential to achieve complementary operation of the transistors, in order to benefit from the low standby power consumption enabled by CMOS logic. In CMOS, silicon is physically doped during the fabrication process with ion implantation to create unipolar devices with Ohmic contacts. The doping process irreversibly sets the polarity of the transistors (*n*- or *p*-type) according to the dopant ions implanted in the silicon substrate (*arsenic* (As) for electron and *phosphorus* (P)) for hole doping). With the physical gate length of modern devices approaching 10 nm, ion implantation has become increasingly more complicated to control [7] [8], and fluctuations in number of dopant atoms present in the transistor channel are responsible for an increased variability of the threshold voltage of the devices [8]. In addition, ion implantation requires high temperature annealing to repair damages in the silicon and achieve proper dopant activation [9] [10] and this high temperature step is not compatible with the process for monolithic 3D-CMOS, which requires a low thermal budget.

Physical doping, through ion-implantation, of 2D material has not proven to be successful due to extreme thinness of the 2D semiconductors, with ions just implanting in the substrate. The possibility of introducing dopant atoms during growth of the 2D material as been reported, but lacks selectivity and does not allow for any control of the doping profile [11–15]. Several chemical and molecular doping techniques have been developed, but are often non-stable and non CMOS compatible, thus not allowing integration of chemically-doped 2D devices in the BEOL [16–18]. A device concept that does not rely on any physical or chemical doping, and use un-doped materials, would be of great interest in this regard.

1.2 Novel Materials and Devices for Future Electronic Systems

Research on innovative device concepts and novel semiconducting materials has produced an amount of results that would be impossible to summarize in a brief section of this thesis. Here, we have selected few of the most exciting concepts, as a representative class for the plethora of solutions that have been proposed for beyond-CMOS scaling. In this

thesis we will focus on 2D-TMDCs, that are introduced in more depth in Ch. 2.

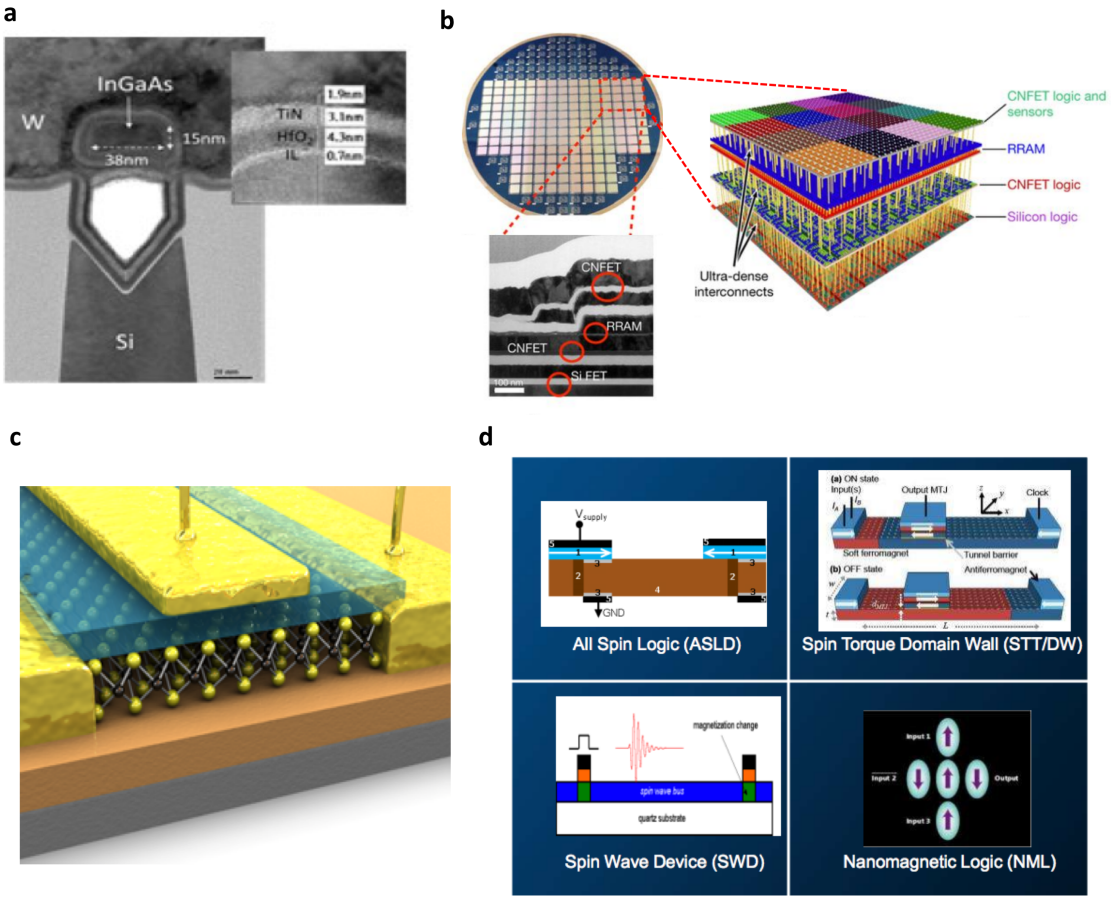


Figure 1.3 – Novel materials and new device concepts. **(a)** TEM image of an optimized high-mobility InGaAs device. Reproduced with permission from [19]. Copyright 2015 IEEE. **(b)** Experimental demonstartion of a 3D nanosystem integrating silicon and *Carbon Nano-Tubes* (CNTs) electronics with resistive memories and sensors. Adapted with permission from [20]. Copyright 2017 Springer Nature. **(c)** Schematic illustration of a monolayer 2D-FET. Reproduced with permission from [21]. Copyright 2011 Springer Nature. **(d)** Proposed spin and magnetic devices for non-charge-based devices. Adapted with permission from [22]. Copyright 2015 IEEE.

Near-term scaling The era of equivalent scaling (see Fig. 1.2) is expected to continue until around 2025, enabled by innovative DTCO efforts and novel devices structures such as *Gate-All-Around* (GAA) nanowires and vertical nanowires [6]. Moreover *Extreme Ultra-Violet* (EUV) lithography is expected to be used for the most critical layers to reduce multi-pattern process complexity while achieving aggressive die area scaling, as shown in Fig. 1.2. Industries such as *Taiwan Semiconductor Manufacturing Company* (TSMC) have already invested billion of dollars in the development of the 5 nm technology node, that is expected to reach the market in 2021.

Long-term scaling For long-term scaling there is no clear path yet. Industries and research institutions are currently looking at innovations in materials, devices with both logic and memory functions, devices with lower *Sub-threshold Slope* (SS), high-performance memories beyond static random-access memory (SRAM) and dynamic random-access memory (DRAM), monolithic 3D integration of logic and memory and heterogeneous integration technologies [6]. Here we focus on the novel materials and device concepts that could provide a successful scaling beyond 2025.

- III-V materials have been extensively studied for the fabrication of *Tunnel Field-Effect Transistors* (TFETs), but the field appears to have come to a hard stop since the effect of charge-impurities at the interface between epitaxially-grown III-V materials seems to not allow the achievement of steep SS. III-V materials (see Fig. 1.3d) are however still considered for conventional devices, especially for radio-frequency applications, thanks to the high mobility of charge carriers (in particular of holes). III-V materials are not currently considered for monolithic 3D and BEOL integration, given the high temperatures needed to grow the materials and the non-feasibility of a transfer process.

- CNTs have shown great potential both for polarity-controllable applications (see Chapter 3) as well as for standard CMOS-like devices, and are still to-date one of the most promising materials for long-term scaling ($>$ 10 years) thanks to their optimal electrostatic control, high mobility and considerable energy band-gap (see Fig. 1.3b). The recent demonstration of a 3D nanosystem that has multiple layers of CNTs logic and resistive memory and sensors stacked on a conventional CMOS die show the promise of such technology [20] (as shown in Fig. 1.4, CNTs are amongst the materials considered for BEOL integration).

- While CNTs and III-V semiconductors have been studied for over two decades the field of 2D semiconducting materials is relatively new, with the most seminal paper (the demonstartion of monolayer *molybdenum di-sulphide* (MoS_2) FETs by Radisavljevic *et al.* [21]) dating only to 2011 (see Fig. 1.3e). Despite the novelty of the field 2D materials have sparked high hopes and are being considered both for the fabrication of ultra-scaled CMOS-like devices, as well as for the realization of TFETs and *Negative-Capacitance Field-Effect Transistors* (NCFETs). Thanks to the possibility of low-temperature fabrication (see Ch. 2 for a more in depth discussion) 2D-TMDCs materials are amongst the candidates for the realization of molithically integrated BEOL transistors (as shown in 1.4).

- A completely disruptive scaling alternative would be to transition to non-charge-based electronics and use spin-, magnetic- or plasmonic-logic (see Fig. 1.3g). The selling point of such devices is the possibility of ultra-low-power and voltage applications, although several technological issues are still to be addressed [23]. A more in-depth discussion on such non-charge-based devices falls outside the scope of this thesis, and we refer the interest reader to the following publications [23–27].

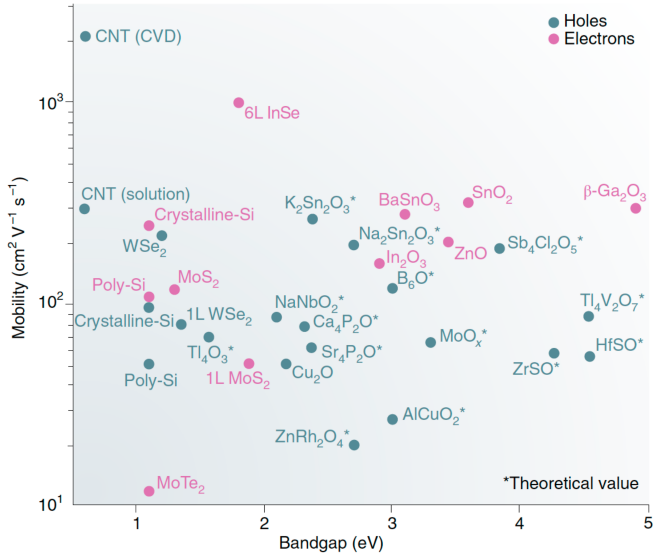


Figure 1.4 – Materials considered for BEOL devices. Depending on the bandgap and mobility of the materials possible applications ranges from logic to memory and power delivery. Reproduced with permission from [6]. Copyright (2018) Spriger Nature.

1.3 Multiple-Independent-Gate FETs

Multiple-Independent-Gate (MIG) FETs are a novel class of devices with multiple gate regions, that independently control the switching properties of the device. The key enabler of such concept is the exploitation and control of the inherently ambipolar behavior, also known as ambipolarity, of *Schottky-Barrier* (SB) FET, for the realization of doping-free devices and circuits. Ambipolarity arises in *Schottky-Barrier Field Effect Transistors* (SB-FETs) since the conduction property are determined by the bands alignment at the source and drain contacts, and by the gate-induced modulation of the Schottky-barriers. Both electrons and holes can be injected in the intrinsic device channel depending on the voltage applied to the gate. Ambipolarity is usually considered a drawback in standard CMOS devices, since it allows the conduction of both charge carriers in the same device, deteriorating the OFF-state of the transistor. As a result, ambipolarity is suppressed thanks to the doping process that creates strictly unipolar devices.

In MIG-FETs instead, the device polarity is not set during the fabrication process, but it can be dynamically changed thanks to the additional gate electrode (*Polarity Gate* (PG)), which modulates the SB at source and drain, and therefore enables to select the carrier type to inject into the channel. The transistor can then be switched ON and OFF by using the other gate electrode, namely *Control Gate* (CG). This device concept does not require any ion-implantation doping, thus there is no need for the separate development of n- and p-type device, to the benefit of fabrication simplicity and device regularity. Moreover the absence of a doping step during the fabrication process eliminates the need for high-temperature dopant annealing, making the device

attractive for 3D monolithic integration. An added advantage of this class of devices is that the dynamic control of the transistor polarity enables the realization of compact operators, such as 4-transistor *2-Input Exclusive OR* (XOR-2) and *3-Input Majority* (MAJ-3) operators, that can be used as the building blocks to realize circuits with higher computational density with respect to CMOS. This class of devices, of core importance for the work presented in this thesis, is introduced in greater details in Ch. 3.

1.4 Thesis Objectives and Achievements

This thesis was conducted in collaboration with IMEC research center in Leuven, Belgium, where all the experimental work presented here has been performed. The main objective of this thesis is to exploit a *Multiple-Independent-Gate* (MIG) device structure to explore doping-free polarity-controllable technologies for *Two-Dimensional* (2D) electronics. Since physical doping of 2D materials is still an open challenge, the realization of *Complementary Metal-Oxide-Semiconductor* (CMOS) logic gates on 2D semiconductors has only been achieved with the use of chemical doping and different metal contacts or using two different 2D materials for n- and p-type devices. Both methods greatly complicate the fabrication process and in the case of chemical doping make it non-scalable and non-compatible with conventional CMOS fabrication.

When no physical or chemical doping is introduced, contact to a 2D-semiconductor usually results in the creation of a Schottky barrier. Thus, the use of electrostatic doping of the contact regions, to reversibly select the polarity of the transistor, adapts perfectly to these emerging class of materials, and provides a path for the realization of CMOS logic with the use of a single 2D ambipolar semiconductor. The main achievements of this thesis are here summarized:

- The demonstration of the first polarity-controllable *tungsten di-selenide* (WSe_2) transistor, and the first device on any 2D semiconductor to exhibit polarity-control with I_{ON}/I_{OFF} ratios greater than 10^6 for both polarities on the same device. This achievement is the focus of Ch. 4 and resulted in the following publications [28], [29] and [30]. The results are also featured in two book chapter dedicated to MIG devices [31] and polarity-controllable WSe_2 devices [32].

- The demonstration of the first logic gates realized with doping-free polarity-controllable *Field-Effect Transistors* (FETs) on 2D-WSe_2. A complete standard-cell library (*Inverter* (INV), *NOT-AND* (NAND), *NOT-OR* (NOR), *2-Input Exclusive OR* (XOR-2), *3-Input Exclusive OR* (XOR-3) and *Majority* (MAJ)) is experimentally shown. This library can be the basis for conventional logic synthesis tools to map any logic functionality. These results are described in detail in Ch. 5 and resulted in the following publications [33] and [34]. The achievements described in the chapter have also been featured in an oral presentation at the 2018 Flatlands beyond graphene conference.

- The study of scaling trends and performance evaluation for polarity-controllable devices on WSe_2 and on low-bandgap 2D-*Transition Metal Di-Chalcogenides* (TMDCs). The simulations performed show a successful scaling path for low-bandgap 2D-TMDCs in the sub-10 nm dimensions. These results are described in detail in Ch. 6 and resulted in the following publication [35] and [29]. They are also featured in a book chapter dedicated to polarity-controllable WSe_2 devices [32].
- The evaluation of the propagation delay and *Energy-Delay Product* (EDP) for a variety of logic gates that are simulated within the Sentaurus TCAD environment, using an optimized device structure. The extracted propagation delays and EDP are compared to the ones of other emerging technologies studied in BCB 3.0 [25], showing how the implementation of XOR-2 gates with 2D *Double-Independent-Gate* (DIG) FETs can provide around 10× lower EDP than any other emerging technology. These results are still unpublished.

Overall this thesis has helped to push the field of doping-free MIG in the realm of 2D electronics, providing experimental proof-of-concepts devices and demonstrating a library of doping-free logic gates, as well as accurate simulations assessing the performances of ultra-scaled transistors and logic gates. The work presented has also contributed to the IMEC beyond-CMOS core program and has been presented at the internal *Partner Technical Week* (PTW), where IMEC core partners (such as Intel, Samsung, Global Foundries, TSMC, etc...) are updated on the recent results achieved at IMEC.

1.5 Thesis Organization

This thesis is organized as follows:

- **Chapter 2 - TMDCs for 2D Electronics** This chapter introduces TMDCs and gives a broad overview of the recent advances in the research field, spanning from growth to 2D electronics. Finally it focuses on the importance of ambipolarity for polarity-controllable devices.
- **Chapter 3 - Multiple Independent Gate Devices** In this chapter we introduce the concept of MIG and review the state-of-the-art of the research field. We describe the basic opration principle of MIG devices and show how they have been realized on silicon and on novel materials that are of interest for beyond-CMOS electronics. We finally introduce the circuit-level advantages that are enabled by the use of MIG transistors.
- **Chapter 4 - Polarity-Controllable WSe_2 FETs** This chapter presents the original research work conducted on 2D-WSe_2 and focuses on the demonstration of the first WSe_2 polarity controllable devices. The fabrication process of the devices is described in detail and the full characterization of the experimental devices is presented.

- **Chapter 5 - Doping-Free WSe_2 Logic Gates** This chapter in combination with Ch. 4 forms the backbone of this thesis and describes the demonstration of first polarity-controllable doping-free logic gates fabricated on WSe_2. We first review the fabrication process of the devices and the improvements made with respect to the transistors presented in Ch. 4 and then focus on the characterization of the demonstrated logic gates (INV, NAND, NOR, XOR-2, XOR-3 and MAJ), creating a complete standard-cell library for use in logic synthesis tools.

- **Chapter 6 - Scaled Devices and Logic Gates Simulations** This chapter is dedicated to the simulation study of scaled polarity-controllable devices and logic gates. To estimate the electrical characteristics of such ultra-scaled devices, we first use ballistic self-consistent quantum simulations in the *Non-Equilibrium Green Function* (NEGF) formalism. We explore scaling for devices based on WSe_2, the most promising material for which experimental results are available (as shown in Ch. 4 and Ch. 5), and then focus on the selection of novel 2D semiconductors, for which experimental demonstrations are still lacking, to enhance the performances of the device. Finally, in order to study the performances of logic gates we develop a Sentaurus TCAD simulation that is able to reproduce the switching characteristics simulated with the quantum-transport simulations and perform transient simulations for the logic gates switching.

- **Chapter 7 - Conclusions and Future Perspectives** Finally, this last chapter is dedicated to concluding this thesis and highlight future perspectives for 2D-TMDCs and polarity-control.

- **Appendix** - The appendix of this thesis provide additional insight in the fabrication and characterization of the polarity-controllable devices and logic gates. In Appendix A we show the steps that are needed to properly clean the dielectric surface before exfoliation, as well as the flakes, after they have been exfoliated or transferred. In Appendix B we report other measurements on different WSe_2 flakes that strengthen our claims regarding the effect of contact annealing presented in Section 4.2. Finally, in Appendix C, we describe the effect of oxide encapsulation, that was studied in order to realize top-gated devices, on the ambipolar characteristics of WSe_2 devices.

2 TMDCs for 2D Electronics

There is plenty of room at the bottom

— Lecture at Caltech, 1959
Richard Feynman

This thesis targets the development of doping-free polarity-controllable devices fabricated with *Two-Dimensional* (2D) *Transition Metal Di-Chalcogenides* (TMDCs). Atomically-thin 2D materials belonging to the TMDCs family are, thanks to their physical and electrical properties, an exceptional vector for the exploration of next-generation semiconductor devices. Research on 2D materials has experienced remarkable growth in the last decade. Major semiconductor companies are looking with interest at this novel class of materials in the hope of addressing the shortcomings that are making scaling of silicon-based electronic devices increasingly difficult. Among TMDCs, thanks to the possibility of ambipolar conduction, *tungsten di-selenide* (WSe_2) provides a platform for the efficient implementation of *Multiple-Independent-Gate* (MIG) polarity-controllable transistors (that will be introduced in Ch. 3).

This chapter is dedicated solely to 2D-TMDCs and aims at giving a broad overview of the research field, and the progresses that have been made in recent years, spanning from growth in Sec. 2.2 to 2D-electronics in Sec. 2.3. Finally in Sec. 2.4 we focus on the ambipolar properties of certain 2D materials, that will be a key feature of the devices studied in this thesis.

2.1 Material Properties

Despite the diversity in conduction properties and atomic composition, all 2D materials are composed by covalently-bonded in-plane layers that are held together by weak Van-der-Waals interatcions to form a 3D crystal. Each layer has a uniform thickness ranging from 0.3 to 0.7 nm, depending on the atomic structure of the layer, with the thinnest material being graphene, which is composed by a single layer of carbon atoms. A TMDCs layer with general formula MX_2, is composed by a transition metal (M) of group IV, V

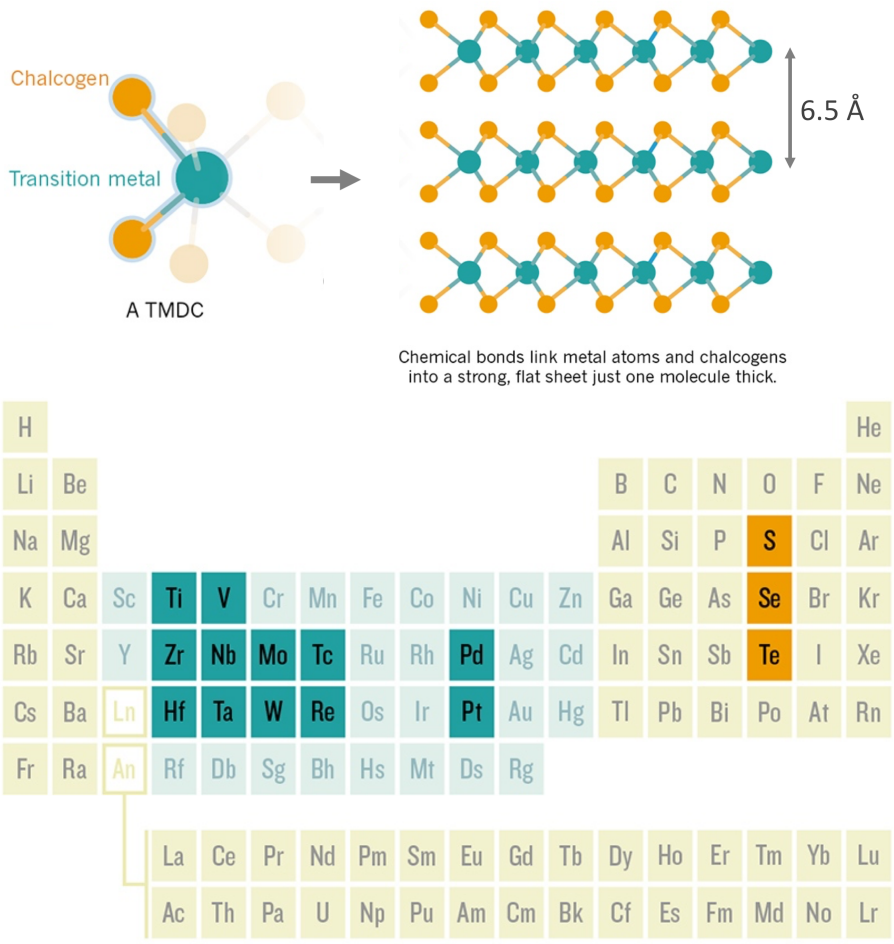


Figure 2.1 – The transition-metal di-chalcogenide family. Reproduced with permission from [36]. Copyright 2015 Springer Nature.

or VI, such as *molybdenum* (Mo), *tungsten* (W), *hafnium* (Hf), etc., sandwiched between two chalcogen atoms (X), such as *sulfur* (S), *selenium* (Se) or *tellurium* (Te) [37, 38]. The composition of a generic MX_2 material is shown in Fig. 2.1. The weak Van-der-Waals interaction are present in the out-of-plane direction thanks to the pristine surface of each layer, *i.e.* presence of no dangling bonds. The peculiar layered structure of graphite and of TMDCs was already known in the early 1970's, and certain optical and electrical properties had already been discovered [37, 38]. It wasn't however until the pioneering work of Novoselov *et al.* in 2004 that a graphite monolayer (now commonly know as graphene) was isolated and studied [39], effectively marking the beginning of 2D electronics. However, the semimetallic nature of graphene prevents it to be used as the primary vehicle for novel digital transistors and circuits. Amongst TMDC materials, the ones formed by group VI (Mo and W) and group IV (Zr and Hf) metals show a semiconducting behaviour and have exhibited excellent electrical properties [40–42], that

will be further analyzed in Sec. 2.3. The presence of a sizeable bandgap (1-2 eV) makes TMDCs materials appealing for electronics applications, as it allows us to realize devices with low leakage floor and high ON/OFF current ratios [17, 18, 43, 44]. Amongst the other

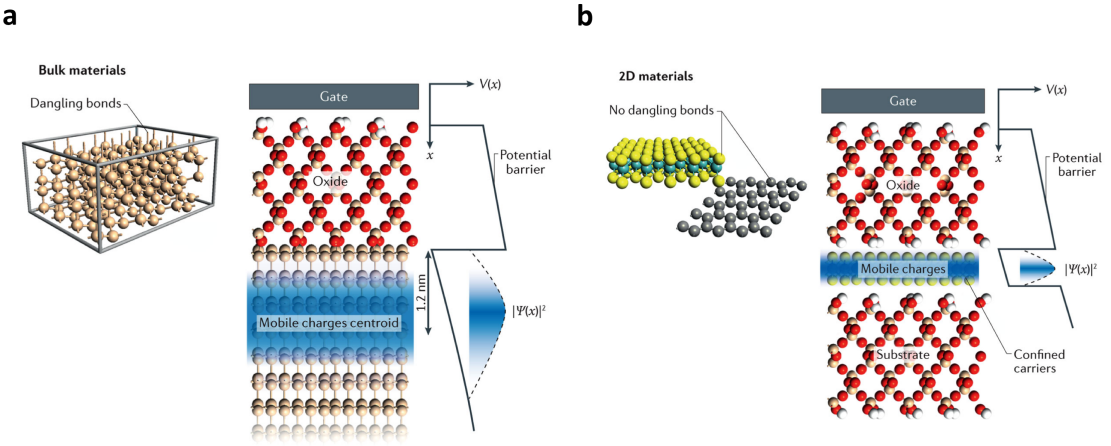


Figure 2.2 – Benefit of 2D-TMDCs for electronic applications. **(a)** Case of a bulk material. **(b)** Case of a 2D material. Adapted with permission from [45]. Copyright 2016 Springer Nature.

remarkable features of TMDCs, their layered structure provides 2D films of controllable uniform thickness with dangling-bonds free interfaces. Moreover, their extreme thinness enables optimal electrostatic control and carrier confinement (see Fig. 2.2). The low in-plane dielectric constant alleviates *Short-Channel Effects* (SCE) and *Drain-Induced Barrier Lowering* (DIBL) [46, 47] which are detrimental to device performances. The high effective mass of charge carriers (especially with respect to III-V materials) helps reducing direct source-to-drain tunneling at ultra-scaled dimensions [48, 49] providing a better control of the device OFF-state by the gate terminals. 2D materials are also attractive for monolithic integration on top of *Complementary Metal-Oxide-Semiconductor* (CMOS) or multi-stacking of TMDCs layers [50], thanks to the low thermal budget needed in the fabrication process. Moreover several semiconducting TMDCs show a transition between an indirect few-layer bandgap to a direct monolayer band-gap, thus enabling the possible use of these monolayers for optoelectronics applications [41, 51]. Beyond their use in established transistor architectures, 2D TMDCs can be used to form heterostructures that present interesting physical phenomena, such as tightly bound excitons [52, 53] and plasmonic effects [54, 55], which can lead to new device concepts for future electronics.

2.2 Synthesis and transfer of 2D TMDCs

The first demonstrations of novel devices based on 2D semiconductors were carried out mainly thanks to the exfoliation technique originally developed for graphene [56]. Although this top-down technique allows for the production of high quality thin flakes, with dimensions as big as tens of microns, this method is not scalable, does not allow

any systematic control of the flake size and thickness and makes the fabrication much more challenging. In order to enable the creation of a reliable technology based on 2D-TMDCs, that would go beyond the simple demonstration of few working devices, it is essential to develop bottom-up methods for the productions of large-area, defect-free, atomically thin films with uniform electrical, optical and structural properties. Current methods for the growth of TMDCs materials are based on *Chemical Vapor*

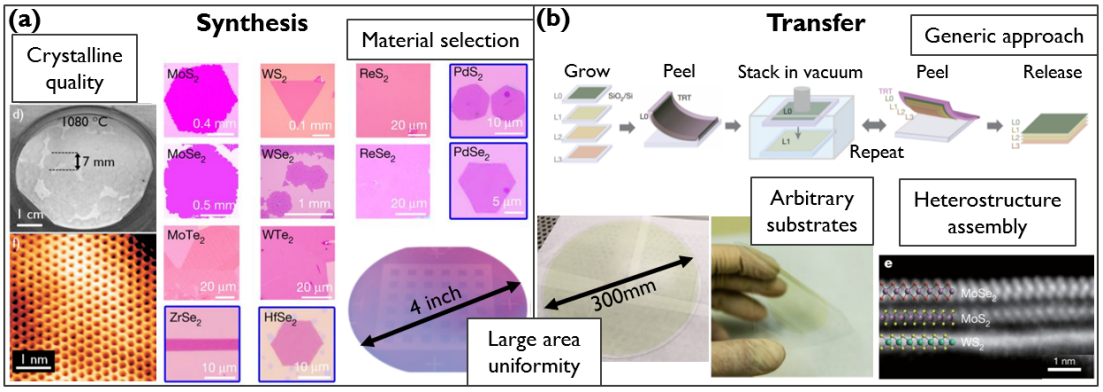


Figure 2.3 – Relevant metrics for synthesis and transfer of 2D materials. (a) Crystalline quality and wide material selection are important to allow high performance devices. **(b)** Transfer is a generic approach to allow integration in arbitrary substrates or assembly of heterostructures. Large area uniformity is essential to both synthesis and transfer, to allow low variability in material properties over wafer scales. Adapted with permission from [57–62].

Deposition (CVD) [63–72], Van der Waals epitaxy [73, 74] and *Metal-Organic Chemical Vapor Deposition* (MOCVD) [50]. These techniques have shown promising results for mono(few)-layer MoS_2 [50, 63–65, 67, 68, 74], WSe_2 [70–72, 75], WS_2 [50, 66] and for the creation of 2D heterostructures [69, 70] that researchers are exploring for the realization of efficient *Tunnel Field-Effect Transistors* (TFETs). Basic operational circuits [63, 76] have been demonstrated on CVD grown MoS_2 and single devices have shown gigahertz radio frequency performances [67] combined with high current densities, exceeding 200 $\mu A/\mu m$, and intrinsic low-field mobility up to 55 $cm^2V^{-1}s^{-1}$. Multilayer WSe_2 grown by CVD using graphene as seed material has shown p-type mobility higher than 80 $cm^2V^{-1}s^{-1}$, when using oxygen as doping material [72]. Recently uniform growth of monolayer MoS_2 and WS_2 has been demonstrated [50] on a 4-inch wafer, using MOCVD, with a resulting device yield of 99%. However, this process has the downside of being very time consuming (26 hours needed to grow a uniform 4-inch monolayer).

Fig. 2.3a presents relevant metrics for synthesis of 2D materials, namely the crystalline quality (e.g. grain size) of the grown layers, the possibility of growing a number of different materials and the large area uniformity of the synthetic layer. Two main synthesis approaches exist, first growth directly on the device wafer, as often done for TMDCs [57, 59, 77], and second, the growth on an optimized growth substrate,

such as metal films for graphene [58, 78] or hexagonal-Boron Nitride (hBN) [79] and sapphire for TMDCs [80, 81], with a subsequent transfer step [60, 82] for integration. Direct growth is limited by the maximum temperature allowed at different process steps, specially when 2D materials are co-integrated with a standard silicon CMOS technology. However, if growth is limited at 450° C, for back-end-of-the-line (BEOL) integration, the resulting material, in particular 2D TMDCs, is highly defective [83, 84]. Besides prohibitive temperatures, the growth environment (corrosive or metal-containing gases) can also result in lower reliability of the dielectric where the 2D material is grown. When using a dedicated growth substrate, the temperature limitations are lifted, which allows this approach to achieve high crystalline quality [78, 80]. The growth substrate can be carefully selected and tailored to achieve the best possible synthesis, where layer-by-layer growth has been demonstrated with precise atomic control and reduction of strain and doping effects [85].

This temperature flexibility comes at the expense of an additional transfer step, which decouples the growth parameters from the device integration. Transfer allows high quality 2D materials to be integrated onto arbitrary substrates, which ranges from standard CMOS wafers (either in the *Front-End-Of-the-Line* (FEOL) or *Back-End-Of-the-Line* (BEOL)) to flexible substrates [60]. It is, in principle, a generic approach, which allows the manipulation of different 2D materials with the same method [62]. In the context of logic devices, uniform transfer of large area 2D materials is a key challenge. Transfer relies on interface interactions between the original substrate, 2D material, and the target wafer, and is normally done using water or acid assisted intercalation [60, 82, 86, 87]. Understanding those interactions and being able to develop an all-dry process is critical to achieve uniform and repeatable transfer which has minimal impact on the 2D material. By allying 300 mm growth capabilities with standard wafer bonding tools, a uniform 300 mm dry transfer was recently reported [61]. Fig. 2.3b illustrates the transfer process, with notable examples of each of these metrics. Besides transferring the 2D materials onto arbitrary substrates, understanding the interactions present after transfer and the impact of different substrates is also necessary. During this integration step, the 2D material is transferred onto a wafer surface, which may have a series of non-idealities such as roughness, surface chemistry, contamination, among others. Due to the atomically thin nature of the 2D material, it is highly sensitive to the surrounding environment, and these non-idealities can cause unintentional doping, strain and increased defectivity. This surface must be carefully engineered in order to result in stable and reliable transistor operation. Current understanding is that other 2D materials are the ideal substrates for both graphene and TMDC devices [88–90].

2.3 Experimental State-of-the-Art in 2D Electronics

Since the first demonstration of a *Mono-Layer* (1L) *molybdenum di-sulphide* (MoS_2) transistor with high mobility and high ON/OFF current ratios in 2011 by Radisavljevic

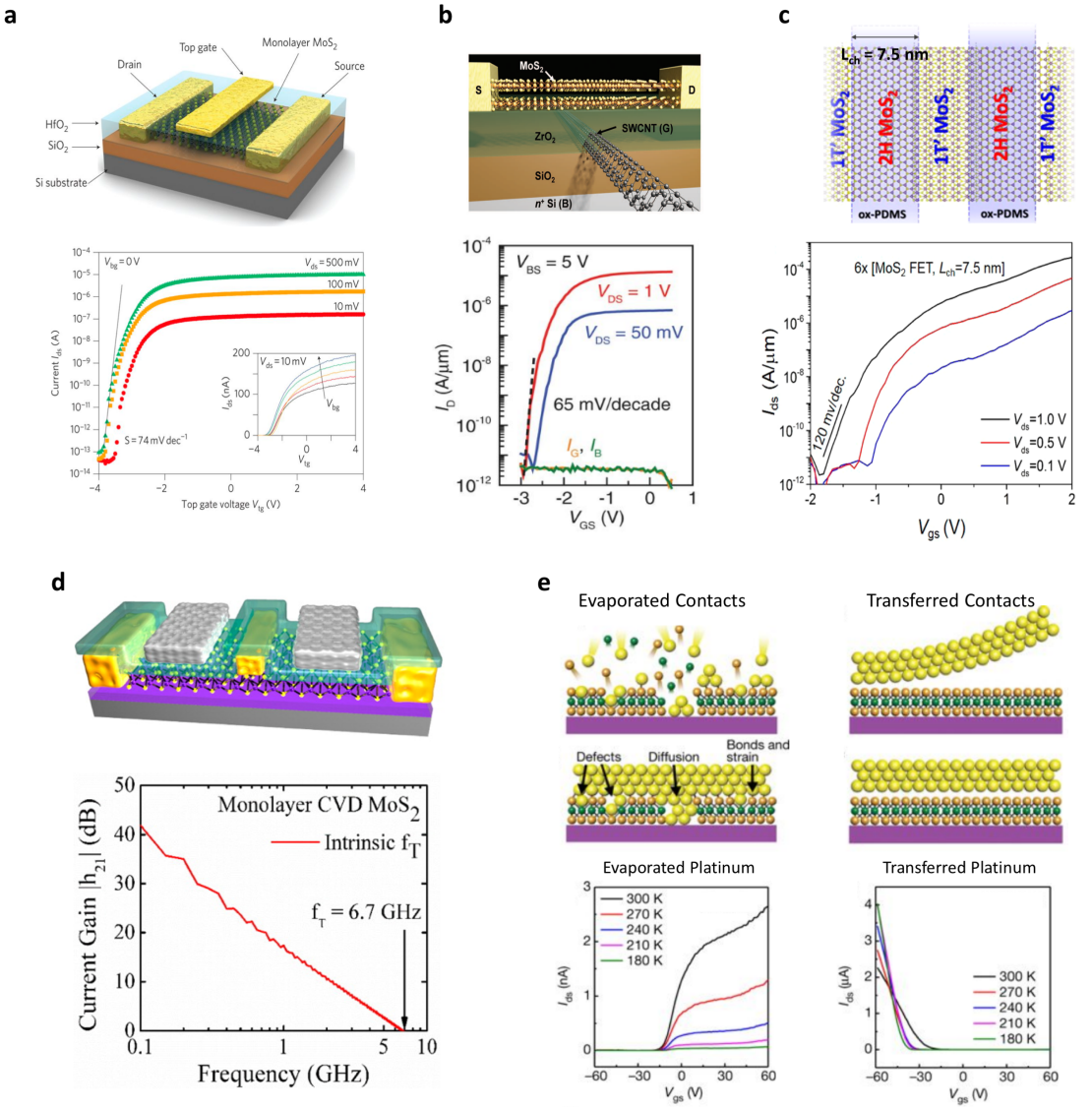


Figure 2.4 – 2D-MoS_2 electronics. **(a)** Adapted with permission from [21] **(b)** Adapted with permission from [91]. **(c)** Adapted with permission from [92] **(d)** Adapted with permission from [67]. **(e)** Adapted with permission from [93]

et al. [43] (see Fig. 2.4a) the field of 2D electronics has gained worldwide traction with a constant increase in the number of publications and a growing interest of the research community. Among the several semiconducting materials belonging to the TMDCs family, and introduced in Sec. 2.2, the most appealing for electronic application have been Molybdenum (MoS_2, *molybdenum di-telluride* ($MoTe_2$) and *molybdenum di-selenide* ($MoSe_2$)) and Tungsten compounds (WSe_2 and *tungsten di-sulfide* (WS_2)). These semiconducting materials are stable in air, even in their monolayer form, are easily exfoliated from commercially available bulk-crystal and are also grown with high-quality in large-area, as shown in Sec. 2.2. Several major results presented in the

following sections have been achieved using mechanical exfoliation, which, despite being a non-scalable approach, provides high-quality flakes that are used to gain insights on the properties of these materials and assess their potential for electronic applications. The most known TMDC material, MoS_2, has proven to be a viable solution for the realization of *n*-MOS transistors [43,44,94–96] and ultra-scaled devices have been recently demonstrated [91, 92, 97] (see Fig. 2.4(b,c)). In Fig. 2.4b a single carbon nanotube was used to gate a transistor with MoS_2 semiconducting channel, proving the superior electrostatic control achievable thanks to the ultra-thin MoS_2 [91]. In Fig. 2.4c devices with gate length below 10 nm were realized by inducing a metallization of the MoS_2 with a lithium solution. This process also allows for a reduced contact resistance thanks to the metallic MoS_2 forming a seamless contact scheme with the 3D metal [98]. High-frequency operation of CVD-grown MoS_2 has also been reported, see Fig. 2.4d. To date, the largest circuit reported on 2D MoS_2 is a 1-bit microprocessor composed of 115 transistors [76], and other small circuits have also been previously demonstrated [44, 63, 94]. However, due to considerable difficulties in achieving *p*-type behavior in MoS_2 [99] all these circuits adopt a non-complementary *n*-MOS logic, that is not power-efficient. It has recently been demonstrated how *p*-type conduction can be achieved on MoS_2 by transferring metal contacts on top of the 2D material, rather than evaporating it [93]. Using this innovative technique it has been possible to show an almost linear relationship between the work function of the contact metal and the height of the Schottky barrier created, and *p*-type conduction has been achieved with high work function metals (such as *gold* (Au) and *platinum* (Pt)).

Being able to develop both *n*- and *p*-type devices on the same semiconducting material is extremely important in order to achieve complementary operation of logic-gates and circuits (see Fig. 2.5). Conventional CMOS uses ion implantation to physically dope silicon creating low-resistance ohmic contacts and irreversibly setting the polarity of the fabricated device (*n*- or *p*-type) according to the dopant atoms used (*arsenic* (As) for electron and *phosphorus* (P) for hole doping). Since a reliable physical doping technique for 2D materials is still lacking, chemical doping techniques have been explored to both reduce contact resistance (thus achieving higher ON-current) and to realize complementary behavior [16–18, 72, 100, 101]. Using WSe_2 as semiconducting material complementary operations of inverters and other small logic gates has been recently shown (see Fig. 2.5(a,b)) [17, 18]. However, chemical doping is often non-scalable, non-stable and non-compatible with conventional CMOS fabrication. An innovative doping strategy has recently been proposed where a strong light source is used to locally create defects in $MoTe_2$ semiconducting channels, that upon oxidation induce *p*-type doping [102]. This technique has allowed the realization of photovoltaic cells and *Bipolar-Junction Transistor* (BJT) arrays [102]. The possibility of using two separate 2D semiconductors to separately develop *n*- and *p*-type transistors has been explored in [103], that have used MoS_2 to fabricate *n*-MOS device and monolithically integrate WSe_2 *p*-type devices on top, demonstrating complementary logic gates. This work shows the potential of 2D materials to be used in combination with CMOS for 3D monolithic integration, as

displayed in Fig. 2.5c.

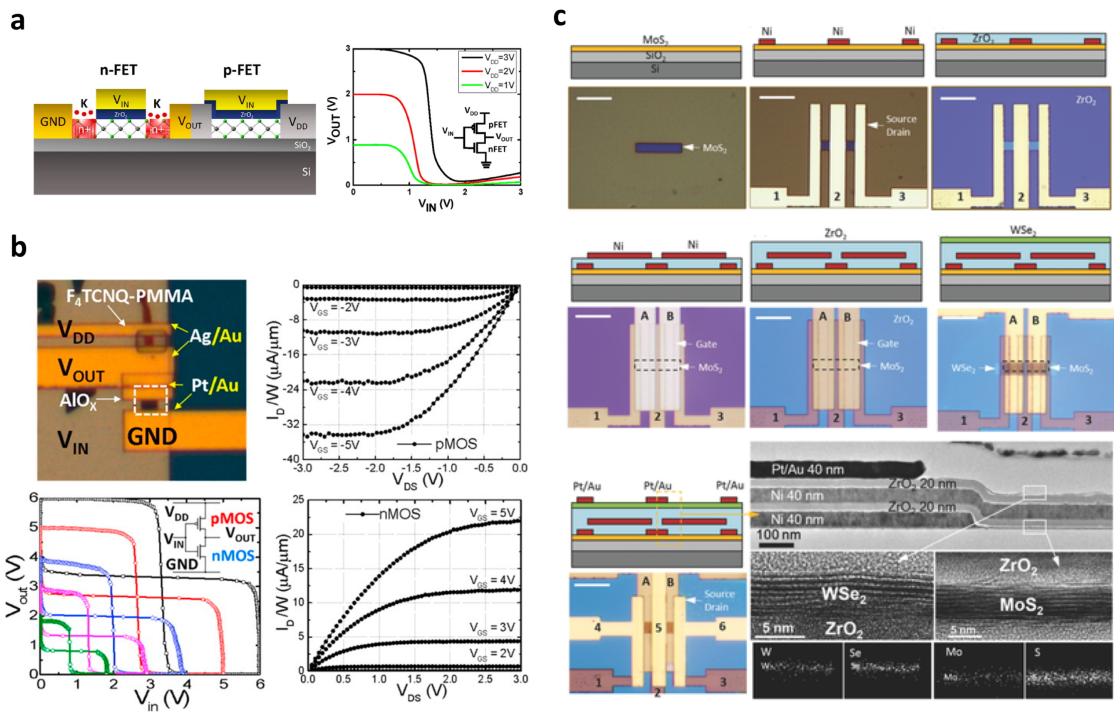


Figure 2.5 – Complementary devices on 2D materials. **(a)** Schematic depiction of the fabricated WSe_2 inverter with chemically-doped contacts for *n*-type *Field-Effect Transistor* (FET) and measured device characteristics. Notice the different contact metal used (Gold and Platinum) for the *n*- and *p*-type FET respectively. Reprinted with permission from [17]. Copyright 2015 American Chemical Society. **(b)** Complementary devices realized on WSe_2 with different metal contacts for *n*- and *p*-type and stable chemical doping. Output characteristics and inverter behavior. Reprinted with permission from [18]. Copyright 2015 American Chemical Society. **(c)** Fabrication process for monolithically integrated 2D logic gates. NAND, NOR and INV are demonstrated with the use of MoS_2 for *n*-type and WSe_2 for *p*-type. Reprinted with permission from [103]. Copyright 2016 John Wiley and Sons.

As already motivated in Ch. 1, a promising alternative to the use of either chemical or physical doping is the exploitation of the ambipolar behavior, which refers to the capability of a semiconductor to conduct both charge carriers, and has been shown on several 2D semiconductors such as WSe_2, $MoTe_2$, WS_2 and $MoSe_2$ [104–108]. As ambipolarity will be one of the key concepts throughout this thesis, it is discussed in more depth in Sec. 2.4. Other 2D materials that are being explored include members of the TMDCs family such as $HfSe_2$ and $ZrSe_2$ that are appealing since their native oxides HfO_2 and ZrO_2 are CMOS compatible [109], and also black phosphurus (BP). BP in particular has recently drawn considerable interest thanks to its high carrier mobility, ambipolar nature and lower semiconducting bandgap compared to TMDCs [110–114]. However BP is non-stable in ambient condition and only few minutes of air exposure

results in a complete oxidation of the semiconducting layer, making it challenging to integrate in a conventional fabrication flow.

2.4 Value of Ambipolarity

Ambipolarity refers to the capability of a semiconducting material to conduct both type of charge carriers, i.e. electrons and holes. Ambipolarity is usually considered a drawback in conventional CMOS electronics, where the building blocks are unipolar, *n*- or *p*-type, doped transistors with Ohmic contacts. Physical doping is introduced in silicon with ion implantation during the fabrication process, and irreversibly sets the polarity of the transistors according to the dopant atoms used (As for *n*-type doping and P for *p*-type doping). Physical doping, through ion-implantation, of 2D material has not proven to be successful due to extreme thinness of the 2D semiconductors, with ions just implanting in the substrate. The possibility of introducing dopant atoms (such as *rhenium* (Re) or *niobium* (Nb)) for MoS_2) during growth of the 2D material has been reported, but lacks selectivity and does not allow for any control of the doping profile [11–15]. The realization of complementary transistors has only been demonstrated with the use of chemical doping and different metal contacts [17, 18] or using two different semiconducting materials for *n*- and *p*-type devices [103], as shown in Fig. 2.5. Several chemical and molecular doping techniques have been developed, but are often non-stable and non CMOS compatible, thus not allowing integration of chemically-doped 2D devices in the BEOL fabrication of VLSI circuits [16–18].

When no physical or chemical doping is introduced, contact to an intrinsic 2D-semiconductor usually results in the creation of Schottky barriers at source and drain. If the Fermi level of the metal aligns with the Fermi level of the semiconductor in such a way that the Schottky barriers created are similar for electrons and holes (mid-gap contact), both charge carriers can be injected in the channel, thus achieving ambipolar conduction. Ambipolarity has been demonstrated in several 2D materials, such as WSe_2, WS_2, $MoTe_2$ and $MoSe_2$, and notable examples are reported in Fig. 2.6. It is clear that a purely ambipolar device would be difficult to switch off with a standard gate configuration, as we cannot selectively suppress the injection of one type of charge carriers [28, 105, 115]. However, a symmetric ambipolar behavior must be regarded as the starting point for the efficient realization of polarity-controllable devices. The key to unlock the possibility of controlling the polarity of the transistor is the separate gating of different channel regions, thanks to a MIG structure [28, 115]. MIG devices will be introduced in Ch. 3 and used throughout this thesis. The original experimental work presented in the thesis uses WSe_2, which to date appears to be the most suitable 2D material for demonstration of polarity-controllable technology.

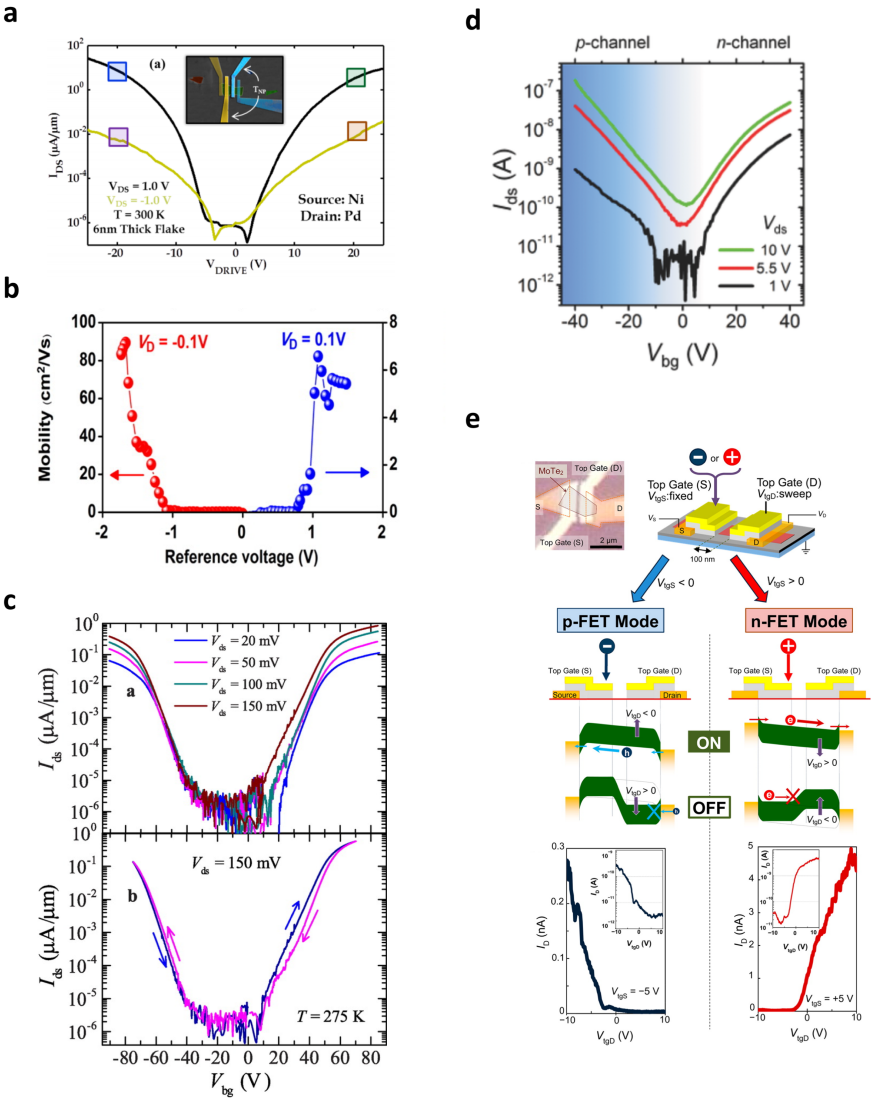


Figure 2.6 – Ambipolarity on 2D materials. **(a)** Transfer characteristics of WSe_2 ambipolar transistor with Nickel source contact (for electrons injection) and Palladium drain contact (for holes injection). Adapted with permission from [105]. Copyright 2013 AIP Publishing. **(b)** High-mobility reported for both electrons and holes on 1LCVD WSe_2 *Electric Double-Layer Transistors* (EDLT). Adapted with permission from [106]. Copyright 2013 American Chemical Society. **(c)** Ambipolar conductance for exfoliated $MoSe_2$ grown by chemical vapor transport and contacted with gold electrodes. Reproduced with permission from [107]. Copyright 2014 American Chemical Society. **(d)** Ambipolar characteristics of exfoliated $MoTe_2$ grown by chemical vapor transport with gold contacts. Adapted with permission from [108]. Copyright 2014 John Wiley and Sons. **(e)** Demonstration of polarity-control on exfoliated $MoTe_2$ grown by chemical vapor transport . Reproduced with permission from [115]. Copyright 2015 American Chemical Society.

3 Multiple Independent Gate Devices

L'unione fa la forza...

— Typical Italian saying

This chapter is dedicated to *Multiple-Independent-Gate* (MIG)-*Field-Effect Transistors* (FETs), that have been introduced in Sec. 1.3, and gives a broad overview of the field of research, summarizing the results achieved by different reseach groups worldwide. MIG FETs are a novel class of devices with multiple gate regions, that independently control the switching properties of the device. The key enabler of such concept is the exploitation and control of the inherently ambipolar behavior, also known as ambipolarity, of *Schottky-Barrier* (SB)-*Field-Effect Transistor* (FET), for the realization of doping-free devices and circuits. Depending on the gate configuration different operation modes can be achieved and have been demonstrated experimentally on silicon as well as on a variety of novel materials. Here, we focus especially on the possibility of achieving polarity control thanks to *Double-Independent-Gate* (DIG)-FETs, which enable the fabrication of both *n*- and *p*-type devices without the use of physical doping. We also briefly touch on the different operation modes that can be achieved by realizing *Triple-Independent-Gate* (TIG)-FETs.

This chapter is organized as follows. In Sec. 3.1, MIG devices realized with silicon nanowires and silicon Fin-FETs, which are appealing for near-term scaling, are presented. Particular focus is given to the explanation of the main operation principle and to the different operation modes of such MIG-FETs. Sec. 3.2 is focused on long-term scaling opportunities for beyond-*Complementary Metal-Oxide-Semiconductor* (CMOS) electronics and different promising materials for the realization of the next generation of DIG-FETs are presented. Here, we purposely omit work on 2D-*Transition Metal Di-Chalcogenides* (TMDCs), as they have already been extensively presented in Ch. 2. Finally, Sec. 3.3 illustrates the circuit design opportunities allowed by the use of DIG-FETs, such as compact arithmetic logic gates and novel design methodology. The chapter is concluded in Sec. 3.4 with a brief summary. This chapter is largely based on

the book chapter by Resta *et. al.* [31], written as a review of MIG FETs.

3.1 Multiple-Independent-Gate Silicon Nanowires Transistors

The MIG structure allows for the fabrication of doping-free FETs and introduces novel functionalities at the device scale that enable innovative circuit-level design opportunities. MIG-FETs are a novel class of devices with multiple gate regions, that independently control the switching properties of the device. The key enabler of such concept is the exploitation and control of the inherently ambipolar behavior, also know as ambipolarity, of SB-FETs. Here we will only focus on SB-FETs as the building block of MIG-FETs, and for a more general coverage of Schottky-barriers physics and application, the interested reader can refer to [116].

Ambipolarity arises in SB-FETs since the conduction property are determined by the bands alignment at the source and drain contacts, and by the gate-induced modulation of the Schottky-barriers. Both electrons and holes can be injected in the intrinsic device channel depending on the voltage applied to the gate. Ambipolarity is usually considered a drawback in standard CMOS devices, since it allows the conduction of the both charge carriers in the same device, deteriorating the OFF-state of the transistor. As a result ambipolarity is suppressed thanks to the doping process that creates strictly unipolar devices. In MIG-FETs instead, the device polarity is not set during the fabrication process, but it can be dynamically changed thanks to the additional gate electrodes, which modulate the SB at source and drain, and therefore enable to select the carrier type to inject into the device. In principle no dopant implantation is required in the fabrication process of the device, thus there is no need for the separate development of n- and p-type device, to the benefit of fabrication simplicity and device regularity. The gate-induced modulation of the SB enables dynamic control of the polarity and of the threshold voltage of the device at run-time. Moreover, with the peculiar gates configuration, the *Sub-threshold Slope* (SS) can be controlled when increasing the V_{DS} applied to the device. In particular, a dynamic control of the transistor polarity enables the realization of compact binate operators, such as 4-transistor XOR operator, that can be used as the building block to realize circuits with higher computational density with respect to CMOS [117, 118]. As introduced in Ch. 1, MIG FETs are devices whose conduction properties can be dynamically controlled via additional gate terminals. These additional gates, usually referred to as *program* or *polarity gates* (PG) act on the Schottky barriers present at the drain and source contact and allow to exploit different functionality and selecting different operation modes. Here, we focus on DIG devices, with different gates configurations, for polarity and sub-threshold swing control mode, Sec. 3.1.1, 3.1.2, and then, as a natural evolution, we highlight TIG transistors, which additionally allow the control of the threshold voltage of the device, Sec. 3.1.3.

3.1.1 Polarity Control

The first experimental reports on silicon-nanowires DIG devices were presented in [119,120] and both adopted a double gate geometry with a top-gate acting as control gate in the central region of the channel and the wafer substrate acting as program gate at the source and drain contacts. These first reports paved the way for the realization of more advanced design with Ω-gates for both control and program terminals first realized in [121] and optimized in [122], as shown in Fig. 3.1(a,b). The devices were fabricated using a bottom-up approach, with single silicon nanowires grown and transferred on a final substrate where two Ω-gates were then patterned. In this *Reconfigurable FET* (RFET) one Schottky junction is controlled to block the undesired charge carrier type, while the other junction controls the injection of the desired carriers into the channel, which is ungated in the central region. In the *p*-type configuration, shown in Fig. 3.1c, the program gate (PG) is set to a negative value and blocks the injection of electrons from the drain contact. The ON/OFF status of the device will then be determined by the voltage applied to the control gate (CG) at source. In a similar fashion, when PG is kept at a positive voltage, it blocks hole injection from the drain, while the CG acting at source controls the injection of electrons, Fig. 3.1c. It should also be noted that with this gate configuration, in order to switch the device from *p*-type to *n*-type behavior, both the polarization of the PG at drain contact and V_{DS} have to be reversed. The experimental transfer characteristics for both *p*- and *n*-type operation of the RFET are reported in Fig. 3.1d and show extremely low leakage current and negligible hysteresis.

Although the devices reported in [119–122] show the great potential of reconfigurable transistors, in order to realize a viable alternative to standard CMOS technology, a scalable top-down fabrication process that doesn't require using bottom-gate electrodes or complex transfer procedure of pre-grown nanowires, is necessary. The first experimental demonstration of a top-down fabrication method for silicon nanowires polarity-controllable devices was reported by De Marchi *et al.* [123] using vertically stacked nanowires, which represent a natural evolution of current Fin-FET technology, and provide greater electrostatic control on the channel, thanks to the gate-all-around (GAA) structure. The fabrication process starts from a lightly p-doped (10^{15}cm^{-3}) silicon-on-insulator (SOI) wafer, where the vertically-stacked silicon nanowires are defined using a Bosch process based on deep reactive ion etching (DRIE) [123, 124]. The nominal length of the defined nanowires is 350 nm with a diameter of 50 nm, with a typical 40 nm vertical spacing between. Thermal oxidation is then performed to grow the gate oxide (15 nm of SiO_2). The polarity gates are then patterned on conformal deposited polycrystalline silicon. A second thermal oxidation is performed in order to assure the separation between the polarity gates and the control gate, which is patterned on polycrystalline silicon in a self-aligned way with respect to the polarity gates. At the end of the process, considering the silicon consumed during the oxidation process, the diameter of the nanowires has been reduced to around 30 nm. After the definition of the nanowires and the gates, a nickel layer is sputtered and then annealed to form nickel silicide contacts at source and drain.

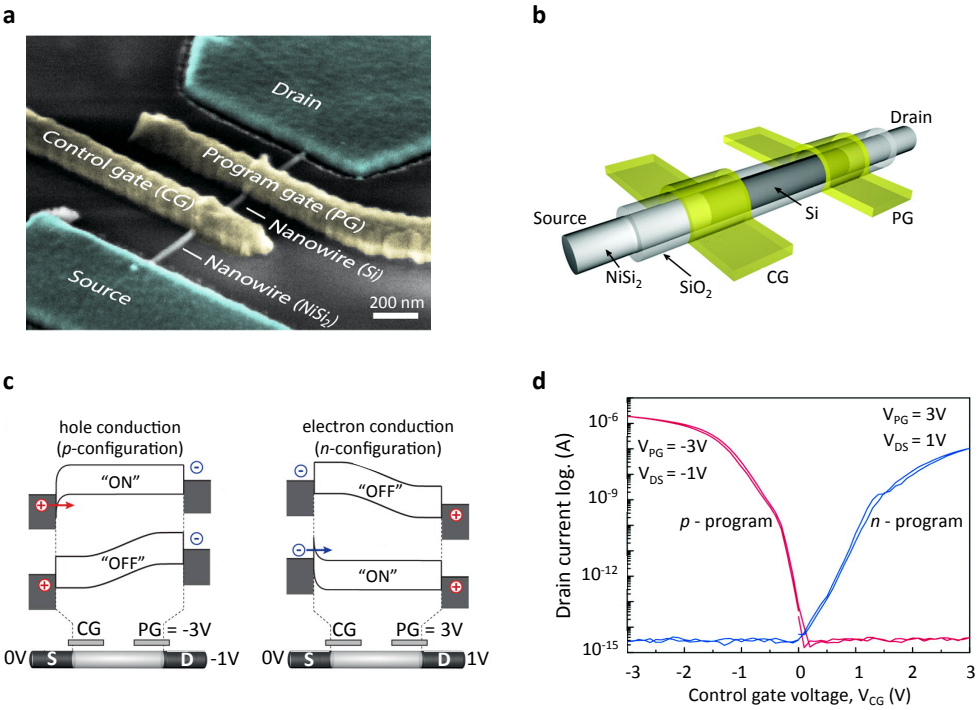


Figure 3.1 – The reconfigurable silicon nanowire FET with independent gates.(a) tilted SEM view of a fabricated device. **(b)** schematic description of the device structure, highlighting the different materials and terminals. **(c)** schematic band diagram of the different operation state of the reconfigurable nanowire FET. Arrows indicate electron (n-type) and hole (p-type) injection from contacts to the channel. The voltage values of all terminal are reported. **(d)** measured transfer characteristics of the reconfigurable nanowire FET. The characteristics are plotted in both forward and backward sweeping and show insignificant hysteresis. Adapted with permission from Heinzig *et al.* [121, 122]. Copyright (2012) and (2013), American Chemical Society.

The annealing temperature and duration are controlled in order to ensure the formation of the proper Ni_1Si_1 phase which provides a near mid-gap workfunction (∼4.8 eV) and low resistivity [125, 126]. The process can be further optimized to replace the SiO_2 with a high-k dielectric and to more aggressively scale both the oxide thickness and the channel length. A 3D schematic view and a SEM micro-graph of the final fabricated device are shown in Fig. 3.2. As can be appreciated in Fig. 3.2, the device geometry is different from the one reported in [121, 122], as now the polarity gate is acting simultaneously on both source and drain Schottky junctions, while the CG is now acting in the central region of the channel. With this particular gate configuration, the device polarity, n- or p-type, can be dynamically set by only the voltage applied to the PG, without having to invert the applied V_{DS}. This new gate configuration will enable tremendous advantages at the circuit level, as it will be further elucidated in Sec. 3.3. The device has four regions of operation, corresponding to the four combinations of high/low bias voltages applied on the two gates, namely CG and PG. In order to clearly illustrate the operation

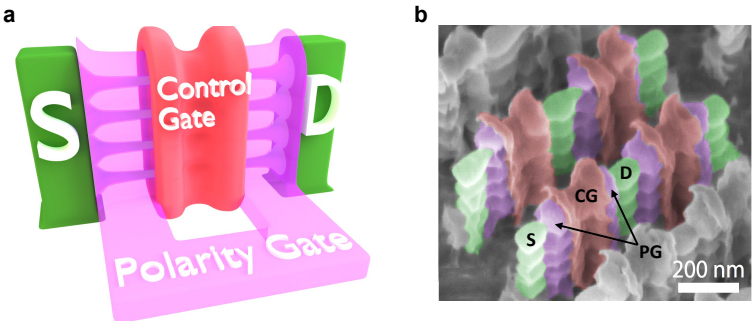


Figure 3.2 – Double-independent-gates silicon nanowires. **(a)** 3D conceptual view of the vertically-stacked silicon nanowires FETs. **(b)** tilted SEM micrograph of the fabricated devices. The SEM view shows several devices fabricated with regular arrangement. For a single device the main terminals are indicated, and the same terminals can also be visually identified on the other transistors. Adapted with permission from De Marchi *et al.* [123, 124]. Copyright (2012) and (2014) IEEE.

principle and the band structure relative to each operation mode we refer to Fig. 3.3:

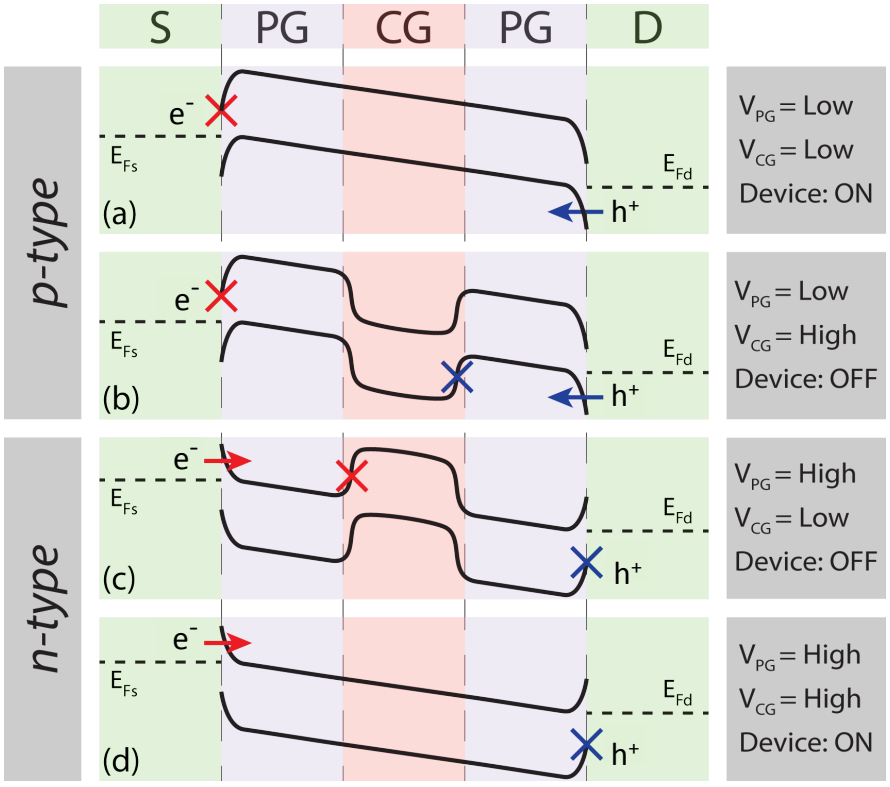


Figure 3.3 – Conceptual band diagrams for the DIG-FET in the different operation modes. Adapted with permission from De Marchi *et al.* [123]. Copyright (2012) IEEE.

1. ***p-type ON state:*** For low voltage values (logic '0') of the PG, the band bending at source and drain allows for hole conduction in the channel, which are injected through the thin tunneling barrier at drain, while electron conduction is blocked by the thick Schottky barrier at source (see Fig. 3.3a). In this configuration, the CG is kept at a low bias allowing for holes conduction through the channel.

2. ***p-type OFF state:*** To switch off hole conduction, the voltage applied to the CG is inverted to high values (logic '1'). The potential barrier created in the central region of the channel does not allow for hole conduction, while electron conduction is still blocked by the Schottky barrier at source (see Fig. 3.3b).

3. ***n-type OFF state:*** For high voltage values of the PG, the band bending at source and drain allows for injection of electrons in the channel through the thin tunneling barrier at the source contact, while hole conduction is blocked by the thick Schottky barrier at drain. Similarly to the *p*-type OFF state, electron conduction is blocked by the potential barrier created by the CG, which is now kept at logic '0' (see Fig. 3.3c).

4. ***n-type ON state:*** The bias on the PG gate is not changed with respect to the *n*-type OFF state, and conduction of electrons is enabled by applying a high voltage value to CG. In this bias configuration, no potential barrier is created in the CG region, and electrons are able to flow from source to drain (see Fig. 3.3d).

The device transfer characteristics are presented in Fig. 3.4 and show the polarity-controllable behavior of the fabricated DIG-SiNWFET. The device showed sub-threshold slope (SS) of 64 mV/dec with II_{ON}/I_{OFF} ratio of 10^6 for *p*-type conduction and SS of 70 mV/dec with I_{ON}/I_{OFF} ratio of 10^7 for *n*-type conduction in the same device.

3.1.2 Sub-Threshold Slope Control

Using the same gating configuration described in [123], we can also exploit the possibility of controlling the sub-threshold slope (SS) of the device and operate with sub-60 mV/dec sub-threshold swings [127]. This feature can be achieved by increasing the V_{DS} voltage in order to create enough electric field in the channel to trigger weak-impact ionization [128], and thanks to a positive-feedback mechanism provided by the potential well created by the CG region. This operation regime was first demonstrated on DIG-FETs in [127] using a DIG-FinFET device, but the same working principle is applicable to silicon-nanowires FETs.

The operation principle of the *n*-type device is depicted in Fig. 3.5a, with a schematic band-diagram of the device structure, and the same operation principle applies in the case of *p*-type operation. For *n*-type behavior, corresponding to a positive voltage ('1') applied to the PG, electrons are injected in the channel from the source contact. When

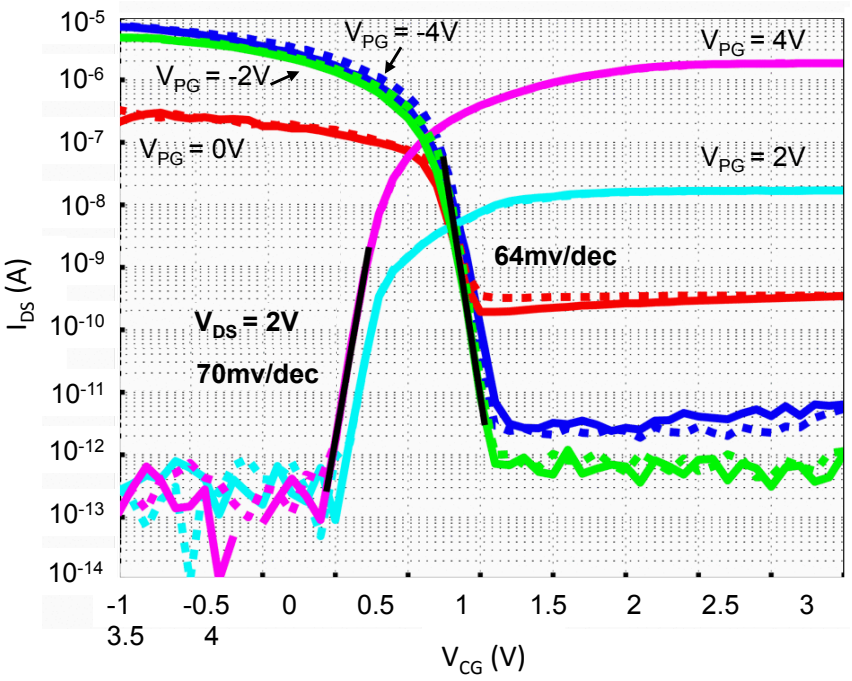


Figure 3.4 – Silicon-nanowires DIG-FET transfer characteristics. The curves are obtained at different bias voltage of the PG gate, sweeping the CG voltage. The device shows controllable unipolar behavior with subthreshold slopes for both n- and p-type conduction branches below 70mV/dec. I_{ON}/I_{OFF} ratios for both polarities are above 10^6. Adapted with permission from De Marchi *et al.* [123]. Copyright (2012) IEEE.

sweeping V_{CG} from logic '0' to logic '1', the full transition between OFF and ON state occurs when the threshold value V_{TH} is reached. At this point, electrons flowing in the channel gain enough energy to trigger weak-impact ionization, generating a larger number of electron-hole pairs, see step 1 in Fig. 3.5a. The generated electrons drift to the drain, thanks to the high electric field in the channel, while holes accumulate in the potential well induced by the CG in the central region of the channel (Fig. 3.5 step 2). A net positive charge is thus created in this region, which lowers the potential barrier in the channel, providing more electrons for the impact ionization process. A positive feedback mechanism is thus created: the generation of more electron/hole pairs leads to a greater amount of holes accumulating under the potential well which continue to lower the potential barrier providing even more electrons injected in the channel [129]. Parts of the generated holes are swept towards the source, increasing the hole density in the PG region at source and thinning the Schottky barrier at source even further. In the meantime the potential well under the CG gate is kept until the final ON state (Fig. 3.5 step 3). The positive feedback mechanism described ultimately enables the steep device turn-on as it is able to provide a faster modulation of the Schottky barriers at source and drain. The operation for p-type behavior is similar but for V_{PG} set to logic '0'. The positive feedback mechanism allows to break the theoretical limit of 60

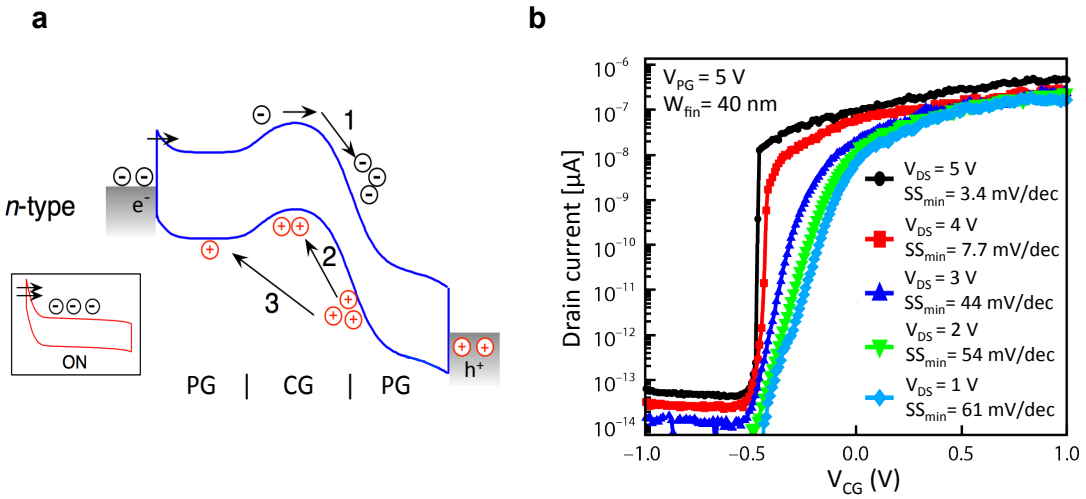


Figure 3.5 – Subthreshold-slope control mechanisms and experimental transfer characteristics. (a) band diagram of n-type behavior highlighting the main switching mechanisms. **(b)** transfer characteristics of the device in the sub-threshold control operation mode measured at different V_{DS} and at room temperature. Adapted with permission from Zhang *et al.* [127]. Copyright (2014) IEEE.

mV/dec subthreshold swing and, as shown in Fig. 3.5b, for $V_{DS} = 5\,\text{V}$ the minimum sub-threshold slope measured is 3.4 mV/dec and remains below 10 mV/dec over 5 decades of current. However further research on the operation principle and scaling of the device dimensions would be needed to reduce the V_{DS} necessary to achieve steep sub-threshold slope operation.

3.1.3 Threshold Voltage Control

Control over the threshold voltage (V_{TH}) of the device can be achieved thanks to the separate modulation of the two Schottky barriers at drain and source. To do so, each device has now three-independent-gates (TIG), namely polarity gate at source (PG_S), control gate (CG) and polarity gate at drain (PG_D) [130, 131], as depicted in Fig. 3.6. The experimental demonstration of dual-V_{TH} operation was done on TIG vertically-stacked SiNWFETs built with the same top-down process described in Sec. 3.1.1, with the only key difference that the two polarity gates were not connected together. It is straightforward to see that this device concept embeds the polarity-control function described in Sec. 3.1.1, which is achieved when the same voltage is applied on PG_S and PG_D. A total of eight operation modes are possible by independently biasing the three gates to either '0' (GND) or '1' (V_{DD}). We can identify two ON states, n- and p-type, two low-V_{TH} OFF states, two high-V_{TH} OFF states and two uncertain states which are not going to be used. Referring to the band-diagrams reported in Fig. 3.7, where all the relevant operation modes are depicted, we have:

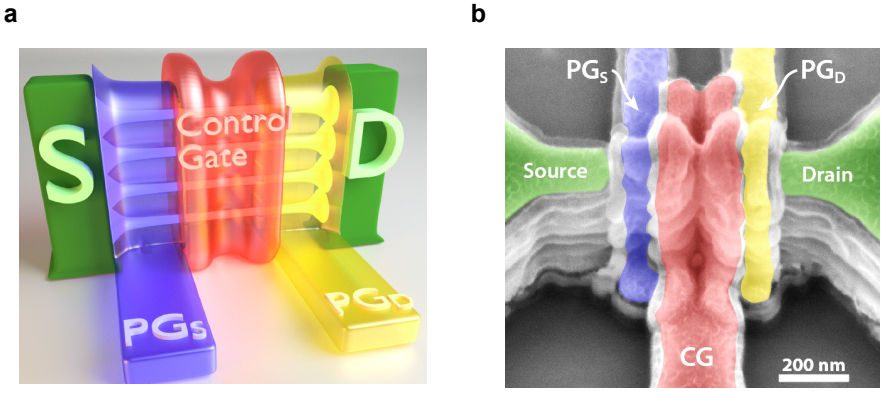


Figure 3.6 – Three-independent-gate FET. (a) Schematic structure of the device. **(b)** Tilted SEM view of the fabricated device, with gates and contacts marked. Adapted with permission from Zhang *et al.* [131]. Copyright (2014) IEEE.

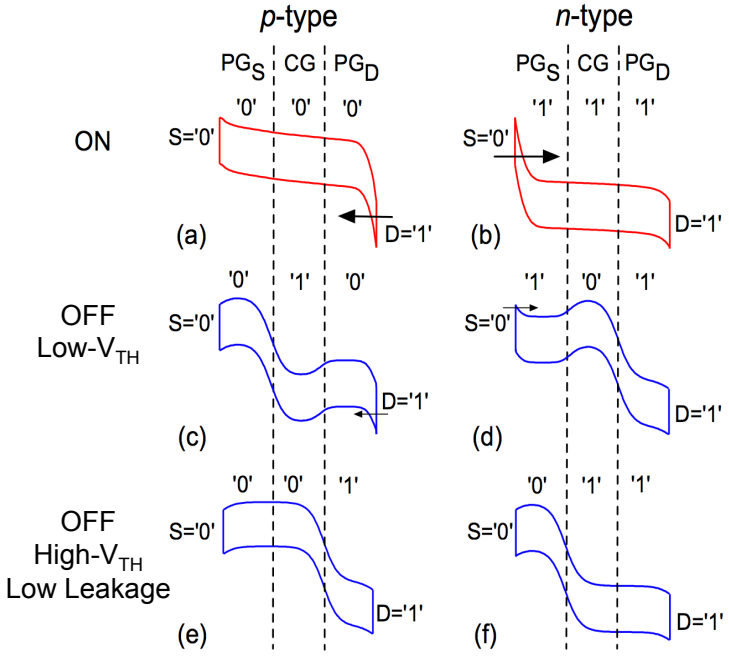


Figure 3.7 – Band diagrams relative to the 6 allowed operation modes for TIG-FETs. Adapted with permission from Zhang *et al.* [131]. Copyright (2014) IEEE.

1. ***ON states:*** As shown in Fig. 3.7(a,b), when $PG_S = PG_D = CG$, one of the Schottky barriers is thin enough to allow injections of holes from the drain (p-type) or of electrons from the source (n-type), and there is no potential barrier created by the CG. Remarkably, and in contrast to multi-threhsold CMOS devices, where the shift in threshold voltage is achieved by changing the channel doping, the ON state remains the same for both low- and high-V_{TH} operation mode.

2. ***Low-V_{TH} OFF states:*** Current flow is blocked by the potential barrier created

by the opposite biasing of the control gate with respect to the polarity gates (Fig. 3.7 (c,d)). However, the tunneling barrier at drain (p-type) or at source (n-type) is still thin enough to allow tunneling of carriers in the channel, and few of them can still be transmitted through the channel, thanks to thermionic emission over the potential barrier created by the CG. This OFF-state is identical to the one presented in Sec. 3.1.1 for the DIG-SiNWFET [123].

3. ***High-V_{TH} OFF states:*** As presented in Fig. 3.7 (e,f), this operation mode is characterized by the PG_S being kept at the same potential of the source contact and the PG_D at the same potential of the drain contact. The voltage applied to the CG discriminates between p-type OFF state (CG = '0') and n-type OFF state (CG = '1'). In this configuration, thick tunneling barriers at source and drain prevent carriers to be injected in the channel, lowering even more the current leakage. This OFF-state closely resembles the one presented in [121, 122].

4. ***Uncertain states:*** When PG_S = '1' and PG_D = '0', both barriers are thin enough for tunneling. However, this condition may also create an unexpected barrier in the inner region that will block the current flow, and cause signal degradation. Hence, the uncertain states should be prohibited by always fixing PG_D ='1' (PG_S ='0') for n-FET (p-FET), or using $PG_D = PG_S$.

The experimental transfer characteristics are shown in Fig. 3.8. Both p- and n-type behaviors with different threshold voltages (low-V_{TH} and high-V_{TH}) were observed in the same device. By extracting the threshold voltages at 1 nA drain current the threshold difference in p-FET configuration is 0.48 V and 0.86 V in n-FET configuration. As mentioned previously, the device ON-state is unchanged when switching from low- and high-V_{TH} and there is no degradation in the device ON-current, as can be appreciated in Fig. 3.8). This represents a competitive advantage for this technology, as the transistor is able to maintain the same current drive in both configurations.

3.2 Novel Materials for Polarity-Controllable Devices

Scaling of conventional silicon-based electronics is reaching its ultimate limit and the quest for a new material, with the potential to outperform silicon, is now open. Here, we focus on materials that have been proven to be adaptable for beyond-CMOS polarity-controllable electronics and show the most recent experimental results achieved by worldwide research groups. We did not include *Two-Dimensional* (2D)-TMDCs is this chapter as they are discussed in depth in Ch. 2.

3.2.1 Germanium Nanowires

Recently polarity-controllable behavior has been demonstrated on semiconducting Germanium nanowires [132] (see Fig. 3.9), with a device structure similar to the one of the

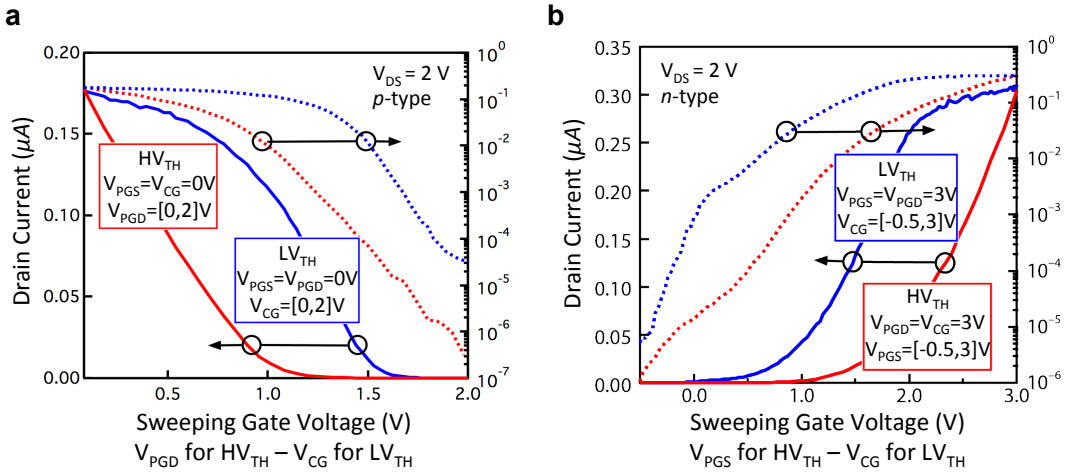


Figure 3.8 – Experimental transfer characteristics of the three-independent-gate device, showing the threshold-voltage control mode. (a) *p*-type transfer characteristics. **(b)** *n*-type transfer characteristics. The reader can appreciate how, for both *n*- and *p*-type operation, there is no current degradation in the device ON-state between the low- and high-V_{TH} mode. Adapted with permission from Zhang *et al.* [131]. Copyright (2014) IEEE.

RFET presented in 3.1. Germanium could be an appealing material for future electronic devices thanks to its superior hole mobility, but due to the low semiconducting band-gap of 0.66 eV typically suffers from high static power dissipation. The use of an additional polarity gate to control the Schottky barrier allows a superior control of the device OFF-state, with simulation showing the possibility of ultra-scaled Germanium nanowires devices with low leakage current and dynamic control of the transistor polarity.

3.2.2 Carbon Nanotubes

Since the modern rediscovery of *Carbon Nano-Tubes* (CNTs) in the early 1990s [133], [134], the field has experience a massive growth, and CNTs have been found to show promising performances and characteristics for a variety of applications, such as microelectronics, biotechnology and material science [135] [136]. For a more comprehensive treatment of carbon-based materials and devices, we refer the interested reader to the book by Wong and Akinwande [137].

CNT-FETs with Schottky metal contacts have been frequently reported in literature and their ambipolar switching behavior has been studied extensevely in litearture (see [138–140] for a in-depth review). Electrostatic doping was first used in CNTs to demonstrate tunable *p*-*n* junction diodes [141]. Researchers at IBM then exploited electrostatic doping for the realization of field-effect transistors with tunable polarity, using a double-independent gate (DIG) CNFET [142]. In the proposed DIG device structure, an aluminum back-gate is fabricated on a Si/SiO_2 substrate to act as the control gate and a

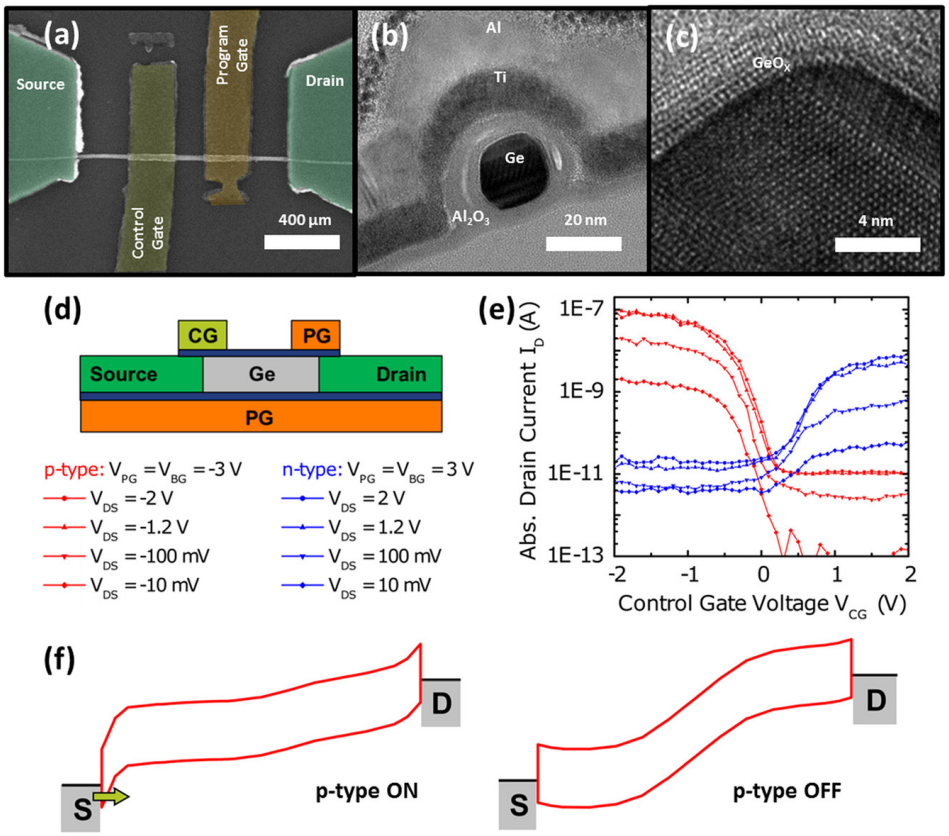


Figure 3.9 – Off-current leakage suppression and polarity control in a Germanium nanowire transistor. (a) Top-view *Scanning Electron Microscope* (SEM) image of a multigated germanium nanowire transistor. **(b)**Cross-sectional TEM image below one of the two top-gates. **(c)** *High-Resolution Trasmission Electron Microscope* (HRTEM)image of the channel region revealing a crystal lattice in the ⟨110⟩ direction and the presence of a sub-1-nm GeOX interface passivation layer. **(d)** Schematic device layout in longitudinal section and applied voltages employed for leakage current suppression and polarity control. Program-gates (PG) at front and back are coupled. **(e)** Unipolar I_{DS}˘V_{CG} transfer characteristics of *p*-type and *n*-type operation due to leakage current suppression. **(f)** Simulated band diagrams in the on-state (typical operation) and off-state (additional barrier near drain contact) of the *p*-type configuration. Barrier tunneling is indicated by an arrow. The *n*-type configuration band diagrams can be constructed in an analogous manner by simply reversing the respective band bending. Reprinted with permission from Trommer *et al.* [132] Copyright (2017) American Chemical Society.

single CNT is transferred on the substrate and aligned with respect to the pre-patterned gate. The silicon substrate acts as a polarity gate in the contact region, creating a gate configuration similar to the one presented in [123], where the polarity gate is acting simultaneously on the source and drain Schottky-barrier. The control-gate, placed in the central region of the channel, controls the ON/OFF state of the device, as shown in Fig. 3.10(a,b).

As previously discussed, Schottky-barrier undoped FETs are intrinsically ambipolar, as they permit to have conduction of both charge carriers. The additional PG allows to selectively choose the charge carriers that are injected in the channel. This effect is clearly shown by the comparison between the experimental transfer characteristics shown in Fig. 3.10c and 3.10d. When the PG bias (V_{gs-Si}) is set to be equal to the CG (V_{gs-Al}), the polarity control mechanism is not used, and the device shows its ambipolar behavior, see Fig. 3.10c. Instead when using PG as a second independent gate, the selection of the charge carriers can be used to create two separate unipolar behaviors on the same device, as shown in Fig. 3.10d. The device transfer characteristics obtained show low ON-current values, ∼3 nA for *p*-type and ∼0.1 nA for *n*-type behavior, with low current leakage (∼0.1 pA) for both polarities. The low ON-currents are a consequence of the reduced dimensionality of the CNT, and could be improved by placing multiple CNTs between the source and drain contact.

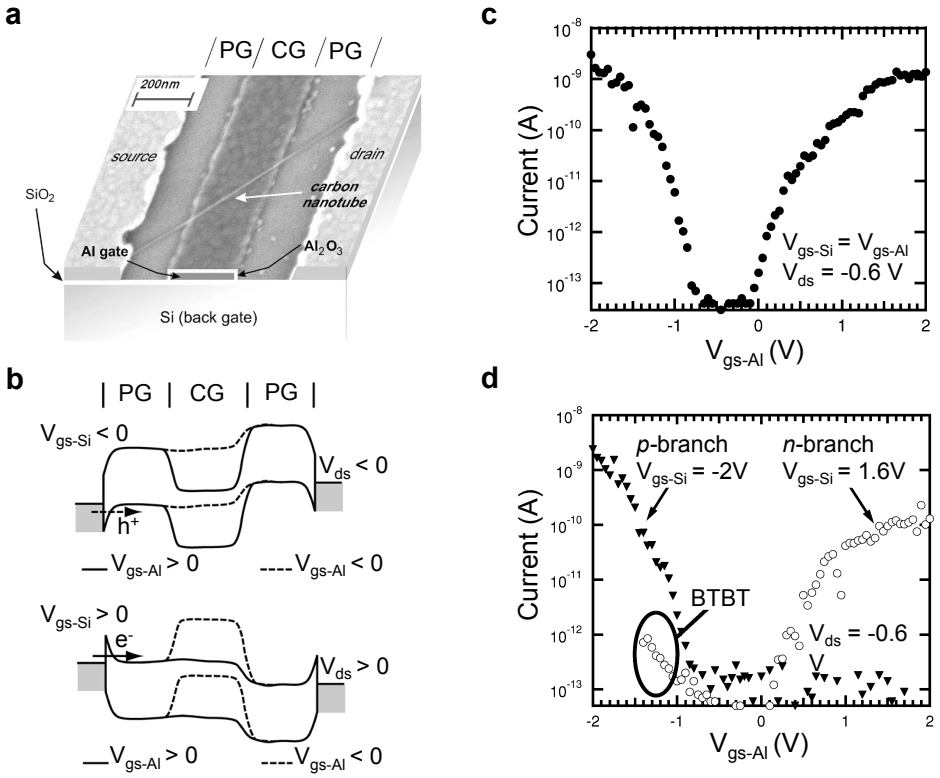


Figure 3.10 – Polarity control in carbon nanotubes FETs. (a) SEM view of the CNFET fabricated. **(b)** Schematic band-diagram of the different operation modes. **(c)** Ambipolar transfer characteristic measured without the use of the polarity gate. **(d)** Transfer characteristics of the same dual-gate CNFET exploiting the polarity-control mechanisms and showing clear *p*- and *n*-type unipolar behavior. *Band-to-Band Tunneling* (BTBT) can be observed in *n*-type operation mode for $V_{gs-Al} < -1V$. Adapted with permission from Lin *et al.* [142]. Copyright (2005) IEEE.

3.2.3 Graphene

Graphene is a 2D allotrope of carbon first discovered in 2004 by Geim and Novoselov at Manchester University [143]. Graphene has been used to realize polarity-controllable devices [144], but due to the absence of a semiconducting band-gap, it has been difficult to achieve low OFF-current and subsequently high ON/OFF current ratios. An improvement in the performances of graphene devices can come from managing to open a transport band-gap in graphene, which can be done either by fabricating nanoribbons [145, 146] or by chemical doping [147]. In [148, 149] a defect-induced bandgap was created in a graphene flake by helium ion-beam irradiation [150]. By using a structure with two independent top-gates, similar to what already described for silicon nanowires in Fig. 3.1(a,b), polarity-controllable behavior on the graphene FET was demonstrated (Fig. 3.11(c,d)). For both polarities the ON-currents are lower than 0.1 nA, indicating how the creation of the defect-induced band-gap causes an increased scattering rate in the channel, and destroys the conventional high mobility of graphene. Moreover the characteristics are measured at 200 K, indicating that behavior at room temperature might be even more degraded.

3.3 Circuit-Level Opportunities

This section is focused on logic gates and circuit design using polarity-controllable DIG-FETs, with the particular geometry presented in [123] (see Fig. 3.2 and 3.3) and described in depth in Sec. 3.1.1. The enhanced functionality of the devices will be addressed and it will be shown how they translate into innovative circuit-level opportunities. For further references on design with MIG devices and dual-threshold operation, presented in Sec. 3.1.3, interested readers can refer to the following articles [117, 151, 152].

Digital circuits based on polarity-controllable DIG-FETs can exploit both PG and CG as inputs, thereby enabling more expressive switching properties. Indeed, while a standard 3-terminal device behaves as a binary switch, the DIG-FET is a 4-terminal device, with the PG being the additional input (see Fig. 3.12a). According to the value of PG, the device abstraction can be either a p-MOS or a n-MOS device, as shown in Fig. 3.12b. The general switching properties of the single device can be regarded as a comparison driven switch, i.e. the DIG-FET compares the voltages applied at the two independent gates [123, 151], and when loaded implements an exclusive OR function (XOR), see Fig. 3.13. Indeed, when the transistor is not conducting, case B and C in Fig. 3.13(a,b) corresponding to opposite logic values of CG and PG, the output is kept at logic '1'. When the voltages on CG and PG have the same logic value, case A and D in Fig. 3.13(a,b), the transistor is conducting and the output voltage drops to logic '0'.

The unique switching properties of the device are the key for the realization of fully-complementary compact logic gates that can be used for the realization of digital circuits. Adopting a pass-transistor configuration, to avoid the threshold drop caused by the use of a n-(p-)type transistor as pull-up(-down), we can realize both unate (NAND) and

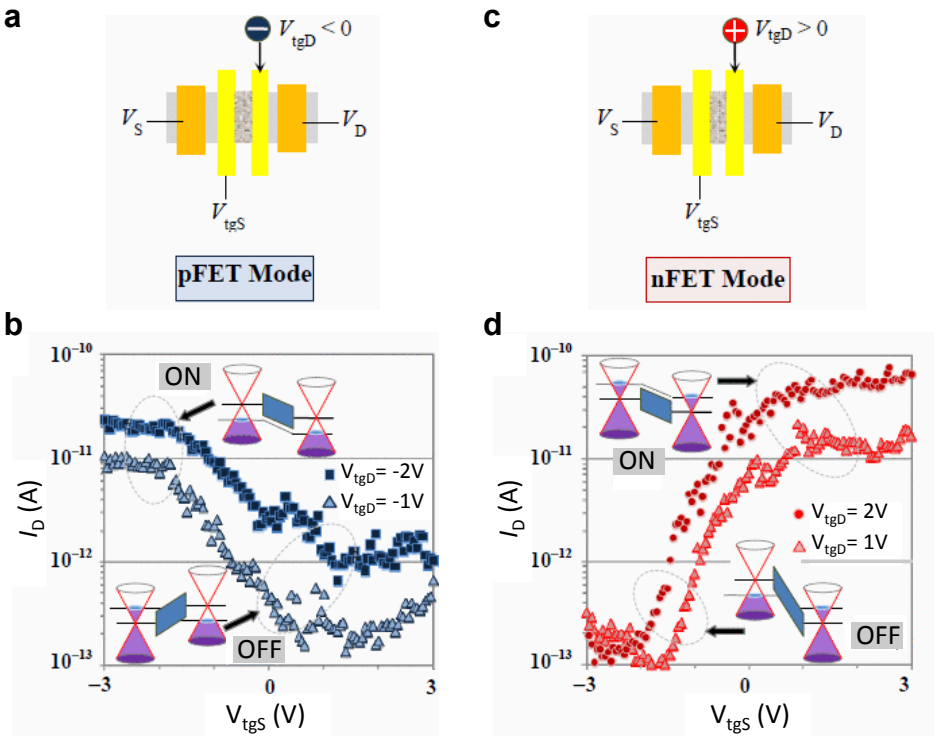


Figure 3.11 – Polarity-control in graphene FETs. **(a)** Schematic representation of the device and of the voltages applied at the terminals for *p*-type operation. **(b)** Transfer characteristics of the *p*-type operation mode with representation of the distribution of the charge-carriers at the contacts. The measurements were taken at 200 K and the applied V_{DS} was 200 mV. **(c)** Schematic depiction of the device and of the voltages applied at the terminals for *n*-type operation. **(d)** Transfer characteristics of the *n*-type operation mode with representation of the distribution of the charge-carriers at the contacts. The measurements were taken at 200 K and the applied V_{DS} was 200 mV. Adapted with permission from Nakaharai *et al.* [148]. Copyrigth (2012) IEEE.

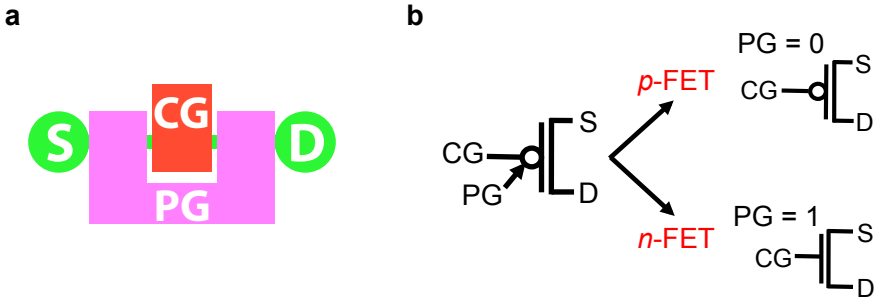
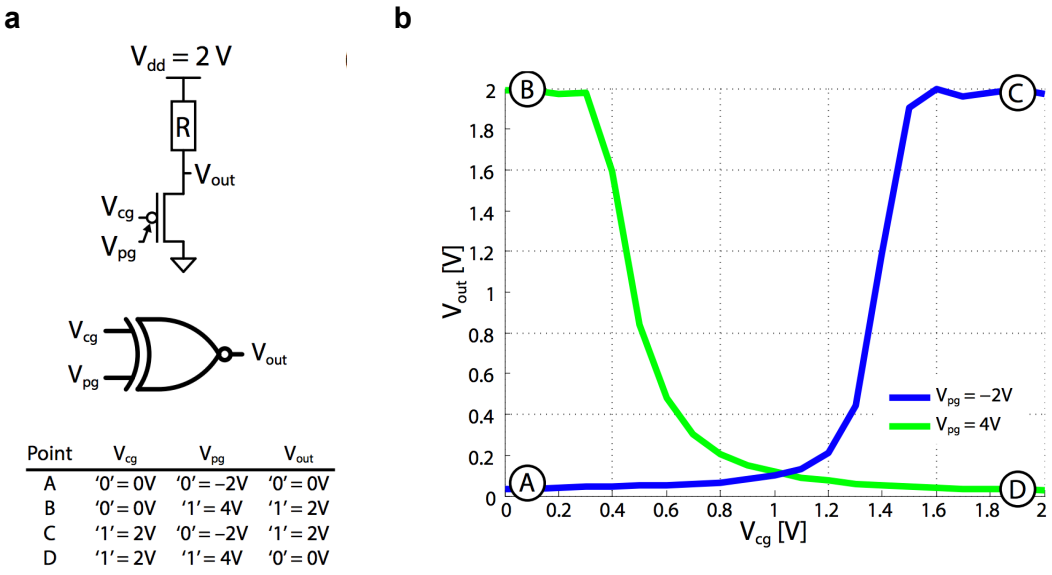


Figure 3.12 – DIG-FET circuit symbol and device abstraction. **(a)** Stick diagram of the DIG-FETs showing the 4 terminals. **(b)** Circuit symbol of the DIG-FETs and effect of PG gate on device behavior.



Point	V_{cg}	V_{pg}	V_{out}
A	'0' = 0V	'0' = −2V	'0' = 0V
B	'0' = 0V	'1' = 4V	'1' = 2V
C	'1' = 2V	'0' = −2V	'1' = 2V
D	'1' = 2V	'1' = 4V	'0' = 0V

Figure 3.13 – XOR behavior of the DIG-FET when loaded with resistor. (a) Circuit schematic of the loaded device, with logic-level abstraction and summary of the different bias points. **(b)** Experimental characteristic showing the XOR-behavior. Adapted with permission from De Marchi *et al.* [124]. Copyright (2014) IEEE.

binate functions (XOR), together with highly compact majority-gates, see Fig. 3.14. As it can be appreciated in 3.14a there is no real advantage in using DIG-FETs to realize unate functions such as NAND gates. In this case the polarity of the devices are set, polarity gates are not connected to any logic-input, and the number of transistor used, 4, is the same as in the standard CMOS realization of NAND gates.

As previously mentioned, the real advantage of DIG-FETs, can be appreciated in the implementation of binate functions, such as XOR, where both transistor gates can be used as logic inputs. Fig. 3.14b shows the efficient implementation of a XOR logic gate with only 4 DIG-FETs (in regular CMOS we would need 8 transistors), that will be used as the building block fro the implementation of XOR- and MAJ-rich circuits. Experimental demonstration of NAND and XOR logic gates realized using DIG-SiNWFETs [153] can be found in Fig. 3.15. It should be noted that in order to obtain fully cascadable logic-gates only positive gate voltages would be required to be applied to both CG and PG. To achieve this tuning of the process parameters would be needed to obtain the desired PG and CG thresholds. This problem could be addressed by applying strain to the nanowires or tuning the work-function of the metal-gate. The impact of this device concept on circuit and logic gates design does not only come from its peculiar switching properties, but also from the doping-free process that can be used for the realization of DIG-FETs. The great advantage in the realization of reconfigurable devices is that they eliminate the need to separate p- and n-type devices, i.e. in standard CMOS technology, p-type

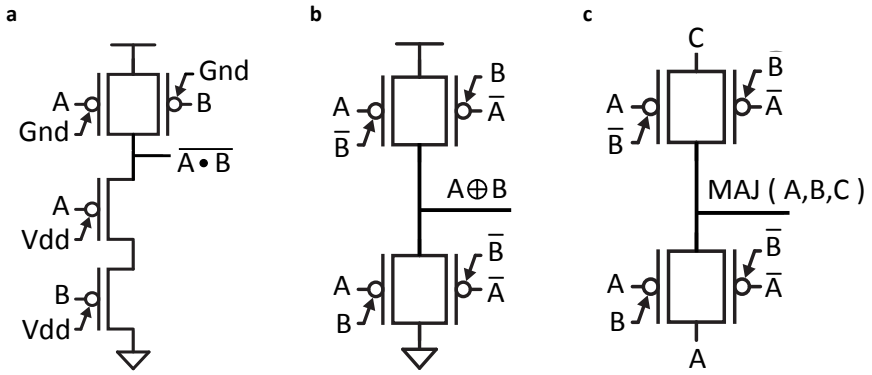


Figure 3.14 – Fully complementary logic gates with polarity-controllable SiNWs-FETs. (a) schematic for a NAND gate relaized using DIG-FETs. **(b)** Schematic of a fully-complementary 4-transistor *2-Input Exclusive OR* (XOR-2) gate realized with DIG-FETs. **(c)** Highly compact implementation of a *3-Input Majority* (MAJ-3) gate with only 4 DIG-FETs.

devices need to be realized on a n-doped region (n-well), opening alternative ways to place devices and allowing to achieve a much higher degree of regularity in the design of digital circuits [154, 155].

The observant reader might, at this point, have noticed that from a device-level perspective the additional polarity gate introduces larger parasitic capacitance and area consumption (a DIG-FETs is intrinsically larger than a conventional single-gate device). Thus, to unlock the full potential of DIG-FETs and ultimately achieve a higher computational density than CMOS technology, not only logic functions need to be re-designed, but also novel circuit synthesis techniques have to be developed [156]. Current logic-synthesis techniques derive from the abilities of CMOS technology, i.e. compact and efficient realization of NAND, NOR and, in general, unate inverting functions, and tend to be less effective in synthesizing XOR-rich circuits, such as arithmetic operators and data paths. The compact implementations of XOR and MAJ functions with DIG-FETs bear the promise for superior automated design of arithmetic circuits and datapaths. The influence of the additional PG on routing connections has also been explored, showing that thanks to the regularity of the devices, routing congestion can be avoided [155]. However, conventional logic synthesis tools are not adequate to take full advantage of the possibilities opened by controllable-polarity feature, as they are missing some optimization opportunities. To overcome these limitations, it is necessary to better integrate the efficient primitives of controllable-polarity FETs (XOR and MAJ) in the logic synthesis tools.

On the one hand, it is possible to propose innovations in the data representation form. For instance, biconditional binary decision diagrams (BBDDs) [157, 158] are a canonical logic representation form based on the biconditional (XOR) expansion. They provide a

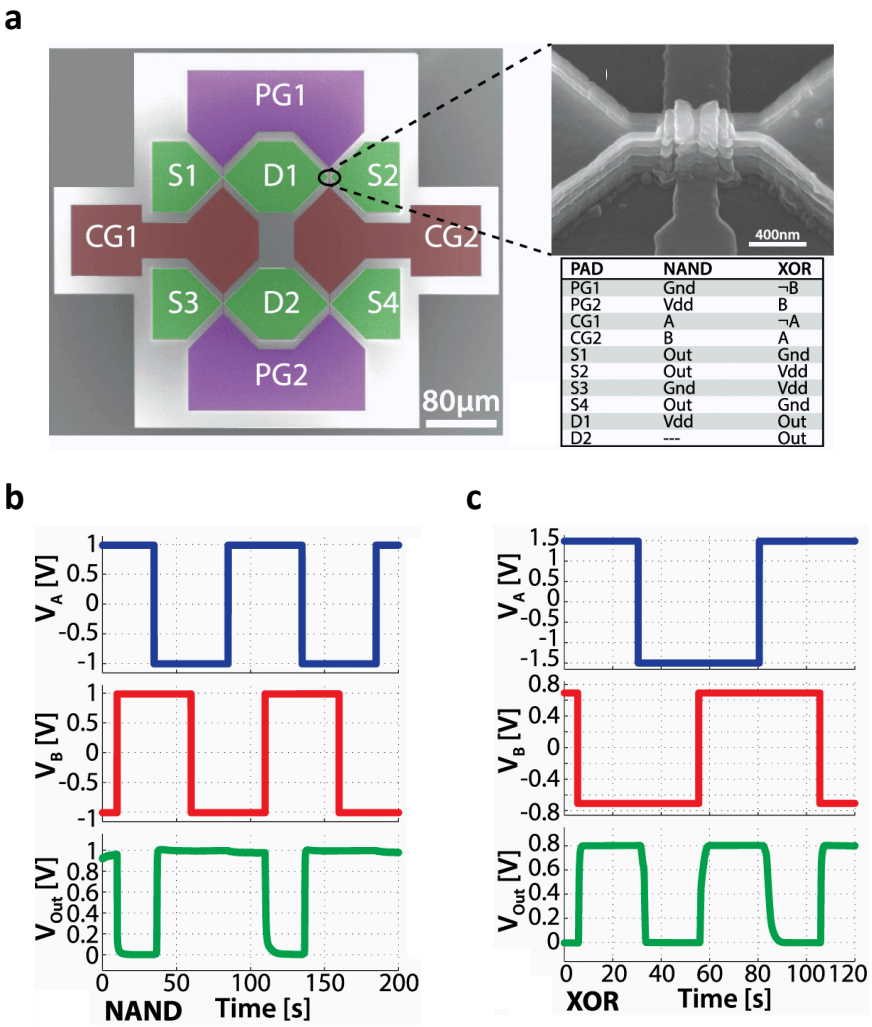


Figure 3.15 – Experimental demonstartion of NAND and XOR logic gates with DIG-FETs. **(a)** SEM micrograph of the fabricated devices with PAD names and zoomed view on the gated region of the transistor. The voltages applied to each PAD in both NAND and XOR operation are also listed. **(b)** Experimental characteristics showing NAND behavior. **(c)** Experimental behavior of XOR logic gate. Reprinted with permission from De Marchi *et a.* [153]. Copyrigth (2014) IEEE.

one-to-one correspondence between the functionality of a controllable-polarity transistors and its core expansion, thereby enabling an efficient mapping of the devices onto BBDD structures. On the other hand, it is also possible to identify the logic primitives efficiently realized by controllable-polarity FETs in existing data structures. In particular, BDD Decomposition System based on MAJority decomposition (BDS-MAJ) [159] is a logic optimization system driven by binary decision diagrams that supports integrated MUX, XOR, AND, OR and MAJ logic decompositions. Since it provides both XOR and MAJ decompositions, BDS-MAJ is an effective alternative to standard tools to synthesize

datapath circuits. In the controllable-polarity transistor context, BDS-MAJ natively and automatically highlights the efficient implementation of arithmetic gates. Finally, very efficient logic optimization can be directly performed on data structures supporting MAJ operator. In [160], a novel data structure, called *Majority-Inverter-Graph* (MIG), exploiting only MAJ and INV operators has been introduced. Such data structure is supported by an expressive Boolean algebra allowing for powerful logic optimization of both standard general logic as well as of arithmetic oriented logic. By applying these logic-synthesis techniques to various industry standard benchmark circuits, such as adders, multipliers, compressors and counters, an average improvement in both area (32%) and delay (38%), with respect to conventional CMOS technology,can be achieved using MIG-FETs [117] [161]. When combining 2D materials with the design possibilities enabled by MIG FETs it has been shown how for a 32-bit adder a $\sim 7\times$ *Energy-Delay Product* (EDP) gain can be achieved over conventional CMOS design at the same technology node [30]. Moreover the use of MIG FETs has been explored for a variety of circuit applications such as flip-flops [162], power-gating [163], multiplexers [164], hardware security [165] and novel memories [166, 167], showing the great flexibility of this class of devices.

3.4 Summary

This chapter was dedicated to functionality-enhanced devices in the form of multiple-independent-gate field effect transistors, which have been referred throughout as MIG-FETs. We aimed at giving a broad overlook of the field, and of the advantages that this technology could bring to future electronic-circuit design. We focused on experimental devices realized with different materials and structures, and showed how the device concept is flexible and adaptable to both silicon and novel emerging semiconductors. We purposely excluded experimental devices fabricated on 2D-TMDCs as they are addressed more in depth in the remainder of this thesis.

4 Polarity-Controllable WSe_2 FETs

A journey of a thousand miles begins with a single step

— Tao Te Ching,
Laozi

The main motivation behind the work conducted in this thesis is the development of a device concept, based on *Two-Dimensional* (2D) *Transition Metal Di-Chalcogenides* (TMDCs) materials, that would not require any physical or chemical doping, but still be able to achieve complementary behavior. In Ch. 2, we introduced the state-of-the-art for TMDCs materials, showing how the ambipolar property of certain materials can be exploited for the realization of un-doped devices. In Ch. 3, we presented the *Multiple-Independent-Gate* (MIG) structure that, starting from an ambipolar device, enables the dynamic control of its polarity by electrostatically tuning the Schottky barriers at source and drain. We also showed how the MIG structure can be applied to both silicon and other emerging materials. Building on these introductory chapters we transition now to the core part of this thesis and focus on the work conducted at IMEC on the fabrication and testing of proof-of-concept doping-free polarity-controllable *tungsten di-selenide* (WSe_2) transistors. We show how we exploited the ambipolar behaviour of WSe_2 to fabricate double-back-gate devices and to demonstrate, for the first time on WSe_2, the control of carrier injection by tuning the contact Schottky barriers with the additional *Polarity Gate* (PG). The device can be turned ON and OFF by gating the central channel region with a second gate, named *Control Gate* (CG), while the PG is able to control the device polarity without the need of changing metal contacts and without introducing any physical or chemical doping. The transistor polarity can thus be dynamically configured and the device abstraction at the logic level becomes a comparison-driven switch, with the device changing status only when the signals applied on CG and PG represent the same logic level.

This chapter is organized as follows. In Sec. 4.1 we describe the fabrication process developed at IMEC and then in Sec. 4.2 we focus on the steps needed to achieve a more

symmetric ambipolar operation. In Sec. 4.3 we experimentally demonstrate the control of carrier injection by tuning the contact Schottky barriers with the additional PG, and also show "on-the-fly" polarity-control by sweeping the PG and keeping the CG constant. Sec. 4.4 concludes with a brief summary. This chapter is largely based on the journal publication by Resta *et. al.* [28].

4.1 Fabrication Process

For our experiments we use WSe_2 flakes, prepared by mechanical exfoliation from commercially available synthetic crystal, provided by HQ-graphene, using a standard low-tack dicing tape. The flakes are exfoliated on 20 nm *silicon di-oxide* (SiO_2)/*silicon* (Si) substrates, which, thanks to the optimal surface roughness of the SiO_2 substrate (as low as 0.16 nm) allows the exfoliation of high-quality defect-free flakes. Thanks to the different optical contrast given by flakes with different thicknesses, we select thin flakes (4-8 nm) with optical inspection [168] , and further characterize them with *Atomic Force Microscope* (AFM) [169] measurements to determine the exact thickness and verify the absence of folds and cracks (see Appendix A). The thickness of the flake, extracted from the cutline shown in Fig. 4.1a, is presented in Fig. 4.1b.

In order to realize our double back-gated geometry the flake was transferred to a target substrate and aligned with respect to predefined buried features, which will be acting as the PG (Fig. 4.1c-d). The buried metal lines, and metal pads to contact them, are fabricated at IMEC on 300 mm wafers. The features are part of a lithography mask used for a variety of research applications, and occupy a small area of each fabricated chip (2×1 cm), which is replicated on the full 300 mm wafer. Starting from a bare heavily-doped silicon wafer, 200 nm of SiO_2 are deposited with a *Plasma-Enhanced Chemical Vapor Deposition* (PECVD) process at 480°C. The oxide is not thermally grown to avoid having to etch the backside of the wafer to be able to contact the silicon substrate during measurements. Then a *tantalum* (Ta) film (70 nm) is sputtered and patterned in the desired shapes with an anisotropic dry-etch step (Cl_2/CH_2F_2, 85/15 sccm at 5 mTorr and 70°C). During this step almost the entire surface of the wafer is left covered with Ta structures (dots in Fig. 4.2) to ensure a conformal result of the subsequent *Chemical Mechanical Polishing* (CMP) step. In Fig. 4.2 it can also be noted how the metal pads are hollowed, a very fine Ta grid is patterned on their area, in order to optimize the CMP process. After the Ta patterning the wafer is further handled with *Back-End-Of-the-Line* (BEOL) optimized process steps. These include oxide deposition to fill the etched areas between the Ta features and the CMP process to flatten the entire stack. At this point the final SiO_2 thickness is around 270 nm and the 300 mm wafer is diced into individual chips and made available to different users for further fabrication. The final process steps that we performed is the deposition of a gate oxide on top of the buried Ta structures and an etch step to properly contact the tantalum pads thought the deposited oxide. We use a commercial tool (*Atomic Layer Deposition*

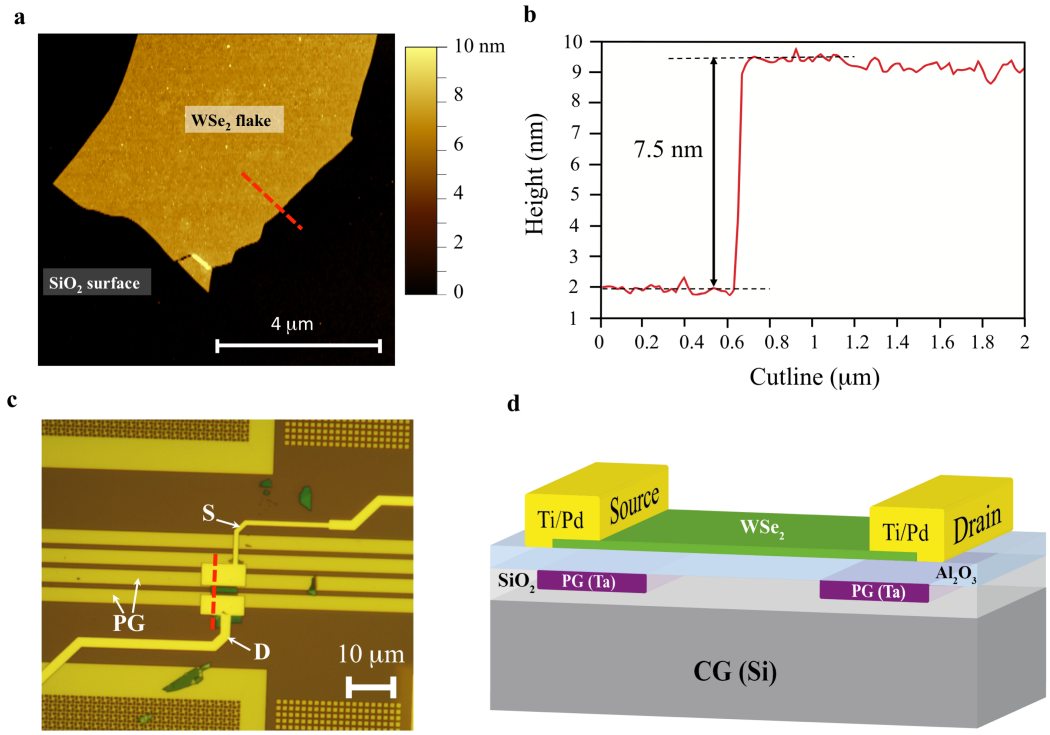


Figure 4.1 – WSe_2 flake properties and device fabrication. **(a)** AFM topography image of the exfoliated flake after cleaning of tape residues with hot 50° C acetone bath. The red line indicated the cutline used to extract the flake thickness. **(b)** Height profile for the cutline showed in a. The extracted flake thickness is 7.5 nm, which corresponds to around 10 monolayers. **(c)** Optical image of the realized device. The channel length, including all gated regions, is 1.5 µm long of which 1um is gated by the bulkSi acting as the CG and two 0.25 µm regions, near the contacts, are controlled by the buried program gate horizontal parallel metal lines marked as PG. The red dotted line indicated the cutline used to represent the device schematic. **(d)** 3D-schematic cross-section of the device along the red cutline in c. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

(ALD)-Savannah from Ultratech/Cambridge NanoTech) for ALD of 20 nm of *aluminium oxide* (Al_2O_3). The temperature of the ALD chamber is 150°C and the precursors used are *trimethylaluminium* (TMA) and *water* (H_2O). To etch the Al_2O_3 deposited on top of the PG metal we use *trimethylammonium hydroxide* (TMAH) based OPD 262 developer. The etching is carried out at room temperature for 10 min (etch-rate 2 nm/min), using only *polymethyl methacrylate* (PMMA) resist as a mask.

The flake is aligned with respect to the buried structures with a dry-transfer process developed in-house at IMEC, and described in Fig. 4.3. We use thick (10 µm) PMMA as transferring agent. After selecting the flake for transfer, PMMA is spin-coated on the

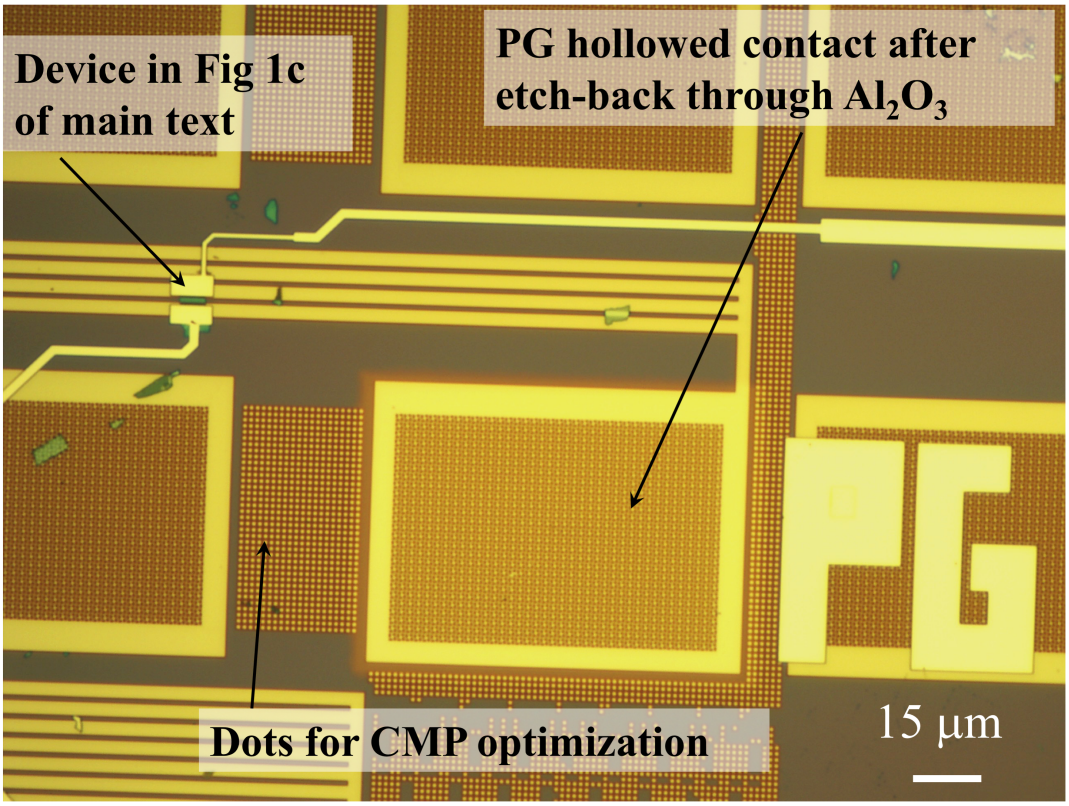


Figure 4.2 – Fabrication of buried features. The optical image shows a wider view of the fabricated device presented in the main text and highlights the Dots for CMP optimization and the hollowed metal contact for the PG gate. The optical image clearly shows the result of the etch step performed to open the PG pad. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

sample and annealed at 165°C on a hot-plate. The PMMA is then diced around the flake using a micro-engraver and, upon release of the WSe_2/PMMA stack, we pick it up using a micro-needle. The WSe_2/PMMA stack is then transferred to the target substrate and aligned with respect to the buried program gate by a manual pick-and-drop process. Adhesion of the WSe_2/PMMA stack is assured by 2 min hot-plate annealing at 190°C. Finally PMMA is dissolved using *di-chloro-methane* (DCM) and the sample is cleaned with an hot acetone bath (12 hours at 50°C) to ensure the absence of PMMA residues.

Metal contacts, *titanium* (Ti) (2 nm)/*palladium* (Pd) (50 nm), are defined by electron-beam lithography and lift-off. We use a single layer PMMA resist (solution with 3% Chlorobenzene). The resist is spinned for 60 seconds at 4500 rpm with a resulting layer thickness of around 180 nm. The resist is then baked on a hot-plate for 3 minutes at 165° C. After exposure the resist is developed in a 1:1 solution (at room temperature) of *methyl-isobutyl ketone* (MIBK) and *isopropyl alcohol* (IPA) for 55 seconds. Following the metal deposition, done with a commercial electron gun evaporator tool, lift-off is carried

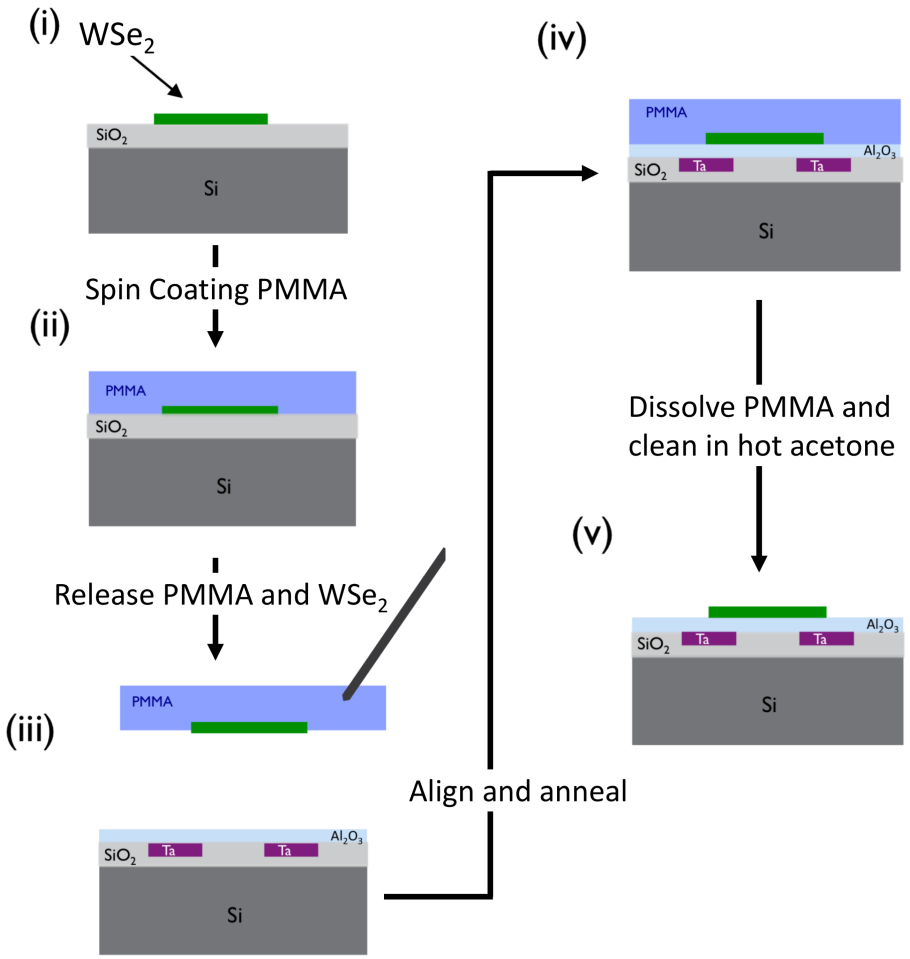


Figure 4.3 – Transfer procedure. Schematic of the transfer process developed at IMEC. This process allows to correctly position the WSe_2 flake with respect to the buried PG lines. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

out in hot acetone (50°C) for around 2 hours. The Ti layer is used only to improve the adhesion of Pd to SiO_2, while only the thicker Pd film determines the contact properties.

The final fabricated device is shown in Fig. 4.1c and a schematic cross-section respect to the cut-line in Fig. 4.1c is presented in Fig. 4.1d. The device has 1.5 µm channel length, of which 1 µm is gated by the bulk-Si (CG) and two regions near the contacts (0.25 µm) are controlled by the buried PG. The channel width is 5.5 µm. The thickness of the SiO_2 layer is 270 nm and the Al_2O_3 is 20 nm. The peculiar position of the flake with respect to the PG allows us to control the carrier concentration underneath the contacts by electrostatic doping, but also to gate a region of the channel. The PG can thus modulate the Schottky barrier at drain and source allowing for the selection of the carriers preferably injected in the channel. The bulk silicon wafer is used as CG to

create a potential barrier in the central region of the channel for either electrons or holes, according to the applied voltage polarity, and allows us to control the ON/OFF status of the device.

4.2 Achieving Ambipolarity

The flakes exfoliated on 20 nm SiO_2 are used to study contact properties and the effect of thermal annealing. All electrical measurements are performed at room temperature in *nitrogen* (N_2) environment using a Keithley 4200 *Semiconductor Characterization System* (SCS) with pre-amplifiers probe station. The current measurements are performed with auto-range setting allowing for highest accuracy (1% of reading + 10 fA) on OFF-current measurements. The voltage step for both V_{CG} and V_{PG} sweeps is fixed at 200 mV, and the gate leakage currents I_{CG} and I_{PG} are measured during all sweeps.

In our experiments, Ti/Pd-contacted WSe_2 *Field-Effect Transistors* (FETs) on SiO_2 dielectric substrate show a considerably higher electron current with respect to the hole current (100× difference), when measured after contact lift-off and without any additional treatment (Fig. 4.4a). This pronounced difference between the p- and n-type conduction properties is not ideal for the realization of polarity-controllable devices, as it will lead to asymmetric current-voltage ($I - V$) characteristics. Hence, we perform a contact annealing step, following what already reported in literature [170–174], in order to improve the ON-current levels. The devices are annealed at 200° C for 12 hours in a Nabetherm open-tube furnace, in vacuum with a constant *argon* (Ar) flow of 0.5 l/hr.

The effect of contact annealing is found to be reproducible and consistent, with an asymmetric increase of the ON-current levels and a decrease of the OFF-current (see Appendix B for additional measurements on different flakes). For the particular device presented in Fig. 4.4a, we obtain a 10× increase of the hole ON-current and a 4× decrease of the OFF-current, while the electron ON-current does not show a significant improvement. This behavior cannot be attributed to a Fermi level shift at the contacts, which results in a change of the Schottky barrier height, since such effect would increase the current for one type of carriers but reduce it for the other one by a similar amount. The increase in both n- and p-type currents suggests an improved physical contacts between the Ti/Pd contacts and the WSe_2 flake, possibly coupled with an improvement in the mobility of the charge carriers. This effect can result from removal of impurities (e.g. photoresist) and desorption of surface adsorbates (e.g water molecules) from the channel region [171–174]. The asymmetry in the improvement could point to an n-type doping of the channel by the impurities, which are then removed by the contact annealing. However, two-terminal measurements, such as those conducted in this study, obscure the intrinsic properties of the material and do not allow decoupling the decrease of contact resistance from an increase in the mobility of the charge carriers.

We perform the same contact annealing procedure on devices realized after transferring the flake to the Al_2O_3 substrate with the buried PG and we measure the full

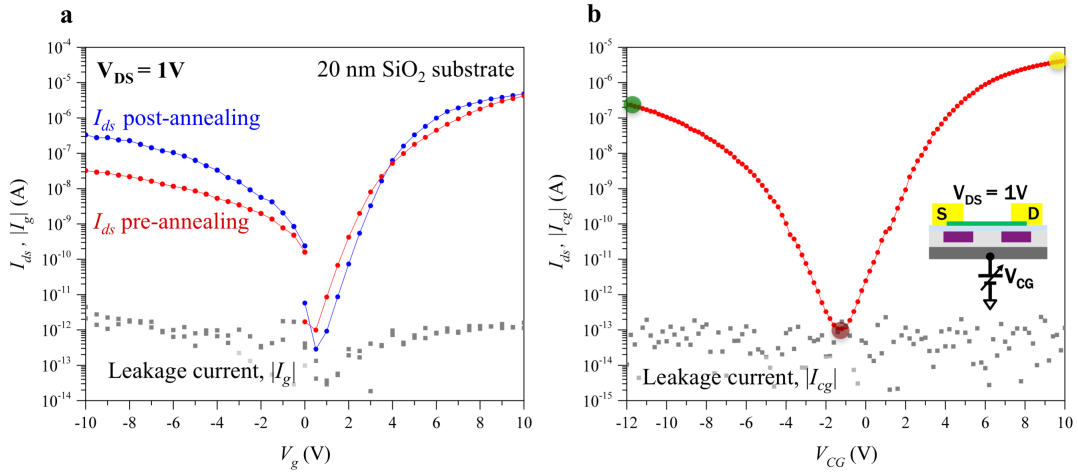


Figure 4.4 – Characterization of ambipolar behavior. (a) Transfer characteristics of a back-gates device fabricated with a 6 nm thick WSe_2 flake exfoliated on 20 nm SiO_2 substrate before and after annealing. The hole current is improved by 1 order of magnitude and the electron current remains unvaried. In this case, the positive and negative V_G sweeps are taken separately, thus the non-continuity of the curves at $V_G = 0$ V. Both curves were taken with $V_{DS} = 1$ V. **(b)** Transfer characteristic of the double-gate device presented in Fig. 4.1 measured with floating program gates. The device shows a ambipolar behaviour, with ON currents of 4 µA for electrons and of 0.25 µA for holes. The OFF current is well below the pA range (100 fA). The three colored dots mark the 3 operating regions in this configuration: OFF state (red), ON state n-type (yellow) and ON state p-type (green). The inset shows the electrical connections used during the measurement. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

back-gate transfer characteristics leaving the PG floating, thus no control of the Schottky barriers is used. Thanks to the annealing procedure we manage to reduce the asymmetry between p- and n-type conduction and achieve a more pronounced symmetry, with 15× difference in ON-current between the electron and hole branch (see Fig. 4.4b). The symmetric ambipolar behavior achieved is a key step towards the realization of polarity-controllable devices without the addition of any physical doping. Contact annealing and the effect of encapsulation in different oxides are further discussed in Appendix B and Appendix C.

4.3 Demonstration of Polarity-Controllable Behavior

Considering the ambipolar transfer characteristics presented in Fig. 4.4b, we now show how applying a voltage on the PG allows us to modulate the Schottky barriers at drain and source and to select the type of carriers (electrons or holes) that are favorably injected in the channel. For negative voltage values of the PG (Fig. 4.5a), we completely suppress electron injection in the channel and introduce local p-type electrostatic doping in the

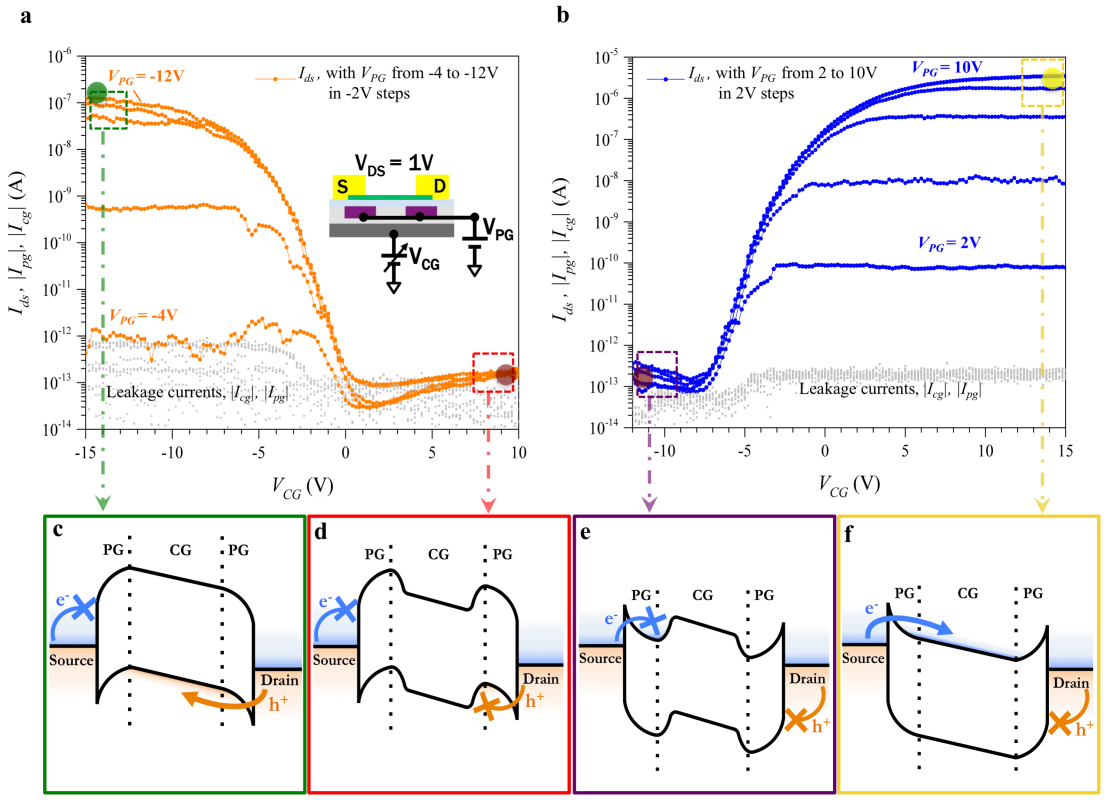


Figure 4.5 – Device transfer characteristics. (a,b) Transfer characteristics of the device obtained for different negative **(a)** and positive **(b)** voltage values applied to the PG as a function of the CG bias. The inset in **(a)** shows the connection used for the measurements. The dashed squares represent the 4 region of operation (ON *p*-type, OFF *p*-type, OFF *n*-type, ON *n*-type) of the transistor for which the corresponding band-diagram is shown in **(c–f)**. The transparent colored circles report the current values extracted from Fig. 4.4b and show how the current levels are not altered by the polarity-control mechanism. **(c–f)** Band-diagrams of the 4 regions of operation. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

contact regions. Further decreasing the PG applied voltage induces more positive charges and causes the effective Schottky barrier height to decrease (thinning of tunnelling barrier and thus increase tunnelling probability for holes). For the lowest negative applied voltage (-12 V in Fig. 4.5a) the ON/OFF-current levels are restored to the previous values extracted from the back-gate measurement with the PG floating. In a similar fashion, when applying a positive voltage to the PG, electrons are preferably injected in the channel and the hole current is completely suppressed for all negative voltages applied on the CG (Fig. 4.5b). Again we show that for the highest program gate applied voltage (10 V in Fig. 4.5b) the ON/OFF-current levels matches with the ones extracted in Fig. 4.4b. Schematic band-diagrams relative to the 4 operation modes of the device

are reported in Fig. 4.5c-f.

We achieve I_{ON}/I_{OFF} ratios of 10^7 for n-type operation and of 10^6 for p-type operation indicating an optimal electrostatic control on the channel for both carriers and the potential for low-power applications, thanks to the low leakage floor (off-current) measured in both configurations. As we mentioned, the ON-current levels corresponding to the highest applied PG values are comparable to the ones extracted from Fig. 4.4b.

In order to extract relevant parameters (such as carrier's mobility and sub-threshold slopes), we focus on the two curves taken at the highest positive and negative PG voltages (see Fig. 4.6). We estimate the extrinsic low-field-effect mobility using:

$$\mu = \frac{L}{W}\frac{1}{C_{ox}V_{ds}}\frac{\partial I_{ds}}{\partial V_{cg}}\bigg|_{V_{pg}=const.} \tag{4.1}$$

where L is the channel length (1.5 µm) , W is the channel width (5.5 µm), V_{ds} is the voltage applied to the contacts (1 V) and C_{ox} is the back-oxide capacitance per unit area, which is based on 270 nm of SiO_2 and 20 nm of Al_2O_3 for the back-gate (C_{ox}= 1.24· 10^{-4} F/m^2). The current derivative is taken with respect to the CG voltage, while the PG voltage is kept constant, i. e., setting the transistor polarity. Figure 4.6a shows the $I_{DS} - V_{CG}$ curve for n-type conduction in linear scale and highlights the linear low-field part of the characteristics where the mobility reaches its maximum value (the complete mobility curve is reported in Fig. 4.6b). Figure 4.6c-d show similar curves for p-type conduction. The maximum extrinsic low-field mobility measured for electrons (μ_e) is 5.5 cm2V^{-1}s^{-1} and 0.23 cm2V^{-1}s^{-1} for holes (μ_h). These values are smaller than those reported in literature for WSe_2 [175, 176] and we attribute this discrepancy to the presence of large Schottky barriers at the contacts, the lack of high-κ passivation and the presence of interface charges at the Al_2O_3/WSe_2 interface, that increase the scattering in the channel. The presence of interface charges is also reflected by the values of sub-threshold swing (S factor) extracted from the measurements. We computed an S factor of 0.875 V/dec over 4 decades of current for n-type conduction and of 0.92 V/dec over 3 decades of current for p-type conduction. These values could be greatly improved by reducing the gate-oxide thickness (switching to a top-gated structure) and by increasing the interface quality between the 2-D material and the dielectric substrate.

Moreover, from Fig. 4.6a,c, we can also extract the threshold voltage (V_{TH}) values by looking at the intercept between the tangent to the curve in the linear regime and the x-axis. For electrons, we estimated V_{TH} = 0.5 V while for holes we have V_{TH} = -5.1 V. In order to have an operational digital circuit, based on polarity-controllable devices, the two threshold voltages should be matching and this could be achieved by reducing the oxide thickness and tuning the V_{TH} by selecting a metal-gate with the appropriate work-function.

We also measure the $I_{DS} - V_{DS}$ characteristics (as shown in Fig. 4.7) by fixing the bias of the PG (10 V for n-type and -17 V for p-type) and changing the CG applied

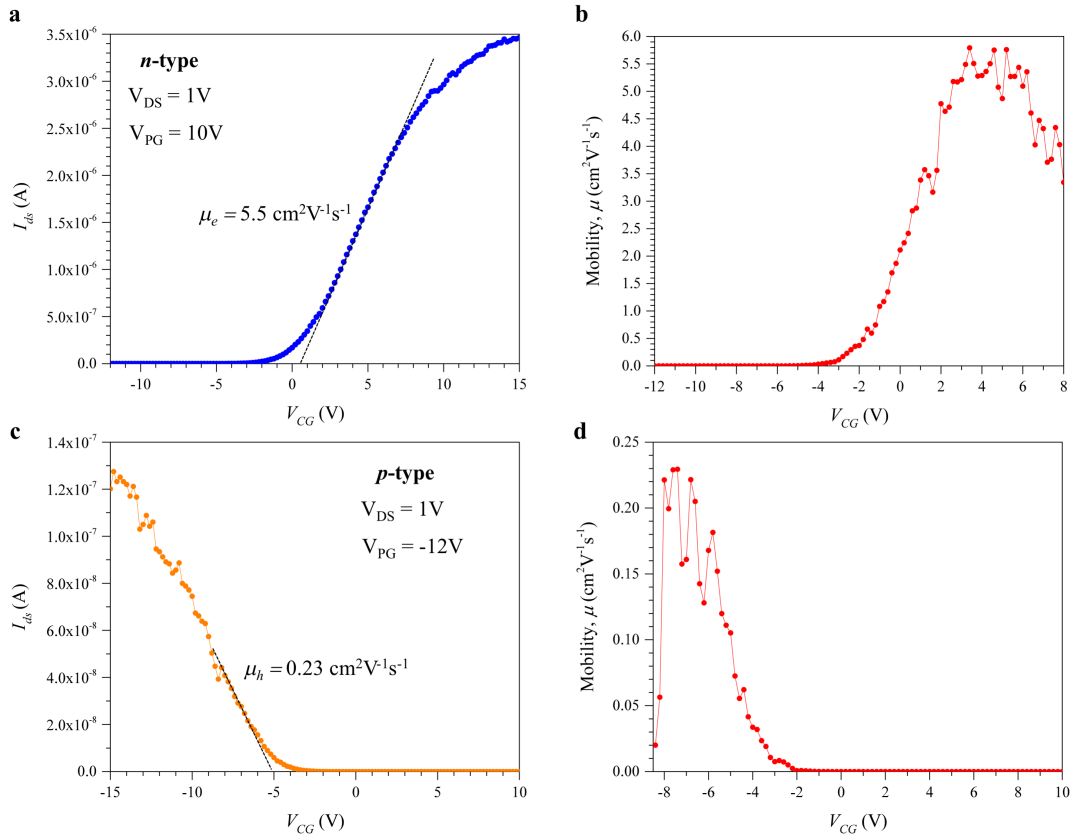


Figure 4.6 – Mobility Extraction. Linear $I_{DS} - V_{CG}$ characteristics for PG = 10 V **(a)**and PG = -12 V **(c)**. **(b)** and **(d)** show the extracted mobility curves respectively for n- and p-type conduction. For both conduction we can see mobility saturation, with the highest value reported in **(a)** and **(c)**. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

voltage to acquire the different curves. It should be pointed out that the $I_{DS} - V_{DS}$ characteristics are convoluted by the voltage drops across the source and drain Schottky barriers, one of which is forward-biased, and the other reverse-biased. The effects of these voltage drops are evident especially in Fig. 4.7a where there is significant non-linearity in the output characteristics close to $V_{DS} = 0$ (typical of Schottky contacts). Also, though we observe saturation in the $I_{DS} - V_{DS}$ characteristics for n-type (Fig. 4.7a), and more so for p-type conduction (Fig. 4.7b), it is difficult to conclude if these represent true pinch-off of the channel, since saturation of I_{DS} might also come from the reverse-biased Schottky junction. The noise in the output characteristics of Fig. 4.7b might be due to factors such as charge trapping in the channel or in the dielectric (which can lead to shifts in the device threshold, and might explain the relatively low current levels, if compared to the ones in Fig. 4.5).

We further characterize the switching properties of the device by sweeping the PG while fixing the value of the CG (as shown in Fig. 4.8). In this configuration the

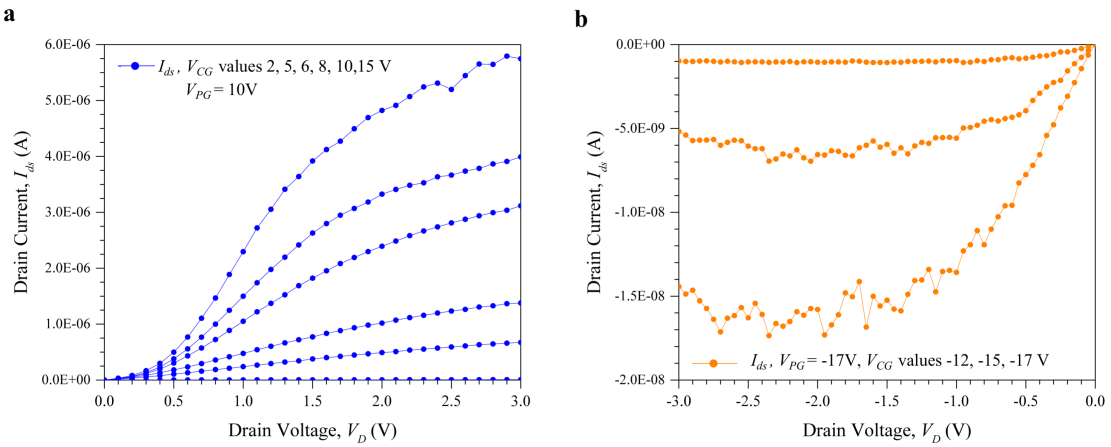


Figure 4.7 – $I_{DS}-V_{DS}$ characteristics for n-type conduction **(a)** and p-type conduction **(b)**. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

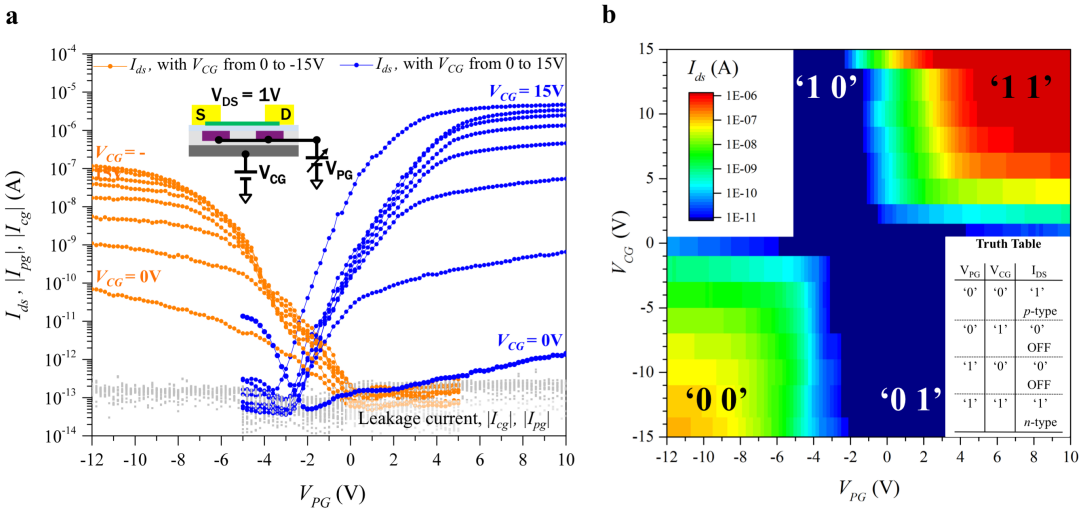


Figure 4.8 – Polarity change "on-the-fly" and XOR behaviour. (a) Transfer characteristics obtained for fixed values of the control gate bias and sweeping the program gate voltage. We can see how for $V_{CG} = 0$ V the device shows its OFF-state ambipolar behaviour by conducting both electrons and holes, according to the value of V_{PG}. The inset shows the measurement configuration. (b) 3D view of the device switching properties, highlighting the XOR operation based on the values of the program and control gates. The inset shows the truth table of the pseudo-logic function implemented. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

polarity of the transistor is changed during each sweep showing the ability of the device to transit from a p- to n-type behaviour, or vice-versa, in the same measurement, thus demonstrating "on-the-fly" polarity transition. To further understand the impact of this novel device concept on circuit design we look more closely at its switching properties.

While a standard 3-terminal device acts as a binary switch, our device compares two values (voltages applied on PG and CG) and when loaded implements an *Exclusive-OR* (XOR) function (see Fig. 4.8b). Indeed, when the transistor is not conducting, in the '01' and '10' cases, then no current would be flowing in the device leaving the output to '1' (high). When the values of PG and CG have the same logic value, both high or both low, then the transistor is conducting and the output of the logic gate would be '0' (low) (see Fig. 4.8b inset). The comparison-driven switching property of our device can be exploited at a circuit level because it gives the possibility of realizing logic gates (e.g. XOR, majority gates) with fewer transistors as compared to conventional CMOS, as will be shown in Ch. 5.

The same switching characteristics and polarity-controllable behavior are also measured on a second device as shown in Fig. 4.9.

4.4 Summary

In this chapter, we show the first polarity-controllable device realized with few-layer WSe_2, using a double-back-gate geometry. We operate our device with fixed polarity, by setting the program gate voltage to either positive or negative values, and we also demonstrated "on-the-fly" polarity control in 2D devices showing a p-to-n or *vice-versa* transition during the same measurement sweep. We achieved high I_{ON}/I_{OFF} ratios for both n-type (10^7) and p-type (10^6) operation modes. This work represents a major step on the path to exploiting the full potential of this technology for the realization of novel digital circuits with dynamically controllable polarity gates in WSe_2 flatronics, and it provides the basis for the realization the doping-free logic gates that are shown in the following chapter.

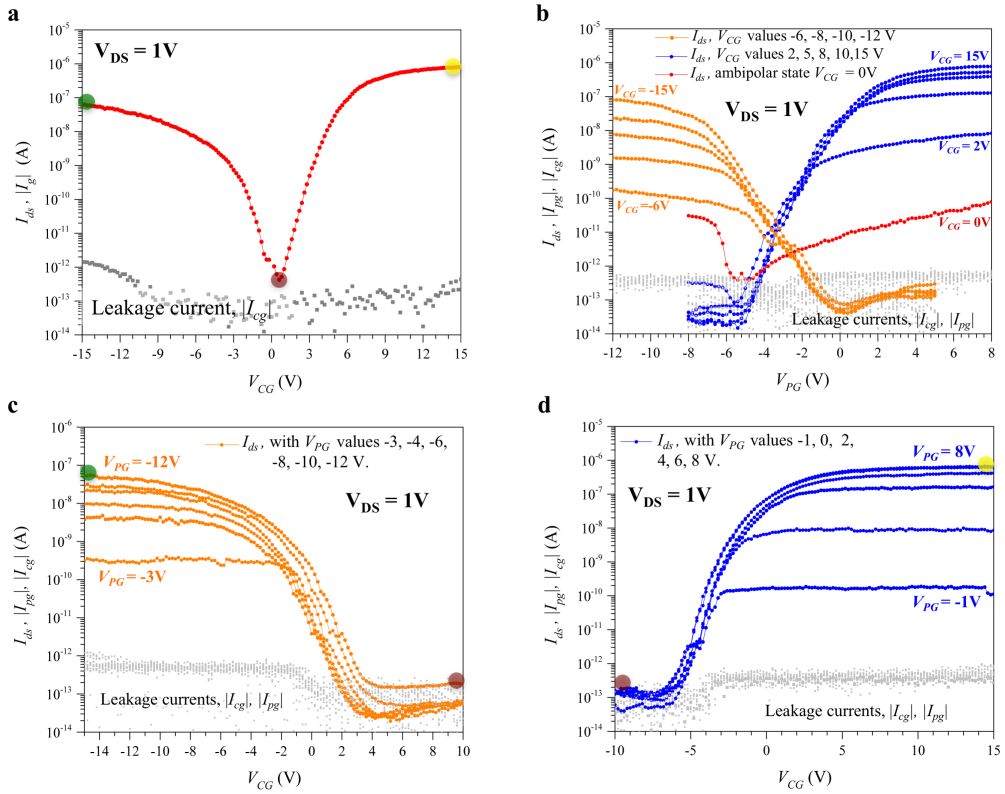


Figure 4.9 – Additional device characteristics. **(a)** Transfer characteristic obtained with PG floating. The device shows a good ambipolar behaviour, with ON currents of 0.8 µA for electrons and of 65 nA for holes. The off-current is below the pA range (400 fA). The three colored dots mark the 3 operation regions in this configuration: OFF state (red), ON state n-type (yellow) and ON state p-type (green). **(b)** Transfer characteristics obtained for fixed values of the control gate bias and sweeping the program gate voltage. We can see how for $V_{CG} = 0$ the device shows its OFF-state ambipolar behaviour by conducting both electrons and holes, according to the value of V_{PG} (red curve). **(c, d)** Transfer characteristics of the device obtained for different negative **(c)** and positive **(d)** voltage values applied to the program gate as a function of the control gate bias. The transparent colored circles report the current values extracted from **(a)**, and show how the current levels are not altered by the polarity-control mechanism. The I_{ON}/I_{OFF} current ratio is 10^7 for electron and 10^6 for hole conduction. Reproduced with permission from Resta *et al.* [28]. Copyright (2016) Nature publishing group.

5 Doping-Free WSe_2 Logic Gates

Ever tried. Ever failed. No matter.
Try Again. Fail again. Fail better.

— Worstward Ho,
Samuel Barclay Beckett

In the previous chapter we focused on the first experimental demonstration of a proof-of-concept polarity-controllable device fabricated on *tungsten di-selenide* (WSe_2). The single devices were fabricated on a wafer with pre-patterned tantalum metal lines, that were used as *Polarity Gate* (PG), while the entire silicon wafer was acting as the *Control Gate* (CG). In order to demonstrate the operation of doping-free logic gates fabricated with polarity-controllable devices, a new process needs to be developed, that would allow to individually control each CG and avoid using the global silicon back-gate. Our aim is also to enable operation of the devices at a lower voltage bias and achieve p-type operation for the PG biased at *Ground* (GND). Due to the challenges encountered when trying to encapsulate the devices, see Appendix C, we still adopted a double back-gate geometry, leaving the WSe_2 not encapsulated, and using no top-gated structure. This chapter is dedicated to first demonstration of fabricated, fully functional doping-free logic gates exploiting the device concept introduced in Ch. 4. We fabricate and characterize a variety of polarity-controllable logic gates such as *Inverter* (INV), *NOT-AND* (NAND) and *NOT-OR* (NOR) gates, that are the building primitives used in the logic synthesis frameworks for conventional *Complementary Metal-Oxide-Semiconductor* (CMOS) logic. Moreover, we experimentally show *2-Input Exclusive OR* (XOR-2), *3-Input Exclusive OR* (XOR-3), and *3-Input Majority* (MAJ-3) gates that, thanks to the polarity-controllable devices, can be realized with fewer transistors than what is achievable in conventional CMOS. We demonstrate a complete standard cell library with the possibility of fabricating compact, highly-expressive logic gates that can be exploited to gain advantages at circuit level, through exploiting matched logic synthesis techniques [157, 160, 177, 178].

This chapter is organized as follows. In Sec. 5.1 we describe in detail the new fabrication process developed to enable the fabrication of the logic gates and focus on the

design regularity enabled by polarity-controllable devices. We then focus on the single transistor and in Sec. 5.2 show the characterization of the switching properties. In Sec. 5.3 we describe the characterization of the fabricated logic gates. Finally we conclude in Sec. 5.4 with a brief summary. This chapter is largely based on the journal publication by Resta *et. al.* [33].

5.1 Fabrication of Logic Gates

For our experiments, we use WSe_2 flakes prepared by mechanical exfoliation from commercially available bulk crystals. The flakes are exfoliated on a Si/*silicon di-oxide* (SiO_2) substrate and then transferred (see Sec. 4.1 Fig. 4.3) on a target substrate with pre-patterned back-gates (2 nm Ti/10 nm Pt) isolated with *zirconium di-oxide* (ZrO_2) deposited by *Atomic Layer Deposition* (ALD). The fabrication process of the back-gates is depicted in Fig. 5.1. We use a double-layer resist consisting of *Lift-Off Resist 1A* (LOR1A) and *polymethyl methacrylate* (PMMA) resist (solution with 3% chlorobenzene) for the patterning of the CG buried gate Fig. 5.1i. The LOR1A is spinned for 45 s at 4500 rpm and subsequently baked on a hot plate for 5 min at 190° C. The PMMA layer is then spinned for 45 s at 4500 rpm and then baked on a hot plate for 5 min at 120°C. After exposure, the PMMA resist is developed in a 1:1 solution (at 20° C) of *methyl-isobutyl ketone* (MIBK) and *isopropyl alcohol* (IPA) for 42 s. The LOR1A is developed with a 3 s dip in *tetramethylammonium hydroxide* (OPD5262) followed by rinsing in deionized water. After the gate metal deposition (2 nm *titanium* (Ti)/10 nm *platinum* (Pt)), done with a commercial electron gun evaporator tool, lift-off is carried out in hot acetone (50°C) for around 2 hours. The remaining LOR1A resist is then removed in OPD5262. High-κ ZrO_2 (10 nm) is deposited with atomic layer deposition at 250° C using an AMAT Centura III–V module with *tetrakis(ethylmethylamino)zirconium* (TEMAZ)/*water* (H_2O) precursor and then the PG structures are defined with the same process described for CG (Fig. 5.1ii). The PG structures are isolated from the flake with High-κ ZrO_2 (10 or 20 nm), and the flake is then transferred on top of the buried structures (Fig. 5.1iii). We use a single-layer PMMA recipe for the pattering of the metal contacts, in order to avoid exposure of the *Two-Dimensional* (2D) material to OPD5262 (LOR1A developer) and water. The source and drain contacts (2 nm glsTi/50 nm*palladium* (Pd)) are then evaporated with a commercial electron gun evaporator tool, and create the appropriate connections for each logic gate (see 5.1iv,v). The Ti is directly in contact with the WSe_2 and acts as an adhesion layer between the 2D flake and the Pd. An annealing step is then performed at 200° C for 12 h in a Nabetherm open-tube furnace in vacuum with a constant *argon* (Ar) flow of 0.5 l/h.

5.1.1 Design Regularity

As already mentioned, the addition of the PG enables us to use a single semiconducting material for the realization of both *n*- and *p*-type transistors, without the addition of phys-

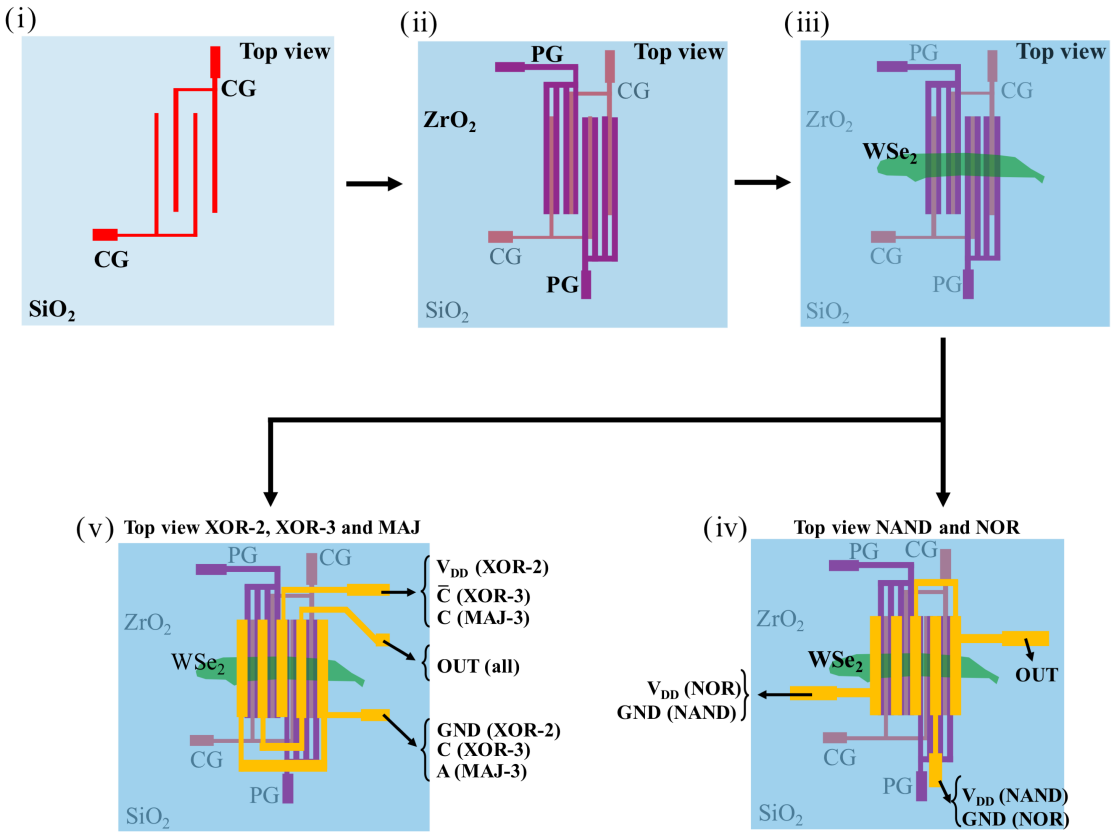


Figure 5.1 – Detailed fabrication process. Schematic of the fabrication process developed at IMEC. **(i)** Patterning of CG gates on a SiO_2 blanket. **(ii)** Isolation with ZrO_2, deposited with ALD, and patterning of the PG gates. **(iii)** Isolation with ZrO_2, deposited with ALD, and transfer of the WSe_2 flake on top of the gate structures. **(iv)** Generic structure for NAND and NOR gates after contact deposition. **(v)** Generic structure for XOR-2, XOR-3 and MAJ-3 gates after contact deposition. Reproduced with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

ical or chemical doping. This is a great advantage because the latter greatly complicates the fabrication process often making it non-scalable and non-CMOS compatible.

Fig. 5.2a shows a cartoon schematic of a 4-transistor XOR-2, with an optical micrograph of the fabricated device and the corresponding circuit schematic presented in Fig. 5.2b. Each transistor has now two independent gates that can be biased with different logic inputs (e.g., CG (A) is a control gate biased with logic input A and PG (B) is a polarity gate biased with logic value B). The design of the CG and PG was chosen in order to allow the use of a single WSe_2 flake for the fabrication of each logic gate. Moreover, the PG and CG structures are identical for all the fabricated logic gates (except for the inverter design), creating a universal gating structure, that enables a highly regular and flexible design of the logic gates. In fact, different logic gates can be obtained from the same gating structure by wiring differently the source and drain

contacts of the transistors (see Fig. 5.1). The fabricated logic gates (NAND, NOR, XOR-2, XOR-3 and MAJ-3) have 4 polarity-controllable transistors (except for the INV which has 2) that share the same semiconducting WSe_2 flake, but behave with opposite polarities according to the bias applied to the respective PG.

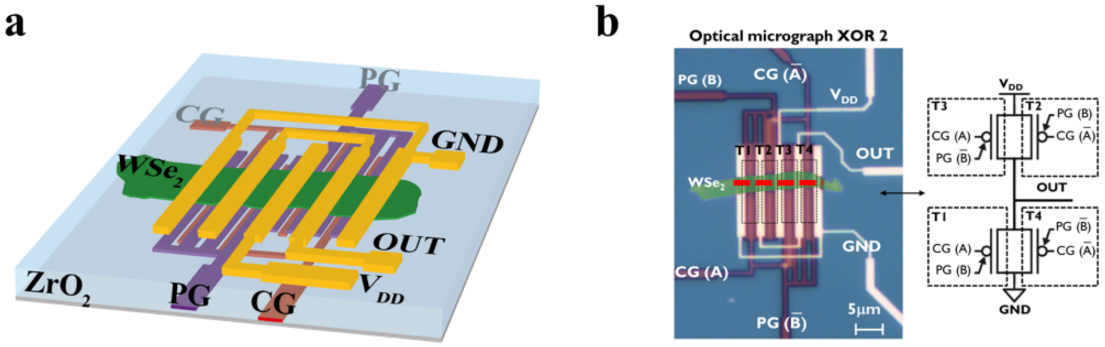


Figure 5.2 – 2D-WSe_2 polarity-controllable two-input XOR (a) Cartoon of the WSe_2 XOR-2 logic gate with platinum buried gates (CG and PG) and Ti / Pd contacts. **(b)** Optical micrograph of the fabricated XOR-2 gate, with corresponding circuit schematic highlighting the position of the four transistors and the logic inputs acting on them. The red dashed line indicates the position where the HRTEM cross sections presented in Fig. 5.3 are taken. Adapted with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

5.2 Device Characterization

Before showing the characterization of the fabricated logic-gates we analyze the structure and behavior of a single device, comparing it to the one presented in Ch. 4.

5.2.1 Physical Characterization

The *High-Resolution Trasmission Electron Microscope* (HRTEM) cross section taken at the contact interface, see Fig. 5.3a, shows the PG buried structure isolated by ZrO_2, with the 2D-WSe_2 flake on top and the Pd contact. *Energy-Disperse X-ray* (EDX) spectroscopy confirms the elemental composition of the device. Fig. 5.3b focuses in the central region of the channel and shows the separation (∼60 nm) and ZrO_2 isolation, between the CG and the PG structures. The atomic layers of the 2D-WSe_2 are clearly visible in the zoomed views of Fig. 5.3a,b and the thickness of the transferred flake can be estimated around 6 nm. Note that the EDX mapping for *selenium* (Se) and *tungsten* (W) (Fig. 5.3a also shows a false signal due to the overlap between the Se, W, and Pt peaks used during the measurements. Se and W are present only in the top 2D layer. The white region between the ZrO_2 and the WSe_2 in Fig. 5.3b is empty space, as confirmed by the lack of C atoms in the region (see Fig. 5.4). It is probably caused by partial

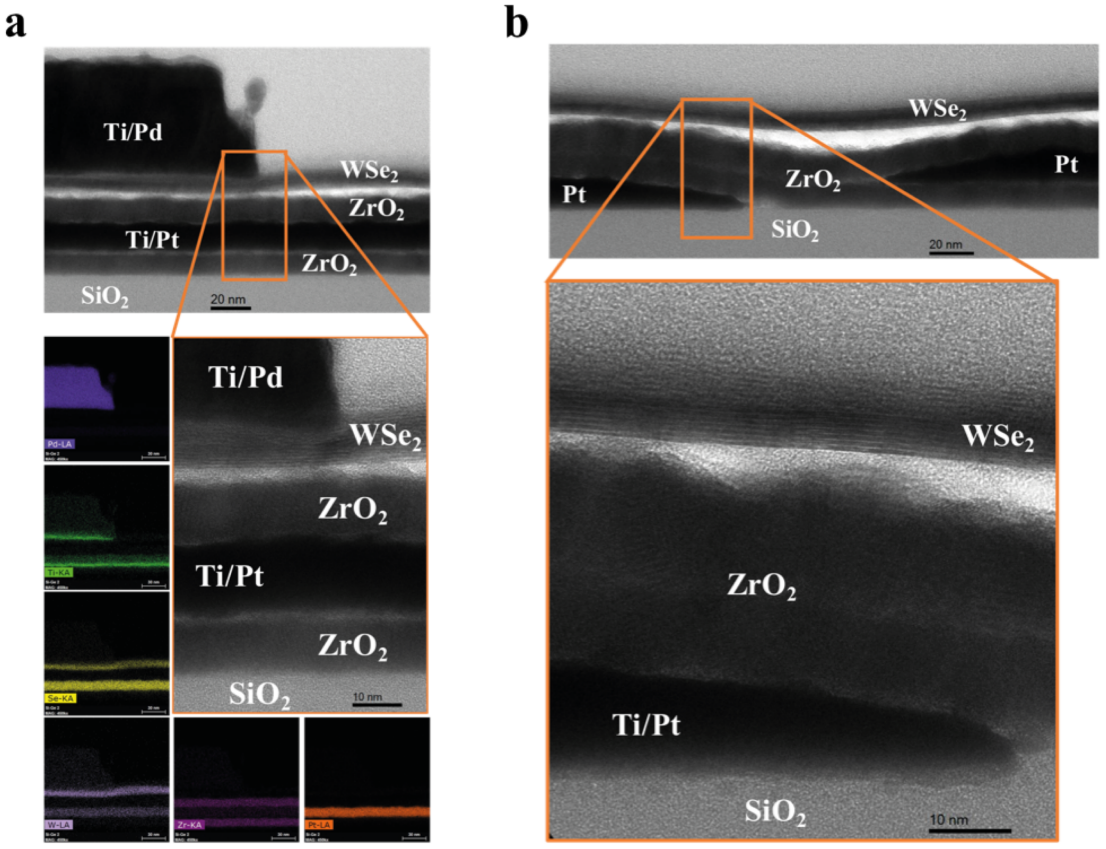


Figure 5.3 – Cross-sectional TEM with EDX mapping. **(a)** Cross-sectional HRTEM image of the contact region with EDX mapping. **(b)** Cross-sectional HRTEM image of the central region of the device, showing the separation between CG and PG. Both cross-sections are taken along the red-dotted line shown in Fig. 5.2b. Adapted with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

delamination of the 2D flake, occurring during the focused ion beam sample preparation.

As mentioned above, the regular and flexible design for the logic gates is made possible by the switching properties of the single polarity-controllable devices, that are also enabling the compact fabrication of the XOR-2 gate, which is presented in Fig. 5.2.

5.2.2 Switching Properties

We will now study in detail the switching properties of the single polarity-controllable devices fabricated with the process presented above, and compare them to the ones in Sec. 4.3.

Ambipolar conduction and polarity control behavior are observed, as shown in Fig. 5.5a. When the PG is biased at 0 V or below, holes are favorably injected in the channel

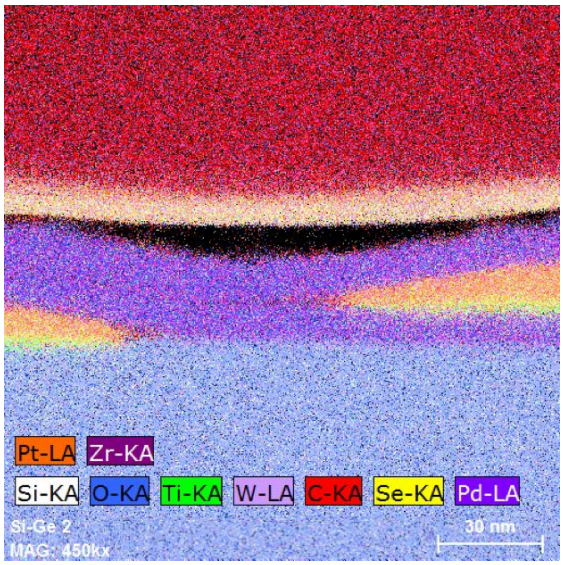


Figure 5.4 – Full EDX map of the central region of the device showing the separation between PG and CG. The lack of carbon in the region between the ZrO2 and the WSe2 proves it to be empty space, probably caused by partial delamination of the 2D-flake, occurring during the FIB sample preparation. Reproduced with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

and the device behaves as a *p*-type transistor. Conversely the transistor is programmed to function as a *n*-type device when the PG is biased at 3 V and above. In both cases, the CG is able to turn ON and OFF the transistor when swept between 0 and 2V. It appears that a higher voltage range is needed to flip the transistor polarity, using PG, with respect to the voltage needed to control the potential barrier in the channel, using the CG. We believe this difference stems from the different mechanism that the two gates are exploiting, i.e. electrostatic-doping of the Schottky-junction and modulation of a potential barrier in the channel, with a different band movement factor probably occurring for the two gates.

We achieve high ON/OFF ratios of respectively 10^5 and 10^6 for *n*- and *p*-type conduction on the same device. The asymmetry between the *n*- and *p*-type transfer characteristics, with the *p*-current around 10× higher than the n-current, stems from the non-perfect mid-gap contact alignment, creating asymmetric Schottky barriers for electrons and holes, that was achieved with Ti/Pd contacts. Current flow in a Schottky-Barrier *Field-Effect Transistor* (FET) is the result of two separate conduction mechanism across the barrier: (i) thermionic emission of carriers over the top of the barrier and (ii) tunneling of charge carriers through the Schottky barrier [128]. Here, the PG acts both at the contact interface between the metal and the semiconductor and also on the region underneath the contact (as can be seen in Fig. 5.3a), which is essential to have an efficient charge injection. It has been recently shown how the gate-induced modulation underneath the contacts (contact gating), provides additional tunneling paths

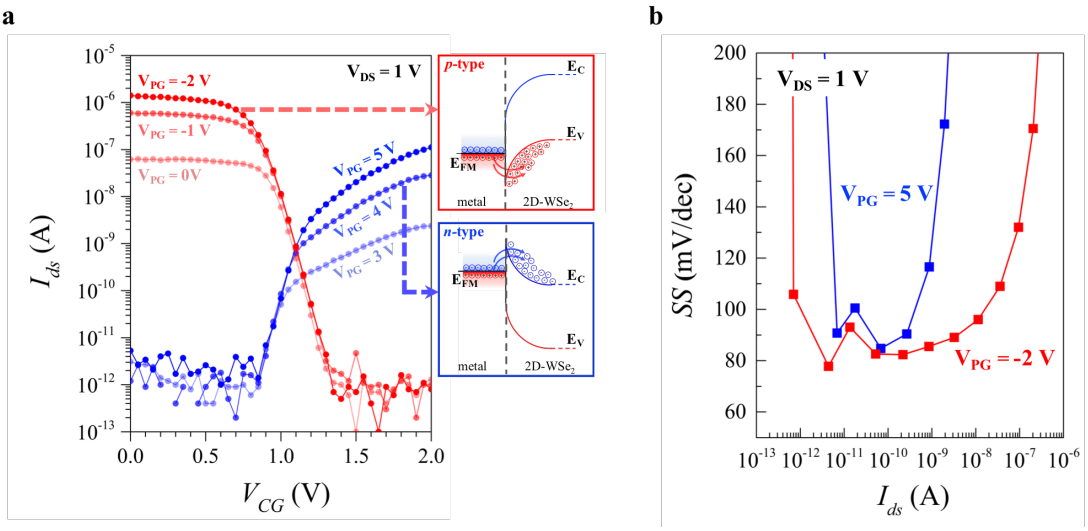


Figure 5.5 – Polarity-controllable device characteristics. (a) Transfer characteristics showing ambipolar conduction and demonstrating the polarity-controllable behavior. The *p*-type (*n*-type) operation is achieved for $V_{PG} < 0$ V (>3 V). The insets show the effect of the PG on the Schottky barrier, leading to the injection of only one type of charge carriers. **(b)** Sub-threshold slopes extracted from the transfer characteristics presented in **(a)** for $V_{PG} = 5$ V and $V_{PG} = -2$ V. Adapted with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

that allow a better carrier injection in the 2D semiconductor [179]. Biasing the PG leads to accumulation of mobile charges underneath and at the contact interface, providing electrostatic doping of the 2D-WSe_2 and considerably thinning the *Schottky-Barrier* (SB). Tunneling of charge carriers through the thinned barrier thus becomes much more favorable. The control of the PG on the barriers is evident as changing the PG bias from 0 to 3 V results in a complete switch of the transistor polarity. However, since the transmission of charge carriers through the barrier depends exponentially on the barrier height (for both thermionic emission and tunneling) [128], it is essential to ensure a mid-gap contact to have symmetric barrier heights for electrons and holes. Future work will focus in improving the symmetry between the n and p branch, which is a desired feature for circuit operation [122], exploring different metals or introducing graphene to finely tune the Fermi level alignment at the contacts.

Moreover, in our previous experiments, reported in Sec. 4.3, we had found the Ti/Pd contact to WSe_2 to provide an enhanced electron conduction, with roughly 10× higher *n*-current with respect to *p*-current [28]. We attribute this difference to the change in the dielectric environment (*aluminium oxide* (Al_2O_3) in the previous experiments, and ZrO_2 in this work) that could lead to a different doping induced to the semiconducting 2D-WSe_2. Further experiments would be needed to assess the influence of the dielectric environment on the conduction properties of 2D-materials (as also elucidated in Appendix C), but are outside of the scope of this thesis.

The extrinsic mobility, extracted from the transfer characteristics (see eq. 4.1), is 1.5 and $0.1\,cm^2V^{-1}s^{-1}$ for hole and electron conduction, respectively. As already mentioned in Sec. 4.3 such mobilities values are lower than those reported in literature for WSe_2 [17, 18] and are determined by the presence of large Schottky barriers at the contacts, the lack of a top high-κ passivation and the presence of interface charges at the ZrO_2 / WSe_2 interface, that could increase charge scattering phenomena in the channel. Thanks to the scaled high-κ oxide and the use of platinum gates, *p*-type operation is achieved when biasing the PG and the CG at GND, which is an essential step to ensure the cascadability of the devices. Moreover, the use of scaled high-κ ZrO_2 creates a high gate-capacitance that translates into improved electrostatic control over the channel. We measured *Sub-threshold Slope* (SS) below 100 mV/dec over 2 and 4 decades of current for *n*- and *p*-type conduction respectively, as shown in Fig. 5.5c. From the minimum SS measured (85 mV/dec), for both electrons and holes, we can extract information on the *Interface-Trap Density* (D_{it}) from the standard expression used to describe the SS:

$$SS = \frac{kT}{q} ln(10) \left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) \tag{5.1}$$

where C_D is the depletion layer capacitance, C_{it} is the interface trap capacitance, C_{ox} is the gate-oxide capacitance and kT/q is the thermal voltage. Assuming $C_D = 0$, due to the extreme thinness of our 2D WSe_2 channel, we can extract C_{it}:

$$C_{it} = C_{ox} \left(\frac{q}{kT} \frac{SS_{min}}{ln(10)} - 1\right) = 3.83 \times 10^{-7} F/cm^2 \tag{5.2}$$

From here D_{it} can be easily computed as:

$$D_{it} = \frac{C_{it}}{q} = 2.4 \times 10^{12} cm^{-2} \tag{5.3}$$

which is in good agreement with previous literature on 2D-materials [180].

5.3 Demonstration of Logic Gates

As mentioned in Sec. 5.1.1 all the logic gates fabricated share the same gate design (except for the INV) and are differentiated only by the final wiring of the transistors contacts. The same wiring design can be used for the realization of NAND and NOR gates, whereas a different wiring is needed to realize XOR-2, XOR-3, and MAJ-3 gates, as shown in Fig. 5.1. Optical micrographs and circuit schematics for all the fabricated logic gates are presented in Fig. 5.6. When using polarity-controllable transistors to fabricate INV, NAND and NOR functions, the PG is biased at a fixed value, setting the polarity of the transistor, and the gates are arranged in a CMOS-like fashion (see Fig. 5.6) with logic inputs only applied on the CG.

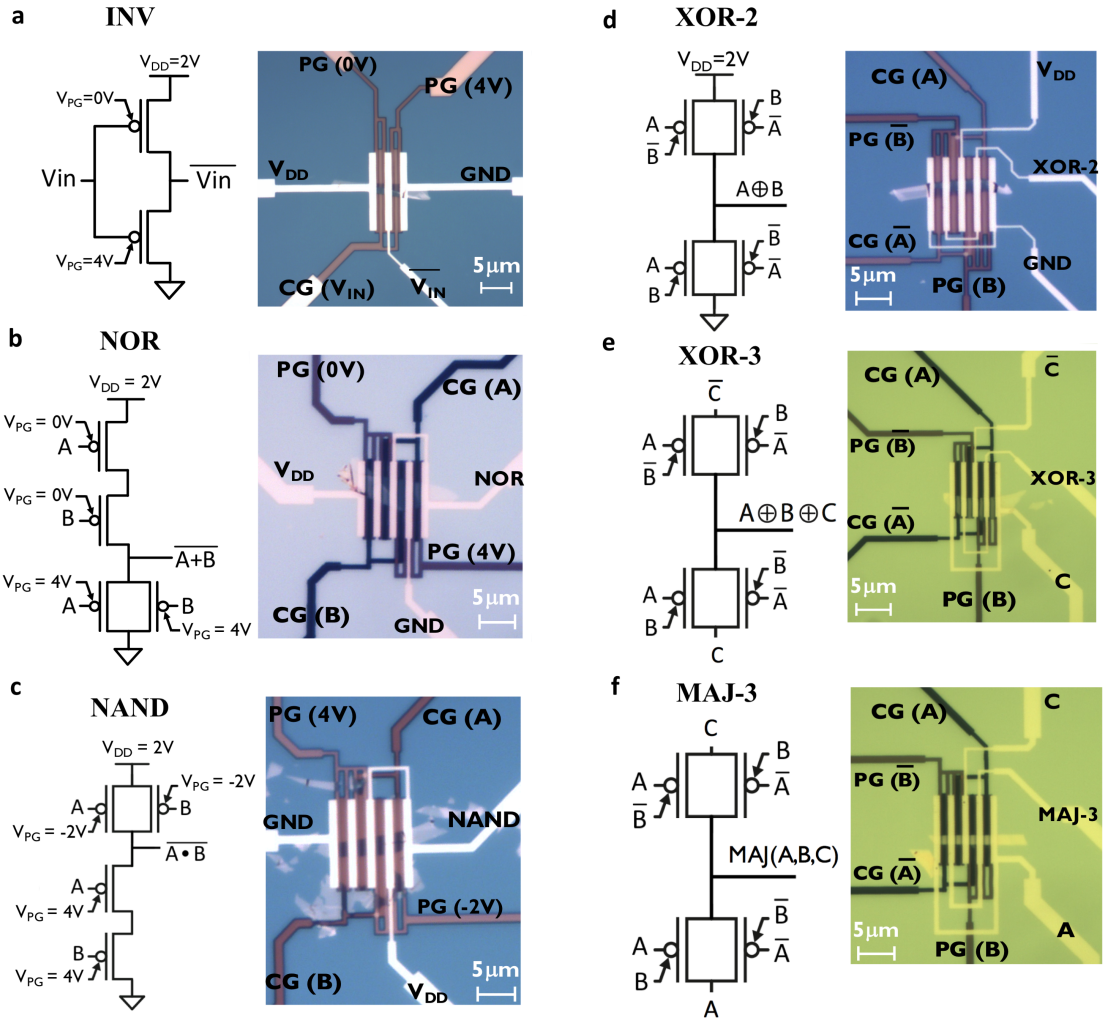


Figure 5.6 – Circuit schematic and optical micrograph of fabricated and tested devices.(a) Inverter. **(b)** NOR gate. **(c)** NAND gate. **(d)** XOR-2 gate **(e)** XOR-3 gate. **(f)** MAJ-3 gate. Notice the difference in color between **(e,f)** and the rest is due to the thicker ZrO_2 layer used for these devices. Reproduced with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

5.3.1 Inverter

For the case of an INV, see Fig. 5.7a-b, proper operation of the logic gate is achieved biasing the PG respectively at 0 V and 4 V for the *p*- and *n*-type transistor, while having V_{DD} = 2 V. The inverter behavior is verified achieving high inverter gains ($d(V_{OUT})/d(V_{IN})$> 30), as exemplified by the desirable sharp transition between the high and low state at around $V_{DD}/2$, see Fig. 5.7c. The imbalance in the transition is caused by the different drive current in the *n*- and *p*-type operation mode, as mentioned in the Sec. 5.2.2, and can be addressed by finely tuning the contacts.

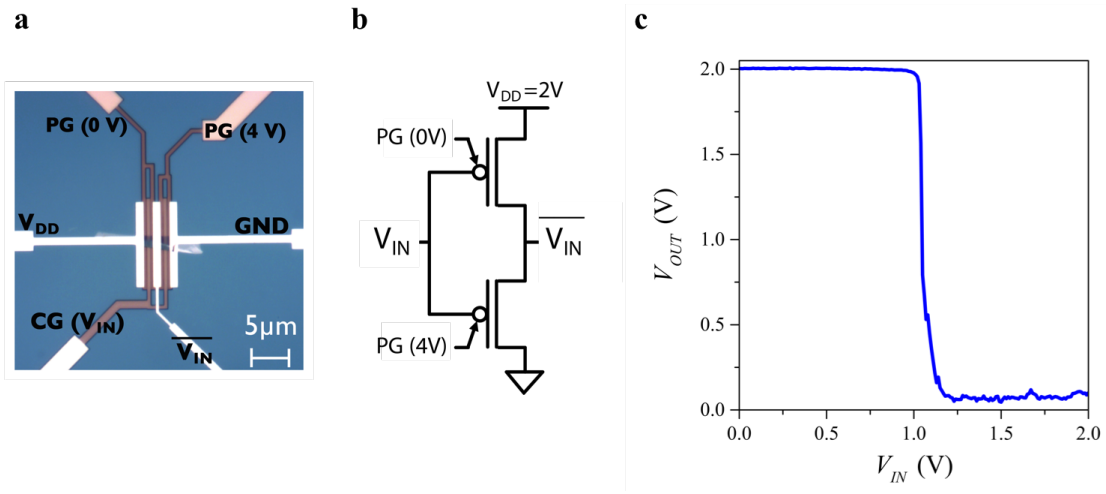


Figure 5.7 – Inverter behavior. **(a)** Optical micrograph of the fabricated inverted with the terminal names reported. **(b)** Corresponding circuit schematic, showing the voltage bias on the program gates. **(c)** Measured inverter behavior for $V_{DD} = 2$ V, showing a sharp transition between the "1" and "0" state around $V_{DD}/2$. Reproduced with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

5.3.2 Two-Input Logic Gates

Using the universal gating structure presented in Sec. 5.1.1, we are able to fabricate NAND and NOR gates with a conventional CMOS-like design, see Fig. 5.8 and Fig. 5.6. The PG of the transistors are biased at a fixed voltage, while the logic inputs, A and B, are only applied to the CG of the transistors. We verified the functioning of the NAND and NOR gates for $V_{DD} = 2$ V, while keeping the bias of the logic inputs between 0 V and 4 V. While for the NOR gate the PG are biased with the same voltage levels of the logic inputs, in the case of the NAND gate, in order to achieve the proper logic behavior, we apply a negative bias of -2 V to the PG of the p-type device. This is most likely caused by some residues on the channel or under the contacts that are preventing the transistor from efficiently conducting holes at $V_{PG} = 0$ V. Moreover, flake-to-flake variations, both in terms of thickness and defect density, can also contribute to the variation in the bias that needs to be applied to the polarity gates.

At this stage, we have demonstrated how polarity-controllable 2D-WSe_2 transistors can be used to replicate CMOS-like logic gates. However, the real advantage in the use of polarity-controllable transistors with respect to CMOS, comes only when exploiting the PG as a logic input, unlocking the enhanced switching properties of the devices. Having a logic input connected to the PG implies that the polarity of the device is no longer fixed, and will change at run-time according to the logic value of the signal (e.g., p-type for logic '0' and n-type for logic '1'). With this configuration, only possible thanks to the enhanced expressive switching function of the single devices, see Fig. 4.8, we can achieve highly compact implementation of XOR-2, XOR-3 and MAJ-3 functions with fewer

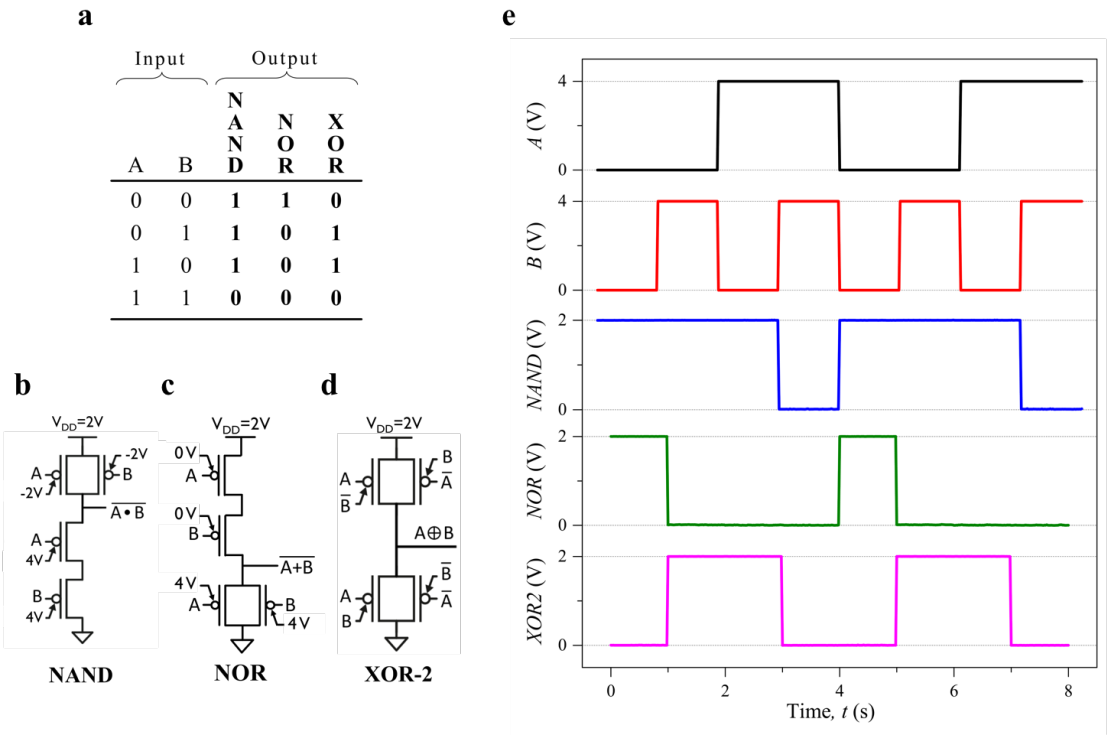


Figure 5.8 – Two-input logic gates. **(a)** Truth table of the NAND, NOR, and XOR-2 logic functions. **(b–d)** Circuit schematic of the logic gates describing where the logic inputs are applied and showing the fixed bias of the PG in the case of NAND and NOR gates. **(e)** Experimental waveforms demonstrating the operation of the NAND, NOR, and XOR-2 gates fabricated with polarity-controllable WSe_2 transistors. Reproduced with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

transistors then what is achievable in conventional CMOS. Disregarding the inverters needed to generate the complemented inputs (A^- and B^-), the XOR-2 is realized with only 4 polarity-controllable devices, while a conventional CMOS design would require 8 transistors. We show the operation of the XOR-2 gate, see Fig. 5.8d-e, with all the logic inputs acting between 0 V and 4 V, thus assuring the full cascadability of the gate. As shown in the circuit schematic of the XOR-2 gate, see Fig. 5.8d, logic input B is now acting on PG and not on CG as was the case for the NAND and NOR gates. It is important to notice that in contrast to the transfer characteristics presented in Fig. 5.5b, where the CG was only swept between 0 and 2 V, we are now operating both the CG and PG between 0 and 4 V. There is no drawback in further sweeping the CG up to 4 V as the current levels would just remain constant in either p-type OFF state or n-type ON state.

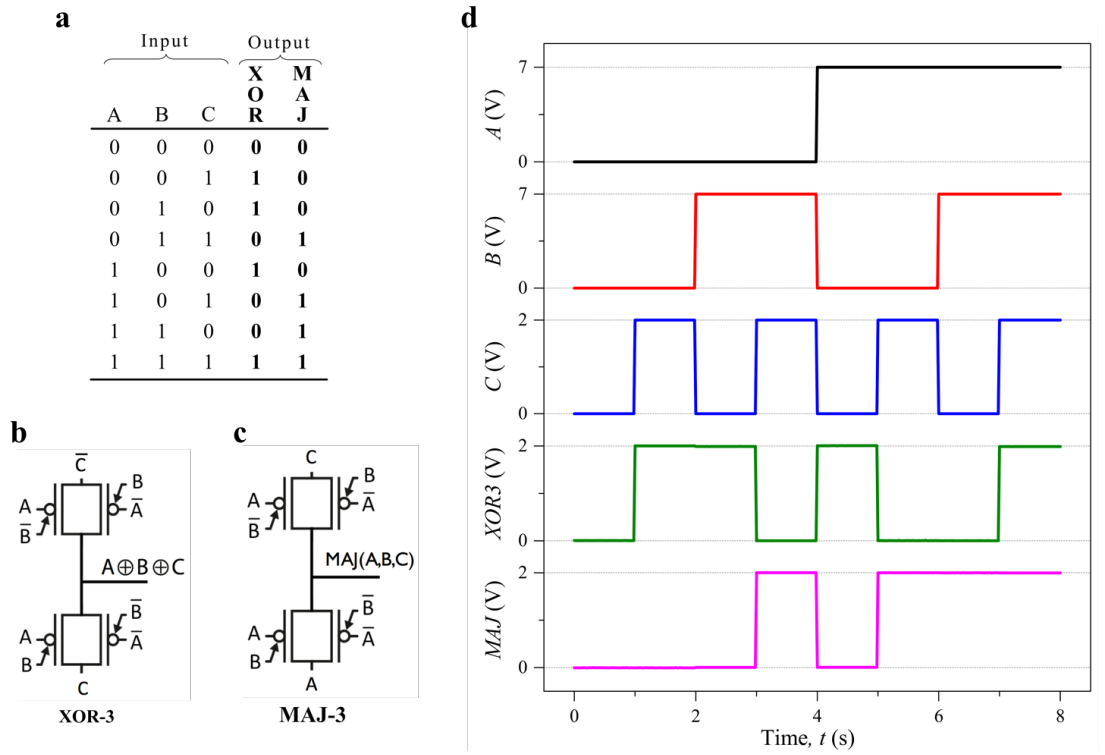


Figure 5.9 – Three-input logic gates. (a) Truth table of the XOR-3 and MAJ-3 logic functions. **(b–d)** Circuit schematic of the logic gates describing where the logic inputs are applied. **(e)** Experimental waveforms demonstrating the operation of the XOR-3 and MAJ-3 gates fabricated with polarity-controllable WSe_2 transistors. For the MAJ-3 gate, the logic input A applied at the *GND* terminal is kept between 0 and 2 V, and the input on the gates is kept between 0 and 7 V. Reproduced with permission from Resta *et al.* [33]. Copyright (2018) American Chemical Society.

5.3.3 Three-Input Logic Gates

By replacing the *Supply Voltage* (V_{DD}) and *GND* terminals with additional inputs, we are also able to demonstrate the logic operation for a highly-compact 4 transistors XOR-3 and MAJ-3, as shown in Fig. 5.9. These gates are realized on a thicker high-κ oxide (20 nm instead of 10 nm), thus requiring a higher voltage range for the logic inputs applied on the gates (between 0 V and 7 V). For the proper operation of the logic gates, the signals replacing the V_{DD} and *GND* terminals (C, C^- and A, C for the XOR-3 and MAJ-3, respectively) are instead kept between 0 V and 2 V. This limitation can be overcome by further scaling the gate oxide, allowing all logic inputs to have the same voltage range. XOR-3 and MAJ-3 are fundamental logic primitives that are present in virtually any arithmetic operator (consider that a 1-bit adder can be realized by a MAJ-3 gate to generate the carry-out and a XOR-3 gate to generate the sum), but are not efficiently realizable in CMOS-logic.

5.4 Summary

Here, we have shown a complete basis for an effective standard cell library of logic gates (INV, NAND, NOR, XOR-2, XOR-3 and MAJ-3), fabricated with WSe_2 polarity-controllable transistors. Thanks to the improved fabrication process we achieved polarity-controllable behavior with ON/OFF ratios $> 10^5$ for both polarities on the same device with subthreshold swings as low as 80 mV/dec. Thanks to the reconfigurable capabilities of the single devices, we achieve the realization of XOR-2, XOR-3 and MAJ-3, with fewer transistors than possible in conventional CMOS logic, that can be exploited as logic primitives to gain advantages at circuit level [157, 160, 177, 178]. This work represents a major step on the path to exploiting the full potential of this technology for the realization of novel digital circuits with dynamically controllable polarity gates in WSe_2 2D electronics.

6 Scaled Devices and Logic Gates Simulations

With four parameters I can fit an elephant,
and with five I can make him wiggle his trunk

— Quote attributed to John von Neuman

The chapter is dedicated to the simulation study of scaled polarity-controllable devices and logic gates. Following the experimental demonstrations of polarity-controllable devices in Ch. 4 and of doping-free logic gates in Ch. 5 we now explore the scaling trends of *Double-Independent-Gate* (DIG) *Two-Dimensional* (2D)-*Field-Effect Transistors* (FETs) in order to identify the fundamental limits of our approach and asses the device behavior. To estimate the electrical characteristics of such ultra-scaled devices, we first use ballistic self-consistent quantum simulations in the *Non-Equilibrium Green Function* (NEGF) formalism, and then develop a TCAD model in order to study the performances of scaled logic gates.

This chapter is organized as follows. In Sec. 6.1 we first explore scaling for devices based on *tungsten di-selenide* (WSe_2), the most promising material for which experimental results are available (as shown in Ch. 4 and Ch. 5. In Sec. 6.1.4, we then focus on the selection of novel 2D semiconductors, for which experimental demonstrations are still lacking, to enhance the performances of the device. We show that such devices can achieve performances that are comparable to unipolar doped devices with Ohmic contacts simulated with a similar approach, while bringing considerable simplifications to the fabrication process and bearing the promise of enhanced performances at circuit level. In Sec. 6.2, in order to study the performances of logic gates we show how we developed a Synopsis Sentaurus *Technology Computer-Aided Design* (TCAD) simulation that is able to reproduce the switching characteristics simulated with the quantum-transport simulations. In Sec. 6.2.4 we show the transient simulations performed to study logic gates switching, evaluating their delay and energy consumption. For selected logic gates the results are compared to other emerging technologies that have been studied in *Beyond-CMOS Benchmark* (BCB) 3.0 [25]. Finally, the chapter is concluded in 6.3 with

Property	**1L-WSe_2**	**2L-Wse_2**	**2L-Mx_2**
a (Å)	3.28	3.28	3.70
E_G (eV)	1.5	1.1	0.8
ϕ_{SB} (eV)	0.75	0.55	0.4
m_e	0.33	0.33	0.3
m_h	0.45	0.45	0.45

Table 6.1 – Material properties used to construct the effective mass Hamiltonian. The properties are: lattice constant, energy bandgap, Schottky-barrier height, electron effective mass and hole effective mass.

a brief summary. This chapter is largely based on the journal publication by Resta *et. al.* [35].

6.1 Quantum Mechanical Simulations

We study scaling trends and evaluate the performances of polarity-controllable devices realized with undoped mono- and bi-layer 2D materials. Using ballistic self-consistent quantum simulations, it is shown that, with the suitable channel material, such polarity-controllable technology can scale down to 5 nm gate lengths, while showing performances comparable to the ones of unipolar, physically-doped 2D electronic devices.

6.1.1 Methodology

The self-consistent ballistic simulations are performed iteratively solving Poisson and Schrödinger equation (within the NEGF formalism), with an open-source quantum transport code (NanoTCAD ViDES) [181, 182]. Fig. 6.1 shows the *Three-Dimensional* (3D) schematic structures of the simulated devices with *Top-Gate* (TG) and *Double-Gate* (DG) geometry (Fig. 6.1a,b respectively). In the TG configuration, *hafnium di-oxide* (HfO_2) ($\kappa = 25$, *Equivalent Oxide Thickness* (EOT) = 0.47 nm) is used as top dielectric, while *silicon di-oxide* (SiO_2) ($\kappa = 3.9$, EOT = 30 nm) is considered as bottom dielectric. It should be noted that for the TG geometry a global back-gate (acting through the bottom dielectric) is introduced and kept grounded during the simulations. For the DG geometry HfO_2 ($\kappa = 25$, EOT = 0.47 nm) is used for top and bottom gate dielectrics.

We model the 2D semiconducting channel with a 2-band *Tight-Binding* (TB) Hamiltonian, created from the material properties shown in Table 6.1 [183–187]. To perform quantum simulations within NEGF formalism, the conduction and valence bands of a chosen material are modeled following the work in [188]. We calculate the hopping parameter (t_{hop}) to be used by NanoTCAD ViDES [181, 182] in the NEGF simulations,

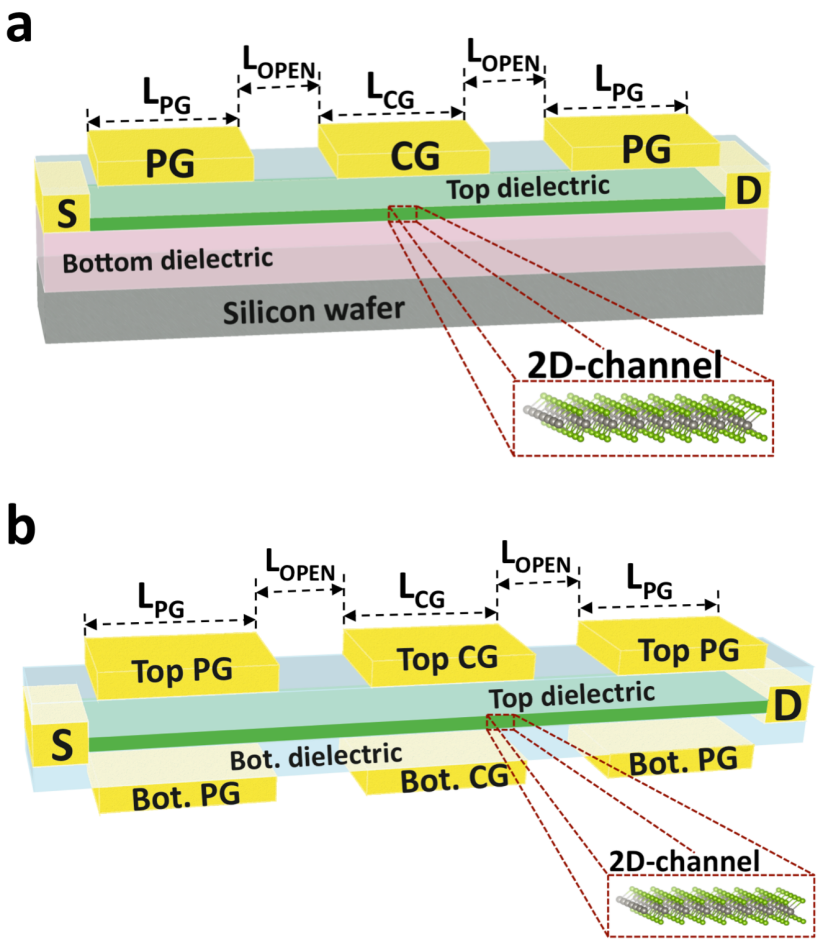


Figure 6.1 – 3D schematic of the simulated devices.(a) TG device structure. (b) DG device structure. In both schematics the semiconducting 2D channel is highlighted, with its atomic structure shown in the dashed boxes.

as [188]:

$$|t_{hop}|^2 = \frac{2\hbar E_G}{3a^2 m_r^*} \tag{6.1}$$

where a is the lattice constant, E_G is the energy band-gap, m_r^* is the reduced effective mass and $\hbar$ is the reduced Plank constant. This approach has been widely used to project performance of nanoscale transistors based on *silicon* (Si), III-V [189] and now 2D materials [46–49]. Further, to model Schottky contacts, we extend our Hamiltonian at the contacts for the zero-bandgap metal and applied Dirichlet boundary conditions. This model provides a good trade-off between accuracy and computational time which is crucial in advanced device design with exotic materials for future technology nodes. The model is extended to *Bi-Layer* (2L) 2D materials by adding an interlayer hopping parameter in the effective-mass Hamiltonian, to account for coupling between the two

layers [190].

No doping was introduced at source and drain contacts for both gate geometries and we assumed mid-gap *Schottky-Barrier* (SB) contacts, to have symmetric characteristics for the two polarities. We evaluated the device performances at different gate lengths, while keeping the same length for both the *Control Gate* (CG) and *Polarity Gate* (PG) gates ($L_{CG} = L_{PG}$) and the length of the un-gated channel region (L_{OPEN}), separating PG and CG, fixed to $L_{CG}/2$, as shown in Fig. 6.1. Thus, in the remainder of the article, we will refer to L_G as the length of each gated segment. The PG are placed in close proximity to source and drain contact (an underlap of 0 nm is used in all simulations) in order to provide the most efficient modulation of the Schottky barrier. For each simulated transfer characteristic, the value of the voltage applied to the program gate (V_{PG}) is fixed, thus setting the device polarity, and the switching properties as a function of the control gate voltage (V_{CG}) are studied.

6.1.2 Simulated Transfer Characteristics for 2D-WSe_2

The operation principle of the devices are verified at ultra-scaled gate lengths as shown in Fig. 6.2 with the help of the band-diagrams extracted from the simulations on *Mono-Layer* (1L) WSe_2 at $L_G = 8$ nm. As expected, following the experimental results presented in previous chapters, the PG controls the device polarity by tuning the effective *Schottky-barrier height* (ϕ_{SB}) at source and drain (n-type behavior at $V_{PG} = 1$ V in Fig. 6.2a and p-type behavior at $V_{PG} =$ -1 V in Fig. 6.2b) while the CG determines the ON/OFF state of the *Field-Effect Transistor* (FET) by controlling the potential barrier in the central region of the channel. Our simulation results show that the polarity of the device can be controlled at ultra-scaled dimensions, down to 4 nm gate lengths, when direct tunneling through the CG potential barrier begins to considerably degrade the device OFF-state.

Fig. 6.3 shows the simulated p- and n-type transfer characteristics for 1L-WSe_2 channel, with TG (Fig. 6.3a,b) and DG (Fig. 6.3c,d) geometry. The gate length is varied to show the impact of scaling on the device characteristics. It is found that 1L-WSe_2 provides excellent control of the device OFF-state, thanks to the high bandgap (1.5 eV) [184], but also severely limits the *ON-current* (I_{ON}) of the device due to the high SB ($\phi_{SB} = 0.75$ eV) present at source, where carriers are injected in the channel. The modulation induced by the PG at $\pm$ 1 V is enough to show conduction of charge carriers, but the I_{ON} only reach values of a few µA / µm for DG geometry. Therefore, to increase the I_{ON} of the devices, 2L-WSe_2 is studied as a channel material. In its bi-layer form WSe_2 shows a reduced bandgap of 1.1 eV [184], which together with the increased mobile charge density, provided by the additional layer, is predicted to improve the device ON-state. Fig. 6.4 shows the simulated transfer characteristics of 2L-WSe_2 FETs for both polarities and gate geometries, at different gate lengths.

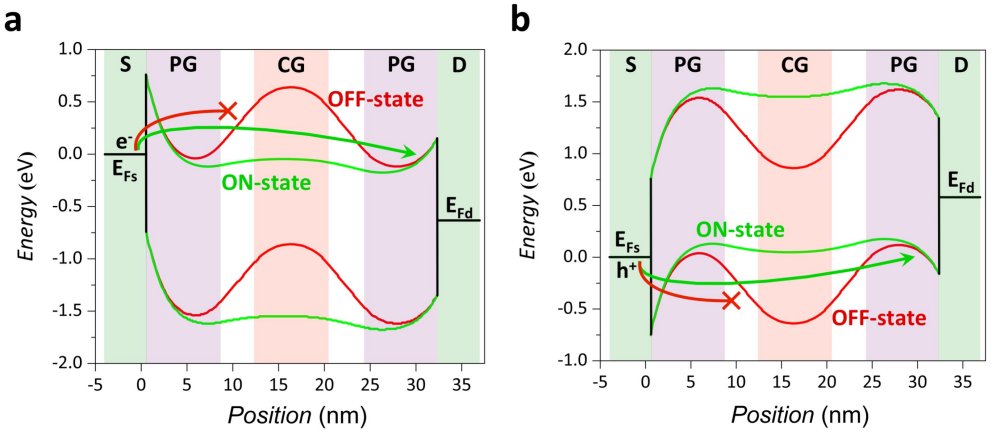


Figure 6.2 – Band-diagrams of the 4 regions of operation extracted from the simulation with 1L-WSe_2 at $L_G = 8$ nm. (a) n-type operation, for $V_{PG} = 1$ V. The PG sets the polarity of the device, by thinning the SB for electrons (e^-) at source and drain, while the CG controls the ON/OFF switching of the FET. In the OFF-state ($V_{CG} = 0$ V), the potential barrier, created in the channel by the CG, blocks electron conduction from source to drain (red crossed line). In the ON-state, with the band diagram extracted at $V_{CG} = 0.8$ V, the barrier is removed and electron conduction takes place (green arrow). **(b)** p-type operation for $V_{PG} = -1$ V. In this case, the negative voltage applied to the PG enables holes (h^+) to be injected in the channel at source (green arrow). In a similar way, as described for n-type operation, the potential barrier created by the CG blocks the flow of holes from source to drain (red crossed line).

6.1.3 Analysis and Comparison of Transfer Characteristics

As a result of the decreased Schottky-barrier height at the contact interface ($\phi_{SB} = 0.55$ eV), the ON-currents of 2L-WSe_2 FETs are increased by 2 orders of magnitude. With the lowering of the semiconducting bandgap ($E_G = 1.1$ eV), the potential barrier created by the CG in the OFF-state of the device is also decreased, deteriorating the device I_{OFF}. The I_{OFF} is increased by almost 3 orders of magnitude. Nevertheless, the transfer characteristics presented in Fig. 6.4, show that even at the shortest gate length simulated ($L_G = 4$ nm), I_{OFF} is still on the range of 10^{-4} µA / µm, providing $I_{ON}/I_{OFF} > 10^6$. The use of a DG geometry benefits the electrostatic control of the gates over the channel, and eliminates the charge screening effect between the layers that occurs in the TG structure. The improvement in the device electrostatics, given by the DG configuration, is shown in Fig. 6.5 where the I_{OFF} and I_{ON} (Fig. 6.5a,b respectively), extracted from the transfer characteristics of n-type devices with TG and DG structures, are compared.

The benefits of the DG structure come both from the use of the double gate and from the thin high-κ oxide encapsulating the 2D semiconductor. The presence of the thin high-κ oxide, in contrast to the 30 nm thick SiO_2 of the TG geometry, provides an improvement in I_{OFF} and *Sub-threshold Slope* (SS) while the presence of a double gate

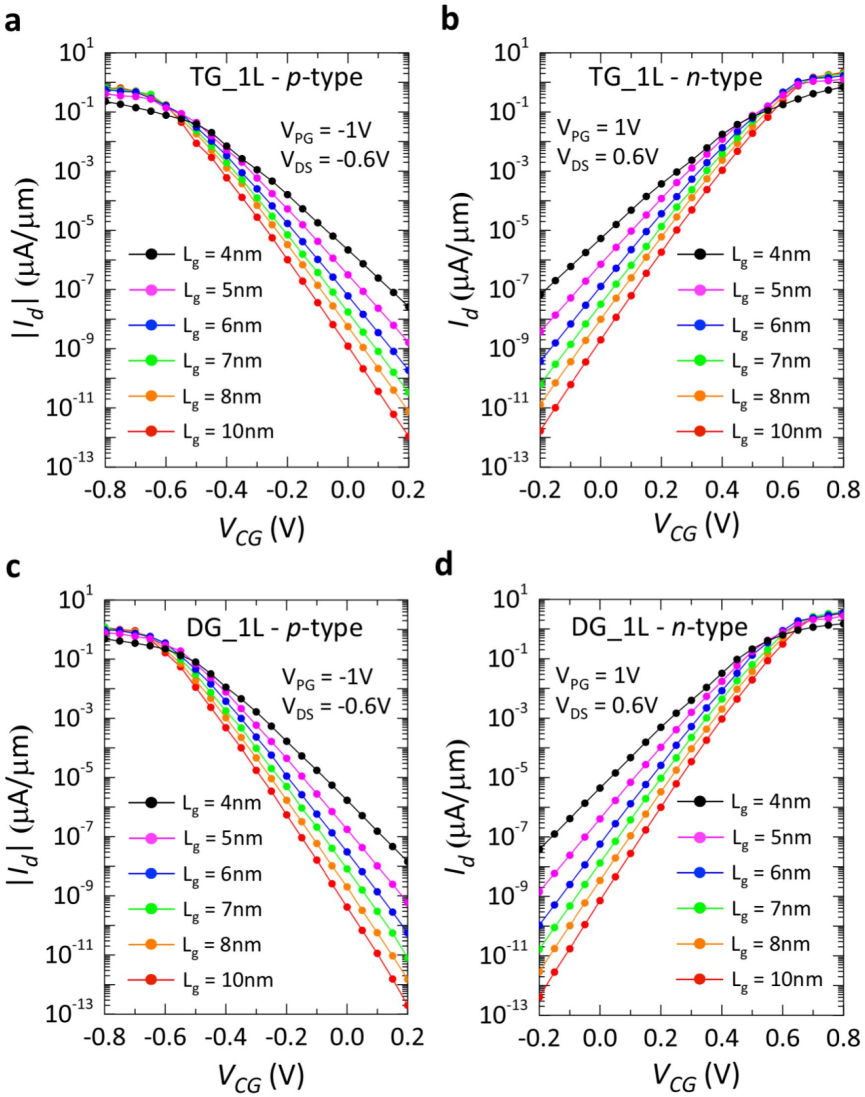


Figure 6.3 – Simulated transfer characteristics for 1L-WSe_2 polarity-controllable FETs at different gate lengths. 1L-WSe_2 was modeled with 1.5 eV bandgap and the hopping parameters of the effective mass Hamiltonian were calculated using an effective mass (m_e) of 0.33 m_0 for electrons and of 0.45 m_0 for holes. The ϕ_{SB} was set to 0.75 eV for both charge carriers, simulating a mid-gap Schottky contact. **(a,b)** Transfer characteristics of p- and n-type FET with TG geometry. The gate length is varied from 10 nm down to 4 nm. **(c,d)** Transfer characteristics of p- and n-type FET with DG geometry. The gate length is varied from 10 nm down to 4 nm.

produce an increase in I_{ON} (this consideration is further explored in Section 6.2. Here, it is found that, until $L_G = 5$ nm, the I_{OFF} in the DG configuration is consistently 1 order of magnitude lower with respect to the TG geometry, while the I_{ON} shows an average 2× improvement. For $L_G = 4$ nm, the potential barrier created by the CG starts to become thin enough to have tunneling effects, deteriorating the OFF-state of the device and thus

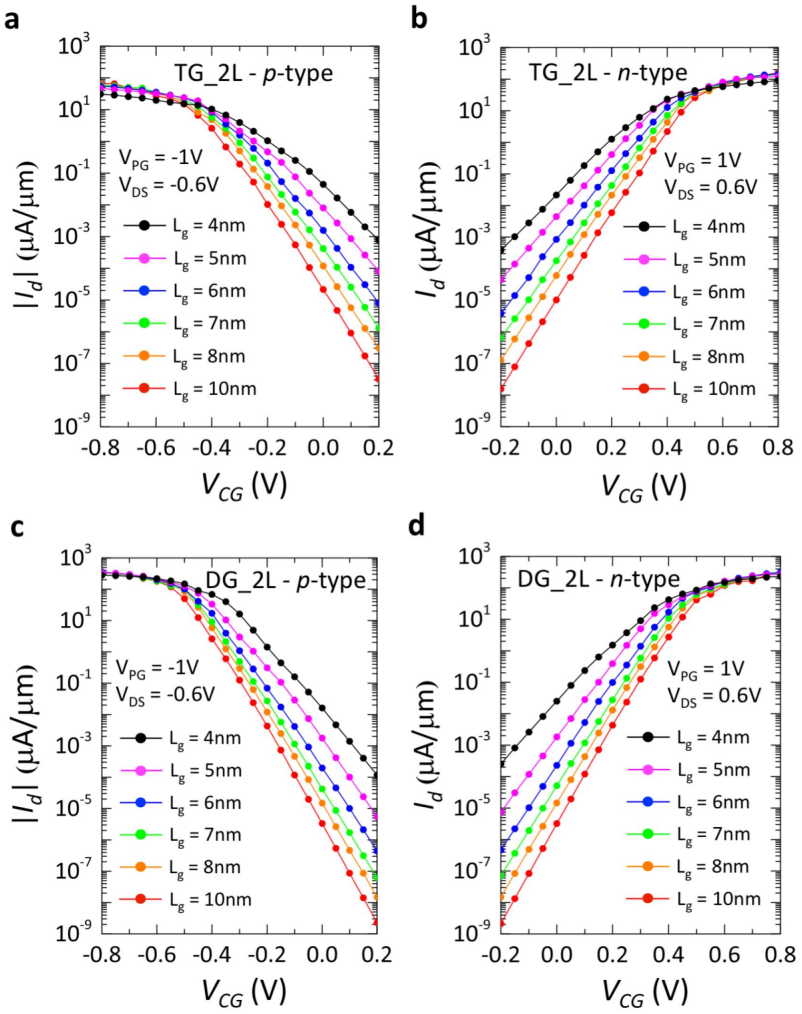


Figure 6.4 – Simulated transfer characteristics for 2L-WSe_2 polarity-controllable FETs at different gate lengths. 2L-WSe_2 was modeled with 1.1 eV bandgap and the hopping parameters of the effective mass Hamiltonian were calculated using an effective mass (m_e) of 0.33 m_0 for electrons and of 0.45 m_0 for holes. The ϕ_{SB} was set to 0.55 eV for both charge carriers, simulating a mid-gap Schottky contact. **(a,b)** Transfer characteristics of p- and n-type FET with TG geometry. The gate length is varied from 10 nm down to 4 nm. **(c,d)** Transfer characteristics of p- and n-type FET with DG geometry. The gate length is varied from 10 nm down to 4 nm.

lowering the positive impact of the double-gate. Similar results can be found for the p-type characteristics simulated on the same device.

Further analysis is presented in Fig. 6.6, where the effect of scaling on the SS and on the DIBL is analysed. The SS is evaluated as the average slope of the transfer characteristics in the sub-threshold regime (from V_{CG} -0.2 V to 0.2 V) for both p- and n-type operation mode (Fig. 6.6a,b respectively). For both polarities, it is shown that the SS greatly benefits from the thin back-gate high-κ oxide present in the DG geometry,

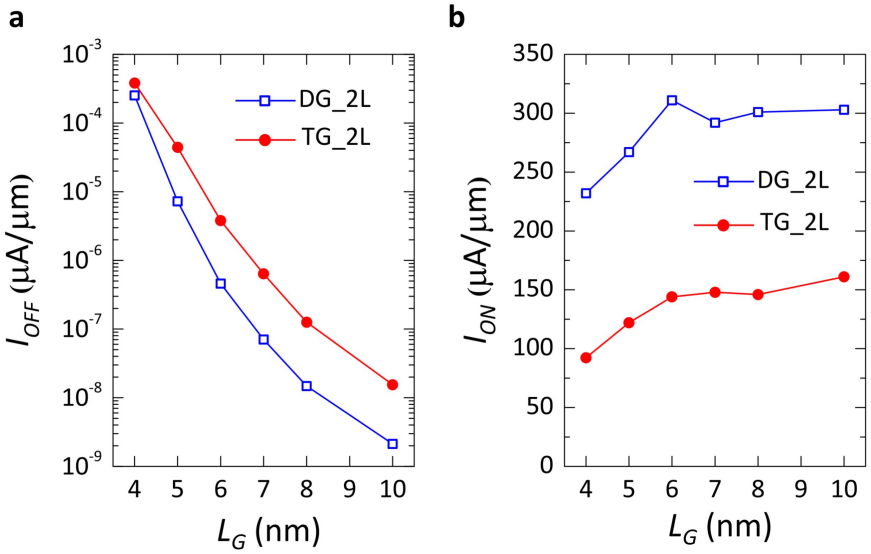


Figure 6.5 – Benefits of DG geometry in 2L-WSe_2 *n*-type FETs. **(a)** Comparison between *OFF-current* (I_{OFF}) extracted at $V_{CG} = -0.2\,V$ and $V_{PG} = 1\,V$ for TG and DG devices, at different gate lengths. **(b)** Comparison of devices I_{ON} extracted at $V_{CG} = 0.8\,V$ and $V_{PG} = 1\,V$ at different gate lengths.

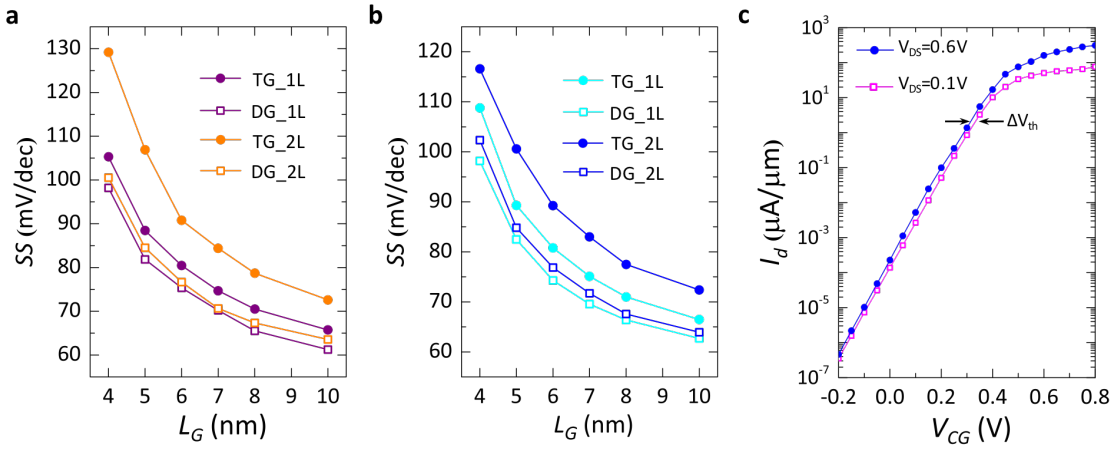


Figure 6.6 – Evaluation of sub-threshold slope and DIBL. **(a)** Sub-threshold slope extracted from the transfer characteristics of *p*-type devices, for both 1L and 2L WSe_2. **(b)** Sub-threshold slope for *n*-type devices. It is shown that for both polarities, the use of the DG geometry benefits the sub-threshold behavior by reducing the SS. **(c)** *Drain-Induced Barrier Lowering* (DIBL) evaluation at $L_G = 6\,nm$ for DG *n*-type device. A *Threshold Voltage* (V_{TH}) shift (ΔV_{TH}) of approximately 25 mV is present, leading to a DIBL of around 50 mV/V.

that is able to mitigate the detrimental effect of increased channel thickness for the bilayer device. The DIBL is calculated as the variation of V_{TH} of the device divided by the variation of applied V_{DS} ($DIBL = \Delta V_{TH}/\Delta V_{DS}$) and is expressed in mV/V. A

V_{TH} shift of 25 mV can be estimated as the lateral shift, at the end of the sub-threshold regime, between the transfer characteristic simulated at $V_{DS} = 0.1$ V and 0.6 V (see Fig. 6.6c). Thus we computed a DIBL of 50 mV/V for $L_G = 6$ nm, showing excellent immunity to DIBL effects. The observed immunity to DIBL is an added benefit of the SB polarity-controllable FETs, as the drain voltage drop in the channel is concentrated at the Schottky junction at drain. The change in V_{DS} does not affect the height of the potential barrier created by the CG, which is ultimately responsible for the lowering of the threshold voltage of the device.

6.1.4 Simulated Transfer Characteristics for Reduced Band-Gap MX_2

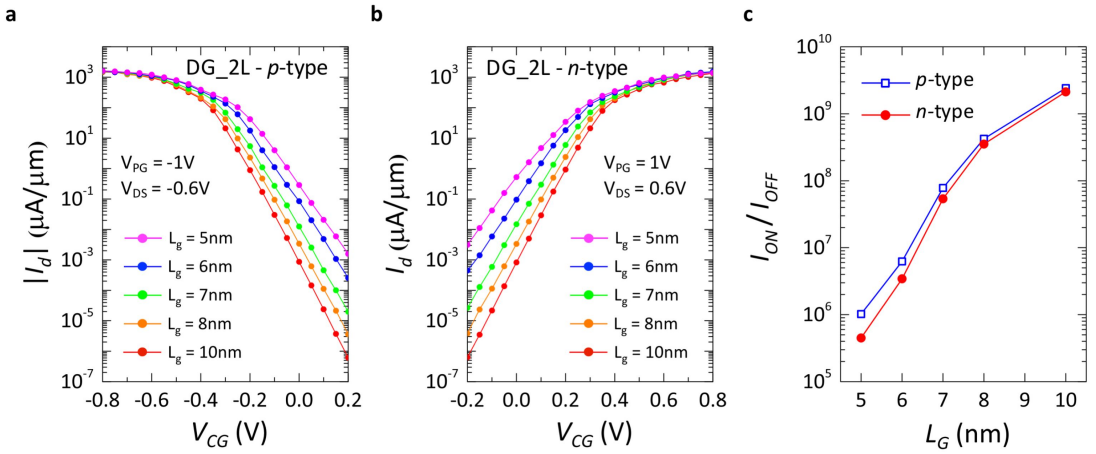


Figure 6.7 – Analysis of performances for double-gate polarity-controllable device with 2L-MX_2 material. The improved MX2 material was modeled with 0.8 eV bandgap, which results in a ϕ_{SB} of 0.4 eV. The effective masses used were $m_e = 0.3\,m_0$ and $m_h = 0.4\,m_0$. **(a)** Transfer characteristics for p-type behavior, with L_G varied from 10 nm down to 5 nm. **(b)** Transfer characteristics for n-type behavior, with L_G varied from 10 nm down to 5 nm. **(c)** I_{ON}/I_{OFF} for both p- and n-type behavior. In both cases, $I_{ON}/I_{OFF} > 10^5$ is shown down to $L_G = 5$ nm.

The analyses, presented in Sec. 6.1.3, show that the DG geometry provides the best electrostatic control and enhances the performances of the device by lowering the I_{OFF}, while improving the I_{ON} and SS. Nevertheless, the ION reachable with 2L-WSe_2, in both n- and p-type operation mode, are still too low to provide a successful scaling path with this material. The Schottky barriers at source and drain ($\phi_{SB} = 0.55$ eV) are too high to have efficient tunneling at the contact interface. However, theoretical calculations [185–187] have shown that in the family of 2D-*Transition Metal Di-Chalcogenides* (TMDCs), several materials, such as ZrS_2, HfS_2, $HfSe_2$, etc., have a lower semiconducting band-gap (0.7 - 0.9 eV) and could prove to be well suited for application in SB-DIG FETs. For many of these materials experimental evidences are still absent or very limited [191–195] [109], and even in the theoretical *ab-initio*

calculations there are discrepancies in the computed material properties [185–187] (with great variations especially in the value of the semiconducting band-gap, depending of the functional used in *ab-initio* simulations).

Based on these theoretical analyses, we modeled a 2D material, according to the properties presented in table 6.1, and studied its potential application as a semiconducting channel in polarity-controllable FETs. We considered a 2L-MX2 material with an increased lattice constant, a lower bandgap and similar effective masses with respect to WSe_2 (as it is predicted for ZrS_2, HfS_2, $HfSe_2$). Fig. 6.7a,b show the transfer characteristics at different L_G for a DG geometry for both p- and n-type polarities, while the device performance in terms of I_{ON}/I_{OFF} ratio is presented in Fig. 6.7c. The lower Schottky-barrier height at source and drain ($phi_{SB} = 0.4\,\text{eV}$) allow for a greater number of carriers to be injected in the channel, increasing the I_{ON} to $1.5\,\mu\text{A}$ / μm, while keeping I_{OFF} well below $10^{-2}\,\mu\text{A}$ / μm down to $L_G = 5\,\text{nm}$. The lower I_{ON}/I_{OFF} ratio for n-type behavior shown in Fig. 6.7c is caused by the lower effective mass of electrons, which increases the transmission probability of carriers over the potential barrier created by the CG, thus increasing the I_{OFF}.

6.2 TCAD Simulations

We used Synopsis TCAD Sentaurus software in order to make accurate predictions on the speed and performance of scaled logic gates realized with polarity-controllable 2D FETs. We first investigate if the results achieved using the quantum transport simulations, performed with NanoTCAD ViDES, can be reproduced by conventional Synopsis Sentaurus Device software. We then use the TCAD tools to predict the behavior of novel device structures and analyze the performances of logic gates. Note that all the following results are still unpublished.

6.2.1 Fit with Quantum Simulation

In order to validate the use of Synopsis Sentaurus Device software to predict the performances of logic gates, we first need to be able to reproduce the switching characteristics of the single devices that have been simulated using NanoTCAD ViDES (see Sec. 6.1). This process involves building a model for the description of the material and evaluating the correct options to be enabled in the Sentaurus Device tool.

To match the conditions of the quantum simulations we used a 2L material, 1.4 nm thick, with a EOT of 0.47 nm. The length of the gated segments (L_G) is kept at 10 nm, so that we can compare with our quantum characteristics simulated at the same L_G, and also with the BCB 3.0 (which has $L_G = 12.8\,\text{nm}$). The material parameters presented in Table 6.1 are kept the same in the TCAD simulations. However, in contrast to ViDES, which takes into account the 2D nature of the semicondcuting material, TCAD tools treat the 2D material as a ultra-thin slab of 3D material, with thickness 1.4 nm. The difference

is that the *Density Of States* (DOS) is then computed as a 3D DOS instead of a 2D DOS. Thus, we recomputed the effective masses to get the correct 2D DOS in our bands. The simulations in ViDES did not specify a mobility for the material (ballistic simulations) so in our TCAD model we chose a constant mobility of $300\,\mathrm{cm^2V^{-1}s^{-1}}$, which is well below the phonon-limited mobility reported for several TMDCs materials [187].

A non-local mesh is introduced at the contact interfaces to account for the tunneling of charge carriers at the Schottky barrier. The non-local mesh encompass all possible tunneling paths from the interface up to 10 nm inside the semiconducting channel. The relative in-plane and out-of-plane dielectric constant (2 and 7 respectively) were chosen from literature [196]. The ϕ_{SB} is kept at $E_G/2$, same as in the quantum simulations, while the work-function of the metal gates is adjusted to fit the quantum simulations. For the simulations with $E_G = 1.1\,\mathrm{eV}$ the work-function is 4.86 eV, while for $E_G = 0.8\,\mathrm{eV}$ it is 4.70 eV.

The drain-source potential (V_{DS}) is kept at 0.6 V as in the quantum simulations. However, it should be noted that there are differences in the way the voltage biases have been applied between the two simulations. In the quantum software, when simulating:

- n-type characteristics the source is kept grounded and the drain is biased at 0.6 V. The PG is biased at 1 V and the CG swept from -0.2 to 0.8 V.
- p-type characteristics the source is again grounded, and the drain is biased at -0.6 V with the PG kept at -1 V (so that $V_{PG} - V_S$ = -1 V) while the CG is swept from 0.2 to -0.8 V.

In the TCAD simulations we are aiming at demonstrating proper device operation between *Ground* (GND) and V_{DD} (1 V), so that no negative voltage is needed. Thus, in TCAD, when simulating:

- n-type characteristics, all voltage biases are the same as in the quantum simulations.
- p-type characteristics, the source is tied at V_{DD} = 1 V. In order to have V_{DS} = -0.6 V the drain terminal was biased at 0.4 V. The PG was kept at 0 V, thus achieving a $V_{PG} - V_S$ of -1 V (which matches the quantum simualtions). The CG is swept between 1.2 and 0.2 V with $V_{CG} - V_S$ = 0.2 - -0.8 V, as in the quantum simulations.

Using this conventions for the different voltage bias we simulate the $I_{ds} - V_{CG}$ transfer characteristics, by self-consistently solving Poisson equation with carrier continuity equations for both electrons and holes, and compare them with the ones obtained with the ViDES software (see Fig. 6.8).

As it can be appreciatd in Fig. 6.8, we achieved a good fit for the 3 conditions that we analyzed (TG with $E_G = 1.1\,\mathrm{eV}$, DG with $E_G = 1.1\,\mathrm{eV}$ and DG with $E_G = 0.8\,\mathrm{eV}$,

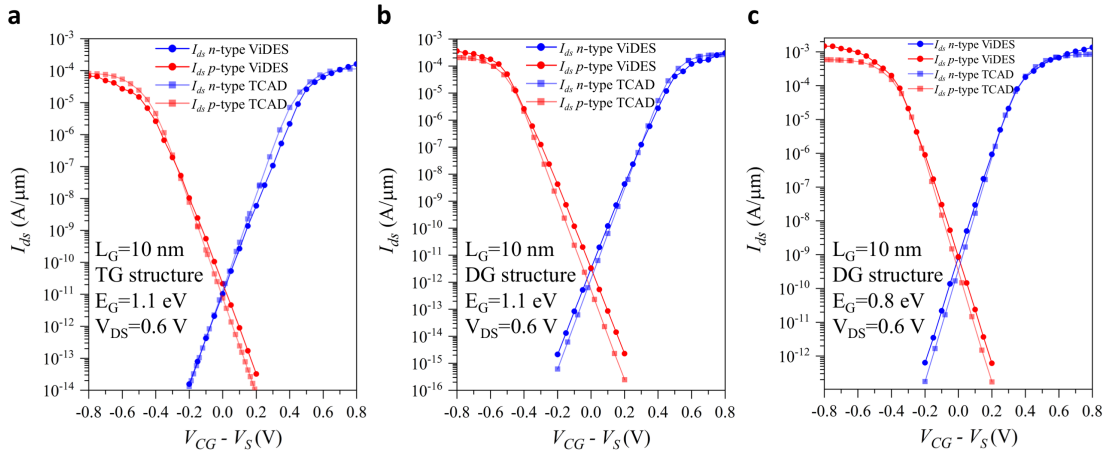


Figure 6.8 – Comparison of transfer characteristics simulated with ViDES and Synopsis Sentaurus. (a) Transfer characteristics $I_{ds} - V_{CG}$ for TG structure with $E_G = 1.1\,\text{eV}$ for the MX_2 material. **(b)** Transfer characteristics $I_{ds} - V_{CG}$ for DG structure with $E_G = 1.1\,\text{eV}$ for the MX_2 material. **(c)** Transfer characteristics $I_{ds} - V_{CG}$ for DG structure with $E_G = 0.8\,\text{eV}$ for the MX_2 material.

Fig. 6.8a,b,c respectively). The most notable discrepancies between the quantum and TCAD simulations are the I_{OFF} of the DG with $E_G = 1.1\,\text{eV}$ structure (see Fig. 6.8b) and the I_{ON} of the *p*-type DG with $E_G = 0.8\,\text{eV}$ one (see Fig. 6.8c). The differences in I_{OFF} and I_{ON} are attributed to the different reproduction of the tunneling mechanism at the contacts by the simulations. It appears that in the simulations performed with ViDES the tunneling process at the contacts is less affected by the higher effective mass of holes, thus resulting in a higher I_{OFF} and I_{ON}.

In general the I_{ON}/I_{OFF} ratios and SS are well reproduced, and we can confidently assume that our TCAD model predicts accurately the behavior of the devices, both when changing E_G and ϕ_{SB} and gate configuration (TG *vs* DG).

6.2.2 Optimized Device Structure and Switching Characteristics

Both structures presented in Sec. 6.1 are challenging to fabricate experimentally as they require an extremely small separation between the gated regions (which we named L_{OPEN} or also *Under-Lap* (UL)), which if not controlled properly might lead to shorts between the gates. Moreover these ungated regions could also have an impact on the conduction of carriers across the device. The DG structure, despite its superior performances, is even harder to fabricate since the patterning of the gates needs to be repeated twice. We will now use the developed TCAD model, validated with respect to the quantum simulations, to optimize the device structure and study the complete switching behavior of the scaled device.

A new optimized structure, that enables an easier fabrication process, is presented in

Fig. 6.9a, in comparison with the structures used in quantum simulations, schematically reproduced in Fig. 6.9b,c. The optimized structure enables the fabrication of the

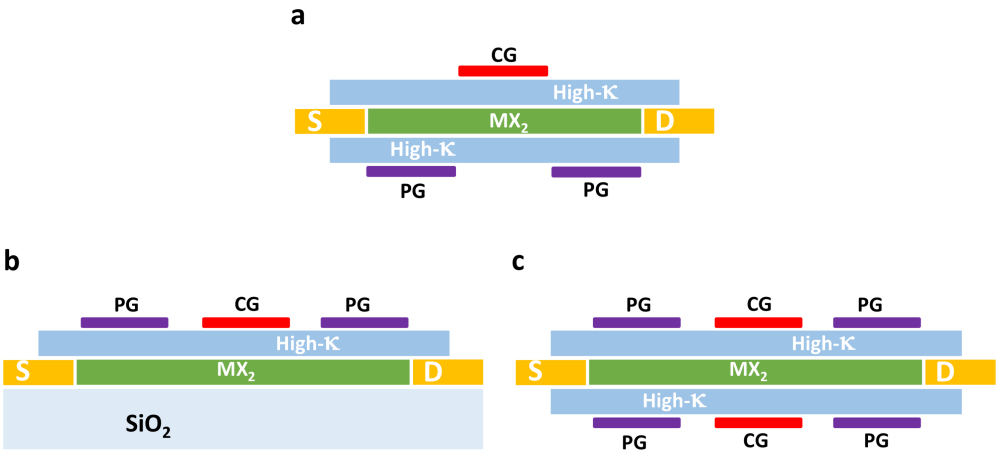


Figure 6.9 – Comparison between optimized, TG and DG structures. (a) Optimized device structure with the CG and PG acting from the top and bottom oxide respectively. As it can be seen the device is shorter than in the TG and DG geometry, even if the gated lengths are kept at 10 nm. **(b)** TG structure used in the Quantum and TCAD simulations. **c** structure used in the Quantum and TCAD simulations.

PG and CG on different levels, with the PG acting from the bottom oxide and theCG acting from the top-oxide. In this way we are able to drastically reduce the UL between the PG and CG down to 1 nm, thus enabling a shorter channel length and virtually no ungated regions in the channel (note that in the quantum simulations the distance between the gates, named L_{OPEN} was kept at 5 nm for the $L_G = 10$ nm length). The optimized structure results in a simpler fabrication process and allows the PG to modulate the carrier concentration under the contacts in case of a top-contact geometry. The electrostatic control over the channel is however inferior to the one enabled by the DG geometry, which as we explained presents a challenging fabrication process.

We can now use the developed TCAD model to fully characterize the switching behavior of the optimized gating structure. We use the same material parameters as the ones described in Sec. 6.2.1 and we optimize the symmetry between n- and p-type branches by tuning the ϕ_{SB} at the contacts. Since electrons have a lower effective mass (0.3 compared to 0.4 of holes for the modeled MX_2 material) the ϕ_{SB} is increased up to 0.485 eV for electrons while it is reduced to 0.315 eV for holes. The tuning of the ϕ_{SB} results in matched transfer characteristics at $|V_{DS}| = 1$ V, as can be seen in Fig. 6.10. Fig. 6.10a shows the $I_{ds}V_{CG}$ at $|V_{DS}| = 1$ V and Fig. 6.10b compares the $I_{ds}V_{CG}$ and $I_{ds}V_{PG}$ transfer characteristics. It can be seen how the higher gate capacitance of the PG, acting both at source and drain, results in a lower SS, but the I_{ON} and I_{OFF} current levels match the ones simulated in the $I_{ds}V_{CG}$ characteristics (see Fig. 6.10).

Further analysis of the transfer characteristics is presented in Sec. 6.2.3. By sweeping

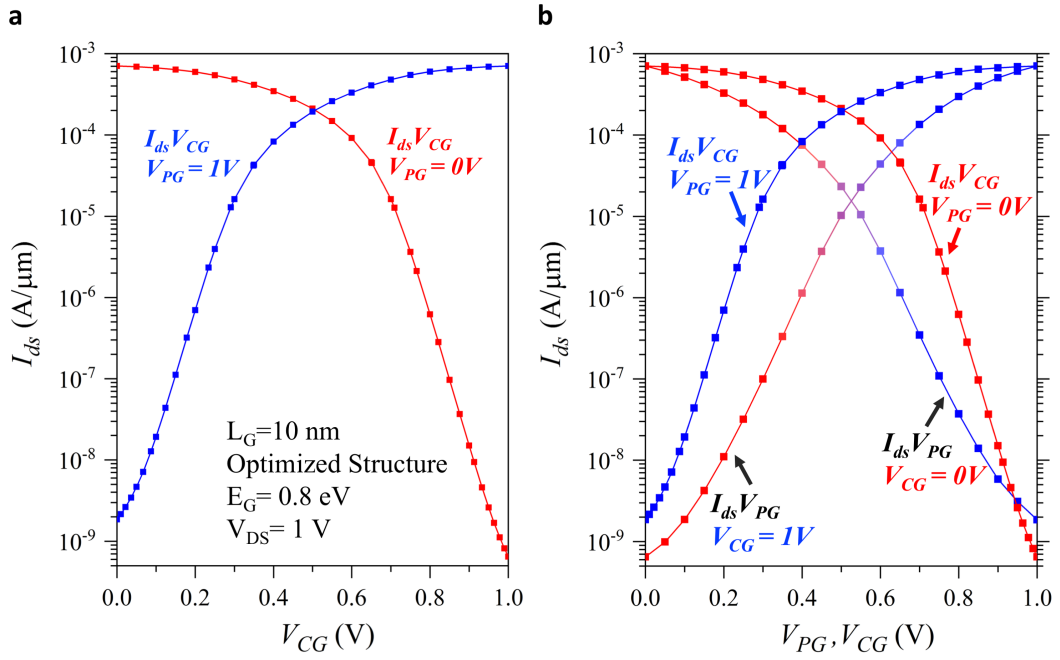


Figure 6.10 – Matched $I_{ds}V_{CG}$ and $I_{ds}V_{PG}$ transfer characteristics. (a) $I_{ds}V_{CG}$ obtained at $|V_{DS}| = 1\,\mathrm{V}$ for the optimized structure for both *n*- and *p*-type operations. **(b)** $I_{ds}V_{PG}$ and $I_{ds}V_{CG}$ characteristics. Notice how the polarity of the device is changing during the V_{PG} sweep.

both the CG and PG we can finally obtain a complete current map of the device, that fully describes fully the switching behavior, as shown in Fig. 6.11 for $|V_{DS}| = 1\,\mathrm{V}$. Repeating this simulation for multiple values of $|V_{DS}|$ can provide us with a description of the device switching properties, that once converted in a table model, could be used for larger circuits simulation. We also simulated the output characteristics ($I_{ds}V_{DS}$) for both *n*- and *p*-type operation ($V_{PG} = 1\,\mathrm{V}$ and $V_{PG} = 0\,\mathrm{V}$ respectively) for different values of V_{CG}, see Fig. 6.12. The $I_{ds}V_{DS}$ show a variation of the slope in the linear region, which is attributed to the disappearing Schottky barrier at drain, when increasing the V_{DS} bias. The effect is more marked in the *n*-type output characteristics (Fig. 6.12b) because of the higher ϕ_{SB}.

6.2.3 Detailed Analysis of Transfer Characteristics for a XOR gate

When studying the switching characteristics of the device we also want to consider how the device will be integrated in a logic gate. For unate gates, such as *Inverter* (INV), *NOT-AND* (NAND) and *NOT-OR* (NOR), the transistor polarity is fixed and the device behaves always as *n*- or *p*-type. In the case of binate functions, such as *2-Input Exclusive OR* (XOR-2) and *3-Input Exclusive OR* (XOR-3) and also for *3-Input Majority* (MAJ-3) gates, the device polarity will change at run-time, as the PG is controlled by a varying

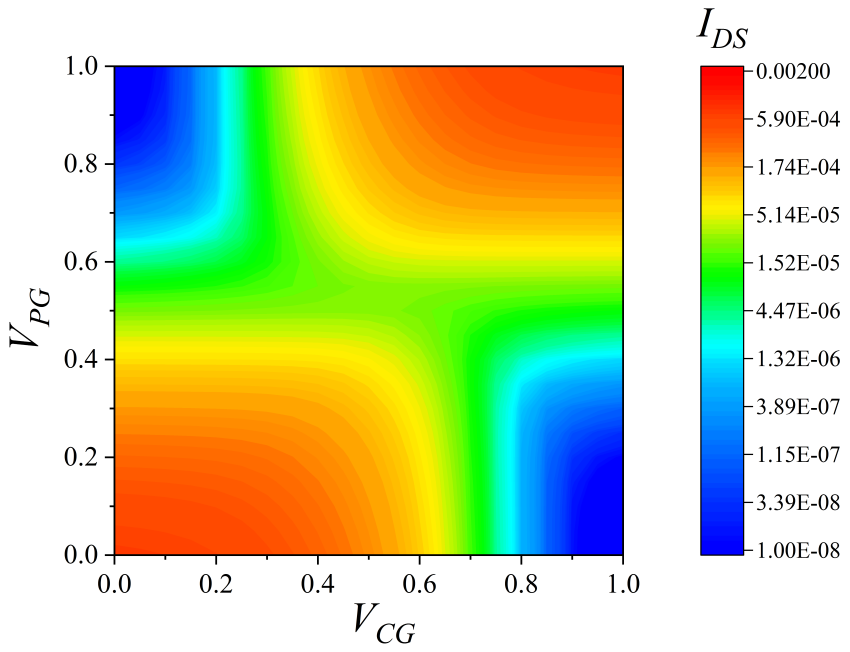


Figure 6.11 – Complete current map of the device. The plot is obtained by sweeping both the CG and PG gate at a constant $V_{DS} = 1\,\mathrm{V}$.

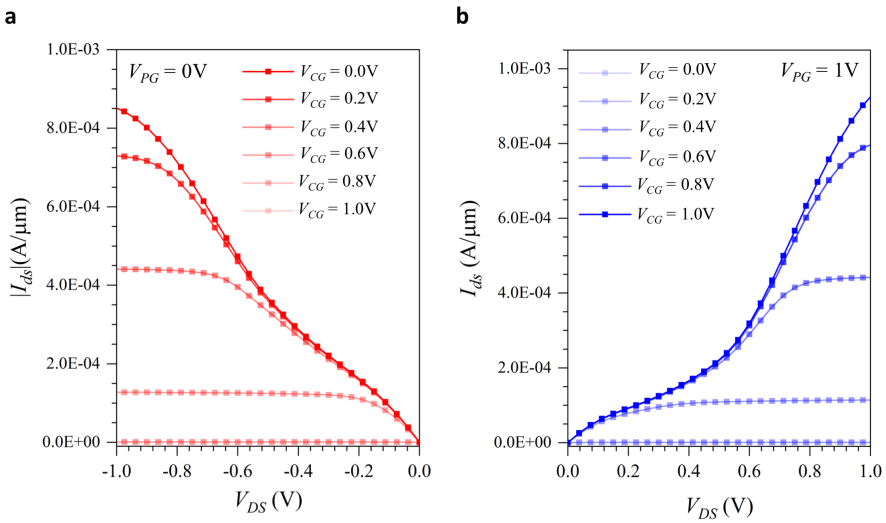


Figure 6.12 – Simulated output characteristics. (a) $I_{ds}V_{DS}$) for p-type operation. **(b)** $I_{ds}V_{DS}$) for n-type operation.

logic signal, leading to few differences in the device transfer characteristics.

To better elucidate this point we take the case study of a XOR-2 gate, realized with polarity-controllable devices, as shown in Fig. 6.13. As it can be seen in Fig. 6.13a, according to the value of logic input A and B each transistor can be operating in different

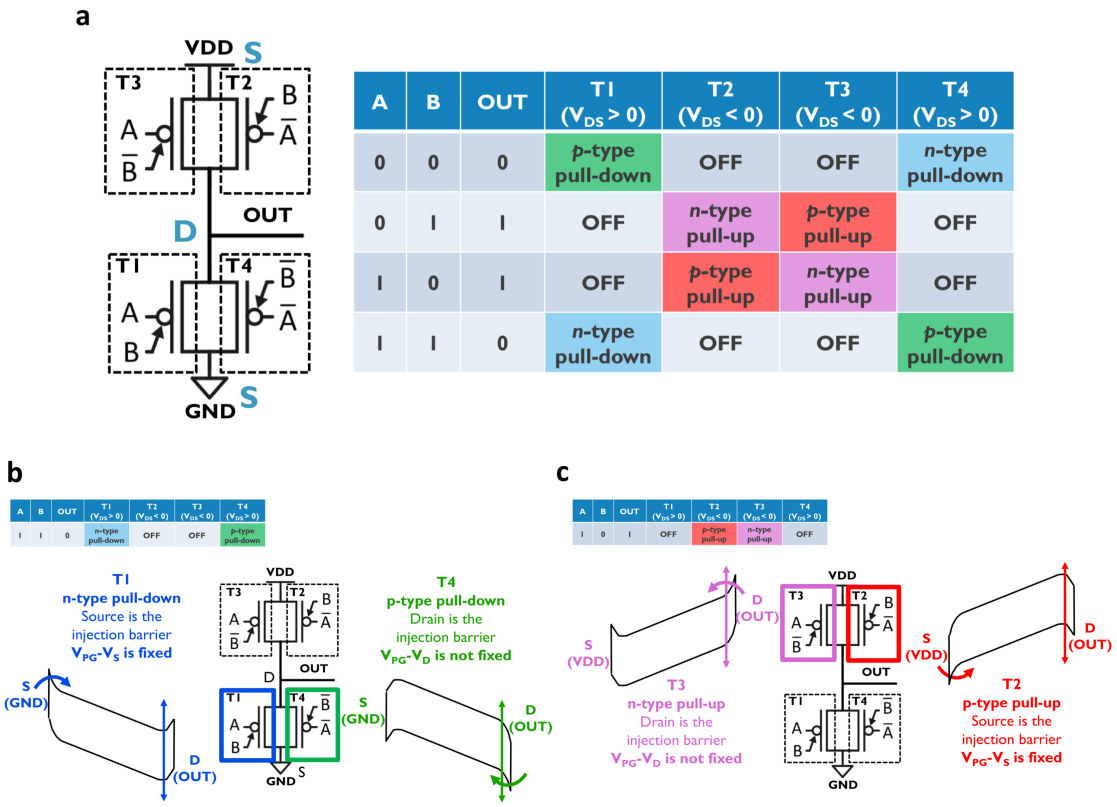
modes, according to the logic inputs applied:

(i) p-type pull-up, with $V_{PG} = GND$ (logic '0') and $V_{DS} < 0\,\text{V}$.

(ii) p-type pull-down, with $V_{PG} = GND$ (logic '0') and $V_{DS} > 0\,\text{V}$.

(iii) n-type pull-down, with $V_{PG} = Supply\ Voltage\ (V_{DD})$ (logic '1') and $V_{DS} > 0\,\text{V}$.

(iv) n-type pull-up, with $V_{PG} = V_{DD}$ (logic '1') and $V_{DS} < 0\,\text{V}$.



A	B	OUT	T1 ($V_{DS} > 0$)	T2 ($V_{DS} < 0$)	T3 ($V_{DS} < 0$)	T4 ($V_{DS} > 0$)
0	0	0	*p*-type pull-down	OFF	OFF	*n*-type pull-down
0	1	1	OFF	*n*-type pull-up	*p*-type pull-up	OFF
1	0	1	OFF	*p*-type pull-up	*n*-type pull-up	OFF
1	1	0	*n*-type pull-down	OFF	OFF	*p*-type pull-down

Figure 6.13 – Analaysis of transistors behavior in XOR gate. **(a)** Circuit schematic of the XOR gate and table describing the transistor operation for each combination of logic inputs. **(b,c)** Transistors operation with schematic band-diagram for A = '1' and B ='1' **(b)** and **(c)** for A = '1' and B = '0'.

In Fig. 6.13b we look at the mode of operation of the devices for A = '1' and B = '1', with the output of the XOR gate being '0'. In this configuration we have transistor T2 and T3 OFF, transistor T1 operates as (iii) n-type pull-down and transistor T4 operates as (ii) p-type pull-down. In Fig. 6.13c we have A = '1' and B = '0', with the output of the XOR gate being '1'. In this configuration we have transistor T1 and T4 OFF, transistor T2 operates as (i) p-type pull-up and transistor T3 operates as (iv) n-type pull-up. When transistor T4 operates in mode (ii) and transistor T3 operates as (iv)

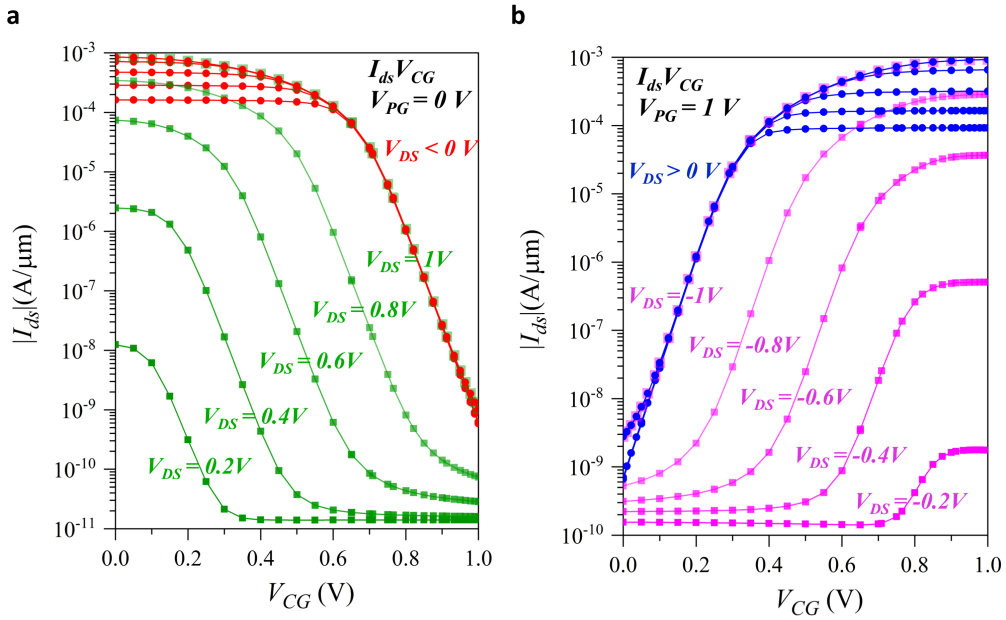


Figure 6.14 – Transfer characteristics for positive and negative V_{DS} for both *n*- and *p*-type operation. (a) $I_{ds}V_{CG}$ curves for *p*-type operations. The negative V_{DS} values, curves in red, are -0.2, -0.4, -0.6, -0.8 and -1 V. **(b)** $I_{ds}V_{CG}$ curves for *n*-type operations. The positive V_{DS} values, curves in blue, are 0.2, 0.4, 0.6, 0.8 and 1 V.

we can see how the injection barrier is at drain (output terminal) and not at source. A consequence of this the injection barrier is being modulated during the transition of the output (*i.e.* the potential difference $V_{PG} - V_D$ is not fixed). This is considerably different from operation mode (i) and (iii), where the the injection barrier is constantly modulated by the $V_{PG} - V_S$ bias. The modulation of the injection barrier at drain in the case of *p*-type pull-down ($V_{DS} > 0\,\text{V}$) and *n*-type pull-up ($V_{DS} < 0\,\text{V}$), causes the device to display different switching characteristics then is the case of a *p-type* pull-up ($V_{DS} < 0\,\text{V}$) and *n*-type pull-down ($V_{DS} > 0\,\text{V}$), as shown in Fig. 6.14. We can also notice how the larger ϕ_{SB} for electrons causes the *n*-type current, for low negative V_{DS} biases, to be lower than the hole current at the same, but positive, V_{DS}. As it can be seen in Fig. 6.14, when $|V_{DS}| = 1\,\text{V}$ the symmetric structure of the device enables the transfer characteristic to match again, as now the drain barrier is modulated by the same potential difference.

This analysis shows that when the output capacitance of the gate is charged and discharged, during a logic transition, the current that flows in each of the devices placed in parallel (see 6.13a) can be considerably different. Similar considerations apply for the $I_{ds}V_{PG}$ transfer characteristics.

6.2.4 Logic Gates Simulations

Sentaurus Device offers the possibility to performs small circuit simulations within the TCAD environment, without the need to develop a compact model. It is sufficient to define a device structure and in the system section define a netlist where the devices can be inserted together with other electronic components (such as voltage sources, resistors, capacitors, *etc*...). Sentaurus Device is then able to couple the Poisson and continuity equation for each device and self-consistently solve the entire circuit defined by the netlist.

We used this technique to study the switching speed and *Energy-Delay Product* (EDP) of different logic gates (*Fan-Out of 4* (FO4) INV, NAND, XOR-2, XOR-3 and MAJ-3) realized with the scaled polarity-controllable devices presented in Sec. 6.2.2. For certain logic gates the EDP computed is compared to the BCB 3.0 (as shown in Fig. 6.18). In order to accurately estimate the delay of the logic gates it is paramount to evaluate the output capacitance to be added on the output node. This capacitance depends on the interconnection capacitance and the capacitance of the load (proportional to size of devices and fan-out). In our simulations we considered the following:

- The metal-1 *half-pitch* (F) is set to 20 nm. Considering the length of each gated segment ($L_G = 10\,\text{nm}$) to be equal to the width of the metal-1 interconnect, we get a metal-1 pitch of 42 nm. F is then approximated to 20 nm.
- The minimum transistor width is set to 4 F, in accordance with BCB 3.0 [25]. All the simulations use minimum-size devices.
- The length of the interconnect at the output is set to 20 F, in accordance with BCB 3.0 [25]. The capacitance of the interconnect ($C_{int} = 126\,\text{aF}/\mu\text{m}$) is also taken from BCB 3.0.
- V_{DD} is set to 1 V.
- Each logic gate simulated, except for the FO4 INV, is loaded with the aforementioned C_{int} and with the capacitance of an inverter ($C_{INV} = 750\,\text{aF}/\mu\text{m}$. C_{INV} is extracted directly from the simulations by evaluating the delay of an INV chain and then replacing the output INV with the appropriate C_{INV} in order to match the output behavior previously simulated. The value of C_{INV} calculated matches the one extracted with the traditional formula describing the inverter delay [197]:

$$\tau = \frac{CV_{DD}}{2}\frac{1}{I_{eff}} \tag{6.2}$$

where

$$I_{eff} = \frac{(I_{ds}(V_{GS} = V_{DD}/2, V_{DS} = V_{DD})) + (I_{ds}(V_{GS} = V_{DD}, V_{DS} = V_{DD}/2))}{2} \tag{6.3}$$

We extracted $\tau = 1.75\,\text{ps}$ and evaluated $I_{eff} = 200\,\mu\text{A}/\mu\text{m}$, thus giving us

$$C = \frac{2\tau}{V_{DD}} I_{eff} = 720\,\text{aF}/\mu\text{m} \tag{6.4}$$

- The total load capacitance ($C_L = C_{INV} + C_{int}$), while for the FO4 INV we set $C_L = 4C_{INV} + 3C_{int}$. We multiplied the C_{int} by only a factor of 3, to account for shared interconnects of the fan-out.
- The energy required during a logic transition is computed via the conventional formula

$$E = C_L V_{DD}^2 \tag{6.5}$$

- The logic gates are realized with the circuit schematics reported for the experimental devices in Fig. 5.6. The inverted input signal are generated by a voltage source, together with the primary inputs.
- The propagation delays for rising and falling transitions (t_{dr} and t_{df} respectively) of the logic gates are extracted from the transient simulations at the 50% level of input and output signals (0.5 V in our simulations).

The switching behavior of the simulated FO4 INV is reported in Fig. 6.15. We extracted $t_{dr} = 6.5\,\text{ps}$ and $t_{df} = 7\,\text{ps}$. This is in agreement with the delays that we extracted for a fan-out of 1 INV and for a fan-out free inverter ($t_d = 2.7\,\text{ps}$ and $t_d = 1.25\,\text{ps}$ respectively). Fig. 6.16 shows the switching behavior of the simulated NAND and XOR-2 gates. In this case for the NAND gate we extracted $t_{dr} = 4\,\text{ps}$ and $t_{df} = 8\,\text{ps}$, while for the XOR-2 gate $t_{dr} \approx t_{df} = 2.25\,\text{ps}$. As expected, given the minimum size of the transistors, the t_{df} of the NAND gate is roughly twice the t_{dr}. The XOR-2 gate presents instead $t_{dr} \approx t_{df}$, thanks to the pass-gate configuration shown in 6.13. The XOR-2 has always 2 transistors conducting in parallel, as explained in detail in Sec. 6.2.3), thus lowering the effective resistance and allowing a higher current to charge and discharge the output capacitance. In order to be accurate, we also factored in the delay that would be introduced by the INV needed to generate the inverted A and B signals. We thus obtained the final propagation delay for the XOR-2 gate to be $t_{dr} \approx t_{df} \approx 5\,\text{ps}$. The switching behavior of the simulated XOR-3, and MAJ-3 gates are shown in Fig. 6.17. A similar consideration as the one presented for the XOR-2 gate applies and the delays are again similar, with $t_{dr} \approx t_{df} = 2.75\,\text{ps}$. Also in this case we added the delay of the INV needed to generate the inverted signals and obtained $t_{dr} \approx t_{df} \approx 5.5\,\text{ps}$. Since the XOR-2, XOR-3 and MAJ-3 have the same size (*i.e.* number of transistors) and are driving the same load, it is reasonable to find that their propagation delay is comparable.

Finally, in Fig. 6.18, the EDP of FO4 INV, NAND and XOR-2 gates are compared with the ones of other emerging technologies, that have been evaluated in BCB 3.0 [25]. As it can be seen in Fig. 6.18a,b, when synthesizing unate functions, 2D-DIG transistors

do not perform better than the projected *Complementary Metal-Oxide-Semiconductor* (CMOS) devices, as they are inherently longer and provide lower ON-currents. The projected EDP of a FO4 INV and of a NAND gate realized with 2D DIG-FETs are roughly 5× and 2× higher than conventional CMOS logic gates. The advantage of using 2D DIG-FETs in this case would only come from the possibility of having a doping-free process and the possibility of *Back-End-Of-the-Line* (BEOL) integration. However, the enhanced expressivity of the DIG devices gives the possibility to realize compact XOR-2 gates, that have only 4 transistors, and are considerably faster than CMOS, as it can be appreciated in Fig. 6.18c. The projected EDP of a XOR-2 gate realized with 2D DIG-FETs is around 6× lower than any other emerging technology. Since for both XOR-3 and MAJ-3 gates we extracted propagation delays similar to the XOR-2, we can assume that they will also perform faster that with any other available technology, although in BCB 3.0 these gates are not evaluated. Moreover, we want to remark that the BCB 3.0 is usually considered as highly optimistic, and the values reported in BCB 3.0 are obtained only through analytic equations, taking into account solely the ON currents and the power supply predicted for the devices. We believe that our simulations, performed with Sentaurus TCAD, provide a more realistic estimation of the performances of our logic gates, thus the EDP comparison might be more favorable than the values reported above.

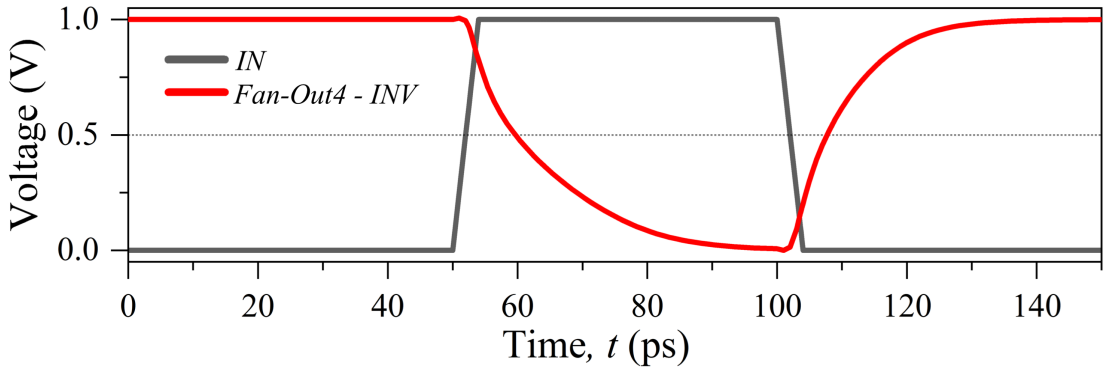


Figure 6.15 – Switching behavior of the simulated FO4 INV.

6.3 Summary

We first evaluated scaling trends and device performances for 2D polarity-controllable FETs using self-consistent ballistic quantum-transport simulations. The device concept presents the great advantage of using only a single 2D channel material for both device polarities and does not require complex doping techniques. We showed the feasibility of controllable-polarity behaviour at the nanoscale level thanks to the additional program gate introduced in the device geometry. We first simulated the performances of mono- and bi-layer WSe_2, as a channel material, and found that the high semiconducting band-gap

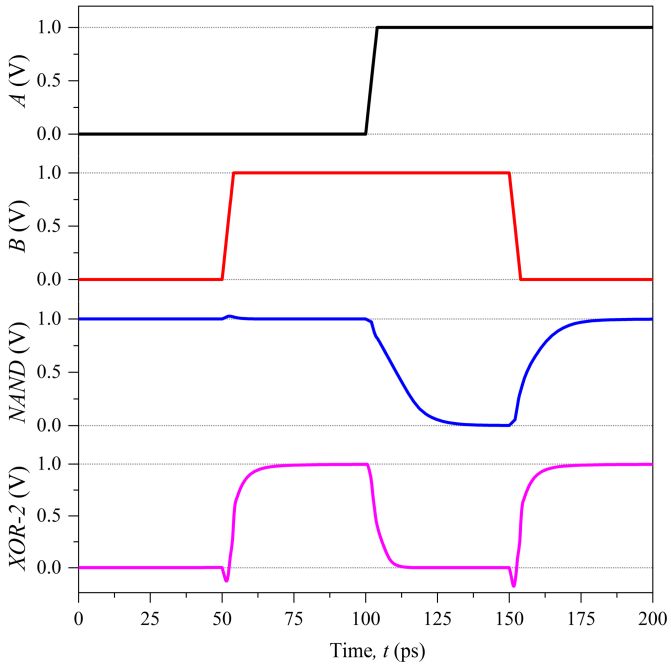


Figure 6.16 – Switching behavior of the simulated NAND and XOR-2 logic gates.

(1.5 eV and 1.1 eV respectively) prevents achieving high ON-currents. Thus we studied the benefits of bilayer-MX_2 materials, such as $ZrSe_2$, HfS_2, or $HfSe_2$, for which ab-initio simulations have shown the presence of a lower semiconducting bandgap (0.7-0.9 eV). Due to the lack of experimental characterization and the disagreement between different ab-initio simulations, we modeled a bilayer-MX_2 with electrical properties (effective masses and bandgap) within the values reported in literature [185] [186] [187]. For the simulated MX_2 material, we showed $I_{ON} > 10^3\,\mu A/\mu m$ and $I_{ON}/I_{OFF} > 10^5$ down to $L_G = 5\,nm$ for both p- and n-type polarities. These performances are comparable with the ones predicted, using ballistic self-consistent transport simulations, for conventional doped devices based on 2D-TMDCs [183] [198] [47] [48], and thus show a feasible scaling path for 2-dimensional polarity-controllable devices for beyond-CMOS flatronics.

Following this analysis, in order to study the performances of logic gates we developed a Synopsis Sentaurus TCAD simulation that is able to reproduce the switching characteristics simulated with the quantum-transport simulations. The switching characteristics of the devices are then studied in great detail, and we performed transient simulations of logic gates. It was found that the projected EDP of a FO4 INV and of a NAND gate realized with 2D DIG-FETs are roughly 2× and 3× higher than conventional CMOS logic gates. The advantage of using 2D DIG-FETs in this case would only come from the possibility of having a doping-free process and the possibility of BEOL integration. However, the enhanced expressivity of the DIG devices gives the possibility to realize compact XOR-2 gates, that have only 4 transistors, and are considerably faster than

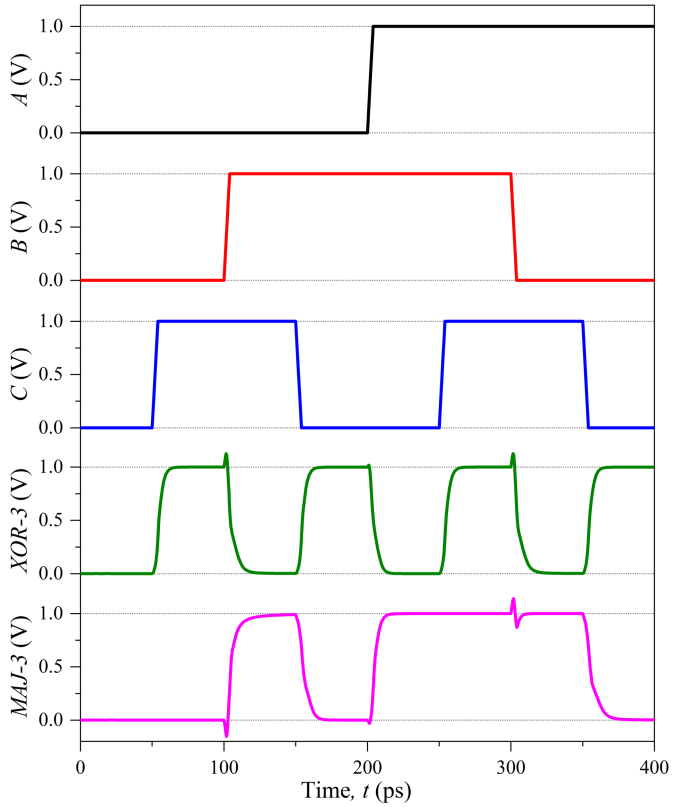


Figure 6.17 – Switching behavior of the simulated XOR-3 and MAJ-3 logic gates.

CMOS. The projected EDP of a XOR-2 gate realized with 2D DIG-FETs was found to be around 6× lower than any other emerging technology studied in BCB 3.0.

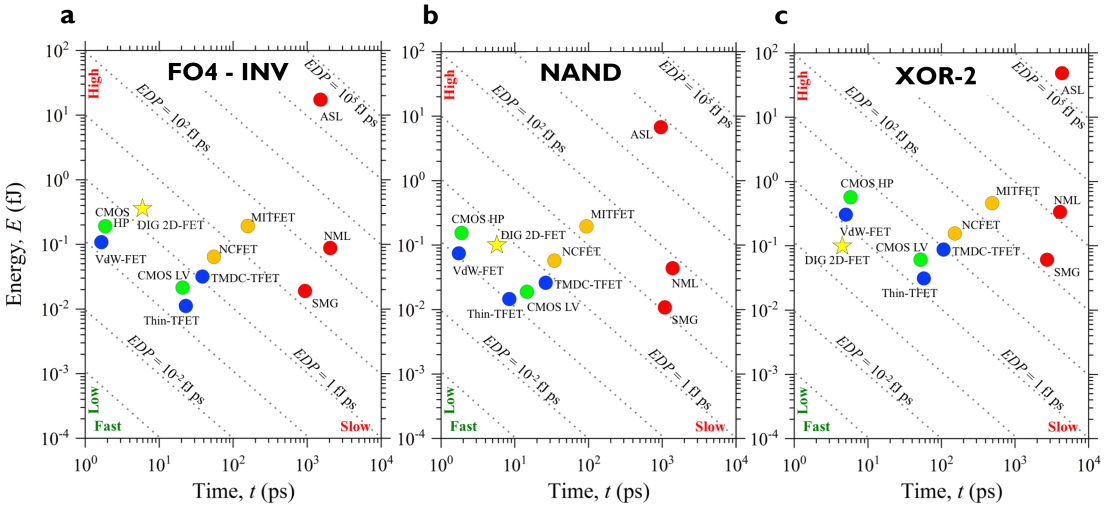


Figure 6.18 – Energy-Delay Product for selected logic gates compared with other devices reported in BCB 3.0. **(a)** EDP of Fan-Out of 4 INV gate. The projected EDP of a FO4 INV is roughly 2× higher than conventional CMOS. **(b)** EDP of NAND gate. The projected EDP of a NAND is roughly 3× higher than conventional CMOS. **(c)** EDP of XOR-2 gate. The projected EDP of a XOR-2 gate realized with 2D DIG-FETs is around 10× lower than any other emerging technology.

7 Conclusions and Future Perspectives

It's a dangerous business, Frodo, going out your door.
You step onto the road, and if you don't keep your feet,
there's no knowing where you might be swept off to.

— The Lord of the Rings,
John Ronald Reuel Tolkien

The work conducted in this thesis was motivated by the interest of the electronic industry and the research community in novel semiconducting materials. In particular this thesis focused on *Transition Metal Di-Chalcogenides* (TMDCs), a class of *Two-Dimensional* (2D) materials that has recently been investigated as a possible silicon replacement for novel electronic devices. TMDCs materials are also appealing in the near term for co-integration with Silicon CMOS in a 3D monolithic structure. One of the main challenges with TMDCs is the development of a stable and CMOS-compatible doping technique, and to date that is not yet being achieved. Our innovative approach enables us to realize doping-free devices, whose polarity can be dynamically controlled at run-time. The key concepts that have been highlighted throughout this thesis are now briefly summarized:

- Atomically-thin 2D TMDCs are, thanks to their physical and electrical properties, an exceptional vector for the exploration of next-generation semiconductor devices
- Since stable and CMOS-compatible doping technique for 2D TMDCs has not yet been developed, the use of electrostatic doping appears a promising alternative.
- Undoped *Schottky-Barrier* (SB) *Field-Effect Transistors* (FETs) are used for the conduction of both types of charge carriers (*i.e.* electrons and holes).
- The ambipolar behavior provides an added degree of freedom for the realization of doping-free 2D devices.
- A *Double-Independent-Gate* (DIG) structure allows us to control the polarity of the transistor at run-time, exploiting the effect of electrostatic doping. An additional

gate (named *Polarity Gate* (PG)), is able to control the polarity of the devices by tuning the Schottky barriers at the contacts, while a conventional gate, named *Control Gate* (CG), placed in the central region of the channel controls the ON/OFF status of the device for both polarities. With this particular gate configuration, the device switching properties lead to highly compact logic gates, *i.e.* XOR and MAJ, and create the opportunity to explore novel design styles and tools for logic synthesis.

7.1 Overview of Thesis contribution

The main achievements of this thesis are here summarized:

- The demonstration of the first polarity-controllable *tungsten di-selenide* (WSe_2) transistor, and the first device on any 2D semiconductor to exhibit polarity-control with I_{ON}/I_{OFF} ratios greater than 10^6 for both polarities on the same device. This achievement is the focus of Ch. 4 and resulted in the following publications [28], [29] and [30]. The results are also featured in two book chapter dedicated to *Multiple-Independent-Gate* (MIG) devices [31] and polarity-controllable WSe_2 devices [32].
- The demonstration of the first logic gates realized with doping-free polarity-controllable FETs on 2D-WSe_2. A complete standard-cell library (*Inverter* (INV), *NOT-AND* (NAND), *NOT-OR* (NOR), *2-Input Exclusive OR* (XOR-2), *3-Input Exclusive OR* (XOR-3) and *Majority* (MAJ)) is experimentally shown. This library can be the basis for conventional logic synthesis tools to map any logic functionality. These results are described in detail in Ch. 5 and resulted in the following publications [33] and [34]. The achievements described in the chapter have also been featured in an oral presentation at the 2018 Flatlands beyond graphene conference.
- The study of scaling trends and performance evaluation for polarity-controllable devices on WSe_2 and on low-bandgap 2D-TMDCs. The simulations performed show a successful scaling path for low-bandgap 2D-TMDCs in the sub-10 nm dimensions. These results are described in detail in Ch. 6 and resulted in the following publication [35] and [29]. They are also featured in a book chapter dedicated to polarity-controllable WSe_2 devices [32].
- The evaluation of the propagation delay and *Energy-Delay Product* (EDP) for a variety of logic gates that are simulated within the Sentaurus TCAD environment, using an optimized device structure. The extracted propagation delays and EDP are compared to the ones of other emerging technologies studied in BCB 3.0 [25], showing how the implementation of XOR-2 gates with 2D DIG FETs can provide around 10× lower EDP than any other emerging technology. These results are still unpublished.

Overall this thesis has helped to push the field of doping-free MIG in the realm of 2D

electronics, providing experimental proof-of-concepts devices and demonstrating a library of doping-free logic gates, as well as accurate simulations assessing the performances of ultra-scaled transistors and logic gates. The work presented has also contributed to the IMEC beyond-CMOS core program and has been presented at the internal *Partner Technical Week* (PTW), where IMEC core partners (such as Intel, Samsung, Global Foundries, TSMC, etc...) are updated on the recent results achieved at IMEC.

7.2 Future Research

2D TMDCs are still a vibrant field of research, and given the interest of the community, further research should be conducted in the future to push forward doping-free polarity-controllable devices.

One of the top priorities for future research should be the growth of large-area ambipolar 2D materials with precise thickness control, in order to control the semiconducting bandgap. The selection of the material should be based on the requirements highlighted in Ch. 6 in terms of bandgap and effective masses. The use of large area material would drastically reduce the variability between fabricated devices, and more accurate experiments could be performed to statistically determine the influence of different process steps on the device performances. If a low-temperature growth (T $<450^{\circ}$ C, in line with the requirements for *Back-End-Of-the-Line* (BEOL) integration) cannot be achieved, research should also focus on improving the transfer process in order to retain the high-quality of the grown material and to not modify its conduction properties. A more reliable transfer process would avoid folds and cracks of the 2D material and prevent contamination with impurities, thus boosting the ON current of the devices. Experimental demonstration of a scaled device structure, similar to the ones presented in Ch. 6, should also be pursued after having gained a deeper understanding of the encapsulations process. As we showed in Appendix C, encapsulation with *Atomic Layer Deposition* (ALD) grown oxides can drastically change the conduction properties of the ambipolar 2D materials, and the most suitable oxide will vary with respect to the 2D material used. Moreover some efforts should be devoted to balancing the n- and p-type conduction branches (*i.e.* similar ON and OFF currents and V_{TH}), and it could be achieved by tunign the Schottky-barrier height at the contacts, as simulated in Ch. 6. The use of graphene contacts could be an interesting approach, as it would allow the PG to modulate the Fermi level of graphene and reduce the Schottky-barrier height.

Finally, further work should be conducted on the modeling side in order to formulate a compact model for the device operations that would fit the Quantum and TCAD simulations. The model could be used in the simulations of larger circuits and could be further enriched by modeling scattering or contact resistance. The accuracy of the model is paramount in order to obtain an accurate comparison with both scaled conventional Si-*Complementary Metal-Oxide-Semiconductor* (CMOS) and other beyond-CMOS technologies. More work can be done at circuit level, to study the impact of

wiring and intra-gate connections on the circuit perfromances, and asses the impact of the additional gate terminals required by DIG transistors.

A Cleaning Procedures and Characterization

In this appendix we give a brief overview of the cleaning procedures that are needed in order to produce high-quality, impurity-free flakes. This procedures not only aim at reducing the amount of residues present on the surface of the flake, but also take care of reducing the roughness of the substrate where the exfoliation or transfer is performed. Fig. A.1 shows an *Atomic Force Microscope* (AFM) image of a clean bare SiO_2 surface before any process has been performed. The parameter used to determine the surface roghness is the root mean square height (Rms(Sq)) that is extracted from the measurements with the dedicated image analysis software Gwiddion®. The optimal surface roughness for the *silicon di-oxide* (SiO_2) surface is around 0.11 nm, as reported in Fig. A.1.

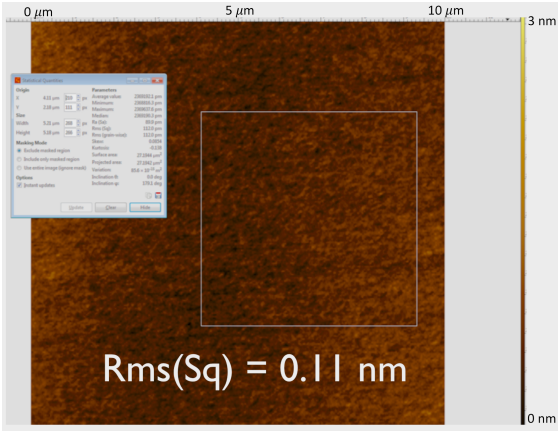


Figure A.1 – Surface roughness of bare SiO_2 blancket before any processing steps.

The first fabrication step that need to be performed is the deposition of the e-beam markers, that will be used by the system to align subsequent exposures. Moreover when working with flakes several more markers are patterned on the sample in order to be able to locate the best flakes within the sample. We studied the residues left on the SiO_2 surface after the marker deposition (with lift-off process) for 3 different e-beam recipes that have been developed at IMEC (see Fig. A.2). As it can be seen even after the standard Acetone (50°C) and *isopropyl alcohol* (IPA) (60°C) cleaning the surface is left with a considerable amount of residues. For the *polymethyl methacrylate* (PMMA) processes we found that a higher resist baking temperature results in the presence of

more residues, while the use of *Lift-Off Resist 1A* (LOR1A) shows the least amount of residues, despite the high temperature (190°C) needed to bake the LOR1A. However, the process with the double-layer resist (LOR1A and PMMA) involves the use of OPD developer and water, that we want to avoid as much as possible when *tungsten di-selenide* (WSe_2) is present on the surface, thus we focused on cleaning procedures for the PMMA process.

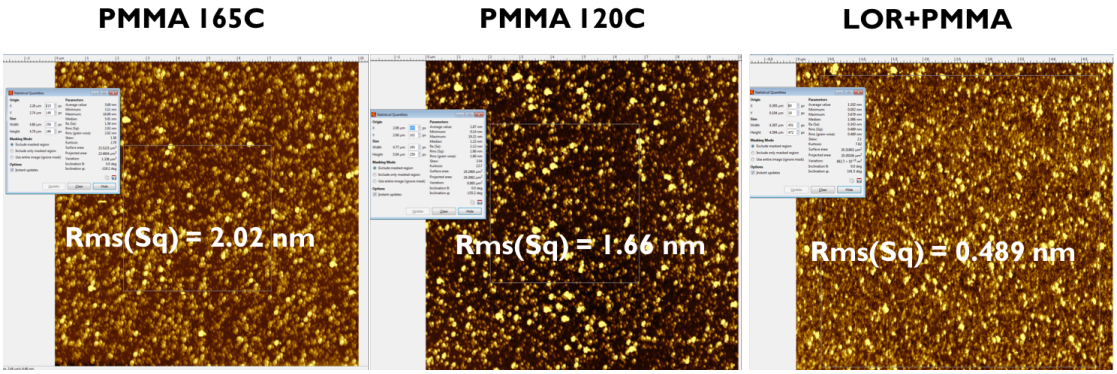


Figure A.2 – Residues on the Sio_2 surface after lift-off of e-beam markers for 3 different processes.

Despite the fact that the resist lift-off is performed in acetone (50°C) and that a mild ultrasonic bath (frequency = 40 KHz and power up to 100 W) is applied, this is not enough the remove the PMMA residues from the surface. Thus, we adopt a new procedure involving a 20 min sonication bath in hot acetone with a stronger sonicator (frequency = 40 KHz and power up to 470 W). Thanks to the higher intensity of the sonicator we achieve a residue-free surface for both PMMA-based processes (see Fig. A.3) with roughness comparable to the one of bare SiO_2.

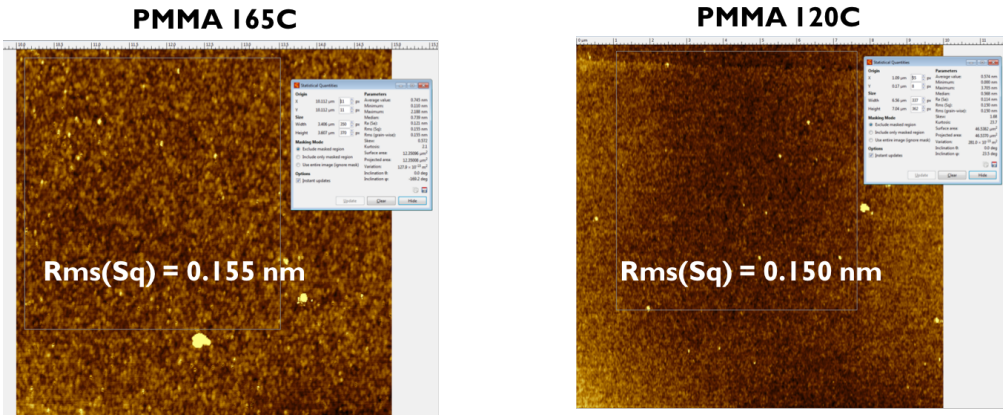


Figure A.3 – Removal of residues on the Sio_2 surface after lift-off of e-beam markers for PMMA-based processes.

After exfoliation the presence of tape residues on the surface of the flake (see Fig.

A.4) is a know issue and they can easily be removed with a 12 hours (overnight) hot acetone bath (50°C) and hot IPA wash. After this treatment the surface of the flake is clean and the roughness of the flake is comparable to the underlying SiO_2 substrate (see Fig. A.5).

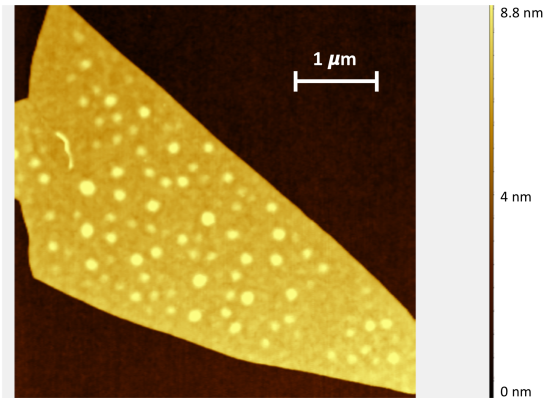


Figure A.4 – AFM image showing tape residues on exfoliated flake.

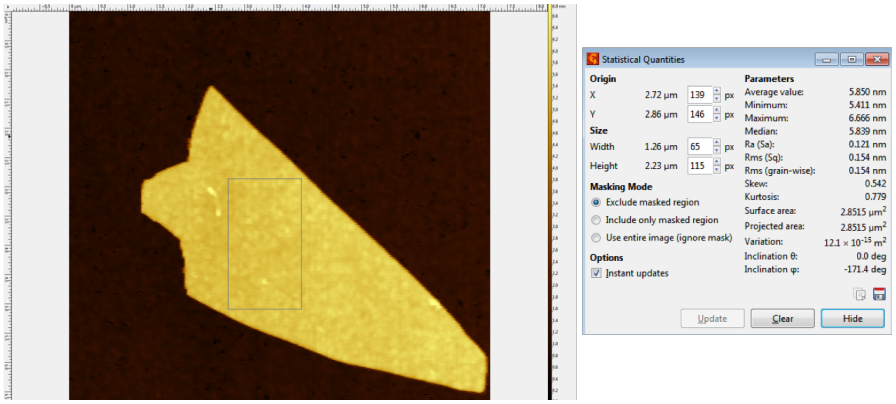


Figure A.5 – AFM image showing the exfoliated flake after cleaning procedure.

B Contact Annealing

The effect of contact annealing on our devices is discussed extensively in Sec. 4.2. Here we present measurements performed on a variety of WSe_2 flakes that show the same annealing effect (increase of the *p*-type ON-current and stable *n-type* ON-current) as the one presented in Fig. 4.4.

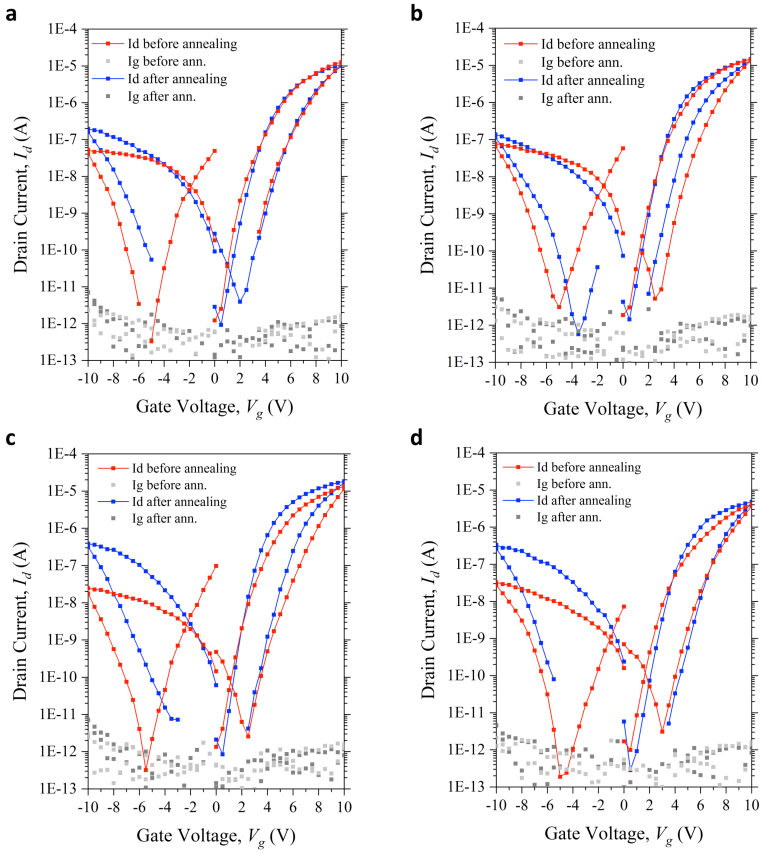


Figure B.1 – Effect of contact annealing on several WSe_2 flakes. The devices are annealed at 200° C for 12 hours in a Nabetherm® open-tube furnace, in vacuum with a constant *argon* (Ar) flow of 0.5 l/hr

C Effect of Oxide Encapsulation

Encapsulation of ambipolar WSe_2 was attempted with different processes in order to protect the 2D WSe_2 and realize top-gated devices. It was found that preserving the ambipolar behavior of WSe_2 is extremely challenging and requires accurate selection of the oxide and process conditions. Here we compare the effect of oxide encapsulation with *aluminium oxide* (Al_2O_3) and *zirconium di-oxide* (ZrO_2) in the following conditions:

- Encapsulation with Al_2O_3 deposited via *Atomic Layer Deposition* (ALD) using a commercial Cambridge Nanotech Savannah® tool. Al_2O_3 is deposited at 150° C starting from unheated H_2O and *trimethylaluminium* (TMA) precursors, and the transfer characteristics measured before and after encapsulation are presented in Fig. C.1.
- Encapsulation with Al_2O_3 deposited via ALD using a Pulsar® XP system, integrated in a Polygon 8200 platform, with H_2O and TMA precursors. In this process Al_2O_3 is grown in 2 steps: first 4 nm are deposited at low temperature (125° C) with a process optimized for growth on graphene, that should promote nucleation on the 2D surface, then the remaining 15 nm of Al_2O_3 are deposited at 200° C. The transfer characteristics measured before and after encapsulation are presented in Fig. C.2.
- Encapsulation with ZrO_2 deposited via ALD using a AMAT Centura III-V® module with H_2O and *tetrakis(ethylmethylamino)zirconium* (TEMAZ) precursors at 150° C. The transfer characteristics measured before and after encapsulation are presented in Fig. C.3.

As it can be seen in Fig. C.1 encapsulation in Al_2O_3 deposited with Savannah-ALD tool causes a complete suppression of the *p*-type current, while preserving or even enhancing *n*-type conduction. This behavior is attributed to poor nucleation on the 2D surface, creating a sub-stochiometric oxide with a higher number of defect sites (oxygen vacancies), inducing electron doping on the 2D semiconductor [199, 200]. When using a process tailored for growth on 2D materials, as in the case of Fig. C.2, the number of defects at the interface can be reduced and the *p*-conduction is not completely suppressed,

although it shows a reduction between 100 and 1000×. Again the *n*-current is enhanced suggesting the presence of electron doping from the Al_2O_3 layer. Encapsulation with ZrO_2 shows a drastically different behavior, and manages to preserve the ambipolar characteristics of the devices. Encapsulation with ZrO_2 results in an improved *p*-type conduction (that increases from 2× up to 100×) and a small reduction of *n*-current, making it a more suitable oxide for encapsulation of WSe_2 flakes. There was unfortunately not enough time to fabricate top-gated devices with ZrO_2 dielectric, but we believe these results clearly show a path for their realization.

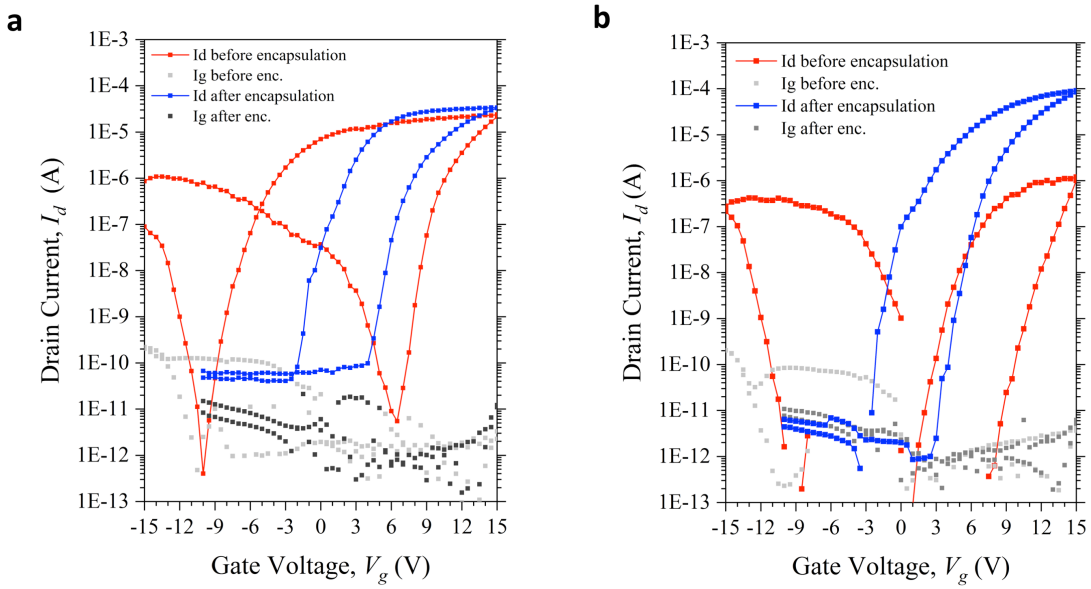


Figure C.1 – **(a,b)** Effect of Al_2O_3 encapsulation with ALD-Savannah, showing a complete suppression of the *p*-type branch.

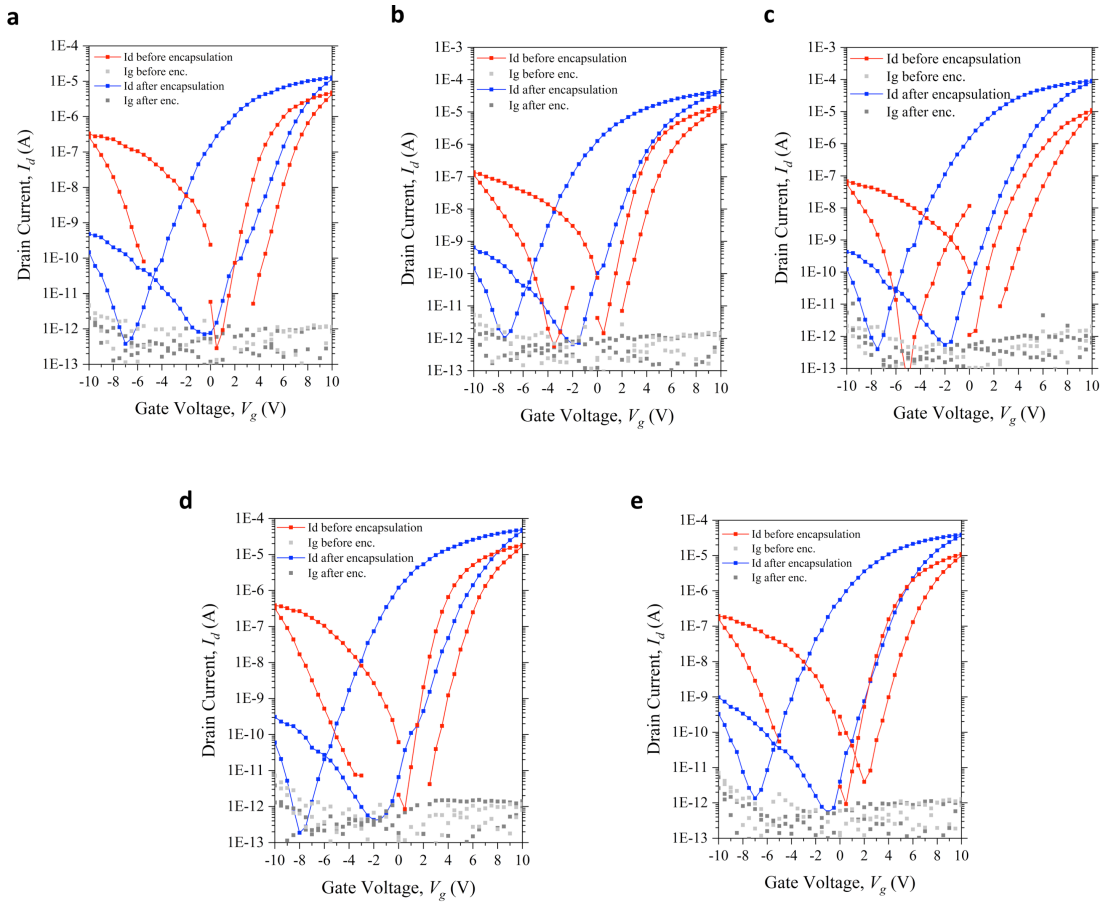


Figure C.2 – **(a-e)**Effect of Al_2O_3 encapsulation with ALD-Polygon, showing considerable degradation of the *p*-type ON-current.

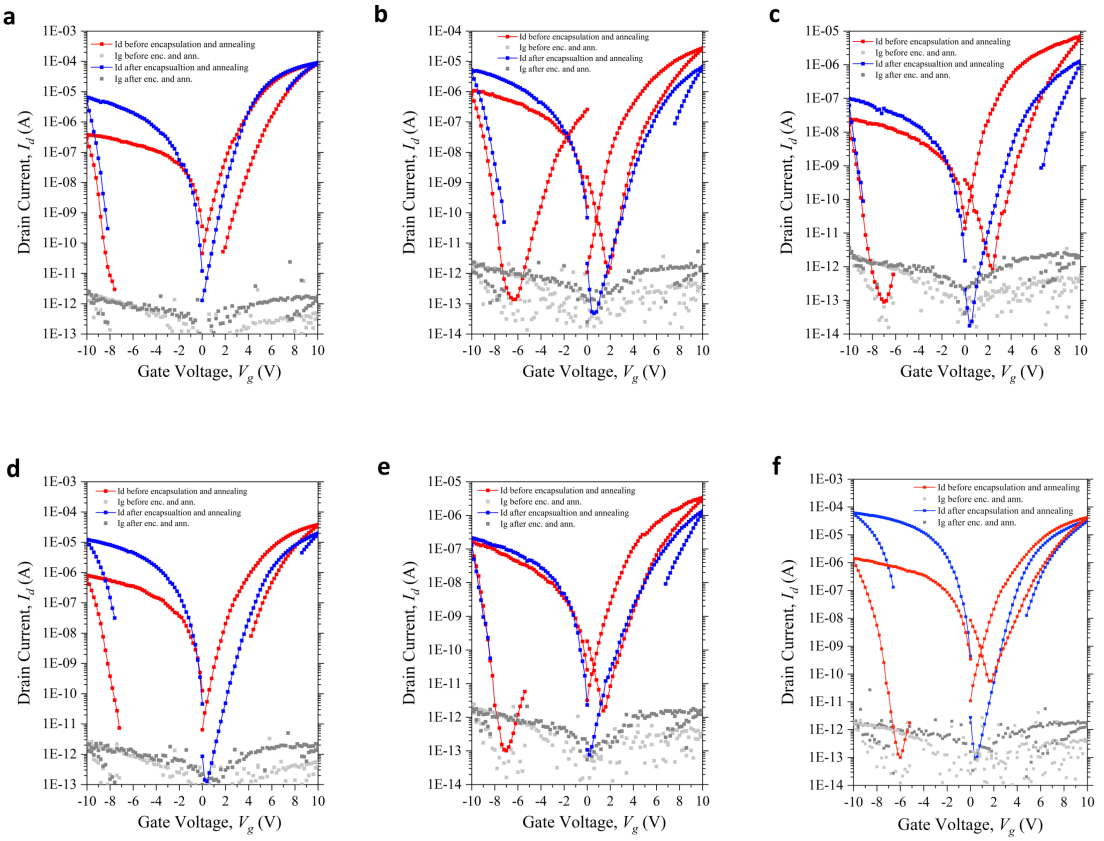


Figure C.3 – **(a-f)**Effect of ZrO_2 encapsulation with ALD-Centura III-V, showing the preservation of the ambipolar behavior and the enhancement of the *p*-current.

Bibliography

[1] Computer history museum. The Silicon Engine - A timeline of semiconductors in computers. https://www.computerhistory.org/siliconengine/, 2016. Accessed: 2019-02-10.

[2] John Kopplin. An Illustrated History of Computers, Part 4. http://www.computersciencelab.com/ComputerHistory/HistoryPt4.htm, 2002. Accessed: 2019-02-17.

[3] G. E. Moore. Cramming More Components onto Integrated Circuits. *Electronics*, 38:1, 1965.

[4] Robert H Dennard, Fritz H Gaensslen, V Leo Rideout, Ernest Bassous, and Andre R LeBlanc. Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE Journal of Solid-State Circuits*, 9(5):256–268, 1974.

[5] M Mitchell Waldrop. The chips are down for Moore's law. *Nature News*, 530(7589):144, 2016.

[6] Sayeef Salahuddin, Kai Ni, and Suman Datta. The era of hyper-scaling in electronics. *Nature Electronics*, 1(8):442, 2018.

[7] Shekhar Borkar. Designing reliable systems from unreliable components: the challenges of transistor variability and degradation. *Ieee Micro*, 25(6):10–16, 2005.

[8] Yiming Li, Chih-Hong Hwang, and Tien-Yeh Li. Random-dopant-induced variability in nano-CMOS devices and digital circuits. *IEEE Transactions on Electron Devices*, 56(8):1588–1597, 2009.

[9] Ming-Yi Shen, Adarsh Basavalingappa, Takeshi Hayakawa, Hidekazu Matsugi, Christopher Borst, and Stock Chang. Effect of Ion Flux in Source-Drain Extension Ion Implantation for 10-nm Node FinFet and beyond on 300/450mm Platforms. In *Ion Implantation Technology (IIT), 2016 21st International Conference on*, pages 1–4. IEEE, 2016.

[10] Yang Qiu, Fuccio Cristiano, Karim Huet, Fulvio Mazzamuto, Giuseppe Fisicaro, Antonino La Magna, Maurice Quillec, Nikolay Cherkashin, Huiyuan Wang, Sèbastien

Duguay, et al. Extended defects formation in nanosecond laser-annealed ion implanted silicon. *Nano letters*, 14(4):1769–1775, 2014.

[11] KK Tiong, PC Liao, CH Ho, and YS Huang. Growth and characterization of rhenium-doped mos2 single crystals. *Journal of crystal growth*, 205(4):543–547, 1999.

[12] Toby Hallam, Scott Monaghan, Farzan Gity, Lida Ansari, Michael Schmidt, Clive Downing, Conor P Cullen, Valeria Nicolosi, Paul K Hurley, and Georg S Duesberg. Rhenium-doped mos2 films. *Applied Physics Letters*, 111(20):203101, 2017.

[13] Joonki Suh, Tae-Eon Park, Der-Yuh Lin, Deyi Fu, Joonsuk Park, Hee Joon Jung, Yabin Chen, Changhyun Ko, Chaun Jang, Yinghui Sun, et al. Doping against the native propensity of mos2: degenerate hole doping by cation substitution. *Nano letters*, 14(12):6976–6982, 2014.

[14] Kapildeb Dolui, Ivan Rungger, Chaitanya Das Pemmaraju, and Stefano Sanvito. Possible doping strategies for mos 2 monolayers: An ab initio study. *Physical Review B*, 88(7):075420, 2013.

[15] Masihhur R Laskar, Digbijoy N Nath, Lu Ma, Edwin W Lee, Choong Hee Lee, Thomas Kent, Zihao Yang, Rohan Mishra, Manuel A Roldan, Juan-Carlos Idrobo, et al. p-type doping of mos2 thin films using nb. *Applied Physics Letters*, 104(9):092104, 2014.

[16] Lingming Yang, Kausik Majumdar, Han Liu, Yuchen Du, Heng Wu, Michael Hatzistergos, PY Hung, Robert Tieckelmann, Wilman Tsai, Chris Hobbs, et al. Chloride molecular doping technique on 2D materials: WS2 and MoS2. *Nano letters*, 14(11):6275–6280, 2014.

[17] Mahmut Tosun, Steven Chuang, Hui Fang, Angada B Sachid, Mark Hettick, Yongjing Lin, Yuping Zeng, and Ali Javey. High-gain inverters based on WSe_2 complementary field-effect transistors. *ACS nano*, 8(5):4948–4953, 2014.

[18] Lili Yu, Ahmad Zubair, Elton JG Santos, Xu Zhang, Yuxuan Lin, Yuhao Zhang, and Tomás Palacios. High-Performance WSe_2 Complementary Metal Oxide Semiconductor Technology and Integrated Circuits. *Nano letters*, 15(8):4928–4934, 2015.

[19] N. Waldron, S. Sioncke, J. Franco, L. Nyns, A. Vais, X. Zhou, H. C. Lin, G. Boccardi, J. W. Maes, Q. Xie, M. Givens, F. Tang, X. Jiang, E. Chiu, A. Opdebeeck, C. Merckling, F. Sebaai, D. van Dorp, L. Teugels, A. S. Hernandez, K. De Meyer, K. Barla, N. Collaert, and Y. Thean. Gate-all-around InGaAs nanowire FETS with peak transconductance of 2200 μS/μm at 50nm Lg using a replacement Fin RMG flow. In *2015 IEEE International Electron Devices Meeting (IEDM)*, pages 31.1.1–31.1.4, Dec 2015.

[20] Max M Shulaker, Gage Hills, Rebecca S Park, Roger T Howe, Krishna Saraswat, H-S Philip Wong, and Subhasish Mitra. Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. *Nature*, 547(7661):74, 2017.

[21] Branimir Radisavljevic, Aleksandra Radenovic, Jacopo Brivio, i V Giacometti, and A Kis. Single-layer MoS_2 transistors. *Nature nanotechnology*, 6(3):147, 2011.

[22] D. E. Nikonov and I. A. Young. Uniform methodology for benchmarking beyond-CMOS logic devices. In *2012 IEEE International Electron Devices Meeting*, pages 25.4.1–25.4.4, Dec 2012.

[23] O Zografos. Novel Design Paradigms for Beyond CMOS Devices - Modeling and Benchmarking of Spin-based Technologies, 2018.

[24] SA Wolf, DD Awschalom, RA Buhrman, JM Daughton, S Von Molnar, ML Roukes, A Yu Chtchelkanova, and DM Treger. Spintronics: a spin-based electronics vision for the future. *science*, 294(5546):1488–1495, 2001.

[25] Dmitri E Nikonov and Ian A Young. Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, 1:3–11, 2015.

[26] Sasikanth Manipatruni, Dmitri E Nikonov, and Ian A Young. Material targets for scaling all-spin logic. *Physical Review Applied*, 5(1):014002, 2016.

[27] Sasikanth Manipatruni, Dmitri E Nikonov, and Ian A Young. Beyond CMOS computing with spin and polarization. *Nature Physics*, 14(4):338, 2018.

[28] Giovanni V Resta, Surajit Sutar, Yashwanth Blaji, Dennis Lin, Praveen Raghavan, Iuliana Radu, Francky Catthoor, Aaron Thean, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Polarity control in WSe_2 double-gate transistors. *Scientific Reports*, 6, 2016.

[29] Giovanni Resta, Yashwanth Balaji, Tarun Agarwal Kumar, Iuliana Radu, Dennis Lin, Francky Catthoor, PE Gaillardon, and Nanni De Micheli. Polarity-controllable 2-dimensional transistors: experimental demonstration and scaling opportunities. 2017.

[30] G. V. Resta, J. R. Gonzalez, Y. Balaji, T. Agarwal, D. Lin, F. Catthor, I. P. Radu, G. De Micheli, and P. Gaillardon. Towards high-performance polarity-controllable FETs with 2D materials. In *2018 Design, Automation Test in Europe Conference Exhibition (DATE)*, pages 637–641, March 2018.

[31] Giovanni V Resta, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Functionality-Enhanced Devices: From Transistors to Circuit-Level Opportunities. In *Beyond-CMOS Technologies for Next Generation Computer Design*, pages 21–42. Springer, 2019.

[32] WSe_2 polarity-controllable devices. In *Functionality-Enhanced Devices An alternative to Moore's Law*, pages 71–86. Institution of Engineering and Technology, 2018.

[33] Giovanni V. Resta, Yashwanth Balaji, Dennis Lin, Iuliana P. Radu, Francky Catthoor, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Doping-Free Complementary Logic Gates Enabled by Two-Dimensional Polarity-Controllable Transistors. *ACS Nano*, 12(7):7039–7047, 2018.

[34] G. V. Resta, Y. Balaji, D. Lin, I. P. Radu, F. Catthoor, P. Gaillardon, and G. De Micheli. Doping-free complementary inverter enabled by 2D WSe2 electrostatically-doped reconfigurable transistors. In *2018 76th Device Research Conference (DRC)*, pages 1–2, June 2018.

[35] Giovanni V. Resta, Tarun Agarwal, Dennis Lin, Iuliana P. Radu, Francky Catthoor, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Scaling trends and performance evaluation of 2-dimensional polarity-controllable FETs. *Scientific Reports*, 7, 2017.

[36] Elizabeth Gibney. 2D OR NOT 2D. *Nature*, 522(7556):274, 2015.

[37] Philip Richard Wallace. The band theory of graphite. *Physical Review*, 71(9):622, 1947.

[38] JA Wilson and AD Yoffe. The transition metal dichalcogenides discussion and interpretation of the observed optical, electrical and structural properties. *Advances in Physics*, 18(73):193–335, 1969.

[39] Kostya S Novoselov, Andre K Geim, Sergei V Morozov, D Jiang, Y_ Zhang, Sergey V Dubonos, Irina V Grigorieva, and Alexandr A Firsov. Electric field effect in atomically thin carbon films. *science*, 306(5696):666–669, 2004.

[40] Deep Jariwala, Vinod K Sangwan, Lincoln J Lauhon, Tobin J Marks, and Mark C Hersam. Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides. *ACS nano*, 8(2):1102–1120, 2014.

[41] Qing Hua Wang, Kourosh Kalantar-Zadeh, Andras Kis, Jonathan N Coleman, and Michael S Strano. Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nature nanotechnology*, 7(11):699–712, 2012.

[42] Gianluca Fiori, Francesco Bonaccorso, Giuseppe Iannaccone, Tomás Palacios, Daniel Neumaier, Alan Seabaugh, Sanjay K Banerjee, and Luigi Colombo. Electronics based on two-dimensional materials. *Nature nanotechnology*, 9(10):768–779, 2014.

[43] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis. Single-layer MoS_2 transistors. *Nature nanotechnology*, 6(3):147–50, 2011.

[44] Han Wang, Lili Yu, Yi-Hsien Lee, Yumeng Shi, Allen Hsu, Matthew L. Chin, Lain-Jong Li, Madan Dubey, Jing Kong, and Tomas Palacios. Integrated Circuits Based on Bilayer MoS_2 Transistors. *Nano Letters*, 12(9):4674–4680, 2012.

[45] Manish Chhowalla, Debdeep Jena, and Hua Zhang. Two-dimensional semiconductors for transistors. *Nature Reviews Materials*, 1(11):16052, 2016.

[46] Wei Cao, Jiahao Kang, Deblina Sarkar, Wei Liu, and Kaustav Banerjee. 2D semiconductor FETs–Projections and design for sub-10 nm VLSI. *IEEE Transactions on Electron Devices*, 62(11):3459–3469, 2015.

[47] Varun Mishra, Samuel Smith, Kartik Ganapathi, and Sayeef Salahuddin. Dependence of intrinsic performance of transition metal dichalcogenide transistors on materials and number of layers at the 5 nm channel-length limit. In *Electron Devices Meeting (IEDM), 2013 IEEE International*, pages 5–6. IEEE, 2013.

[48] Youngki Yoon, Kartik Ganapathi, and Sayeef Salahuddin. How good can monolayer MoS_2 transistors be? *Nano letters*, 11(9):3768–3773, 2011.

[49] L. Liu, S. B. Kumar, Y. Ouyang, and J. Guo. Performance Limits of Monolayer Transition Metal Dichalcogenide Transistors. *IEEE Transactions on Electron Devices*, 58(9):3042–3047, 2011.

[50] Kibum Kang, Saien Xie, Lujie Huang, Yimo Han, Pinshane Y Huang, Kin Fai Mak, Cheol-Joo Kim, David Muller, and Jiwoong Park. High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature*, 520(7549):656–660, 2015.

[51] Kin Fai Mak and Jie Shan. Photonics and optoelectronics of 2D semiconductor transition metal dichalcogenides. *Nature Photonics*, 10(4):216, 2016.

[52] Dmitrii Unuchek, Alberto Ciarrocchi, Ahmet Avsar, Kenji Watanabe, Takashi Taniguchi, and Andras Kis. Room-temperature electrical control of exciton flux in a van der waals heterostructure. *Nature*, 560(7718):340, 2018.

[53] E. V. Calman, M. M. Fogler, L. V. Butov, S. Hu, A. Mishchenko, and A. K. Geim. Indirect excitons in van der Waals heterostructures at room temperature. *Nature Communications*, 9(1):1895, 2018.

[54] Pablo Alonso-González, Alexey Y. Nikitin, Yuanda Gao, Achim Woessner, Mark B. Lundeberg, Alessandro Principi, Nicolò Forcellini, Wenjing Yan, Saül Vélez, Andreas J. Huber, Kenji Watanabe, Takashi Taniguchi, Félix Casanova, Luis E. Hueso, Marco Polini, James Hone, Frank H. L. Koppens, and Rainer Hillenbrand. Acoustic terahertz graphene plasmons revealed by photocurrent nanoscopy. *Nature Nanotechnology*, 12:31 EP –, Oct 2016.

[55] Baicheng Yao, Yuan Liu, Shu Wei Huang, Chanyeol Choi, Zhenda Xie, Jaime Flor Flores, Yu Wu, Mingbin Yu, Dim Lee Kwong, Yu Huang, Yunjiang Rao, Xiangfeng Duan, and Chee Wei Wong. Broadband gate-tunable terahertz plasmons in graphene heterostructures. *Nature Photonics*, 12(1):22–28, 2018.

[56] KSA Novoselov, Andre K Geim, SVb Morozov, Da Jiang, MIc Katsnelson, IVa Grigorieva, SVb Dubonos, and AAb Firsov. Two-dimensional gas of massless Dirac fermions in graphene. *nature*, 438(7065):197–200, 2005.

[57] Kibum Kang, Saien Xie, Lujie Huang, Yimo Han, Pinshane Y. Huang, Kin Fai Mak, Cheol-Joo Kim, David Muller, and Jiwoong Park. High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature*, 520(7549):656–660, 2015.

[58] Ken Verguts, Yves Defossez, Alessandra Leonhardt, Joke De Messemaeker, Koen Schouteden, Chris Van Haesendonck, Cedric Huyghebaert, Stefan De Gendt, and Steven Brems. Growth of millimeter-sized graphene single crystals on al2o3(0001)/pt(111) template wafers using chemical vapor deposition. *ECS Journal of Solid State Science and Technology*, 7(12):M195–M200, 2018.

[59] Jiadong Zhou, Junhao Lin, Xiangwei Huang, Yao Zhou, Yu Chen, Juan Xia, Hong Wang, Yu Xie, Huimei Yu, Jincheng Lei, Di Wu, Fucai Liu, Qundong Fu, Qingsheng Zeng, Chuang-Han Hsu, Changli Yang, Li Lu, Ting Yu, Zexiang Shen, Hsin Lin, Boris I. Yakobson, Qian Liu, Kazu Suenaga, Guangtong Liu, and Zheng Liu. A library of atomically thin metal chalcogenides. *Nature*, 556(7701):355–359, 2018.

[60] Hua Yu, Mengzhou Liao, Wenjuan Zhao, Guodong Liu, X. J. Zhou, Zheng Wei, Xiaozhi Xu, Kaihui Liu, Zonghai Hu, Ke Deng, Shuyun Zhou, Jin-An Shi, Lin Gu, Cheng Shen, Tingting Zhang, Luojun Du, Li Xie, Jianqi Zhu, Wei Chen, Rong Yang, Dongxia Shi, and Guangyu Zhang. Wafer-Scale Growth and Transfer of Highly-Oriented Monolayer MoS_2 Continuous Films. *ACS Nano*, 11(12):12001–12007, 2017.

[61] C. Huyghebaert, T. Schram, Q. Smets, T.Kumar Agarwal, D. Verreck, S. Brems, A. Phommahaxay, D. Chiappe, S. El-Kazi, C.Lockhart de la Rosa, G. Arutchelvan, D. Cott, J. Ludwig, A. Gaur, S. Sutar, A. Leonhardt, D. Lin, M. Caymax, I. Asselberghs, G. Pourtois, and I.P. Radu. 2D materials: roadmap to CMOS integration. In *2018 IEEE International Electron Devices Meeting (IEDM)*, Dec 2018.

[62] Kibum Kang, Kan-Heng Lee, Yimo Han, Hui Gao, Saien Xie, David A. Muller, and Jiwoong Park. Layer-by-layer assembly of two-dimensional materials into wafer-scale heterostructures. *Nature*, 550, Sep 2017.

[63] Han Wang, Lili Yu, Y-H Lee, Wenjing Fang, Allen Hsu, Patrick Herring, Matthew Chin, Madan Dubey, L-J Li, Jing Kong, et al. Large-scale 2D electronics based on

single-layer MoS_2 grown by chemical vapor deposition. In *Electron Devices Meeting (IEDM), 2012 IEEE International*, pages 4–6. IEEE, 2012.

[64] Lili Yu, Yi-Hsien Lee, Xi Ling, Elton JG Santos, Yong Cheol Shin, Yuxuan Lin, Madan Dubey, Efthimios Kaxiras, Jing Kong, Han Wang, et al. Graphene/MoS_2 hybrid technology for large-scale two-dimensional electronics. *Nano letters*, 14(6):3055–3063, 2014.

[65] Yi-Hsien Lee, Lili Yu, Han Wang, Wenjing Fang, Xi Ling, Yumeng Shi, Cheng-Te Lin, Jing-Kai Huang, Mu-Tung Chang, Chia-Seng Chang, et al. Synthesis and transfer of single-layer transition metal disulfides on diverse surfaces. *Nano letters*, 13(4):1852–1857, 2013.

[66] Yang Gao, Zhibo Liu, Dong-Ming Sun, Le Huang, Lai-Peng Ma, Li-Chang Yin, Teng Ma, Zhiyong Zhang, Xiu-Liang Ma, Lian-Mao Peng, et al. Large-area synthesis of high-quality and uniform monolayer WS_2 on reusable Au foils. *Nature communications*, 6:8569, 2015.

[67] Atresh Sanne, Rudresh Ghosh, Amritesh Rai, Maruthi Nagavalli Yogeesh, Seung Heon Shin, Ankit Sharma, Karalee Jarvis, Leo Mathew, Rajesh Rao, Deji Akinwande, et al. Radio frequency transistors and circuits based on CVD MoS_2. *Nano letters*, 15(8):5039–5045, 2015.

[68] Kirby KH Smithe, Christopher D English, Saurabh V Suryavanshi, and Eric Pop. High mobility in monolayer MoS_2 devices grown by chemical vapor deposition. In *Device Research Conference (DRC), 2015 73rd Annual*, pages 239–240. IEEE, 2015.

[69] Yongji Gong, Sidong Lei, Gonglan Ye, Bo Li, Yongmin He, Kunttal Keyshar, Xiang Zhang, Qizhong Wang, Jun Lou, Zheng Liu, et al. Two-step growth of two-dimensional WSe_2/$MoSe_2$ heterostructures. *Nano letters*, 15(9):6135–6141, 2015.

[70] Ming-Yang Li, Yumeng Shi, Chia-Chin Cheng, Li-Syuan Lu, Yung-Chang Lin, Hao-Lin Tang, Meng-Lin Tsai, Chih-Wei Chu, Kung-Hwa Wei, Jr-Hau He, et al. Epitaxial growth of a monolayer WSe_2-MoS_2 lateral pn junction with an atomically sharp interface. *Science*, 349(6247):524–528, 2015.

[71] Yang Gao, Yi-Lun Hong, Li-Chang Yin, Zhangting Wu, Zhiqing Yang, Mao-Lin Chen, Zhibo Liu, Teng Ma, Dong-Ming Sun, Zhenhua Ni, et al. Ultrafast Growth of High-Quality Monolayer WSe_2 on Au. *Advanced Materials*, 2017.

[72] Hao-Ling Tang, Ming-Hui Chiu, Chien-Chih Tseng, Shih-Hsien Yang, Kuan-Jhih Hou, Sung-Yen Wei, Jing-Kai Huang, Yen-Fu Lin, Chen-Hsin Lien, and Lain-Jong Li. Multilayer Graphene–WSe_2 Heterostructures for WSe_2 Transistors. *ACS nano*, 11(12):12817–12823, 2017.

[73] Andre K Geim and Irina V Grigorieva. Van der Waals heterostructures. *Nature*, 499(7459):419–425, 2013.

[74] Yumeng Shi, Wu Zhou, Ang-Yu Lu, Wenjing Fang, Yi-Hsien Lee, Allen Long Hsu, Soo Min Kim, Ki Kang Kim, Hui Ying Yang, Lain-Jong Li, et al. van der Waals epitaxy of MoS_2 layers using graphene as growth templates. *Nano letters*, 12(6):2784–2791, 2012.

[75] Hailong Zhou, Chen Wang, Jonathan C Shaw, Rui Cheng, Yu Chen, Xiaoqing Huang, Yuan Liu, Nathan O Weiss, Zhaoyang Lin, Yu Huang, et al. Large area growth and electrical properties of p-type WSe_2 atomic layers. *Nano letters*, 15(1):709–713, 2014.

[76] S. Wachter, D. K. Polyushkin, O. Bethge, and T. Mueller. A Microprocessor based on a Two-Dimensional Semiconductor. *Nat. Commun.*, 8:14948, 2017.

[77] Kirby K.H. Smithe, Chris D. English, Saurabh V. Suryavanshi, and Eric Pop. Intrinsic electrical transport and performance projections of synthetic monolayer MoS_2 devices. *2D Materials*, 4(1), 2017.

[78] Luca Banszerus, Michael Schmitz, Stephan Engels, Jan Dauber, Martin Oellers, Federica Haupt, Kenji Watanabe, Takashi Taniguchi, Bernd Beschoten, and Christoph Stampfer. Ultrahigh-mobility graphene devices from chemical vapor deposition on reusable copper. *Science Advances*, 1(6), 2015.

[79] Zhongguang Xu, Hao Tian, Alireza Khanaki, Renjing Zheng, Mohammad Suja, and Jianlin Liu. Large-area growth of multi-layer hexagonal boron nitride on polished cobalt foils by plasma-assisted molecular beam epitaxy. *Scientific Reports*, 7:43100 EP –, Feb 2017. Article.

[80] Wei Chen, Jing Zhao, Jing Zhang, Lin Gu, Zhenzhong Yang, Xiaomin Li, Hua Yu, Xuetao Zhu, Rong Yang, Dongxia Shi, Xuechun Lin, Jiandong Guo, Xuedong Bai, and Guangyu Zhang. Oxygen-Assisted Chemical Vapor Deposition Growth of Large Single-Crystal and High-Quality Monolayer MoS_2. *Journal of the American Chemical Society*, 137(50):15632–15635, 2015.

[81] Daniele Chiappe, Jonathan Ludwig, Alessandra Leonhardt, Salim El Kazzi, Ankit Nalin Mehta, Thomas Nuytten, Umberto Celano, Surajit Sutar, Geoffrey Pourtois, Matty Caymax, Kristof Paredis, Wilfried Vandervorst, Dennis Lin, Stefan De Gendt, Kathy Barla, Cedric Huyghebaert, Inge Asselberghs, and Iuliana Radu. Layer-controlled epitaxy of 2D semiconductors: Bridging nanoscale phenomena to wafer-scale uniformity. *Nanotechnology*, 29(42), aug 2018.

[82] Ken Verguts, Koen Schouteden, Cheng-Han Wu, Lisanne Peters, Nandi Vrancken, Xiangyu Wu, Zhe Li, Maksiem Erkens, Clement Porret, Cedric Huyghebaert, Chris Van Haesendonck, Stefan De Gendt, and Steven Brems. Controlling Water

Intercalation Is Key to a Direct Graphene Transfer. *ACS Applied Materials & Interfaces*, 9(42):37484–37492, oct 2017.

[83] Ruoyu Yue, Yifan Nie, Lee A Walsh, Rafik Addou, Chaoping Liang, Ning Lu, Adam T Barton, Hui Zhu, Zifan Che, Diego Barrera, Lanxia Cheng, Pil-Ryung Cha, Yves J Chabal, Julia W P Hsu, Jiyoung Kim, Moon J Kim, Luigi Colombo, Robert M Wallace, Kyeongjae Cho, and Christopher L Hinkle. Nucleation and growth of WSe_2: enabling large grain transition metal dichalcogenides. *2D Materials*, 4(4):045019, 2017.

[84] Wen Wan, Linjie Zhan, Binbin Xu, Feng Zhao, Zhenwei Zhu, Yinghui Zhou, Zhilin Yang, Tienmo Shih, and Weiwei Cai. Temperature-Related Morphological Evolution of MoS_2 Domains on Graphene and Electron Transfer within Heterostructures. *Small*, 13(15):1603549, 2017.

[85] Woo Hyun Chae, Jeffrey D Cain, Eve D Hanson, Akshay A Murthy, and Vinayak P Dravid. Substrate-induced strain and charge doping in CVD-grown monolayer MoS_2. *Applied Physics Letters*, 111(14):143106, 2017.

[86] Xuesong Li, Yanwu Zhu, Weiwei Cai, Mark Borysiak, Boyang Han, David Chen, Richard D. Piner, Luigi Colombo, and Rodney S. Ruoff. Transfer of large-area graphene films for high-performance transparent conductive electrodes. *Nano Letters*, 9(12):4359–4363, 2009.

[87] Alper Gurarslan, Yifei Yu, Liqin Su, Yiling Yu, Francisco Suarez, Shanshan Yao, Yong Zhu, Mehmet Ozturk, Yong Zhang, and Linyou Cao. Surface-energy-assisted perfect transfer of centimeter-scale monolayer and few-layer mos2 films onto arbitrary substrates. *ACS Nano*, 8(11):11522–11528, 2014.

[88] L Banszerus, H Janssen, M Otto, A Epping, T Taniguchi, K Watanabe, B Beschoten, D Neumaier, and C Stampfer. Identifying suitable substrates for high-quality graphene-based heterostructures. *2D Materials*, 4(2):025030, 2017.

[89] Bong Gyu Shin, Gang Hee Han, Seok Joon Yun, Hye Min Oh, Jung Jun Bae, Young Jae Song, Chong Yun Park, and Young Hee Lee. Indirect Bandgap Puddles in Monolayer MoS_2 by Substrate-Induced Local Strain. *Advanced Materials*, 28(42):9378–9384, 2016.

[90] Changhee Lee, Servin Rathi, Muhammad Atif Khan, Dongsuk Lim, Yunseob Kim, Sun Jin Yun, Doo-Hyeb Youn, Kenji Watanabe, Takashi Taniguchi, and Gil-Ho Kim. Comparison of trapped charges and hysteresis behavior in hBN encapsulated single MoS_2 flake based field effect transistors on SiO_2 and hBN substrates. *Nanotechnology*, 29(33):335202, 2018.

[91] Sujay B Desai, Surabhi R Madhvapathy, Angada B Sachid, Juan Pablo Llinas, Qingxiao Wang, Geun Ho Ahn, Gregory Pitner, Moon J Kim, Jeffrey Bokor,

Chenming Hu, et al. MoS_2 transistors with 1-nanometer gate lengths. *Science*, 354(6308):99–102, 2016.

[92] Amirhasan Nourbakhsh, Ahmad Zubair, Redwan N Sajjad, Amir Tavakkoli KG, Wei Chen, Shiang Fang, Xi Ling, Jing Kong, Mildred S Dresselhaus, Efthimios Kaxiras, et al. MoS_2 Field-Effect Transistor with Sub-10 nm Channel Length. *Nano letters*, 16(12):7798–7806, 2016.

[93] Yuan Liu, Jian Guo, Enbo Zhu, Lei Liao, Sung-Joon Lee, Mengning Ding, Imran Shakir, Vincent Gambin, Yu Huang, and Xiangfeng Duan. Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. *Nature*, page 1, 2018.

[94] Branimir Radisavljevic, Michael Brian Whitwick, and Andras Kis. Integrated Circuits and Logic Operations Based on Single-Layer MoS_2. *ACS Nano*, 5(12):9934–9938, 2011.

[95] Lingming Yang, Kausik Majumdar, Yuchen Du, Han Liu, Heng Wu, Michael Hatzistergos, PY Hung, Robert Tieckelmann, Wilman Tsai, Chris Hobbs, et al. High-performance MoS 2 field-effect transistors enabled by chloride doping: Record low contact resistance (0.5 k$\Omega\cdot\ \mu$m) and record high drain current (460 μA/μm). In *VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on*, pages 1–2. IEEE, 2014.

[96] Saptarshi Das, Hong-Yan Chen, Ashish Verma Penumatcha, and Joerg Appenzeller. High performance multilayer MoS_2 transistors with scandium contacts. *Nano letters*, 13(1):100–105, 2012.

[97] K. S. Li, B. W. Wu, L. J. Li, M. Y. Li, C. C. K. Cheng, C. L. Hsu, C. H. Lin, Y. J. Chen, C. C. Chen, C. T. Wu, and M. C. Chen. MoS_2 U-shape MOSFET with 10 nm Channel Length and Poly-Si Source/Drain Serving as Seed for Full Wafer CVD MoS_2 availability. *IEEE Symposium on VLSI Technology*, page 1, 2016.

[98] Adrien Allain, Jiahao Kang, Kaustav Banerjee, and Andras Kis. Electrical contacts to two-dimensional semiconductors. *Nature Materials*, 14(12):1195, 2015.

[99] Cheng Gong, Luigi Colombo, Robert M Wallace, and Kyeongjae Cho. The unusual mechanism of partial Fermi level pinning at metal–MoS_2 interfaces. *Nano letters*, 14(4):1714–1720, 2014.

[100] Hafiz MW Khalil, Muhammad Farooq Khan, Jonghwa Eom, and Hwayong Noh. Highly stable and tunable chemical doping of multilayer WS2 field effect transistor: Reduction in contact resistance. *ACS applied materials & interfaces*, 7(42):23589–23596, 2015.

[101] Du Xiang, Cheng Han, Jing Wu, Shu Zhong, Yiyang Liu, Jiadan Lin, Xue-Ao Zhang, Wen Ping Hu, Barbaros Özyilmaz, AH Castro Neto, et al. Surface transfer

doping induced effective modulation on ambipolar characteristics of few-layer black phosphorus. *Nature communications*, 6:6485, 2015.

[102] Seung-Young Seo, Jaehyun Park, Jewook Park, Kyung Song, Soonyoung Cha, Sangwan Sim, Si-Young Choi, Han Woong Yeom, Hyunyong Choi, and Moon-Ho Jo. Writing monolithic integrated circuits on a two-dimensional semiconductor with a scanning light probe. *Nature Electronics*, (9):512–517.

[103] Angada B Sachid, Mahmut Tosun, Sujay B Desai, Ching-Yi Hsu, Der-Hsien Lien, Surabhi R Madhvapathy, Yu-Ze Chen, Mark Hettick, Jeong Seuk Kang, Yuping Zeng, et al. Monolithic 3D CMOS using layered semiconductors. *Advanced Materials*, 28(13):2547–2554, 2016.

[104] Saptarshi Das, Madan Dubey, and Andreas Roelofs. High gain, low noise, fully complementary logic inverter based on bi-layer WSe_2 field effect transistors. *Applied Physics Letters*, 105(8):083511, 2014.

[105] Saptarshi Das and Joerg Appenzeller. WSe_2 field effect transistors with enhanced ambipolar characteristics. *Applied Physics Letters*, 103(10):103501, 2013.

[106] Jing-Kai Huang, Jiang Pu, Chang-Lung Hsu, Ming-Hui Chiu, Zhen-Yu Juang, Yung-Huang Chang, Wen-Hao Chang, Yoshihiro Iwasa, Taishi Takenobu, and Lain-Jong Li. Large-area synthesis of highly crystalline WSe_2 monolayers and device applications. *ACS nano*, 8(1):923–930, 2013.

[107] Nihar R. Pradhan, Daniel Rhodes, Yan Xin, Shahriar Memaran, Lakshmi Bhaskaran, Muhandis Siddiq, Stephen Hill, Pulickel M. Ajayan, and Luis Balicas. Ambipolar Molybdenum Diselenide Field-Effect Transistors: Field-Effect and Hall Mobilities. *ACS Nano*, 8(8):7923–7929, 2014. PMID: 25007391.

[108] Yen-Fu Lin, Yong Xu, Sheng-Tsung Wang, Song-Lin Li, Mahito Yamamoto, Alex Aparecido-Ferreira, Wenwu Li, Huabin Sun, Shu Nakaharai, Wen-Bin Jian, et al. Ambipolar $MoTe_2$ transistors and their applications in logic circuits. *Advanced Materials*, 26(20):3263–3269, 2014.

[109] Michal J Mleczko, Chaofan Zhang, Hye Ryoung Lee, Hsueh-Hui Kuo, Blanka Magyari-Köpe, Robert G Moore, Zhi-Xun Shen, Ian R Fisher, Yoshio Nishi, and Eric Pop. $HfSe_2$ and $ZrSe_2$: Two-dimensional semiconductors with native high-κ oxides. *Science Advances*, 3(8):e1700481, 2017.

[110] Likai Li, Yijun Yu, Guo Jun Ye, Qingqin Ge, Xuedong Ou, Hua Wu, Donglai Feng, Xian Hui Chen, and Yuanbo Zhang. Black phosphorus field-effect transistors. *Nature nanotechnology*, 9(5):372, 2014.

[111] Fengnian Xia, Han Wang, and Yichen Jia. Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics. *Nature communications*, 5:4458, 2014.

[112] Weinan Zhu, Maruthi N. Yogeesh, Shixuan Yang, Sandra H. Aldave, Joon-Seok Kim, Sushant Sonde, Li Tao, Nanshu Lu, and Deji Akinwande. Flexible Black Phosphorus Ambipolar Transistors, Circuits and AM Demodulator. *Nano Letters*, 15(3):1883–1890, 2015.

[113] Dong Li, Mingyuan Chen, Qijun Zong, and Zengxing Zhang. Floating-Gate Manipulated Graphene-Black Phosphorus Heterojunction for Nonvolatile Ambipolar Schottky Junction Memories, Memory Inverter Circuits, and Logic Rectifiers. *Nano Letters*, 17(10):6353–6359, 2017.

[114] Matthew C Robbins and Steven J Koester. Black Phosphorus p-and n-MOSFETs With Electrostatically Doped Contacts. *IEEE Electron Device Letters*, 38(2):285–288, 2017.

[115] Shu Nakaharai, Mahito Yamamoto, Keiji Ueno, Yen-Fu Lin, Song-Lin Li, and Kazuhito Tsukagoshi. Electrostatically Reversible Polarity of Ambipolar α-$MoTe_2$ Transistors. *ACS nano*, 9(6):5976–5983, 2015.

[116] BL Sharma. *Metal-semiconductor Schottky barrier junctions and their applications*. Springer Science & Business Media, 2013.

[117] Pierre-Emmanuel Gaillardon, Luca Amaru, Jian Zhang, and Giovanni De Micheli. Advanced system on a chip design based on controllable-polarity FETs. In *Proceedings of the conference on Design, Automation & Test in Europe*, page 235. European Design and Automation Association, 2014.

[118] M. De Marchi, J. Zhang, S. Frache, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli. Configurable Logic Gates Using Polarity-Controlled Silicon Nanowire Gate-all-Around FETs. *IEEE Electron Device Lett.*, 35:880, 2014.

[119] Sang-Mo Koo, Qiliang Li, Monica D Edelstein, Curt A Richter, and Eric M Vogel. Enhanced channel modulation in dual-gated silicon nanowire transistors. *Nano letters*, 5(12):2519–2523, 2005.

[120] J Appenzeller, J Knoch, E Tutuc, M Reuter, and S Guha. Dual-gate silicon nanowire transistors with nickel silicide contacts. In *Electron Devices Meeting, 2006. IEDM'06. International*, pages 1–4. IEEE, 2006.

[121] André Heinzig, Stefan Slesazeck, Franz Kreupl, Thomas Mikolajick, and Walter M Weber. Reconfigurable silicon nanowire transistors. *Nano letters*, 12(1):119–124, 2011.

[122] André Heinzig, Thomas Mikolajick, Jens Trommer, Daniel Grimm, and Walter M Weber. Dually active silicon nanowire transistors and circuits with equal electron and hole transport. *Nano letters*, 13(9):4176–4181, 2013.

[123] Michele De Marchi, Davide Sacchetto, Stefano Frache, Juyong Zhang, Pierre-Emmanuel Gaillardon, Yusuf Leblebici, and Giovanni De Micheli. Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs. In *Electron Devices Meeting (IEDM), 2012 IEEE International*, pages 8–4. IEEE, 2012.

[124] Michele De Marchi, Davide Sacchetto, Jian Zhang, Stefano Frache, Pierre-Emmanuel Gaillardon, Yusuf Leblebici, and Giovanni De Micheli. Top–Down Fabrication of Gate-All-Around Vertically Stacked Silicon Nanowire FETs With Controllable Polarity. *Nanotechnology, IEEE Transactions on*, 13(6):1029–1038, 2014.

[125] Yu-Jeng Chang and JL Erskine. Diffusion layers and the Schottky-barrier height in nickel silicide–silicon interfaces. *Physical Review B*, 28(10):5766, 1983.

[126] QT Zhao, U Breuer, E Rije, St Lenk, and S Mantl. Tuning of NiSi/Si Schottky barrier heights by sulfur segregation during Ni silicidation. *Applied physics letters*, 86(6):62108–62108, 2005.

[127] J. Zhang, M. De Marchi, P. Gaillardon, and G. De Micheli. A Schottky-barrier silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 decades of current. In *2014 IEEE International Electron Devices Meeting*, pages 13.4.1–13.4.4, 2014.

[128] Simon M Sze and Kwok K Ng. *Physics of semiconductor devices*. John wiley & sons, 2006.

[129] Z Lu, N Collaert, M Aoulaiche, B De Wachter, A De Keersgieter, JG Fossum, L Altimime, and M Jurczak. Realizing super-steep subthreshold slope with conventional FDSOI CMOS at low-bias voltages. In *Electron Devices Meeting (IEDM), 2010 IEEE International*, pages 16–6. IEEE, 2010.

[130] Jian Zhang, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Dual-threshold-voltage configurable circuits with three-independent-gate silicon nanowire FETs. In *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on*, pages 2111–2114. IEEE, 2013.

[131] Jian Zhang, Michele De Marchi, Davide Sacchetto, Pierre-Emmanuel Gaillardon, Yusuf Leblebici, and Giovanni De Micheli. Polarity-controllable silicon nanowire transistors with dual threshold voltages. *Electron Devices, IEEE Transactions on*, 61(11):3654–3660, 2014.

[132] Jens Trommer, André Heinzig, Uwe Mühle, Markus Löffler, Annett Winzer, Paul M Jordan, Jürgen Beister, Tim Baldauf, Marion Geidel, Barbara Adolphi, et al. Enabling Energy Efficiency and Polarity Control in Germanium Nanowire Transistors by Individually Gated Nanojunctions. *ACS nano*, 11(2):1704–1711, 2017.

[133] Sumio Iijima and Toshinari Ichihashi. Single-shell carbon nanotubes of 1-nm diameter. 1993.

[134] DS Bethune, CH Klang, MS De Vries, G Gorman, R Savoy, J Vazquez, and R Beyers. Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls. 1993.

[135] Ray H Baughman, Anvar A Zakhidov, and Walt A de Heer. Carbon nanotubes–the route toward applications. *science*, 297(5582):787–792, 2002.

[136] Michael FL De Volder, Sameh H Tawfick, Ray H Baughman, and A John Hart. Carbon nanotubes: present and future commercial applications. *Science*, 339(6119):535–539, 2013.

[137] H-S Philip Wong and Deji Akinwande. *Carbon nanotube and graphene device physics*. Cambridge University Press, 2011.

[138] S Heinze, J Tersoff, R Martel, V Derycke, J Appenzeller, and Ph Avouris. Carbon nanotubes as Schottky barrier transistors. *Physical Review Letters*, 89(10):106801, 2002.

[139] R Martel, V Derycke, C Lavoie, J Appenzeller, KK Chan, J Tersoff, and Ph Avouris. Ambipolar electrical transport in semiconducting single-wall carbon nanotubes. *Physical Review Letters*, 87(25):256805, 2001.

[140] Phaedon Avouris, Zhihong Chen, and Vasili Perebeinos. Carbon-based electronics. *Nature nanotechnology*, 2(10):605–615, 2007.

[141] Ji Ung Lee, PP Gipp, and CM Heller. Carbon nanotube p-n junction diodes. *Applied Physics Letters*, 85(1):145–147, 2004.

[142] Yu-Ming Lin, Joerg Appenzeller, Joachim Knoch, and Phaedon Avouris. High-performance carbon nanotube field-effect transistor with tunable polarities. *Nanotechnology, IEEE Transactions on*, 4(5):481–489, 2005.

[143] K S Novoselov, A K Geim, S V Morozov, D Jiang, Y Zhang, S V Dubonos, I V Grigorieva, and A A Firsov. Electric Field Effect in Atomically Thin Carbon Films. *Science*, 306(5696):666–669, 2004.

[144] Sansiri Tanachutiwat, Ji Ung Lee, Wei Wang, and Chun Yung Sung. Reconfigurable multi-function logic based on graphene pn junctions. In *Design Automation Conference (DAC), 2010 47th ACM/IEEE*, pages 883–888. IEEE, 2010.

[145] Young-Woo Son, Marvin L Cohen, and Steven G Louie. Energy gaps in graphene nanoribbons. *Physical review letters*, 97(21):216803, 2006.

[146] Melinda Y Han, Barbaros Özyilmaz, Yuanbo Zhang, and Philip Kim. Energy band-gap engineering of graphene nanoribbons. *Physical review letters*, 98(20):206805, 2007.

[147] Hongtao Liu, Yunqi Liu, and Daoben Zhu. Chemical doping of graphene. *Journal of materials chemistry*, 21(10):3335–3345, 2011.

[148] Shu Nakaharai, Toru Iijima, Shinichi Ogawa, Satoshi Suzuki, Kazuhito Tsukagoshi, Seiki Sato, and Naoki Yokoyama. Electrostatically-reversible polarity of dual-gated graphene transistors with He ion irradiated channel: Toward reconfigurable CMOS applications. In *Electron Devices Meeting (IEDM), 2012 IEEE International*, pages 4–2. IEEE, 2012.

[149] Shu Nakaharai, Toru Iijima, Shinichi Ogawa, Song-Lin Li, Kazuhito Tsukagoshi, Seiki Sato, and Naoki Yokoyama. Electrostatically Reversible Polarity of Dual-Gated Graphene Transistors. *Nanotechnology, IEEE Transactions on*, 13(6):1039–1043, 2014.

[150] Shu Nakaharai, Tomohiko Iijima, Shinichi Ogawa, Shingo Suzuki, Song-Lin Li, Kazuhito Tsukagoshi, Shintaro Sato, and Naoki Yokoyama. Conduction tuning of graphene based on defect-induced localization. *ACS nano*, 7(7):5694–5700, 2013.

[151] Pierre-Emmanuel Gaillardon, Luca Gaetano Amarù, Shashikanth Bobba, Michele De Marchi, Davide Sacchetto, and Giovanni De Micheli. Nanowire systems: technology and design. *Philosophical Transactions of the Royal Society of London A: Mathematical, Physical and Engineering Sciences*, 372(2012):20130102, 2014.

[152] Jian Zhang, Xifan Tang, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Configurable circuits featuring dual-threshold-voltage design with three-independent-gate silicon nanowire FETs. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 61(10):2851–2861, 2014.

[153] Michele De Marchi, Jian Zhang, Stefano Frache, Davide Sacchetto, Pierre-Emmanuel Gaillardon, Yusuf Leblebici, and Giovanni De Micheli. Configurable logic gates using polarity-controlled silicon nanowire gate-all-around FETs. *Electron Device Letters, IEEE*, 35(8):880–882, 2014.

[154] Shashikanth Bobba, Pierre-Emmanuel Gaillardon, Jian Zhang, Michele De Marchi, Davide Sacchetto, Yusuf Leblebici, and Giovanni De Micheli. Process/design co-optimization of regular logic tiles for double-gate silicon nanowire transistors. In *2012 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pages 55–60. IEEE, 2012.

[155] Odysseas Zografos, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Novel grid-based power routing scheme for regular controllable-polarity FET arrangements. In *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1416–1419. IEEE, 2014.

[156] Luca Amarù, Pierre-Emmanuel Gaillardon, Subhasish Mitra, and Giovanni De Micheli. New Logic Synthesis as Nanotechnology Enabler. *Proceedings of the IEEE*, 103(11):2168–2195, 2015.

[157] Luca Amarù, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Biconditional BDD: a novel canonical BDD for logic synthesis targeting XOR-rich circuits. In *Proceedings of the Conference on Design, Automation and Test in Europe*, pages 1014–1017. EDA Consortium, 2013.

[158] Luca Amarù, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. An efficient manipulation package for biconditional binary decision diagrams. In *Proceedings of the conference on Design, Automation & Test in Europe*, page 296. European Design and Automation Association, 2014.

[159] Luca Amarù, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. BDS-MAJ: A BDD-based logic synthesis tool exploiting majority logic decomposition. In *Proceedings of the 50th Annual Design Automation Conference*, page 47. ACM, 2013.

[160] Luca Amarù, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. Majority-inverter graph: A novel data-structure and algorithms for efficient logic optimization. In *Proceedings of the 51st Annual Design Automation Conference*, pages 1–6. ACM, 2014.

[161] Jorge Romero-Gonzàlez and Pierre-Emmanuel Gaillardon. BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field-Effect Transistors. *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, 4:35–43, 2018.

[162] Xifan Tang, Jian Zhang, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. TSPC flip-flop circuit design with three-independent-gate silicon nanowire FETs. In *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*, pages 1660–1663. IEEE, 2014.

[163] Luca Amarú, Pierre-Emmanuel Gaillardon, Jian Zhang, and Giovanni De Micheli. Power-gated differential logic style based on double-gate controllable-polarity transistors. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(10):672–676, 2013.

[164] Edouard Giacomin, Jorge Romero Gonzalez, and Pierre-Emmanuel Gaillardon. Low-power multiplexer designs using three-independent-gate field effect transistors. In *2017 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pages 33–38. IEEE, 2017.

[165] Yu Bi, Kaveh Shamsi, Jiann-Shiun Yuan, Pierre-Emmanuel Gaillardon, Giovanni De Micheli, Xunzhao Yin, X Sharon Hu, Michael Niemier, and Yier Jin. Emerging technology-based design of primitives for hardware security. *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 13(1):3, 2016.

[166] Kaveh Shamsi, Yu Bi, Yier Jin, Pierre-Emmanuel Gaillardon, Michael Niemier, and X Sharon Hu. Reliable and high performance STT-MRAM architectures based on controllable-polarity devices. In *Computer Design (ICCD), 2015 33rd IEEE International Conference on*, pages 343–350. IEEE, 2015.

[167] Alexandre Levisse, Pierre-Emmanuel Gaillardon, Bastien Giraud, Ian O'Connor, Jean-Philippe Noel, Mathieu Moreau, and Jean-Michel Portal. Resistive Switching Memory Architecture Based on Polarity Controllable Selectors. *IEEE Transactions on Nanotechnology*, 2018.

[168] MM Benameur, B Radisavljevic, JS Heron, S Sahoo, H Berger, and A Kis. Visibility of dichalcogenide nanolayers. *Nanotechnology*, 22(12):125706, 2011.

[169] Gerd Binnig, Calvin F Quate, and Ch Gerber. Atomic force microscope. *Physical review letters*, 56(9):930, 1986.

[170] Wei Liu, Jiahao Kang, Deblina Sarkar, Yasin Khatami, Debdeep Jena, and Kaustav Banerjee. Role of metal contacts in designing high-performance monolayer n-type WSe_2 field effect transistors. *Nano letters*, 13(5):1983–1990, 2013.

[171] Michael S Fuhrer and James Hone. Measurement of mobility in dual-gated MoS_2 transistors. *Nature nanotechnology*, 8(3):146, 2013.

[172] Seok Daniel Namgung, Suk Yang, Kyung Park, Ah-Jin Cho, Hojoong Kim, and Jang-Yeon Kwon. Influence of post-annealing on the off current of MoS_2 field-effect transistors. *Nanoscale research letters*, 10(1):62, 2015.

[173] Sunkook Kim, Aniruddha Konar, Wan-Sik Hwang, Jong Hak Lee, Jiyoul Lee, Jaehyun Yang, Changhoon Jung, Hyoungsub Kim, Ji-Beom Yoo, Jae-Young Choi, et al. High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals. *Nature communications*, 3:ncomms2018, 2012.

[174] Britton WH Baugher, Hugh OH Churchill, Yafang Yang, and Pablo Jarillo-Herrero. Intrinsic electronic transport properties of high-quality monolayer and bilayer MoS_2. *Nano letters*, 13(9):4212–4216, 2013.

[175] Hema CP Movva, Amritesh Rai, Sangwoo Kang, Kyounghwan Kim, Babak Fallahazad, Takashi Taniguchi, Kenji Watanabe, Emanuel Tutuc, and Sanjay K Banerjee. High-mobility holes in dual-gated WSe_2 field-effect transistors. *ACS nano*, 9(10):10402–10410, 2015.

[176] NR Pradhan, D Rhodes, S Memaran, JM Poumirol, D Smirnov, S Talapatra, S Feng, N Perea-Lopez, AL Elias, M Terrones, et al. Hall and field-effect mobilities in few layered p-WSe_2 field-effect transistors. *Scientific reports*, 5:8979, 2015.

[177] Winston Haaswijk, Mathias Soeken, Luca Amarù, Pierre-Emmanuel Gaillardon, and Giovanni De Micheli. A novel basis for logic rewriting. In *Design Automation*

Conference (ASP-DAC), 2017 22nd Asia and South Pacific, pages 151–156. IEEE, 2017.

[178] Michael Raitza, Akash Kumar, Marcus Völp, Dennis Walter, Jens Trommer, Thomas Mikolajick, and Walter M Weber. Exploiting transistor-level reconfiguration to optimize combinational circuits. In *Proceedings of the Conference on Design, Automation & Test in Europe*, pages 338–343. European Design and Automation Association, 2017.

[179] A. Prakash, H. Ilatikhameneh, P. Wu, and J. Appenzeller. Understanding contact gating in schottky barrier transistors from 2d channels.

[180] A. Gaur, Y. Balaji, D. Lin, C. Adelmann, J. Van Houdt, M. Heyns, D. Mocuta, and I. P. Radu. Demonstration of 2e12 cm$^{\breve{}2}$eV$^{\breve{}1}$ 2D-Oxide Interface Trap Density on Back-Gated MoS_2 Flake Devices with 2.5nm EOT. *Microelectron. Eng.*, 178:145, 2017.

[181] Gianluca Fiori and Giuseppe Iannaccone. NanoTCAD ViDES. 2008.

[182] G. Fiori and G. Iannaccone. Multiscale Modeling for Graphene-Based Nanoscale Transistors. *Proceedings of the IEEE*, 101(7):1653–1669, 2013.

[183] W. Cao, J. Kang, W. Liu, Y. Khatami, D. Sarkar, and K. Banerjee. 2D electronics: Graphene and beyond. In *2013 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, pages 37–44, 2013.

[184] Weijie Zhao, Ricardo Mendes Ribeiro, Minglin Toh, Alexandra Carvalho, Christian Kloc, AH Castro Neto, and Goki Eda. Origin of indirect optical transitions in few-layer MoS_2, WS_2, and WSe_2. *Nano letters*, 13(11):5627–5634, 2013.

[185] Cheng Gong, Hengji Zhang, Weihua Wang, Luigi Colombo, Robert M Wallace, and Kyeongjae Cho. Band alignment of two-dimensional transition metal dichalcogenides: Application in tunnel field effect transistors. *Applied Physics Letters*, 103(5):053513, 2013.

[186] Filip A Rasmussen and Kristian S Thygesen. Computational 2D materials database: electronic structure of transition-metal dichalcogenides and oxides. *The Journal of Physical Chemistry C*, 119(23):13169–13183, 2015.

[187] Wenxu Zhang, Zhishuo Huang, Wanli Zhang, and Yanrong Li. Two-dimensional semiconductors with possible high room temperature mobility. *Nano Research*, 7(12):1731–1737, 2014.

[188] Tarun Agarwal, Iuliana Radu, Praveen Raghavan, Gianluca Fiori, Aaron Thean, Marc Heyns, and Wim Dehaene. Effect of material parameters on two-dimensional materials based TFETs: An energy-delay perspective. In *Solid-State Device Research Conference (ESSDERC), 2016 46th European*, pages 47–50. IEEE, 2016.

[189] Seung Hyun Park, Yang Liu, Neerav Kharche, Mehdi Salmani Jelodar, Gerhard Klimeck, Mark S Lundstrom, and Mathieu Luisier. Performance comparisons of III–V and strained-Si in planar FETs and nonplanar FinFETs at ultrashort gate length (12 nm). *IEEE Transactions on Electron Devices*, 59(8):2107–2114, 2012.

[190] Gianluca Fiori and Giuseppe Iannaccone. Performance analysis of graphene bilayer transistors through tight-binding simulations. In *Computational Electronics, 2009. IWCE'09. 13th International Workshop on*, pages 1–4. IEEE, 2009.

[191] Liang Li, Xiaosheng Fang, Tianyou Zhai, Meiyong Liao, Ujjal K Gautam, Xingcai Wu, Yasuo Koide, Yoshio Bando, and Dmitri Golberg. Electrical Transport and High-Performance Photoconductivity in Individual ZrS_2 Nanobelts. *Advanced Materials*, 22(37):4151–4156, 2010.

[192] Xiaoting Wang, Le Huang, Xiang-Wei Jiang, Yan Li, Zhongming Wei, and Jingbo Li. Large scale ZrS 2 atomically thin layers. *Journal of Materials Chemistry C*, 4(15):3143–3148, 2016.

[193] Moonshik Kang, Servin Rathi, Inyeal Lee, Dongsuk Lim, Jianwei Wang, Lijun Li, Muhammad Atif Khan, and Gil-Ho Kim. Electrical characterization of multilayer $HfSe_2$ field-effect transistors on SiO_2 substrate. *Applied Physics Letters*, 106(14):143108, 2015.

[194] Kai Xu, Zhenxing Wang, Feng Wang, Yun Huang, Fengmei Wang, Lei Yin, Chao Jiang, and Jun He. Ultrasensitive Phototransistors Based on Few-Layered HfS_2. *Advanced Materials*, 27(47):7881–7887, 2015.

[195] Toru Kanazawa, Tomohiro Amemiya, Atsushi Ishikawa, Vikrant Upadhyaya, Kenji Tsuruta, Takuo Tanaka, and Yasuyuki Miyamoto. Few-layer HfS_2 transistors. *Scientific reports*, 6:22277, 2016.

[196] Akash Laturia and William G Vandenberghe. Dielectric properties of mono-and bilayers determined from first principles. In *Simulation of Semiconductor Processes and Devices (SISPAD), 2017 International Conference on*, pages 337–340. IEEE, 2017.

[197] MH Na, EJ Nowak, W Haensch, and J Cai. The effective drive current in CMOS inverters. In *Digest. International Electron Devices Meeting,*, pages 121–124. IEEE, 2002.

[198] Á. Szabó, R. Rhyner, and M. Luisier. Ab Initio Simulation of Single-and Few-Layer MoS_2 Transistors: Effect of Electron-Phonon Scattering. *Phys. Rev. B: Condens. Matter Mater. Phys.*, 92:035435, 2015.

[199] Amithraj Valsaraj, Jiwon Chang, Amritesh Rai, Leonard F Register, and Sanjay K Banerjee. Theoretical and experimental investigation of vacancy-based doping of monolayer MoS2 on oxide. *2D Materials*, 2(4):045009, 2015.

[200] Javier Martín-Sánchez, Antonio Mariscal, Marta De Luca, Aitana Tarazaga Martín-Luengo, Georg Gramse, Alma Halilovic, Rosalía Serna, Alberta Bonanni, Ilaria Zardo, Rinaldo Trotta, et al. Effects of dielectric stoichiometry on the photoluminescence properties of encapsulated WSe 2 monolayers. *Nano Research*, 11(3):1399–1414, 2018.

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SOFT SKILLS

- **Critical Thinking**
- **Positive Attitude**
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- **Teamwork**
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LANGUAGES

- **Italian (native)**
- **English (C2)**
- **French (B1+)**

INTERESTS

- **Sports:** Tennis, Skiing, Climbing
- **Cooking**
- **Travel**
- **Photography**

EDUCATION

2014 – 2019 **PhD in Microtechnology and Nanoelectronics Engineering** from École polytechnique fédérale de Lausanne (EPFL), Lausanne, Switzerland.

2011 – 2013 **Master of Science in Nanotechnologies for ICTs** joint master degree among Polytechnic of Turin, INP Grenoble Phelma and EPFL. Degree cum laude

2008 – 2011 **Bachelor in Electronic Engineering** from University of Pisa, Italy. Final GPA: 109/110.

RESEARCH EXPERIENCE

2014 – 2019 Integrated system laboratory (LSI), **EPFL and IMEC Research Center**, working on 2D materials for reconfigurable polarity-controllable devices.

2013 – 2014 **NASA and Caltech Jet Propulsion Laboratory**, worked on superconducting nanowire single photon detectors for deep space optical communication as a master thesis project.
Awarded JPL graduate fellowship to extend the duration of the internship position.

Jun – Sept 2012 **Max Planck Institute for Quantum Optics**, intern in the Attoelectronics group. Worked on attosecond control and measurements on the nanoscale.

SELECTED FIRST AUTHOR PUBLICATIONS

- Book Chapter: Functionality-Enhanced Devices: from Transistors to Circuit Level Opportunities. In *Beyond-CMOS Technologies for Next Generation Computer Design*, pp. 21-42. **Springer, Cham, (2019).**
- Doping-Free Complementary Logic Gates Enabled by 2D Polarity-Controllable Transistors. ***ACS Nano* 12(7), (2018).**
- Scaling Trends and Performance Evaluation of 2D Polarity-Controllable FETs. ***Sci. Rep.* 7, (2017).**
- Polarity Control in WSe2 Double-Gate Transistors. ***Sci. Rep.* 6, (2016).**

TECHNICAL SKILLS

- Broad theoretical background spanning from electronics, optics and optoelectronics to micro-nano devices, material science and physics.
- Strong knowledge in CMOS and beyond-CMOS electronics, with particular emphasis on 2D materials.
- Good experience in cleanroom and laboratory work, cryogenic systems and low noise measurements at room and cryogenic temperatures.
- Proficient in the use of Labview, Matlab, Origin and Comsol multiphysics.
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