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Interfacing Qubits via Cryo-CMOS Front Ends

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***Abstract* — This work describes a basic interface between solid-state quantum bits (qubits) and classical environments. We describe a multiplexer, a circulator, and a low noise amplifier, designed for cryogenic temperature operation in a 40 nm CMOS technology node. The circuits take advantage of traditional design styles, such as transmission gates, passive LC filters and switches, and recent developments, such as differential noise cancelling with six-port transformers, while exploiting new cryogenic CMOS (cryo-CMOS) modeling for design and verification purposes.**

Keywords* — *Cryo-CMOS, quantum bit, qubit, quantum computer, qubit readout, multiplexer, circulator, noise cancelling low noise amplifier.

I. Introduction

Physical implementations of scalable and reliable quantum processors have achieved significant progress in the last decade [1]. CMOS technology has been proposed to implement quantum bit (qubit) controller circuits at cryogenic temperatures (4 K), so as to reduce the complex interconnections between the deep-cryogenic quantum processor (20 mK) and room temperature microarchitectures [2]. A cryo-CMOS qubit controller consists of a write-in block to change the state of a qubit and a read-out block to sense the state. Both blocks make use of radio-frequency components and have similarities to a RF receiver. Qubit read-out front-end circuits are generally operating at 0.5-1.5 GHz (for spin qubits) and at 5-7 GHz (for transmon qubits). The drawback of a lossy substrate in bulk CMOS can be mitigated at cryogenic temperature due to increased resistivity of the frozen-out substrate, which is beneficial to design RF controller circuits. Analog circuits, such as ADC, DAC or PLL can also be integrated on the same system-on-chip (SoC) to implement a quantum processor controller. In this work, we describe three blocks, i.e. a multiplexer (MUX), a circulator, and a low noise amplifier (LNA), used in the readout of circuits that directly interface with the physical qubit as shown in Fig. 1 [2],[3]. Due to the sensitivity limitation of the qubit sensor and the weakness of the qubit signal (~ -135 dBm), a strict low noise operation is required.

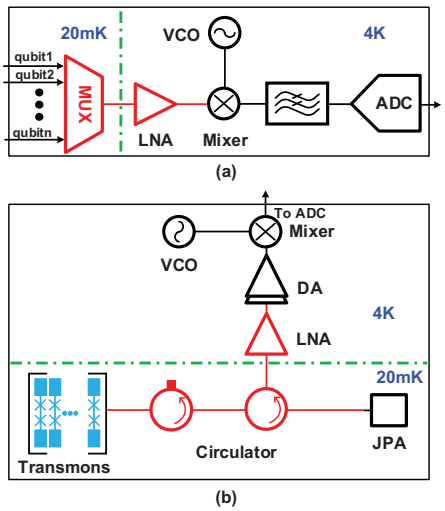

Fig. 1. Qubit readout front-end circuits for (a) spin qubit and (b) transmon qubit.

II. Cryo-CMOS circuits for qubit readout

A. Multiplexer

Multi-qubit readout and control platforms advocate the use of frequency- and time-domain multiplexing. In time-domain multiplexing, the same hardware can be shared by multiple qubits by means of switches, for example in a RF reflectometry readout for spin qubits. Cryo-CMOS 4-to-1 analog multiplexers have been designed, fabricated in 40 nm bulk technology, and measured to verify operation at 300 K and 4 K. A transmission gate based architecture and tree structure, as shown in Fig. 2, has been chosen to minimize area, power, and delay. The tested chips show an insertion loss (and noise figure) of 0.5 dB, with an isolation of 30 dB using a 50 Ω reference impedance when operating at 4.2 K. The measured bandwidth is ~100 MHz, limited by the large capacitance of the test setup. The designed multiplexers show reduced insertion loss, improved isolation and larger bandwidth at cryogenic temperature, thus confirming the suitability of the approach.

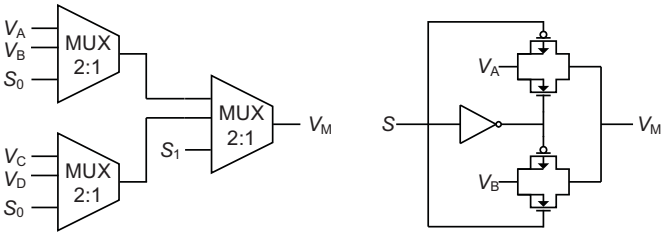

Fig. 2. Cryo-CMOS multiplexer structure.

B. Circulator

Circulators are used to route signals, while isolating the qubits from noisy environments, mostly in superconducting qubit readout systems, but also in some spin qubit experiments. Commonly, this is done by ferrite devices, which are bulky and sensitive to magnetic fields. Thus, an integrated cryo-CMOS passive circulator has been designed as a compact and non magnetic alternative. The circuit operates at 5-7 GHz and uses passive LC filters and switches, as shown in Fig. 3, to realize non-reciprocity via constructive and destructive interference [4]. In 40 nm technology, at 300 K the insertion loss is ~3 dB and the isolation 18 dB over the bandwidth, while they are expected to reduce to less than 2 dB insertion loss and 20 dB isolation at 4.2 K, thanks to the reduced ON resistance of switches and improved Q factor of passives. The power consumption is

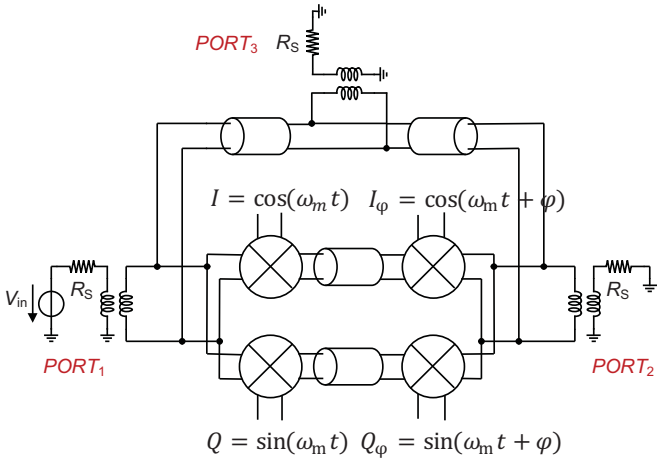

Fig. 3. Cryo-CMOS circulator block diagram [4].

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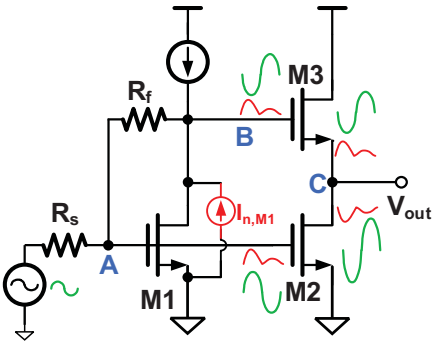

Fig. 4. Simplified schematic of NC LNA for spin qubit RF reflectometry [2].

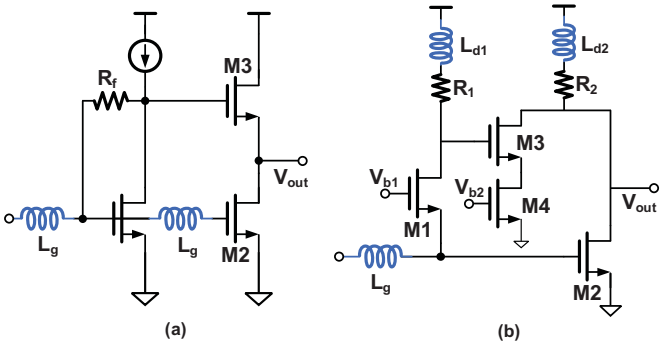

Fig. 5. NC LNAs use inductors for high frequency application in (a) common-source NC and (b) common-gate NC.

below 5 mW in all operating conditions, making it suitable for operation in a dilution fridge.

C. Low Noise Amplifier

To read out the qubit state with high fidelity, the noise figure (NF) of the LNA should be < 0.1 dB at 4 K. With the aid of frequency multiplexing, a single wideband LNA (0.5-1.5 GHz) can be utilized to sense and amplify multichannel spin qubit signals, so as to lower power dissipation and reduce system complexity [5]. For transmon qubits, a LNA with bandwidth of 5-7 GHz is also required. The common source noise cancellation (NC) topology has been used to fulfill a wideband CMOS cryogenic LNA for spin-qubit RF-reflectometry and is shown in Fig. 4 [2]. This structure cannot be easily ported to design LNAs operating at 6 GHz for superconducting qubit readout due to the large input parasitic capacitance. Assuming dimensions of M1 and M2 are 30 µm/60 nm and 160 µm/60 nm respectively, the total parasitic capacitance of node A is about 0.2 pF, which degrades input return loss S_{11} to about 9.5 dB as frequency increases from 1 GHz to 6 GHz. In addition, the phase difference of two combined noise signals at node C will deviate from 180° to ~160° with frequency rising to 6 GHz, then noise cancellation will be incomplete. Similar performance degradation will also occur to a common gate NC LNA working at higher frequency [6]. NC techniques are extended for high frequency applications by using inductors to counteract the capacitive effects, as shows Fig. 5 [7]. Nevertheless, a 0.8 nH two-turn spiral inductor realized by 3.4 µm Cu metal in bulk CMOS still induces ~0.4 dB insertion loss at cryogenic temperature, which will compromise the NF. Another drawback of traditional NC structures is that only channel noise of M1 ($4k_BT\gamma g_m\Delta f$) can be cancelled out, then large transconductance of M2 (g_{m2}) should be used to partially suppress noise of the auxiliary path at the cost of high power consumption, which also should be avoided to relax cooling requirements.

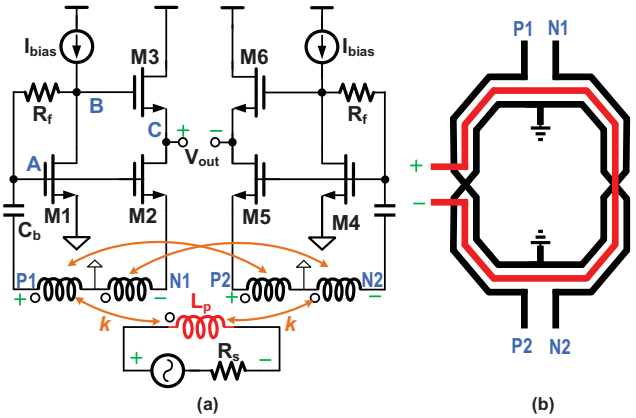

Fig. 6. Differential mutual NC LNA: (a) circuit structure, (b) transformer footprint.

Considering the challenging requirements on NF (< 0.1 dB), bandwidth (>33%) and power dissipation (<150 µW/qubit) for transmons qubit readout, a fully differential LNA as shown in Fig. 6(a) is proposed. First, the half circuit is a combination of common source and common gate NC circuits, and this mutual noise cancellation between two paths suppresses channel thermal noise of M1 and M2 [8]. By careful design of biases and dimensions of M1-6, noise of M1/M4 can be entirely cancelled out and noise contributed by M2/M5 will be reduced by 75%. Second, the input transformer is used for wideband impedance matching at the center frequency (6 GHz). The transformer is easily compressed to a single footprint to save area and to reduce the insertion loss. One possible layout is shown in Fig. 6(b): unlike the single-ended configuration (noise mutual coupling for NC is via the two turns of a symmetrical inductor), the noise coupling is through the arms of the two secondary coils in the transformer, which makes the transformer design more flexible. In addition, the differential topology is appropriate to integrate with differential circuits such as circulators in the qubit readout system.

III. Conclusions

Cryogenic CMOS (cryo-CMOS) circuits for qubit readout are described in the paper. The 4-to-1 MUX utilizes transmission gate based architecture and exhibits the expected functionality with improved performance at 4.2 K. The passive circulator is based on LC filters and switches, and is expected to achieve < 2 dB IL and 20 dB isolation. The NC LNA topologies are reviewed and briefly analyzed. The inductorless NC LNA can hardly be used for 6 GHz applications, so a differential mutual NC circuit is proposed for qubit readout. All the circuit blocks are designed in standard bulk CMOS process, which offers the possibility to achieve a fully integrated readout system.

References

[1] N. M. Linke et al., "Experimental comparison of two quantum computing architectures," Proceedings of the National Academy of Sciences, p. 201618020, 2017.

[2] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," IEEE Journal of Solid-State Circuits, vol. 53, no. 1, pp. 309–321, Jan. 2018.

[3] D. Riste, et al., "Deterministic entanglement of superconducting qubits by parity measurement and feedback," Nature, vol. 502, no. 7471, pp. 350–354, 2013.

[4] T. Dinc, A. Nagulu and H. Krishnaswamy, "A Millimeter-Wave Non-Magnetic Passive SOI CMOS Circulator Based on Spatio-Temporal Conductivity Modulation," IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3276-3292, Dec. 2017.

[5] J. Hornibrook et al., “Frequency multiplexing for readout of spin qubits,” Appl. Phys. Lett., vol. 104, no. 10, p. 103108, 2014.

[6] W.-H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, “A highly linear broadband CMOS LNA employing noise and distortion cancellation,” IEEE Journal of Solid-State Circuits, vol. 43, no. 5, pp. 1164–1176, May 2008.

[7] C.-F. Liao and S. I. Liu, “A broadband noise-canceling MOS LNA for 3.1–10.6-GHz UWB receiver,” IEEE Journal of Solid-State Circuits, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[8] M. Rahman and R. Harjani, “A 2.4 GHz, Sub-1 V, 2.8 dB NF, 475 μW Dual-Path Noise and Nonlinearity Cancelling LNA for Ultra-Low-Power Radios,” IEEE Journal of Solid-State Circuits., vol. 53, no. 5, pp. 1423–1430, May 2018.