17.8 A 2.6 μ W Monolithic CMOS Photoplethysmographic Sensor Operating with 2 μ W LED Power

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Photoplethysmography (PPG) is a key technology allowing non-invasive monitoring of vital indicators such as heart rate (HR) and oxygen saturation (SpO_2). Today, the total PPG sensor power consumption is dominated by the few tens of mA of the LEDs driving current. Different solutions have been proposed to solve this bottle-neck, either by reducing the LED duty cycle [1-2] or by non-uniform sub-sampling [3]. A heart-beat-locked loop system that significantly reduces the LED power has been recently demonstrated [4]. However, this power reduction comes at the cost of more complexity since it requires a non-trivial heart beat prediction scheme and intrinsically hinders the full PPG wave representation.

In this work, we address the power issue by combining a high sensitivity photo-detector with an ultra-low noise and low power readout chain achieving the same signal-to-noise ratio (SNR) compared to conventional solutions, but at significantly lower LED power. We present a PPG sensor integrating an array of pinned-photodiodes (PPD), commonly used in CMOS imagers for achieving sub-electron noise [5]. The PPDs array is implemented on the same chip with the full analog front-end (AFE) including the analog-to-digital conversion (ADC). The full CMOS integration allows one to dramatically reduce the parasitic capacitance leading to a larger conversion gain and a lower noise. This approach also provides higher miniaturization and lower cost compared to traditional solutions with off-chip photodiodes. The use of an array additionally enables spatial averaging leading to further noise reduction. Consequently, the LED power can be reduced dramatically. A prototype has been implemented in a 0.18 μ m CMOS Image Sensor (CIS) process, achieving 4.6 μ W total power consumption, including 1.97 μ W LED power, at 1.38bpm HR average error.

The block diagram of the PPG sensor is shown in Fig. 17.8.1. It consists of a fully integrated chip embedding an array of PPDs, a passive averaging block, a switched-cap (SC) amplifier and an ADC. The photosensitive area consists of four clusters of 50 rows and 256 columns. The 50 pixels along the i-column are assembled in a macro-pixel (MP). The pixels of one MP share the same source-follower (SF) saving power while maintaining a reasonably low parasitic capacitance at the shared sense node (SN). The spatial averaging is done in two steps: first, a charge averaging on the shared SN within the same column and, second, a voltage averaging among the 1024 columns at the SFs output. This leads to a considerable shot and read noise reduction, together with a full pre-filtering of the PPG signal itself. Next, the PPG signal is amplified by a low noise programmable gain SC amplifier. In addition to the noise optimization, the chosen pixel achieves between 66% and 75% quantum efficiency (QE) for the selected LED wavelengths (Fig. 17.8.4) further reducing the LED power needed for achieving the target SNR [1].

Figure 17.8.2 shows the circuit implementation together with the timing diagram. The sense nodes, shared by 50 PPDs and corresponding to the SFs inputs, are first reset. In parallel, each individual PPD starts integrating the impinging light corresponding to the ambient light (AL). In order to precisely control the light-induced charge integration, the PPDs are first emptied by the sink switch TGs. At the end of the first integration phase, the generated photoelectrons are transferred, via the transfer gate TGT, to the SNs. The capacitance of each SN, shared by the 50 pixels along the same column, converts the integrated photoelectrons into a voltage and performs the charge averaging across the 50 rows. After the transfer is completed the SF output voltages are sampled on capacitors C1_i, via S1_i. Next, the SNs are reset again and the LED is pulsed on. As above, the PPDs precisely integrate the LED light superimposed to AL, and the related voltage level is sampled on C2_i, via S2_i. The power switch S_{SF} is only closed during this charge transfer and sampling phase for minimal power consumption. By closing S3_i and S4_i, all the capacitors C1_i and C2_i related to the same sample are connected in parallel and share their charge, resulting into a voltage equal to the passive spatial average of the array pixel output samples. In addition, the large capacitor resulting from the parallel connection of multiple column-level capacitors acts as a large hold capacitor for the following stage. The full averaging operation comes with a shot noise variance reduction of 50 $\times$ 1024 and a read noise variance reduction of

1024. In order to extract the difference of the two averaged samples, corresponding to the AL and the AL plus LED light, a SC amplifier is operated as shown in Fig. 17.8.2: first, the averaged AL sample is stored in C3, via S5 and SAZ. Then, SAZ is opened and the charge stored in C3 is transferred to C4. At the closing of S6, the amplified difference between the two average values is obtained at the amplifier's output, leading to an efficient AL cancellation. The amplifier embeds a programmable gain, from 1 to 32 to adapt to different operating conditions. It then drives a 14b incremental ADC, through SF2. The power switches S_{Amp} and S_{ADC} are only closed at the beginning of the array averaging and opened after the digitization.

A die micrograph of the 180nm chip is shown in Fig. 17.8.7. The linearity of the light to digital conversion and the total noise measurements are shown in Fig. 17.8.3. The sensor is exposed to an LED shining at increasing driving current and the resulting output digital number is acquired. The programmable amplifier gain has been set to 8, which enables a wide range of emitting light conditions without saturation. With the exception of sub-mA LED operations, the chip shows $\pm 3\%$ non-linearity in the light to digital conversion. Note that this includes all the sources of non-linearity from the LED, the readout chain to the ADC. Figure 17.8.3 also shows that the output noise standard-deviation (STD) remains constant across the dynamic range, demonstrating the effectiveness of the shot noise reduction by spatial averaging. The total noise measured at the output of an off-chip 11 taps FIR low-pass filter is 3.1 DN_{RMS} in average corresponding to an input-referred noise as low as 0.68 e_{RMS} per PPD, thanks to the noise shaping introduced by the incremental ADC. Indeed, the noise measured directly at the output of the ADC corresponds to 9.43 DN_{RMS}. This accounts for all the noise components including the readout noise, quantization noise, shot noise and LED flicker noise.

An in-vivo acquisition of PPG has been performed in reflection mode on the index finger. Figure 17.8.4 shows the LEDs and sensor module used for the experiment, as well as samples of the PPG signal obtained using different LED wavelengths at a record-low LED average power of 1.97 μ W. Figure 17.8.5 shows a comparison between the HR directly extracted from the sensor output and a commercial ECG chest strap featuring a HR average error of 1.38bpm only measured on three healthy male subjects. These measurements have been obtained with a sampling frequency of 40Hz, an average LED driving power of 1.97 μ W, at a duty cycle of 0.07%, and a readout (AFE+ADC) average power consumption of 2.63 μ W only. This is obtained, referring to Figure 17.8.2, by closing S_{SF} for 80 μ s and S_{Amp} with S_{ADC} for 0.5ms.

Compared to recent state-of-the-art (SOA), shown in Fig. 17.8.6, this work achieves the lowest power consumption. Moreover, among the most relevant SOA works, this is the only solution featuring a full integration of the photosensitive area together with the AFE and the ADC. This last feature, in addition to the extremely low power consumption, makes this solution a serious candidate for the future of wearable digital healthcare.

References:

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Figure 17.8.1: Block diagram of the monolithic PPG sensor embedding an array of macro-pixels, as photosensitive area, an averaging block, an amplifier and an ADC.

Figure 17.8.2: Architecture of the monolithic PPG sensor and detailed schematic of the OTA used in the amplifier, the averaging block, with the timing diagram.

Figure 17.8.3: Measured light-to-digital linearity and total noise standard-deviation (STD), both at the ADC output and an off-chip FIR digital low-pass filter.

Figure 17.8.4: LEDs, chip and optical barrier. QE of the photodetector. PPG signals at two LEDs emitting power levels and colors and 2.63 μW at the readout level.

Figure 17.8.5: HR correlation with a commercial ECG chest strap. PPG signal of a subject. The experiment has been performed at 4.6 μW total power (LED+AFE+ADC).

	This work	[2]	[3]	[4]
Year	2018	2015	2016	2018
Technology	180 nm	180 nm	180 nm	180 nm
Supply Voltage	3.3/1.8 ¹	1.8	1.2	3.3
Sampling Frequency	40 Hz	165 Hz	4 Hz	100 Hz
LED Duty Cycle	0.07%	0.7%	0.0125%	0.0175%
Fully Integration ²	Yes	No	No	No
Feature Extraction	HR/SpO ₂ /RR ³	HR	HR	HR
Avg HR error	1.38 bpmf	NA	NA	NA
Max HR error	3 bpmf	NA	10 bpm	2.1 bpm
Power LED	1.97 μW	120 μW ⁴	43 μW ⁴	16 μW ⁴
Power AFE+ADC	2.63 μW	216 μW	172 μW	27.4 μW
Power TOT ⁵	4.6 μW	336 μW ⁶	215 μW ⁶	43.4 μW ⁶

1: ADC supplied at 1.8V.
2: Photosensitive area+AFE+ADC.
3: HR (heart rate), SpO₂ (oxygen saturation), RR (respiration rate).
4: Measured at 4.6 μW total power vs a commercial ECG chest strap on 222 separate measurements on three healthy individuals, corresponding to data from Fig. 5.
5: Best case from the given data.
6: HR mode.

Figure 17.8.6: Comparison table.

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Figure 17.8.7: Micrograph of the fully integrated PPG sensor (4 mm × 5 mm).