28-nm Bulk and FDSOI Cryogenic MOSFET

(Invited Paper)

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***Abstract*—This paper presents an intensive overview of the characterization and modeling of advanced 28-nm bulk and FDSOI CMOS processes operating continuously from room down to deep cryogenic temperature.**

I. Introduction

Over the past few years, the challenges associated with using advanced FETs at cryogenic temperatures for several applications (deep space satellites and rovers, read-out of ultra-low-noise detector arrays, and more recently, quantum computing) have increased. The co-integration of silicon qubits with advanced CMOS processes has attracted great attention recently as a solution to the scale-up difficulty of present-day quantum computers (see Fig. 1a).

II. Physics-based modeling of Cryogenic MOSFET

Very recently a new approach, so-called *body partitioning*, was introduced to obtain a set of analytical expressions for the electrostatic profile and the thicknesses of the freezeout and ionized layers under the gate of a cryogenic MOSFET (see t_{II} and t_{III} in Fig. 1b) [1]. As discussed in [2], the free carrier density strongly defers from the implanted doping concentration at cryogenic temperature, known as freeze-out. However, due to the field effect, the dopants become nearly fully ionized already in early depletion through *field-assisted ionization*. A fully physics-based, dc core model for the long-channel MOSFET operating from room down to deep cryogenic temperature was then developed covering all regions of operation [2]. The proposed model includes the freezeout and field-assisted ionization of the dopants, bandgap widening, mobility reduction, and interface charge traps (see Fig. 1c). The temperature-dependent occupation of interface charge traps degrades the subthreshold swing and a discrepancy between the measured subthreshold swing and the thermal limit appears at cryogenic temperatures. This was explained in [2], treating the interface trapping process and defining the trap potentials similar to what was established in [3]. The bandgap does not have a strong temperature dependence in the cryogenic regime, since the position of the atoms in the lattice and the resulting band structure do not change significantly. Validated by 28-nm bulk CMOS process experimental results [2], the model assumes drift-diffusion transport and derives the charge densities from the Poisson-Boltzmann equation. Boltzmann statistics has been shown to hold down to the deep cryogenic regime ($< 10\,\mathrm{K}$), in the limit to 0 K, however only when incomplete dopant ionization is taken into account. Complete ionization would predict a degenerate semiconductor, rendering the Boltzmann statistics invalid. Furthermore, the value of the intrinsic carrier density in the deep cryogenic regime takes on extremely small values due to the exponential scaling of the Fermi-Dirac distribution, and hence, of the Boltzmann tail.

III. Measurements, Characterization and Compact Modeling of 28-nm Bulk and FDSOI

Fig. 2 shows the measurements and characterization of 28-nm bulk [4], [1] and 28-nm FDSOI [5], [6] CMOS processes from room temperature down to 4.2 K. The transfer characteristics for similar devices of the two processes are shown in Figs. 2a-c and 2e-g. Interface traps strongly degrade the subthreshold swing in the deep cryogenic regime for both processes (Figs. 2d and 2h). This degradation is reflected in the large increase of the slope factor following a $1/T$ law below a critical cryogenic temperature (Figs. 2j and 2l). The threshold voltage increases in the order of 0.2 V due to the net effect of Fermi scaling and incomplete ionization (Figs.2i and 2k). Fig. 3 shows the compact modeling of the 28-nm bulk and FDSOI MOSFETs [1], [4], [5], [6] using the design-oriented simplified-EKV model. For both processes, the transfer characteristics (Figs. 3a-c and 3e-g) and transconductance efficiencies (Figs. 3d and 3h) can be accurately predicted.

IV. Conclusion

An overview on cryogenic modeling of advanced FETs, i.e. commercial 28-nm bulk and FDSOI FETs, is presented. The simplified-EKV compact model was used to accurately capture the DC characteristics of these technologies down to 4.2 K. This constitutes the first milestone towards a complete compact model that can be used for an efficient design of CMOS circuits operating at cryogenic temperatures.

References

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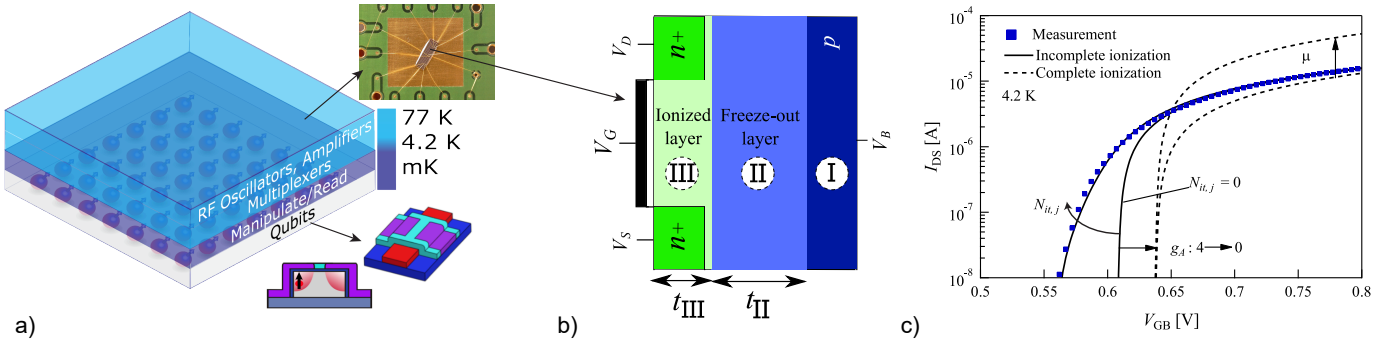

Fig. 1. a) Envisioned 3-D quantum computing architecture, b) Illustration of body partitioning [1] inside a cryogenic MOSFET. Using this technique, in each layer the electrostatic solution can be found explicitly, as well as t_{II} and t_{III} as a function of temperature, doping, and gate voltage [1]. c) Physics-based modeling of cryogenic bulk MOSFET, showing the influence of interface traps (N_{it}) on the degradation of the subthreshold swing at 4.2 K, and the decrease in threshold voltage when incomplete ionization is included.

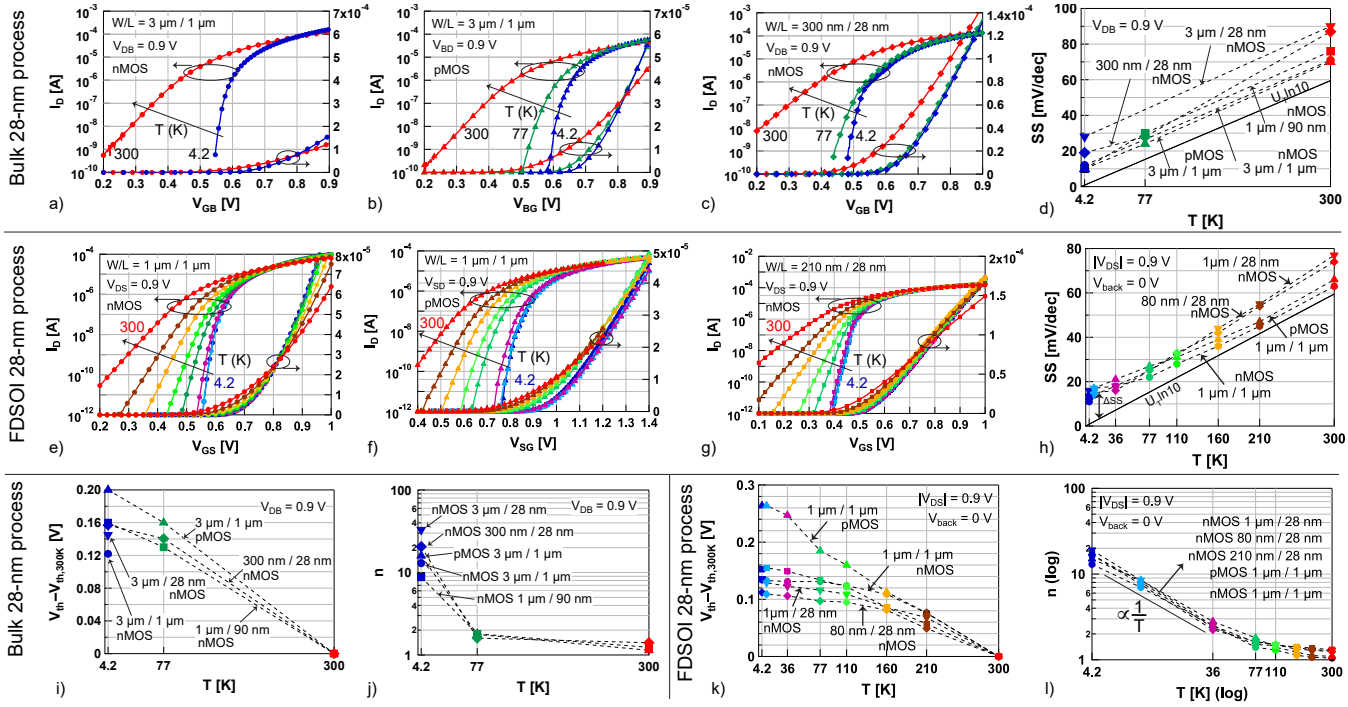

Fig. 2. Measured transfer characteristics and characterization of bulk [1], [4] and FDSOI [5], [6] 28-nm CMOS processes down to 4.2 K.

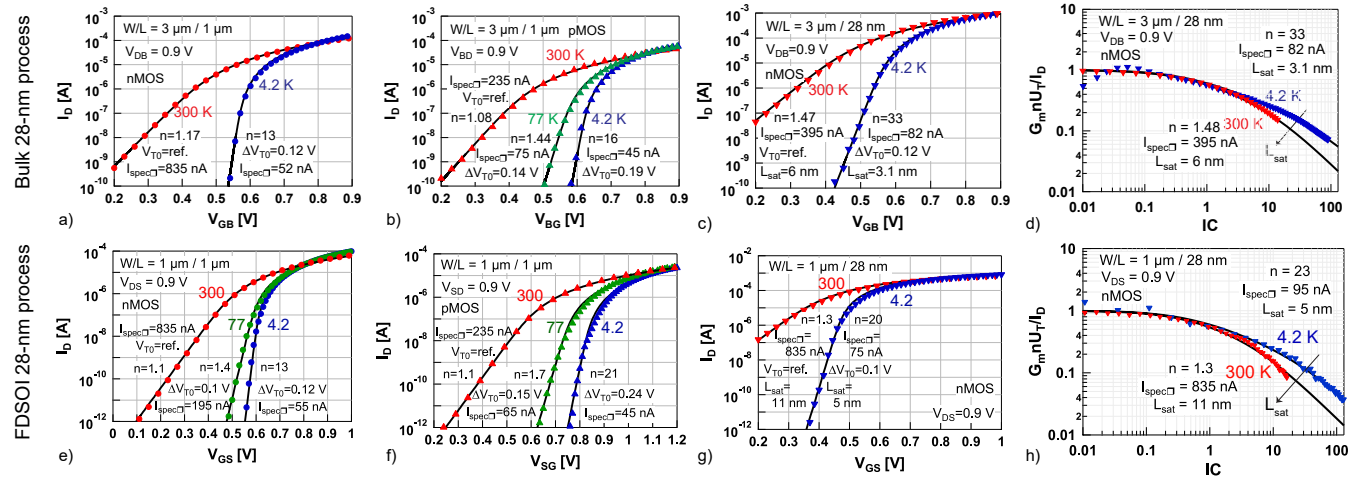

Fig. 3. Compact modeling of 28-nm bulk [1], [4] and FDSOI [5], [6] CMOS processes from room temperature down to 4.2 K. The slope factor n, threshold voltage V_{T0}, specific-current-per-square $I_{spec\square}$, and the saturation length L_{sat} are the model parameters of the simplified-EKV model.