

Exploration of Negative Capacitance Devices and Technologies

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Do the difficult things while they are easy
and do the great things while they are small.
A journey of a thousand miles must begin
with a single step.
— Lao Tzu

To my parents...

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Dr. Ali!

Abstract

Conventional device scaling has been the main guiding principle of the MOS device engineering over these past years. However, this aggressive scaling would be eventually limited due to the inability to remove the heat generated by MOSFET devices. The power dissipation would be lowered significantly if FETs could be operated at lower voltages, which is in contrast with having a sufficiently high on -current. In that pursuit, it was proposed that the minimum voltage requirement could be overcome if the ordinary gate oxide could be replaced by another stack that provides an effective negative capacitance (NC). For a MOSFET, a negative capacitor in the gate stack can make the total capacitance, looking into the gate, larger than the classical MOS capacitance. Thus, to induce the same amount of charge in the channel, one would require a smaller voltage than what would be needed classically. It is well established that ferroelectric materials can provide an effective NC in a certain range of polarization.

The objective of this thesis is to study the negative capacitance effect of ferroelectrics on the performance of field-effect transistors. For this purpose, various NC-FETs and NC-TFETs have been designed and characterized. First, this work proposes a matching condition between the ferroelectric's NC and the gate intrinsic capacitance of the reference transistor to ensure the maximum enhancement due to the NC effect as well as optimizing the hysteretic behavior. Afterward, based on the proposed condition, hysteretic, low hysteresis, and non-hysteretic NC-FETs using 28 nm CMOS node planar MOSFETs and FD-SOI FETs are experimentally demonstrated. In another device structure, the impact of the ferroelectric NC on TFETs is investigated and discussed. It is validated that by combining the advantages of band-to-band tunneling as the carrier injection mechanism and the NC of ferroelectrics, it is possible to obtain steep slope energy efficient switches with improved analog and digital performances. Novel InAs/InGaAsSb/GaSb nanowire TFETs and InGaAs planar TFETs are employed as the reference transistors. The potentials of the recently proposed CMOS compatible ferroelectric, silicon-doped HfO₂, as the NC booster is investigated. The results show that further engineering and advancement is required to optimize the leakage and remanent polarization of this type of ferroelectrics. This work also suggests that a ferroelectric TFET using Si:HfO₂ can be considered as an energy efficient 1T memory that can be scaled down to sub-100 nm technology nodes. Overall, this Ph.D. work highlights and validates the potentials of ferroelectric field-effect transistors for both steep slope and memory applications.

Résumé

La miniaturisation conventionnelle des dispositifs a été le principe directeur principal de l'ingénierie des dispositifs MOS au cours de ces dernières années. Cependant, cette miniaturisation agressive serait finalement limitée en raison de l'impossibilité d'éliminer la chaleur générée par les transistors à effet de champ à grille isolée (MOSFET). La dissipation énergétique serait considérablement réduite si les transistors à effet de champ (FET) pouvaient fonctionner à des tensions plus basses, ce qui rentre en contradiction avec l'obtention d'un courant 'On' suffisamment élevé. Dans cette optique, il a été hypothétisé la possibilité de surmonter cette exigence de tension minimale en remplaçant l'oxyde de grille ordinaire par un autre empilement de matériaux fournissant une capacité négative effective (NC). Pour un MOSFET, un condensateur négatif dans l'empilement de la grille peut rendre la capacité totale, en regardant dans la grille, plus grande que la capacité MOS classique. Il faudrait ainsi une tension inférieure à celle qui serait nécessaire de manière classique pour induire la même quantité de charge dans le canal. Il est bien établi que les matériaux ferroélectriques peuvent fournir une NC effective dans une certaine plage de polarisation. L'objectif de cette thèse est d'étudier l'effet de capacité négative des ferroélectriques sur les performances des transistors à effet de champ. À cet effet, divers NC-FET et NC-TFET ont été conçus et caractérisés. Dans un premier lieu, ce travail propose une condition d'adaptation entre la NC du ferroélectrique et la capacité intrinsèque de la grille du transistor de référence pour assurer une amélioration maximale découlant de l'effet de NC ainsi qu'une optimisation du comportement hystérétique. Dans un second lieu, sur la base de la condition proposée, des NC-FET hystérétiques, peu hystérétiques, et non hystérétiques utilisant des MOSFET planaires dans un nœud CMOS de 28 nm et des FD-SOI FET sont expérimentalement démontrés. Dans une autre structure de dispositif, l'impact de la NC ferroélectrique sur les FET à effet tunnel (TFET) est étudié et discuté. On prouve qu'en combinant les avantages de l'effet tunnel bande à bande en tant que mécanisme d'injection de porteurs de charge et la NC des ferroélectriques, il est possible d'obtenir des commutateurs à forte pente à haute efficacité énergétique offrant de meilleures performances analogiques et numériques. De nouveaux TFET basés sur des nanofils de InAs/InGaAsSb/GaSb et des TFET planaires de InGaAs sont utilisés comme transistors de référence. Le potentiel du HfO₂ dopé au silicium, récemment proposé comme ferroélectrique compatible avec la technologie CMOS, en tant qu'amplificateur de NC est étudié. Les résultats montrent que plus d'ingénierie et de progrès sont nécessaires afin d'optimiser les fuites et la polarisation rémanente de

Résumé

ce type de ferroélectriques. Ce travail suggère également qu'un TFET ferroélectrique utilisant du Si:HfO₂ peut être considéré comme une mémoire 1T à basse consommation énergétique pouvant être miniaturisée à des nœuds technologiques inférieurs à 100 nm. Globalement, ce travail de doctorat met en évidence et valide le potentiel des transistors à effet de champ ferroélectriques pour les applications de commutateurs à forte pente et de mémoire.

Acronyms

AC	Alternate Current
AFM	Atomic Force Microscopy
BHF	Buffered Hydrofluoric acid
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
FET	Field-Effect Transistor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
GND	Ground
IC	Integrated Circuit
LTO	Low Thermal Oxide
MEMS	Micro Electro Mechanical System
MIS	Metal Insulator Semiconductor
NEMS	Nano Electro Mechanical System
NVM	Non Volatile Memory
PZT	Lead Zirconate Titanate
RT	Room Temperature
SEM	Scanning Electron Microscopy
SOI	Silicon On Insulator
FD-SOI	Fully Depleted Silicon On Insulator
TEM	Transmission Electron Microscopy
VLSI	Very Large Scale Integration
SBT	Strontium Bismuth Tantalate
Si:HfO ₂	Silicon-doped HfO ₂

Units of measurements

$^{\circ}\text{C}$	Celsius degree
A	Ampere
C	Coulomb
eV	electron Volt
J	Joule
$^{\circ}\text{K}$	Kelvin degree
kg	Kilogram
m	Meter
N	Newton
s	Second
V	Volt
W	Power
Ω	Ohm

SI decimal prefixes

Tera	T	10^{12}
Giga	G	10^9
Mega	M	10^6
kilo	k	10^3
hecto	h	10^2
Deca	da	10^1
		1
deci	d	10^{-1}
centi	c	10^{-2}
milli	m	10^{-3}
micro	μ	10^{-6}
nano	n	10^{-9}
pico	p	10^{-12}
femto	f	10^{-15}

Physical constants

Elementary Charge	e (or q)	$= 1.60206 \times 10^{-19} \text{ C}$
Planck Constant	h	$= 6.62606896 \times 10^{-34} \text{ J.s}$
Boltzmann Constant	k_B	$= 8.617343 \times 10^{-5} \text{ eV.K}^{-1}$
Free Space Permittivity	ϵ_0	$= 8.85418782 \times 10^{-12} \text{ F.m}^{-1}$
Air Relative Permittivity	ϵ_r	$= 1$
Speed of Light	c	$= 2.99792458 \times 10^8 \text{ m.s}^{-1}$
Number Pi	π	$= 3.14159265$

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1 Introduction

Abstract:

In this chapter, a general introduction to the CMOS scaling and the increasing power challenge, arising from physical limitations of MOSFET switches, is presented. It is remarked that the increasing power dissipation issue can be addressed by the evolution of small swing switches. The solutions that have been found by now to achieve a subthreshold swing below the 60 mV/decade thermal limit of MOSFETs, are introduced. Next in this chapter, the operation principle of negative capacitance transistors, as one of the most important steep slope switch candidates, will be demonstrated. By exploiting the general theory of ferroelectrics and the approach of the Landau model, it is explained that ferroelectric materials can provide an effective negative capacitance in a certain range of operation. The negative capacitance region of ferroelectric materials can be utilized to reduce the subthreshold swing of conventional transistors. Exploration of negative capacitance devices is the main topic of this thesis. The rest of this chapter dedicates to the comparison of ferroelectric materials and their potentials for the integration with the CMOS technology. Lastly, a quick overview of this Ph.D. work is presented.

1.1 CMOS scaling and MOSFET limitations

Microelectronics was among the most leading technologies in the past recent years. All the developed industries that are affecting the everyday life of human beings owe their achievements to the advancement of microelectronics. Everything started with the invention of the transistor by W. Shockley, J. Bardeen, and W. Brattain in 1947 [1]. The transistor was the first manufactured device that could turn the signal *on* or *off* and amplify it in the on-state. This was called "the most important invention of 20th century" and it was just the beginning of a long road toward modern electronics and integrated circuits. It is no understatement to say that modern electronic devices could not be able to function without a transistor processing electrical signals [2].

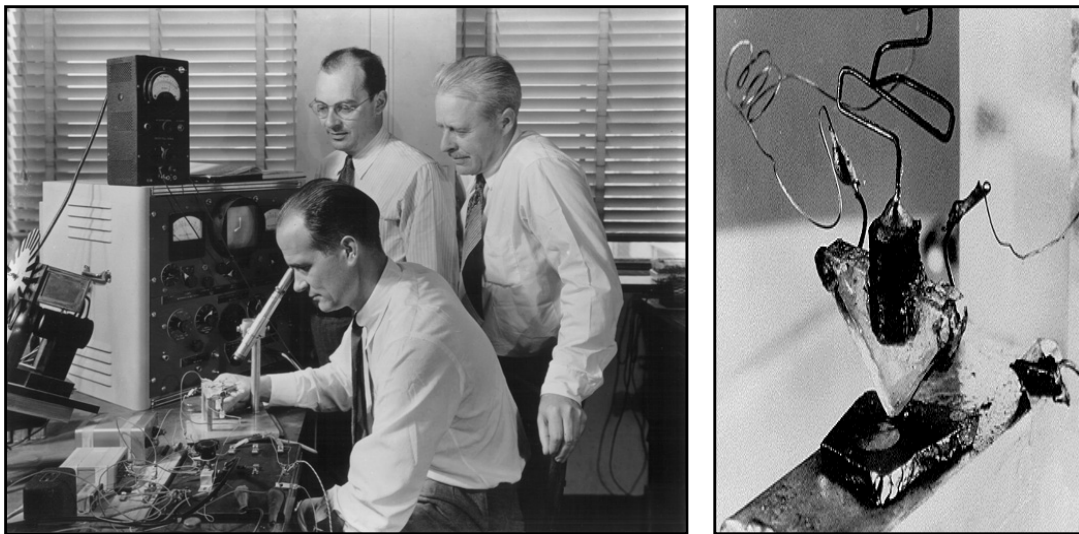


Figure 1.1 – John Bardeen, William Shockley, and Walter Brattain (left) and their first transistor (right) [1].

The silicon technology has advanced with an exponential rate in terms of performance and productivity during past decades, which was anticipated by Moore in 1965 [3]. Moore's Law was actually based on observation regarding the optimized density of transistors in terms of cost. It arises from the fact that the cost decreases by increasing the number of transistors, but it also increases the chance of having defects. Moore stated that the number of transistors on an integrated circuit would be doubled every two years. This law became a self-fulfilling prophecy for the semiconductor industry and was valid until now, which is evidenced by the International Roadmap for Semiconductors (ITRS) [4].

The scaling in microelectronics has been driven by the demand for a higher density integration in order to minimize the fabrication cost and also increase the speed. The switching energy of a silicon MOSFET can be calculated by $0.5\epsilon_d(V_{DD} \times L_{ch})^2/d_d$ where ϵ_d refers to the dielectric permittivity, V_{DD} is the supply voltage, L_{ch} represents the

Introduction

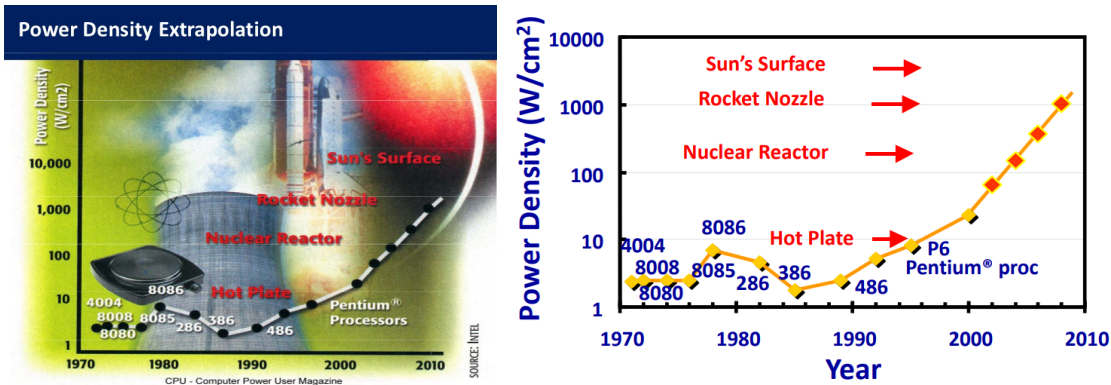


Figure 1.3 – Increasing power challenge involved in the scaling of CMOS [3, 6].

MOSFETs with the minimum gate length of $5\ \mu\text{m}$, but devices with smaller gate lengths were already built in laboratories that were demonstrating the benefits of further scaling. The scaling principles by Dennard were quickly adopted by the semiconductor industry as the roadmap. The results of the Dennard’s scaling rules are summarized in Table 1.1.

Table 1.1 – Dennard’s scaling rules at the device and circuit levels [7].

Device and circuit parameters	Scaling factor
device dimension: t_{ox} , W , L	$1/K$
doping concentration: N_A , N_D	K
voltage	$1/K$
current	$1/K$
capacitance $A\epsilon/t$	$1/K$
delay time VC/I	$1/K$
power dissipation VI	$1/K^2$
power density VI/A	1
electric field	1

The proposed ideas by Dennard and Moore set the course of semiconductor industry on developing new integrated processes and products on a regular pace and providing consistent improvements in the transistor density, performance, and power. Each new generation of technology was expected to reduce the minimum feature size by a factor of 0.7 ($K \sim 1.4$). Indeed by applying the rules of scaling, the dissipated power remains constant and the frequency, f , increases by K . These rules have been fulfilled ever since, until sub-65 nm technology nodes. Below the 65 nm CMOS technology node, the Dennard’s scaling rules are no longer working as well as they did before due to the challenges involved in the voltage scaling.

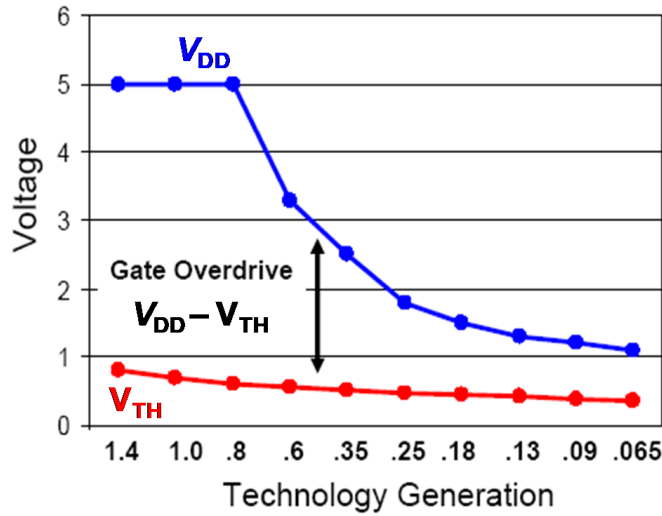


Figure 1.4 – V_{DD} scaled more than V_{TH} which leads to the reduction of the gate overdrive, $(V_{DD}-V_{TH})$ [9].

The voltage scaling has an extremely important role in the CMOS scaling due to numerous reasons such as reliability, lowering the transistor power, and maintaining the constant power density. Dennard assumed that the threshold voltage, V_{TH} , of transistors, would scale down along with the supply voltage and provides improved performance and power. However, Dennard ignored the impact of the sub-thermal leakage of the transistor on the total power consumption of the chip. This sub-thermal leakage was low by the time (back in 1970s) and was a small fraction of the logic circuits power consumption. Nevertheless, after years of scaling, V_{TH} has been scaled to the point where the leakage current has increased significantly. Thereby, it is impossible to further scale V_{TH} and hence, scale the operation voltage. This can be clearly observed in Figure 1.4, which shows the scaling trend of V_{DD} and V_{TH} from the 1.4 μm technology node to 65 nm. The supply voltage is decreased down to 20% of its starting value while the threshold voltage could not be scaled more than 50% [8].

The main consequence of the supply voltage scaling without a sufficiently scaled threshold voltage is the decrease of the overdrive voltage, $V_{OV}=V_{DD}-V_{TH}$. This results in a reduced on -current, which can be formulated as $I_{ON} = 0.5\mu C_{OX}(W/L) \times (V_{DD}-V_{TH})^2$ when the device is working in the saturation region. Hence, the performance and the dynamic speed of the transistor, $C_g V_{DD}/I_{ON}$, decreases. The first solution to overcome this issue and provide an acceptable performance/overdrive is slowing down the supply voltage scaling.

Figure 1.5 depicts the scaling of the channel length, gate dielectric thickness, and the supply voltage. The scaling of the channel length, L_g , is the only parameter that has been scaled down properly. In contrast, the scaling of V_{DD} , as well as that of the electrical oxide thickness, is clearly deficient. The supply voltage almost remains constant

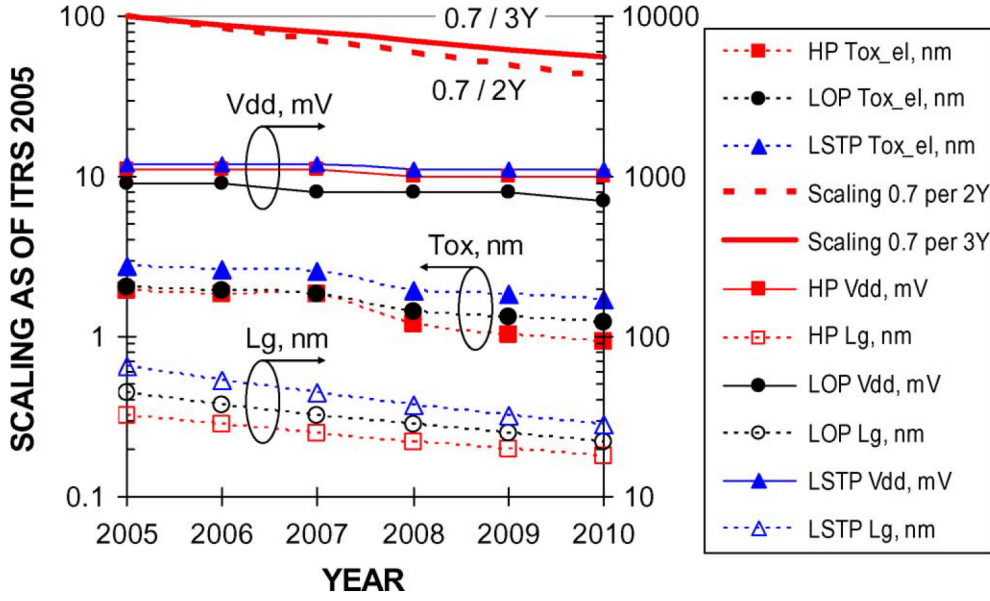


Figure 1.5 – Scaling of the supply voltage, gate dielectric thickness, and the gate length [9].

because of many reasons, but the most important one is the race for the performance.

In case of the ideal scaling of the supply voltage along with device dimensions, the power density ($I_{ON}V_{DD}/A$) remains constant. This means that the energy needed to drive the chip and the resulting heat generated by the transistors remains constant. When V_{DD} does not scale down along with the device dimensions, the power density increases. The total energy dissipation of each transistor can be calculated by sum of the dynamic power (the dissipated power during the switching of the transistor) and the static power (consumed power in the off-state).

The dynamic power is usually modeled by equation 1.1, where f is the frequency and C_L is the total switching capacitance load:

$$P_{dyn} = f \times C_L \times V_{DD}^2. \tag{1.1}$$

The static power originates from the leakage of transistors during their off-state:

$$P_{static} = I_{leakage} \times V_{DD}, \tag{1.2}$$

where $I_{leakage}$ is the total leakage current of the transistor while it is operating in the off-state. The scaling of the transistor dimensions without a sufficient reduction of the supply voltage leads to a considerable increase in the power consumption [10].

The second possibility to have a sufficiently high overdrive, rather than keeping V_{DD}

1.1. CMOS scaling and MOSFET limitations

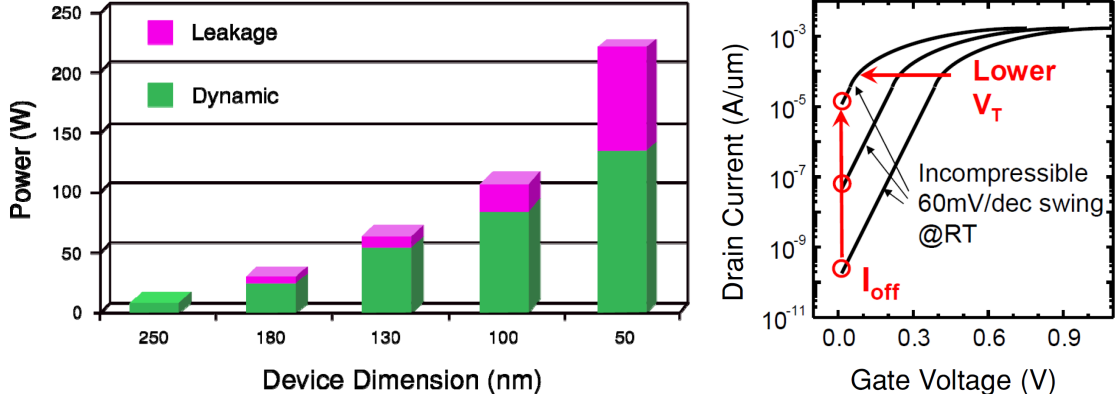


Figure 1.6 – Static power is increasing much faster than the dynamic power (left) [12] due to the incompressibility of the SS and scaling of the threshold voltage [13].

high, is to scale down the threshold voltage. The scaling of V_{TH} is actually the main reason for the faster increase of the static power comparing the dynamic power which can be traced back to a physical limitation in MOSFET switches. The steepness of the *off*-to-*on* transition of a switch is characterized as the minimum gate voltage required for a 10-fold increase in the drain current, known as the subthreshold swing (SS). The general expression for the subthreshold swing of a MOSFET is [11]:

$$SS = \left[\frac{\partial V_g}{\partial (\log_{10} I_d)} \right] = \frac{\partial V_g}{\partial \psi_s} \times \frac{\partial \psi_s}{\partial \log_{10} I_d}, \quad (1.3)$$

where ψ_s denotes to the surface potential of the semiconducting channel. The first term of the right-hand side of equation 1.3, which is known as the m-factor (body factor), generally has a value greater than one since V_g is linked to ψ_s through a capacitive voltage divider.

The second term, n-factor, has a lower limit of $(kT/q) \ln 10$, 60 mV/decade at 300° K, in a conventional MOSFET or any device using the thermionic injection of carriers over an energy barrier as the main operating principle. This limit is a consequence of the thermally broadened Fermi-distribution of carriers which is irrespective of dimensionality or the material in use. The reduction of the threshold voltage by 60 mV under the noted limit will translate in increasing the *off*-current by a factor of 10 and hence, increase of the static power (Figure 1.6). It should be noted that the minimum swing of a MOSFET can be also written as

$$SS = \left(1 + \frac{C_s}{C_{ins}} \right) \frac{kT}{q} \ln 10, \quad (1.4)$$

where C_s and C_{ins} are the semiconductor and insulator capacitances, k is the Boltzmann constant, and q is the elementary charge.

Today, the static power (the consumed power in the off-state of transistors) is

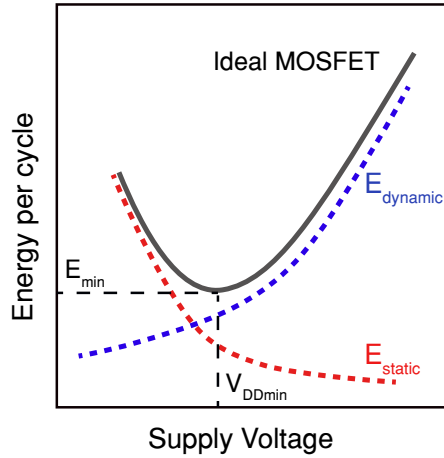


Figure 1.7 – Increased leakage (static) power dominates over the dynamic power in modern chips [15].

dominated over the switching (dynamic) power and became the most important challenge of the CMOS industry. This is mainly because of the Boltzmann limit on the subthreshold swing of MOSFETs and also the broken scaling rules. Figure 1.7 shows the constraint of the dynamic and static power that defines the minimum energy per cycle of operation [14].

1.2 Concept of ideal switch

Rescue strategies for the increasing leakage power challenge can be followed in two main directions: (i) circuit level by developing new software/hardware techniques dedicated to power saving and (ii) device level by identifying novel power aware or energy efficient device architectures. The most reasonable approach is to find a device level solution by identifying energy efficient switches, having a transfer characteristic closer to the one of the ideal switch.

An ideal switch supposes to provide an *on*-current as high as possible together with an almost zero *off*-current, thus maximizing the I_{ON}/I_{OFF} ratio (Figure 1.8). Additionally, the ideal switch should have a super steep *off*-to-*on* transition, near 0 mV/decade, in order to make us eligible to scale down the threshold voltage without increasing the leakage current.

Due to the fact that it is impossible to actually demonstrate an ideal switch, small swing switches would provide a more realistic device level solution. A small swing switch should have sub-thermal SS and a smaller *off*-current in comparison with a conventional MOSFET. Therefore, a small swing switch makes it possible to reduce the supply voltage

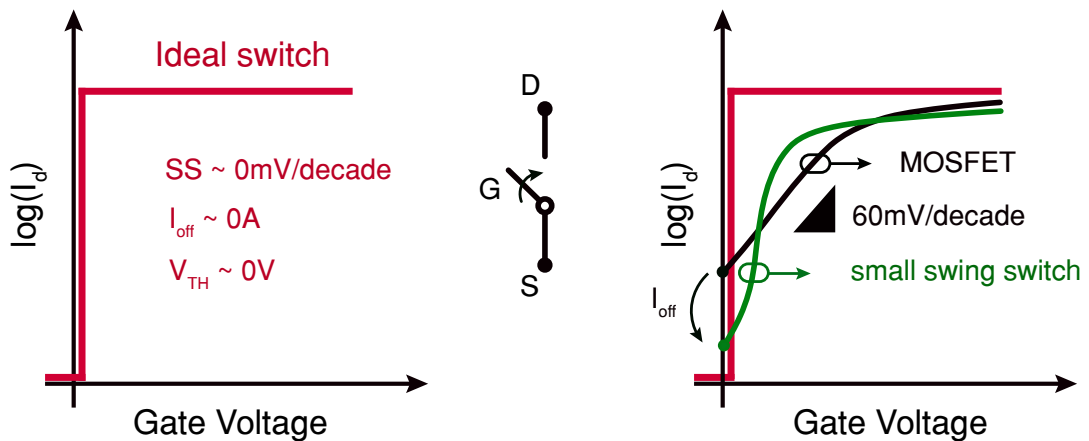


Figure 1.8 – Transfer characteristic of an ideal switch (left) and comparison of an ideal switch, a MOSFET, and a small swing switch (right).

without performance loss and simultaneously deals with the increasing static power issue. Figure 1.8 shows and compares the transfer characteristic of a conventional transistor with a small swing switch and also an ideal MOSFET.

Considering equation 1.3, a sub-thermal swing can be achieved by two means:

(i) reducing the second term in the right-hand-side (RHS) of equation 1.3, known as the n-factor, below 60 mV/decade (at room temperature). This can happen by employing other physics principles, rather than the thermionic injection of carriers over a barrier, to inject charge carriers into the channel.

(ii) another prominent way of reducing the subthreshold swing to lower the body factor, the first term in the RHS of equation 1.3, is integrating new materials or physics into the gate stack of transistors. In a conventional MOSFET, the body factor, which relates to the electrostatic coupling of the gate to the channel, is always greater than 1.

1.3 Small swing switches

To overcome the so-called "Boltzmann Tyranny", several steep switching devices are proposed to provide a sub-thermal swing by either reducing the n-factor or body factor of transistors. Lowering one of the two terms could lead to a steeper switching compared to the conventional MOSFETs.

Any attempt to modify the subthreshold slope of transistors must necessarily involve either modifying the mode of carrier injection from diffusion-based to tunneling-based mechanisms or steepening the nonlinearity using an amplifier.

Among alternative structures, Tunneling Field-Effect Transistors (TFETs) [15], Im-

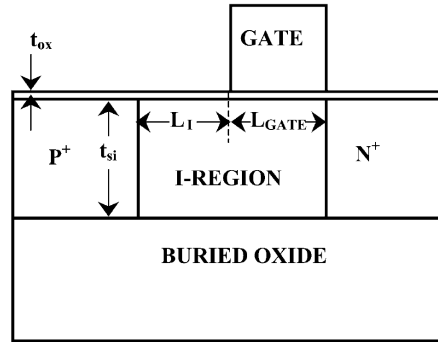


Figure 1.9 – Device schematic of an I-MOSFET [20].

pact Ionization MOSFETs (I-MOSFETs) [16], NanoElectromechanical FETs (NEMFETs) [17], and Negative Capacitance MOSFETs (NC-FETs) [18] have been extensively studied as the promising steep slope switches. In the following, we briefly describe each of the noted candidates.

1.3.1 Impact Ionization MOSFETs

Use of an amplifier to enhance the on-state and suppress the off-state seems to be an interesting solution, but this approach needs to address the following major challenges [19]:

(i) the amplification mechanism must be internal to the device and must arise from some gain within the device.

(ii) the device must not latch up and a fast mechanism such as drift, rather than recombination, must remove all the injected carriers while the device is switching from on to off-state.

(iii) the most important challenge arises is that a finite bandwidth associated with every gain mechanism and the gain-bandwidth product may impose fundamental limitations on the intrinsic switching speed of the device.

The impact ionization related breakdown was found such a gain mechanism that fulfills all the noted conditions. In this regard, impact ionization MOSFET (I-MOSFET) is proposed by employing the modulation of the avalanche breakdown voltage of a gated-structure to switch from *off-to-on* and vice-versa [21, 22]. In this type of transistors, a p-n junction diode is used in the post-breakdown mode (i.e., with voltages higher than the breakdown voltage). The delay of an I-MOSFET is proportional to the logarithm of the desired gain and hence, it is very fast. As a result, the subthreshold swing of an I-MOSFET can reach values much lower than the $(kT/q)\ln 10$ limit of a conventional MOSFET [23, 24].

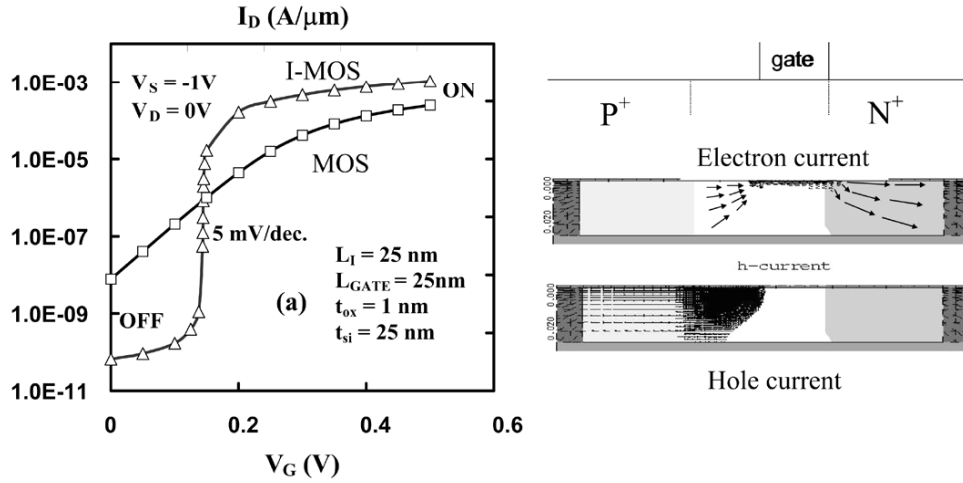


Figure 1.10 – Simulated transfer characteristic of an I-MOSFET with a sub-thermionic swing [20].

The device structure of an n-channel SOI impact ionization MOSFET is presented in Figure 1.9. This n-channel device has an overlap with the drain (n+) and an offset toward the source (p+) side of the device. Figure 1.10 demonstrates the simulated results of the described structure, achieving a swing of about 5 mV/decade. Experimental reports also confirm the possibility of having a sub-thermionic swing in an I-MOSFET [21].

The main challenge of impact ionization MOSFETs relates to their reliability over time. An avalanche breakdown requires the presence of hot carriers in high densities that compromises the reliability. Hot electrons can be trapped in the oxide after a period of time which changes the threshold voltage [25].

1.3.2 Tunneling Field-Effect Transistors

Tunnel field-effect transistors (TFETs) [26] have attracted a great deal of attention for achieving a steep subthreshold swing by employing quantum mechanical band-to-band tunneling (BTBT) of carriers from source to the channel (reducing n-factor to values below 60 mV/decade) [27]. The current of a TFET is the integral of the transmission probability, T_{WKB} , of the interband tunneling over the source-channel junction, which can be approximated as [28]:

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q(E_g \Delta\Phi)}\right), \quad (1.5)$$

where m^* is the effective mass and E_g is the bandgap. Here, λ is the screening tunneling length that describes the spatial extent of the transition region at the source-channel interface. In a TFET (Figure 1.11), at a constant drain voltage (V_d), the increase of the

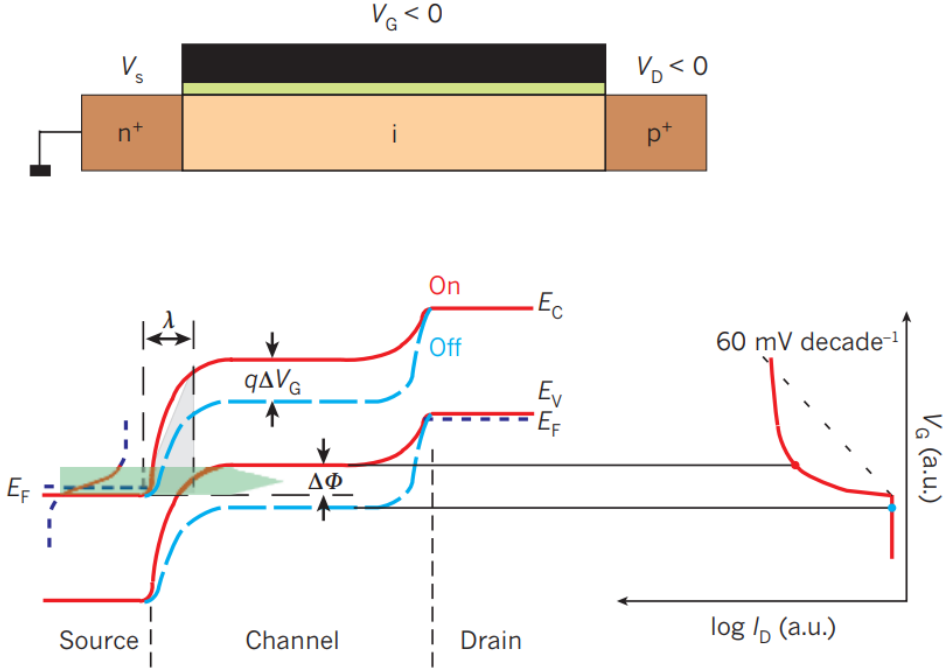


Figure 1.11 – Schematic cross-section of a p-type TFET (top). The energy band diagram (bottom) of the TFET is presented for its on-state (red line) and off-state (dashed blue line)[15].

gate voltage (V_g) modulates the device surface potential, which reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel ($\Delta\Phi$).

The subthreshold swing of a TFET can be calculated as:

$$SS = \frac{\partial V_g}{\partial(\log_{10} I_d)} = \ln(10) \left[\frac{\partial V_d}{V_d \partial V_g} + \frac{E b}{E^2} \frac{\partial E}{\partial V_g} \right]^{-1}, \quad (1.6)$$

where V_d is the drain voltage, E is the electric field, and b is a constant. Equation 1.6 reveals that the SS of a TFET is not limited by the Boltzmann electron energy distribution.

Recently, highly scaled vertical InAs/InGaAsSb/GaSb nanowire TFETs with well below 60 mV/decade subthreshold swings are experimentally fabricated [29, 30]. The nanowire structure and the corresponding electrical measurements of TFETs are depicted in Figure 1.12. Some of the presented devices show the ability to reach a value of SS down to 43 mV/decade. This outstanding performance has been achieved by realizing an extremely low defect interface regarding the III-V heterojunction, which is one of the main limitations to achieve an SS well below the thermal limit of MOSFETs in III-V TFETs.

However, the *on*-current of TFETs is unacceptably low for a technology which

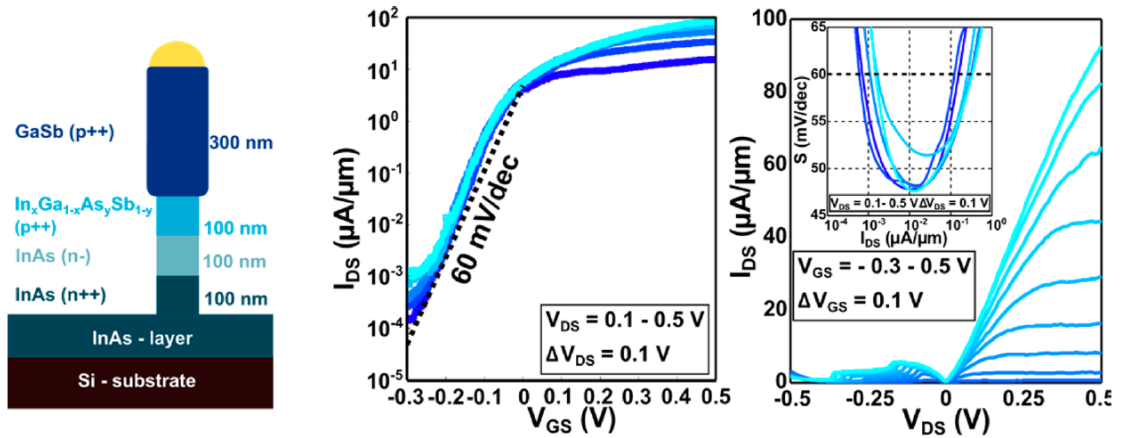


Figure 1.12 – Nanowire structure (left) and electrical measurements (right) of vertical InAs/InGaAsSb/GaSb nanowire TFETs, showing a sub-thermionic swing [30].

would like to replace the CMOS technology. Moreover, achieving $SS < 50$ mV/decade is extremely challenging in the most fabricated TFETs and the steep slope region is typically limited to 1-3 decades of the drain current, which is far less than that of a MOSFET (4-6 orders). Therefore, providing an acceptable I_{ON}/I_{OFF} ratio together with a sufficiently low SS has emerged as one of the most important technology issues involved in the fabrication of TFETs.

1.3.3 Nano ElectroMechanical Field-Effect Transistors

The convergence of silicon CMOS and MEMS technologies in terms of functionality added devices that combine MEMS and solid-state principles, such as NanoElectroMechanical (NEM) FETs or Suspended-Gate (SG) MOSFETs [31]. This type of transistors has been suggested to break theoretical limitations of the solid-state MOSFET, such as the 60 mV/decade limit on the subthreshold swing [32].

The principle of the SG-MOSFET is shown in Figure 1.13 where a metal gate is suspended over the oxide or semiconducting channel of an MOS transistor by supporting arms (with an equivalent stiffness of k). When the gate voltage is set at 0 V, the air-gap between the gate and channel make the *off*-current of the transistor at its lowest possible value. By applying a voltage on the gate, a combined electro-mechanical action results: while the inversion of the channel is forming, the gate deflects vertically and increases the gate to channel capacitance. This leads to a super-exponential dependence of the inversion charge on the applied gate voltage in the subthreshold regime. The gate approaches the channel and at a point, when the equilibrium condition of the mechanical elasticity and the electric field is not anymore fulfilled, the gate collapses and sticks to the substrate. This results in an abrupt increase in the drain current [17].

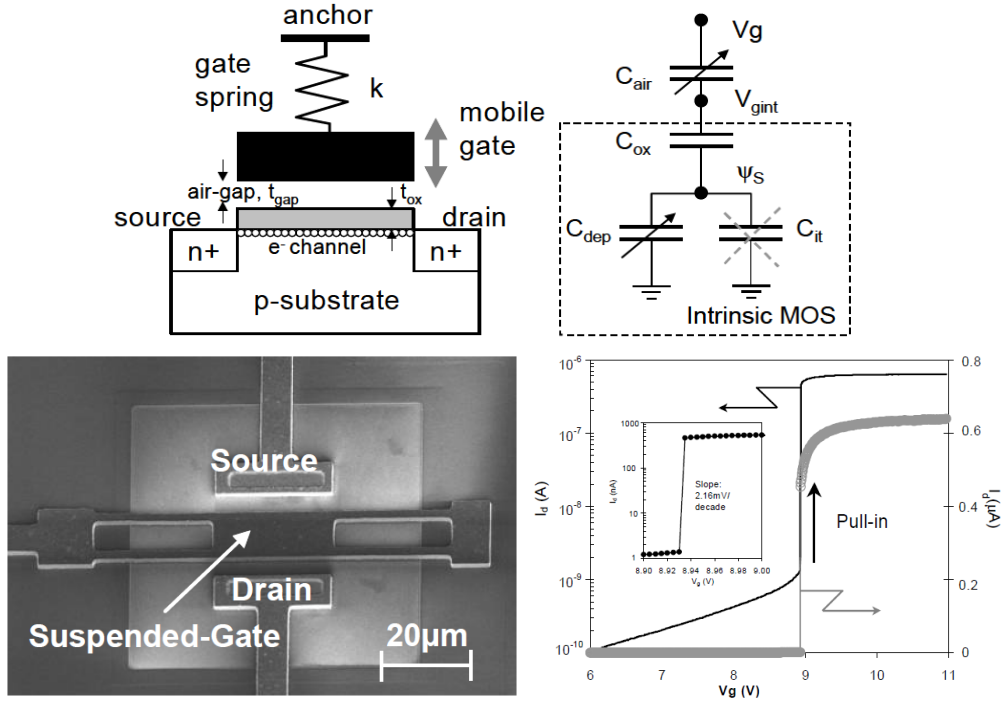


Figure 1.13 – Schematic and operation principle of an SG-MOSFET (top) along with an experimentally fabricated device and its electrical characteristic (bottom) [33].

Figure 1.13 also shows the Scanning Electron Microscopy (SEM) image of a fabricated suspended-gate MOSFET with a physical length of 20 μm and a width of 4 μm . The transfer characteristic of the described switch demonstrates a super steep transition of 2 mV/decade. The main drawback of this kind of switches is the need for a high pull-in voltage (tens of volts). The suspended-gate MOSFET switch also suffers from the hysteresis of the drain current due to the additional force, which is required to eliminate the sticking energy and separate the gate from the substrate.

1.3.4 Ferroelectric Field-Effect Transistors

It has been proposed that if we integrate a ferroelectric insulator, having a polarization characteristic as described in Figure 1.14, into the gate stack of a conventional MOSFET, it is possible to obtain values of the body factor less than one and hence a value of SS below 60 mV/decade at 300° K [34, 35]. This can be understood by considering the fact that a ferroelectric capacitor can perform as an effective negative capacitance (NC) around the origin ($Q = 0$) [36]. This negative slope of the polarization is ordinarily unstable and cannot be observed in experiments, exhibiting hysteretic jumps in the polarization. However, it is evidenced that the noted negative segment can be stabilized if the ferroelectric placed in series with a positive capacitor of proper value [37].

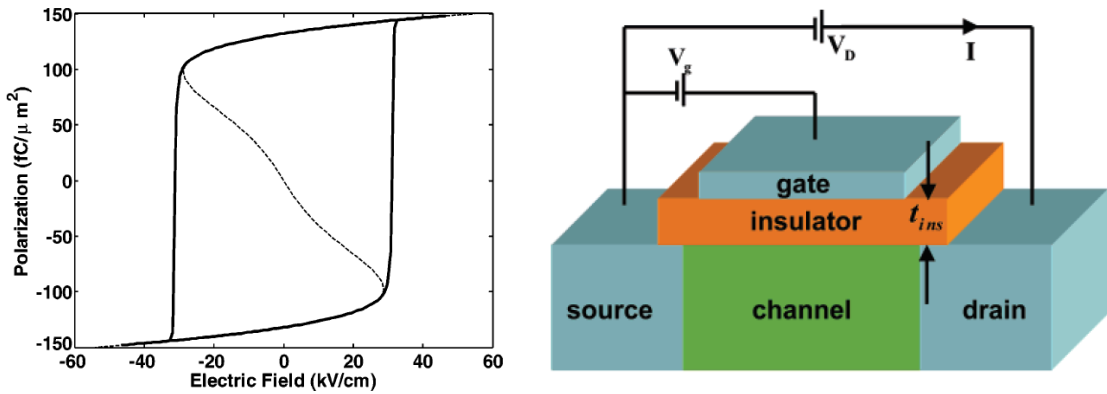


Figure 1.14 – Polarization characteristic of a ferroelectric material and its ability to provide an effective NC while integrated to the gate of an MOS device [18].

A ferroelectric capacitor interconnecting with the gate stack of an MOS transistor creates a series connection between the ferroelectric capacitor (C_{FE}) and the gate intrinsic capacitance of the MOS transistor (C_{MOS}). The ferroelectric capacitor can increase the total capacitance of the gate ($C_{total}^{-1} = C_{FE}^{-1} + C_{MOS}^{-1}$) if it operates in the NC regime. Accordingly, an NC booster can provide an internal voltage amplification which results in a body factor reduction, leading to an improved subthreshold [38].

The rest of this chapter is dedicated to ferroelectric materials, physics behind the negative capacitance of ferroelectrics, and the operation principle of NC transistors which are the main topics of interest in this thesis.

1.4 Ferroelectric materials

1.4.1 History

The phenomenon of ferroelectricity was discovered in 1921 by J. Valasek who was investigating the dielectric properties of Rochelle salt ($\text{NaKC}_4\text{H}_4\text{O}_6 \cdot 4\text{H}_2\text{O}$) [39]. At its early age, ferroelectricity was considered only as an academic curiosity with a little application value. Certainly, one of the major turning points in ferroelectricity came in the early 1940s with the discovery of unusual dielectric properties of mixed oxides that crystallize in the perovskite structure. Barium Titanate (BaTiO_3) was discovered to be a robust ferroelectric in 1943 by A. Van Hippel. Since then, ferroelectric oxides were widely used as capacitors in the electronics industry. Afterward, until the 80s, the main challenges in ferroelectric materials were the modeling of the operation principle of ferroelectrics as well as the discovery of novel materials. Perhaps the most significant theoretical development in ferroelectricity occurred in 1960 with the formulation of the elegant soft-mode description of the ferroelectric transition made almost simultaneously and independently by Cochran and Anderson [40]. This was followed by integration of

ferroelectric thin films on silicon integrated circuits [41].

The development of ferroelectric thin films was a significant step towards the integration of this type of materials in electronic components. This can be highlighted by taking into account the polarization reversal of ferroelectrics as their main functionality. The base characteristic of all ferroelectric materials is the hysteretic behavior relating the polarization (P) to the electric field (E). There is a nominal threshold, called the coercive field (E_c), above which the polarization changes sign. The polarization of a typical ferroelectric requires an electric field of about 50 kV/cm. This means that a 1 mm bulk ferroelectric needs about 5 kV to switch from one stable polarization state to the other one which is not suitable for any kind of electronic devices. However, for a thin film with a thickness of micrometer/nanometer range, the coercive voltage would be less than 5 V which opens a path to the integration of ferroelectrics in ICs [42].

The most important use of ferroelectric materials relates to the memory applications. Ferroelectrics offer an electrically switchable, two-state device. Such a device could encode the 1 and 0 states required for the Boolean algebra of binary computer memories [43]. Nowadays, there are several research directions regarding ferroelectricity such as ferroelectric memories (DRAM and FeRAM), finite size effect, substrate-film interface, piezoelectric devices, developing novel CMOS compatible ferroelectrics, and ferroelectric transistors as steep slope switches.

This thesis is focused on the applications of steep switching transistors by exploiting the negative capacitance region of ferroelectrics. A CMOS compatible ferroelectric, silicon-doped HfO_2 , is developed along this Ph.D. work. Additionally, the potentials of this type of ferroelectric as a negative capacitance booster of MOS transistors is investigated.

1.4.2 Ferroelectricity

A ferroelectric is a sort of materials that provide a permanent electric dipole. The name "ferroelectric" is taken from "ferromagnetic" as ferromagnetic materials have a permanent magnetic dipole. In fact, in one of the earliest observations of ferroelectricity by Rochelle, the salt was described as "analogous to the magnetic hysteresis in the case of iron" [39]. Ferroelectricity can be understood by looking in the physics of small molecules. A non-symmetric molecule has a dipole moment which is defined as

$$\vec{P} = \int dV \rho(\vec{r}) \vec{r}, \quad (1.7)$$

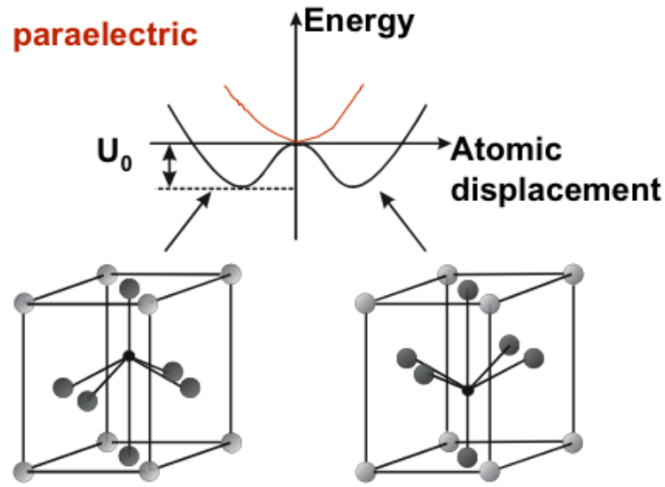


Figure 1.15 – Crystal structure of BaTiO₃ in its two different polarization states [44].

where $\rho(\vec{r})$ is the charge density of the molecule. Considering atoms as point charges Q_i at the corresponding position of R_i ;

$$\vec{P} = \sum Q_i \vec{R}_i. \quad (1.8)$$

The ferroelectricity is prohibited if there is a center of symmetry. Otherwise, the crystal classes have one or more polar axis. Those with a unique polar axis are ferroelectric and provide spontaneous polarization. The rest demonstrate a piezoelectric effect, inducing an electric polarization under mechanical stress [37]. In another word, the spontaneous polarization of ferroelectrics originates from the atomic arrangement of ions in the crystal structure. A crystal with a polar group can provide a non-zero spontaneous polarization. However, in the case of ferroelectric materials, the polarization should be switchable between two stable states. The example of BaTiO₃, as the first discovered robust ferroelectric, is depicted in Figure 1.15. The Ti ion displaced between two different states, breaking the symmetry.

In an electric field of \vec{E} , the two stable states no longer have the same energy due to the electric polarization energy of $\vec{P} \cdot \vec{E}$ and the wells get tilted by the externally applied electric field. It should be noted that the polarization does not switch immediately because there is a barrier to be overcome. In an ideal case, there will be hysteresis as it is presented in Figure 1.16 which simply explains the hysteretic behavior of a ferroelectric material. However, it should be noted that the mentioned explanation is too simple to describe the operation principle of real ferroelectrics due to the fact that all dipoles never switch together. Nucleation of the polarization reversal usually occurs in particular locations in a real ferroelectric. Each time that the polarization gets switched, domains

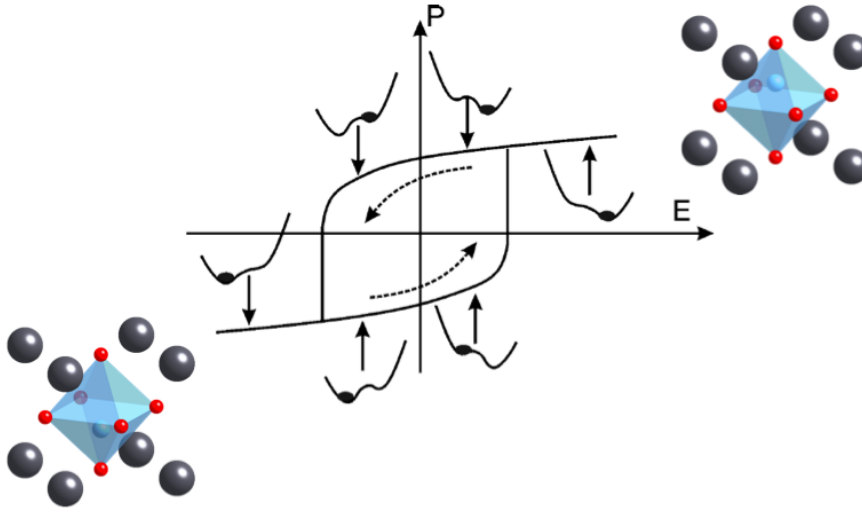


Figure 1.16 – Phase transition of ferroelectric BaTiO₃ [44].

nucleate at the same favorable sites. Afterward, the nucleate sites grow. The period of the domain growth strongly depends on the properties of the material itself, geometry, and the strength of the applied electric field [37].

1.4.3 Landau's theory

The Landau-Ginzburg-Devonshire theory (simply called Landau's theory) can provide a reliable description of a system's behavior near a phase transition based on symmetry considerations. The Landau's theory defines a phenomenological description of the macroscopic properties [46]. Generally, the thermodynamic state of a system in equilibrium can be determined by specific variables. In the case of bulk ferroelectrics, temperature (T), polarization (P), electric field (E), stress (σ), and strain (η) are the mentioned variables. A fundamental postulate of the applied thermodynamics to a ferroelectric is that its free energy G can be expressed as a function of 10 variables. The Landau theory actually expands the free energy in powers of the dependent variables, with known coefficients that can be fitted with experiments [34]. This approach is a straightforward phenomenology to link measurable thermodynamic quantities in the vicinity of a phase transition. It should be remarked that the Landau theory is a macroscopic model and cannot explain the microscopic physics behind the phase transition. Figure 1.17 depicts the schematic of the relationship between Landau's theory, first-approach calculations, microscopic models, and experimental data. In general, Landau's theory can be calculated from the first order calculation or a microscopic model and validated experimentally.

Here, we take a simple example and expand the free energy in terms of a single component of the polarization and ignore other variables, which can be adequate for a

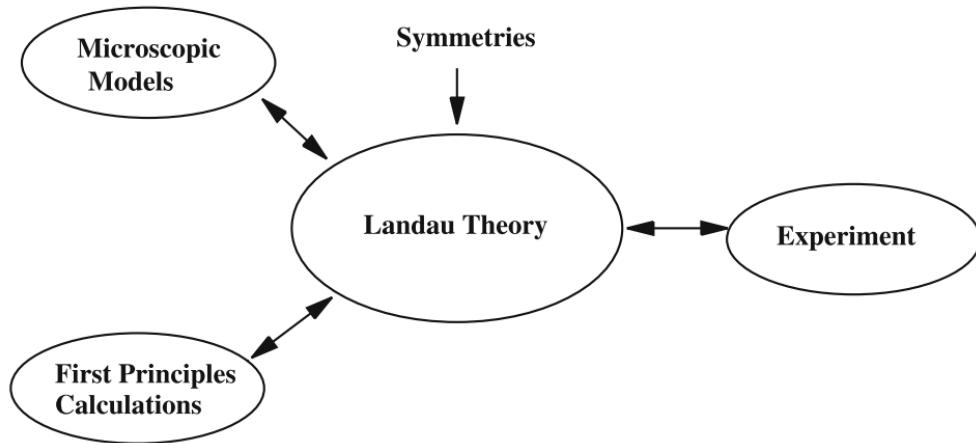


Figure 1.17 – Relationship between the Landau theory and first-principles calculations, microscopic models, and experiment in the vicinity of a phase transition [45].

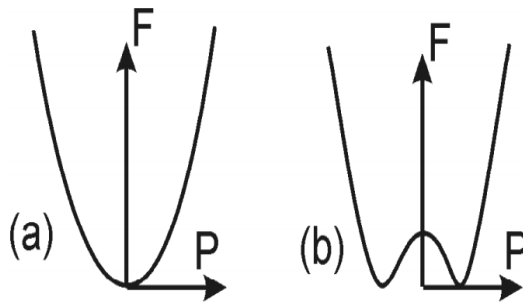


Figure 1.18 – Free energy as a function of polarization in case of a paraelectric (a) and a ferroelectric material (b) [37].

uniaxial ferroelectric. Therefore, the free energy can be written as [47]

$$G = \frac{1}{2}aP^2 + \frac{1}{4}bP^4 + \frac{1}{6}cP^6 + \dots - EP, \quad (1.9)$$

where we have dropped the vector signs as we have assumed one-dimensional spatial variation. In equation 1.9, E denotes to the electric field and a , b , and c are the material dependent parameters. The minima of the free energy defines the equilibrium condition, where we shall have

$$\frac{\partial G}{\partial P} = 0. \quad (1.10)$$

If the material coefficients of a , b , c , etc. are positive, the free energy performs a

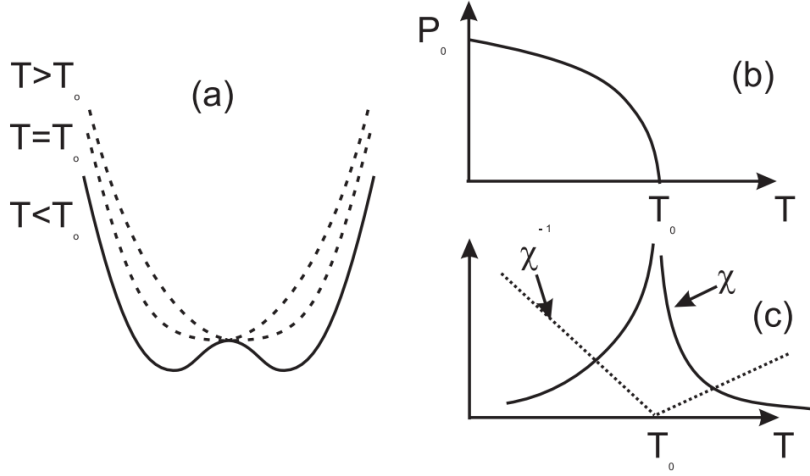


Figure 1.19 – (a) Free energy as a function of the polarization at $T > T_0$, $T = T_0$, and $T < T_0$. (b) Spontaneous polarization as a function of temperature. (c) Inverses of the susceptibility, χ [37].

minimum at the origin. In this case, equation 1.10 can be simplified as

$$\frac{\partial G}{\partial P} = aP - E = 0. \quad (1.11)$$

Equation 1.11 shows a linear relationship between the polarization and the electric field ($\chi = P/E = 1/a$), which is actually the dielectric susceptibility of a paraelectric material.

On the other hand, if a gets negative values, the free energy will look like Figure 1.18-b. In this case, the material is ferroelectric as it has a spontaneous polarization at its ground state. The behavior of ferroelectric materials suggests that a should be a temperature dependent parameter that changes sign at a specific temperature (T_0). Thereby, a simple description of ferroelectrics can be obtained by a linear approximation of $a = a' \times (T - T_0)$. This approximation will predict the demonstrated free energy, polarization, and susceptibility in Figure 1.19. Therefore, a ferroelectric material is traditionally modeled using a double well energy landscape. In equilibrium the ferroelectric resides in one of the wells, providing spontaneous polarization.

The capacitance of a ferroelectric material can be determined by

$$C_{FE} = \left[\frac{d^2 U_{FE}}{dQ_{FE}^2} \right]^{-1}, \quad (1.12)$$

while $Q_{FE} \propto P_{FE}$ and U_{FE} is the energy of the capacitor. Considering the curvature of the E_{FE} vs. P_{FE} of a ferroelectric near the noted wells (Figure 1.18-b), the capacitance of

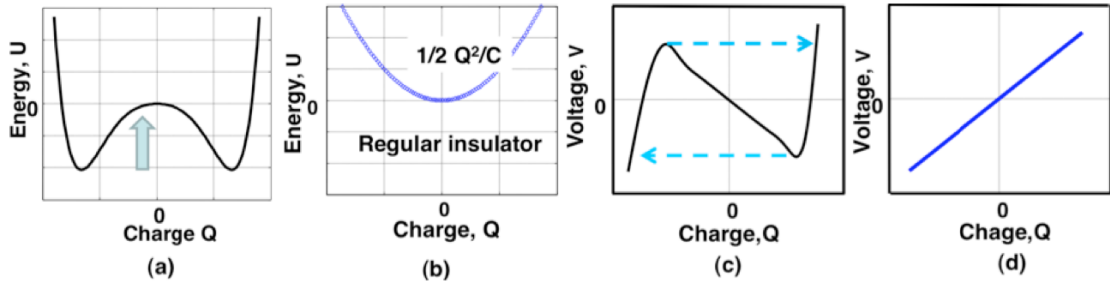


Figure 1.20 – Energy landscape and dU/dQ vs. Q plots of a ferroelectric and a linear dielectric [49].

a ferroelectric capacitor is positive in its equilibrium states. Nevertheless, this curvature is negative around the origin ($Q_{FE} = 0$) while the material is switching from one stable polarization state to the other one.

The negative capacitance has been proven elusive for ferroelectrics in isolation and cannot be observed in experiments, exhibiting hysteretic jumps in the polarization. However, it is evidenced that this negative segment can be stabilized if it is placed in series with a positive capacitor of the proper value. It should be remarked that NC refers to the "negative differential capacitance" due to the small signal concept of the capacitance and relationship between C_{FE} and U_{FE} (equation 1.12).

1.5 Negative Capacitance MOSFETs

It has been proposed that if the conventional insulator of a MOSFET transistor replaced with a stack includes a ferroelectric capacitor, it should be possible to obtain values of m-factor below 1 (Figure 1.14). A negative capacitor integrated into the gate stack of the transistor leads to a subthreshold swing below the thermal limit of MOSFETs. This can be further explained by considering equation 1.4 and taking into account that a ferroelectric can provide an effective negative capacitance. The main advantage of using NC to achieve a sub-60 mV/decade swing is that it does not change the operation principle of the MOS transistor and can be applied in parallel with any other performance boosters of CMOS technology [48].

The relation between the polarization (charge) and electric field (voltage) in a ferroelectric capacitor can be derived by the simplified form of the Landau's theory [48]:

$$E_{FE} = a'(T - T_0)P + b(T)P^3 + c(T)P^5. \quad (1.13)$$

Therefore, as demonstrated in Figure 1.20, the energy landscape and the dU/dQ vs. Q curve of a ferroelectric capacitor explains that how a ferroelectric material can provide

an effective NC near the origin.

It was previously noted that the negative slope part of the polarization is unstable and cannot be separately measured. This NC segment can be stabilized if a positive capacitor attached in series with the ferroelectric, making the total capacitance of the structure positive. If we replace the conventional insulator of a MOSFET with a ferroelectric one (or a stack that consists of a ferroelectric and a linear dielectric), the NC can be stabilized by the semiconductor capacitance (or the series of the semiconductor and linear dielectric capacitances). Indeed the negative permittivity of ferroelectrics can provide a signal amplification which can be understood in terms of a positive feedback mechanism. A non-linear capacitor can be modeled using the following equation [49]:

$$Q=C_0(V+\alpha Q). \quad (1.14)$$

In equation 1.14, the charge of the capacitor (C_0) is a function of the applied voltage (V) plus a voltage feedback of αQ . Therefore, the capacitance of the ferroelectric insulator can be written as

$$C_{ins}=C_0/(1-\alpha C_0). \quad (1.15)$$

In the case of negative capacitance, αC_0 is greater than one, which leads to instability until the non-linear term limits the charge.

In case of the proposed structure of the NC transistor in Figure 1.14, the negative capacitance part of ferroelectric can be stabilized by the semiconductor capacitance, C_s , and hence, the body factor can be defined as

$$\frac{\partial V_g}{\partial \psi_s}=1+\frac{C_s}{C_{ins}}=1-\frac{C_s}{C_0}(\alpha C_0-1). \quad (1.16)$$

Equation 1.16 demonstrates that the NC of ferroelectrics can be used as a step-up voltage transformer that amplifies the applied gate voltage and lowers the body factor below 1. The NC-FET can provide an SS better than the 60 mV/decade thermal limit of conventional transistors, however, it presents some serious technological problems such as the large hysteresis (which comes from the hysteretic behavior of ferroelectrics) and the need of a ferroelectric capacitor with a CMOS compatible fabrication process [50].

1.6 Ferroelectric materials comparison

Ferroelectric materials can exist in various compositions and forms. Ceramics are considered as one of the first discovered ferroelectrics can be processed, shaped, and

1.6. Ferroelectric materials comparison

manipulated. With the high demand of device miniaturization, the interest in thin film ferroelectrics grew fast. Ferroelectric thin films offer various materials and deposition techniques, much easier than of ceramics. In this regard, many ferroelectric materials and deposition methods are studied in order to open a path to adoption of ferroelectric materials in the electronics industry.

Ferroelectricity was discovered in different materials such as liquid crystals and polymers. In case of liquid crystals, a unit cell consists of atoms and ions that are stacked in the crystal lattice of a ferroelectric oxide [51]. A ferroelectric polymer works quite different; in this case, the unit cell is made of macromolecules that are arranged in a lower symmetry [52]. As a result of this complexity, ferroelectricity in polymers was discovered decades after one of the ionic structures.

One of the most studied and industrialized types of ferroelectrics are perovskites. This class of materials has a pseudo-cubic structure with a chemical formulation of ABO_3 . Most of the electronic devices utilizing ferroelectric thin films, such as ferroelectric random access memories (FeRAM), have been based on perovskite structured materials, like $Pb(Zr,Ti)O_3$ (PZT), $BaTiO_3$ (BTO), and $SrBi_2Ta_2O_9$ (SBT). Lead Zirconate Titanate (PZT) is the most known perovskite due to its extensive applications in the memory industry. PZT has extraordinary ferroelectric properties such as high spontaneous polarization, low leakage, and high retention time. However, a proper CMOS compatible fabrication process of PZT (or any other perovskites) is still missing. Although some of the conventional ferroelectrics such as BTO can be epitaxially grown on a silicon substrate by carefully optimizing the fabrication process, the quality of the interface between the ferroelectric layer and the silicon substrate is inappropriate in most cases. Another important challenge involves in the fabrication of PZT, relates to its scalability which obstructed the scaling of PZT-based memories below the 130 nm technology node [43].

The recent discovery of ferroelectricity in doped high-k oxides, such as HfO_2 , has created a new path for the CMOS compatible manufacturing of ferroelectric devices.

Generally, high-quality epitaxial ferroelectrics are considered suitable for negative capacitance devices as they are more likely to form a mono-domain state characterized by a single coercive field. However, deposition of single crystalline ferroelectrics is extremely challenging which makes polycrystalline ferroelectrics more favorable. In the following, we will discuss PZT, as a well-known ferroelectric, and silicon-doped HfO_2 , as the recently proposed CMOS compatible ferroelectric, that are the exploited ferroelectric materials to perform NC effect in this thesis.

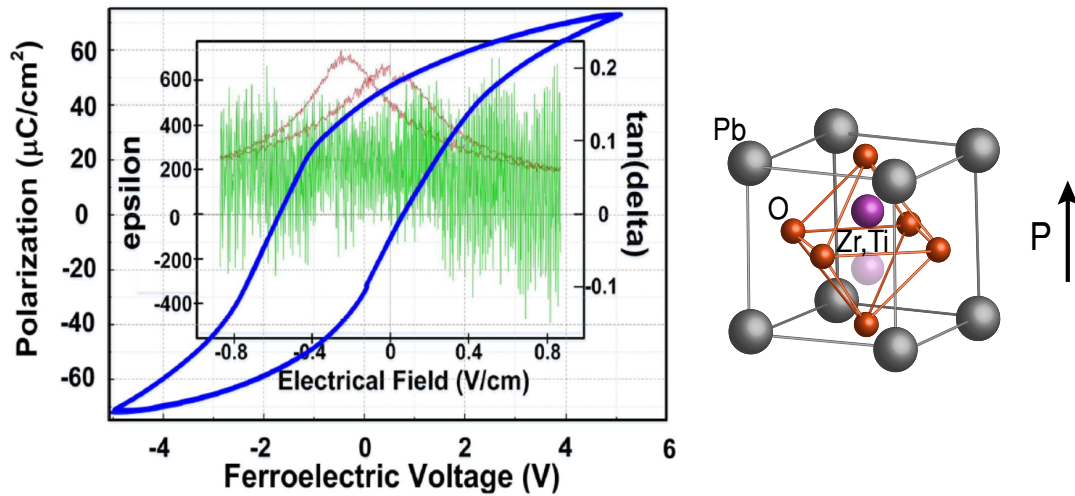


Figure 1.21 – Electrical characterization of a typical polycrystalline PZT thin film with a thickness of 50 nm (left) along with its crystal structure (right) [55].

1.6.1 Lead Zirconate Titanate (PZT)

Lead Zirconate Titanate ($\text{Pb}[\text{Zr}_x\text{Ti}_{1-x}]\text{O}_3$; $0 < x < 1$) is a ceramic perovskite material that shows a marked piezoelectric effect. PZT was developed by Y. Takagi, G. Shirane, and E. Sawaguchi around 1952 in Tokyo Institute of Technology [53]. This type of ferroelectrics is composed of Lead, Zirconium, and Titanate that are combined under high-temperature conditions [54].

PZT first became famous thanks to its outstanding piezoelectric properties. Piezoelectricity is an ability in which the material changes its physical shape under a sufficiently high electric field. Additionally, PZT attracted a great deal of attention due to its high electromechanical coupling coefficient, k , and a high relative dielectric constant, ϵ_r . Thereby, PZT has become an interesting material because of its wide applications such as piezoelectric vibrators, Surface Acoustic Wave (SAW) devices, pyroelectric detectors, and nonvolatile random access memories.

PZT is also a ferroelectric, having a relatively high spontaneous polarization that can change the direction in presence of an externally applied electric field. The crystal structure of PZT regarding the two stable polarization states together with a polarization characteristic of a typical PZT is presented in Figure 1.21. The main drawback of PZT, despite the various available deposition techniques, is the absence of a CMOS compatible fabrication process. Moreover, the high diffusibility of lead atoms makes it extremely challenging to integrate this type of ferroelectrics into the gate stack of transistors. This would be only possible by using a barrier to confine lead atoms [56].

1.6. Ferroelectric materials comparison

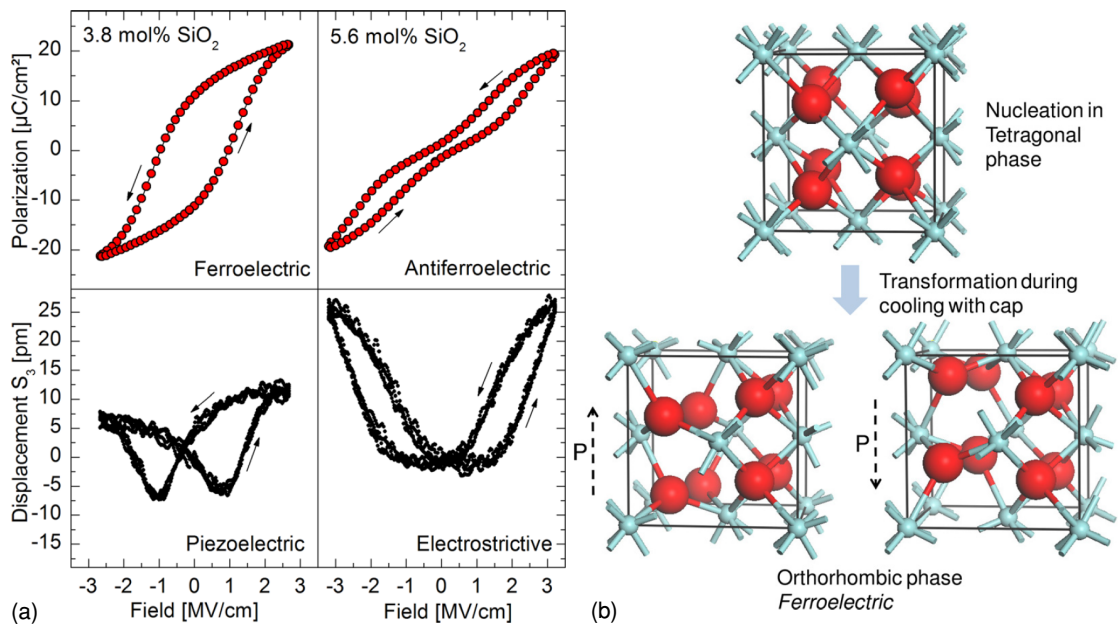


Figure 1.22 – (a) Polarization (top row) and piezoelectric displacement (bottom row) measurement of a TiN/Si:HfO₂/TiN capacitor sample with ferroelectric (left column) and anti-ferroelectric (right column) composition. (b) The formation of the orthorhombic III phase proceeds by transformation from the tetragonal phase during cooling with a TiN capping layer. The bottom row indicates two different polarization states [57].

1.6.2 Silicon-doped HfO₂

Most of the ferroelectric devices utilizing ferroelectric thin films, such as random access memories (FeRAMs), have been based on perovskites such as PZT and BTO. This type of materials is called conventional ferroelectrics because of the recently discovered ferroelectricity in doped high- k materials such as doped HfO₂. However, there is an epitaxial deposition method available for some of the conventional ferroelectrics which in most cases leads to an inappropriate interface. Generally, an interfacial native oxide (SiO₂) is formed that weakens the stability of the polarization states [58].

In contrary to conventional ferroelectrics, the recently proposed HfO₂-based thin films offer a fully CMOS compatible fabrication process. Moreover, HfO₂ has been utilized as the gate stack of conventional transistors for many years and its related challenges have been already extensively investigated and addressed [59].

HfO₂ is an electrical insulator with an energy gap around 5.3-5.7 eV and a relative permittivity of 17 in its mono-domain structure, the most stable form of HfO₂.

The ferroelectricity in HfO₂-based films was first discovered in 2007 by Boske et al. One of the first reports regarding the ferroelectricity in HfO₂ thin films is depicted in Figure 1.22, where the polarization characteristic and piezoelectric response of the

ferroelectric and anti-ferroelectric silicon-doped HfO₂ thin films with a thickness of 10 nm are demonstrated. The silicon-doped HfO₂ with a Si% of 2.6-4.3% showed a feasible ferroelectricity. A silicon concentration above 4.3% leads to the anti-ferroelectric behavior while a sufficiently higher Si% results in a characteristic close to a linear dielectric (Si% > 8.5%).

The unit cell structure of the ferroelectric form of HfO₂ when crystallized in the orthorhombic phase is presented in Figure 1.22-b. The ferroelectric properties of doped HfO₂ have been reported for various dopants such as Si [60, 61, 62], Zr [63, 57], Y [64, 65], Al [66], Gd [67], Sr [68], and La [58].

1.7 Thesis overview

This Ph.D. work highlights and validates the potentials of ferroelectric field-effect transistors for both steep slope and memory applications. First, in Chapter 2, the physics behind negative capacitance FETs is investigated and discussed the following two main topics: (i) the condition for negative capacitance to occur in a ferroelectric transistor and, (ii) design of an NC-FET in order to optimize the boosting effect of as well as the hysteretic behavior. The condition for NC to occur is developed based on Landau's theory of ferroelectrics combined with the surface potential model of MOSFETs. It is later validated by the previously reported experimental results by our group. Additionally, a matching condition is proposed between the ferroelectric NC and the gate intrinsic capacitance of the baseline transistor to optimize the hysteresis and the amplification due to the negative capacitance effect. The condition is then confirmed with experimentally calibrated simulations using Silvaco TCAD coupled with a realistic Landau model of ferroelectric materials. This chapter is written based on the following publications:

1) *Rusu, A., Saeidi, A., and Ionescu, A. M. (2016). Condition for the negative capacitance effect in metal-ferroelectric-insulator-semiconductor devices. Nanotechnology, 27(11), 115201.*

2) *Saeidi, A., et al. (2016). Double-gate negative-capacitance MOSFET With PZT gate-stack on ultra thin body SOI: an experimentally calibrated simulation study of device performance. IEEE Transactions on Electron Devices, 63(12), 4678-4684.*

Chapter 3 summarizes the experimental results obtained on n- and p-type NC-FETs, showing a significant enhancement in both digital and analog performances of MOSFETs. The hysteretic behavior of NC-FETs is tuned based on the proposed condition of the previous chapter. For the first time, a hysteresis-free NC-FET is successfully demonstrated. The potentials of the silicon-doped HfO₂ ferroelectric thin film as the NC booster is also shown and discussed, showing that further engineering is required to reduce the leakage current Si:HfO₂. The contents of this chapter can be found in the

following publications:

1) Saeidi, A., et al. (2017, September). *Negative capacitance field effect transistors; capacitance matching and non-hysteretic operation*. In *Solid-State Device Research Conference (ESSDERC), 2017 47th European* (pp. 78-81). IEEE.

2) Saeidi, A., et al. (2017). *Negative capacitance as performance booster for tunnel FETs and MOSFETs: an experimental study*. *IEEE Electron Device Lett*, 38(10), 1485-1488.

3) Saeidi, A., et al. *Design Considerations of Ferroelectric Properties for Negative Capacitance MOSFETs*. In *2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)* (pp. 10-12). IEEE.

4) Saeidi, A., et al. *Negative Capacitance as Digital and Analog Performance Booster for Complementary MOS Transistors*. *Nature Scientific reports*, under revision.

Chapter 4 suggests that the NC effect can be effectively utilized to significantly improve the digital and analog performances of tunneling field-effect transistors. Hysteretic and non-hysteretic NC-TFETs with a super steep *off-to-on* transition are experimentally demonstrated. The basis of this chapter is the following articles:

1) Saeidi, A., et al. (2017, June). *Negative Capacitance Tunnel FETs: Experimental Demonstration of Outstanding Simultaneous Boosting of On-current, Transconductance, Overdrive, and Swing*. In *Silicon Nanoelectronic Workshop (No. EPFL-CONF-231864)*.

2) Saeidi, A., et al. (2018). *Effect of hysteretic and non-hysteretic negative capacitance on tunnel FETs DC performance*. *Nanotechnology*, 29(9), 095202.

3) Saeidi, A., et al. (2018). *Near Hysteresis-Free Negative Capacitance InGaAs Tunnel FETs with Enhanced Digital and Analog Figures of Merit below $V_{DD}=400$ mV*. to be presented at *International Electron Device Meeting (IEDM 2018)*.

4) Saeidi, A., et al. (2018). *Negative Capacitance Tunneling Field Effect Transistors as Energy Efficient Electronic Switches*. *Nature Electronic*, under revision.

Chapter 5 proposes that ferroelectric TFETs using the Si:HfO₂ can be a potential candidate for the future of low power energy efficient 1T memories, even in highly scaled dimensions. The operation principles of FeTFETs is theoretically studied. The reported results confirm that a FeTFET can operate as an ultra-low power nonvolatile memory in aggressively scaled dimensions. This chapter is based on the following manuscript:

1) Saeidi, A., Biswas, A., and Ionescu, A. M. (2016). *Modeling and simulation of low power ferroelectric non-volatile memory tunnel field effect transistors using silicon-doped hafnium oxide as gate dielectric*. *Solid-State Electronics*, 124, 16-23.

1.8 Summary

In this chapter, the evolution of CMOS technology and the power challenge regarding the aggressive scaling of the transistor's dimensions were described. It was explained that this increased power consumption issue arises from the physical limitation of MOSFETs. This is due to the fact that a minimum voltage of 60 mV is required for a 10-fold increase in the drain current.

Small swing switches were presented as the device level solution of the increasing power challenge. In this regard, different types of steep slope switch candidates such as TFETs, suspended gate MOSFETs, impact ionization FETs, and negative capacitance MOSFETs were demonstrated. The operation principle of NC-FETs, as the main research topic of this thesis, were explained using the Landau's theory of ferroelectrics. Lastly, different ferroelectric materials were compared and their potentials for the integration with the CMOS technology was discussed.

The main motivation of this work is to obtain reliable negative capacitance transistors with a steeper *off-to-on* transition than conventional MOSFETs. A negative capacitance transistor offers major advantages comparing other steep slope switch candidates: a higher *on-current* than TFETs, a more reliable operation than I-MOSFETs, and a much simpler fabrication and packaging process than SG-FETs.

One of the main challenges of negative capacitance transistors is the large hysteresis, which is the signature of ferroelectric materials. We have theoretically proposed and experimentally validated in this Ph.D. work that the hysteretic behavior of an NC-FET can be removed or alleviated in a well-designed device configuration. We have also suggested that the NC effect can be efficiently utilized as the most important performance booster of TFETs. Lastly, in this work, a ferroelectric TFET using Si:HfO₂ is proposed as a scalable and energy efficient 1T nonvolatile memory.

2 Theory of Negative Capacitance Transistors

Abstract:

The main goal of this chapter is to investigate the physic of negative capacitance transistors. In this regard, there are two main topics that should be addressed: (a) The condition for the NC effect to occur in a ferroelectric transistor and then, (b) optimizing the boosting effect of NC as well as its hysteretic behavior that comes from the nature of ferroelectric materials. First, we present the condition for the negative capacitance to occur. The condition is developed based on Landau's theory of ferroelectrics which is combined with the surface potential model of MOSFETs. The validity of the proposed theory is confirmed on previously reported experimental NC-FETs of our group, using a gate stack that is made of P(VDF-TrFE) and SiO₂. The proposed analytical modeling shows good agreement with the experimental data. Then, we propose a condition to ensure the maximum boosting effect in the non-hysteretic operation of an NC transistor. In this regard, we investigated the high performance and low power design space of non-hysteretic negative capacitance MOSFETs for the 14 nm CMOS technology node. Results are achieved based on the calibrated simulations using an experimental gate stack with PZT ferroelectric to demonstrate the NC effect. The proposed approach leads to a ferroelectric thickness that ensures the maximum enhancement in the non-hysteretic operation of an NC-FET. We report a clear and significant double improvement in (i) subthreshold swing and (ii) gate overdrive, using the negative capacitance of ferroelectrics. Silvaco TCAD commercial simulator coupled with a realistic Landau model of ferroelectrics demonstrates that a 14 nm node UTBB FDSOI-FET can operate at 0.26 V instead of 0.9 V gate voltage using an NC booster.

2.1 Condition to obtain Negative Capacitance in FeFETs

It has been suggested by Salahuddin (2008) that the ferroelectric transistor could provide a new mechanism to amplify the surface potential above the gate voltage due to the negative capacitance effect [18, 69]. Several experiments showed proof of the NC in ferroelectric materials [70, 71]. Recent theoretical studies propose that a non-hysteretic behavior of negative capacitance FET with a subthreshold slope less than 30 mV/decade, but the device is only in the simulation state [72].

Recently, there were reported ferroelectric transistors with under-thermionic characteristics that presented [73] both hysteretic and non-hysteretic negative capacitance behavior [35, 74, 75]. However, there was a slight difference between the reported devices and the Salahuddin's first proposal [18], the insertion of a linear dielectric as the buffer layer to suppress the diffusion of the ferroelectric into the silicon and also to provide a proper interface [76]. The ferroelectric stability condition to obtain the negative capacitance effect was still missing despite the countless number of publications on this topic.

In this chapter, first, we describe the physical explanation of the stability condition, setting its boundaries based on the electrical and physical properties of the materials. The condition is obtained based on the basic Maxwell [77] charge equation and Tsividis model of the MOS transistor [78]. The stated stability condition is then validated with measurements on fabricated devices that shows voltage amplification and hysteresis at the same time. Based on the presented theory, a complete set of equations is reported for the successful design of a negative capacitance transistor.

2.1.1 Theory

In this section, we demonstrate the analytical modeling of the Metal-Ferroelectric-Oxide-Silicon (MFIS) field-effect transistor. It is then employed to derive a theoretical condition for the negative capacitance to occur in a FeFET. Figure 2.1 shows the schematic diagram of a FeFET, where the conventional gate dielectric of a MOSFET is replaced by a stack of a linear and a ferroelectric dielectric. Each layer can be defined as a single capacitor so that the entire gate stack can be considered as an in-series combination of capacitors (Figure 2.1). This is possible because of the presence of the intermediate metal layer between the two dielectrics.

The ferroelectric layer has been considered ideal, and the formation of the dead layer at the interface with the electrode is neglected in our calculations [79]. Forming the dead layer has a drastic effect on the dielectric response of a ferroelectric capacitor. The presence of the dead layer triggers the formation of a domain structure in ferroelectric films, so the dielectric response of the ferroelectric layer is going to be different with what

2.1. Condition to obtain Negative Capacitance in FeFETs

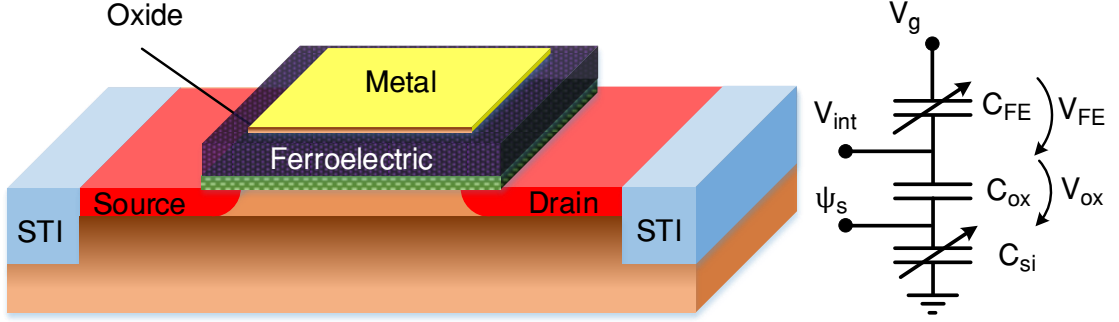


Figure 2.1 – (left) Generic ferroelectric transistor; (right) equivalent capacitance model of the structure. It should be remarked that the ferroelectric and MOS capacitances are bias-dependent.

is stated by the capacitor model. With respect to the equivalent circuit of Figure 2.1,

$$V_g = V_{FE} + V_{ox} + \psi_s, \quad (2.1)$$

where V_g is the gate voltage, V_{FE} and V_{ox} are the voltage drop over ferroelectric and linear dielectrics and ψ_s is the silicon surface potential. We will consider the case that there are no trapped charges on the SiO_2 -PVDF interface [80]. Thus, the electric displacement is conserved [81], which can be expressed as:

$$\begin{aligned} D_{FE} &= D_{ox}, \\ \epsilon_0 E_{FE} + P &= \epsilon_0 k_{ox} E_{ox}, \\ P &= \epsilon_0 k_{ox} \frac{V_{ox}}{t_{ox}} - \epsilon_0 \frac{V_{FE}}{t_{FE}}, \end{aligned} \quad (2.2)$$

where D_{FE} and D_{ox} are the displacements of the ferroelectric and oxide, E_{FE} and E_{ox} are the electric field inside the ferroelectric and oxide thin films, P is the ferroelectric polarization, t_{FE} and t_{ox} are the ferroelectric and oxide thicknesses, k_{ox} is the relative permittivity of the oxide, and ϵ_0 is the vacuum permittivity. By substituting the voltage drop across the linear oxide from equation 2.1, the ferroelectric polarization can be calculated as follows:

$$P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} - E_{FE} t_{FE} \epsilon_0 \left(\frac{1}{t_{FE}} + \frac{k_{ox}}{t_{ox}} \right) - \frac{\epsilon_0 k_{ox}}{t_{ox}} \psi_s. \quad (2.3)$$

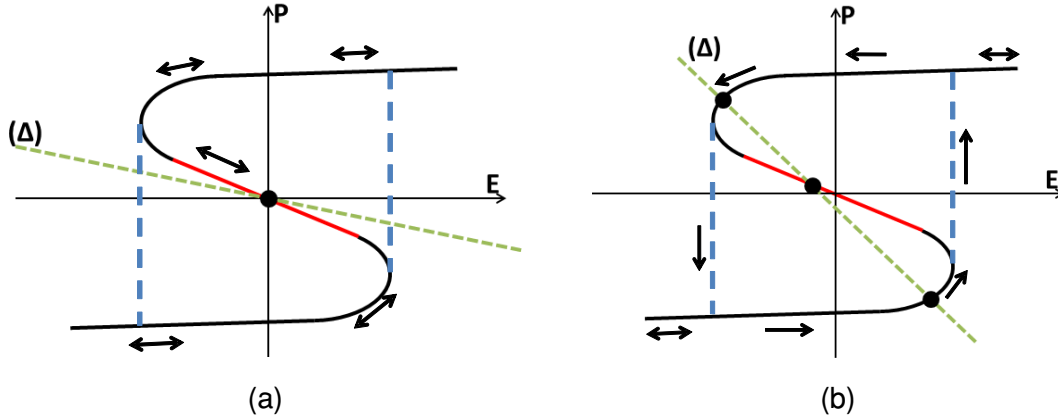


Figure 2.2 – Transistor charge line intersecting the polarization. (a) The condition for the negative capacitance is fulfilled. In (b), the condition for negative capacitance does not appear, and we encounter the hysteresis [78].

Equation 2.3 represents the charge stability of the system in a certain gate voltage. In order for the negative capacitance to occur in a FeFET, the slope of the charge line (defined by equation 2.3) must be smaller than the negative slope of the ferroelectric polarization. This is qualitatively presented in Figure 2.2.

Figure 2.2-a shows a stable system, which the charge line is intersecting the polarization in only one point. This is in contrast to the case of Figure 2.2-b where the charge line is intersecting the polarization curve in 3 points. Therefore, for the stable operation of a negative capacitance device, the slope of the transistor charge line, Δ , must be *smaller* than the negative slope of the ferroelectric polarization when it is operating in the NC region.

In order to calculate the slope of the charge line, the surface potential should be expressed regarding the voltage drop over the ferroelectric capacitor. Due to the fact that the surface potential cannot be expressed mainly by a unique compact analytical expression in all regions of operation, we have studied the MOS transistor in different regions. We start with strong inversion, the surface potential in strong inversion has an almost constant value of $\psi_s \sim 2\phi_F + 6\phi_t$, where ϕ_F is the Fermi potential and ϕ_t is the thermal voltage. By considering the equation 2.3, the charge line of the transistor in the strong inversion regime can be stated as

$$\Delta = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} - E_{FET} t_{FE} \epsilon_0 \left(\frac{1}{t_{FE}} + \frac{k_{ox}}{t_{ox}} \right) - \frac{\epsilon_0 k_{ox}}{t_{ox}} (2\phi_F + 6\phi_t). \quad (2.4)$$

The slope of the charge line at a gate voltage that sets the transistor in the strong

2.1. Condition to obtain Negative Capacitance in FeFETs

inversion will be

$$\frac{\partial \Delta}{\partial E_{FE}} = -t_{FE} \epsilon_0 \left(\frac{1}{t_{FE}} + \frac{k_{ox}}{t_{ox}} \right). \quad (2.5)$$

In the weak inversion regime, the surface potential can be approximated by a linear function [81]. Therefore, the slope of the surface potential can be addressed as

$$n = \left(\frac{d\psi_s}{dV_g} \right)^{-1} = 1 + \frac{\gamma}{2\sqrt{\psi_s}}, \quad (2.6)$$

where γ is the body factor.

The surface potential varies from ϕ_F to $2\phi_F$ in the weak inversion region. Therefore, the n does not vary a lot, and we can approximate it by an average surface potential value. Thus, we will have an average slope at $\psi_s = (3/2)\phi_F$,

$$n = 1 + \frac{\gamma}{2\sqrt{(3/2)\phi_F}}. \quad (2.7)$$

The surface potential has a linear dependence on the gate voltage by considering the noted approximation. Coming back to equation 2.3,

$$P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} - \epsilon_0 V_{FE} \left(\frac{1}{t_{FE}} + \frac{k_{ox}}{t_{ox}} \right) - \frac{\epsilon_0 k_{ox}}{t_{ox}} \times \frac{V_{int}}{n}, \quad (2.8)$$

$$P = \epsilon_0 k_{ox} \frac{V_g}{t_{ox}} + \frac{\epsilon_0 k_{ox}}{nt_{ox}} V_g - E_{FE} t_{FE} \epsilon_0 \left(\frac{1}{t_{FE}} + \frac{k_{ox}}{t_{ox}} \left(1 - \frac{1}{n} \right) \right). \quad (2.9)$$

The last equation describes the charge line of an NC-FET that is biased in the weak inversion regime. The slope of the charge line can be expressed as

$$\frac{\partial \Delta}{\partial E_{FE}} = -\epsilon_0 t_{FE} \left(\frac{1}{t_{FE}} + \frac{k_{ox}}{t_{ox}} \left(1 - \frac{1}{n} \right) \right). \quad (2.10)$$

The slope of the transistor charge line is not constant regarding the gate voltage. This means the charge line is getting influenced by the slope of the surface potential. The slope of the charge line decreases by increasing the $1/n$ parameter, implying that having a steep slope transistor is an advantage in achieving the NC effect in a FeFET. The $1/n$ parameter depends on the fabrication criterions and physical parameters of the transistor.

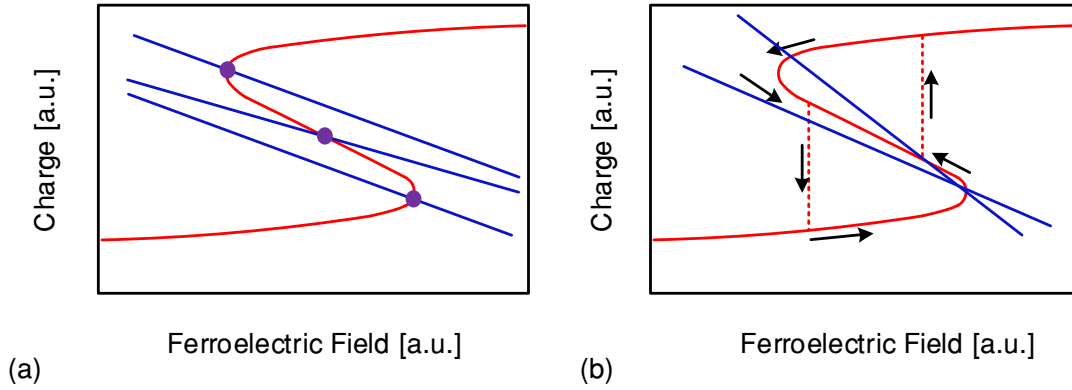


Figure 2.3 – Transistor charge line that changes the slope regarding the operation regime of the ferroelectric transistor. (a) The slope of the charge line changes with the bias but the stability condition remains fulfilled at the entire range of the applied voltage. (b) The condition for the stability is fulfilled only on a small interval of applied voltage so that negative capacitance can be obtained together with hysteresis.

The surface potential of the transistor in the depletion mode cannot be approximated by a linear function and the charge line become a second-degree equation. Again, the important factor is the slope of the parabola. The slope of the charge line, which depends on the gate voltage, must be continuous and monotone to fulfill the continuity. Thus, we can state that the charge line slope is high in the depletion region, lowers gradually in weak inversion, and increasing again in the inversion region.

As it is previously demonstrated, the slope of the charge line must be *smaller* than the negative slope of the polarization to have a successful NC-FET.

Next, we will pass to the calculation of the negative part of the ferroelectric S-shape polarization. The S-shape hysteresis is defined according to the Landau's theory [82]:

$$E = \alpha_0(T - T_c)P + B(T)P^3, \quad (2.11)$$

where α_0 and $B(T)$ are material dependent parameters, T_c is the ferroelectric Curie temperature and T is the temperature. For simplicity, the first order approximation is considered for the calculation of the negative slope of the polarization. We have used the first order approximation in the region where the slope of the polarization is negative. The first order approximation is valid mathematically as the polarization has the value near zero in the negative capacitance region that makes us eligible to neglect the third order term in comparison with the first order term. Besides that, based on our experimental results which are depicted later in this thesis, the P-E diagram clearly has a linear behavior in the negative capacitance region that validates our theoretical

2.1. Condition to obtain Negative Capacitance in FeFETs

approximation. Therefore,

$$E = \alpha_0(T - T_c)P. \quad (2.12)$$

Hence, the derivation of the ferroelectric polarization in the negative region is:

$$\frac{\partial P}{\partial E} = \frac{1}{\alpha_0(T - T_c)}. \quad (2.13)$$

Based on the equations listed above, we can theoretically state that the negative capacitance appears only in the weak inversion where the slope of the charge line is minimum. Therefore, we are reporting the mathematical condition to obtain the NC effect in FeFETs as follows;

$$\frac{\partial \Delta}{\partial E_{FE}} \leq \frac{\partial P}{\partial E}, \quad (2.14)$$

$$-\epsilon_0 \left(\frac{1}{t_{FE}} + \frac{k_{ox}}{t_{ox}} \left(1 - \frac{1}{n} \right) \right) \leq \frac{1}{\alpha_0(T - T_c)}, \quad (2.15)$$

where $\gamma = \sqrt{2q\epsilon_s N_A} / (\epsilon_{ox}/t_{ox})$, $\phi_F = \phi_t \ln N_A/n_i$, and n is presented in equation 2.7. With this algorithm, we have given a complete set of equations, to design a negative capacitance ferroelectric MOS transistor. The following parameters (t_{ox} , t_{FE} , N_A , α_0 , T_c , and ϵ_{ox}) should be considered for a successful design.

The slope of the charge line in an NC-FET depends on the gate voltage. As a result, in the case that the slope of the charge line and the negative slope of the ferroelectric polarization are close, the stability of the system is not consistent for all gate voltages. This is due to the fact that once the slope of the charge line attains the ferroelectric polarization slope, the system reaches equilibrium and the NC effect appears. Increasing further the gate voltage leads the system to instability as the slope of the charge line exceeds the slope of the ferroelectric polarization. The variation of this slope and the possibility to obtain hysteresis and negative capacitance effect is qualitatively demonstrated in Figure 2.3. It also validates that devices with a larger surface potential derivative (subthreshold slope closer to 60 mV/decade), have a larger zone (better chance) that the negative capacitance can be observed.

The obtained gain of the FeFET can be also calculated based on the negative slope of the polarization (dP/dE_{FE}) and the subthreshold slope of the series MOS transistor under the ferroelectric layer (considering the FeFET as a ferroelectric capacitor in series with a conventional MOSFET) [83]. The amplification effect of negative capacitance basically

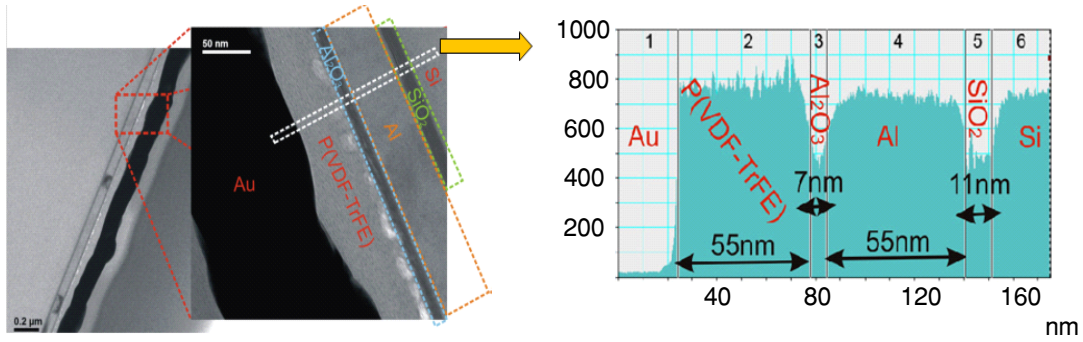


Figure 2.4 – TEM analysis of the device gate stack. The thickness of each layer is depicted in the right image.

depends on the α_0 parameter of the ferroelectric, meaning that a high amplification corresponds to a low α_0 .

In addition to the amplification, the negative capacitance stability also depends on this parameter, higher α_0 corresponds to a wider zone of negative capacitance. The condition of the stability highly depends on the ferroelectric properties and the electrical characteristic of the corresponding MOS transistor. This could be the main reason that many trials for measuring negative capacitance had failed [84].

2.1.2 Experimental verification

We have verified the stated condition using previously reported NC-FETs from our group [74]. The gate stack is composed of P(VDF-TrFE)70:30 and a thin layer of SiO₂. Between these two insulators, a layer of Al was introduced to provide access to the internal contact. A thin layer of Al₂O₃ was formed during Al deposition. The TEM image of the gate cross section is demonstrated in Figure 2.4.

Figure 2.5 presents the polarization curve and its derivative with respect to the electrical field across the ferroelectric layer. The Al₂O₃ layer was taken into consideration for the polarization extraction. The polarization-voltage hysteresis in Figure 2.5 is slightly different compared to other experimental results reported in the literature [85]. Usually, the P-E diagram of a ferroelectric capacitor is symmetric while the polarization hysteresis loop of a FeFET has an S-like behavior only in one branch of the hysteresis [86]. This is actually due to the fact that the condition for NC effect to occur is fulfilled only in the positive going branch of the transistor. Figure 2.5 shows the region where the negative capacitance condition is fulfilled.

Next, the slope of the PVDF S-shape polarization will be calculated. The $\alpha_0 = 9.02 \times 10^9$ J.m/cm.V.K [87] and the $T_c = 355^\circ$ K [88]. Calculating the negative slope of

2.1. Condition to obtain Negative Capacitance in FeFETs

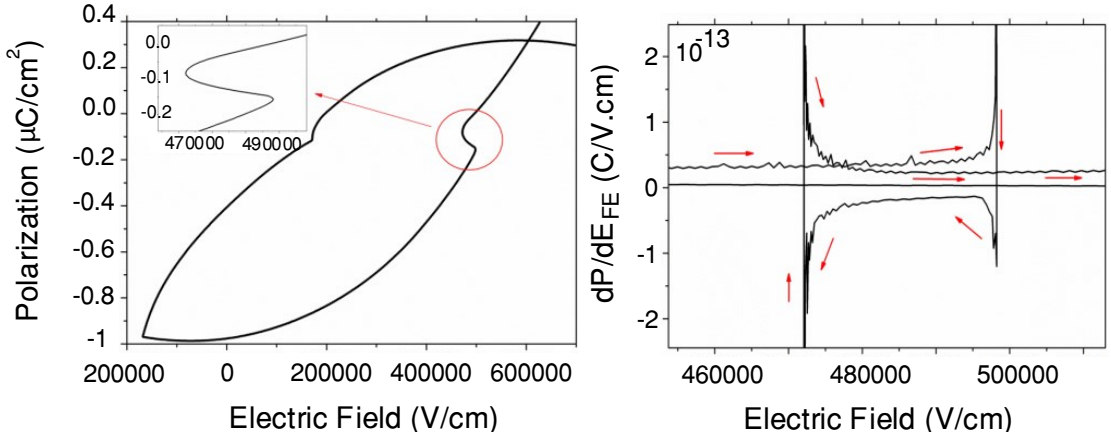


Figure 2.5 – Ferroelectric polarization that is extracted from measurements (left) and the polarization derivative with respect to the ferroelectric field (right).

the polarization for PVDF,

$$\frac{\partial P}{\partial E} = \frac{1}{\alpha_0(T - T_c)} = 2.0157 \times 10^{-14} \frac{C}{cm.V}. \quad (2.16)$$

Figure 2.6 demonstrates the measured charge line slope (continuous line) and the calculated slope of the S-shape polarization (dotted line). The system is stable where the slope of the charge line is smaller than the slope of the polarization. As stated in equation 2.14, the dotted line represents the threshold imposed by the ferroelectric material for the system to achieve the stability.

These results accurately prove our mentioned theory. Even if the threshold of the ferroelectric does not cover all the zone that the NC appears, one can observe that it covers the zone where the system is stable. After this limit, noise starts prevailing and the system exits the stability regime. We have stated that the slope of the charge line is a function of the derivative of the surface potential with respect to the internal voltage. Figure 2.7 shows the surface potential and its derivative which was extracted based on the Tsividis model.

Figure 2.7 shows that the slope of the charge line lowers significantly if the derivative of the surface potential exceeds a certain value. This value is 0.723 in case of our reported experimental results. A better MOS with a subthreshold slope closer to the 60 mV/decade thermal limit has a derivation of the surface potential closer to 1. A surface potential derivative closer to 1 translates to an extended negative capacitance zone, providing amplification over multiple decades of the current.

The ferroelectric material must be polarized at a certain value to have a stable system. Here, we cannot sufficiently polarize the ferroelectric due to the thin oxide that results

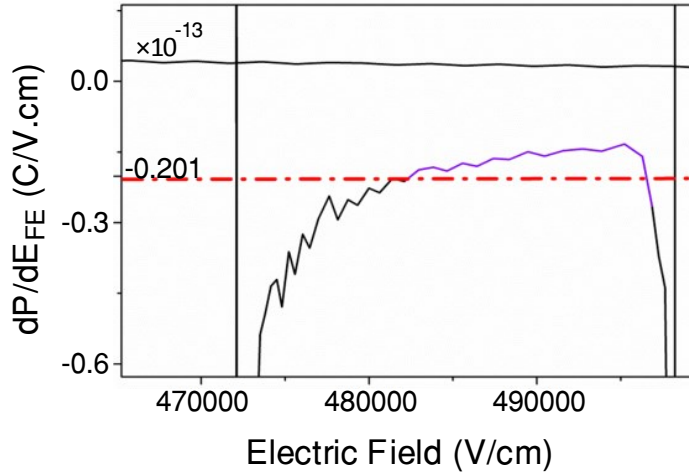


Figure 2.6 – Negative capacitance area where the system reaches stability. This graph illustrates the condition from equation 2.14 applied to the measured device. The continuous line ($\partial P/\partial E$) is the measured value, and the dotted line is the theoretical threshold limit calculated from the literature data, equation 2.16, in order to achieve negative capacitance. We can observe that above this threshold, the measurement starts to go into the instability regime and the ferroelectric pops off the negative capacitance regime.

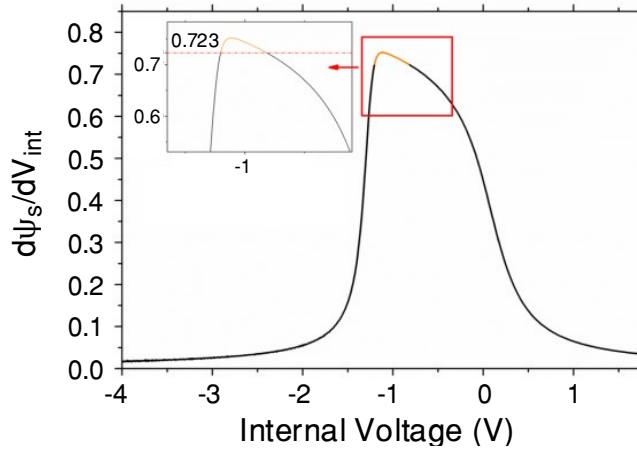


Figure 2.7 – Surface potential derivative with respect to the internal potential. The highlighted zone corresponds to the points where we have obtained the negative capacitance. We can clearly observe that the points that are corresponding to the negative slope of the polarization belong to the area that the derivative of the surface potential has a value higher than 0.723. Better fabricated MOS transistors with a higher derivative of the surface potential with respect to the internal voltage will result in a wider area of negative capacitance effect.

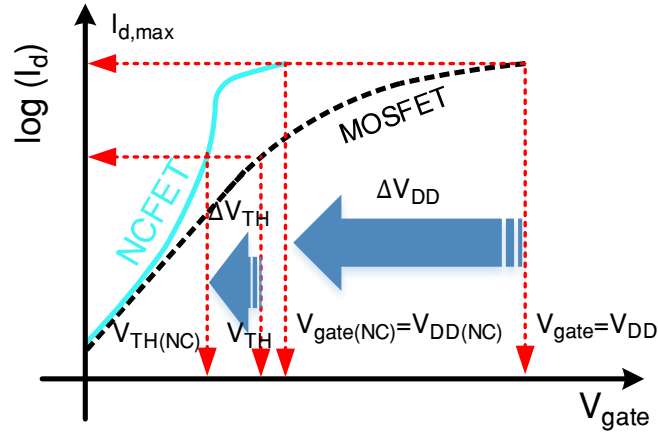


Figure 2.8 – Transfer characteristics of the NC-FET versus MOSFET highlighting the gain in terms of overdrive and reduction of the threshold voltage, V_{TH} and supply voltage, V_{DD} .

in exploring the minor loops of the ferroelectric. An inconvenience of this fact is that the ferroelectric polarization curve can shift between two successive measurements because of the remaining dipoles that are already polarized from the previous measurement. One can observe the asymmetry of the polarization curve toward the negative side and no NC effect is observed in the negative going branch of the transfer characteristic.

2.2 Capacitance matching condition

2.2.1 Theory

A ferroelectric capacitor interconnecting with the gate stack of an MOS transistor creates a series connection between C_{FE} and C_{MOS} . The ferroelectric capacitor can increase the total capacitance of the gate ($C_{total}^{-1} = C_{FE}^{-1} + C_{MOS}^{-1}$) while it is stabilized in the NC region [89, 90]. Specifically, the series structure brings an abrupt increase in the differential charge in the internal node (V_{int}) by changing the gate voltage. This provides a step-up voltage transformer [83]. The internal gain of NC can be defined as $\beta = \partial V_{int} / \partial V_g = C_{FE} / (C_{FE} + C_{MOS})$. Accordingly, an NC booster can provide an internal voltage amplification ($\beta > 1$), which results in a body factor reduction, i.e. $1/\beta$. A body factor smaller than 1 leads to an improvement in both analog and digital performances of the baseline transistor. The advantage of this approach is that the effect is universal for all transistors where the gate stack contributes to the signal amplification and enhances the surface potential (Figure 2.8).

As we have discussed in details in the previous section, in order for NC to occur, the charge line of the baseline transistor is acquired to have an intersection with the negative slope of the polarization [85]. Otherwise, the device characteristic shows a hysteresis,

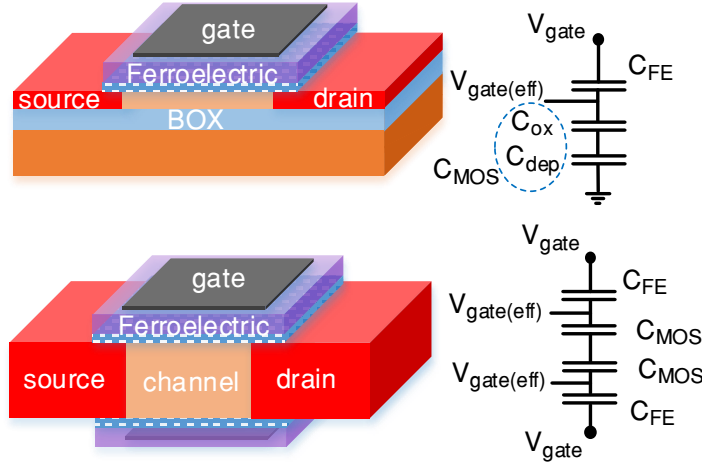


Figure 2.9 – Device schematic and the simplified capacitance model of the UTBB FDSOI/Double Gate NC-FETs. The MOS capacitance (C_{MOS}) is a series combination of the oxide capacitance (C_{ox}) and the silicon depletion capacitance (C_{dep}). The NC-FET can be considered as a ferroelectric capacitor in series with a conventional MOSFET.

corresponding to the coercive fields of the ferroelectric without performance-boosting. In this section, we propose a matching condition between the ferroelectric negative capacitance and the gate intrinsic capacitance of the reference transistor to ensure the maximum enhancement in the non-hysteretic operation of an NC-FET.

The NC-FET can be considered as a conventional transistor with an added amplifier. Therefore, the amplification factor of the NC effect can be expressed as,

$$\beta = \partial V_{int} / \partial V_g = C_{FE} / (C_{FE} + C_{int}). \quad (2.17)$$

The following conditions are required to provide a sufficient amplification in the non-hysteretic behavior of an NC-FET: (i) the absolute value of the ferroelectric negative capacitance (C_{FE}) and the intrinsic gate capacitance (C_{int}) need to be relatively close, and (ii) the total capacitance should remain positive in the whole range of operation; $C_{total}^{-1} = C_{FE}^{-1} + C_{int}^{-1} > 0$.

The most important parameters that can be optimized in order to satisfy the NC matching conditions in the ferroelectric thickness and area. In an integrated FeFET, the area of the ferroelectric capacitor is fixed to the gate dimensions. Therefore, considering the fact that the physical parameters of the transistor are set by the technology node, the ferroelectric thickness is the key to fulfill the negative capacitance matching conditions and obtain a true hysteresis-free NC-FET. In this regard, we proposed and investigated the high performance and low power design space of non-hysteretic negative capacitance MOSFETs for the CMOS 14 nm technology node based on the calibrated simulations

2.2. Capacitance matching condition

using an experimental gate stack with PZT ferroelectric to obtain the negative capacitance effect. All necessary parameters are extracted by carefully characterizing experimentally fabricated ferroelectric capacitors, to ensure realistic simulation results.

The operation principle of NC-FETs has been theoretically investigated [91, 92, 93, 94]. However, previous findings of device performance investigations have been obtained considering either the analytical approach [94, 93, 95] or numerical simulations [89, 96] to study the device performance. Moreover, the presented models are not valid in recent technology nodes as they are not considering short channel and quantum mechanical effects. It is well-known that quantum mechanical and short channel effects modify the charge distribution (and as a result of the gate capacitance) in the channel, especially in nanoscale dimensions. The capacitance (charge) matching conditions directly depend on the charge distribution as it defines the MOS capacitance (MOS capacitance is the series combination of the oxide capacitance and the silicon capacitance that depends on the charge distribution in the channel). The MOS device is simulated by employing the Silvaco TCAD commercial simulator that can predict the device behavior precisely down to the nanoscale considering short channel and quantum mechanical effects. Using the presented method, we have designed and explored the electrical properties of the 14 nm node UTBB FD-SOI negative capacitance MOSFET. The ferroelectric layer is modeled using 1-D Landau equation. The 2-D electrostatic effects in the ferroelectric that are expected to be pronounced in short channel devices are justified by averaging of the electrostatic fields in the metallic intermediate layer. This intermediate metallic film provides the uniform electrostatic field inside the ferroelectric layer and makes us eligible to model the ferroelectric dielectric with 1-D Landau model. The idea of using the metallic intermediate layer comes from the experimentally reported results that expressing the negative capacitance behavior occurs only in FeFETs that is using this metallic film (as it provides a uniform electric field inside the ferroelectric material) [74].

The ferroelectric thickness obtained by the proposed approach leads to the maximum enhancement in the non-hysteretic operation of an NC-FET. Our results reveal a clear and significant double improvement in (i) subthreshold swing and (ii) gate overdrive, using the negative capacitance effect. Simulations using Silvaco TCAD coupled with a realistic Landau model of ferroelectrics demonstrates that a 14 nm node UTBB FDSOI FET can operate at 0.26 V instead of 0.9 V gate voltage using negative capacitance effect, with an average subthreshold swing of 55 mV/decade at room temperature. The double gate structure is proposed to overcome the large mismatch between the ferroelectric and MOS capacitor to enhance the negative capacitance effect and reduce the ferroelectric's optimized thickness. A 14 nm node DG NC-FET can operate at 0.24 V gate voltage with an average subthreshold swing of 45 mV/decade.

Here, we combine both numerical simulations and analytical models to have a detailed study of nanoscale NC-FETs. We design and explore the electrical properties of the 14 nm node (20 nm physical gate length) Ultra-Thin Body and Box Fully Depleted Silicon On

Insulator (UTBB FDSOI) and Double Gate (DG) NC-FETs. The 2-D electrostatic effects that are expected to be pronounced in short channel devices are justified by averaging of the electrostatic fields in the metallic intermediate layer [74]. This intermediate metallic film provides the uniform electrostatic field inside the ferroelectric layer and makes us eligible to model the ferroelectric dielectric with 1-D Landau model. We also propose and examine a practical design guideline to have the maximum enhancement in the non-hysteretic operation of an NC-FET [72]. We found that the negative capacitance not only improves the subthreshold slope but also increases the overdrive voltage significantly. Lastly, we propose the DG NC-FET to overcome the large mismatch between the MOS and ferroelectric capacitors and pin the MOS capacitance in a relatively large value. This improves the NC amplification effect and reduces the optimized thickness of the ferroelectric to have the maximum enhancement in the non-hysteretic operation of the device [72].

The single and double gate FeFET schematics including a simple capacitance model are depicted in Figure 2.9. Simulation results have been obtained by combining Silvaco TCAD commercial simulator [97] with Landau's theory of ferroelectrics. Results are reported for the devices at the state-of-the-art of the technology, 14 nm CMOS node UTBB FDSOI FET [98] and DG MOSFET with the same physical gate length. PZT is used as the gate ferroelectric, and Landau parameters are extracted by characterizing the experimentally fabricated ferroelectric capacitors.

2.2.2 Simulation method and device structure

The device schematic of the UTBB FDSOI NC-FET and the DG NC-FET are presented in Figure 2.9. The conventional gate stack of a MOSFET is replaced by a stack of a linear and a ferroelectric dielectric. An intermediate metallic film is considered between the linear and ferroelectric dielectrics. As mentioned before, the intermediate metallic film is chosen following the experimental results [74] to ensure a uniform potential profile along the ferroelectric. This layer averages out the non-uniform potential profile along the channel as well as any charge non-uniformity coming from the domain formation in the ferroelectric. This also provides the possibility to model the ferroelectric capacitor with the 1-D Landau approach even in nanoscale devices. Ferroelectric negative capacitance transistors with the Metal-Ferroelectric-Metal-Insulators-Semiconductor (MF MIS) structure cannot be simulated even with the state-of-the-art device simulators. We have considered the NC-FET as a series combination of a ferroelectric capacitor and a conventional MOSFET without imposing any boundary condition due to the presence of the intermediate layer. The device performance of an MF MIS structure is numerically calculated by combining Silvaco Atlas commercial simulator with the Landau-Khalatnikov (L-K) theory of ferroelectrics [99, 35].

According to the L-K equation, in the vicinity of a phase transition, the Gibbs free

2.2. Capacitance matching condition

energy density (U) of the ferroelectric layer can be expanded in powers of the polarization (P).

$$U = \alpha t_{FE} P^2 + \beta t_{FE} P^4 + \gamma t_{FE} P^6 - V_{FE} P$$

$$U = \alpha t_{FE} Q^2 + \beta t_{FE} Q^4 + \gamma t_{FE} Q^6 - V_{FE} Q, \quad (2.18)$$

where α , β , and γ are material dependent constants (Landau parameters), t_{FE} is the ferroelectric film thickness, V_{FE} is the applied voltage across the ferroelectric layer, and Q is the electrical charge of the ferroelectric capacitor. The equilibrium state of the ferroelectric layer is determined by finding the minima of U, where we have

$$\frac{\partial U}{\partial Q} = 2\alpha t_{FE} Q + 4\beta t_{FE} Q^3 + 6\gamma t_{FE} Q^5 - V_{FE} = 0. \quad (2.19)$$

Therefore, the charge-voltage characteristic of the ferroelectric capacitor can be obtained as

$$V_{FE} = 2\alpha t_{FE} Q + 4\beta t_{FE} Q^3 + 6\gamma t_{FE} Q^5. \quad (2.20)$$

Considering the presented structure in Figure 2.9, equation 2.20 can be written as

$$V_g - V_{g_eff} = 2\alpha t_{FE} Q + 4\beta t_{FE} Q^3 + 6\gamma t_{FE} Q^5, \quad (2.21)$$

where V_g is the applied gate voltage and V_{g_eff} is the intermediate contact potential. The left-hand side of equation 2.21 corresponds to the voltage drop across the ferroelectric film, and its right-hand side represents the charge characteristic of a ferroelectric capacitor.

The MFMIS structure can be assumed as a series combination of a ferroelectric capacitor and a regular MOSFET. The 2-D electrostatics for the MOSFET has been carried out by mean of Silvaco TCAD commercial simulator taking into account the nonlocal path band-to-band model, standard Shockley-Reed-Hall recombination, drift-diffusion model, and quantum mechanical model. The analysis of the regular MOS part of the device can be simulated independently without imposing any boundary condition.

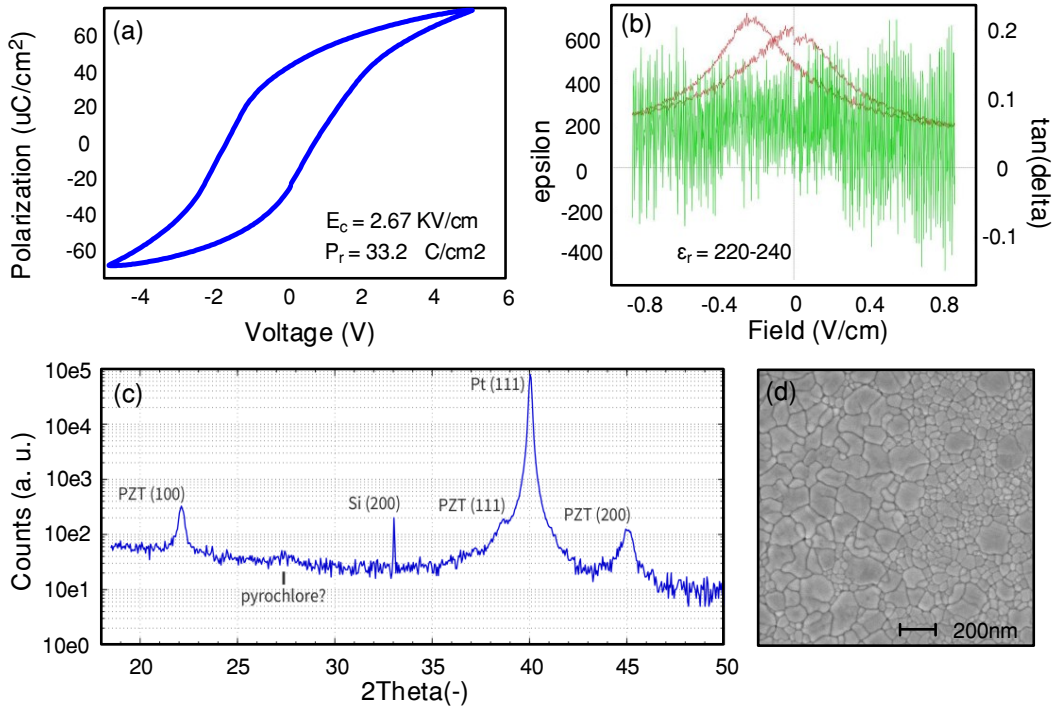


Figure 2.10 – Electrical and physical characterization of PZT ferroelectric thin film. The film polarization, permittivity, and the phase angle of the capacitance measurement hysteresis loops regarding the applied voltage (electric field) on the ferroelectric layer are depicted in (a). The relative permittivity, coercive field, and remanent polarization of the PZT thin film are 220-240, 260 KV/cm, and $30.2 \mu\text{C}/\text{cm}^2$, respectively (b). XRD 2-theta profile (c) and SEM analysis (d) of the PZT thin film illustrate that the film is polycrystalline (see microstructures in SEM image) and textured 111-oriented, which is the most commonly used orientation.

This is due to the presence of the metallic intermediate layer between the ferroelectric and linear dielectrics. Moreover, the potential is the same at any grid point of this intermediate layer and makes the possibility to model the ferroelectric film with 1-D Landau approach. This 2-D hybrid Electrostatics for MOSFET and 1-D Landau model are solved self-consistently to simulate the negative capacitance MOSFET [18].

PZT is used as the gate ferroelectric due to its numerous advantages like reliability, having a sufficient polarization value even in thin films, high dielectric constant, and most importantly its nanosecond polarization reversal [100]. However, PZT is not employed only for its technological advantages, but also for its robust properties regarding the film thickness variation. The ferroelectric properties mostly change regarding the layer thickness [45]. However, no considerable variation was observed in the PZT properties for the films having a thickness below 100 nm.

It should be noted that PZT has some drawbacks such as the high temperature

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deposition process, diffusion of lead to the silicon channel, and lack of a CMOS compatible deposition technique for single crystalline growth of the PZT. However, these problems can mostly be solved by developing a last gate process, considering a diffusion barrier underneath the PZT thin film, and using a proper seed layer for PZT growth.

In order to obtain realistic simulation results for the FeFET operation, we used experimentally extracted Landau parameters of the PZT thin film. In that pursuit, 46 nm of PZT with 43/57 (Zr/Ti) ratio is deposited on a stack of TiO₂(2 nm)/Pt(100 nm)/TiO₂/Ti/SiO₂/Si by employing the sputtering technique. Pt top electrode is deposited by room temperature sputtering and patterned by shadow masking.

Electrical and physical characterization of the fabricated PZT thin film is presented in Figure 2.10. The coercive field (E_c), remanent (P_r), and saturation polarizations (P_s) are extracted from the polarization-voltage hysteresis loop (Figure 2.10-a) by averaging the value of the positive and negative going branches of the diagram. The PZT coercive field, remanent, and saturation polarization are 260 KV/cm, 30.2 $\mu\text{C}/\text{cm}^2$, and 70.3 $\mu\text{C}/\text{cm}^2$, respectively. XRD 2-theta profile (Figure 2.10-c) and SEM analysis (Figure 2.10-d) of the PZT thin film indicate that the film is polycrystalline and textured 111-oriented which is the most common orientation in PZT.

Landau coefficients (α , β , and γ) are determined and fitted based on the presented approach in [101] and employing the experimentally extracted values of the coercive field, remanent, and saturation polarization. The PZT ferroelectric thin film Landau parameters are calculated as follows; $\alpha = -13.5 \times 10^7$, $\beta = 3.05 \times 10^8$, and $\gamma = -2.11 \times 10^7$ (SI unit) at room temperature, which are close to the reported parameters for a high quality polycrystalline PZT thin films. It is well-known that PZT properties alters regarding the Zr/Ti ratio, doping concentration, and the process temperature [102, 103, 104, 105]. However, considering the Landau equation, the charge-voltage characteristic of ferroelectric capacitors also depends on the layer thickness. This can compensate for the Landau parameters variation. Although using a different ferroelectric material changes the NC-FET behavior, however, this approach will lead to a different optimized thickness of the material that can provide almost the same performance boosting. Therefore, we use the experimentally extracted Landau coefficients of a specific PZT capacitor, highlighting the fact that the operation principle of the device would be the same for different ferroelectrics.

2.2.3 UTBB FDSOI NC-FET

In this section, we focused our analysis on a 14 nm CMOS node high-performance UTBB FDSOI nMOSFET [98]. The device physical gate length is 20 nm while each spacer has 3 nm width. The channel, BOX, and the gate equivalent oxide thickness are 6 nm, 25 nm, and 0.9 nm, respectively. The channel is undoped ($1 \times 10^{15} \text{ cm}^{-3}$) and the source and

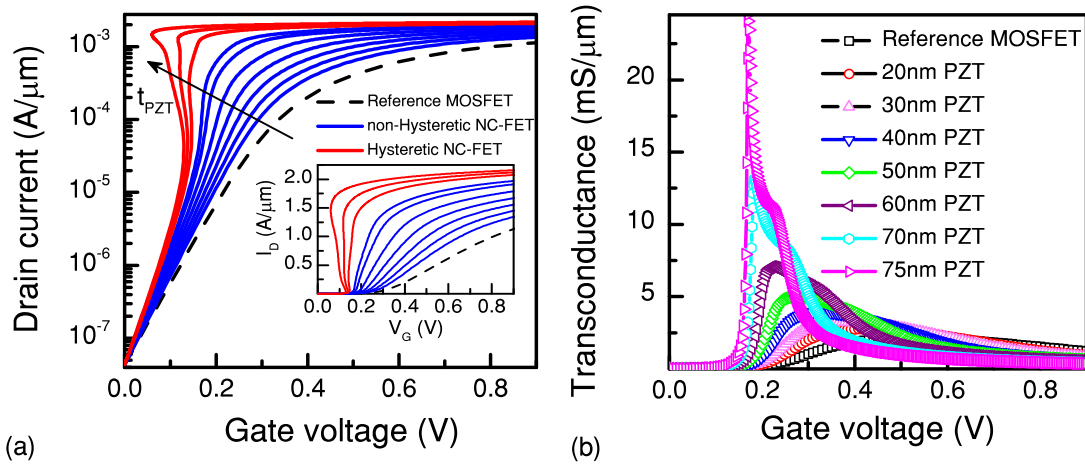


Figure 2.11 – (a) Transfer characteristic of the reference UTBB FDSOI FET [98] (dashed line) comparing the non-hysteretic (blue curves) and hysteretic (red curves) negative capacitance devices. (b) illustrates the transconductance improvement in non-hysteretic negative capacitance devices which is increasing by increasing the ferroelectric thickness.

drain doping level is greater than $5 \times 10^{20} \text{ cm}^{-3}$ to achieve low external resistance. The supply voltage is 0.9 V, the drain saturation current (at $V_{drain} = V_{DD}$) is $1.12 \text{ mA}/\mu\text{m}$, and the leakage current is below $100 \text{ nA}/\mu\text{m}$. The source contact is grounded, and the back gate (substrate) contact is used to adjust the threshold voltage.

The signature of the operation in the non-hysteretic NC region is a single-valued gate capacitance characteristic (single-valued drain current or surface potential transfer characteristic). In Figure 2.11 the blue curves indicate the non-hysteretic operation of the device.

The key to the negative capacitance effect is that the negative differential capacitance of the ferroelectric ($C_{FE} < 0$) compensates the positive capacitance (C_{MOS}) in the device such that the resulting gate capacitance $C_g = (C_{FE}^{-1} + C_{MOS}^{-1})^{-1}$ can be made larger than C_{MOS} and boosts the surface potential [90]. The ferroelectric capacitor is effectively a negative one as the slope of the Q-V (P-E) characteristic of a ferroelectric material is negative around the origin.

The negative slope of the ferroelectric charge diagram is unstable and exhibit hysteretic jumps in the charge (polarization). However, it has been shown that if the ferroelectric capacitor is placed in series with a positive capacitor, the negative capacitance segment can be effectively stabilized and provides voltage amplification [18, 74]. A series positive capacitor can make the total capacitance of the structure positive in the whole range of the operation and hence, the NC effect can be stabilized. As long as the total capacitance of the structure is positive, the system behaves like a positive capacitor with a value larger than both C_{MOS} and C_{FE} .

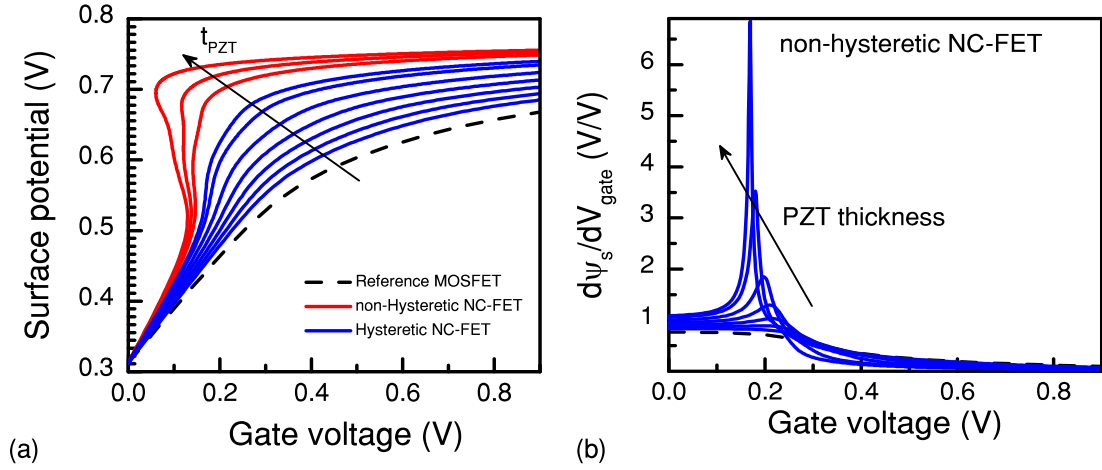


Figure 2.12 – (a) explains how the surface potential of the MFIS structure is boosted due to the NC effect. (b) demonstrates the surface potential derivative in non-hysteretic NC-FETs.

The electrical properties of the 14 nm node UTBB FDSOI negative capacitance MOSFET are depicted in Figure 2.11. Results are presented for sweeping the PZT thickness from 20 nm to 100 nm. As it was mentioned before, one of our motivations for choosing PZT as the gate ferroelectric was its stable properties regarding the film thickness variation of below 100 nm. The PZT properties such as remanent polarization and coercive field vary by changing the film thickness. However, we did not observe any considerable changes in the PZT properties for a few nanometer film thickness variation. Besides that, the effect of the ferroelectric properties variation can be compensated by tuning the film thickness, and the operation principle of the device would be the same.

As a general rule, high- t_{FE} values (t_{FE} is the ferroelectric thickness) give rise to the hysteretic behavior (red curves in Figures 2.11 and 2.11). Reducing t_{FE} , hysteresis disappears, and voltage amplification can be reached. By decreasing the t_{FE} values, the step-up conversion capability degrades and vanishes below a certain thickness [89, 94]. As a consequence of these constraints, a key parameter of the device design is to properly tune t_{FE} . The optimized thickness of the ferroelectric for negative capacitance FETs provides the maximum enhancement while the transfer characteristic of the device is still single-valued.

In our case, 75 nm of PZT provides the highest improvement before the device operation gets hysteretic. The transconductance improvement in non-hysteretic devices is illustrated in Figure 2.11-b. The transconductance peak is boosted more than 10 times of its original value.

The unique signature of the negative capacitance effect in an MFIS (or MFMIS) structure is providing surface potential derivative greater than 1 (Figure 2.12-b). The

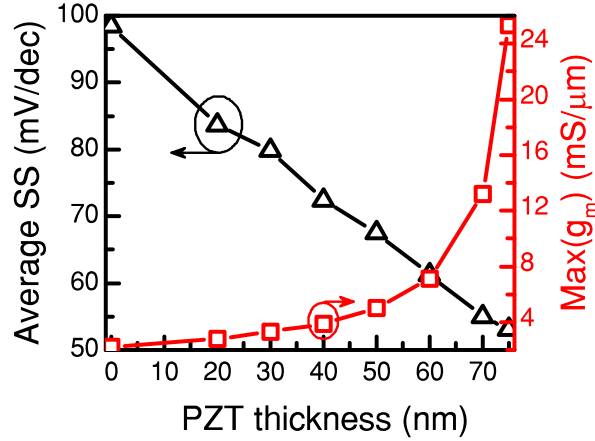


Figure 2.13 – Average subthreshold swing (left-axis) and the transconductance peak (right axis) with respect to the ferroelectric thickness for a 14 nm UTBB FDSOI NCFET. An average SS below 60 mV/decade and a Max(g_m) higher than 25 mS/ μ m are obtained using 75 nm of PZT.

partial of the gate voltage regarding the surface potential can be written as

$$\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_{MOS}}{C_{FE}}, \quad (2.22)$$

that illustrates how the ferroelectric negative capacitance can provide a voltage amplification and a value of surface potential derivative greater than 1.

One of the most important parameters of switching devices is how steep they can switch from the off-state to the on-state. It is known that due to the Boltzmann thermal limit, the *off-to-on* transition in conventional MOSFET devices cannot be any steeper than 60 mV/decade. The step-up conversion in ferroelectric devices can be utilized to reduce the device subthreshold swing (SS) [18].

The simulation results (Figure 2.11) demonstrate that the negative capacitance amplification starts in the subthreshold region and continues up to the overdrive region. This property can be used to increase the I_{ON}/I_{OFF} figure of merit for a prescribed supply voltage or reducing the required supply voltage for an arbitrary output current. The subthreshold swing and overdrive voltage can be expressed as

$$SS = \frac{\partial V_g}{\partial \log I_d} = \frac{\partial V_g}{\partial \psi_s} \times \frac{\partial \psi_s}{\partial \log I_d}, \quad (2.23)$$

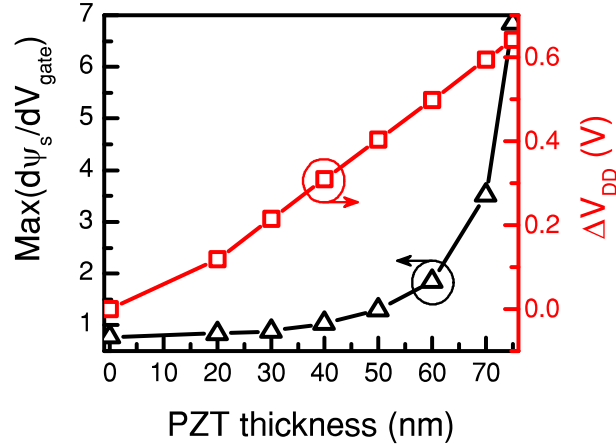


Figure 2.14 – Surface potential derivative peak (left axis) and the gate voltage reduction (right axis) in case of the 14 nm node UTBB FDSOI NCFET. The surface potential derivative which is below 1 in conventional MOSFETs, can be increased up to 7, using 75 nm of PZT. Due to the subthreshold swing and the overdrive enhancement caused by the negative capacitance effect the gate voltage can be reduced up to 72% with the same level of the output current (1.12 mA/μm).

$$V_{OD} = V_g - V_{TH}, \quad (2.24)$$

where V_{OD} , V_g , and V_{TH} are the overdrive voltage, the gate voltage, and the device threshold voltage, respectively. The ferroelectric dielectric causes the gate voltage amplification (in both subthreshold and overdrive regions) and threshold voltage reduction. This results in a significant reduction of the required gate voltage sustaining the same level of the output current. Figure 2.13 depicts the average subthreshold swing and the maximum of the transconductance regarding the ferroelectric thickness.

The average SS is calculated from the zero gate voltage to the threshold voltage, representing the effect of NC on both overdrive and subthreshold swing of the MOSFET. The average SS is reduced from 100 mV/decade (reference device) down to 55 mV/decade and the maximum of the transconductance is increased from 2.2 mS/μm up to 25.3 mS/μm employing 75 nm of PZT as the gate ferroelectric. Moreover, the NC effect boosts the maximum of the transconductance from 2.2 mS/μm to 25.3 mS/μm.

The gate voltage reduction (ΔV_{DD}) and the maximum of the surface potential derivative are presented in Figure 2.14. The surface potential derivative greater than 7 and up to 72% gate voltage reduction is obtained due to the NC effect. The 14 nm node UTBB FDSOI NC-FET using 75 nm of PZT as the ferroelectric dielectric can operate at 0.26 V instead of 0.9 V gate voltage providing the same I_{ON}/I_{OFF} figure of merit.

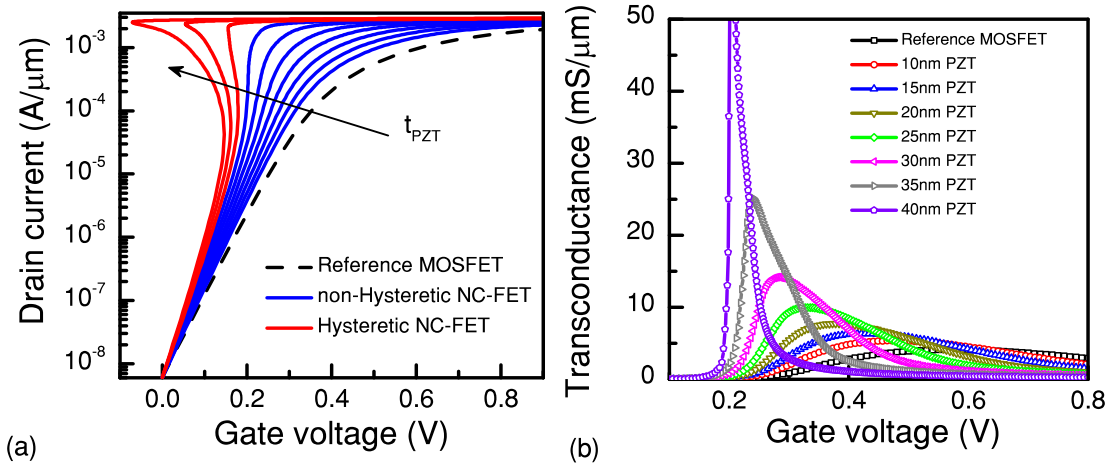


Figure 2.15 – (a) I_d - V_g characteristic of the reference DG MOSFET (dashed line) comparing the non-hysteretic (blue curves) and hysteretic (red curves) negative capacitance devices transfer characteristic. (b) Transconductance improvement in non-hysteretic negative capacitance devices which is increasing by increasing the ferroelectric thickness.

2.2.4 Double Gate NC-FET

As it was mentioned previously, an NC-FET can be modeled as a conventional transistor with an added amplifier. Considering a simple capacitance model (Figure 2.9), the amplification factor of the negative capacitance effect can be expressed as

$$\beta = \Delta V_{MOS} / \Delta V_g = C_{FE} / (C_{FE} + C_{MOS}). \quad (2.25)$$

In order to obtain a meaningful enhancement (large β), the magnitude of the ferroelectric negative capacitance ($|C_{FE}|$) and the MOS capacitance (C_{MOS}) needs to be relatively close. However, C_{MOS} is not a constant and varies with the gate voltage; therefore, β is a voltage-dependent parameter. On the other side, to have a non-hysteretic operation, the total capacitance of the gate ($C_g^{-1} = C_{FE}^{-1} + C_{MOS}^{-1}$) needs to be positive in the whole range of the gate voltage ($|C_{FE}|$ should be greater than C_{ox}).

In a conventional single gate MOSFET with a uniformly doped substrate, the depletion capacitance and therefore the MOS capacitance could be much lower than C_{ox} as C_{MOS} is the series combination of the depletion capacitance and the oxide capacitance. So, the amplification factor cannot be significantly larger than 1 over a broad range of the gate voltage.

To have a significant amplification, we have to pin the depletion capacitance in a relatively large value. By employing the fully depleted silicon on insulator structure,

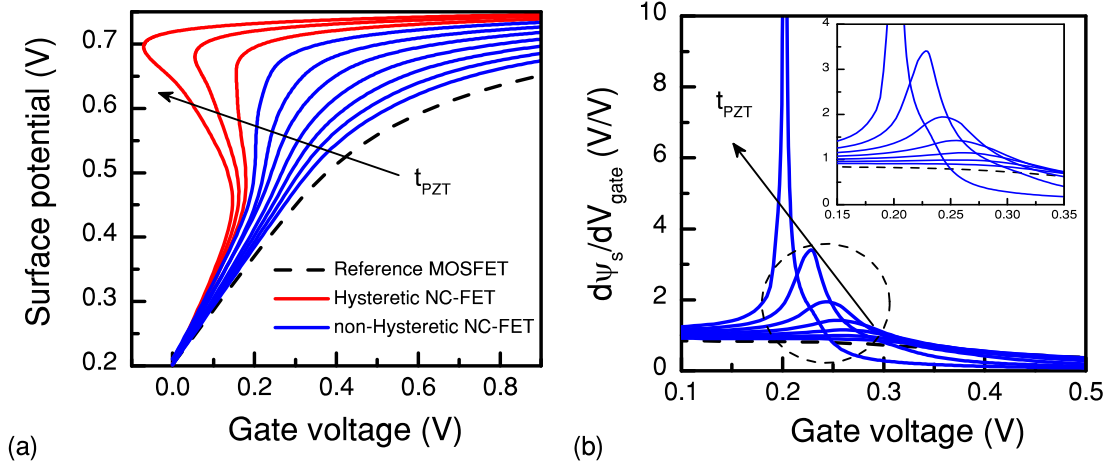


Figure 2.16 – (a) explains how the surface potential of the MFIS structure is boosted due to the NC effect and (b) demonstrates the surface potential derivative in non-hysteretic DG NC-FETs.

the depletion depth is anchored to the silicon thickness (6 nm), providing a sufficient amplification over a wide range of the gate voltage.

The capacitance of the ferroelectric layer around the origin can be expressed as $0.5\alpha t_{FE}$ ($V_{FE} \sim 2\alpha t_{FE} \times Q$) where the parameter α is negative in ferroelectric materials as the key feature of the upconversion. A relatively low ferroelectric capacitance requires a large t_{FE} , which is not appropriate for nanometer scale device fabrication due to the high aspect ratio of the gate stack (20 nm physical gate length with nearly 80 nm height gate stack).

We propose the DG NC-FET structure in order to reduce the optimized ferroelectric thickness and improve the negative capacitance amplification effect at the same time. In a symmetric double gate structure, the depletion thickness is pinned to half of the silicon thickness, providing a relatively high depletion capacitance. Moreover, in the case of the double gate structure, there is no additional series capacitance to reduce the MOS total capacitance (as the BOX capacitance reduces the total C_{MOS} in UTBB FDSOI FET).

We designed and simulated a 14 nm CMOS node DG NC-FET, corresponding to the UTBB FD SOI FET of the previous section. The device nominal gate length, the channel thickness, and the gate equivalent oxide thickness is 20 nm, 6 nm, and 0.9 nm, respectively. Again, we have considered 3 nm width for each spacer. The channel is undoped ($1 \times 10^{15} \text{ cm}^{-3}$) and the source and drain doping level is $> 5 \times 10^{20} \text{ cm}^{-3}$ to minimize the series resistance. The supply voltage is 0.9 V, the saturation current ($V_{drain} = V_{DD}$) is 2.1 mA/ μm , and the device leakage current is below 10 nA/ μm . Again, PZT is considered as the gate ferroelectric. Figure 2.15 represents the electrical properties of the double gate negative capacitance MOSFET sweeping the PZT thickness. The

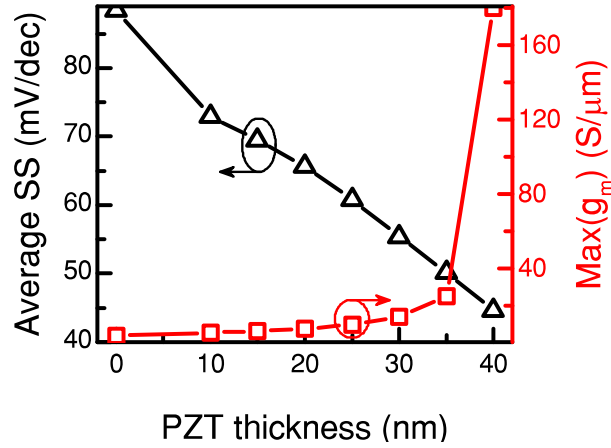


Figure 2.17 – Average subthreshold swing (left-axis) and the transconductance peak (right-axis) with respect to the ferroelectric thickness for a 14 nm node DG NC-FET. The average SS below 50 mV/decade and the $\text{Max}(g_m)$ higher than 180 mS/ μ m are obtained using 40 nm of PZT.

transform characteristic of the device is illustrated in Figure 2.15-a (PZT thickness is varied from 10 nm to 55 nm).

As we discussed in the previous section, increasing the ferroelectric thickness improves the device performance. Nevertheless, after a critical thickness, the device operation gets hysteretic (red curves in Figure 2.15 and Figure 2.16 belongs to the hysteretic NC-FETs). The optimized thickness of the PZT for the DG NC-FET is 40 nm where we have the maximum enhancement in the non-hysteretic operation of the device. The transconductance of the non-hysteretic cases is compared with the reference transistor in Figure 2.15-b, the dashed-line indicates the baseline MOSFET. The surface potential derivative regarding the gate voltage is depicted in Figure 2.16-b. A surface potential derivative > 1 is obtained that ensures the presence of negative capacitance effect in the MFIS structure.

Figure 2.17 illustrates the average subthreshold swing (left y-axis) and the maximum of the transconductance (right y-axis). The average subthreshold slope of the device (calculated by considering the device current at the zero gate voltage up to the threshold voltage) that indicates the steepness of the *off-to-on* transition is reduced from 84.4 mV/decade down to 44.6 mV/decade using 40 nm of PZT. The transconductance peak is also enhanced from 4.1 mS/ μ m (reference DG MOSFET) to 180 mS/ μ m.

The surface potential derivative regarding the PZT thickness is illustrated in Figure 2.18 (left y-axis). The maximum of the surface potential derivative is increased from 0.8 in the reference device up to 24.8 using the ferroelectric optimized thickness. As a result of the significant subthreshold swing and overdrive enhancement that is caused by

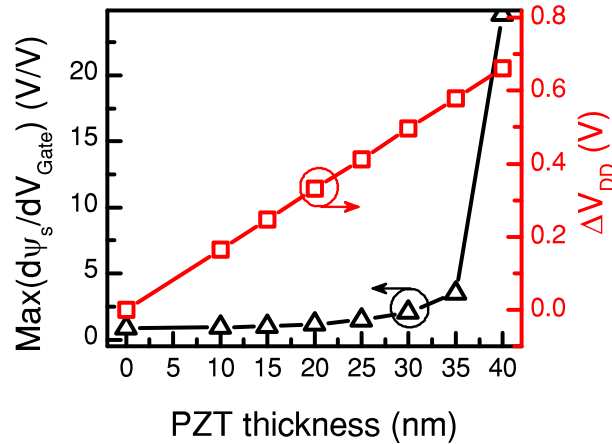


Figure 2.18 – Surface potential derivative peak (left-axis) and the gate voltage reduction (right-axis) in case of the 14 nm node DG NC-FET. The surface potential derivative which is below 1 in conventional MOSFETs can be increased up to 24 using 40 nm of PZT. Due to the subthreshold swing and the overdrive enhancement caused by the negative capacitance we can reduce the gate voltage by 73% providing the same level of the output current ($2.1 \text{ mA}/\mu\text{m}$).

the negative capacitance effect, the gate voltage can be reduced without performance reduction. The supply voltage reduction (ΔV_{DD}), which is depicted in the right y-axis of Figure 2.18 illustrates that the gate voltage can be lowered down to 0.24 V by integrating 40 nm of PZT into the gate stack.

Besides better electrical properties of the DG NC-FET comparing the single gate NC-FET, the critical thickness of the ferroelectric (PZT in our case) is much lower in the double gate device compared to the UTBB FDSOI NC-FET. The optimized thickness of the PZT for the DG NC-FET is 40 nm while it is 75 nm in the case of UTBB FDSOI NC-FET.

2.3 Summary

Overall in this chapter, first, we have proposed a theoretical condition for the negative capacitance of ferroelectric materials to occur when integrated to the gate stack of an MOS transistor. The theory was based on a physical model using basic Maxwell's equations and Tsividis model for MOS transistor. The condition was verified on previously reported NC-FETs, presenting the negative capacitance together with a large hysteresis. The devices were fabricated with an organic ferroelectric where we could observe a voltage amplification, and we found an excellent agreement with the presented theory. A complete set of equations was presented as a design rule for negative capacitance transistors.

Lastly, a matching condition between the ferroelectric negative capacitance and the gate intrinsic capacitance of the baseline transistor to obtain the maximum enhancement in the non-hysteretic operation of an NC-FET is proposed and theoretically examined. In this regard, a new design space for non-hysteretic negative capacitance MOSFETs has been proposed and examined on 14 nm CMOS node UTBB FDSOI/Double Gate NC-FETs. PZT is used as the gate ferroelectric and Landau parameters are extracted by characterizing the experimentally fabricated PZT thin films. We have shown that the negative capacitance effect leads to both enhanced subthreshold slope and gate overdrive. It is demonstrated that the 14 nm UTBB FDSOI high-performance MOSFET can operate at 0.26 V gate voltage instead of 0.9 V. This device shows a leakage current less 100 nA/ μm and a saturation current of 1.21 mA/ μm using 75 nm of PZT as the NC booster. The device average subthreshold swing is reduced down to 55 mV/decade while the reference device's average SS is 100 mV/decade. It has also been presented that using the double gate structure reduces the ferroelectric's optimized thickness by pinning the MOS capacitor in a relatively large value. A 14 nm DG NC-FET can operate at 0.24 V gate voltage (instead of 0.9 V) sustaining the same current level (2.1 mA/ μm) by integrating 40 nm of PZT into the gate stack. Providing 44.6 mS/ μm average SS and 180 mS/ μm transconductance peak indicates that the DG NC-FET has a transfer characteristic closer to the ideal switch.

3 Negative Capacitance MOSFETs

Abstract:

Negative Capacitance (NC) in ferroelectric materials is proposed in order to address this physical limitation of CMOS technology. The novelty and universality of this approach relate to the fact that the gate stack is not anymore a passive part of the transistor and contributes to the signal amplification. In this chapter, we experimentally validate NC as a universal performance booster: (i) for complementary MOSFETs, of both n- and p-type in an advanced CMOS technology node, and, (ii) for both digital and analog significant enhancements of key figures of merit for information processing (subthreshold swing, overdrive, and current efficiency factor). Accordingly, a sub-thermal swing down to 10 mV/decade together with an enhanced current efficiency factor up to 10^5 V^{-1} is obtained in both n- and p-type MOSFETs at room temperature by exploiting a PZT capacitor as the NC booster. The overdrive voltage is enhanced up to 0.45 V, leading to a supply voltage reduction of 50%. The negative capacitance MOSFETs are demonstrated in hysteretic and non-hysteretic modes of operation. A matching condition is proposed to tune the hysteretic behavior of NC-FETs. For the first time, we achieve a non-hysteretic switch configuration in our fabricated MOSFETs, suitable for analog and digital applications, for which a reduction in the subthreshold swing is obtained down to 20 mV/decade. Lastly, the impact of physical parameters of the ferroelectric layer on the performance of NC-FETs is experimentally studied. Electrical performances of PZT-based and Si:HfO₂-based NC-FETs are investigated and discussed. In a PZT-based p-type NC-FET, a sub-thermal swing down to 20 mV/decade is achieved due to the remarkable voltage gain of NC, reaching a maximum value of 10 V/V. Nevertheless, the performance improvement of the Si:HfO₂ NC booster is significantly lower than the one of PZT due to the coexistence of different phases and also high leakage current, which can enormously reduce the enhancement of NC.

3.1 Negative Capacitance as performance booster of CMOS

As it is briefly mentioned in the Introduction chapter, Complementary Metal-Oxide-Semiconductor (CMOS) scaling will be eventually limited by the inability to remove the heat generated in the switching process [106]. The origin of this issue can be traced back to the operation principle of the silicon CMOS devices governed by the non-scalability of thermal voltage (Boltzmann's tyranny). This results in preventing these devices to achieve a sub-60 mV/decade subthreshold slope (SS) at room temperature. The SS of a MOSFET is obtained by

$$SS = \frac{\partial V_g}{\partial(\log I_d)} = \frac{\partial V_g}{\partial \psi_s} \times \frac{\partial \psi_s}{\partial(\log I_d)}, \quad (3.1)$$

where ψ_s corresponds to the surface potential of the silicon channel. In a conventional MOSFET, the lower limit of the second term in RHS of equation 3.1 is $(k_B T/q) \ln(10)$ and cannot be any lower than 60 mV/decade at 300° K. Since V_g is linked to ψ_s through a capacitive voltage divider, the first term that is known as the body factor, m , is obtained as

$$\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{MOS}}, \quad (3.2)$$

exceeds one, thus limits the SS to 60 mV/decade at $T=300^\circ$ K [107, 108]. A sub-thermal swing can be achieved using the proposed negative capacitance (NC) of ferroelectric materials [49, 18]. Negative capacitance in ferroelectrics arises from the imperfect screening of the spontaneous polarization. Imperfect screening is intrinsic to semiconductor-ferroelectric and metal-ferroelectric interfaces due to their screening lengths. The physical separation of ferroelectric bound charges from the metallic screening charges creates a depolarizing field inside the ferroelectric and destabilizes the polarization [109]. Hence, intentionally destabilizing this polarization causes an effective NC that has been proposed as a way of overcoming the fundamental limitation on the power consumption of MOSFETs [110, 111]. The negative capacitance, originating from the dynamics of the stored energy in the phase transition of ferroelectric materials, results in an internal voltage amplification in an MOS device when integrated into the gate stack.

The concept of NC can be understood by considering the free energy of ferroelectrics. A ferroelectric material is traditionally modeled using a double well energy landscape. The energy characteristic of a ferroelectric capacitor, depicted in Figure 3.1-a, is calculated by $U_{FE} = \alpha P^2 + \beta P^4 + \gamma P^6 + E_{ext} \cdot P$, where P is the polarization, E_{ext} is the externally applied electric field, and α , β , and γ are material dependent parameters [18]. In equilibrium, the ferroelectric resides in one of the wells, providing spontaneous polarization. The

3.1. Negative Capacitance as performance booster of CMOS

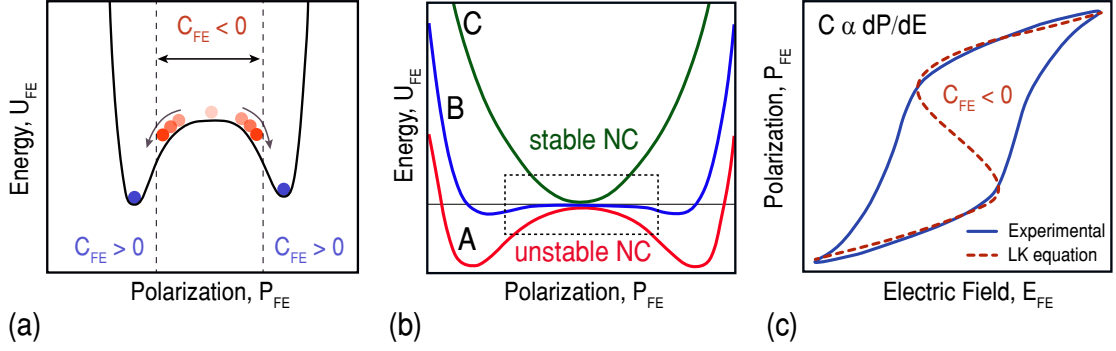


Figure 3.1 – Negative capacitance in ferroelectric materials. (a) Energy density function of a ferroelectric capacitor in equilibrium, showing an effective NC while switching from one stable polarization state to the other one. (b) Ferroelectric’s NC is unstable by itself (A), but it can be partially (B) or fully stabilized (C) by placing in-series with a positive capacitor. (c) Measured polarization vs. electric field of a PZT film (experimental) and the fitting results of L-K equation (dashed curve).

capacitance of a ferroelectric material can be determined by

$$C_{FE} = \left[\frac{d^2 U_{FE}}{dQ_{FE}^2} \right]^{-1}, \quad (3.3)$$

which is positive at the wells considering the curvature of U_{FE} vs. Q_{FE} characteristic (Figure 3.1-a). Nevertheless, the curvature is negative around the origin ($Q_{FE} = 0$). More specifically, a ferroelectric material shows an effective NC while switching from one stable polarization state to the other one [85]. It should be remarked that NC refers to the negative differential capacitance due to the small signal concept of the capacitance and relation between C_{FE} and U_{FE} (equation 3.3). The NC has been proven elusive for ferroelectrics in isolation and cannot be observed in experiments, exhibiting hysteretic jumps in the polarization. However, as it is qualitatively explained in Figure 3.1-b, if the ferroelectric placed in-series with a positive capacitor, the NC segment can be partially or fully stabilized [38, 112]. This NC region can be modeled by the state-of-the-art approach for modeling the dynamics of ferroelectric capacitors relying on L-K equation, $\rho(dP/dt) + \nabla_p U_{FE} = 0$. Figure 3.1-c compares the experimentally measured polarization vs. electric field of a PZT capacitor with the fitting result of the L-K equation.

A ferroelectric capacitor interconnecting with the gate stack of an MOS transistor creates a series connection between C_{FE} and C_{MOS} . The ferroelectric capacitor can increase the total capacitance of the gate ($C_{total}^{-1} = C_{FE}^{-1} + C_{MOS}^{-1}$) while it is stabilized in the NC region [89, 90]. Specifically, the series structure brings an abrupt increase in the differential charge in the internal node (V_{int}) by changing the gate voltage, thus providing a step-up voltage transformer [83, 113]. The internal gain of NC can be defined

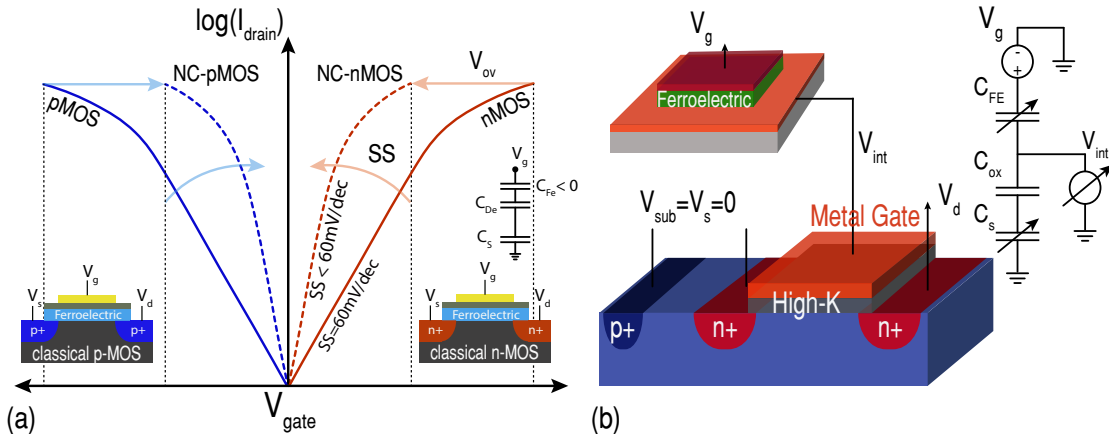


Figure 3.2 – Negative capacitance MOSFET. (a) Performance-boosting that can be achieved in both n- and p-type MOS transistors using NC of ferroelectrics in terms of SS reduction and overdrive improvement. (b) The employed experimental configuration of an n-type NC-FET including the capacitance model.

as $\beta = \partial V_{int} / \partial V_g = C_{FE} / (C_{FE} + C_{MOS})$. Accordingly, an NC booster can provide an internal voltage amplification ($\beta > 1$) which results in a body factor reduction, i.e. $1/\beta$, leading to the improvement of both analog and digital performances of the transistor. This effect is universal for all transistors where the gate stack contributes to the signal amplification and enhances the surface potential [114, 115]. The impact of a ferroelectric gate stack on the operation of complementary MOSFETs, in terms of SS reduction and overdrive improvement, is schematically shown in Figure 3.2.

In order for NC to occur, the charge line of the baseline transistor is acquired to have an intersection with the negative slope of the polarization [85]. Otherwise, the device characteristic shows a hysteresis, corresponding to the coercive fields of the ferroelectric without performance boosting [116]. Additionally, to ensure the maximum enhancement in the non-hysteretic operation of an NC-FET, the negative value of C_{FE} should be well-matched with C_{MOS} ($|C_{FE}| = C_{MOS}$ while $C_{total} > 0$ in the whole range of operation) [114, 113]. Both C_{MOS} and C_{FE} are voltage-dependent, making it extremely challenging to fully satisfy the matching condition. Therefore, the ferroelectric’s NC commonly partially gets stabilized, proposing a trade-off between the hysteretic behavior and the performance-boosting due to the NC effect.

With the validity of NC concept being experimentally established [117, 112, 118, 93, 119, 120], it is now of paramount importance to understand the challenges involved in the design of NC-FETs, so that the steepness and hysteresis of the device characteristic can be optimized in both n- and p-type MOSFETs. In this respect, a PZT capacitor is fabricated for thoroughly understanding the negative capacitance concept. It is then connected to various commercial MOSFETs, fabricated in 28 nm CMOS technology node, which is demonstrated in Figure 3.2-b. A practical matching condition is proposed and

employed to tune the hysteretic behavior of both n- and p-type NC-FETs. Afterward, the impact of NC on the performance of conventional MOSFETs is investigated by measuring and analyzing the internal node voltage. Sub-thermal swing down to 10 mV/decade is observed in n- and p-type hysteretic NC-FETs. We also report and discuss the trade-off between the performance-boosting of NC and the hysteresis, degrading the performance by reducing the hysteretic behavior. Low hysteresis NC-FETs with subthreshold swing below 30 mV/decade are reported.

The strong dependence of the NC effect on the source to drain electric field is also evidenced, reducing the impact by increasing the absolute value of V_{ds} . It is also experimentally validated that a poly-domain ferroelectric capacitor in steady states cannot have more than one stable NC domain at a time, showing a different polarization characteristic from the expected S-shape of a single-domain ferroelectric. By fully satisfying the proposed matching condition, a hysteresis-free NC-FET is also experimentally demonstrated in this chapter. The non-hysteretic NC-FET shows a subthreshold swing below the theoretical limit at room temperature, down to 20 mV/decade.

Additionally, we have compared the impact of a PZT capacitor as a commonly used ferroelectric on DC electrical behavior of commercial MOSFETs, fabricated in 28 nm CMOS technology node with the performance of an NC-FET using the CMOS compatible ferroelectric, silicon doped HfO₂ [121]. A limited boosting is observed in comparison to the PZT-based NC-FET due to the formation of non-ferroelectric phases in Si:HfO₂ and also its high leakage.

3.2 Ferroelectric materials

In this chapter, polycrystalline Lead Zirconate Titanate (PZT) thin film is mainly employed to experimentally demonstrate the negative capacitance effect. In the last section of this chapter, the recently proposed CMOS compatible ferroelectric, silicon doped HfO₂, is employed as the NC booster to compare the performance of a PZT-based NC-FET with a Si:HfO₂-based NC-FET.

3.2.1 Pb(Zr,Ti)O₃

For this experiment, 46 ± 3 nm of Pb(Zr₄₃,Ti₅₇)O₃ (PZT) ferroelectric film has been grown via the chemical solution deposition route (REF) on a Pt-coated silicon wafer. The stack of Pt(100 nm)/TiO₂(30 nm) has been sputtered on SiO₂(500 nm)/Si wafer at 300° C. The PZT film consisted of tetragonal ferroelectric phase with the predominant (100) orientation, with virtually no inclusion of any secondary non-ferroelectric phase like pyrochlore, as confirmed by XRD theta-2theta scans. The polycrystalline PZT film had dense columnar grain structure with the grain size of 200 ± 100 nm. Pt top electrodes

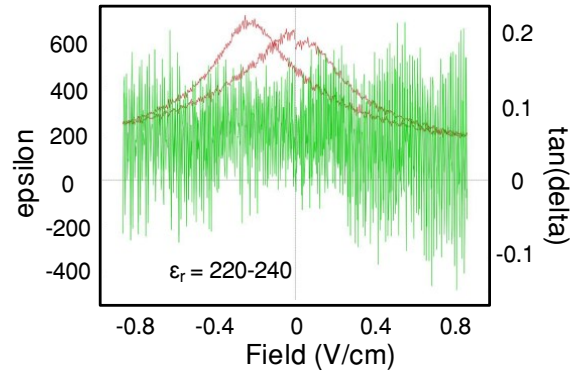


Figure 3.3 – Electrical characterization of a 46 nm thick PZT ferroelectric thin film, showing the film polarization, permittivity, and the phase angle of the capacitance measurement hysteresis loops.

were deposited on PZT film by sputtering and post-annealed at 550° C in an oxygen atmosphere in order to remove the sputtering damage at the Pt/PZT top interface.

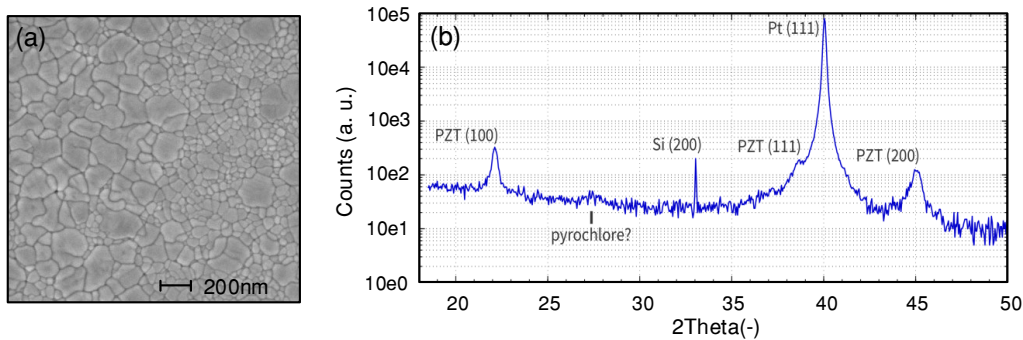


Figure 3.4 – Physical characterization of the PZT ferroelectric thin film. SEM analysis (a) and XRD 2-theta profile (b) of the PZT thin film illustrates that the film is polycrystalline (see microstructures in SEM image) and textured 111-oriented, which is the most commonly used orientation.

The ferroelectric capacitors exhibited the dielectric properties typical for high-quality ferroelectric PZT layers of this type as it is illustrated in Figure 3.3. Specifically, the polarization hysteresis loop (Figure 3.5) measured at 1 KHz showed the remanent polarization of $25 \pm 3 \mu\text{C}/\text{cm}^2$ and coercive fields of $+80/-300 \text{ KV}/\text{cm}$, with the polarization imprint that favors the top-to-bottom polarization direction. Low-signal C-V measurements show the hysteretic behavior of the dielectric constant with the maximum values of 600-700 near the coercive voltage [122].

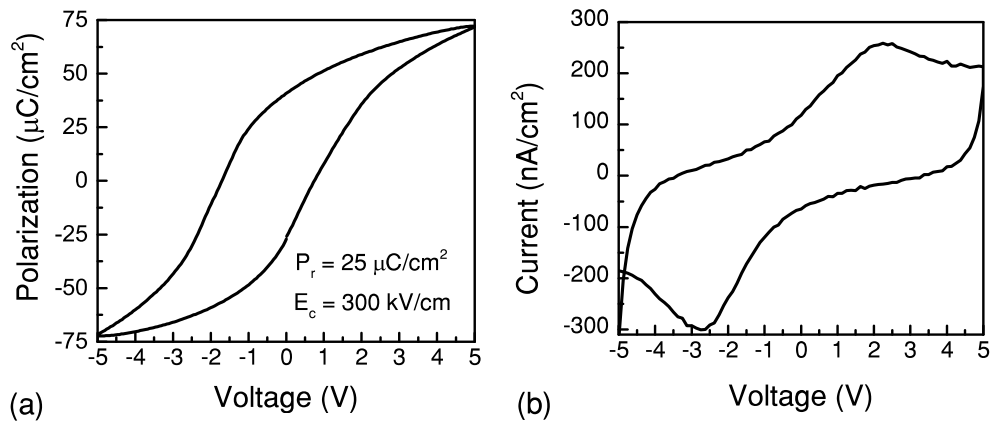


Figure 3.5 – Polarization (a) and current (b) hysteresis loops of the PZT capacitor.

3.2.2 Silicon-doped HfO₂

Silicon doped HfO₂ thin films were recently discovered to enable the CMOS compatible manufacturing of ferroelectrics [123, 124]. The origin of this ferroelectricity attributed to the formation of non-centrosymmetric orthorhombic phase, which is found to be stabilized preferably by crystallization of the as-deposited amorphous dopant(Si):HfO₂ thin films in the presence of a top TiN electrode [125]. In comparison to popular perovskite ferroelectrics such as Pb(Zr,Ti)O₃ (PZT) and SrBi₂Ta₂O₉ (SBT), HfO₂-based ferroelectrics offer distinct advantages including CMOS compatible fabrication process with atomic-layer-deposition (ALD), relatively low dielectric constant, possibility to adoption of industrial gate electrodes, and appropriate remanent polarization [124, 60].

The silicon-doped HfO₂ film was deposited using atomic layer deposition (ALD) on silicon wafers covered by 10 nm of TiN as the bottom electrode of capacitors. The precursors were tetrakis(ethylmethylamino)hafnium (TEMAHf) for Hf and SiH₂(N(C₂H₅)₂)₂ (SAM24) for SiO₂. Ozone and water were used as the oxygen source. The deposition temperature was 300° C and the silicon concentration has been defined by the cycle ratio of SiO₂ and HfO₂. A 10 nm TiN capping layer was deposited by sputtering technique at the room temperature on the oxide film prior to rapid thermal annealing (RTA) at 800° C for 20 s in a nitrogen ambient. The Metal-Insulator-Metal capacitor was completed by the deposition of 50 nm of Pt as the top electrode. The Pt layer was patterned using a lift-off process. Then the top TiN was removed by a wet etching process, using RCA1 solution.

The structure of Si:HfO₂ capacitors is depicted in Figure 3.6 (left) where the ferroelectric film is placed between a sandwich of TiN (10 nm) and a 50 nm thick top Pt electrode. The film has a thickness of 13.2 nm and a Si concentration of about 3.4%, which was found to be the optimized Si% in terms of remanent polarization and leakage [126, 62]. The detail of the fabrication process and optimization steps of Si:HfO₂ is

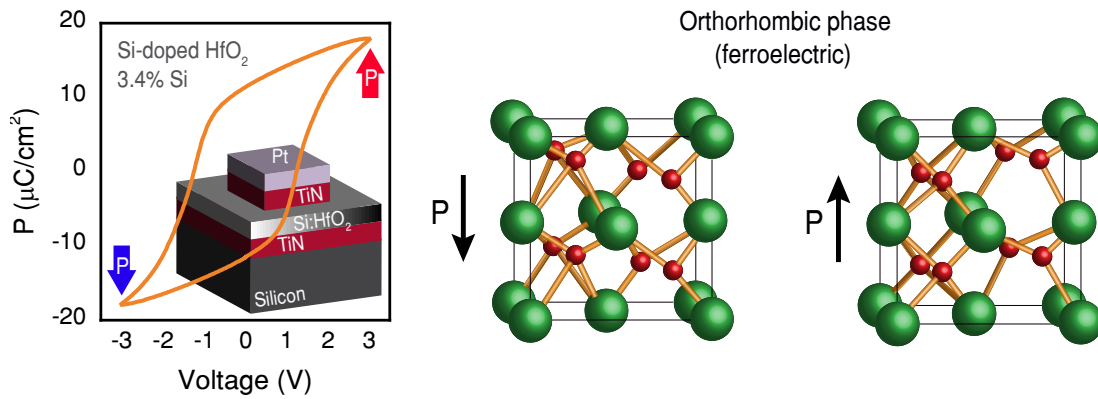


Figure 3.6 – Ferroelectricity of the CMOS compatible ferroelectric, Si:HfO₂. P-V curve (left) that is measured through the top electrode of the Si:HfO₂ capacitor, having a thickness of 13.2 nm and a Si concentration of 3.4 %. The right image shows the crystal structure of HfO₂ in the orthorhombic phase and its two stable polarization state.

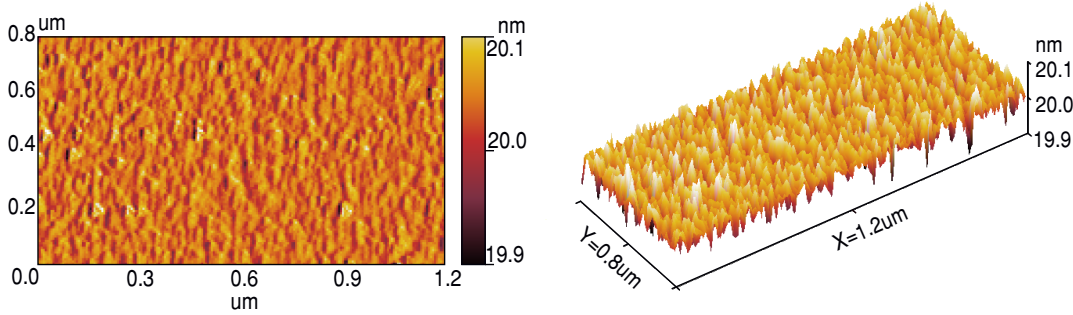


Figure 3.7 – AFM results on the surface of Si:HfO₂ confirms the conformality that was expected from the ALD technique.

presented later in this chapter. The crystal structure of the two stable polarization states of the ferroelectric Si:HfO₂, orthorhombic phase, is schematically shown in Figure 3.6 (right). The atomic-force-microscopy (AFM) of the surface of Si:HfO₂ film confirms the conformality that was expected from the Atomic Layer Deposition (ALD) technique, having a variation of less than 0.1 nm (Figure 3.7).

Essential prerequisites for ferroelectric layers suitable for exploiting the NC effect include sharp and coherent switching and weak intrinsic leakage. In order to evaluate ferroelectricity in the Si:HfO₂ layer in the nanometer scale, we measured local polarization switching and mapped the polarization domain structure using the off-resonance piezoelectric force microscopy (PFM). The technique has been enhanced for probing extremely weak electromechanical coupling typical for thin HfO₂-based films with an outstanding sensitivity < 0.1 pm.

For most device-relevant data, the local piezoelectric response was detected through

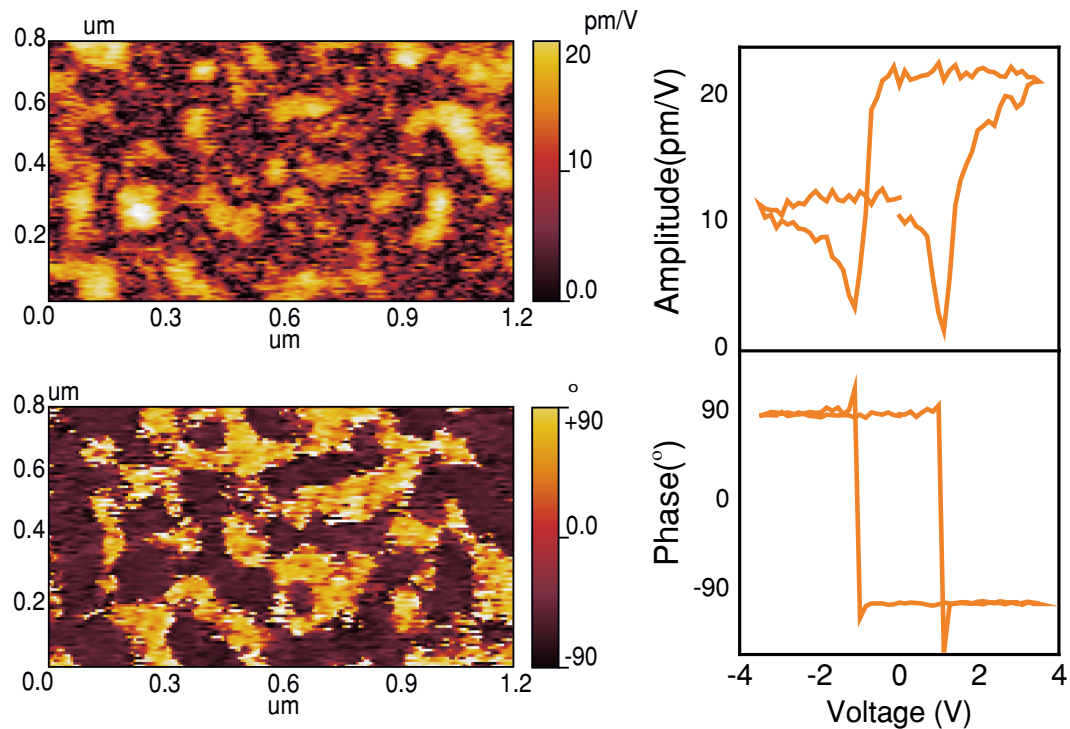


Figure 3.8 – Maps of amplitude and phase of the local piezoelectric response reveal a polarization domain pattern typical for good quality polycrystalline ferroelectrics (left). The loop of the transverse piezoelectric coefficient d_{33} through the top electrode shows that the polarization switches in a sharp, complete and saturated way.

the top electrode, using a sub-coercive AC driving signal of 0.5 V/92 kHz. The resulting maps of amplitude and phase of local piezoelectric response (Figure 3.8) reveal a sharp polarization domain pattern expected for good quality polycrystalline ferroelectric layers. The loop of transverse piezoelectric coefficient d_{33} measured through the top electrode (right) shows that the polarization switches under voltage in a sharp, complete and saturating way, with the coercive voltage close to 1 V. An abrupt 180° flip of the phase of local piezoelectric signal observed at the coercive voltage indicates that the leakage conduction is relatively low and does not affect the measurements. The use of low leakage ferroelectrics is crucial for the NC effect because the leakage causes intrinsic polarization screening and therefore inhibits the conditions required for NC regime.

For switching performance of polycrystalline ferroelectric films, the grain boundaries often represent a critical issue. Charged defects accumulated at the grain boundaries can block propagation of polarization domains and/or pin the domain walls resulting in a domain pattern that closely follows the grain structure. The PFM data in Figure 3.8 suggests that the grain boundaries in the studied Si:HfO₂ layer do not obstruct the switching process. This is confirmed by the size of polarization domains of 50-300 nm, which incorporate many grains of Si:HfO₂ with an average size of about 25 nm.

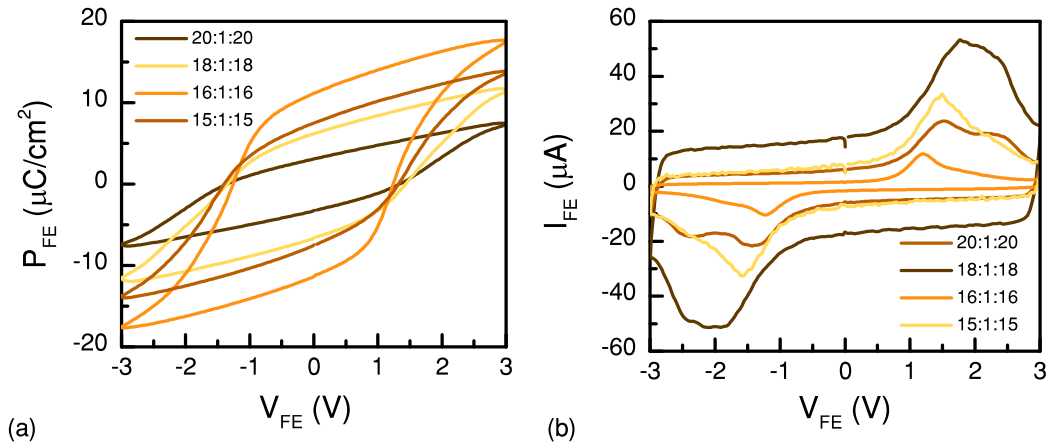


Figure 3.9 – Impact of Si% on the polarization characteristic of Si:HfO₂. The Si% is varied by the cycle ratio of HfO₂ and SiO₂. The legend is depicted in correspondence to the HfO₂:SiO₂:HfO₂ cycle ratio. The 16:1:16 condition (silicon concentration of 3.4%) provides the highest level of remanent polarization. Results are reported for capacitors with an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$ and a thickness of about 13.2 nm.

The sharp boundaries between the polarization domains attest to the homogeneous ferroelectric phase, without any visible inclusions of secondary non-ferroelectric phase earlier reported in HfO₂-based ferroelectric films [123, 125]. Thus the PFM analysis suggests that the structural features of the ferroelectric film do not significantly disturb the uniform polarization response required for the NC effect.

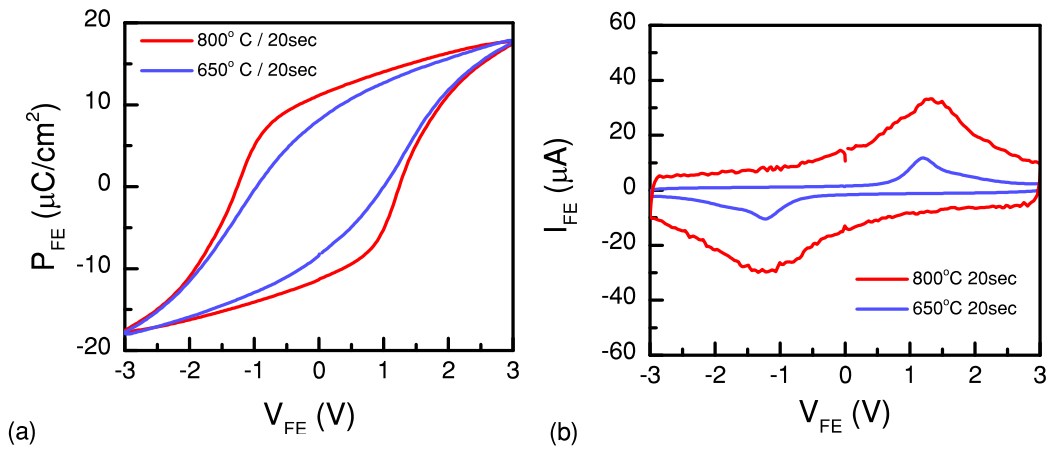


Figure 3.10 – Effect of the annealing temperature on the ferroelectric properties of Si:HfO₂. A higher annealing temperature provides a higher level of ferroelectric polarization and a greater amount of leakage current. Results are reported for capacitors with an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$ and a thickness of about 16.5 nm.

The fabrication process of the silicon-doped HfO₂ is optimized by varying the silicon concentration (Figure 3.9), annealing temperature (Figure 3.10), and the film thickness (Figure 3.11) to ensure a sufficient remanent polarization together with a relatively

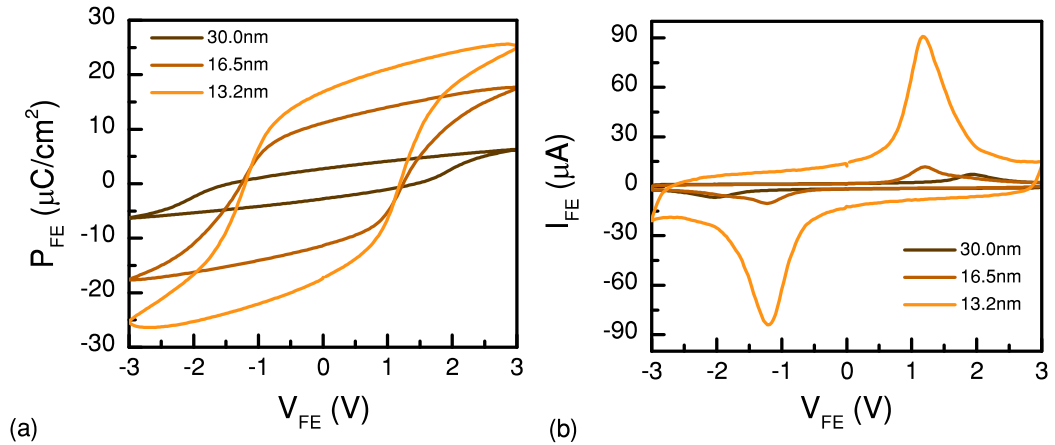


Figure 3.11 – Impact of the layer thickness on the properties of Si:HfO₂. By increasing the thickness the crystallized portion of Si:HfO₂ reduces and hence, the remanent polarization. The leakage current decrease by increasing the thickness as our expectation. Results are reported for capacitors with an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$.

low leakage current. Figure 3.9 shows the impact of the silicon concentration on the polarization characteristic of Si:HfO₂, having a thickness of 13.2 nm. The Si% has been defined by the cycle ratio of HfO₂ and SiO₂, i.e. HfO₂:SiO₂:HfO₂. The cycle ratio of 16:1:16, leading to a silicon concentration of 3.4%, shows a higher remanent polarization and a better ferroelectric response comparing other cycle ratios. It should be noted that the rest of the fabrication process was identical. It is also evidenced that the optimized concentration of 3.4% provides lower leakage/switching current comparing other Si% concentrations. Increasing or decreasing the Si% from the noted value degrades the polarization response of the Si:HfO₂ thin film.

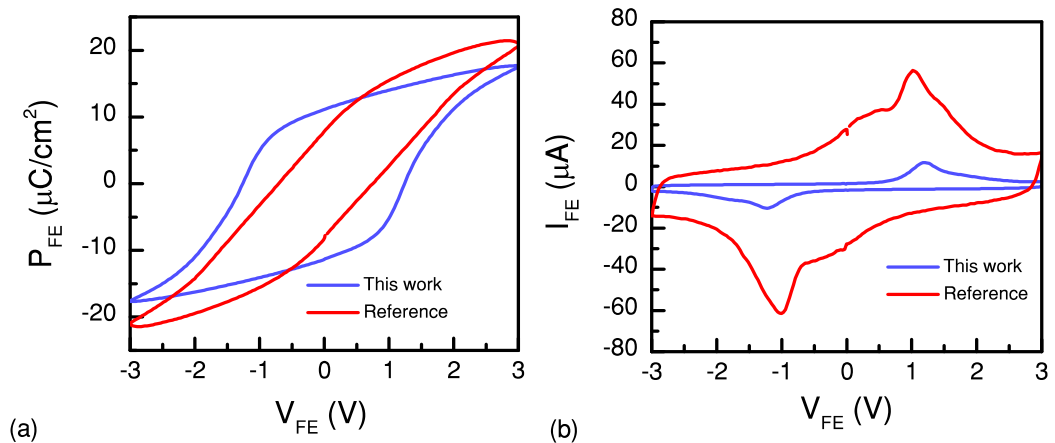


Figure 3.12 – The optimized conditions of Si:HfO₂ in this work is compared with the previously reported results, showing a similar remanent polarization and a relatively lower leakage. Results are reported for capacitors with an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$.

Figure 3.10 illustrates the effect of the annealing temperature on the ferroelectric

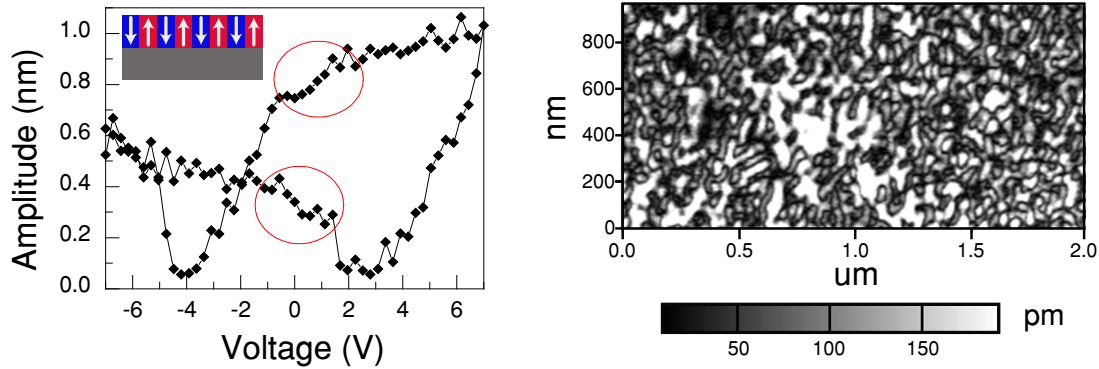


Figure 3.13 – Piezoelectric response of the as-fabricated PZT thin film, illustrating a broad distribution of nucleation energies and coercive fields.

behavior of silicon doped HfO_2 . It is validated that a higher annealing temperature, 800°C comparing to 650°C , leads to a higher level of remanent polarization together with a higher leakage current. Any annealing temperature superior to 800°C causes a large amount of leakage current and hence, the P-V loop of the ferroelectric could not be measured. On the other hand, a Si:HfO_2 thin film annealed at a temperature lower than 600°C shows a lower remanent polarization.

The impact of the layer thickness on the P-V curve of Si:HfO_2 is demonstrated in Figure 3.11, degrading the ferroelectric properties by increasing the thickness. This is due to the fact that a lower portion of HfO_2 gets crystallized in a thicker film. Figure 3.12 compares the P-V curve of a Si:HfO_2 that is fabricated with the proposed optimized conditions of this work and previous reports [60, 125, 62].

3.2.3 Training procedure of ferroelectrics

Generally, the high-quality epitaxial ferroelectric layers are considered suitable for NC devices [109] as they are more likely to form a mono-domain state characterized by a single coercive field. This is in contrast with the typical behavior of the polycrystalline films, which tend to form complicated poly-domain patterns with a broad distribution of nucleation energies and coercive fields (Figure 3.13).

In this section, we show that this behavior can be changed dramatically by applying a repetitive bipolar voltage stress known as the “training” procedure of ferroelectrics. Piezoelectric loops measured through the top electrode of the PZT capacitor after 20 cycles at $\pm 7\text{V}$ show sharp switching and nearly constant piezoelectric response amplitude (Figure 3.14).

This behavior suggests that the poled ferroelectric layer approaches the mono-domain-like behavior. Note that the piezoelectric loops collected on the as-fabricated capacitor

3.3. Capacitance matching and hysteresis tuning

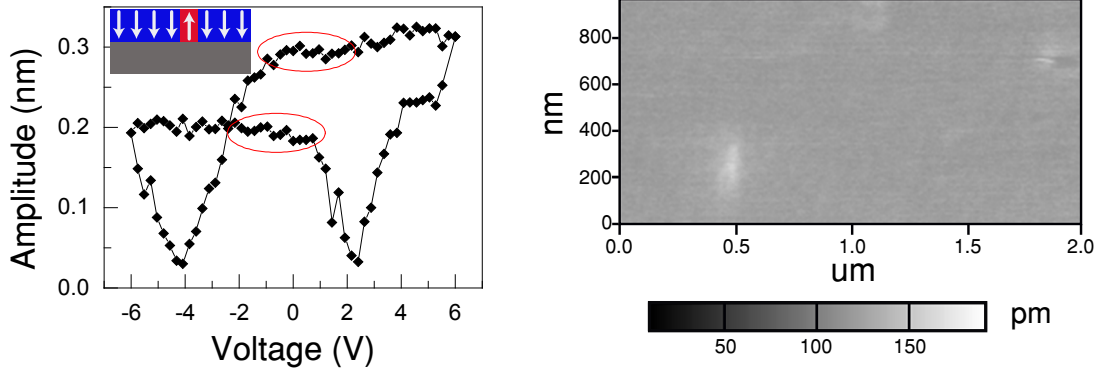


Figure 3.14 – Piezoelectric response of the PZT thin film after the training procedure of ferroelectric, representing the mono-domain like behavior of the poled PZT after 20 cycles at ± 7 V.

without any training reveal a different behavior typical for region-by-region poly-domain switching expected from a polycrystalline film. The demonstration of NC effect using a polycrystalline ferroelectric layer constitutes a significant step towards the integration of NC gates in CMOS technology. In fact, fabrication of epitaxial perovskite layers on silicon is an extremely challenging task, whereas polycrystalline ferroelectrics like PZT can be integrated, as shown in previous reports [127, 38].

3.3 Capacitance matching and hysteresis tuning

As it was previously noted, one may consider an NC-FET as a conventional transistor with an added amplifier. Considering a simple capacitance model (Figure 3.15), the amplification factor of the NC effect can be expressed as

$$\beta = \partial V_{int} / \partial V_g = C_{FE} / (C_{FE} + C_{int}). \quad (3.4)$$

It should be noted that the following conditions are required to provide a sufficient amplification together with a non-hysteretic behavior in an NC-FET: (i) the absolute value of the ferroelectric negative capacitance ($|C_{FE}|$) and the intrinsic gate capacitance (C_{int}) need to be relatively close, and (ii) the total capacitance should remain positive in the whole range of operation; $C_{total}^{-1} = C_{FE}^{-1} + C_{int}^{-1} > 0$. Using the amplification factor, β , the subthreshold swing of an NC-FET, SS_{NC} , can be indicated as:

$$SS_{NC} = \left(\frac{\partial \text{Log} I_d}{\partial V_g} \right)^{-1} = \frac{\partial V_{int}}{\partial \text{Log} I_d} \times \frac{\partial V_g}{\partial V_{int}} = \frac{SS_{ref}}{\beta}. \quad (3.5)$$

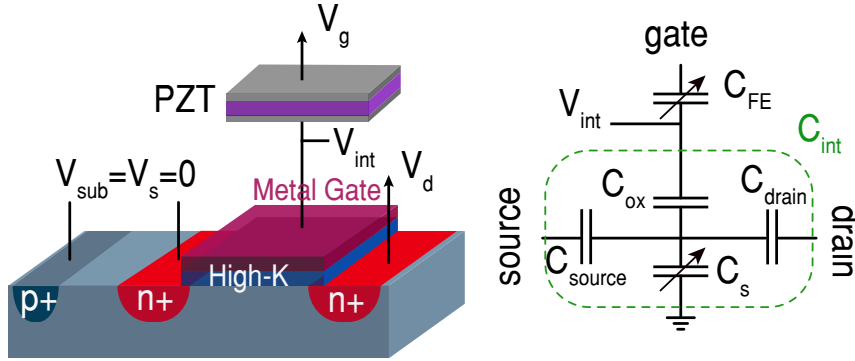


Figure 3.15 – Investigated experimental configuration of the NC-FET (left) and the capacitance model of the structure (right). C_{int} is the total capacitance of the reference MOSFET looking into the gate.

In the subthreshold region, providing an effective NC by the ferroelectric leads to $\beta > 1$ and the SS will be reduced [18]. Large hysteresis, low hysteresis, and also a non-hysteretic NC-FET which fulfills above conditions will be discussed in the following sections.

3.4 Large hysteresis NC-FETs

In this section, hysteretic NC-FETs with a large hysteresis are demonstrated. In this context, we experimentally investigated the impact of the ferroelectric NC on DC electrical behavior of commercial MOSFETs fabricated in 28 nm CMOS technology. The experimental configuration of the NC-FET including the capacitance model of the device is schematically depicted in Figure 3.15, where a PZT capacitor is externally connected to the gate of a conventional MOSFET. Such external electrical connection offers the flexibility of testing tens to hundreds of PZT capacitor values and MOSFETs until the best matching is obtained.

High-performance commercial n -type MOSFETs fabricated in 28 nm CMOS technology have been employed as the reference devices and $\text{Pb}(\text{Zr}_{46}, \text{Ti}_{57})\text{O}_3$ (PZT) is exploited as the ferroelectric material. The experimental setup used for the electrical characterization of NC-FETs is represented in Figure 3.16.

The internal contact is probed (V_{int}) while a voltage is applied to the top gate (a zero current is injected in the internal node). As reported in [74], this probing has a negligible impact on the measurement results of the SS. Agilent 4156C semiconductor analyzer has been employed for electrical characterization of NC-FETs.

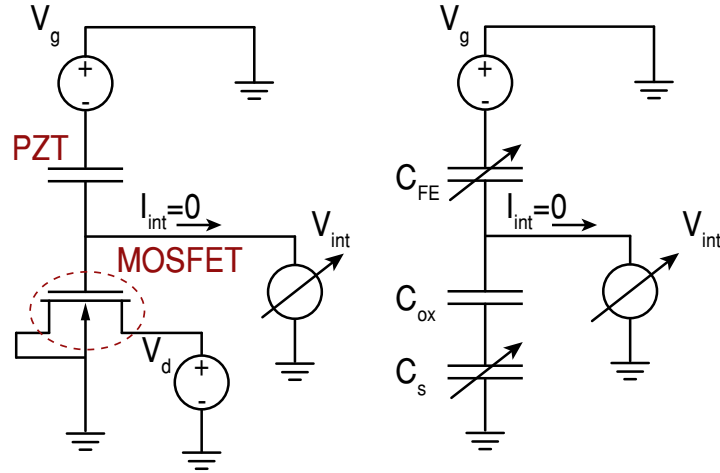


Figure 3.16 – Measurement setup utilized for probing the internal voltage, V_{int} , using an Agilent 4156C semiconductor analyzer.

3.4.1 p-type NC-FET

Figure 3.17-a illustrates the input transfer characteristic of a p-type NC-FET where the gate of a baseline FET ($W=1 \mu\text{m}$, $L=90 \text{ nm}$) is loaded with a PZT capacitor having an area of $40 \mu\text{m} \times 40 \mu\text{m}$. The gate voltage is swept from 3 V to -3 V and back to 3 V while the drain voltage is set to -0.9 V in all measurements performed in this part, otherwise mentioned. In order to decouple the impact of the threshold voltage variation, curves are plotted with respect to the effective gate voltage, i.e. $V_{gs_eff} = V_{gs} - V_{TH}$. This makes the results comparable for different values of the threshold voltage. With the aid of an internal electrode, a step-up conversion of the internal voltage is explicitly observed as a result of the ionic movement in PZT. To qualitatively determine the voltage gain, dV_{int}/dV_g vs. V_{gs_eff} is calculated, representing a significant amplification up to 7 V/V (Figure 3.17-b). This internal voltage increase allows the surface potential to be higher than the gate voltage, leading to a body factor below 1. Therefore, an SS of 10 mV/decade is observed over seven orders of magnitude of the drain current, which is the widest operation range of NC ever reported. The overdrive voltage is also improved by 50% (0.45 V). Using the internal electrode and imposing the displacement vector continuity, a negative slope of the polarization is extracted in a certain range of the polarization. This corresponds to the subthreshold region where a significant boosting of performance is reached.

Imposing the displacement vector continuity, a unique S-shape behavior in the polarization, P , is obtained and illustrated in Figure 3.17-d. The extracted polarization characteristic of the PZT capacitor shows an effective NC over a wide range of the gate voltage during the forward sweep that leads to a significant voltage amplification. It

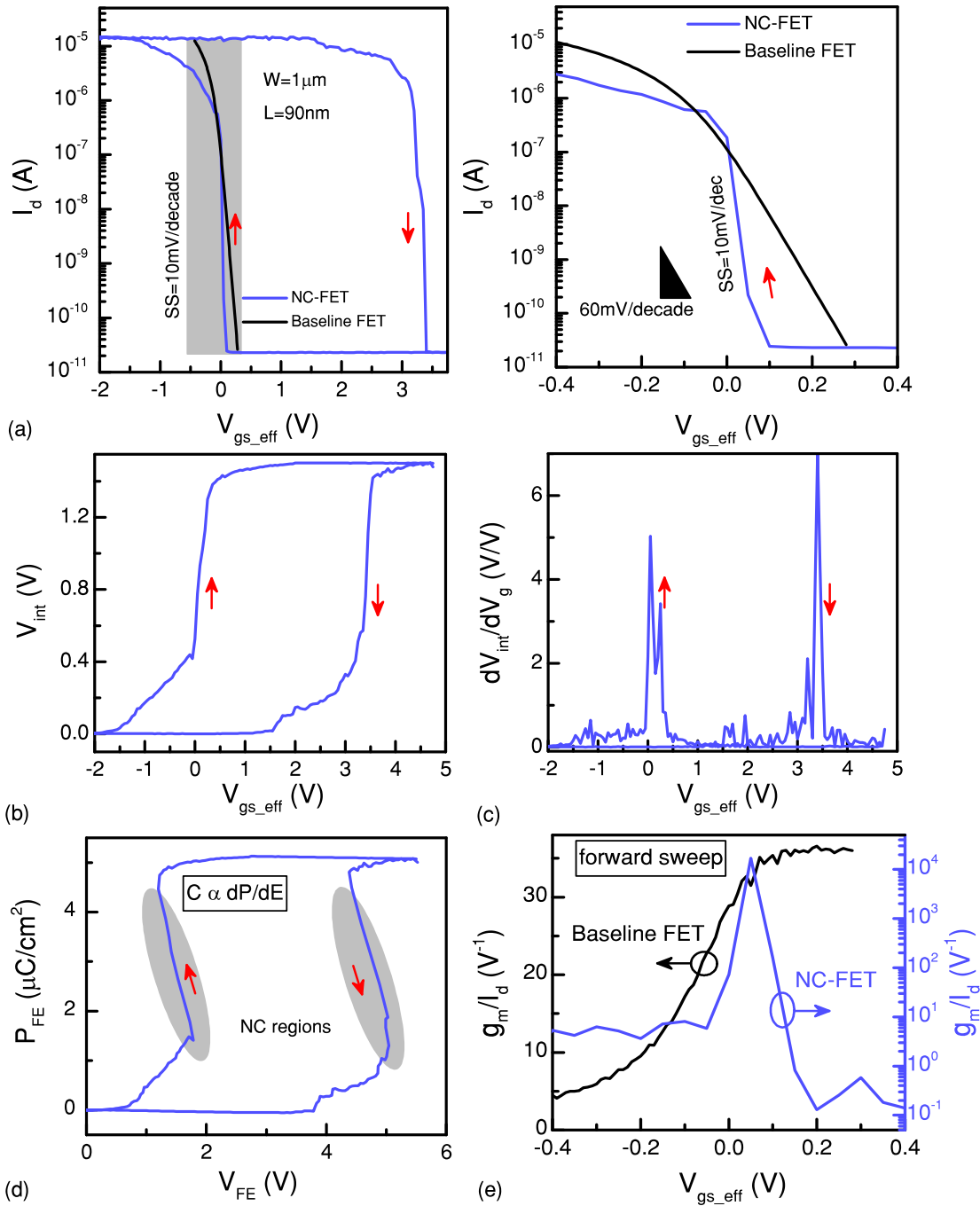


Figure 3.17 – Large hysteresis p-type NC-FET. (a) Transfer characteristic of a p-type NC-FET with a large hysteresis of 3 V ($|V_{ds}| = 900$ mV) and a swing of 10 mV/decade over five decades of current. The internal voltage measurement (b) shows an internal voltage gain (c) greater than one that is measured in both positive and negative going branches. (d) The extracted polarization characteristic of the PZT capacitor during the device operation demonstrates a clear NC region in both branches. (e) Current efficiency factor is also enhanced and reached a factor of 10^5 V^{-1} .

should be noted that due to the charge balance conditions, only a small fraction of the polarization get switched [128] and the results are obtained based on the minor loops. A remarkable enhancement of the current efficiency factor, g_m/I_d , with a peak of 10^4 V^{-1} , is demonstrated when the device is operating in the weak-inversion regime (Figure 3.17-e). A significant improvement of both digital and analog FoM of the reference MOSFET is realized due to the NC effect of the PZT capacitor. The huge gain of NC, resulting in the super steep switching feature, is accompanied by a large hysteresis of 3.5 V as a trade-off [114, 55]. This is attributed to the second term of the RHS of the L-K equation (the third term has a negligible effect), which causes a non-linearity. Hence, to implement NC switches without hysteresis, the ferroelectric and transistor parameters should be chosen wisely to maximize the steepness as well as minimizing the hysteresis [114].

3.4.2 n-type NC-FET

The impact of the same NC booster on an n-type commercial MOSFET is reported in Figure 3.18. The drain-to-source voltage was set at 0.1 V in all measurements performed in this part. Figure 3.18-a depicts the input transfer characteristic of an n-type NC-FET ($W=200 \text{ nm}$, $L=1 \text{ }\mu\text{m}$) using a PZT capacitor ($30 \text{ }\mu\text{m} \times 30 \text{ }\mu\text{m}$) as an NC booster. The gate voltage swept from -3 V to 3 V and returns back to the initial bias by reverse sweep. Using the NC booster, similar to the p-type NC-FET, the internal voltage is enhanced and reached values greater than the applied gate voltage. Therefore, a steep *off-to-on* transition of 10 mV/decade is achieved over at least five orders of magnitude of the drain current. The NC condition is fulfilled in both forward and reverse sweeps so that a similar SS is demonstrated in both branches [129]. Due to the poor matching of capacitances, a large hysteresis of 4.5 V is obtained. Analyzing the internal electrode voltage (Figure 3.18-b) shows a considerable internal voltage amplification in the regions where the ferroelectric capacitor provides a clear S-shape negative slope of the polarization (Figure 3.18-c). An effective NC over a wide range of operation (Figure 3.18-d) ensures a steep *off-to-on* transition together with a significantly enhanced g_m/I_d FoM, reaching a peak of 10^5 V^{-1} (Figure 3.18-e).

The NC-FET operation is hysteretic due to the fact that the $C_{total}^{-1} = C_{FE}^{-1} + C_{int}^{-1} > 0$ is not fulfilled in a wide range of operation. Device characterizations of another architecture with a better matching of capacitances is illustrated in Figure 3.19. A subthreshold swing of 10 mV/decade in the forward sweep (and 20 mV/decade in negative going branch) with a 1.5 V hysteresis is obtained (Figure 3.19-b). The representation of the voltage amplification of this architecture is shown in Figure 3.19-d with $\beta > 1$ in both branches (having a peak of above 12 V/V). The extracted P-V hysteresis of the ferroelectric capacitor clearly demonstrates the negative slope of the polarization, confirming the NC effect (Figure 3.19-e). The g_m/I_d figure of merit if the transistor is significantly enhanced and reached a peak of $2.6 \times 10^5 \text{ V}^{-1}$ (Figure 3.19-f).

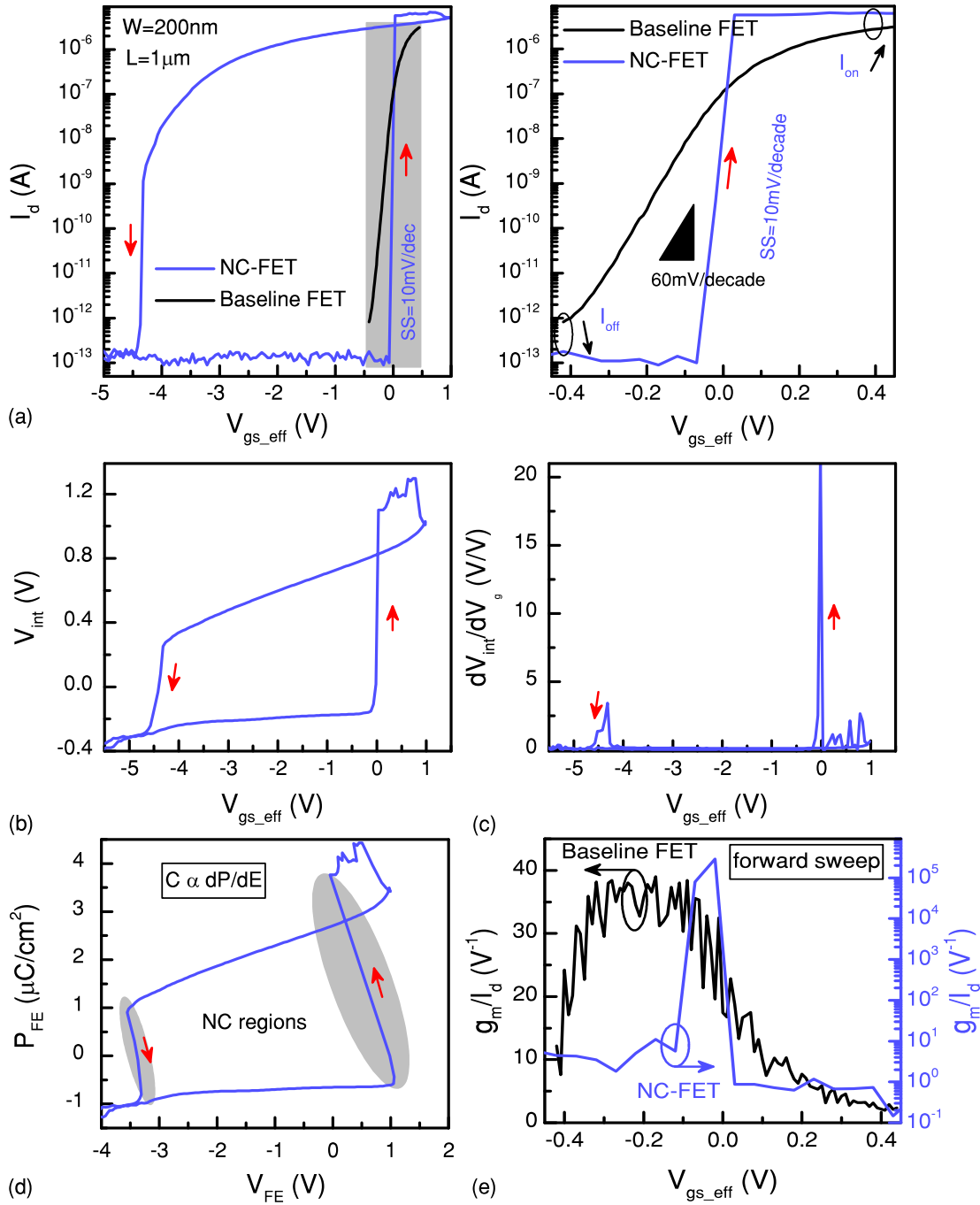


Figure 3.18 – Large hysteretic n-type NC-FET(1). (a) Transfer characteristic shows a super steep transition of 10 mV/decade together with a hysteresis of 4.5 V ($V_{ds} = 100$ mV). By measuring the internal node (b), a remarkable amplification (defined as dV_{int}/dV_g) up to 20 V/V is achieved (c) in the regions corresponding to the negative slope of the polarization. (d) The extracted P-V loop of the PZT capacitor confirms the existence of NC in both branches. (e) The current efficiency factor of the device represents a significant boosting, up to 10^5V^{-1} .

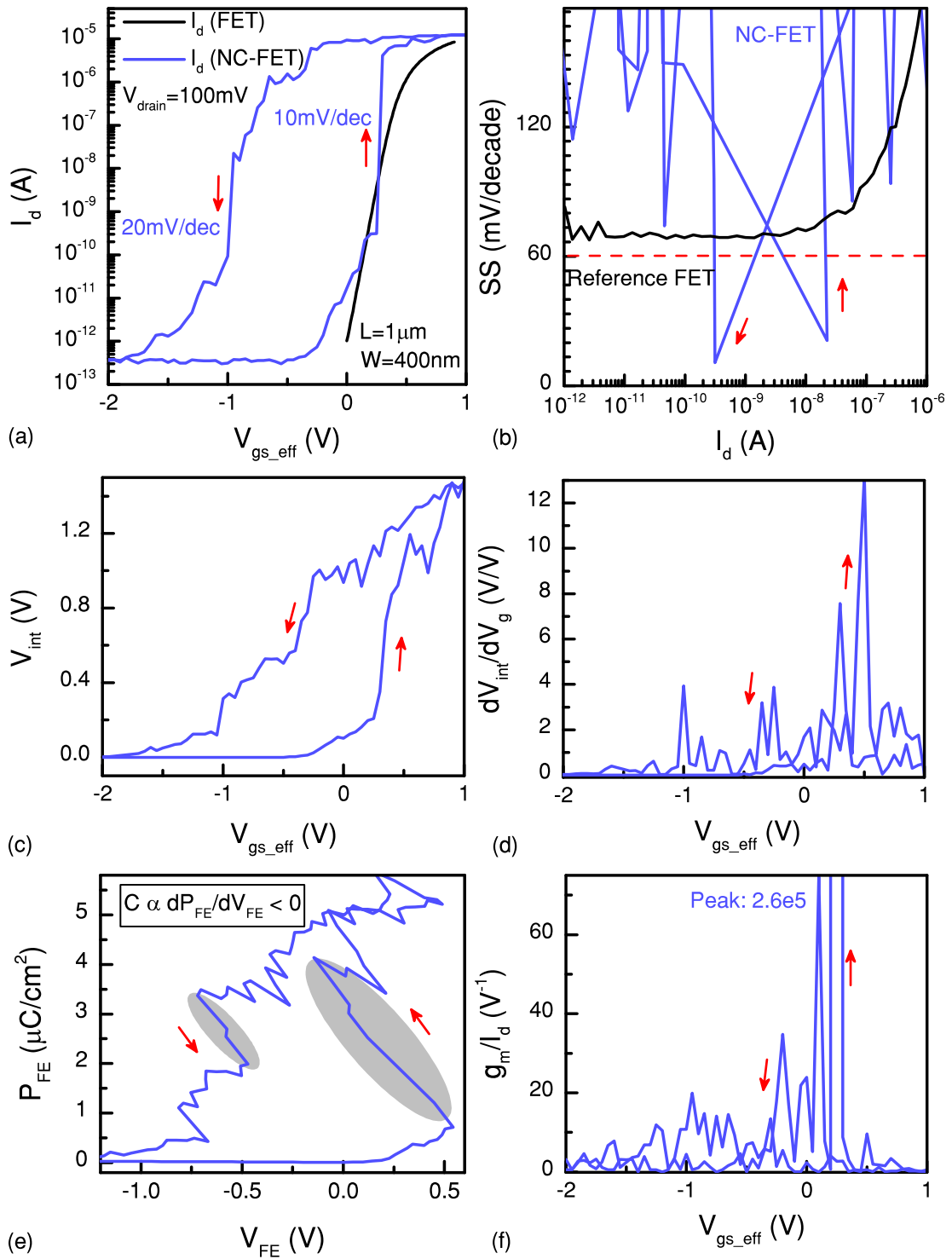


Figure 3.19 – Large hysteretic n-type NC-FET(2). (a) Transfer characteristic shows a super steep transition of 10 mV/decade with a better matching of capacitances (b). By measuring the internal node (c), a remarkable amplification up to 12 V/V is achieved (d) in the regions corresponding to the negative slope of the polarization. (e) The extracted P-V loop of the PZT capacitor confirms the existence of NC in both branches. (e) g_m/I_d FOM of the device represents a significant boosting, up to $2.6 \times 10^5 \text{ V}^{-1}$.

3.5 Low hysteresis NC-FETs

The undesirable hysteretic operation of NC-FETs can be alleviated with a better matching of the ferroelectric and MOS capacitances which ensures the $C_{total} > 0$ stability condition in a wide range of the applied gate voltage [130]. Considering $C_{total}^{-1} = C_{FE}^{-1} + C_{ox}^{-1} + C_{si}^{-1}$, where C_{ox} and C_{si} correspond to the gate linear dielectric and silicon capacitances, the stability condition can be written in a practical way as follows:

$$\left(\frac{S_g}{S_{FE}}\right) < \frac{5\gamma}{4(3\beta^2 - 5\alpha\gamma)} \left(\frac{1}{d_{FE}}\right) \left[\frac{d_{ox}}{\epsilon_{SiO_2}} + \frac{d_{si}}{\epsilon_{si}}\right]. \quad (3.6)$$

In equation 3.6, d , S , and ϵ are the thickness, area, and the permittivity of the corresponding layer, respectively.

In this regard, p- and n-type negative capacitance MOSFETs with a reduced hysteresis are achieved and reported in this section.

3.5.1 n-type NC-FET

In consideration of equation 3.6, another NC-FET with a different baseline FET ($W=100$ nm, $L=1$ μ m) and a PZT capacitor of the same thickness and an area of 20 μ m \times 20 μ m with a better matching of capacitances is demonstrated in Figure 3.20. A reduced hysteresis of 150 mV is observed while the transistor is operating at a constant drain voltage i.e. 0.1 V. An SS below 30 mV/decade at 300° K is reliably achieved in both positive and negative going branches of the input transfer characteristic (see Figure 3.20-b). A possible reason for a steeper transition in the forward sweep, compared to the reverse sweep, can be explained by the asymmetry of the polarization. This occurs due to the difficulty of the dipole flipping during the reverse sweep. Hence, dipoles partially get switched that reduces the impact of NC effect. The SS is below 30 mV/decade over four decades of the drain current. As a result, the effective gate voltage can be reduced by 50%, maintaining the same level of the output current. Figure 3.20-c depicts the internal voltage and internal gain plots (V_{int} vs. V_{gs_eff} and dV_{int}/dV_g vs. V_{gs_eff}), illustrating a remarkable step-up conversion (Figure 3.20-d) [18].

The extracted polarization characteristic of the series connected PZT capacitor (Figure 3.20-e) shows a clear S-shape polarization close to the ideal expectation of NC by L-K equation. A small hysteresis is observed between the forward and reverse sweeps of the gate voltage. The current efficiency factor is also enhanced and reached a maximum value of about 600 V^{-1} (Figure 3.20-f). Although the performance-boosting of the low hysteresis NC-FET in this last case is lower than the large hysteresis one, both analog and digital performances are remarkably enhanced compared to the reference

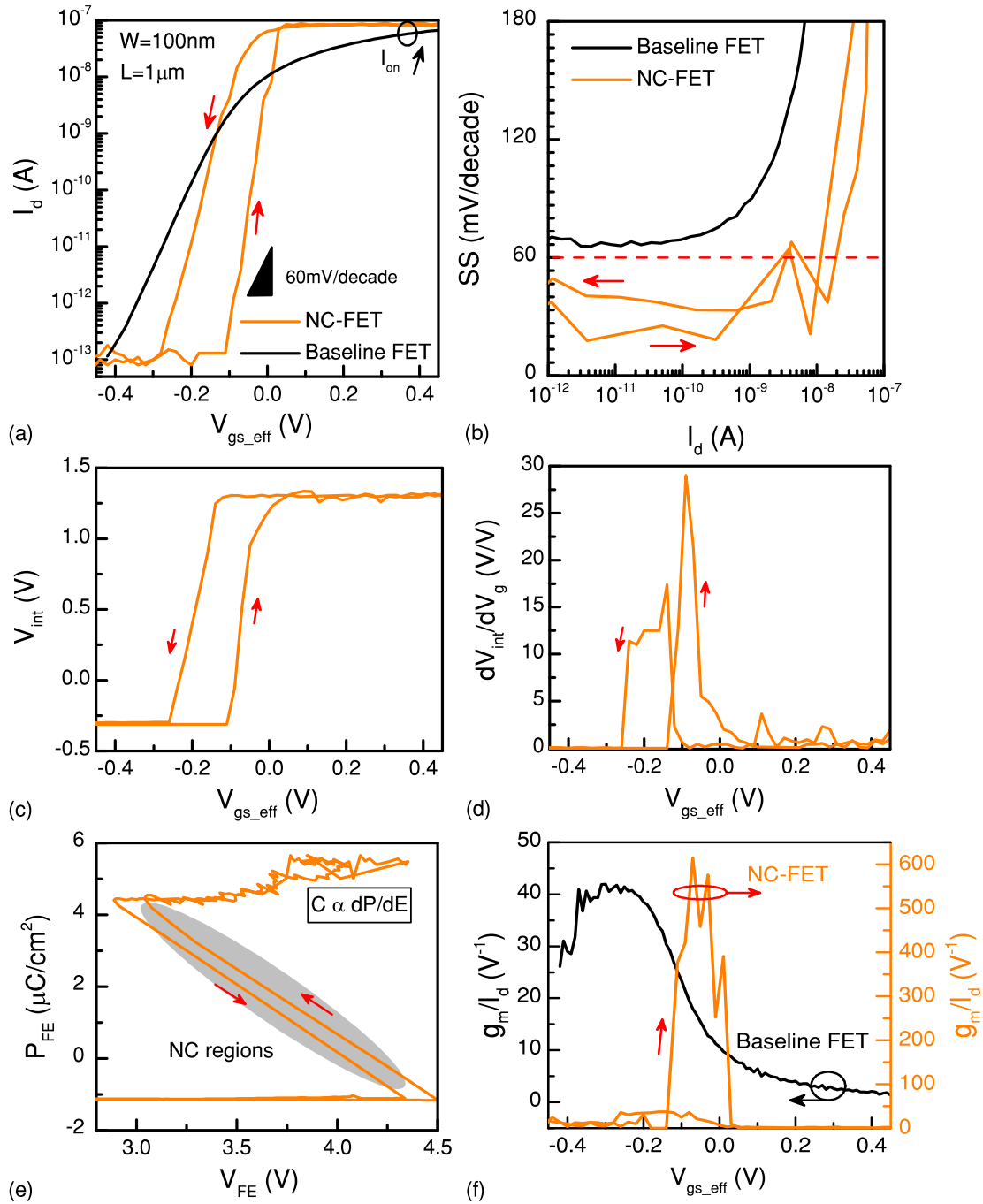


Figure 3.20 – (a) Performance of an n-type NC-FET with a small hysteresis of 150 mV and a swing below 30 mV/decade while V_{ds} is set to 100 mV (b). A step off -to- on transition is realized in both positive and negative going branches of the drain current. (c) Internal voltage measurement shows a voltage gain of up to 25 V/V (d). (e) The extracted P - E curve of the ferroelectric shows a clear S-shape in a wide range of operation with a negligible hysteresis. (f) g_m/I_d is also boosted and reached a factor of 600 V^{-1} .

transistor. This means that a trade-off is required between the hysteretic behavior and the performance-boosting that is caused by the NC of ferroelectric. Generally, considering that the SS can be expressed as $SS = (60 \text{ mV/decade}) \cdot (1 + C_{MOS}/C_{FE})$, the transistor transfer characteristic becomes steep as $|C_{FE}|$ gets close to C_{MOS} . However, a value of $|C_{FE}|$ too close to C_{MOS} gives rise to the hysteretic behavior due to the instability of NC in the strong inversion regime [55].

3.5.2 p-type NC-FET

In a different structure, a p-type NC-FET with a small hysteresis is presented in Figure 3.21. A PZT capacitor with an area of $10 \mu\text{m} \times 10 \mu\text{m}$ is connected to the gate of a p-MOSFET ($W=3 \mu\text{m}$, $L=1 \mu\text{m}$). A small hysteresis of 200 mV is achieved due to the proper capacitance matching. Figure 3.21-b reports the SS vs. I_d plot which is well below the thermal limit of MOSFETs (down to 20 mV/decade) at 300°K . The internal node measurement confirms a voltage gain greater than 1 while having a peak of 10 V/V (Figure 3.21-d). The polarization vs. voltage plot of the PZT capacitor indicates a clear S-like curve in the positive going branch while it shows a different behavior in the reverse sweep (Figure 3.21-e). The ferroelectric performs two separate NC regions, demonstrating a zig-zag polarization characteristic. This mainly happens: first, due to the fact that the polycrystalline PZT is showing two main polarization domains and second, a multi-domain ferroelectric capacitor in steady states cannot hold more than one negative capacitance domain at a time [115, 131]. As a result, the manifested polarization characteristic of the multi-domain ferroelectric is different from the S-shaped curve, which is expected for a single-domain ferroelectric. Therefore, each domain shows a separated NC region. This was also expected from dV_{int}/dV_g vs. V_{gs_eff} curve where two individual peaks of the voltage amplification were clearly observed. The equipotential connections by metal layers at the top and bottom surfaces of the ferroelectric capacitor are key parameters, preventing a multi-domain ferroelectric to exhibit the S-shaped $P_{FE}-V_{FE}$ ($Q_{FE}-V_{FE}$) curve expected from single domain ferroelectrics. Thus, a direct deposition of the ferroelectric on top of the gate oxide on semiconductor and reducing the area of the ferroelectric solve the addressed issue. Figure 3.21-f illustrates the current efficiency enhancement with a maximum value of 400 V^{-1} .

The presented experimental results confirm the same impact and behavior of NC on both n- and p-type MOSFETs. Therefore, NC can be applied as an effective performance booster of CMOS with similar considerations for both types of transistors.

Figure 3.22 investigates the impact of the drain-to-source voltage, $|V_{ds}|$, on the input transfer characteristic of the same NC-FET. Besides the common effect of V_{ds} on the level of the drain current, it is evidenced that the NC-FET under higher lateral electric field performs a wider hysteresis window. In fact, the hysteretic behavior can be dramatically controlled by the drain voltage as the charge and MOS capacitances vary with V_{ds}

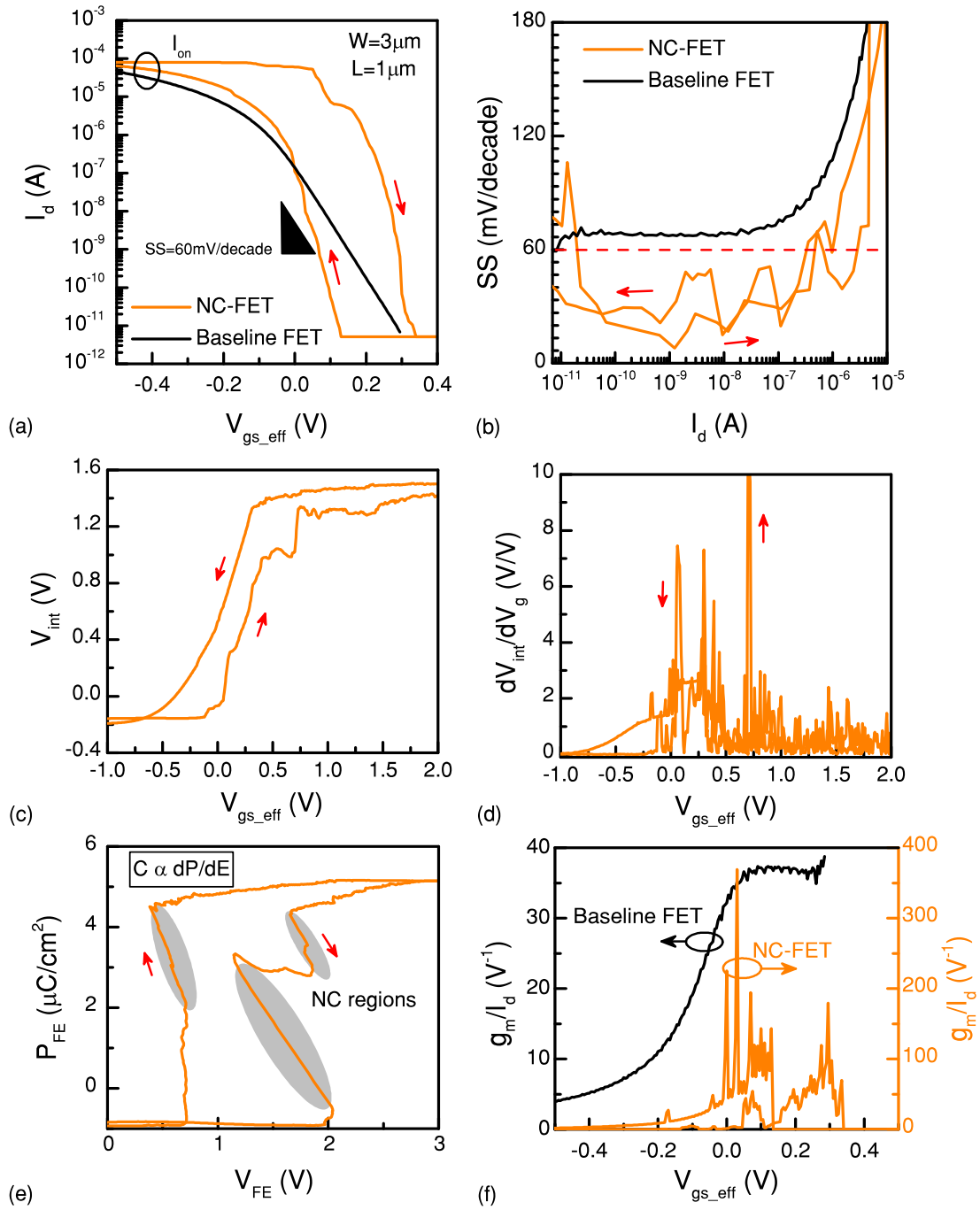


Figure 3.21 – p-type NC-FET with a reduced hysteresis. (a) Input transfer characteristic of an NC-FET with a small hysteresis of 200 mV at $|V_{ds}| = 900\text{mV}$. (b) A sub-threshold swing well below 60 mV/decade is obtained. (c) Measurement of the internal node shows a significant voltage gain, having a peak of 10 V/V. (d) Polarization characteristic of the ferroelectric capacitor shows an effective NC in both branches. Two discrete NC regions are observable in the reverse sweep of the gate voltage due to the polycrystallinity of the ferroelectric film. (e) g_m/I_d is considerably enhanced and reached a value of 400V^{-1} .

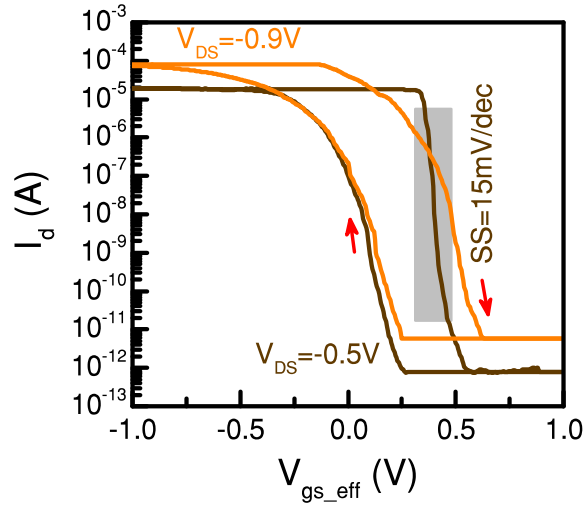


Figure 3.22 – Impact of the drain-to-source electric field on the steepness and hysteresis of the reported NC-FET in Figure 3.21.

[129]. Moreover, the shape of the polarization curve is dictated by relative magnitudes of MOS and ferroelectric capacitances, meaning that the hysteresis can be tuned by V_{ds} . Additionally, it is observed that the steepness of the *off-to-on* transition also changes with the drain voltage. An SS of 15 mV/decade is observed at a lower $|V_{ds}|$ of 0.5 V. In a ferroelectric MOS transistor, the ferroelectric polarization charge density and the channel charge density should match. Therefore, the operation point of the NC-FET is determined by the cross point of the P-E curve and the channel charge load line which depends on the drain voltage. Hence, changing the V_{ds} affects the operation point of the NC-FET and boosting effect of NC.

3.6 Hysteresis-free NC-FET

Due to the relatively small intrinsic gate capacitance of commercial MOSFETs, the full capacitance matching between PZT capacitors and MOS capacitors is challenging. The impact of the non-hysteretic negative capacitance on DC electrical characteristic is schematically demonstrated in Figure 3.23.

Here, we fabricated MOSFETs on an SOI silicon wafer in relatively large dimensions, fulfilling the condition for the non-hysteretic negative capacitance effect. The devices are built on a *p*-type SOI substrate with 88 nm of epitaxial silicon and 145 nm BOX. A cycle of dry oxidation plus HF-based etching is used to thin down the Si layer to 30 nm, improving the gate electrostatic control. After the source and drain phosphorus implantation and annealing, the FET body is shaped using photolithography and selective plasma etching. HfO_2 with 3 nm thickness has been deposited by ALD on an ultra-thin layer of SiO_2 as the gate dielectric.

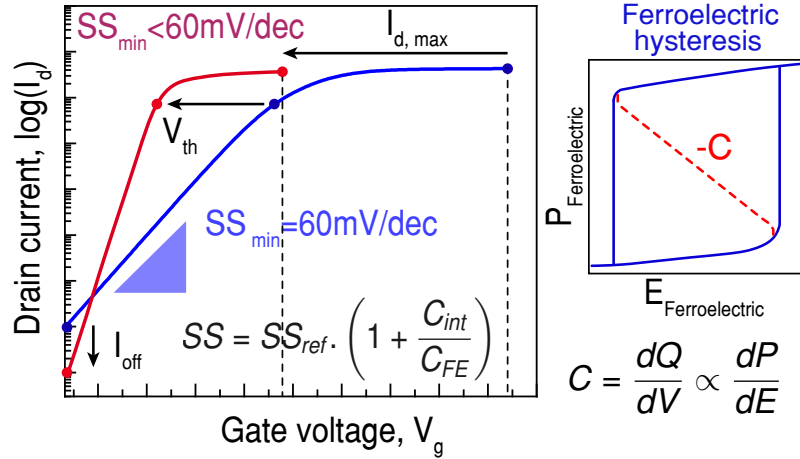


Figure 3.23 – Schematic diagram of the expected transfer characteristic of a non-hysteretic NC-FET versus the base MOSFET highlighting the gain of using the ferroelectric negative capacitance in terms of SS improvement and threshold voltage reduction.

As reported in [132], SiO₂ is used in order to provide a proper interface with the Si channel. Photolithography is used to define the source/drain dielectric openings for electrical contact, which are then created by BHF etching. AlSi1% metal contacts have been created by sputtering and lift-off process. The fabrication process of the baseline SOI MOSFET is schematically depicted in Figure 3.24 together with the Transmission Electron Microscopy (TEM) of the device gate stack and the microscopic image of the transistor array.

In order to obtain the non-hysteretic negative capacitance effect, A 10 $\mu\text{m} \times 10 \mu\text{m}$ PZT capacitor is connected to the gate of a MOSFET, figured out above, with a gate length of 2 μm and a gate width of 19 μm . Figure 3.25-a shows I_d - V_g characteristics of the reference MOSFET and the NC-FET at a drain voltage of 50 mV. The recorded gate leakage confirms that its level is systematically lower than I_{on} and the leakage and charge trapping mechanisms can be neglected in the reported effects. A significant improvement in the SS of the device is obtained when the ferroelectric and gate capacitances are matched so that a non-hysteretic NC operation can be achieved over the whole range of the gate voltage. A sub-thermal swing, down to 20 mV/decade, is observed due to the voltage amplification of the effective NC of ferroelectric (Figure 3.25-b). The internal voltage measurement represents an amplification factor up to 7 (Figure 3.25-d) in the subthreshold region. Figure 3.25-e reports the ferroelectric polarization showing an effective NC in a wide range of the polarization. Figure 3.25-f compares g_m/I_d (g_m is the transconductance) of the NC-FET with the reference MOSFET, indicating a significant improvement in the subthreshold region.

The impact of the drain voltage on the NC effect is exploited in Figure 3.26. By varying the drain voltage changes the operation point of the transistor and hence, the

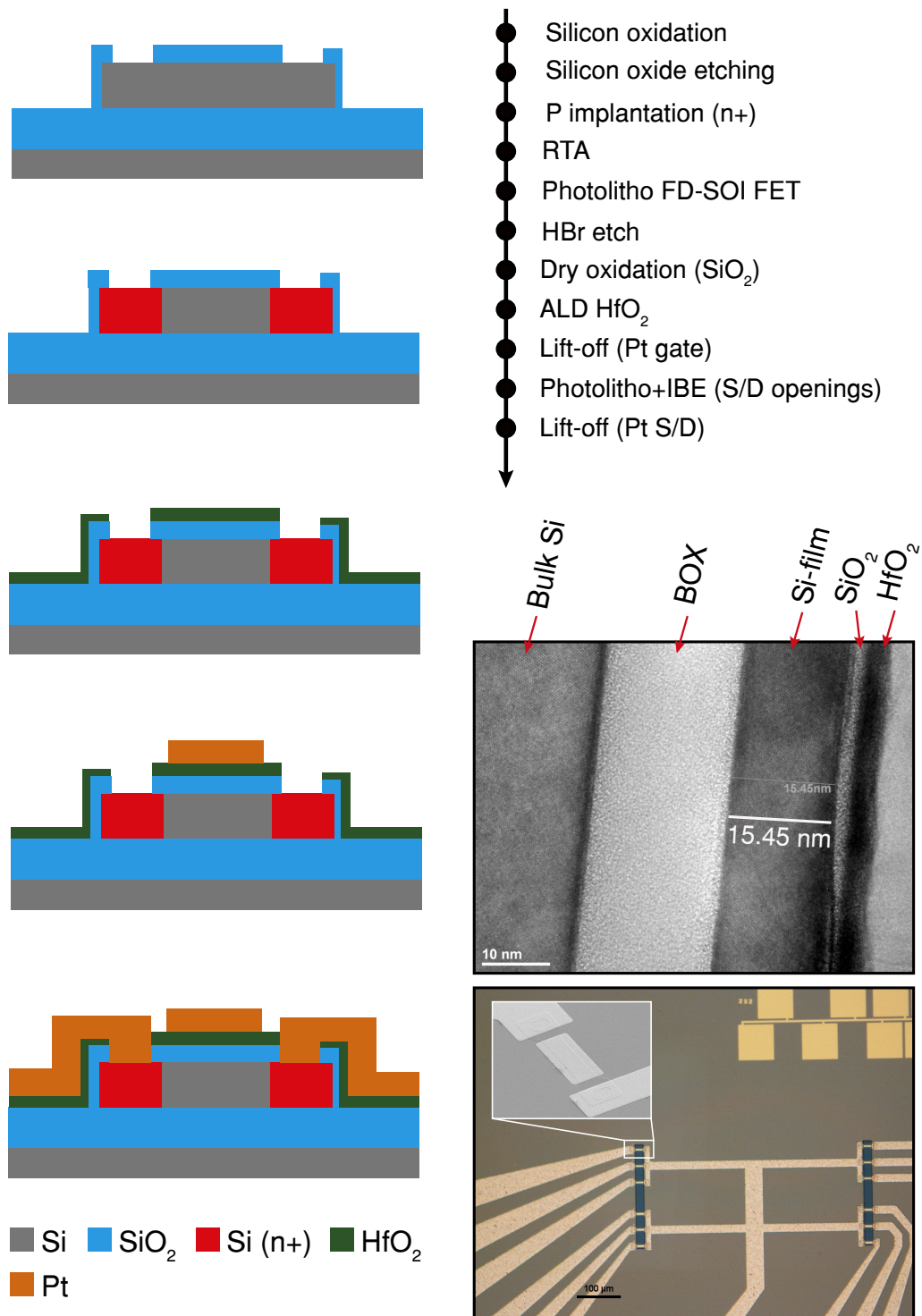


Figure 3.24 – Fabrication steps for the reference SOI MOSFET. The layer thicknesses are shown in the TEM image and the array of transistors in the optical microscope image below.

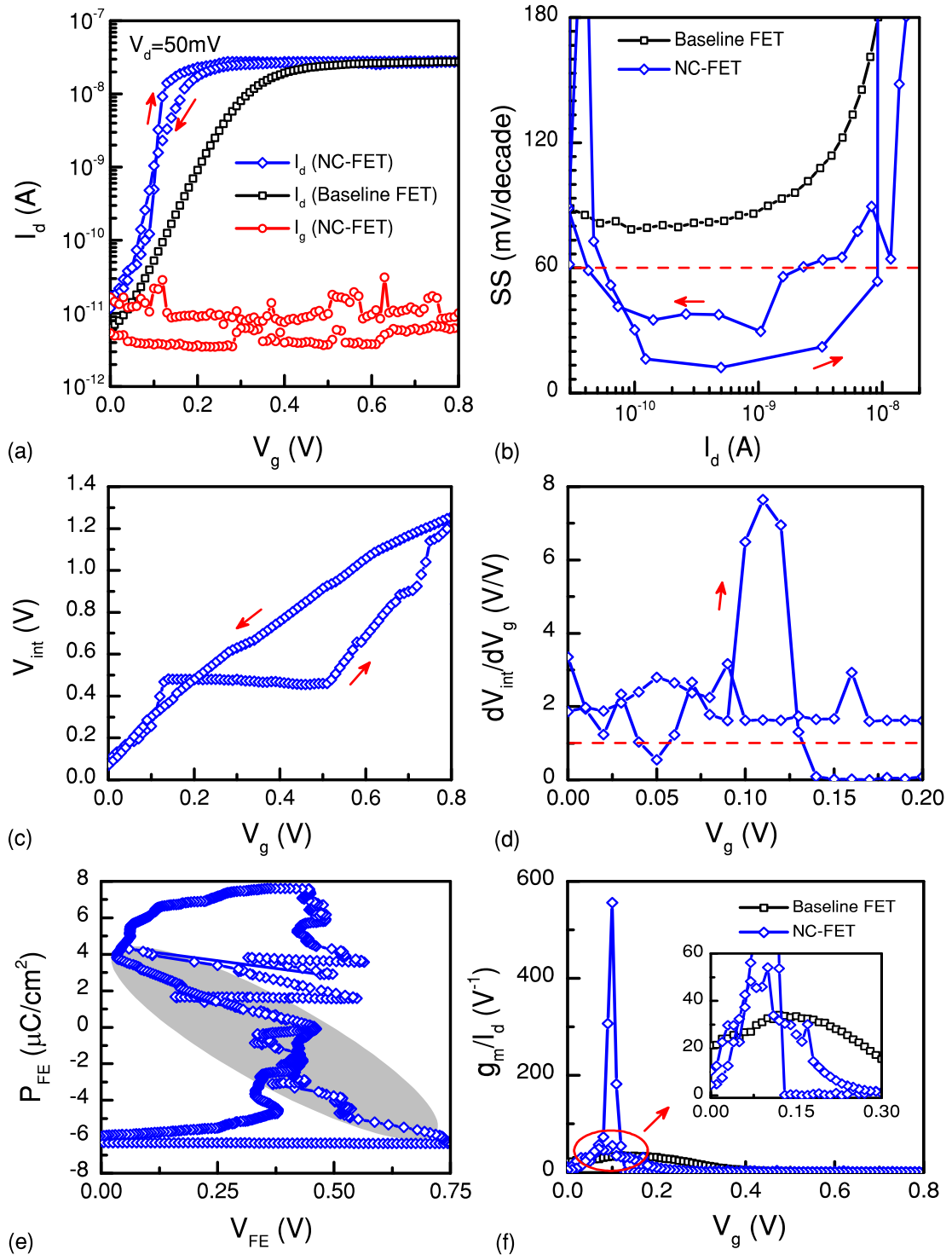


Figure 3.25 – (a) Electrical characteristic of the proposed non-hysteretic NC-FET, showing a sub-thermionic swing down to 20 mV/decade (b). The internal voltage measurement (c) depicts an amplification factor greater than 1 in the subthreshold region (d). The polarization of the ferroelectric demonstrates a negative slope in a wide range of the polarization (e). The calculated g_m/I_d of the NC-FET represents a significant boosting in the subthreshold region of the device (f).

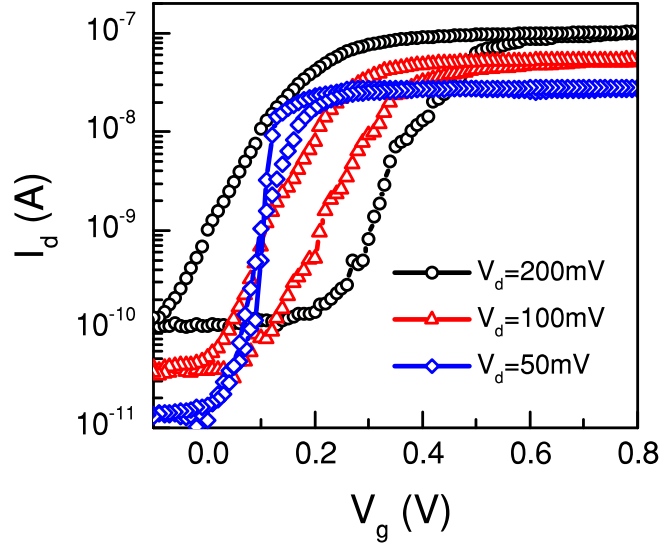


Figure 3.26 – Impact of the drain voltage on the transfer characteristic of the non-hysteretic NC-FET. The increase of the drain voltage degrades the improvement of the NC effect and increases the hysteretic behavior.

intersection of the polarization characteristic of the PZT capacitor with the charge line of the transistor. Here, the increase of the drain voltage leads to a degraded improvement due to the negative capacitance effect. Additionally, increasing the source to drain electric field disturbs the capacitance matching condition and results in a hysteretic behavior.

3.7 Design considerations of ferroelectric properties for Negative Capacitance MOSFETs

Impact of physical parameters of the ferroelectric layer on the performance of NC-FETs is experimentally studied in this section. In this regard, Electrical behaviors of PZT-based and Si:HfO₂-based NC-FETs are investigated and discussed. In a PZT-based p-type NC-FET, a sub-thermal swing down to 20 mV/decade is achieved due to the remarkable voltage gain of NC, reaching a maximum value of 10 V/V. Nevertheless, the performance improvement with the Si:HfO₂ NC booster is significantly lower than the one of PZT. This is due to the coexistence of different phases and also high leakage current which can enormously reduce the enhancement by NC.

First, we experimentally investigate the impact of a PZT capacitor as a commonly used ferroelectric on DC electrical behavior of commercial MOSFETs, fabricated in 28 nm CMOS technology node. The matching condition between the ferroelectric NC and MOS capacitance of the baseline FET is mostly fulfilled, leading to a small hysteresis. A sub-thermal swing down to 20 mV/decade is realized as a result of the internal voltage gain of NC, reaching a factor of 10 V/V. Additionally, results are compared with the

3.7. Design considerations of ferroelectric properties for Negative Capacitance MOSFETs

performance of an NC-FET using the CMOS compatible ferroelectric, Si:HfO₂ [121]. A limited boosting is observed in comparison to the PZT-based NC-FET due to the formation of non-ferroelectric phases in Si:HfO₂ and also its high leakage.

3.7.1 PZT-based NC-FET

We report an experimental NC-FET demonstrated by connecting an external PZT capacitor to the gate of a p-type MOSFET (L=1 μm , W=3 μm), which is previously discussed in Figure 3.21. 46 nm of polycrystalline PZT layer has been deposited via the chemical-solution-deposition route on a Pt-coated silicon wafer. The polarization and current characteristics of PZT are illustrated in Figure 3.5, showing a low switching current in the order of nA/cm². It should be remarked that the leakage current of a ferroelectric capacitor is comparable to its switching current. As it was previously mentioned in this chapter, well-trained ferroelectric capacitors are employed to demonstrate the NC effect.

Here, we shortly re-state the reported results in Figure 3.21 that are the electrical performance of the PZT-based NC-FET compared to its reference transistor ($|V_{ds}|$ is 900 mV). The output transfer characteristic of the NC-FET shows a relatively small hysteresis of about 220 mV as the matching condition between the ferroelectric NC and MOS capacitance is mostly fulfilled [113]. A subthreshold swing well below the thermal limit of MOSFETs, down to 20 mV/decade, is evidenced as a result of the internal voltage gain of NC, reaching values greater than one up to 10 V/V. The P-V curve of the PZT capacitor is obtained by imposing the displacement vector continuity, showing an effective negative capacitance in both forward and reverse sweeps of the gate voltage. The ferroelectric shows two separated NC regions despite the training procedure, which is limiting the performance-boosting of NC effect.

3.7.2 Si:HfO₂-based NC-FET

Another NC-FET configuration, using the same baseline transistor and silicon-doped HfO₂ as the NC booster is demonstrated. A 15 nm layer of Si:HfO₂ (4.3% Si) is deposited with ALD on a TiN coated silicon wafer. A 10 nm TiN capping layer is then sputtered to provide the mechanical stress during annealing (800° C for 20 s). Top Pt electrodes are sputtered and patterned using the shadow masking technique. The TiN layer is removed in a wet etching process. P-V and I-V curves of Si:HfO₂ MIM structure is compared with the ones of PZT in Figure 3.27. A remanent polarization of about 15 $\mu\text{C}/\text{cm}^2$ and a coercive field of 1 MV/cm are measured together with a relatively large switching current (leakage) in the range of mA/cm².

In this last case, a limited boosting of performance is observed when a Si:HfO₂ ferroelectric capacitor is connected to the gate of a conventional MOSFET (Figure 3.28-a). A small yet clear improvement of SS, down to 50 mV/decade, is obtained (Figure 3.28-b).

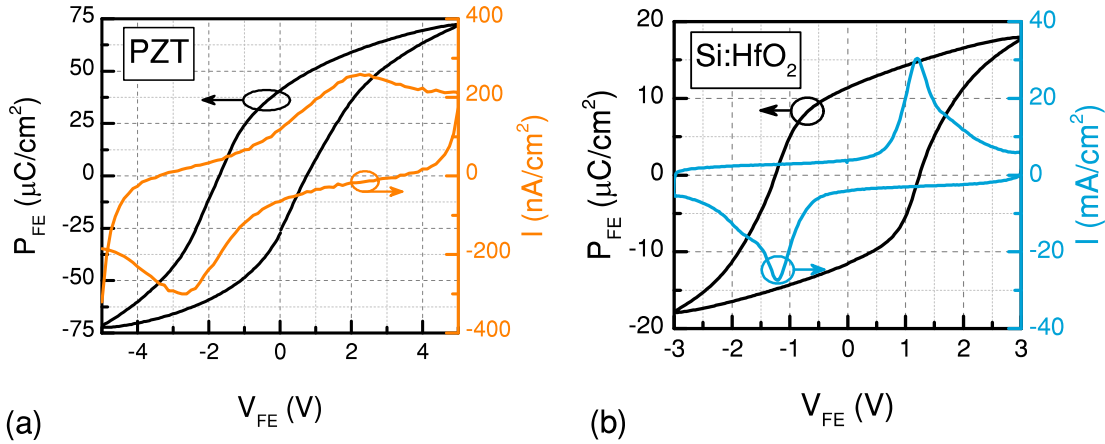


Figure 3.27 – (a) Polarization and current characteristics of the 46 nm thick PZT capacitor. A coercive field of +80 kV/cm; -260 kV/cm and a remanent polarization of ± 30 $\mu\text{C}/\text{cm}^2$ is measured. The capacitor shows a very low leakage current in the order of nA/cm^2 . (b) P-V and I-V characteristics of a silicon-doped HfO₂ ferroelectric capacitor with a thickness of 15 nm and a Si concentration of 4.3%. The coercive field of ± 1 MV/cm and a remanent polarization of about ± 15 $\mu\text{C}/\text{cm}^2$ are extracted together with a relatively high switching current.

The internal voltage measurement shows discrete regions of amplification where β is greater than 1, never exceeding 2 V/V (Figure 3.28-d). This is due to the fact that Si:HfO₂ is not well stabilized and performed discrete regions of NC (Figure 3.28-e). The calculated g_m/I_d figure of merit of the transistor is also demonstrating a limited boosting of performance (Figure 3.28-f).

A stark difference between vigorous NC effect observed on the device with PZT capacitor and a relatively weak effect measured on the device connected to the Si:HfO₂ capacitor implies that the two ferroelectrics operates differently. Unlike PZT consisting of a single tetragonal perovskite ferroelectric phase, doped HfO₂ has several phases coexisting in different portions depending on processing and mechanical, thermal, and electrical conditions [121]. The ferroelectric orthorhombic phase can be promoted by choosing the right dopant and processing conditions. However, other non-ferroelectric phases (mostly monoclinic and tetragonal) cannot be eliminated completely even in the state of the art of this material. The presence of the secondary phase, even in small quantity, may severely impede the formation of a stable mono-domain state, and consequently, deteriorate the NC gate performance [120]. Previous studies indicate a possibility to promote a single phase state by voltage cycling [121]. However, this technique provokes an increase in the leakage, which also undermines the NC effect [123]. Besides that, the high leakage of ferroelectric results in instability of NC in an MFMIS structure [133]. This analysis highlights the importance of further improvements of HfO₂ based ferroelectrics for devices with NC-enhanced gates. Specifically, ferroelectric materials composed of a single ferroelectric phase with a low leakage are required for a strong and stable NC effect.

3.7. Design considerations of ferroelectric properties for Negative Capacitance MOSFETs

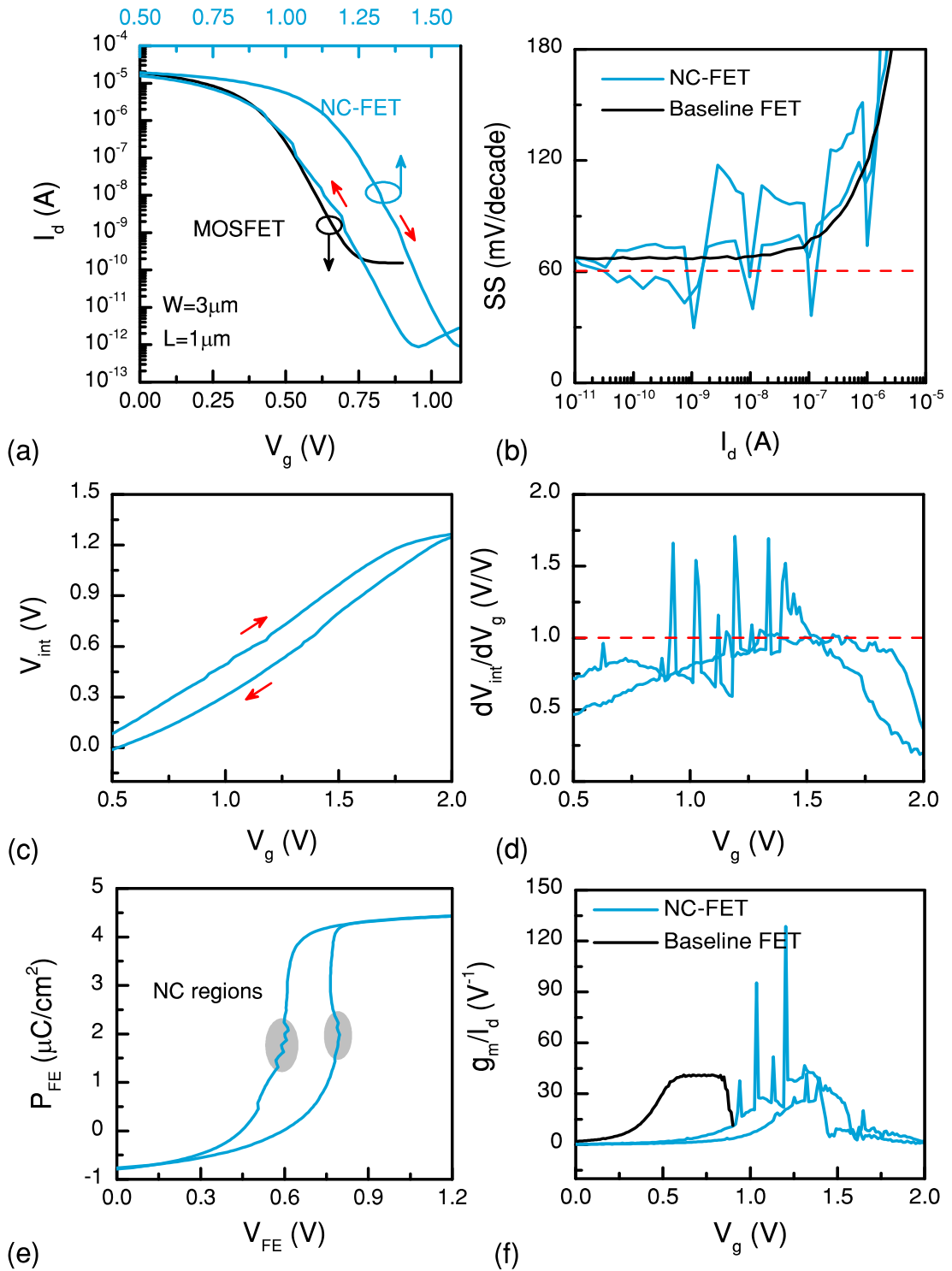


Figure 3.28 – (a) Transfer characteristic of a p-type NC-FET ($L=1\ \mu\text{m}$, $W=3\ \mu\text{m}$) using Si:HfO_2 ($30\ \mu\text{m} \times 30\ \mu\text{m}$), showing a limited improvement is observed in the device performance due to the NC effect ($|V_{ds}|=900\ \text{mV}$). (b) SS is slightly improved and reached a minimum value of 50 mV/decade. (c) Internal voltage measurements show discrete points of amplification with values below 2 V/V (d). (e) P-V plot of the ferroelectric shows multiple small regions of negative capacitance. (f) g_m/I_d FoM is also demonstrating a limited enhancement.

Recent progress in the use of different dopants stabilizing the orthorhombic ferroelectric phase suggests that devices with CMOS compatible ferroelectric NC gates are feasible.

3.8 Summary

In conclusion, it has been shown that the negative capacitance effect can be effectively applied as a universal performance booster to enhance both digital and analog FoM of complementary MOS switches. The measured input transfer characteristics of advanced n- and p-type MOSFETs using PZT as the NC booster shows a steep subthreshold swing down to 10 mV/decade together with an enhanced efficiency factor up to 10^5 V^{-1} . The *on*-current over *off*-current ratio is improved and the overdrive is boosted up to 0.45 V. Therefore, the supply voltage can be reduced by 50%, maintaining the same performance. This is due to the fact that with the aid of a series connected negative capacitor (i.e., with the internal voltage amplification provided by the NC component of the PZT capacitor) the surface potential in MOS devices is increased beyond the applied gate voltage. It has been also demonstrated that the hysteretic behavior of NC-FETs can be tuned considering the proposed stability condition. Both n- and p-type NC-FETs with large (3-4.5 V) and reduced hysteresis windows (150-200 mV) are implemented, arguing that a trade-off is required between the steepness and hysteretic behavior of an NC-FET. A matching condition between the ferroelectric and MOS capacitances is obtained for the non-hysteretic operation in MOSFETs fabricated on SOI substrates leading to a subthreshold swing of 20 mV/decade. The impact of the drain-to-source electric field on the boosting of NC is demonstrated and discussed. Overall, this experimental study proposes and validates that a properly designed ferroelectric capacitor can be employed as a universal performance booster of CMOS transistors by offering an active gate stack, contributing to the signal amplification by improving the surface potential. Additionally, the performance of NC p-type MOSFETs using PZT and Si:HfO₂ is compared. A subthermal swing down to 20 mV/decade is achieved by a significant internal gain of NC up to 10 V/V when PZT is employed as the NC booster. The operation of an NC-FET with CMOS compatible ferroelectric, Si:HfO₂, is also reported and discussed. A limited improvement is observed in this latter case due to the coexistence of different phases and also the high leakage current of silicon doped HfO₂.

4 Negative Capacitance Tunneling Field-Effect Transistors

Abstract:

Subthreshold Swing (SS) of MOSFETs is limited to 60 mV/decade at room temperature by the Boltzmann electron energy distribution. This fundamental limit obstructs the lowering of the supply voltage and hence, the total power consumption. Tunnel FETs avoid this limit by using quantum mechanical band-to-band tunneling (BTBT), rather than thermionic injection, to inject charge carriers into the channel. However, the experimental demonstration of a sub-60 mV/decade swing TFET is extremely challenging. Here, we propose to employ the negative capacitance of ferroelectrics as a performance booster of TFETs. First, we confirm the impact of the ferroelectric's negative capacitance on moderate TFETs with relatively large values of subthreshold swing in both hysteretic and non-hysteretic modes of operation. Then, we report another device configuration using novel InAs/InGaAsSb/GaSb nanowire TFETs with sub-60 mV/decade swing as the baseline TFET. The well-known perovskite ferroelectric, PZT, and the recently proposed CMOS compatible ferroelectric, silicon-doped HfO₂, are investigated as the NC booster. The PZT-based NC-TFET exhibits an SS of 10 mV/decade over three orders of magnitude of the drain current, an enhanced g_m/I_d factor having a peak of 3000 V⁻¹, and an improved I_{ON}/I_{OFF} ratio with a small hysteresis of 500 mV. In another case, using Si:HfO₂ as ferroelectric, an average SS of 30 mV/decade over five decades of current is observed with a negligible hysteresis of 50 mV due to the proper matching of capacitances. Lastly, well behaved InGaAs planar ring TFETs with a minimum swing of 55 mV/decade at room temperature are combined with high-quality single crystalline PZT capacitors. The exact NC matching conditions are satisfied by a single crystalline ferroelectric that can perform a mono-domain state and provides a hysteresis-free NC-TFET. The supply voltage is thereby reduced by 50%, providing the same drive current. The presented results show that NC can open a new direction as a universal performance booster in the TFET design by significantly improving the low I_{60} and low overdrive of TFETs.

4.1 Negative Capacitance as performance booster of Tunnel FETs

Energy efficient logic devices are required for the recent advancements of the Internet of Things (IoT) technology [134, 135]. Modern mobile computing including emerging IoT technologies such as wearables and smart sensor networks demand low-power and large-scale integration systems. The energy efficiency can be evaluated by analyzing the balance of the active ($P_{dynamic}$) and static ($P_{leakage}$) components of the total switching energy. The active power is defined as $P_{dynamic} = CV_{DD}^2 f / 2$, where C is the capacitive load, V_{DD} is the supply voltage, and f is the frequency. As mentioned in previous chapters, the most feasible approach to reduce the active power is reducing the supply voltage (V_{DD}) and the threshold voltage (V_{TH}) accordingly to maintain the same performance. On the other hand [15], the leakage current exponentially increases with the decrease of V_{TH} as $I_{leakage} = (I_d @ V_{gs} = V_{TH}) \times 10^{-V_{TH}/SS}$.

A way of reducing the supply voltage without performance loss and simultaneously deal with the mentioned problem is to increase the steepness of the *off-to-on* transition of the transistor [106]. The steepness of a switch is defined as the minimum gate voltage required for a 10-fold increase in the drain current, known as the subthreshold swing (SS) [136, 137]. The general expression for SS is:

$$SS = \left[\frac{\partial V_g}{\partial (\log_{10} I_d)} \right] = \frac{\partial V_g}{\partial \psi_s} \times \frac{\partial \psi_s}{\partial (\log_{10} I_d)}, \quad (4.1)$$

where ψ_s denotes the surface potential of the semiconducting channel. The first term of the RHS of equation 4.1, known as m-factor (body factor), generally has a value ≥ 1 since V_g is linked to ψ_s through a capacitive voltage divider. The second term (n-factor) has a lower limit of $k_B T / q \ln(10)$, 60 mV/decade at 300° K, in a conventional MOSFET or any device using the carrier injection mechanism over an energy barrier as the operation principle [93]. This limit is a consequence of the thermally broadened Fermi-distribution of carriers which is irrespective of dimensionality or the material in use.

In order to overcome the so-called "Boltzmann Tyranny", steep switching devices such as Tunnel FETs (TFETs) [138, 28], impact ionization MOSFETs (I-MOSFETs) [16, 22], nanoelectromechanical FETs (NEMFETs) [17, 139], and negative capacitance (NC) MOSFETs [38, 35, 18, 140] with a sub-60 mV/decade swing have been extensively studied. Tunnel Field-Effect Transistors (TFETs) have attracted a great deal of attention for achieving a steep subthreshold swing by employing quantum mechanical band-to-band tunneling (BTBT) of carriers from source to the channel (reducing n-factor to values below 60 mV/decade) [141]. The current of a TFET is the integral of the transmission probability, T_{WKB} , of the interband tunneling over the source-channel junction, which

4.1. Negative Capacitance as performance booster of Tunnel FETs

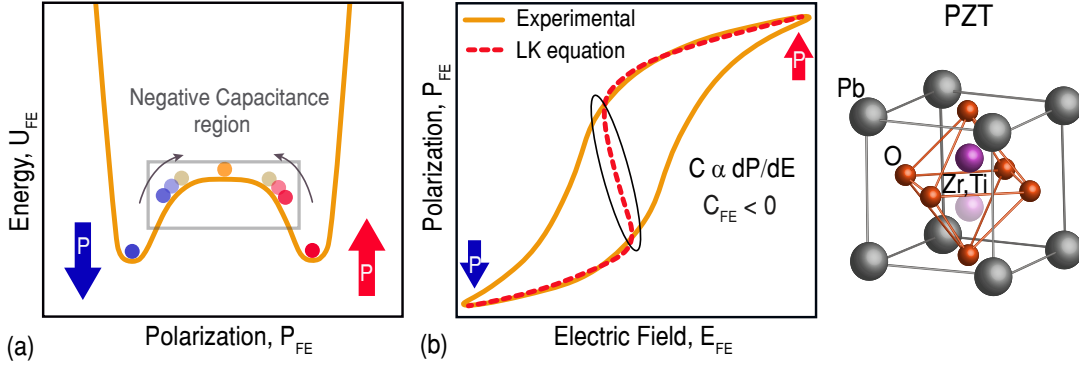


Figure 4.1 – Negative capacitance of ferroelectrics. (a) Energy function of a ferroelectric capacitor, showing an effective NC while switching from one stable polarization state to the other one. (b) Measured and fitting results of the L-K equation for the P-V curve of a PZT capacitor.

can be approximated as [142]:

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3qh(E_g+\Delta\Phi)}\right), \quad (4.2)$$

where m^* is the effective mass and E_g is the bandgap. Here, λ is the screening tunneling length that describes the spatial extent of the transition region at the source-channel interface. In a TFET, at a constant drain voltage (V_d), the increase of the gate voltage (V_g) modulates the device surface potential, which reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel ($\Delta\Phi$). The subthreshold swing of a TFET can be calculated as [15, 138]:

$$SS = \frac{\partial V_g}{\partial(\log_{10} I_d)} = \ln(10) \left[\frac{\partial V_d}{V_d \partial V_g} + \left(\frac{E+b}{E^2} \right) \frac{\partial E}{\partial V_g} \right]^{-1}, \quad (4.3)$$

where V_d is the drain voltage, E is the electric field, and b is a constant. Equation 4.3 reveals that the SS of a TFET is not limited by the Boltzmann electron energy distribution. However, the *on*-current of TFETs is unacceptably low for a technology which would like to replace the MOSFET [143]. Moreover, achieving SS 50 mV/decade is extremely challenging in most fabricated TFETs [144] and the steep slope region is typically limited to 1-3 decades of the drain current [15, 142], far less than that of a MOSFET (4-6 orders). Therefore, providing an acceptable I_{ON}/I_{OFF} ratio together with a sufficiently low SS has emerged as one of the most important technology issues involved in the fabrication of tunneling field effect transistors.

Another prominent way of SS reduction is lowering the body factor by exploiting

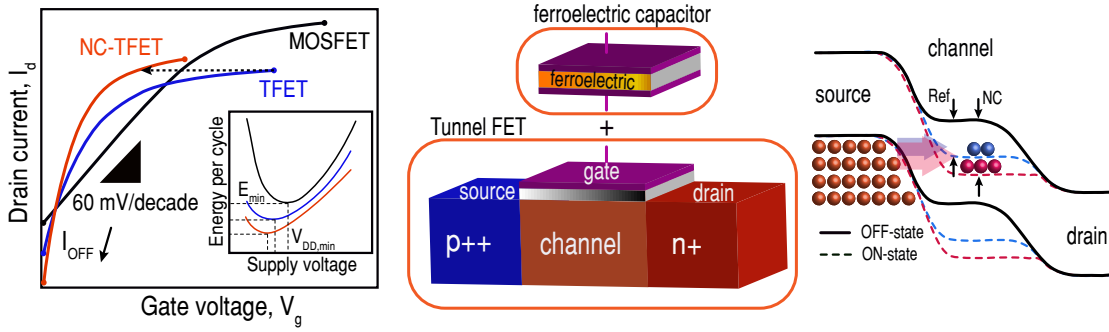


Figure 4.2 – An NC booster integrated into the gate stack of a TFET, increases the tunneling probability, resulting in a more energy efficient switching characteristic.

the negative capacitance (NC) region of ferroelectric materials, as previously mentioned. Here, we briefly explain again the concept of NC and its corresponding physics. Negative capacitance originates from the dynamic of the stored energy in the phase transition of ferroelectrics [101]. The concept of NC can be understood by considering the free energy of ferroelectric materials, which is traditionally modeled using a double well energy landscape (Figure 4.1-a). The energy characteristic of a ferroelectric capacitor is calculated by [145, 109]:

$$U_{FE} = \alpha P^2 + \beta P^4 + \gamma P^6 + E_{ext}.P, \quad (4.4)$$

where U_{FE} denotes the energy, P is the polarization, E_{ext} is the externally applied electric field, and α , β , and γ are material dependent parameters. In equilibrium, the ferroelectric resides in one of the wells, providing spontaneous polarization. The capacitance value is positive around these stable states considering the curvature of the P-E curve [101]. Nevertheless, it shows an effective negative capacitance around the origin while switching from one stable polarization state to the other one [146, 73]. The NC state has been proven elusive for ferroelectrics in isolation and cannot be observed in experiments, exhibiting hysteretic jumps in the polarization. However, it is validated that if a ferroelectric placed in series with a positive capacitor of proper value, this NC can be stabilized [55, 74].

The NC region can be modeled by the state of the art approach for modeling the dynamics of ferroelectric capacitors relying on L-K equation, $\rho(dP/dt) + \nabla_p U_{FE} = 0$ [147]. Figure 4.1-b shows and compares the experimentally measured P-V curve of a PZT capacitor as a well-known perovskite ferroelectric with the fitting result of the L-K equation, which can be observed when the NC segment is stabilized [105, 103]. A ferroelectric capacitor interconnecting with the gate stack of a MOS transistor can increase the total capacitance of the gate ($C_{total}^{-1} = C_{FE}^{-1} + C_{MOS}^{-1}$) when it is operating in the NC region. Specifically, the series structure offers a step-up voltage transformer that brings an abrupt increase in the differential charge of the internal node, V_{int} . Accordingly,

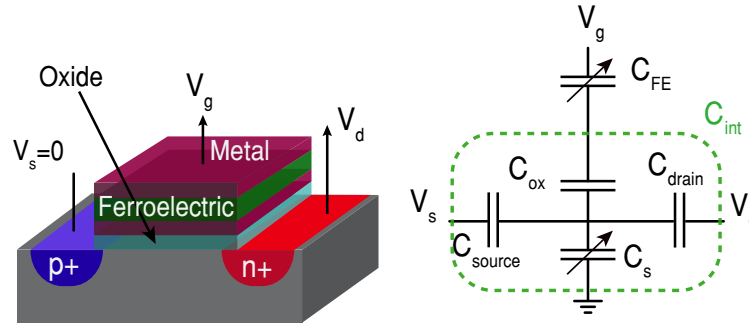


Figure 4.3 – Device schematic of an NC-TFET including its simple capacitance model.

an NC booster provides an internal voltage amplification ($\partial V_{int}/\partial V_g$), leading to a body factor reduction and a value of SS below the thermal limit of conventional MOSFETs [148, 149].

It has been proposed that the concept of NC being integrated into the gate stack of TFETs would be highly beneficial for energy band bending due to the internal voltage amplification, enhancing the BTBT probability [115, 150]. This results in a body factor < 1 , reducing the SS and expands the steep slope region of a TFET (Figure 4.2). Thereby, NC can be one of the most effective performance boosters of TFETs that ensures a steep *off-to-on* transition together with an acceptable I_{ON}/I_{OFF} . Previous works have mainly focused on the theoretical investigation of NC-TFETs [151, 152, 153, 154]. Here, we report a comprehensive experimental study of the performance-boosting that can be achieved in TFETs by employing negative capacitance of ferroelectrics. The double beneficial effect of NC on both subthreshold and overdrive regions of the TFET operation is demonstrated in both hysteretic and non-hysteretic devices. These effects are highlighted on both digital and analog performances of TFETs. Overall, this chapter argues that the NC can be effectively utilized in parallel with other performance boosters to improve both analog and digital performances of TFETs and opens a new path to adoption of TFETs as energy efficient electronic switches.

4.2 Predictive simulations

In this section, we have performed a simulation study to anticipate the impact of NC on TFETs. We focused our analysis on an n-type low-doped ultra-thin body (UTB) fully depleted silicon-on-insulator (FD SOI) FeTFET, as shown in Figure 4.3.

The device behavior of the metal-ferroelectric-MOS structure is numerically calculated by combining Silvaco Atlas TCAD simulations with the L-K equation. The experimentally extracted Landau parameters are used for PZT as the gate ferroelectric. The following phenomena are expected via the NC effect: (i) subthreshold swing (SS) improvement,

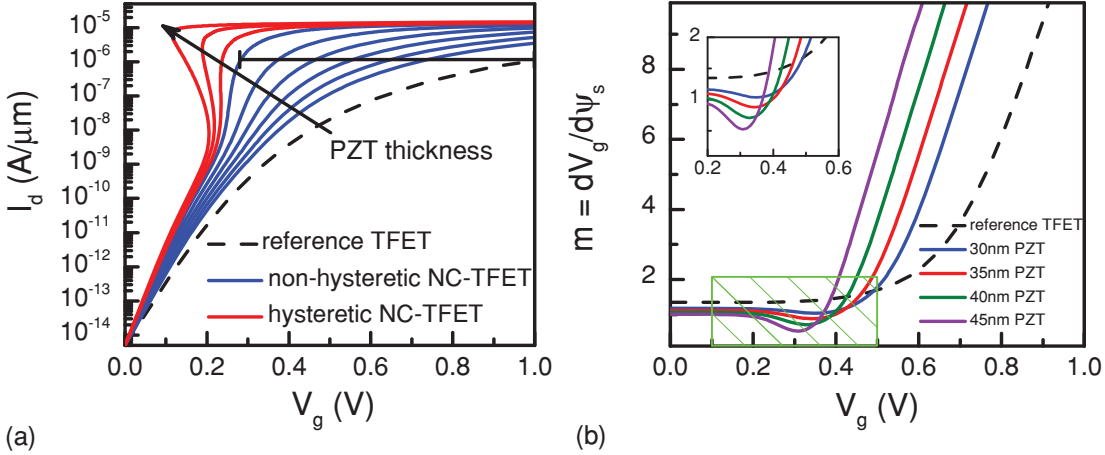


Figure 4.4 – Predictive simulations of an NC-TFET. (a) Transfer characteristic of the NC-TFET ($L_{ch}=20$ nm, $N_{ch}=10^{15}$ cm $^{-3}$, EOT=0.9 nm, $t_{BOX}=25$ nm, $V_{DD}=1$ V, and sweeping the PZT thickness as the gate ferroelectric). (b) Body factor of non-hysteretic NC-TFETs with respect to the PZT thickness, reducing by increasing the thickness.

and (ii) overdrive current enhancement due to the reduction of the device body factor (m) for the gate voltage larger than the threshold voltage. As simulation results in Figure 4.4 clarify, by changing the thickness of the PZT in the range of 20-60 nm, a strong effect of performance-boosting can be induced on the TFET. The simulated device corresponds to a 14 nm CMOS technology node p-i-n gated structure with $L_{ch}=20$ nm, $N_{ch}=10^{15}$ cm $^{-3}$, EOT=0.9 nm, $t_{BOX}=25$ nm, and $V_{DD}=1$ V. Results are presented for different values of PZT thickness, which plays the major role for matching conditions of NC in-series with the gate of a transistor ($C_{total} = (C_{FE}^{-1} + C_{MOS}^{-1})^{-1} > 0$ and $\beta = C_{FE}/(C_{FE} + C_{MOS}) \gg 1$). As simulation results predict, by increasing the PZT thickness, after a critical thickness, the NC condition for a non-hysteretic switch is not anymore fulfilled. Moreover, significant *on*-current, transconductance, and overdrive boosting and a relatively limited improvement in SS is predicted. The amplification factors of non-hysteretic cases, due to the body factor lowering and the matching conditions are reported in Figure 4.4. We greatly demonstrate that the saturation of the TFET current with respect to V_g is removed due to the differential internal amplification effect of $\beta = dV_{int}/dV_g \gg 1$. Physically, this corresponds to the body factor of the NC-TFET, which is smaller than 1 (the body factor of the presented case is predicted to be around 0.6).

4.3 Experimental demonstration of NC-TFETs

In the following sections, we report experimental results obtained on NC-TFETs with different device structures, having various reference TFETs and NC boosters (ferroelectric capacitors). First, the performance-boosting due to the NC effect on moderate silicon nanowire array TFETs is reported in both hysteretic and non-hysteretic modes of

operation. It has been reported that the NC can be efficiently utilized to significantly improve the most limiting factors of TFETs: *on*-current, transconductance, and overdrive. It was demonstrated that by designing properly the ferroelectric gate stack, fulfilling the condition for the non-hysteretic negative capacitance effect, the conduction performance can be improved by many orders of magnitude for $V_g > V_{TH}$ and a significant overdrive can be obtained. This strong effect is explained by the voltage amplification that is caused due to the ferroelectrics negative capacitance.

In the second case, novel InAs/InGaAsSb/GaSb nanowire TFETs with sub-60 mV/decade swing are employed as the baseline device. The well-known perovskite ferroelectric, PZT, and the recently proposed CMOS compatible ferroelectric, Si:HfO₂, are investigated as the NC booster. The PZT-based NC-TFET exhibits an SS of 10 mV/decade over three orders of magnitude of the drain current, an enhanced g_m/I_d factor having a peak of 3000 V⁻¹, and an improved I_{ON}/I_{OFF} ratio with a small hysteresis of 500 mV. In another NC-TFET, using Si:HfO₂ as ferroelectric, an average SS of 30 mV/decade over five decades of current is observed with a negligible hysteresis of 50 mV due to the proper matching of capacitances.

Lastly, well behaved InGaAs ring TFETs with a minimum swing of 55 mV/decade at room temperature are combined with high-quality single crystalline PZT capacitors, placed in series with the gate to demonstrate a nearly hysteresis-free NC effect. When fully satisfying the exact NC matching conditions by a single crystalline ferroelectric that can perform a mono-domain state, a hysteresis-free (sub-10 mV over 4 decades of current) NC-TFET with a sub-thermionic swing and an SS_{min} of 40 mV/decade is demonstrated. In other devices, improvement in the subthreshold swing, down to 30 mV/decade, and analog current efficiency factor, up to 180 V⁻¹, are achieved in NC-TFETs with a hysteresis as small as 30 mV. Importantly, the I_{60} FoM of the TFET is improved up to 2 orders of magnitude. The supply voltage is thereby reduced by 50%, down to 300 mV, providing the same *on*-current.

4.4 Silicon nanowire array NC-TFETs

The employed experimental configuration of the NC-TFET of this section is depicted in Figure 4.5 where a PZT capacitor is externally connected to the gate of a strained Silicon-Nanowire (Si-NW) array TFET. Such external electrical connection offers the flexibility of testing tens to hundreds of PZT capacitor values until the best matching ($C_{total} = (C_{FE}^{-1} + C_{MOS}^{-1})^{-1} > 0$ and $\beta = C_{FE}/(C_{FE} + C_{MOS}) \gg 1$) is achieved. The employed configuration is actually a Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) structure that is commonly used for the experimental configuration of NC field-effect transistors [74]. For this study, 46 ± 3 nm of Pb(Zr₄₃,Ti₅₇)O₃ (PZT) ferroelectric film has been grown via the chemical solution deposition route on a Pt-coated silicon wafer. The polycrystalline PZT film has a dense columnar grain structure with the grain size of

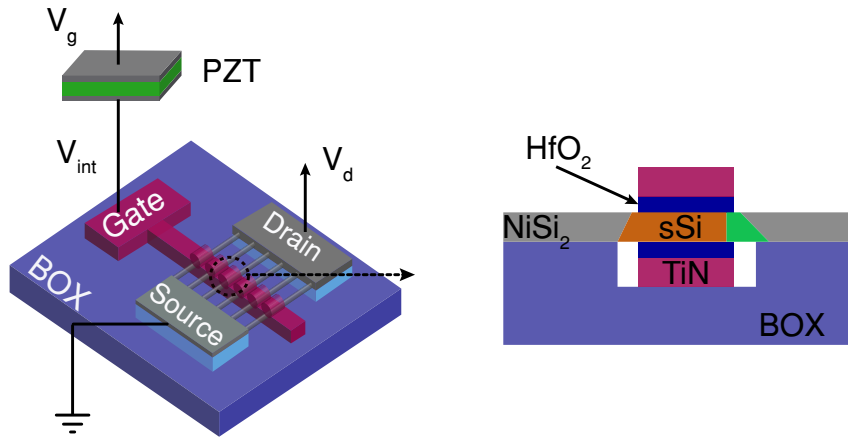


Figure 4.5 – Investigated experimental configuration of the NC-TFET, where the gate of a Si-NW array TFET is loaded by a PZT capacitor.

200±100 nm (Figure 4.6-a). The fabrication process and the electrical characterization of the employed PZT thin film are extensively discussed in the previous chapter. The nanowire array TFETs have a cross section of 30×5 nm² with a gate length of 350 μm (Figure 4.6-b). The structural data and the fabrication procedure of reference TFETs are also explained in detail in Figure 4.6.

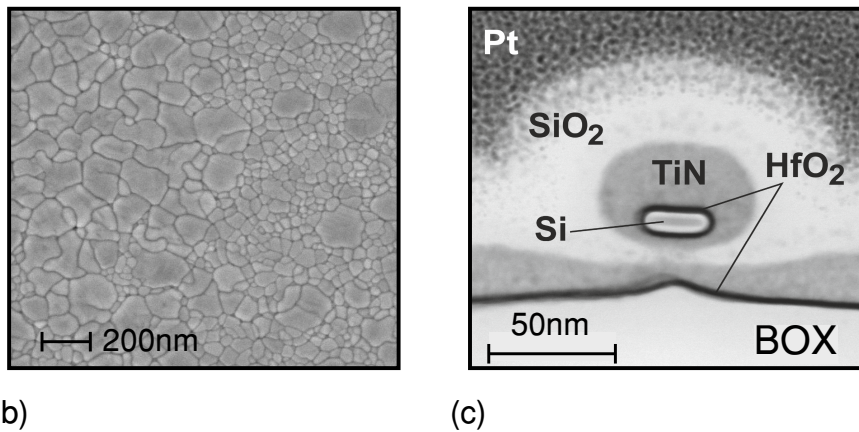


Figure 4.6 – Physical characterization of the NW array NC-TFET. (a) SEM analysis of the PZT indicating the polycrystalline nature of the film. (b) Transmission electron microscopy image of the silicon-nanowire TFET. The nanowire array TFETs have a cross section of 30×5 nm² with a gate length of 350 μm.

The strained Silicon (sSi) Nanowire (NW) array TFETs are fabricated with a top-down approach. The investigated sSi-NW array TFETs have a nanowire cross-section of 30×5 nm², a gate length of 350 μm, and ~1:4 GPa tensile strain booster (translated into bandgap reduction of the order of 95 meV per 1% axial strain). A rough overview of the

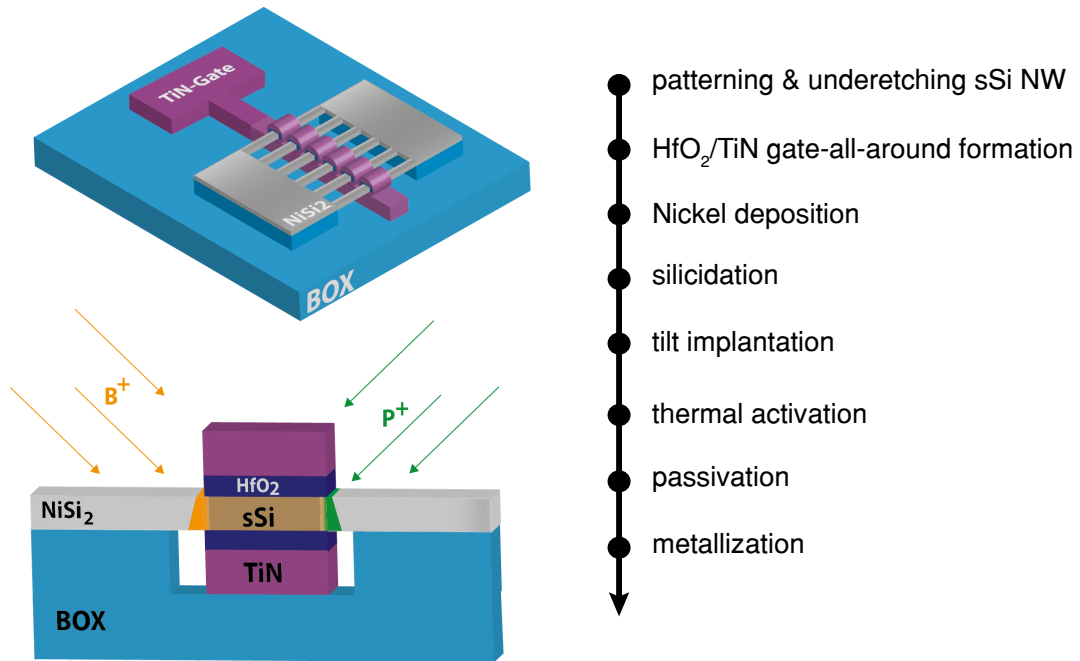


Figure 4.7 – Strained Silicon (sSi) Nanowire (NW) array TFETs (TFETs) are fabricated with a top-down approach. The investigated sSi NW-array TFETs have a nanowire cross-section of $30 \times 5 \text{ nm}^2$, a gate length of $350 \text{ }\mu\text{m}$, and $\sim 1:4 \text{ GPa}$ tensile strain booster.

process steps is shown in Figure 4.7.

The fabrication process started with patterning and under-etching of the sSi-NWs. The applied gate stack around the nanowires consists of a 3 nm thick HfO_2 dielectric and 40 nm of TiN as the gate metal using ALD. Next, Ni was deposited and a silicidation (NiSi_2) step was performed at the entire Si area which was not covered by the gate. Depending on the type of the TFET, the source/drain junctions were formed by tilted P+ and B+ implantations into the silicide with subsequent out-diffusion annealing at 500°C for 10 s to form shallow doping pockets by dopant segregation right at the channel interface [155].

4.4.1 Results and discussions

Figure 4.8 reports experimental transfer characteristics data measured on *n*-type sSi-NW array TFETs with and without connecting a PZT capacitor. The reference homojunction TFETs have $I_{on} \sim 0.1 \text{ }\mu\text{A}$ at $V_g=2 \text{ V}$ and $V_d=0.5 \text{ V}$ with a swing in the order of 100-150 mV/decade and show ambipolar behavior.

The presented characteristics in Figure 4.8 are indeed for two different TFETs that are not identical due to the process variation. The gate current of TFETs is very low and negligible compared to the drain current over the whole operation range. A significant

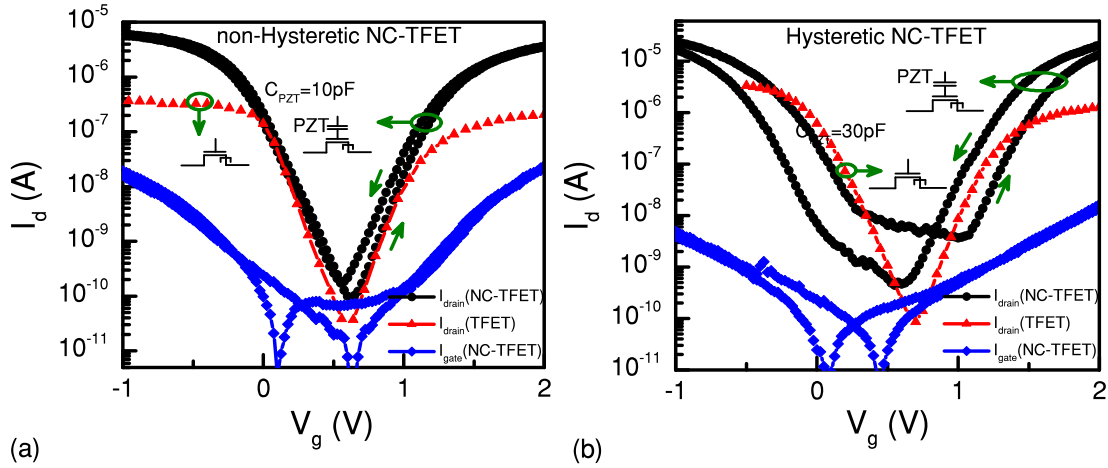


Figure 4.8 – Transfer characteristics of a non-hysteretic and a hysteretic NC-TFET where the negative capacitance matching condition is fulfilled in the entire range of the operation (a) and in a limited range of the gate voltage (b). The reference devices correspond to sSi-NW array n -type TFETs with the drain voltage of 0.5 V.

double improvement in the subthreshold slope and overdrive of the TFET is shown in Figure 4.8-a when the ferroelectric and the gate capacitances are matched so that a non-hysteretic NC operation can be achieved. The I_{ON} is boosted over the whole range of the operation, enhanced up to 100 times of its original value at the maximum gate voltage. This is explained by the fact that the NC behaves as an efficient electrical booster of the surface potential (ψ_s) and the body factor (m) of the TFET in the region following the barrier narrowing. This is fundamentally reflected into a body factor reduction less than 1, acting as a performance booster where the on -current of the TFETs would otherwise start to have a sloppy dependence on the gate voltage [15, 28]. It should be remarked that the surface potential boosting of NC effect not only increases the tunneling probability but also improves the region over which the tunneling current is integrated.

In addition to, considering the L-K equation, high order terms of the ferroelectric charge cannot be neglected at high gate voltages that results in an enhanced negative capacitance effect [141]. The NC effect acts as the TFET performance booster near subthreshold ($V_g < V_{TH}$) and for the overdrive region ($V_g > V_{TH}$). Therefore, the gate voltage can be reduced by 65%, maintaining the same level of the output current. Another device architecture with a different PZT capacitor and TFET, matching the condition of NC only in a limited region (at high V_g) is reported in Figure 4.8-b. In this late case, the NC-TFET operation is fully hysteretic and the performance boosting is narrowed down to a reduced region. All measurements have been carried out at the low drain voltage of 0.5 V due to the fact that the high values of the drain voltage provide a non-uniform potential profile that will change the negative capacitance condition [129].

Both Figures 4.8-a and 4.8-b report the recorded gate leakage current in all range

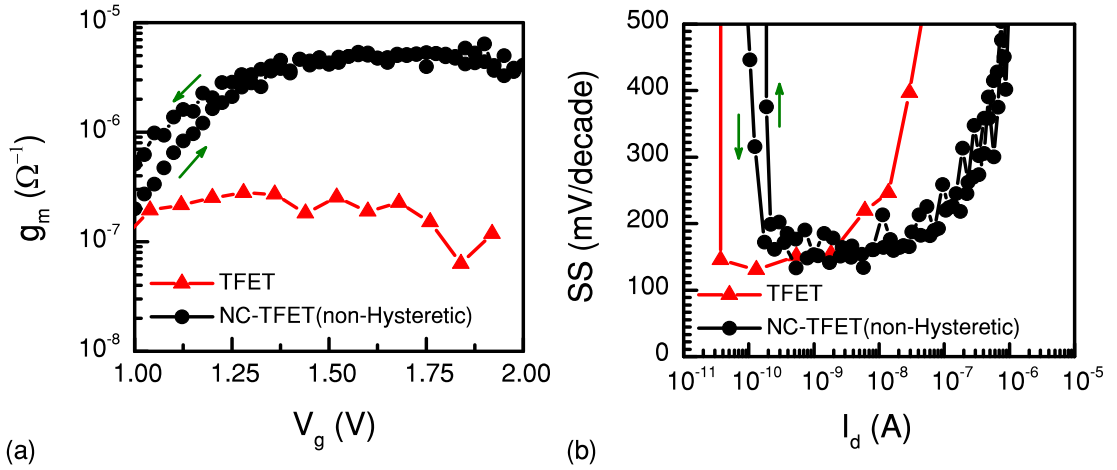


Figure 4.9 – Experimental performance improvement of the non-hysteretic NC-TFET corresponding to the presented device in Figure 4.8-a. The transconductance is boosted up to 100 times of its original value (a) and the low slope region is extended over 2 decades of current (b) in the case of the non-hysteretic NC-TFET.

of experiments, proving that its level is systematically lower than the I_{ON} and, then, that leakage and charge trapping mechanisms can be neglected in the reported effect. Moreover, this hysteretic leakage presents the typical signature of the ferroelectricity of PZT capacitors. The obtained enhancement in the TFET performance should not be mistaken with the effect of the ferroelectric polarization switching that always causes a huge hysteresis. The reported non-hysteretic improvement in the current and conductance can be only achieved in a well-designed negative capacitance transistor.

In Figures 4.9 and 4.10, we report the improvement induced by the use of the negative capacitor on TFET transconductance and subthreshold slope, in non-hysteretic and hysteretic modes of operation. Double sweep measurements with a negligible hysteresis for a device that fulfills the analytical condition of the non-hysteretic NC, corresponding to the presented device Figure 4.8-a, are depicted in Figure 4.9. In this case, the ferroelectric is stabilized and provides an effective NC in the whole range of the gate voltage, which results in an amplification factor above unity ($\beta > 1$) in both subthreshold and overdrive regions.

Figure 4.9-a represents the transconductance boosting by a factor of 10 to 100 compared to the reference TFET. The largest improvement (higher β value) occurs in the overdrive region ($V_g > V_{TH}$) due to the surface potential amplification, caused by the NC effect where g_m is increased by up to two orders of magnitude. This evidences that the negative capacitance provides a very strong performance-boosting effect in TFETs. Figure 4.9-b illustrates a smaller, yet clear improvement of the subthreshold swing by the NC effect, in agreement with the recently reported theoretical results [89, 116]. As a consequence of the SS and overdrive enhancement, the *on*-current is boosted over the

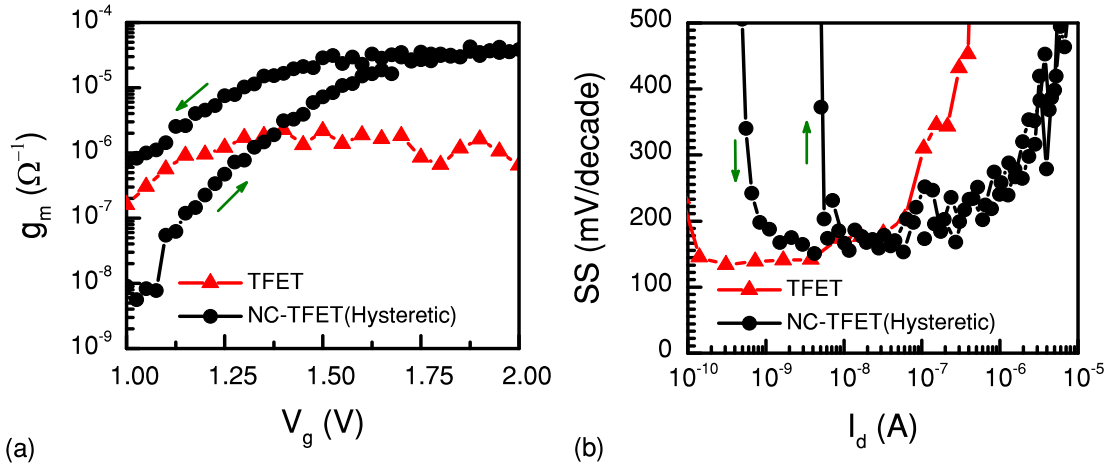


Figure 4.10 – Experimental performance improvement of the non-hysteretic NC-TFET, corresponding to the presented device in Figure 4.8-b. A limited enhancement is obtained in the transconductance of the hysteretic NC-TFET (a) and its subthreshold slope (b) comparing the non-hysteretic NC-TFET case.

whole operation range.

Figure 4.10 summarizes the effect of the PZT capacitor on DC electrical performance of the hysteretic NC-TFET (Figure 4.8-b), fulfilling the NC matching condition in a limited region. The transconductance is boosted for high V_g , reaching a factor of 10x at the maximum gate voltage (Figure 4.10-a). The subthreshold slope shows no considerable enhancement (Figure 4.10-b) as the NC matching condition is not fulfilled for low gate voltages. It is remarkable that from variously tested devices, only for the ones that closely verifying the NC stability condition, such a performance boosting is observed. Otherwise, a ferroelectric capacitor out of the range of the stability condition in-series with the gate of a TFET would provide a hysteresis without performance boosting. This type of device could be a proper candidate for hysteretic low power logic or for one transistor (1T) FeTFET memory applications [116].

4.5 InAs/InGaAsSb/GaSb nanowire NC-TFETs

The employed experimental configuration of the NC-TFET of this section is the same as the previous one where a ferroelectric capacitor is externally connected to the gate of a TFET. Novel vertical InAs/InGaAsSb/GaSb nanowire TFETs, which are the best ever reported experimental TFET [29], are considered as the reference transistor. Polycrystalline PZT and Si:HfO₂ capacitors are fabricated in various dimensions in order to fulfill the matching condition of NC and compare the impact of a perovskite and a CMOS compatible ferroelectric on the operation of an NC-TFET. In case of Si:HfO₂, due to the large leakage current of capacitors that severely degrades the NC effect,

the measurements have been conducted at a low temperature of 80° K to suppress the trap-assisted tunneling. This reduces the leakage current of the Si:HfO₂ capacitor by at least three orders of magnitude.

4.5.1 Baseline TFET

An SEM-image of a nanowire after the growth can be viewed in Figure 4.11-a, and an illustration of the different segments and their doping in Figure 4.11-b. Every device has 184 nanowires divided into four parallel lines with nanowires into double rows as SEM image in Figure 4.11-c shows. The first step of the device fabrication was digital etching, to remove the GaSb-shell and reduce the diameter of the channel region down to 26 nm, thereby improving the electrostatics. Directly after the digital etching, a high-k bilayer (Al₂O₃/HfO₂) was deposited using ALD. Estimated EOT of the high-k layer was 1.4 nm. To separate the drain and gate regions, a 30 nm-thick SiO_x spacer layer (Bottom-spacer), was deposited by utilizing thermal evaporation. The gate layer was formed by sputtering of a 30 nm-thick tungsten film, followed by the definition of the physical length ($L_g = 240$ nm), using reactive ion etching and mask definition. A spacer to separate the source and gate metals (top-spacer) was realized with S1800 photoresist. Top-contacts and pads were formed by sputtering on a Ni and an Au layer, followed by masking and UV-lithography. An illustration of the final device can be viewed in Figure 4.11-d.

A more detailed description of the growth and fabrication process can be found in the following subsections. Transfer data from one of the devices in Figure 4.11-e, confirms that the devices exhibit good electrostatics with low drain induced barrier lowering (DIBL) and small hysteresis. However, there is some source depletion mainly observed at low drive voltage due to the gate overlap. The device exhibits a point subthreshold swing that is below 60 mV/decade, for both sweeps in forward and reverse direction, Figure 4.11-f. Previously, devices with the same heterostructure but with fewer and thinner nanowires, have demonstrated an even lower subthreshold swing well below the thermal limit [29, 30]. The output data shown in Figure 4.11-g confirms that this device exhibits a negative resistance region (NDR). The highest peak-to-valley current ratio (PVCR) is 6.9 which is similar to values for devices with fewer nanowires obtained in [30]. This demonstrates a good uniformity between nanowires in the array.

4.5.2 Nanowire growth

Metal-Organic Vapor Phase Epitaxy (MOVPE) growth was performed in an Aixtron CCS 18313 reactor with EPISON controllers to control the concentrations of the non-dopant metalorganic precursors used. The vapor-liquid-solid mechanism was utilized to grow nanowires from 44 nm diameter 15 nm thick Au seeds patterned by EBL on high resistivity Si(111) substrates with a 260 nm highly doped InAs layer on top. The total flow was 8000

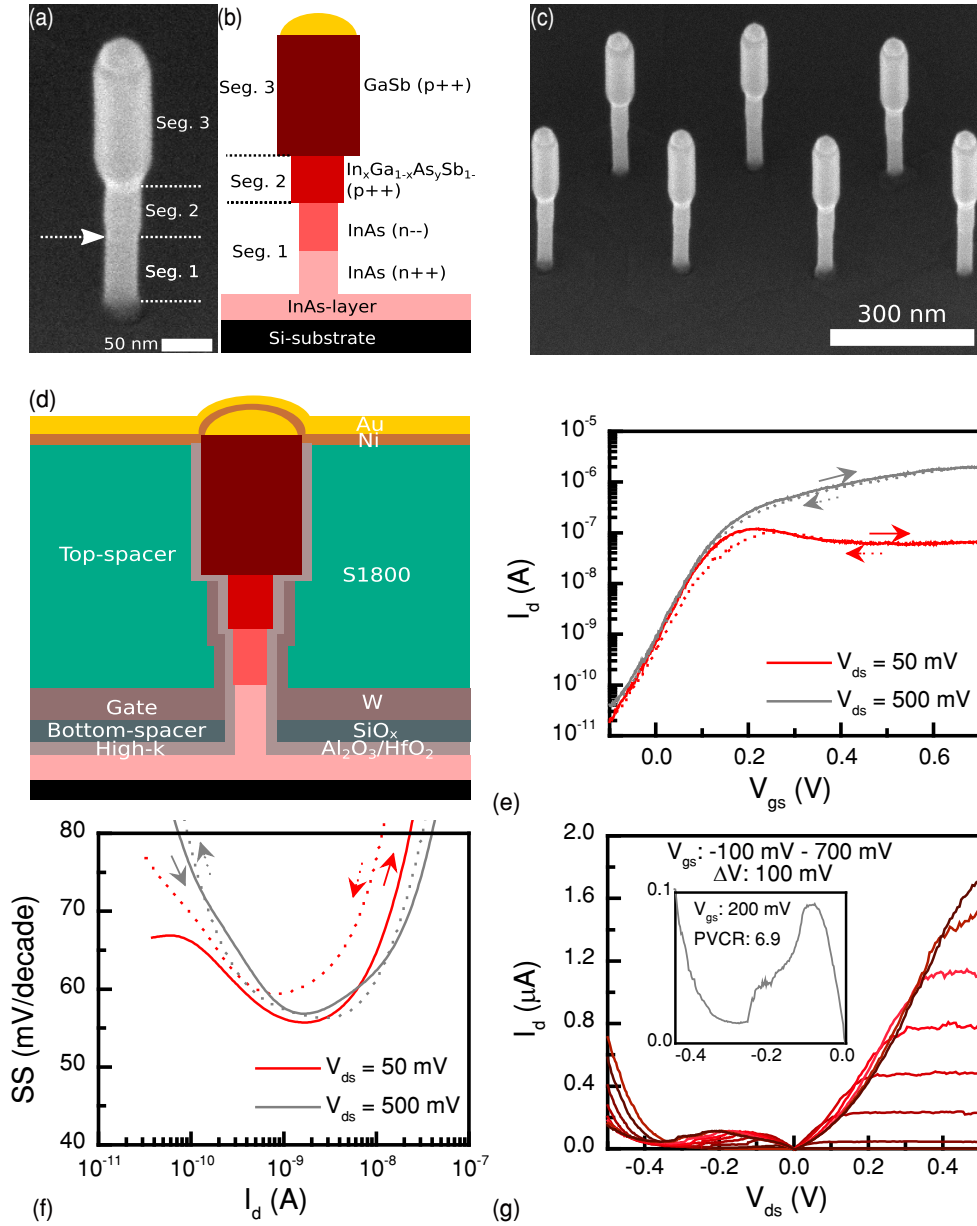


Figure 4.11 – Baseline TFET structure and electrical characterization. (a) SEM image of an InAs/InGaAsSb/GaSb nanowire after growth. (b) Schematic illustration of the nanowire including the doping profile. The composition of segment 2 is $x=0.29$ and $y=0.66$. (c) SEM image of nanowires in an array with 46 nanowires. (d) Schematic diagram of all layers of the device. (e) Transfer data for one of the devices with forward and reverse direction sweeps at drain voltages of 50 mV and 500 mV. At low drive voltage, there is an impact from source depletion due to the overlapping gate. (f) Subthreshold swing as a function of I_d . In spite of a large number of relatively thick nanowires, SS_{min} is lower than 60 mV/decade. (g) Output data from the same device, showing a superlinear behavior in the reverse direction and a negative differential resistance in the forward direction. The highest peak-to-valley current ratio (PVCR) is 6.9 (inset).

scm at a pressure of 100 mbar. The growth was initiated by 10 min annealing at 550° C in Arsine (AsH₃) followed by InAs growth at 460° C using Trimethylindium (TMIn) and Arsine (AsH₃) with a molar fraction of $X_{TMIn} = 6.1 \times 10^{-6}$ and $X_{AsH_3} = 1.3 \times 10^{-4}$, respectively. The bottom part of the InAs segment was n-doped by Tetraethyltin (TESn) ($X_{TESn} = 6.1 \times 10^{-6}$). The growth was then paused in an Arsine flow to reduce the amount of In dissolved in the Au seed particles. After this the InGaAsSb segment was grown using Trimethylgallium (TMGa) ($X_{TMGa} = 4.9 \times 10^{-5}$), Trimethylantimony (TMSb) ($X_{TMSb} = 1.3 \times 10^{-4}$), and AsH₃ ($X_{AsH_3} = 5.1 \times 10^{-6}$) corresponding to a gas phase composition of AsH₃/(AsH₃+TMSb) = 0.04. In remaining in the Au particle after the InAs growth is incorporated into the InGaAsSb segment. Finally, a GaSb segment was nucleated at 460° C with TMGa ($X_{TMGa} = 4.9 \times 10^{-5}$) and TMSb ($X_{TMSb} = 1.3 \times 10^{-4}$). The growth continued with reduced V/III ($X_{TMSb} = 7.6 \times 10^{-5}$) while heating to 515° C to avoid significant radial growth. Both the InGaAsSb and the GaSb segments were p-doped using Diethylzinc (DEZn) ($X_{DEZn} = 1.9 \times 10^{-5}$).

4.5.3 Detailed of the fabrication process of TFETs

During the growth of GaSb segment, a shell was formed on the bottom segments, which was removed by subsequent digital etching steps. Ozone plasma was used to oxidize the surface followed by wet etching with citric acid to remove the oxide. This process also reduced the diameter of InAs and InGaAsSb segments down to 26 nm and 28 nm, respectively. There was no observed etching of GaSb segment. Nanowires were covered with a high-k bilayer using atomic layer deposition. This layer was applied by using 5 cycles of Al₂O₃ and 36 cycles of HfO₂ at temperatures of 300° C and 120° C, respectively. A 30-nm-thick SiO_x bottom spacer layer was deposited using thermal evaporation without tilt but with rotation. The thicker GaSb-segment helps to keep the channel region free of SiO_x due to shadowing. However, sidewalls of the GaSb segment were covered with SiO_x-flakes, which were removed in subsequent HF etching step. To compensate for the thinning of high-k, another 12 cycles of HfO₂ at 120° C were deposited.

The gate was formed by first sputtering on a 30-nm-thick tungsten (W) layer, followed by spin-coating of the sample with S1800 resist. The physical gate-length was defined by usage of an etch-back process, with O₂-plasma in a reactive ion etching reactor (RIE). Using RIE, the W was removed from exposed sections with SF₆/Ar. The gate-pad was defined utilizing photoresist and UV-lithography followed by etching of W in exposed regions. The top-spacer was formed by spin-coating the sample with S1800 photoresist followed by etching back of the resist to wanted thickness with RIE. UV-lithography and RIE were used to realize gate and drain vias. Formation of source and drain contacts began by removal of the high-k on top of the nanowires and in drain-via using HF, followed by sputtering of 10-nm-thick Ni and 150 nm-thick Au. The contact pads were patterned using UV-lithography and wet-etching.

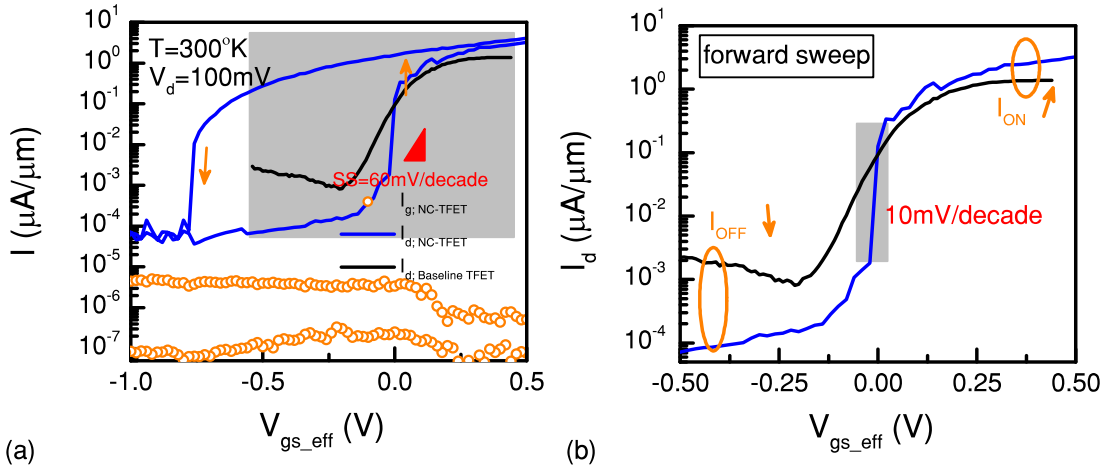


Figure 4.12 – Transfer characteristic of the PZT-based NC InGaAs nanowire TFET using a PZT capacitor ($10 \mu\text{m} \times 10 \mu\text{m}$) with a thickness of 46 nm as the ferroelectric. I_d - V_g curve shows a small hysteresis of 500 mV and a steep transition of 10 mV/decade at a drain voltage of 100 mV. The I_{ON}/I_{OFF} ratio is improved significantly.

4.5.4 PZT-based NC-TFET

For this experiment, 46 ± 3 nm of $\text{Pb}(\text{Zr}_{43}\text{Ti}_{57})\text{O}_3$ (PZT) ferroelectric film has been grown via the chemical solution deposition route (REF) on a Pt-coated silicon wafer. The stack of Pt(100 nm)/ TiO_2 (30 nm) has been sputtered on SiO_2 (500 nm)/Si wafer at 300°C . The PZT film consists of tetragonal ferroelectric phase with the predominant (100) orientation, with virtually no inclusion of any secondary non-ferroelectric phase like pyrochlore, as confirmed by XRD theta-2theta scans. The polycrystalline PZT film had dense columnar grain structure with the grain size of 200 ± 100 nm. Pt top electrodes were deposited on PZT film by sputtering and post-annealed at 550°C in an oxygen atmosphere in order to remove the sputtering damage at the Pt/PZT top interface. The electrical and physical characterizations of the employed polycrystalline PZT of this section is previously reported in chapter 3.

Figure 4.12 illustrates the input transfer characteristic of an n-type NC-TFET where the gate of the reference TFET (with 184 nanowires) is loaded with a PZT capacitor with an estimated area of $10 \mu\text{m} \times 10 \mu\text{m}$. The gate voltage is swept from -3 V to 3 V and back to the starting point while the drain voltage is set to 100 mV. In order to decouple the impact of the threshold voltage variation, curves are plotted with respect to the effective gate voltage, $V_{gs_eff} = V_{gs} - V_{TH}$. The NC of ferroelectric is partially stabilized, leading to a relatively small hysteresis of 500 mV, compared to the 5 V hysteresis loop of the PZT capacitor in isolation. The recorded gate leakage is extremely low and can be neglected in the reported effects. A super steep *off*-to-*on* transition of 10 mV/decade over three decades of the drain current is demonstrated in both positive and negative going branches of the drain current.

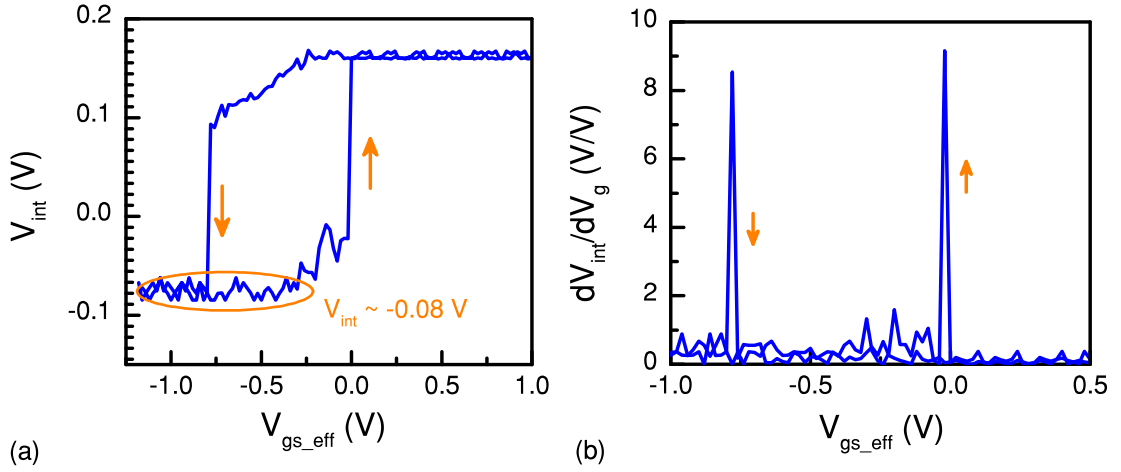


Figure 4.13 – (a) Internal node measurement of the PZT-based NC InGaAs nanowire TFET shows a remarkable amplification (b), up to 8 V/V, in both positive and negative going branches.

In order to quantitatively determine the voltage amplification by NC, the internal node is measured and the dV_{int}/dV_g vs. V_{gs_eff} curve is plotted in Figure 4.13. A significant gain with a peak of 8 V/V is observed in the both forward and reverse sweeps of the gate voltage. This internal amplification allows the surface potential to change faster than the gate voltage, leading to an enhanced tunneling probability and reduced SS that can be understood by taking into account equations 4.2 and 4.3 [156].

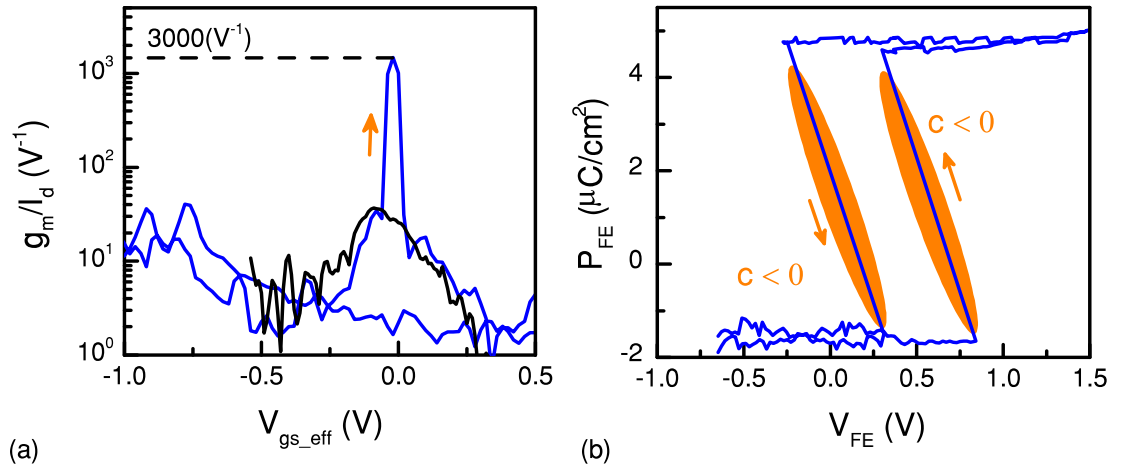


Figure 4.14 – (a) Current efficiency factor depicts a significant enhancement with a peak of 3000 V^{-1} . (b) The extracted polarization characteristic of the PZT capacitor during the NC-TFET operation demonstrates a broad range of NC behavior.

In addition to digital properties, an outstanding improvement in the current efficiency factor, as an analog figure of merit of transistors, is achieved with a maximum value of 3000 V^{-1} (Figure 4.14-a). Figure 4.14-b depicts the expected S-shape polarization

behavior of the ferroelectric, which is extracted by applying the conservation of the electric field displacement between the ferroelectric and oxide [74]. An effective NC in a wide range of the TFET operation is realized in both forward and reverse sweeps with a small hysteresis window of 500 mV, corresponding to the hysteresis of the I_d - V_g curve of the NC-TFET. It has been previously reported that the huge gain of NC, leading to a super steep switching feature in a transistor, is accompanied by a hysteresis as a trade-off [114, 157]. This is attributed to the second term on the right-hand side of the L-K equation, which causes non-linearity. Therefore, the ferroelectric and transistor should be chosen wisely to maximize the steepness of the *off-to-on* transition as well as minimizing the hysteresis. The hysteresis of a negative capacitance transistor can be alleviated or removed with better matching of capacitances. In this regard, the total capacitance of the structure should remain positive in the whole range (or at least in a broad range) of the applied gate voltage [115].

It is evident that the *off*-current of NC-TFETs is considerably lower than the one of the reference device (Figure 4.15). This can be explained by focusing on the internal voltage, the actual gate voltage of the baseline TFET, and the related band diagram of the TFET. Here, we explain the impact on the PZT-based NC-TFET and it would be similar for the Si:HfO₂-based NC-TFET. The measured internal voltage of the NC-TFET, V_{int} , demonstrates that the gate voltage of the baseline TFET is almost constant in the off-state, having an average of -0.08 V. This happens as a result of the charge balance condition between the ferroelectric dipoles and electrical charges in the channel. Therefore, the PZT capacitor set the internal voltage at -0.08 V. The band diagram of the TFET in the off-state is simulated and compared with various gate biases, using the Silvaco Atlas commercial TCAD tool. The physical parameters of the InAs/InGaAsSb/GaSb nanowire have been chosen in correspondence to the fabricated TFET. Figure 4.15-c depicts the band diagram of the InAs(n++)/InAs(n-)/InGaAsSb(p++)/GaSb(p++) nanowire TFET while the gate bias of -0.08 V is applied. Figure 4.15-c demonstrates the band diagram of the nanowire TFET, showing that there is no narrow tunneling path available in the source-channel or drain-channel junction. This is the main reason that the proposed NC-TFET provides a remarkably low *off*-current. A value of V_{int} lower than -0.08 V, -0.5 V in case of Figure 4.15-d, effectively reduces the tunneling barrier near the channel-drain junction and creates a leakage path, which extends by using lower internal voltages. On the other hand, a high V_{int} , such as 0.0 V and 0.5 V that are presented in Figures 4.15-e and 4.15-f, provides a tunneling path in the source-channel junction and the TFET operates in the on-state. In short, the reduction of the *off*-current in the proposed NC-TFETs is due to the fact that the ferroelectric dipoles set the value of the internal node in a voltage that blocks the tunneling current in the off-state.

4.5. InAs/InGaAsSb/GaSb nanowire NC-TFETs

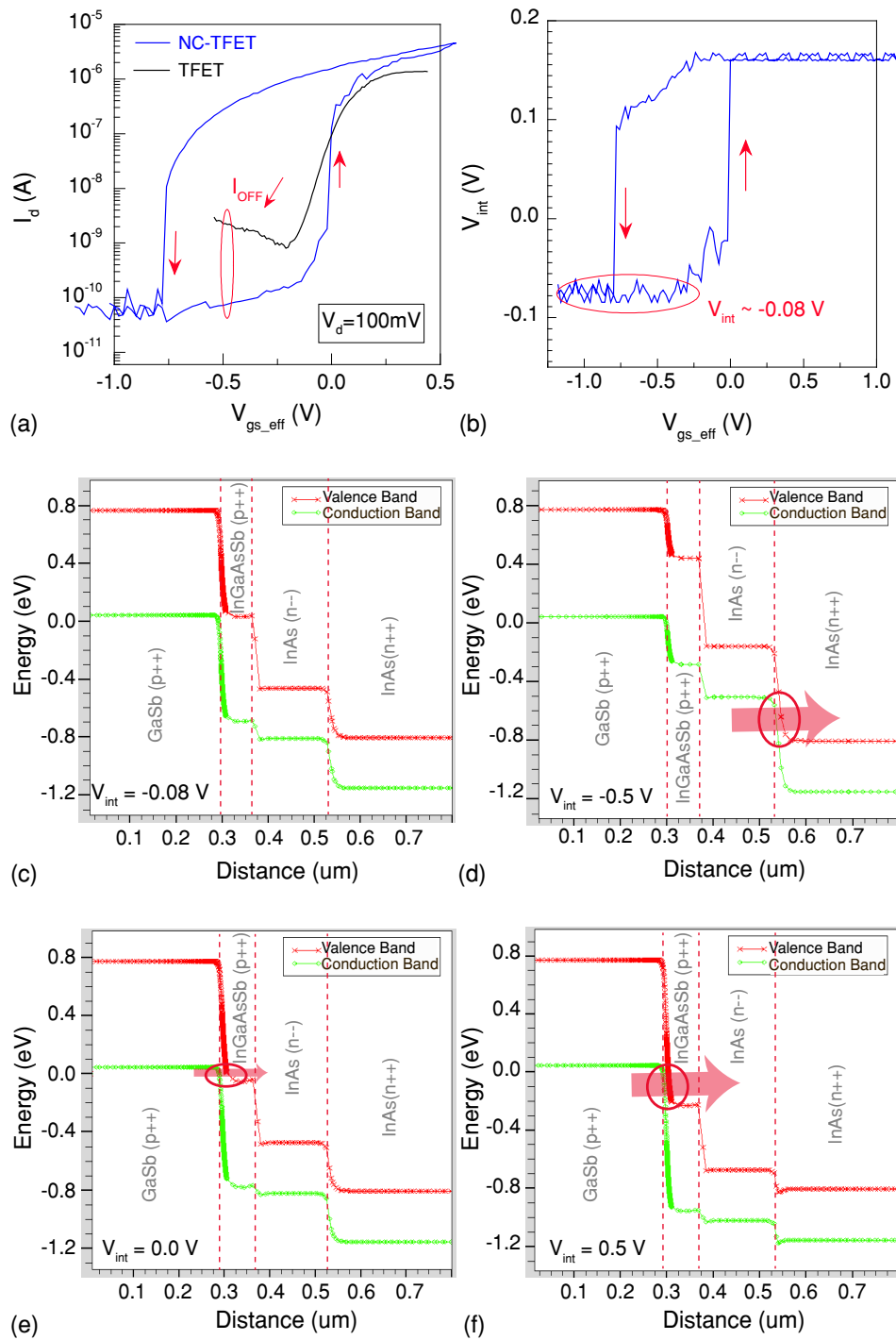


Figure 4.15 – Impact of the ferroelectric capacitor on *off*-current of the NC-TFET. (a) I_d - V_g curve of the PZT-based NC-TFET comparing with the reference device. The measured internal voltage (b) demonstrates a relatively constant voltage around -0.08 V on the gate of the baseline TFET during the OFF state. The simulated band diagram of the TFET depicts that with a gate voltage of around -0.08 V (c), there is no tunneling path in the OFF state. On the Other hand, any gate voltages lower (d) or higher than the mentioned value (e) and (f), provides a tunneling region that causes a leakage current.

4.5.5 Si:HfO₂-based NC-TFET

Silicon-doped HfO₂ thin films were recently discovered to enable the CMOS compatible manufacturing of ferroelectrics [123, 124]. The origin of this ferroelectricity attributed to the formation of non-centrosymmetric orthorhombic phase which is found to be stabilized preferably by crystallization of the as-deposited amorphous dopant(Si):HfO₂ thin films in the presence of a top TiN electrode [125]. In comparison to popular perovskite ferroelectrics such as Pb(Zr,Ti)O₃ (PZT) and SrBi₂Ta₂O₉ (SBT), HfO₂-based ferroelectrics offer distinct advantages including CMOS compatible fabrication process with ALD, relatively low dielectric constant, possibility to adoption of industrial gate electrodes, and appropriate remanent polarization [124, 60]. In this section, Si:HfO₂ ferroelectric capacitors are employed to demonstrate NC on InAs/InGaAsSb/GaSb nanowire TFETs.

The structure of Si:HfO₂ capacitors is depicted in Figure 3.6 where the ferroelectric film is placed between a sandwich of TiN (10 nm) and a 50 nm thick top Pt electrode. The film has a thickness of 13.2 nm and a Si concentration of about 3.4%, which was found to be the optimized Si% in terms of remanent polarization and leakage [126, 158]. The detail of the fabrication process and optimization steps of Si:HfO₂ is previously presented in chapter 3. The crystal structure of the two stable polarization states of the ferroelectric Si:HfO₂, orthorhombic phase, is schematically shown in Figure 3.6 (right). The atomic-force-microscopy (AFM) of the surface of Si:HfO₂ film confirms the conformality that was expected from the ALD technique, having a variation of less than 0.1 nm (Figure 3.7). Essential prerequisites for ferroelectric layers suitable for exploiting the NC effect include sharp and coherent switching and weak intrinsic leakage.

In order to evaluate ferroelectricity in the Si:HfO₂ layer in the nanometer scale, we measured local polarization switching and mapped the polarization domain structure using the off-resonance piezoelectric force microscopy (PFM). The technique has been enhanced for probing extremely weak electromechanical coupling typical for thin HfO₂-based films with an outstanding sensitivity < 0.1 pm. For most device-relevant data the local piezoelectric response was detected through the top electrode, using a sub-coercive AC driving signal of 0.5 V/92 kHz. The resulting maps of amplitude and phase of local piezoelectric response (Figure 3.8) revealed a sharp polarization domain pattern expected for good quality polycrystalline ferroelectric layers. The loop of transverse piezoelectric coefficient d₃₃ measured through the top electrode (right) showed that the polarization switches under voltage in a sharp, complete and saturating way, with the coercive voltage close to 1 V. An abrupt 180° flip of the phase of local piezoelectric signal observed at the coercive voltage indicates that the leakage conduction is relatively low and does not affect the measurements. The use of low leakage ferroelectrics is crucial for the NC effect because the leakage causes intrinsic polarization screening and therefore inhibits the conditions required for NC regime. For switching performance of polycrystalline ferroelectric films the grain boundaries often represent a critical issue. Charged defects

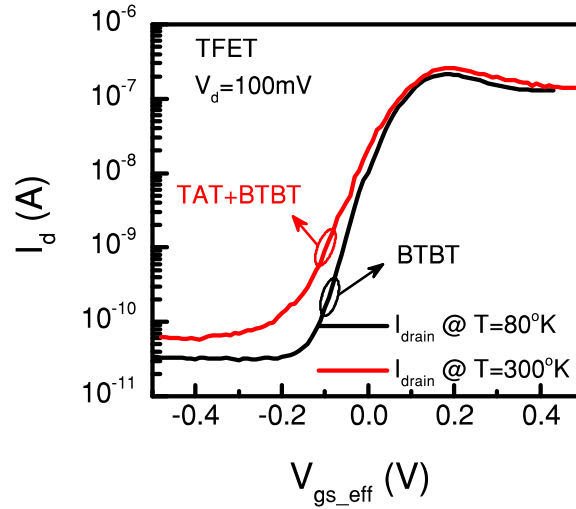


Figure 4.16 – Impact of the temperature on the operation of the reference TFET. I_d - V_g curve of a TFET at the room temperature is compared with the input transfer characteristic of the same device at 80° K.

accumulated at the grain boundaries can block propagation of polarization domains and/or pin the domain walls resulting in a domain pattern that closely follows the grain structure.

The PFM data in Figure 3.8 suggests that the grain boundaries in the studied Si:HfO₂ layer do not obstruct the switching process. This is confirmed by the size of polarization domains of 50-300 nm, which incorporate many grains of Si:HfO₂ with an average size of about 25 nm. The sharp boundaries between the polarization domains attest to the homogeneous ferroelectric phase, without any visible inclusions of the secondary non-ferroelectric phase earlier reported in HfO₂-based ferroelectric films [123, 125]. Thus the PFM analysis suggests that the structural features of the ferroelectric film do not significantly disturb the uniform polarization response required for the NC effect.

It is observed that a crystallized HfO₂ capacitor with relatively large dimensions, which is needed for our experimental setup, has a large leakage current that kills the NC effect. Thus, the measurements have been carried out at the low temperature of 80° K, which cancels out the trap-assisted tunneling in the ferroelectric capacitor. The leakage current is reduced more than three orders of magnitude at 80° K comparing the one of the room temperature. This low-temperature measurement does not starkly affect the baseline TFET operation. Ideally, the main carrier injection mechanism in TFETs is the band-to-band tunneling of carriers from source to the channel, which is independent of temperature. At room temperature, trap-assisted tunneling (TAT) also collaborates with the channel current and degrades the steepness of the transfer characteristic. Due to the low-defect fabrication process of nanowire TFETs, the TAT has a small impact on the performance of the employed TFETs.

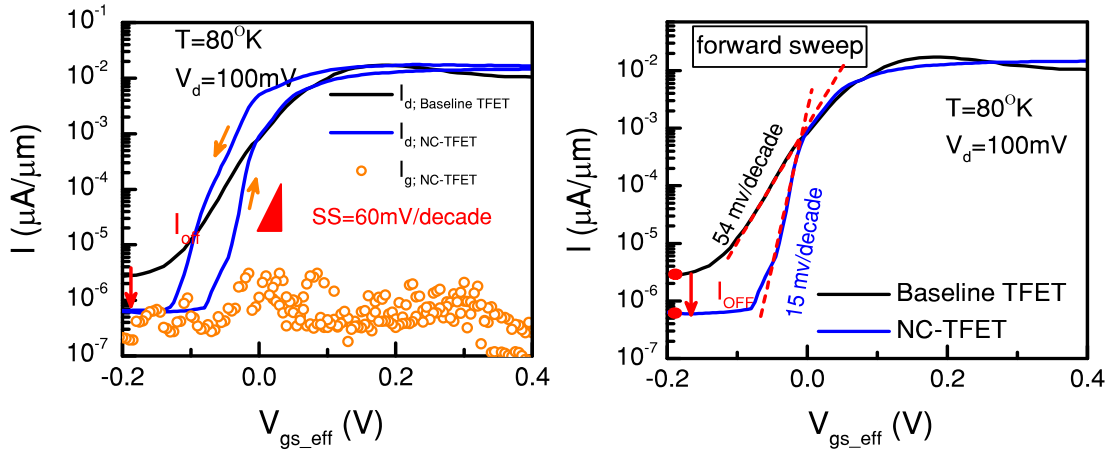


Figure 4.17 – Si:HfO₂-based NC-TFET. Transfer characteristic of an NC-TFET using a Si:HfO₂ capacitor with a thickness of 13.2 nm and an area of 10 μm × 10 μm. The measurement has been conducted at the low temperature of 80° K in order to reduce the leakage of Si:HfO₂ by suppressing the trap-assisted tunneling. A small hysteresis, less than 50 mV, is obtained as a result of the proper capacitance matching (V_d was set at 100 mV). The I_{ON}/I_{OFF} ratio is enhanced and the impact of the source depletion due to the overlapping gate has vanished. The SS_{min} is remarkably improved, down to 15 mV/decade, and the low slope region is extended over 5 decades of current.

In order to make sure that the low-temperature measurement does not severely affect the baseline TFET operation, the input transfer characteristic of the reference device at room temperature and 80° K are compared. The main current mechanism in TFETs is band-to-band tunneling of carriers from source to the channel, which is independent of the operating temperature. However, at high temperatures, trap-assisted tunneling also collaborates to the channel current. This impact is observable in Figure 4.16, where the I_d - V_g curve of a TFET at 300° K and 80° K are demonstrated. The input transfer characteristic of the TFET at 80° K is steeper and the *off*-current is lower comparing the room temperature measurement. This is due to the fact that the current of the TFET at 80° K is purely a BTBT current.

It is worth noting that the impact of the TAT in the employed TFETs of this work is weak as a result of the extremely low defect fabrication of the heterostructure which makes us eligible to demonstrate a Si:HfO₂-based NC-TFET at low temperature of 80° K as a proof of concept [29, 30]. This makes us eligible to demonstrate the impact of negative capacitance effect of Si:HfO₂ on the TFET performance as a proof of concept. The reference TFET shows a minimum swing of 54 mV/decade at 80° K, which is close to its room temperature value. Figure 4.17 depicts the I_d - V_g plot of an NC-TFET, using a Si:HfO₂ capacitor (10 μm × 10 μm) as the NC booster. The ferroelectric NC and the gate intrinsic capacitance of the baseline TFET are well-matched, leading to an inconsequential hysteresis of 50 mV while the drain voltage was set at 100 mV.

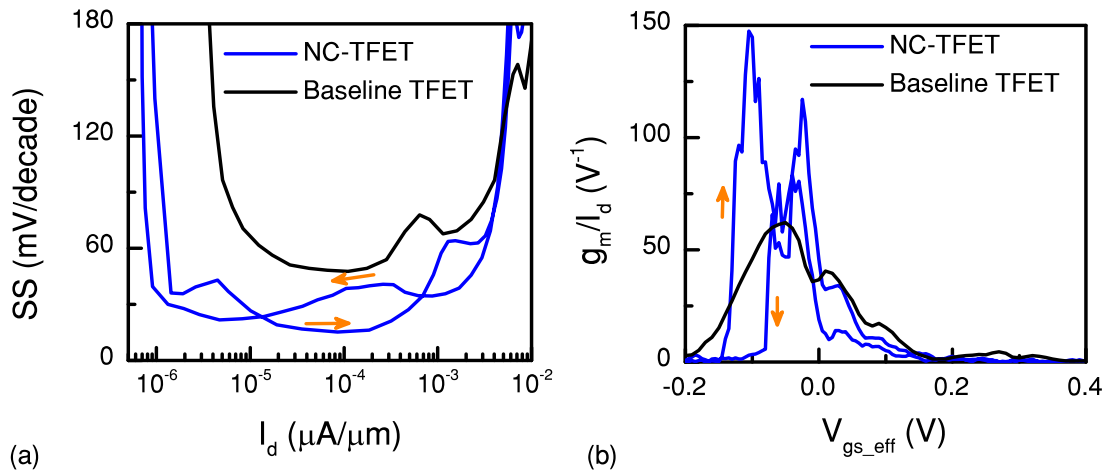


Figure 4.18 – Performance improvement in Si:HfO₂-based NC InGaAs nanowire TFET. (a) SS_{min} is remarkably improved, down to 15 mV/decade, and the low slope region is extended over 5 decades of current. (b) g_m/I_d figure of merit is increased and reached a maximum value of about 150 V^{-1} .

The I_{ON}/I_{OFF} ratio is enhanced and the impact of the source depletion due to the overlapping gate, which reduces the drain current at elevated gate voltages, is removed. The gate leakage is lower than the drain current in the whole range of operation and can be neglected in the reported effect. Figure 4.18-a compares the SS of the reference TFET and the negative capacitance one, showing that the minimum value of swing is reduced remarkably and the low slope region is extended over about five decades of the drain current. An average SS of about 30 mV/decade with a minimum value of 15 mV/decade is achieved.

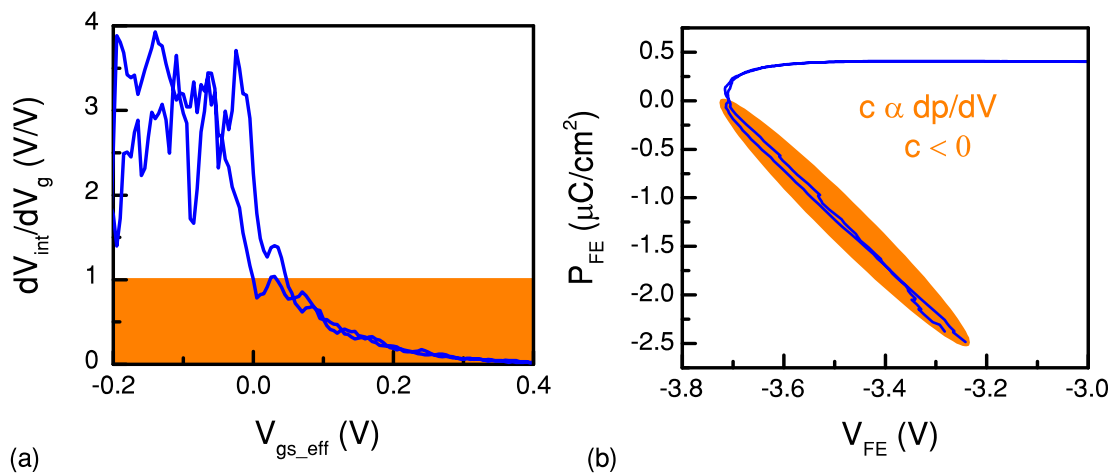


Figure 4.19 – Internal voltage amplification in Si:HfO₂-based NC InGaAs nanowire TFET. (a) An internal voltage amplification due to the effective NC effect of ferroelectric (b) is demonstrated in a wide range of operation (35%).

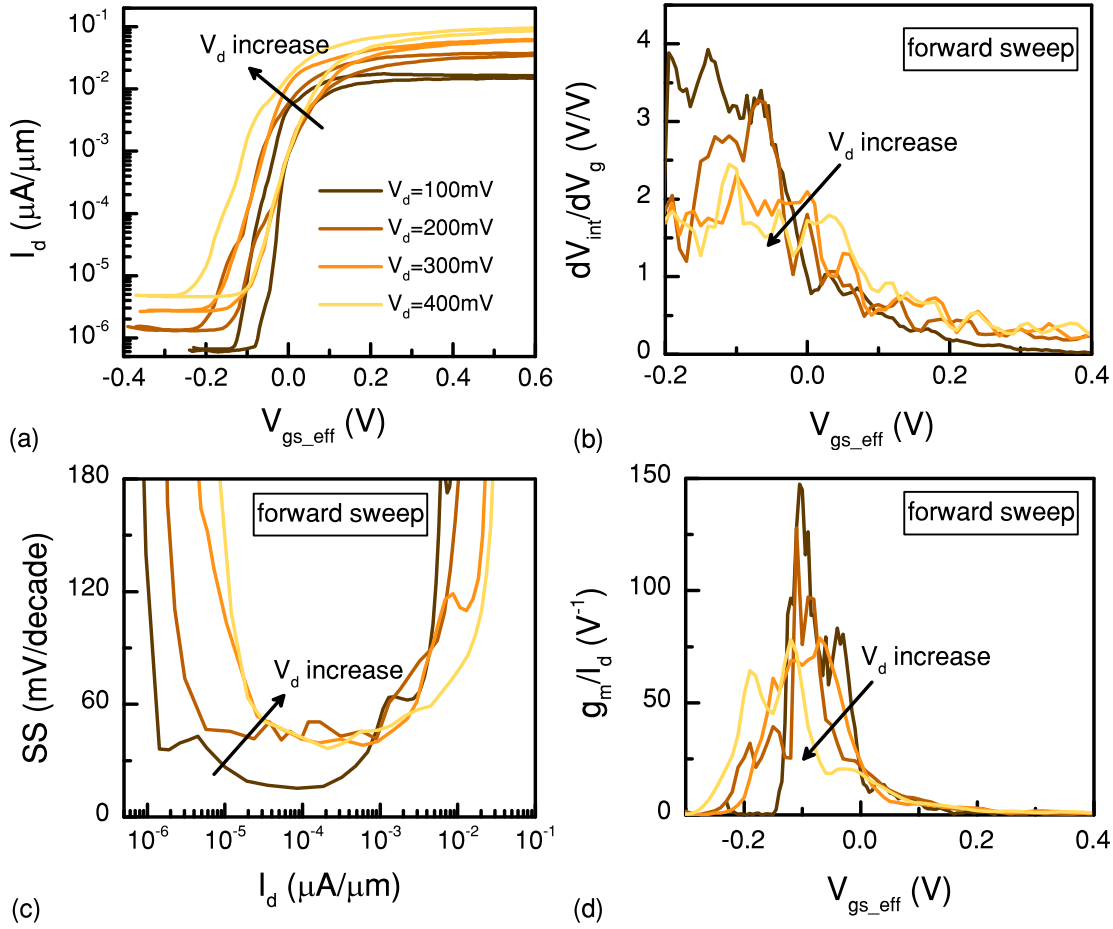


Figure 4.20 – Impact of the source-to-drain electric field on the performance of the Si:HfO₂-based NC-TFET. (a) The drain voltage has been swept from 100 mV to 400 mV, showing that the increase of V_d gives rise to the hysteretic behavior. (b) The internal gain of NC is considerably reduced by increasing V_d . Therefore, the SS (c) and current efficiency factor (d) are severely degraded. Results are compared for the forward sweep of the gate voltage due to the similar behavior of the positive and negative going branches.

The g_m/I_d factor is enhanced and reached a maximum value of 150 V^{-1} . The internal voltage measurement illustrates a voltage gain with an average of 3 V/V over 35% of the gate voltage range for both positive and negative going branches (Figure 4.19-a). The extracted P-V loop of the ferroelectric capacitor confirms the existence of an almost non-hysteretic negative capacitance (Figure 4.19-b). The polarization characteristic of the series connected Si:HfO₂ capacitor exhibits a lower negative value comparing to the PZT case. This can be understood by considering the fact that the capacitance of a non-linear dielectric is proportional to the dP_{FE}/dV_{FE} value. In the case of the Si:HfO₂-based NC-TFET, a smaller hysteresis and a smaller voltage gain is demonstrated compared to the previous case. This proposes that the previously reported trade-off between the steepness and hysteretic behavior of NC-FETs [114] is also valid for NC-TFETs.

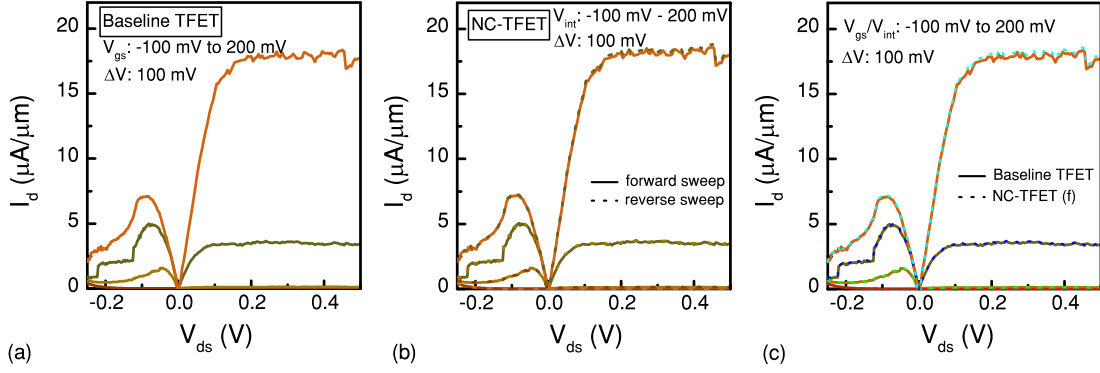


Figure 4.21 – Impact of NC on the output transfer characteristic. (a) demonstrates the I_d - V_d curve of the baseline TFET for gate voltages from -100 mV to 200 mV. (b) compares the output transfer characteristic of the NC-TFET for the forward and reverse sweeps of the drain voltage. The gate voltage has been tuned to provide an internal voltage corresponding to the previous case. (c) I_d - V_d plot of the forward sweep of the NC-TFET shows similar results comparing to the baseline TFET. It should be noted that the V_{gs} of the NC-TFET was tuned to provide an internal voltage (V_{int}) similar to the gate voltage of the reference TFET.

Figure 4.20 investigates the impact of the source-to-drain electric field on the electrical performances of the same NC-TFET. The drain voltage, V_d , is swept from 100 mV to 400 mV while the source contact is grounded. Figure 4.20-a depicts the I_d - V_g curve of the NC-TFET with different V_d values. Besides the common effect of V_d on the increase of *on*-current and *off*-current, which is universal for TFETs or any other transistors, the hysteresis of the NC-TFET is increased and the steepness of the transfer characteristic is reduced for higher V_d values. In fact, the hysteretic behavior and boosting effect in a negative capacitance transistor can be dramatically controlled by the drain voltage as the charge and MOS capacitances vary with V_{ds} . This is due to the fact that the shape of the polarization characteristic is dictated by the relative values of MOS and ferroelectrics negative capacitance. The internal voltage gain of NC is significantly degraded (Figure 4.20-b) for higher drain voltages that increases the SS_{min} value and limits the low-slope region.

The current efficiency factor is also reduced by increasing the source-to-drain electric field. In a negative capacitance transistor, the ferroelectric polarization charge density and the channel charge density should match. Thereby, the operation point, which is the intersection of the transistor charge line and P-V characteristic of ferroelectric depends on the drain voltage [74]. This means that by varying V_{ds} , the operation point of the NC-TFET changes and so the boosting effect due to the negative capacitance of ferroelectric. It is worth noting that no considerable impact was observed on the output transfer characteristic of the reported NC-TFETs comparing their reference devices when the gate voltage of the TFET has the same value as the V_{int} of the NC-TFET. More specifically, no observable impact of NC was evidenced by sweeping the drain voltage at

Table 4.1 – Performance of previously reported NC-FETs compared to the proposed Si:HfO₂-based NC-TFET of this work.

Device type	Ferroelectric	L_g	Hysteresis	SS_{min}	Range
Si- nMOSFET [127]	PZT	10 μm	12 V	13 mV/dec	1
Si- FinFET [133]	BiFO ₃	100 nm	5 V	15 mV/dec	7
Si- nMOSFET [130]	PVDF	-	≈ 0 V	52 mV/dec	2-4
Si- nMOSFET [159]	PZT	70 nm	1 V	20 mV/dec	5
Si- nMOSFET [160]	HZO	-	100 mV	52 mV/dec	1-2
Ge- NW FET [161]	HZO	80 nm	≈ 0 V	54 mV/dec	1
Ge- FinFET [162]	HZO	60 nm	≈ 0 V	58 mV/dec	1-2
Si- nMOSFET [163]	Al:HfO ₂	30 μm	≈ 10 mV	40 mV/dec	1-2
TFET- This Work	Si:HfO₂	240 nm	< 50 mV	15 mV/dec	5

a constant V_g . The variation of V_d does not affect the vertical electric field inside the ferroelectric layer and hence, the ferroelectric acts as a positive capacitor.

In order to investigate the impact of the NC effect on the output transfer characteristic of NC-TFETs, I_d - V_d curves of the reference TFET (corresponding to the case of the PZT-based NC-TFET) and NC-TFET are plotted in Figure 4.21. Figure 4.21-a shows the output transfer characteristic of the baseline TFET while V_{gs} was swept from -100 mV to 200 mV with a 100 mV step. Figure 4.21-b demonstrates the I_d - V_d curve of the NC-TFET for both forward and reverse sweeps of the drain voltage. The gate voltage was set in order to provide an internal voltage, V_{int} , corresponding to the V_{gs} of the previous case. Figure 4.21-c compares the I_d - V_d curves of the baseline TFET with the one of the NC-TFET (forward sweep). It is evident that by sweeping the drain voltage, there is no considerable impact due to the negative capacitance can be observed. This is due to the fact that sweeping of the drain voltage does not provide any considerable change in the vertical electric field inside the ferroelectric. Hence, ferroelectric dipoles do not change their stable state and the capacitor acts as a linear dielectric. In this case, the structure works as a capacitive voltage divider between V_{gs} and V_{int} .

The reported measurements of this section are the first experimental demonstration of NC-TFETs with a sub-60 mV/decade swing. Therefore, we have benchmarked the proposed NC-TFET with the previously reported negative capacitance MOSFETs. Due to the high interest in the recently proposed CMOS compatible ferroelectric, doped HfO₂, the performance of the reported Si:HfO₂-based NC-TFET is compared with the recently reported NC-FETs. Despite the fact that the Si:HfO₂-based NC-TFET of this work is measured at 80° K, it is possible to compare it with NC devices at room temperature as the performance of TFETs is almost independent of the operating temperature. Hence,

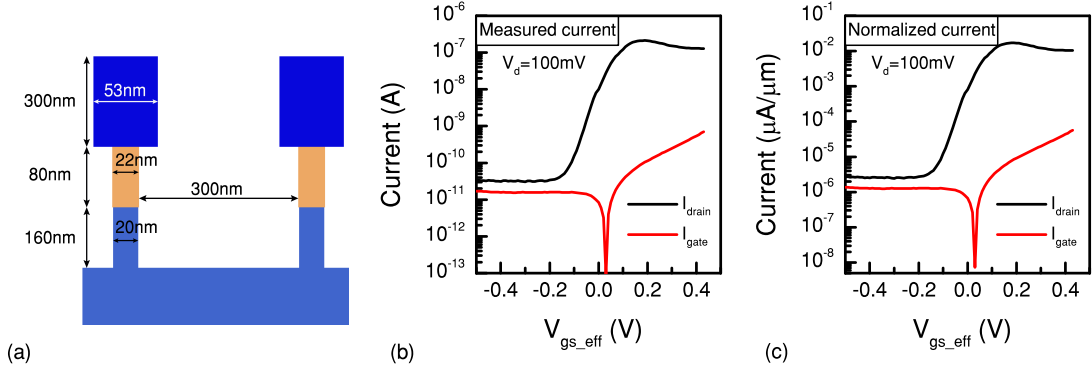


Figure 4.22 – Normalizing the measured current of nanowire InGaAs TFETs. (a) shows the schematic diagram of the employed reference TFETs in the PZT and Si:HfO₂-based NC-TFETs. In both cases, the baseline device has 184 nanowires with the presented dimensions and a pitch of 300 nm. The measured and normalized values of the drain and gate currents are demonstrated in (b) and (c), respectively.

the DC electrical performance of the proposed Si:HfO₂-based NC-TFET is demonstrated and compared with reported NC-FETs in Table 4.1. The proposed NC-TFET with a minimum swing of 15 mV/decade, a sub-thermal swing over 5 decades of current, A relatively high I_{ON}/I_{OFF} ratio of 5, and an extremely low *off*-current together with a negligible hysteresis below 50 mV, shows a significant performance boosting.

4.5.6 Current normalization

All the reported normalized current values of this section were calculated with respect to the channel width of the baseline transistor. The reference devices that have been employed for both PZT and Si:HfO₂-based NC-TFETs have the same physical dimensions, as it is schematically depicted in Figure 4.22-a. Each transistor consists of 184 nanowires, having a pitch of 300 nm. The real measurement data and the normalized value of the gate and drain current, belongs to the reference device of the Si:HfO₂-based NC-TFET, are reported in Figures 4.22-b and 4.22-c.

4.6 InGaAs planar NC-TFETs

In this section, we report the universal boosting impact of a true negative capacitance (NC) effect on digital and analog performances of TFETs, mirrored in near hysteresis-free experiments and exploiting the S-shaped polarization characteristics. Well behaved InGaAs TFETs with a minimum swing of 55 mV/decade at room temperature are combined with high-quality single crystalline PZT capacitors, placed in series with the gate. When fully satisfying the exact NC matching conditions by a single crystalline ferroelectric that can perform a mono-domain state, a hysteresis-free (sub-10 mV over 4

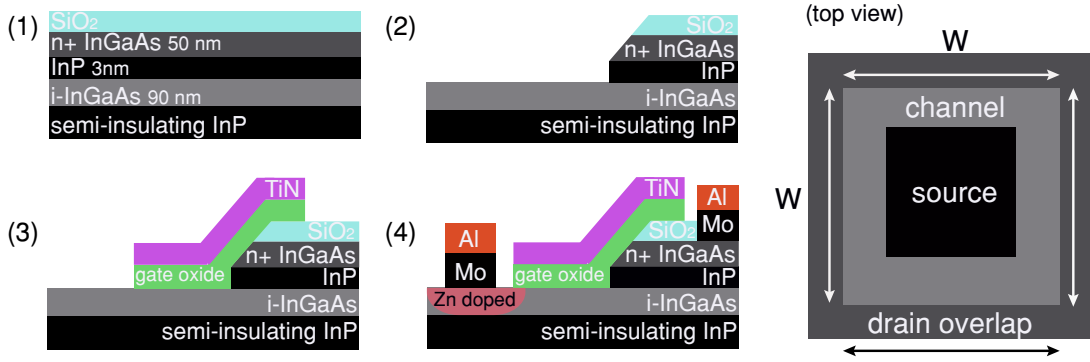


Figure 4.23 – Process flow and the cross-section schematic of the InGaAs planar TFET. (1) MOCVD growth and SiO₂ deposition. (2) drain isolation etch. (3) gate stack (1 nm Al₂O₃ + 2 nm HfO₂) ALD deposition and patterning. (4) Zn diffusion from the gas phase at 500° C for 60 seconds and source/drain contacts with the lift-off process. Finally, devices are annealed in the forming gas at 400° C for 15 minutes.

decades of current) NC-TFET with a sub-thermionic swing and an SS_{min} of 40 mV/decade is demonstrated. In other devices, improvement in the subthreshold swing, down to 30 mV/decade, and analog current efficiency factor, up to 180 V⁻¹, are achieved in NC-TFETs with a hysteresis as small as 30 mV. Importantly, the I_{60} FoM of the TFET is improved up to 2 orders of magnitude. The supply voltage is thereby reduced by 50%, down to 300 mV, providing the same drive current. These results show that NC can open a new direction as a universal performance booster in the FET design by significantly improving the low I_{60} and low overdrive of TFETs.

A major drawback of most reported NC devices is that they show large hysteresis, as little effort was dedicated to the analytical design to correctly fulfill the conditions of negative capacitance, which in theory should provide hysteresis-free characteristics as it was previously mentioned. Many of the reported hysteretic and claimed NC devices are, in fact, exploiting a ferroelectric polarization switching and do not meet the initial NC theory of Salahuddin [18], later refined by our group [74]. The important value of the NC effect, with a proper design and matched conditions, is that it can act as a universal swing and *on*-current booster for any field-effect device.

In this section, we have combined the tunneling of carriers as the operation principle with a NC gate and experimentally demonstrated NC-TFETs. Here, InGaAs ring TFETs are investigated as the baseline transistors with a sub-thermionic swing down to 55 mV/decade at room temperature. Single crystalline PZT capacitors with the ability to form a mono-domain state are employed as the NC booster. Firstly, an NC-TFET with a hysteresis as small as 30 mV shows a significant performance boosting in NC operation conditions. An improved SS down to 30 mV/decade together with an enhanced current efficiency factor, g_m/I_d , up to 180 V⁻¹ highlights the important point that the NC effect simultaneously enhances both digital and analog performances of TFETs. In a fully

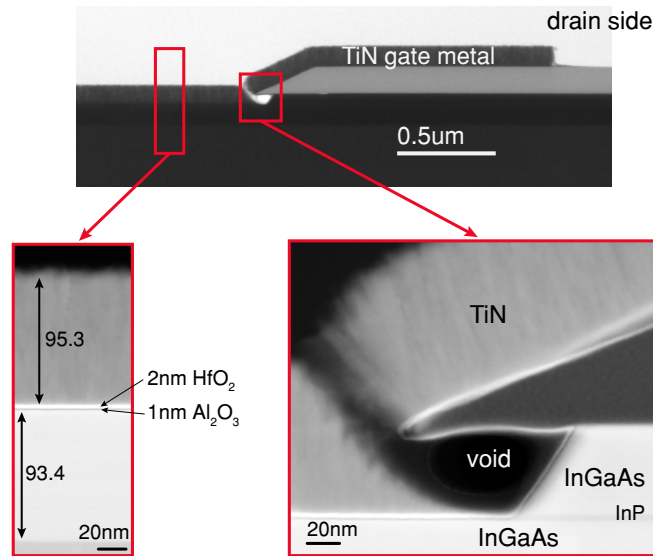


Figure 4.24 – TEM image of the InGaAs planar TFET, showing a clean surface along the channel and source and a void at the drain to avoid ambipolar current.

matched design of capacitances, a hysteresis-free NC-TFET with a sub-60 mV/decade swing down to 40 mV/decade, an enhanced g_m/I_d factor with a maximum value of 120 V^{-1} , and an improved I_{60} by nearly 2 orders of magnitude, is achieved.

4.6.1 InGaAs planar TFETs

InGaAs homojunction TFETs with 53% In content and a sub-60 mV/decade swing are used as the baseline devices [164]. The fabrication process starts with the Metal Organic Chemical Vapor Deposition (MOCVD) growth of the III-V stack on an InP substrate. The stack consists of a 10 nm InP seed layer, a 90 nm thick doped $In_{0.53}Ga_{0.47}As$ layer as the channel material, 3 nm of InP etch stop layer and a 50 nm n+ $In_{0.53}Ga_{0.47}As$ drain layer. A SiO_2 layer is then deposited as the hard mask and the drain is defined through wet etching (Figure 4.23). The gate stack is deposited next with ALD and consists of a bilayer of Al_2O_3 (1 nm) and HfO_2 (2 nm) (Figure 4.24). The EOT for the gate stack is about 0.8 nm. A 100 nm TiN layer is then deposited as the gate metal and is etched to define the source, which is doped via Zn diffusion. The room temperature transfer characteristic and the gate current on the same plot are depicted in Figure 4.25. The TFET achieves a sub-thermionic swing, down to 55 mV/decade, for all drain voltages.

4.6.2 Single crystalline PZT as ferroelectric

For this experiment, 46 nm of high-quality epitaxial $Pb(Zr,Ti)O_3$ (PZT) was grown by pulsed laser deposition on a (110) $DyScO_3$ (DSO) substrate. A 20 nm $SrRuO_3$ (SRO)

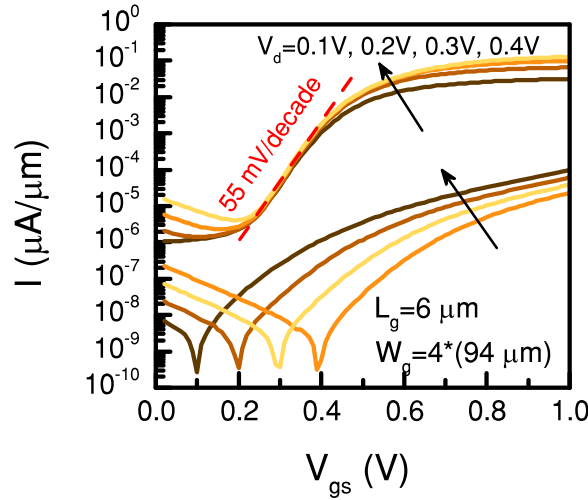


Figure 4.25 – I_d - V_g and I_g - V_g plots of an InGaAs TFET with a gate length of $6 \mu\text{m}$ for different drain voltages.

layer was grown between the substrate and PZT film to serve as the bottom electrode. A 50 nm Pt layer is sputtered and patterned using the shadow masking technique. Figure 4.26-a depicts the schematic of the PZT capacitor (top) along with the crystal structure of PZT in its two stable polarization states (bottom). Reflection high-energy electron diffraction (RHEED) (Figure 4.26-b) and XRD (Figure 4.26-c) analysis of the deposited layer confirm the crystallinity as well as the coherency of the epitaxial interface, without any grain boundaries or other extended defects. The polarization hysteresis loop measured at 100 Hz shows a remanent polarization of $80 \mu\text{C}/\text{cm}^2$ and coercive voltages of $\pm 1.2 \text{ V}$ (Figure 4.26-d). The surface of the PZT layer is conformal and the polarization in all c-domains is oriented from bottom to top interface as confirmed by piezoelectric force microscopy (Figure 4.26-e).

4.6.3 InGaAs planar NC-TFET with a sub-30 mV hysteresis

Here, we report a hysteretic NC-TFET where the gate stack of the reference TFET ($L_g = 6 \mu\text{m}$ and $W_g = 4 \times 94 \mu\text{m}$) is loaded with a PZT capacitor with an estimated area of $15 \mu\text{m} \times 15 \mu\text{m}$. The V_g is swept from -1 V to 2 V and back to the starting point while the drain voltage is set to 200 mV. In order to decouple the effect of the threshold voltage (V_{TH}) variation, curves are plotted with respect to the effective gate voltage: $V_{gs_eff} = V_{gs} - V_{TH}$. Figure 4.27-a compares the I_d - V_g plot of the NC-TFET with the baseline device. The NC of the ferroelectric is partially stabilized, as is schematically explained in Figure 3.1, leading to a small hysteresis (ΔV_{TH}) of 30 mV, while V_{TH} is extracted at $I_d = 10^{-3} \mu\text{A}/\mu\text{m}$. The small hysteresis of 30 mV suggests that this condition is not fulfilled only in a limited region [115]. The subthreshold swing is significantly lowered, down to 30 mV/decade, and a sub-60 mV/decade swing over about 3 decades of current

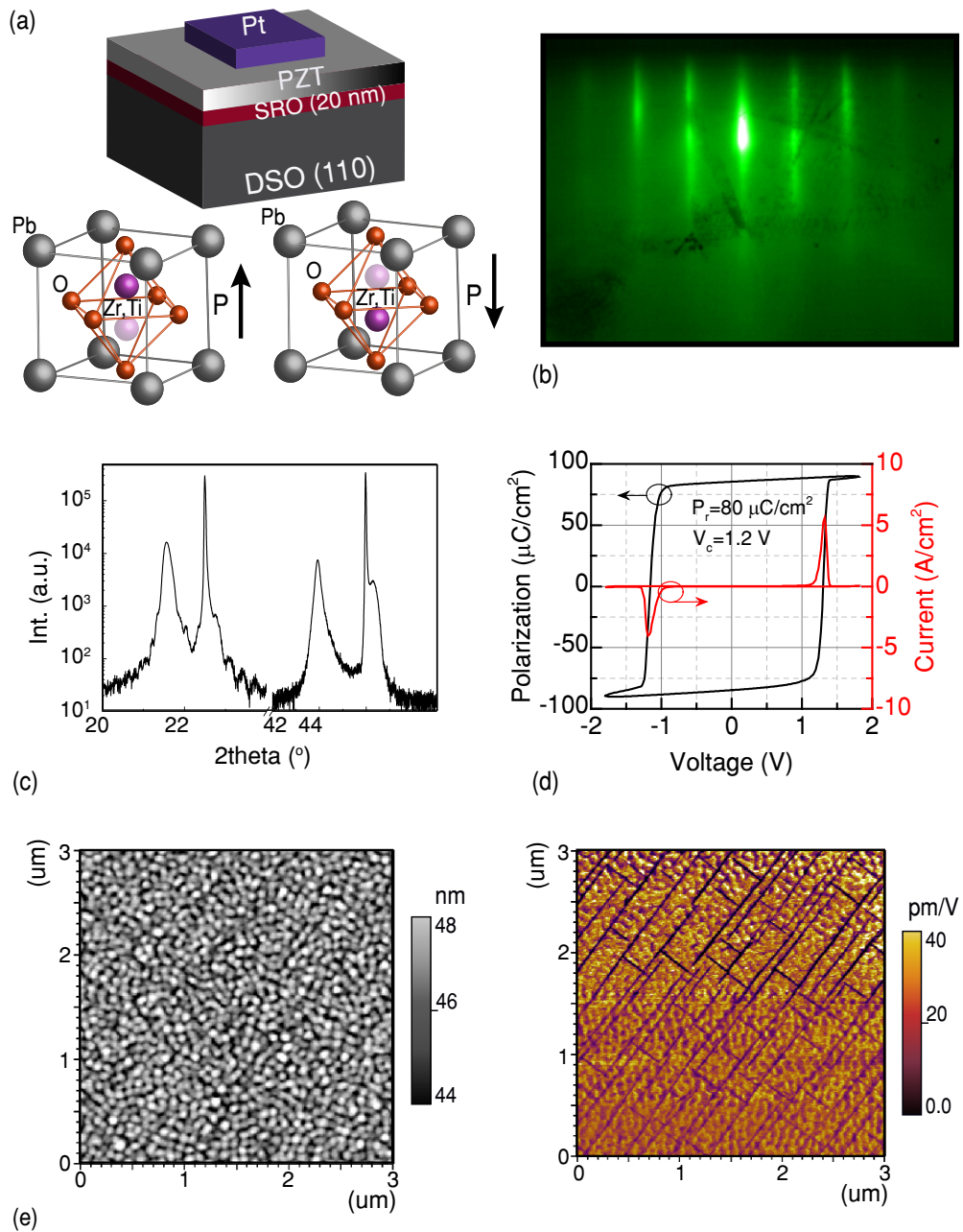


Figure 4.26 – Single crystalline PZT as NC booster. (a) Schematic of a PZT capacitor (top) and the two stable polarization states of PZT, which occur due to ionic movement (bottom). 46 nm of PZT was grown on a (110) DyScO_3 (DSO) substrate. RHEED (b) and XRD (c) analysis of the surface of the deposited PZT confirm the crystallinity of the layer as well as the coherency of the epitaxial interface. (d) The P-V and I-V curves of the PZT capacitor show a sharp and coherent switching. (e) The AFM measurement demonstrates a smooth surface (left) and the piezo-force microscopy confirms that the polarization in all c-domains of PZT is oriented from bottom to top interface (right).

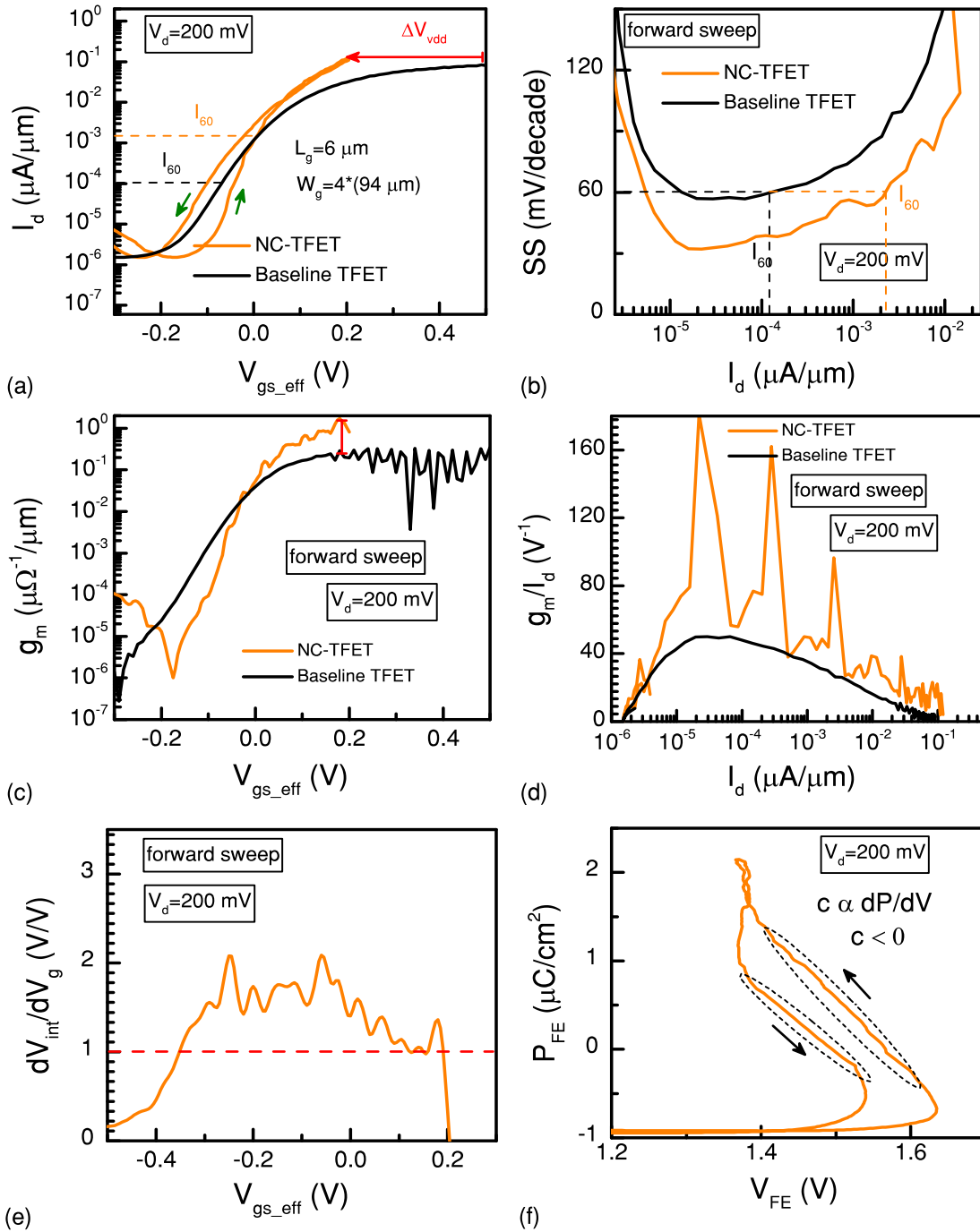


Figure 4.27 – Small-hysteresis InGaAs planar NC-TFET. (a) I_d - V_g curve of the NC-TFET compared to the base TFET ($V_d=200$ mV). (b) The SS is significantly reduced, down to 30 mV/decade. (c) g_m is enhanced, up to 10 times of its original value. (d) g_m/I_d is also improved, having a peak of 180 V^{-1} . (e) A voltage gain, $dV_{int}/dV_g > 1$, over about 50% of the device operation range is observed. (f) The extracted S-shaped P-V of the PZT capacitor confirms the existence of an effective NC.

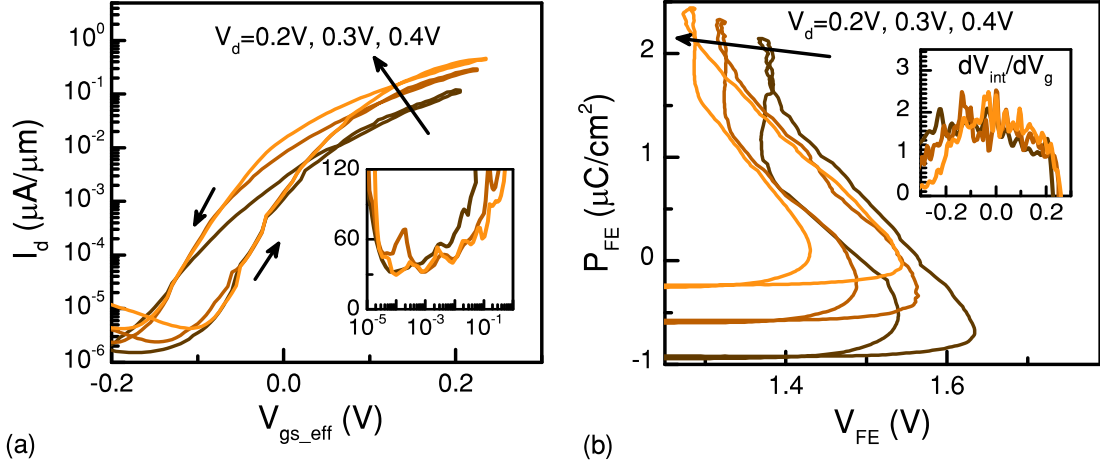


Figure 4.28 – Impact of the drain voltage variation on the InGaAs NC-TFET shows no major impact on the I_d - V_g (a) and P-V (b) curves of the NC-TFET, confirming a sub-60 mV/decade swing over almost 4 decades of current.

is obtained (Figure 4.27-b).

The I_{60} FoM, which is the maximum current below which the TFET still has a sub-60 mV/decade swing, is improved by more than one decade. Figure 4.27-c demonstrates that the transconductance (g_m) also has a steeper transition and its maximum value is improved by a factor of 10. The extracted g_m/I_d factor, an analog FoM of transistors, is remarkably improved and reached a maximum value of 180 V^{-1} (Figure 4.27-d). To quantitatively determine the voltage amplification of the NC, the internal node is measured and the dV_{int}/dV_g curve, defined as the internal gain of NC, is plotted in Figure 4.27-e. A voltage amplification up to 2 with an average of 1.5 is observed over 40% of the operation range. This internal amplification allows the surface potential to change faster than the gate voltage, leading to an enhanced tunneling probability and a reduced subthreshold swing. Due to the voltage amplification, the NC-TFET can demonstrate the same output current at a supply voltage of 0.3 V, which is 50% lower than the one of the reference TFET. The existence of NC effect is confirmed by extracting the P-V characteristic of the PZT capacitor during the NC-TFET operation, which displays a clear S-shape (Figure 4.27-f).

Figure 4.28 summarizes the impact of the source-to-drain electric field on the electric performance of the same NC-TFET. The drain voltage is varied from 200 mV to 400 mV while the source contact is grounded. Besides the common impact of V_d on the increase of on -current, it does not severely affect the electrical properties of the NC-TFET. Generally, the variation of V_d changes the operation point of the transistor, the intersection of the TFET charge line and the negative slope of the polarization, which is expected to affect the NC-TFET electrical performances [129]. However, in contrast to polycrystalline ferroelectrics, the employed single crystalline PZT capacitor provides a uniform NC over

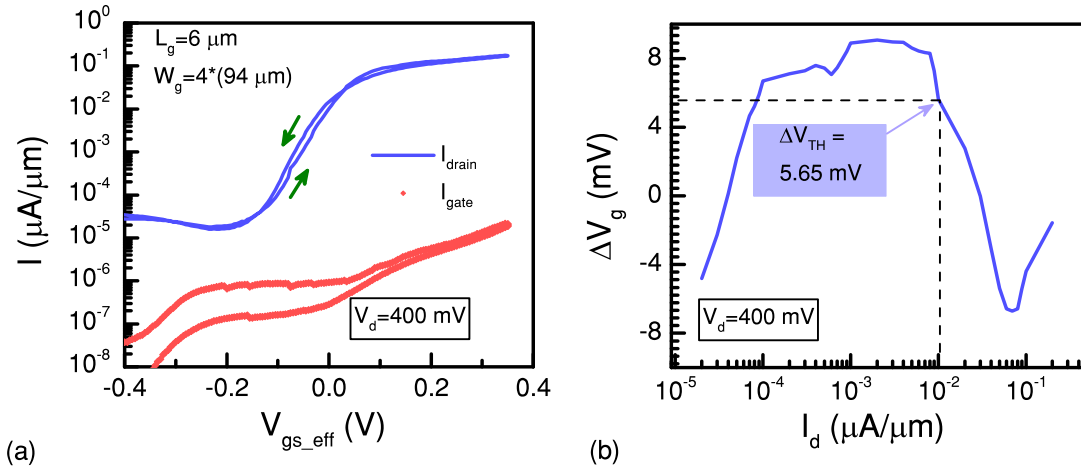


Figure 4.29 – Hysteresis-free InGaAs planar NC-TFET. (a) I_d - V_g and I_g - V_g curves of the NC-TFET at a drain voltage of 400 mV, showing a sub-10 mV hysteresis over the whole range of operation (b).

a wide range of applied gate voltages. Therefore, the variation of the operation point does not change the value of the ferroelectrics NC, leading to a similar subthreshold swing and voltage gain for different drain voltages.

4.6.4 Near Hysteresis-free (sub-10 mV) InGaAs planar NC-TFET

In a different structure, the gate stack of the InGaAs planar TFET is loaded with a PZT capacitor, having the same thickness and with a smaller area of $10 \mu\text{m} \times 10 \mu\text{m}$, close to the ideal NC matching conditions. Thereby, a hysteresis-free transfer characteristic of the NC-TFET, around 5 mV at $I_d = 10^{-2} \mu\text{A}/\mu\text{m}$, is achieved (Figure 4.29-a). A sub-10 mV hysteresis over the whole range of operation is evidenced (Figure 4.29-b). A single crystalline ferroelectric that can exhibit a mono-domain state is essential to fulfill the matching conditions. The gate voltage was swept from -1 V to 2 V and back to -1 V at the drain voltage of 400 mV. The gate leakage is negligible compared to I_d and is not impacting the reported effects.

Figure 4.30-a compares the I_d - V_g curves of the NC-TFET and its baseline transistor, showing a remarkable improvement in the steepness of the *off*-to-*on* transition, which allows reducing the supply voltage by 50%. Figure 4.30-b depicts the SS, showing a sub-60 mV/decade swing down to 40 mV/decade. The I_{60} parameter is improved by 2 orders of magnitude and reaches a value of $10 \text{ nA}/\mu\text{m}$. The transconductance of the NC-TFET exhibits an improvement in the overdrive region, up to 6 times of its original value (Figure 4.30-c). The internal node measurement confirms the non-hysteretic operation of PZT as the step-up voltage transformer (Figure 4.30-d). The internal gain, dV_{int}/dV_g , demonstrates an effective gain higher than 1 over 50% of the NC-TFET operation range (Figure 4.30-e). The polarization characteristic of the PZT capacitor is

Table 4.2 – Boosting of digital and analog performances of the hysteresis-free InGaAs planar NC-TFET compared the baseline TFET at $V_d=400\text{mV}$.

	SS_{min}	sub-thermionic range	Hysteresis
TFET	55 mV/decade	$10^{-5}\text{-}10^{-4} \mu\text{A}/\mu\text{m}$	-
NC-TFET	40 mV/decade	$10^{-5}\text{-}10^{-2} \mu\text{A}/\mu\text{m}$	± 10 mV
	V_{DD} ($I_{on}=0.1 \mu\text{A}/\mu\text{m}$)	I_{60}	$(g_m/I_d)_{max}$
TFET	0.6 V	0.1 nA/ μm	50 V^{-1}
NC-TFET	0.3 V	10 nA/ μm	120 V^{-1}

extracted (Figure 4.30-f), showing an effective NC over a wide range of operation.

Overall, NC effect can be employed as an effective universal performance booster of FETs, significantly improving the SS and overdrive. By properly satisfying the matching condition, a hysteresis-free NC-TFET, suitable for logic applications, can be achieved. A well-designed negative capacitor integrated to the gate stack of a TFET significantly increases both I_{60} and the drive current, which are the main challenges involved in the fabrication of TFETs (see Table 4.2).

Extrapolating the improvements to state-of-the-art TFETs [30], the NC effect brings a MOSFET competitive $I_{60} = 10 \mu\text{A}/\mu\text{m}$ within reach. The novelty and universality of this approach relate to the fact that the gate stack is not anymore a passive part of a field-effect transistor and contributes to the signal amplification. Therefore, an NC booster can be applied in parallel with other conventional performance boosters of TFETs.

4.7 Summary

In conclusion, negative capacitance tunneling field-effect transistors are proposed as one of the most promising steep-slope energy efficient switches, which is required for the recent advancements of the Internet of Things (IoT) technology. It is experimentally validated in this chapter that the NC effect, with the possibility to be applied in parallel with any other performance boosters, significantly enhances both analog and digital figures of merit of TFETs. A negative capacitance TFET that benefits from the internal voltage amplification of the ferroelectric's NC together with the band-to-band tunneling as the carrier injection mechanism provide an average subthreshold swing much lower than the thermal limit of MOSFETs. This enables the simultaneous scaling of the supply voltage and power per operation. The use of a series-connected NC booster to the gate of TFETs improves the I_{ON}/I_{OFF} ratio together with a significant enhancement of the subthreshold swing, the main challenges involved in the fabrication of TFETs.

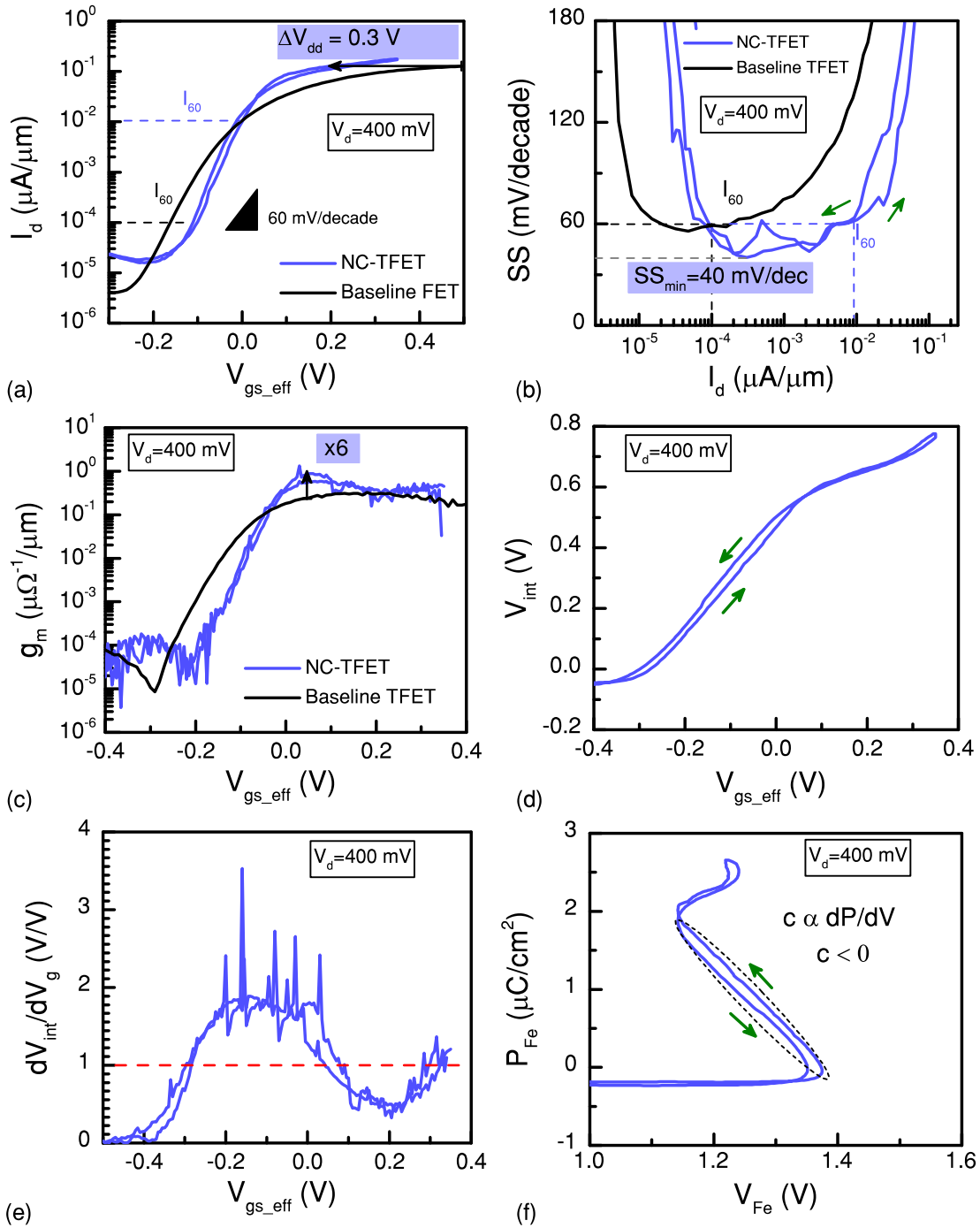


Figure 4.30 – (a) Transfer characteristic of the NC-TFET is compared with the base device, confirming a significant improvement in the swing (b). Transconductance is also improved (c). The voltage of the internal node is measured (d) and a clear voltage gain over 50% of the operation range is observed (e). The extracted P-V plot confirms the existence of an effective NC with a negligible hysteresis (f).

The impact of NC on TFETs operation is first confirmed on moderate silicon nanowire array TFETs. Afterward, the measured input transfer characteristic of an InAs/InGaAsSb/GaSb nanowire TFET benefits from a series-connected PZT capacitor to the gate, demonstrating a super steep transition of 10 mV/decade together with an improved I_{ON}/I_{OFF} ratio and an enhanced current efficiency factor up to 3000 V^{-1} . In another device configuration, using silicon-doped HfO_2 as ferroelectric, a minimum subthreshold swing of 15 mV/decade is achieved while the reference device shows and SS_{min} of 54 mV/decade. It is evidenced that the NC effect not only reduces SS_{min} , also extends the low-slope region of the input transfer characteristics of TFETs. An average swing of 30 mV/decade over five decades of current is obtained. It is also shown that with a proper capacitance matching, the hysteretic behavior of NC-TFETs can be alleviated, leading to a negligible hysteresis of 50 mV. The impact of the source-to-drain electric field on the operation of NC-TFETs is also discussed, showing that the boosting effect is reduced by increasing the drain voltage.

In another experiment, near hysteresis-free InGaAs planar NC-TFETs with a sub-thermionic swing over about 4 decades of current and a minimum of 30-40 mV/decade are experimentally demonstrated by fulfilling the NC matching conditions. The supply voltage can be reduced by 50%, down to 0.3-0.4 V, as a result of the overdrive improvement by NC. The NC effect also enhances the analog FoM of TFETs, in addition to digital performances, showing a new path to advance the performance engineering of TFETs for improved efficiency. By its insights and reported experiments, this chapter proposes a new path to address the most limiting performances of TFETs, while a negative capacitance booster is properly designed and integrated into their gate stack.

5 Ferroelectric Tunnel FET as Low Power non-Volatile Memory

Abstract:

The implementation and operation of nonvolatile ferroelectric memory (NVM) tunnel field-effect transistors, using silicon-doped HfO_2 as ferroelectric, is proposed and theoretically examined. It is theoretically demonstrated that the FeTFET can operate as an ultra-low power nonvolatile memory even in aggressively scaled dimensions. A FeTFET analytical model is derived by combining the pseudo 2-D Poisson equation and Maxwell's equation. The model describes the FeTFET behavior when a time-dependent voltage is applied to the device with a hysteretic output characteristic due to the ferroelectric's dipole switching. The theoretical results provide unique insights into how the device geometry and ferroelectric properties affect the FeTFET transfer characteristic. The recently explored ferroelectric, silicon-doped HfO_2 , is employed as the gate ferroelectric. With the ability to engineer ferroelectricity in HfO_2 thin films, a high-k dielectric well established in the semiconductor industry, a new route for improved manufacturability and scalability of future 1-T ferroelectric memories is opened. In this chapter, a Si:HfO₂ based FeTFET with a sufficiently large memory window and low power dissipation is designed and simulated. Utilizing our presented model, the device characteristics of a FeTFET that takes full benefits from Si:HfO₂ is compared with the same devices using well-known perovskite ferroelectrics. Finally, the FeTFET is compared with a conventional ferroelectric memory transistor highlighting the advantages of using a FeTFET for memory applications.

Ferroelectric materials can be utilized as electrically switchable nonvolatile data storage elements as their polarization can change by applying an external electric field. Recently, novel devices called ferroelectric transistors [157] have been proposed as promising candidates for the future of nonvolatile memories [165, 166]. In ferroelectric field-effect devices, two stable states of the ferroelectric's polarization are used for data storage [167]. Nonvolatile data storage, fast writing, and nondestructive read-out operation have been reported for ferroelectric FETs [168]. However, the industrial implementation of ferroelectric devices, especially in nanoscale, is still missing due to the integration and scaling obstacles of conventionally used perovskite type ferroelectrics such as Lead Zirconate Titanate (PZT). The recently discovered ferroelectricity in HfO₂ thin films [60], enabled CMOS-compatible manufacturing of highly scaled ferroelectric devices down to 28 nm ground rule [60, 169].

By scaling devices down to the nanoscale, power density becomes a challenging issue as the power density per area of the chip increases. TFETs have been investigated intensely in recent years [170] due to their considerable potentials for ultra-low power applications [171, 15]. Using the advantages of both ferroelectric thin films for data storage and TFETs as energy efficient devices, it is possible to design a new class of nonvolatile memories, with a relatively large memory window, fast writing, nondestructive read-out operation, and low power consumption. In this work, we propose a comprehensive, quantitative model for investigation of FeTFETs. The successful design of a FeTFET for nonvolatile data storage requires a thorough understanding of the device operation principals. It is necessary to develop an analytical model for FeTFETs design optimization. Hence, an analytical model is proposed and verified with Sentaurus TCAD [172] simulation tool. The model is developed by solving the 2-D Poisson equation [28] for a single gate TFET and considering the effect of the ferroelectric polarization on the surface potential. The polarization effect is calculated by solving the Maxwell's first equation in the gate stack. A numerical method is employed to calculate the polarization hysteresis for both saturated and nonsaturated hysteresis loops [173].

Based on our proposed model, the memory window of the ferroelectric memory TFETs using different ferroelectric materials is investigated. It should be noted that short channel effects are neglected in the proposed model, and a 200 nm gate length device is utilized for model verification. Finally, a 28 nm gate length FeTFET benefits from Si:HfO₂ as the gate ferroelectric is designed and simulated using Sentaurus TCAD commercial simulator. Results confirm the potentials of the proposed structure for the future of low power nonvolatile memories. Moreover, we present that the ferroelectric's negative capacitance improves the output current of TFETs by amplifying the gate potential.

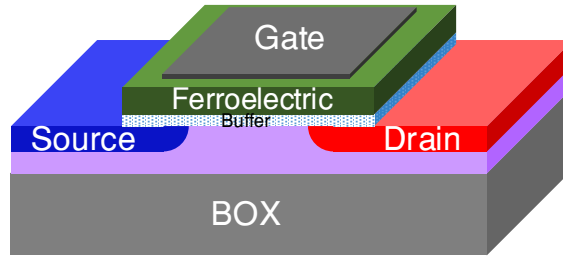


Figure 5.1 – Device schematic of an SOI FeTFET where the gate stack of a conventional single gate TFET is replaced by a series combination of a ferroelectric and a linear dielectric.

5.1 Device modeling

5.1.1 Approach and definitions

Here, an n-type SOI ferroelectric TFET is studied. The device is schematically depicted in Figure 5.1. The length of the channel is considered 200 nm to suppress short channel effects, the doping concentration of the lightly doped channel is $5 \times 10^{14} \text{ cm}^{-3}$, the highly doped p+ source concentration is $1 \times 10^{20} \text{ cm}^{-3}$ and the n+ doped drain is $1 \times 10^{18} \text{ cm}^{-3}$ to eliminate the ambipolar behavior [173]. Si:HfO₂ is utilized as the ferroelectric layer due to its unique property of exhibiting the ferroelectricity even in a 5 nm thick, thin film [124, 174]. For the model verification, we have used 10 nm of Si:HfO₂ with a remanent polarization of $9 \mu\text{C}/\text{cm}^2$ and a coercive field of 1.1 MV/cm [60]. We will discuss later on this chapter that how the relatively high coercive field and remanent polarization guarantee a large memory window (which can be translated into a longer retention time) in ferroelectric memory TFETs.

To develop the FeTFET model, we have combined the switching analytical modeling of ferroelectric capacitors [175] with the band-to-band tunneling modeling of TFETs. Wu et al. [28] proposed the analytical modeling of TFETs based on the gate and drain dual modulation effects by solving the Poisson equation in the device channel. Miller et al. [176, 173, 177] developed the compact modeling of ferroelectric capacitors that accurately describes the dipole polarization switching by employing Maxwell’s first equation. We employed the Maxwell and Poisson equations consistently to precisely calculate the surface potential profile along the channel. Finally, the device current is calculated by determining the potential profile around the tunneling junctions. The computer-aided design (TCAD) tool, Sentaurus, is used to verify the proposed model. The non-local BTBT model is enabled to take into account the tunneling mechanism [178]. In order to calculate the tunneling probability using the electron-hole wave vector throughout the tunneling path, the non-local model uses Wetzels-Kramer-Brillouin (WKB) approximation.

Also, Fermi statistics and Shockley-Reed-Hall (SRH) recombinations are adopted while the gate tunneling is ignored. In order to incorporate the ferroelectric properties of the gate stack, we have enabled the Ferro model of Silvaco in our simulations. Moreover, the standard library of Sentaurus TCAD is used for linear dielectrics (where the SiO₂ and Si₃N₄ relative permittivity is 3.9 and 7.5 respectively). These models are considered in all TCAD simulations unless otherwise mentioned. It should be noted that the ferroelectric layer is considered ideal from the point of view of hysteresis loss related issues like fatigue (loss of switched charge owing to repetitive destructive reads), retention (decreasing the stored charge to a level where the positive and negative state of the polarization cannot be reliably sensed), and direct current breakdown (as a result of applying constant writing voltage) [179].

5.1.2 Model

In this subsection, we describe the relationship between the ferroelectric polarization and the silicon surface potential in an MFIS structure [180]. The electrostatic equations are derived starting with Maxwell's equation,

$$\nabla \cdot D = \rho, \quad (5.1)$$

$$D = \epsilon_0 \epsilon E + P_d, \quad (5.2)$$

where D is the displacement, ρ is the free charge density, E is the electrical field, ϵ_0 is the vacuum permittivity, ϵ is the linear dielectric constant, and P_d is the contribution of the switching dipoles. Solving equation 5.1 and 5.2 in conjunction with the definition $E = -\nabla \phi$ (ϕ is the electrostatic potential) leads us to

$$V_{gb} = \phi_s - \frac{\sigma_s}{C_{stack}} - P_d(E_{FE}) \frac{d_{FE}}{\epsilon_0 \epsilon_{FE}}. \quad (5.3)$$

In equation 5.3, C_{stack} describes the gate total capacitance, σ_s is the silicon charge, d_{FE} and ϵ_{FE} are ferroelectric thickness and relative permittivity and ϕ_s is the silicon surface potential. The ferroelectric polarization changes the surface potential by a value of $P_d(d_{FE}/\epsilon_0 \epsilon_{FE})$. The ferroelectric polarization can also be calculated using the Landau-Khalatnikov theory [181, 182, 183]. Using Landau theory, equation 5.3 can be rewritten as follow

$$V_{gb} - \phi_s + \frac{\sigma_s}{C_{buffer}} = (2\alpha t_{FE}) P_d(E_{FE}) + (4\beta t_{FE}) P_d^3(E_{FE}) + (6\gamma t_{FE}) P_d^5(E_{FE}), \quad (5.4)$$

where α , β , and γ are the ferroelectric Landau parameters, t_{FE} is the ferroelectric thickness, and C_{buffer} is the capacitance of the buffer layer. The FeTFET modeling can

be obtained using either equation 5.3 or 5.4. However, equation 5.3 is employed in this study to derive an analytical model for the device operation.

We explain the FeTFET behavior by considering the effect of the polarization on the surface potential for a known polarization. Combining Maxwell's first equation with Wu's analytical solution for TFET surface potential [28], the surface potential in the middle of the channel for the whole range of the operation can be given as

$$\phi_{ch}=F+\frac{kT}{q}\ln\left[1+\frac{q}{kT}(\sqrt{F}/(\sqrt{F}+\gamma))(V_{gs}-V_{fb}+P_d\frac{d_{FE}}{\epsilon_0\epsilon_{FE}}-F)+\frac{q}{2kT}(F/(\sqrt{F}+\gamma)^2-\gamma(F-2)/(2(\sqrt{F}+\gamma)^3))(V_{gs}-V_{fb}+P_d\frac{d_{FE}}{\epsilon_0\epsilon_{FE}}-F)^2\right], \quad (5.5)$$

$$F=\frac{1}{2}[V_{ds}+\Phi+\phi_{ch,dep}-((\phi_{ch,dep}-V_{ds}-\Phi)^2+\delta^2)^{1/2}], \quad (5.6)$$

$$\phi_{ch,dep}=[(V_{gs}-V_{fb}+P_d\frac{d_{FE}}{\epsilon_0\epsilon_{FE}}+\frac{\gamma^2}{4})^{1/2}-\frac{\gamma}{2}]^2, \quad (5.7)$$

where V_{fb} is the flat band voltage, T is the temperature, k is the Boltzmann's constant, q is the electrical charge of a single electron, γ is the body factor defines as $\sqrt{2\epsilon_{si}qN_{ch}/C_{stack}}$ (N_{ch} is the channel doping), δ is a small smoothing factor and $\phi_{ch,dep}$ is the surface potential in the gate control regime [28]. ϕ is the required surface potential for sufficient inversion charge to screen the gate modulation and can be expressed as $(kT/q)\ln(N_{ch}N_{inv}/n_i^2)$, and N_{inv} is the required inversion charge density to screen the gate voltage.

An accurate expression of the surface potential profile around the tunnel junction is needed to calculate the tunneling current. We use the pseudo 2-D Poisson equation to obtain the potential profile along the channel [184]. The parabolic approximation of the potential in a direction normal to the surface is adopted so that the Poisson equation can be reduced to the well-known form

$$\frac{d^2\phi_s(x)}{dx^2}-(1/\lambda^2)[\phi_s(x)-(V_{gs}-V_{fb}+P_d\frac{d_{FE}}{\epsilon_0\epsilon_{FE}})]=\frac{qN_{ch}}{\epsilon_{si}}, \quad (5.8)$$

where $\lambda=\sqrt{\epsilon_{si}t_{si}/C_{stack}}$ (t_{si} and ϵ_{si} represent the silicon thickness and relative permittivity) is the characteristic length of the channel [28]. Solving equation 5.8 by considering the boundary conditions and the continuity of potential and electric field at the source-channel and channel-drain junctions, the surface potential profile around the tunneling

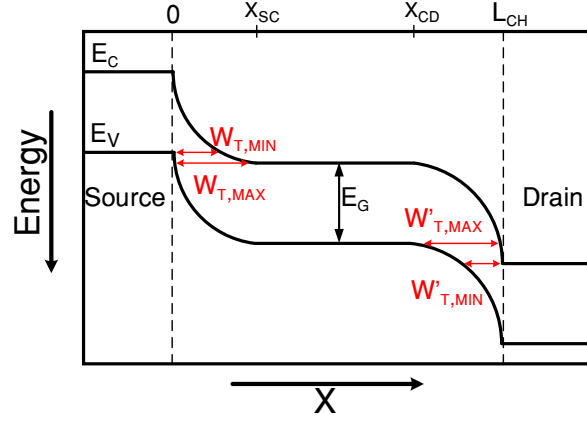


Figure 5.2 – Energy bands in a TFET indicating the maximum and minimum of the tunneling width in the source-channel and channel-drain junctions [28]. x_{sc} and x_{cd} represent the source and drain tunneling junction width.

junctions can be obtained as

$$\phi_s(x) = (V_{gs_eff}) + (\phi_{ch} - V_{gs_eff}) \cosh\left(\frac{x - x_{sc}}{\lambda}\right) \dots 0 \leq x \leq x_{sc}, \quad (5.9)$$

$$\phi_s(x) = (V_{gs_eff}) + (\phi_{ch} - V_{gs_eff}) \cosh\left(\frac{x - x_{sd}}{\lambda}\right) \dots x_{cd} \leq x \leq L_{ch}, \quad (5.10)$$

$$x_{sc} = \lambda \cosh\left(\frac{V_{s0} - (V_{gs_eff})}{\phi_{ch} - (V_{gs_eff})}\right), \quad (5.11)$$

$$x_{cd} = L_{ch} - \lambda \cdot \cosh^{-1}\left(\frac{V_{d_eff} - (V_{gs_eff})}{\phi_{ch} - (V_{gs_eff})}\right). \quad (5.12)$$

In the performed equations, V_{s0} subscribes to the source potential, V_{d_eff} is the potential in the drain region ($V_{d_eff} = V_{s0} + V_{bi,sd} + V_{ds}$), V_{gs_eff} is the gate effective voltage ($V_{gs_eff} = V_{gs} - V_{fb} + P_d(d_{FE}/\epsilon_0\epsilon_{FE}) - (qN_{ch}/\epsilon_{si})\lambda^2$), and ϕ_{ch} is the surface potential in the center of the channel that we have derived before. The tunneling width

at the source junction can be expressed as

$$W_{t,min} = x(V_{s0} + \frac{E_g}{q}) - x(V_{s0}) = x_{sc} - \lambda \cdot \cosh^{-1}(\frac{V_{d_eff} - (V_{gs_eff})}{\phi_{ch} - (V_{gs_eff})}), \quad (5.13)$$

$$W_{t,max} = x(\phi_{ch}) - x(\phi_{ch} - \frac{E_g}{q}) = \lambda \cosh^{-1}(\frac{V_{s0} - \frac{-E_g}{q} - (V_{gs_eff})}{\phi_{ch} - (V_{gs_eff})}). \quad (5.14)$$

where $W_{t,min}$ and $W_{t,max}$ are the minimum and maximum of the tunneling width along the lateral tunneling path at the source-channel junction (the source-channel and channel-drain tunneling widths are schematically depicted in Figure 5.2). Regarding Kane's model [185], the tunneling current can be calculated by integrating the tunneling probability over the effective tunneling length,

$$I_{tunnel,s \rightarrow c} = q \cdot W \cdot \int_{W_{t,min}}^{W_{t,max}} \int_0^{t_{si}} G_{Kane} dy dx. \quad (5.15)$$

In equation 5.15, G_{Kane} is the Kane's tunneling probability factor. The tunneling current at the drain junction can be calculated similarly,

$$W'_{t,min} = x(V_{d_eff}) - x(V_{d_eff} - \frac{E_g}{q}), \quad (5.16)$$

$$W'_{t,max} = x(\phi_{ch} + \frac{E_g}{q}) - x(\phi_{ch}), \quad (5.17)$$

$$I_{tunnel,c \rightarrow d} = q \cdot W \cdot \int_{W'_{t,min}}^{W'_{t,max}} \int_0^{t_{si}} G_{Kane} dy dx, \quad (5.18)$$

where, $W'_{t,min}$ and $W'_{t,max}$ are minimum and maximum of the lateral path at the channel-drain junction. Finally, the total value of the device output current can be expressed as,

$$I_{ds} = I_{tunnel,s \rightarrow c} + I_{tunnel,c \rightarrow d}. \quad (5.19)$$

5.1.3 Dipole polarization

The value of the dipole polarization in each step is a function of the history of the applied electric field. Therefore, the polarization is determined by integrating $dP_d(E_{FE})/dE_{FE}$ from a specified initial condition. Since this form has been extensively discussed before for the arbitrary field histories [176], the results are simply stated here. The saturated polarization hysteresis loop is defined by

$$P_{+sat}(E_{FE})=P_s \tanh\left(\frac{E_{FE}-E_C}{2\delta}\right), P_{-sat}=-P_{+sat}(-E), \quad (5.20)$$

where

$$\delta=E_c\left[\ln\left(\frac{1-\frac{-P_r}{P_s}}{1-\frac{P_r}{P_s}}\right)\right]^{-1}, \quad (5.21)$$

and + (or -) superscript signifies the positive (or negative) going branch of the loop. The derivative of the polarization is given by the following equations:

$$\frac{dP_d}{dE_{FE}}=\Gamma \frac{dP_{sat}}{dE_{FE}}, \quad (5.22)$$

$$\Gamma=1-\tanh\left[\left(\frac{P_d-P_{sat}}{\xi P_s-P_d}\right)^{1/2}\right]. \quad (5.23)$$

where $\xi = +1$ when $dE/dt > 0$ and $\xi = -1$ when $dE/dt < 0$.

Considering equations 5.1 to 5.19, the FeTFET drain current can be calculated as a function of the gate voltage history, device geometry, and material properties while the dipole polarization can be obtained using equations 5.20 to 5.23. In the following section, we will present a numerical analysis technique in order to obtain the FeTFET transfer characteristic.

5.1.4 Numerical analysis technique

Since the ferroelectric polarization depends on the history of the electric field, the polarization can be obtained by integrating from a known value. For the first step, we should define the initial values for the gate voltage and the polarization. Note that the initial conditions must satisfy the physical requirement that the polarization lies on or

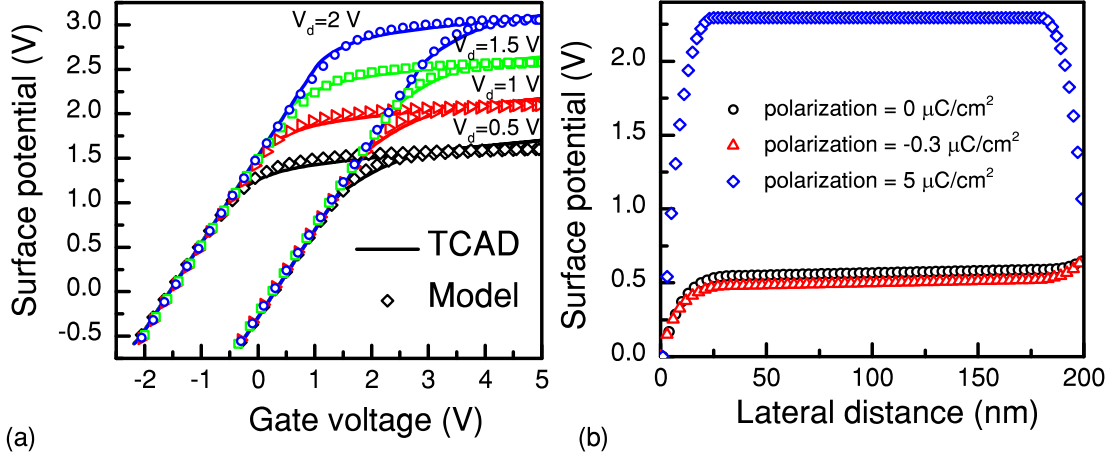


Figure 5.3 – Ferroelectric TFET surface potential. (a) Model verification of the surface potential in the middle of the channel using different drain voltages and sweeping the gate voltage with Sentaurus TCAD simulations results. (b) The surface potential profile along the channel with the polarization as a parameter. Results are obtained using the proposed model for a device with $V_g = 1$ V, $V_d = 1.5$ V, and considering the gate oxide has 0, -0.003 , and $0.05 \text{ C}/\text{m}^2$ polarization to illustrate how the positive and negative values of the polarization affect the potential profile.

within the hysteresis loop. We considered $V_g = V_{fb}$ and $P_d = 0$ as the initial condition. Having the polarization and the gate voltage, all TFET parameters are calculated using equations 5.1 to 5.19. Furthermore, the ferroelectric field and the silicon surface charge density can be calculated as follows:

$$\sigma_s = -\sqrt{2\epsilon_{si}kTN_{ch}} \left[q \frac{\phi_{ch}}{kT} + \left(\frac{n_i}{N_{ch}} \right)^2 \exp\left(q \frac{\phi_{ch} - V}{kT} \right) \right]^{\frac{1}{2}}, \quad (5.24)$$

$$E_{FE} = -(\sigma_s + P_{d_FE}) / (\epsilon_0 \epsilon_{FE}). \quad (5.25)$$

The approach to perform the integration from the initial conditions to a new set of conditions is to compute the m 'th value of the relevant quantities, and numerically integrate. We now introduce the subscript m , which signifies that the given quantity is evaluated at the m 'th integration increment. First, we should solve equations 5.1 to 5.19 to find the m 'th value of the surface potential. Then, we calculate the m 'th value of the silicon surface charge and the electric field inside the ferroelectric film using equations 5.24 and 5.25. The polarization can be expressed as

$$P_d(E_m) = P_d(E_{m-1}) + (E_m - E_{m-1}) \frac{d}{dE} [P_d(E)]_{E_{m-1}}. \quad (5.26)$$

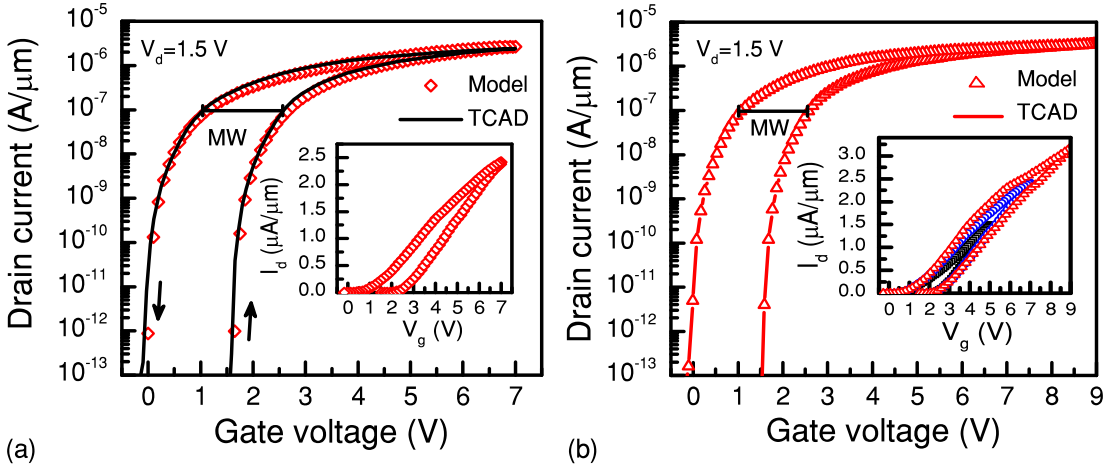


Figure 5.4 – FeTFET transfer characteristic for different drain and gate voltages. (a) FeTFET model vs. TCAD results obtained for 1.5 V drain voltage. (b) FeTFET drain current for different sweeps of the gate voltage.

Equation 5.26 can be rewritten as

$$P_d(E_m) = \frac{P_d(E_{m-1}) - \left[\frac{\sigma_s}{\epsilon_0 \epsilon_{FE}} \right] \left[\left(\frac{d}{dE} \right) P_d(E) \right]_{E_{m-1}} - E_{m-1} \left[\left(\frac{d}{dE} \right) P_d(E) \right]_{E_{m-1}}}{1 - \left(\frac{-1}{\epsilon_0 \epsilon_{FE}} \right) \left[\left(\frac{d}{dE} \right) P_d(E) \right]_{E_{m-1}}}. \quad (5.27)$$

The next value of the polarization in each step can be obtained using equation 5.27. Sweeping the gate voltage and calculating the next value of the polarization in each step, the drain current is calculated as a function of the gate voltage.

The model predicted results were verified by comparing with TCAD simulation results. The device surface potential is presented in Figure 5.3. First, we verified the surface potential in the middle of the channel, which is the primary parameter to compute the potential profile and the drain current. The surface potential profile in the middle of the channel for different drain voltages and sweeping the gate voltage is illustrated in Figure 5.3-a. Results confirm that our proposed model replicates well with the TCAD simulations. The effect of the dipole polarization on the surface potential profile along the channel is presented in Figure 5.3-b. The surface potential profile is calculated for a TFET with a 1 V gate voltage and a 1.5 V drain voltage considering the gate oxide performs no ferroelectricity, ferroelectric with -0.003 C/m^2 , and 0.05 C/m^2 values of polarization to illuminate the effect of the positive and negative values of the polarization on the potential profile. Finally, the output current of the device is shown in Figure 5.4. Figure 5.4-a represents the output current while the drain voltage is 1.5 V. The device's transfer characteristic for a drain voltage of 1.5 V and different sweeps of the gate voltage is illustrated in Figure 5.4-b.

5.2 Memory window

The memory window (MW), a critical parameter in nonvolatile memory devices, is the threshold voltage difference between the two states of the device. Here, the constant current method at 10^{-7} A/ μm is utilized for the threshold voltage extraction [186]. The memory window should be large enough to ensure a significant retention time and ease of data detection in nonvolatile memories. In this section, we discuss the quantitative influence of different device parameters that affect the memory window based on our presented model and theoretically highlight the advantages of the Si:HfO₂ ferroelectric thin film.

5.2.1 Ferroelectric material

It is well known that a FeFET memory window while the ferroelectric layer contains a sufficient remanent polarization and applying an electric field higher than the material's coercive field mostly depends on the ferroelectric coercive field and thickness. In this subsection, we investigate the effect of the ferroelectric coercive voltage on the FeTFET memory window using the same thickness of different ferroelectrics. The properties of two well-known perovskite ferroelectrics, Lead Zirconate Titanate (PZT) and Strontium Barium Titanate (SBT), are compared with Si:HfO₂ in Table 5.1. The recently discovered ferroelectric thin film, Si:HfO₂ [187, 60], has a relatively high coercive field that ensures a sufficiently large memory window [188, 189].

Table 5.1 – Ferroelectric properties of PZT [190, 191], SBT [188, 189], and Si:HfO₂ [187].

Ferro Material	$P_r(\frac{\mu\text{C}}{\text{cm}^2})$	$P_s(\frac{\mu\text{C}}{\text{cm}^2})$	$E_c(\frac{\text{MV}}{\text{cm}})$	ϵ_r
PZT	32	40	0.26	250
SBT	8	15	0.08	250
Si:HfO₂	9	9.5	1.1	32

The I_d - V_g characteristics of a FeTFET using 10 nm of PZT, SBT, and Si:HfO₂ are depicted in Figure 5.5-a. We have used the same thickness of each material to eliminate the influence of the ferroelectric thickness on the MW. The FeTFET that is using PZT or SBT as the gate ferroelectric provides higher current level due to their higher relative permittivity compared Si:HfO₂. The high dielectric constant of PZT and SBT reduces the voltage drop across the ferroelectric layer and enhances the silicon surface potential. Therefore, considering equations 5.11 to 5.14, the tunneling width at the source and drain tunneling junctions increases, which leads to an improved tunneling current.

Based on the presented results in Figure 5.5-a, Si:HfO₂ theoretically provides a larger memory window compared to the well-known ferroelectric materials PZT and SBT. Up to 1.7 V memory window is obtained for a device using 10 nm of Si:HfO₂. In Figure 5.5-b

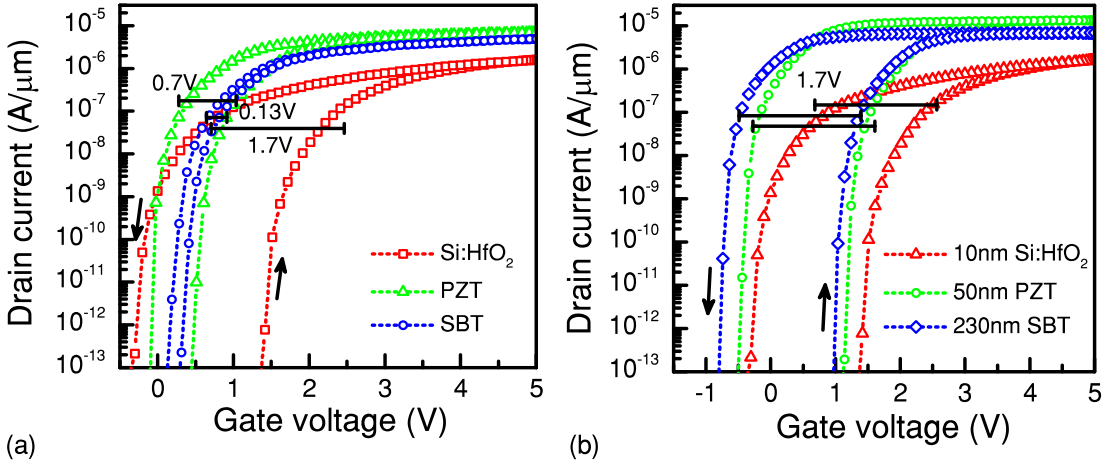


Figure 5.5 – (a) Transfer characteristic of FeTFETs using 10 nm of PZT, SBT, and Si:HfO₂ as the gate ferroelectric obtained by our proposed model. The device benefits from the Si:HfO₂ thin film provides a larger memory window due to its high coercive field while all ferroelectrics has the same thickness. (b) Transfer characteristic of FeTFETs using different thicknesses of mentioned ferroelectric materials providing the same memory window. 10 nm of Si:HfO₂, 50 nm of PZT, and 230 nm of SBT are required to provide 1.7 V memory window.

different thicknesses of PZT and SBT are used to maintain the same memory window as the FeTFET using 10 nm of Si:HfO₂. 50 nm of PZT and 230 nm of SBT is required to provide 1.7 V memory window while 10 nm of silicon-doped HfO₂ grant the same memory window. The theoretical results provide a great insight into the benefits of the silicon-doped HfO₂ ferroelectric thin film. Besides the theoretical advantages of Si:HfO₂ compared to perovskite ferroelectrics, it is challenging to fabricate a device with a thin layer of perovskites ferroelectrics due to the high relative permittivity of the PZT and SBT (over 200). Moreover, CMOS compatibility, scalability and the ability to deposit a high-quality layer by ALD are some of the technological advantages of using Si:HfO₂.

The presented MWs in Figure 5.5 are lower than the theoretical maximum of the ferroelectric field effect devices memory window ($\sim 2E_c \times d$ which is 2.2 V in the case of 10 nm Si:HfO₂) due to the depolarization field and gate leakage current effects. The depolarization field always exists in a ferroelectric capacitor due to the finite dielectric constant of the semiconductor that causes incomplete charge compensation. Moreover, the injected electrons from the gate and semiconductor to the ferroelectric layer lead to the local charge compensation and reducing polarization [192].

5.2.2 Buffer layer

Due to the large number of defects, leakage current, and large lattice mismatch between perovskite ferroelectrics and silicon, it is always necessary to use a buffer layer with a

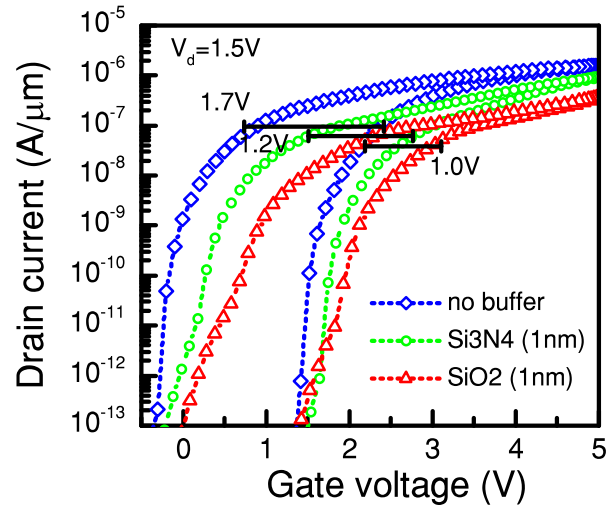


Figure 5.6 – Output characteristic of a FeTFET using a 10 nm thick Si:HfO₂ film as the gate stack with devices using 10 nm of Si:HfO₂ and 1 nm of SiO₂ and Si₃N₄ as the buffer layer. The device without buffer layer provides 1.7 V memory window, 1 nm of Si₃N₄ reduces the MW down to 1.2 V, and 1 nm of SiO₂ provides 1.0 V memory window. The presented results are derived by employing the proposed model.

proper interface with the substrate. However, the voltage drop over the buffer layer reduces the memory window.

To study the effect of the buffer layer on the MW, we utilized 10 nm of Si:HfO₂ as the ferroelectric dielectric and 1 nm of SiO₂ and Si₃N₄ as the buffer layer. Results are compared with a device using only 10 nm of Si:HfO₂ as the gate stack in Figure 5.6. Employing 1 nm of SiO₂ drops the MW to 1.0 V while the use of 1 nm of Si₃N₄ reduces the memory window to 1.2 V as the voltage drop over the buffer layer reduces the electric field inside the ferroelectric. The voltage drop over the buffer layer is considerable as SiO₂ and Si₃N₄ have lower relative permittivity comparing the ferroelectric layer. Reducing ferroelectric voltage results in the formation of minor polarization hysteresis loops instead of the saturation polarization loop that reduces the memory window significantly [175, 173]. Moreover, the presence of the buffer layer reduces the silicon surface potential results in low energy carriers and insufficient tunneling through the tunneling barrier, leading to the deformation of the transfer characteristic and reduced saturation current.

The negative influence of the buffer layer can be reduced in case of high-k materials, lowering the voltage drop across this layer, but it can never be zero. In this subsection, we emphasize another advantage of Si:HfO₂, which is the proper interface with silicon. Therefore, the doped HfO₂ thin film can be deposited directly on the silicon, and no buffer layer is required. However, it should be noted that a thin layer of HfSiO forms at the interface during the deposition and annealing of the Si:HfO₂, which is called the

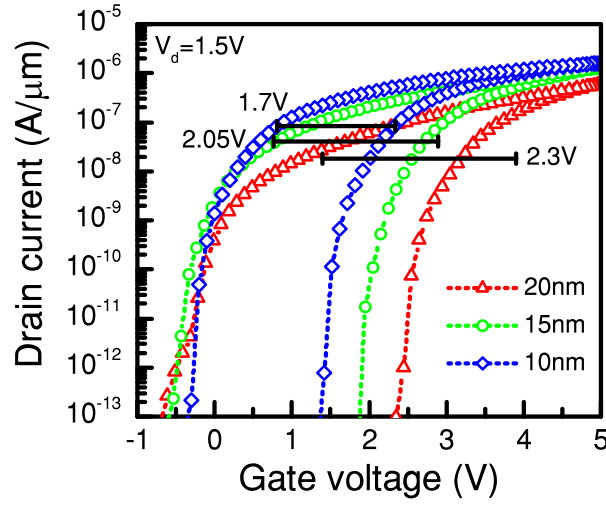


Figure 5.7 – I_d - V_g curves of the FeTFETs using different thicknesses of Si:HfO₂. Results are obtained using the developed model of this study.

dead layer. The dead layer performs no ferroelectricity, and it behaves like a buffer layer and reduces the memory window [60, 187]. As the dead layer is a related issue for all ferroelectric materials, we have neglected this effect in our simulations.

Besides reducing the memory window, the presence of the buffer layer also increases the subthreshold slope, affecting the response time and power dissipation.

5.2.3 Ferroelectric thickness

Another important parameter that greatly affects the memory window is the ferroelectric thickness. The ferroelectric thickness strongly affects the MW as it specifies the total number of the dipoles ($MW \sim 2E_c \times d$ where E_c and d are the ferroelectric coercive field and thickness relatively [192]). Furthermore, the ferroelectric coercive field might change by varying the film thickness, especially in the case of the doped HfO₂. Increasing the film thickness in Si:HfO₂ reduces the coercive field. The ferroelectric properties of the Si:HfO₂ regarding the film thickness is depicted in Table 5.2.

Table 5.2 – Ferroelectric properties of Si:HfO₂ regarding the film thickness [60, 187].

Thickness	P_r ($\frac{\mu C}{cm^2}$)	P_s ($\frac{\mu C}{cm^2}$)	E_c ($\frac{MV}{cm}$)	ϵ_r
20nm	5.5	5.75	1.00	28.5
15nm	7.25	7.62	1.05	30.25
10nm	9	9.5	1.1	32

The transfer characteristic of the FeTFET using different thicknesses of Si:HfO₂ is

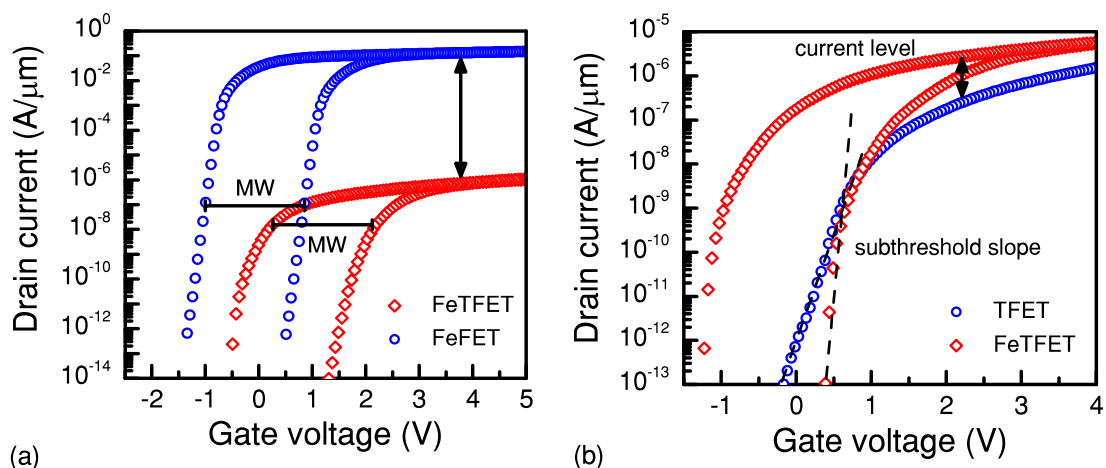


Figure 5.8 – (a) Transfer characteristic of a 28 nm gate length FeFET vs. FeTFET, using 10 nm of Si:HfO₂ as the ferroelectric. The drain voltage is considered 1 V for all simulations, which is the supply voltage of the 28 nm ITRS node. Results confirm that the FeTFET provides the same memory window as the FeFET with lower power consumption. (b) The quick injection of charges to the internal node improves the subthreshold slope of the FeTFET comparing the conventional TFET. Results are obtained using Sentaurus TCAD commercial simulator.

illustrated in Figure 5.7. The coercive field slightly reduces by increasing the Si:HfO₂ thickness. However, simulation results confirm that the effect of the film thickness is dominant and the memory window enhances significantly by increasing the thickness. Up to 2.7 V memory window is obtained in a device with a 20 nm layer thick Si:HfO₂.

5.3 Highly scaled FeTFET

Unique properties of the ferroelectric Si:HfO₂ such as relatively low dielectric constant, CMOS compatibility, good interface with the silicon [169], and relatively high remanent polarization even in a 5 nm thick, thin film [174] make it a promising candidate for the fabrication of future nonvolatile memories [187, 60].

The unique properties of Si:HfO₂ allows us to fabricate ferroelectric MOSFETs down to the nanoscale. However, on the nanometer scale, the high power consumption per area of the chip becomes a challenging issue. To eliminate the power dissipation problem we need to design energy efficient devices with an extremely low *off*-current. Tunnel FETs have been proposed as energy efficient devices due to their low *off*-current and steep *off* to *on* transition. The FeTFET can be a decent candidate for future nonvolatile memories due to its ability to provide a sufficient memory window with low power dissipation. As we did not consider short channel effects in our model, the results of the model may not be reliable for a nanometer scale device. Therefore, Sentaurus TCAD commercial simulator is employed for the design and simulation of a 28 nm gate length FeTFET.

In Figure 5.8-a, the transfer characteristic of a 28 nm gate length single gate ferroelectric MOSFET is compared to a FeTFET with the same physical dimensions. 10 nm of Si:HfO₂ is used as the gate ferroelectric. Regarding the presented results in Figure 5.8-a, FeTFET provides the same memory window as FeFET with a much lower *off*-current (static power) [192]. However, the TFET low output current is the main drawback of this device as it may not be sufficient to drive the circuit capacitors. It should be noted that besides the ability of ferroelectrics for data storage, a ferroelectric transistor can also benefit from the impact of the polarization switching that injects a relatively large amount of charges into the internal gate node quickly that enhances the output current and SS of the device. In Figure 5.8-b, the I_d - V_g characteristic of a 28 nm FeTFET with 10 nm of Si:HfO₂ is compared with a 28 nm gate length conventional TFET with the same equivalent oxide thickness. As a result of the ferroelectric polarization switching, the subthreshold slope of the device is decreased, and the drain current is increased significantly. Simulation results suggest that the FeTFET meets our expectation for a low power random access nonvolatile memory providing sufficient memory window.

5.4 Summary

The analytical modeling of ferroelectric TFETs is developed and validated using Sentaurus TCAD commercial simulator. The model is obtained by solving Maxwell's first equation in conjunction with the Poisson equation. Based on the proposed model, the memory window of a FeTFET memory is extensively investigated as a key parameter of nonvolatile memories. The recently discovered ferroelectric, Si:HfO₂, is integrated into the TFET gate stack in order to highlight the advantages of this ferroelectric thin film. Theoretical results represent that Si:HfO₂ stands as a promising candidate for the future of ferroelectric nonvolatile memories. Besides the outstanding properties of the Si:HfO₂ for the device fabrication, a large memory window is obtained as the result of the integration of this ferroelectric thin film with TFETs. Finally, a 28 nm gate length FeTFET is designed and simulated providing the same MW as a 28 nm FeFET, consuming less power dissipation. The presented results confirm that a FeTFET, using Si:HfO₂ as the gate ferroelectric, can be utilized as the ultra-low power nonvolatile memory applications. Moreover, the polarization switching effect of ferroelectric TFETs can offer a solution for the low output current of tunneling devices, which is one of the main drawbacks of this type of transistors.

6 Conclusions and Perspectives

Abstract:

This short chapter summarizes the main conclusions concerning the most important contributions of this work. It highlights and validates the potential of ferroelectric field-effect transistors for both steep slope and memory applications and the achieved progress during this Ph.D. work. In the end, the open challenges will be discussed and some less conventional perspectives for the future will be discussed.

6.1 Conclusions

The presented thesis mainly focused on the experimental validation of negative capacitance in ferroelectric transistors in order to provide steep slope switches. A matching condition is proposed between the ferroelectric's negative capacitance and the reference transistor to maximize the performance-boosting of NC as well as reducing their hysteretic behavior, as the main challenge of ferroelectric transistors. The proposed condition is then validated experimentally on state-of-the-art MOSFETs and Tunnel FETs. Various ferroelectric materials, from high quality single crystalline perovskite to CMOS compatible doped high-k ferroelectrics, are employed as the negative capacitance booster. All the presented NC transistors were carefully characterized and the presence of the negative capacitance effect has been confirmed by extracting the polarization characteristic of the ferroelectric capacitor during the device operation.

The main technical and scientific achievements can be summarized as follows:

6.1.1 Negative capacitance matching condition

The condition for negative capacitance to occur has been previously proposed and experimentally validated. However, another condition was required in order to optimize the hysteretic behavior of ferroelectric transistors, as the main challenge of negative capacitance transistors, and boosting performance due to the NC. As a general rule, an NC-FET with a large hysteresis shows a significant performance-boosting and a sharp switching. The performance of an NC-FET reduces by reducing the hysteresis. Here, we have proposed and both theoretically and experimentally validated that the following conditions are required to provide a sufficient amplification together with a non-hysteretic behavior in an NC-FET: (i) the absolute value of the ferroelectric negative capacitance ($|C_{FE}|$) and the intrinsic gate capacitance of the reference transistor (C_{int}) need to be relatively close while (ii) the total capacitance of the structure should remain positive in the whole range of the operation.

6.1.2 Experimental demonstration of hysteretic and non-hysteretic NC-FETs

The hysteretic and non-hysteretic behavior of negative capacitance MOSFETs is experimentally investigated in this thesis. It has been demonstrated that a significant reduction of the subthreshold swing can be obtained by the impact of the NC on field-effect transistors. Commercial MOSFETs fabricated in 28 nm CMOS technology node and also fully depleted thin body SOI MOSFETs are employed as the reference transistors and low leakage polycrystalline PZT is considered as the ferroelectric. Sub-thermionic swings down to 5 mV/decade are achieved in hysteretic NC-FETs. By totally fulfilling the proposed matching condition, a totally hysteresis-free NC-FET with a subthreshold

swing down to 20 mV/decade is demonstrated.

6.1.3 Experimental demonstration of hysteretic and non-hysteretic NC-TFETs

For the first time, experimental negative capacitance TFETs in hysteretic and also near hysteresis-free modes of operations have been demonstrated in this Ph.D. work. Novel InAs/InGaAsSb/GaSb nanowire TFETs and InGaAs planar TFETs with sub-thermionic subthreshold slopes are employed as the reference transistors. Poly and single crystalline PZT and the CMOS compatible ferroelectric, silicon doped HfO₂, are utilized as the ferroelectric capacitor. By combining the band-to-band tunneling of TFETs with the negative capacitance of ferroelectrics, energy efficient steep slope switches are realized. It has been evidenced that the negative capacitance can be efficiently utilized to significantly enhance both analog and digital figures of merit of TFETs.

6.1.4 Comparison between silicon doped HfO₂ and Pb(Zr,Ti)O₃

The performance of negative capacitance devices using PZT as the NC booster is compared with NC-FETs using Si:HfO₂, as the recently proposed CMOS compatible ferroelectric. It is evidenced that although Si:HfO₂ enables the CMOS compatible fabrication of FeFETs, its properties are not adequate to provide an effective negative capacitance effect. Si:HfO₂ has a lower remanent polarization and a much higher leakage comparing conventional ferroelectrics that degrade the impact of the NC effect.

6.1.5 Ferroelectric TFET as low power nonvolatile memory

It is proposed that ferroelectric TFETs can be employed as low power non-volatile memories with improved performance and a higher *on*-current. The analytical modeling of ferroelectric TFETs is developed and validated by Sentaurus TCAD commercial simulator. S:HfO₂ is integrated into the gate stack of the TFET in order to highlight the advantages of this ferroelectric thin film. Theoretical results suggest that a FeTFET using Si:HfO₂ as the gate ferroelectric stands as a promising candidate for enabling the CMOS compatible manufacturing of energy efficient 1T memory devices even in aggressively scaled dimensions.

6.2 Perspectives

The presented work can be improved in future researches at different levels: modeling, fabrication, and exploitation of new applications.

6.2.1 Fabrication challenges

A fully CMOS compatible fabrication process should be developed. In this regard, a CMOS compatible ferroelectric with adequate properties is highly needed. Si:HfO₂ has an almost CMOS compatible process, however, it does not ensure a sufficient negative capacitance effect mainly due to its high leakage current.

6.2.2 Modeling of Negative Capacitance effect

A full comprehensive model that can actually anticipate the operation of negative capacitance transistors is missing. There is some theoretical model developed by considering so many simplification and assumptions that can never truly anticipate an NC-FET behavior. Therefore, a working negative capacitance FET cannot be actually designed and it is always a huge difference theoretical expectation and experimental results. This was the main reason that in this thesis an external connection between the ferroelectric capacitor and the reference transistor is considered so that the capacitor and/or reference transistor can be changed in order to obtain the best possible negative capacitance effect.

6.2.3 Frequency measurements

The small signal regime should be studied as a steep slope switch is not meant to work at the quasi-static regime. It is important to investigate the frequency response of negative capacitance transistors due to the fact that ferroelectric materials show a different electric response in small signal regime compared to quasi-static measurements.

6.2.4 Negative Capacitance FET as 1T memory cell

It is well demonstrated in this work that the hysteretic behavior of negative capacitance transistors can be tuned. This would be beneficial for the design of ferroelectric 1T memory cells with the ability to define the memory window. Additionally, the proposed memory cell can benefit from the NC of ferroelectric in a well-designed structure, showing improved performance and lower leakage current.

A Appendix: Silicon-doped HfO₂ Runcard

Projet : Ferroelectric silicon-doped HfO₂

Operator : Ali Saeidi

Created : 01.06.2016

Substrates : silicon test wafer <100>, 100mm, 525um, single side, Prime, p type, 0.1-0.5 Ohmcm

Step N°	Description	Equipement	Program / Parameters	Target	Actual
0	WAFER PREPARATION				
0.1	Stock out				
0.2	Check				
1	CLEANING				
1.1	RCA1 clean	Z3/WB_PreOx_Clean	H2O:NH4OH:H2O2 (5:1:1)	15min 75°C	
2	SPUTTERING				
2.1	TiN Deposition	Alliance-Concept DP650	TiN	100 nm	
3	ATOMIC LAYER DEPOSITION				
3.1	Si:HfO2 deposition	BENEQ TFS200	SiO2+HfO2	8-30 nm	
4	SPUTTERING				
4.1	TiN Deposition	Alliance-Concept DP650	TiN	100 nm	
5	ANNEALING				
5.1	Annealing	Jipelec jetfirst 200	20 seconds @ 800 C		
6	PHOTOLITHOGRAPHY				
6.1	HMDS	Z1/YES3	Prog. 0		
6.2	AZ 1512 coating	Z6/ EVG150	AZ_1512_1um1	1.1 um	
6.3	PR bake	Z6/ EVG150	AZ_1512_1um1		
6.4	PR expose	Z1/MA150	First mask, HC, 10.0 mW/cm2		
6.5	PR develop	Z6/ EVG150	Dev_AZ1512_upto_1um3		
6.6	PR postbake	Z6/ EVG150	Dev_AZ1512_upto_1um3		
6.7	Inspection	Z6/uScope	Resolution and alignment		
6.8	Descum	Z2/Oxford	Descum O2, 5min		
7	SPUTTERING				
7.1	Pt Deposition	Alliance-Concept DP650	Pt	50 nm	
8	LIFT-OFF				
8.1	Remover 1165	Z1/ Plade_Solvent	PT 1		
8.2	Remover 1165 + US	Z1/ Plade_Solvent	Bac US		
8.3	IPA	Z1/ Plade_Solvent	PT 2		
8.4	Fast Fill Rinse	Z1/ Plade_Solvent	DI Rinse		
8.5	Trickle tank	Z1/ Plade_Solvent	DI Rinse		
8.6	Spin Rinser Dryer	Z1/ Semitool SRD	Prog. 1		
8.7	Optical Inspection	Z1/ uScope			
9	TiN WET-ETCHING				
9.1	RCA1	Z14/Base wet bench	2 min	10 nm	
10	CLEANING				
10.1	Plasma O2 clean	Z2/Oxford	O2 , 20 min		
10.2	Remover 1165	Z2/WB_PR_Strip	Bath 1 : main remover	15min, 70°C	
10.3	Remover 1165	Z2/WB_PR_Strip	Bain 2 : clean remover	15min, 70°C	
10.4	Fast fill rinse	Z2/WB_PR_Strip	DI Rinse		
10.5	Trickle tank	Z2/WB_PR_Strip	DI Rinse		
10.6	Spin Rinser Dryer	Z2/Semitool SRD	prog 1		
10.7	Plasma O2 clean	Z2/Oxford	O2 , 20 min		
10.8	Inspection	Z6/uScope			

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Ali Saeidi Ph.D. student

summary

As an energetic, enthusiastic and hardworking professional I love to challenge myself with complex questions in design, fabrication, modelling, and characterization of semiconductor devices. In the last six years as a researcher I have proven my ability for finding sustain solutions, thinking out of the box and working on parallel tasks. I am versatile, sociable, and able to work in a team.

experience

August. 2014 - present

Ph.D. student / Research engineer
NANOLAB | EPFL, Switzerland

Exploration of Negative Capacitance devices and technologies: *exploration of novel devices and technologies based on the concept of ferroelectric's negative capacitance that serve as alternatives for low-power low-voltage digital circuits and memories.*

Detailed achievements

- Modeling and simulation of low-power non-volatile memory tunnel FETs.
- Modeling and simulation of state-of-the-art negative capacitance FETs.
- Derive the theoretical condition for negative capacitance to occur in ferroelectric transistors.
- Fabrication and characterization of hysteretic and non-hysteretic negative capacitance Tunnel FETs.
- Fabrication and characterization of hysteretic and non-hysteretic negative capacitance MOSFETs.
- Cryogenic measurement of negative capacitance effect in ferroelectric Tunnel FETs.
- Developing a repeatable process for fabrication of silicon-doped HfO₂ as a CMOS compatible ferroelectric using Atomic Layer Deposition technique.
- Modeling of HEMT power devices.
- Modeling of junction-less field effect transistors.

March 2012 – August 2014

Master student / Researcher
Nanoelectronic Lab | University of Tehran

Silicon Nanowire and Nanotube based biosensors for cancer detection: *Investigation of CVD growth silicon nanowires and silicon nanotubes and their applications for biosensors with the focus of cancer cell detection.*

Detailed achievements

- Developing the process for the CVD growth of silicon nanowires and silicon nanotubes.
- Fabrication and modeling of high sensitivity humidity sensors based on doped silicon nanowires.
- Cell membrane electrical charge investigations by silicon nanowires incorporated with field effect transistor suitable in cancer research.
- Propose and verify a single-cell correlative Nanoelectro-mechanosensing approach to detect cancerous transformation; monitoring the function of F-Actin microfilament in the modulation of the Ion channel activity.
-

Special achievements

Patent: "Electromechanical approach for cancer detection," **US patent** App. 15/238,795,2016.

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Skills

Micro/Nano fabrication
Cleanroom process
Device measurements, IC-CAP
Cryogenic
Characterization/Parameter extraction
Device design and TCAD
IC design (Cadence, Hspice)
Sensor characterizations
Biosensors
Physics and computational methods

Languages

Persian	Native
English	Business fluent
French	Basic

education**Ecole Polytechnique Fédérale de Lausanne**

August 2014 – present

Ph.D. Microelectronics

Focus: Microsystems and Micro Electronics

University of Tehran

August 2012 – August 2014

M.Sc. Electronics and Semiconductor DevicesWeighted grade avg. **19.65/20****detailed technical skills**

- Electronic devices development specialist: design, fabrication and testing.
- 6+ years experience in CMOS and MEMS microfabrication
- Cleanroom fabrication: Photo and e-beam lithography, all physical and chemical deposition techniques, wet and dry etching processes, and all required expertise for fabrication of complex semiconductor devices.
- Extensive experience in CMOS process.
- Device measurement, characterization, and parameter extraction of complex semiconductor devices (IC-CAP).
- Device design and TCAD: Sentaurus device simulation, Silvaco, L-edit, Comsol
- Extensive skills in mathematics, physics, and computational methods
- IC design: Spice

awards and honors

- Electron Device Society **George E. Smith Award, 2017.**
- Ranked 1st among electrical engineering graduate students, 2014.
- Directly admitted to the Master program as an excellent student award, 2012.
- Being an exceptional talent student in University of Tehran for 6 years (B.Sc. and M.Sc.)
- Ranked 351st among more than 600,000 participants in the national wide university entrance exam (2008).

list of publicationsJournal papers

- **Saeidi, Ali**, et al. *Nature Electronics* (2018): *under revision*.
- **Saeidi, Ali**, et al. *Nature Scientific Reports* (2018): *under revision*.
- **Saeidi, Ali**, et al. *Nanotechnology* 29.9 (2018): 095202.
- Jazaeri, Farzan, Makris, Nikolaos, **Saeidi, Ali**, Bucher, Matthias, and Sallese, Jean-Michel. *IEEE Transactions on Electron Devices* (2018): *under revision, accepted*.
- **Saeidi, Ali**, et al. *IEEE Electron Device Letters* 38.10 (2017): 1485-1488.
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