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Multiport Energy Gateway

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Abstract: Medium-voltage-direct-current collection and distribution grids are being considered for emerging applications, and require enabling power electronic technologies. Medium-voltage high power DC–DC converters are one of the solutions that will play an important role in future energy systems. This study presents a novel bidirectional multiport power electronic converter, interfacing medium-voltage and low-voltage distribution grids while integrating distributed energy storage elements, such as batteries and super-capacitors. The multiport energy gateway concept is based on a modular input-series output-parallel topology includes medium frequency transformer for the galvanic isolation, and combines open-loop and closed-loop operated converter stages. Comprehensive converter design aspects and operating principles are presented and discussed considering representative cases of studies. The validity of the approaches is proved by simulation and experimental results obtained on a small scale prototype.

1 Introduction

Nowadays, energy supply has an ever increasing dependence on renewable energy resources, mostly due to the growing number of new solar, photo-voltaic (PV) and wind power plants. The volatility of renewable resources, e.g. due to their dependence on weather conditions and issues related to their geographical distribution, leads to new power system stability challenges. Integration of controllable energy storage (ES) elements has been found as a good countermeasure to mitigate weak spots associated to green resources [1].

DC microgrid is a natural solution to integrate ES in a higher level distribution AC/DC grid. For typical power levels of ES resources, DC microgrids are a good alternative to AC microgrids, in terms of size, cost, efficiency, simplicity and stability [2]. Undoubtedly, recent advances in the field of semiconductors have emerged as a key driver for very high efficiency and high power density conversion technologies: in the past, step-up or step-down conversion was not feasible because of the absence of suitable devices; nowadays, the current and voltage levels of power switches allow to reach high power, high-frequency DC–DC conversion, which permits to substitute bulky low-frequency transformers by medium frequency transformers (MFTs) [3].

Medium-voltage-direct-current (MVDC) technologies have raised as a natural solution to interface energy resources in the power range of an MW to tens of MW. However, despite there are mature low-voltage-DC (LVDC) and high-voltage-DC (HVDC) solutions in the market, MVDC grids are still not deployed massively, mostly due to the absence of power electronics conversion and protection technologies. Although they are not yet numerous and standardised nowadays, commercial MVDC, offerings start to appear in the portfolio of key industry players [4].

The MVDC electrical distribution has been considered for future all-electric ships [5]. Present MVAC on-board distribution allows for the spatial decoupling of the generation and propulsion which offers great flexibility in ship design. The MVDC will enable further frequency decoupling of the generation and distribution, which permits for AC generators to run at optimal speed, improving the overall fuel efficiency [6]. Moreover, MVDC systems simplify integration of ES [7]. With bidirectional DC–DC converters it is possible to use the stored energy for peak shaving or provide support for the black start conditions (Fig. 1*a*). While the LVDC electrical distribution has been already successfully demonstrated [8], MVDC systems still lack various conversion [9] and protection components for practical realisation [10].

Another application in which AC and DC distribution systems are being compared are data-centres, already well in excess of several MW power rating [11]. The power supply of data-centres is very critical, and ES elements can greatly increase the reliability of such systems. Nowadays the power to the chip is delivered through the multiple conversions in order to reach low operating voltage levels of the processors. In perspective, DC would allow for a reduction of the number of conversion stages and enable simpler integration of hybrid storage elements (Fig. 1*b*). MVDC distribution goes hand in hand with the promising concept of DC microgrids [12, 13] and the geographical clustering of energy resources and loads. The fact that grid nodes can produce and consume power depending on the time of the day forces the development of bidirectional interfaces (Fig. 1*d*).

The volatile PV production is subject to low-frequency variations (hours), due to the climate and average daily irradiation levels, which can be predicted fairly well [14] and mitigated with the help of bulk storage [15]. ES is also employed to mitigate higher frequency fluctuation effects (seconds to tens of minutes) due to partial shading which can affect grid stability. Since MVDC networks have some potential as a collector grid [16] and intermediate stage between LV PV generation and transmission grid, it is possible to integrate distributed hybrid ES at every LV–MV collection point (Fig. 1*c*).

Considering large scale off-shore wind farms, comparative analyses (AC versus DC) have been presented in [17–20], that highlight the techno-economic trade-offs between the initial capital investment, the cost of lost energy due to losses within the system, unavailability due to scheduled maintenance or wind turbine failure, and other system faults. While a number of advantages have been recognised, a number of challenges still remain (protection, no standardised DC voltage level, no suitable power converters etc.); as a result, there are no large scale MVDC distribution systems in commercial use at this point in time. Nevertheless, the volatility of wind energy generation, either at LV or MV, would benefit from an integrated energy buffer (Fig. 1*c*).

The few examples depicted in Fig. 1 illustrate the potential advantages resulting from the integration of the ES elements in the MV to LV (and vice-versa) conversion chain. In addition, the idea of increasing the efficiency and reliability of the charge–discharge cycle by reducing the number of conversion steps motivates the development of a fully bidirectional multiport power electronics

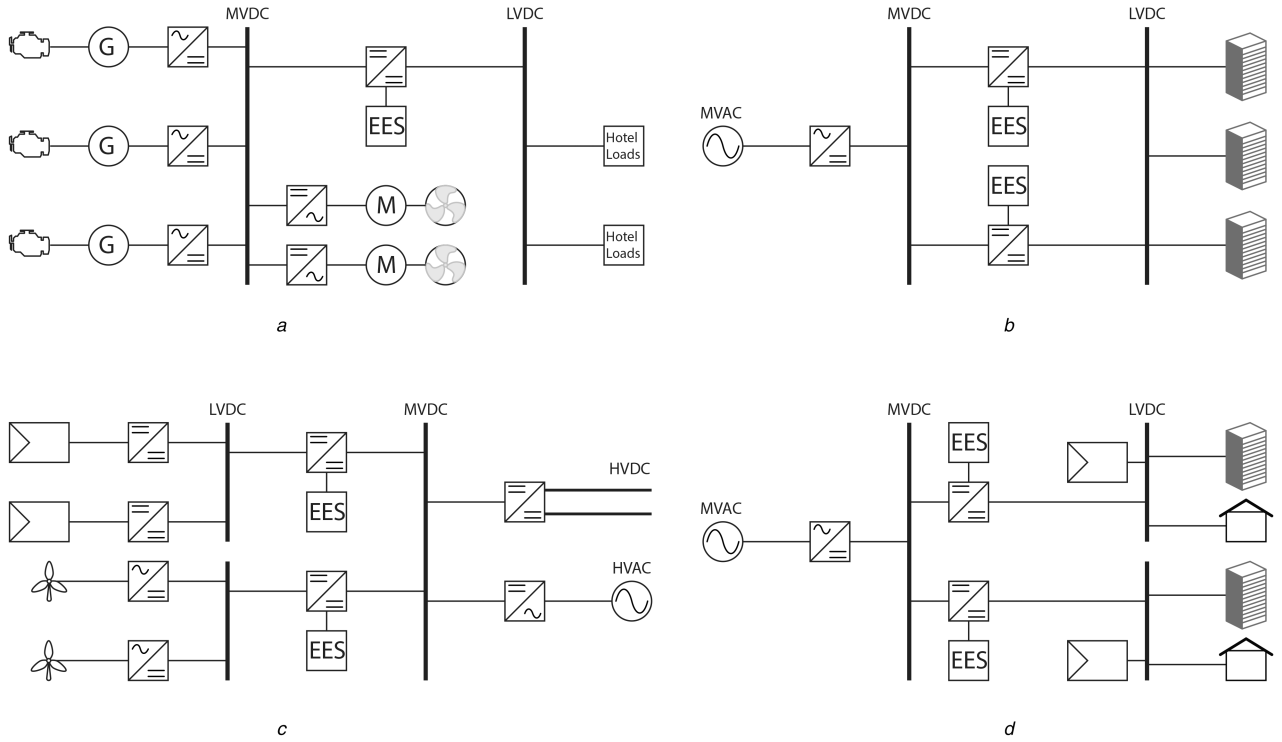

Fig. 1 *Future applications of MVDC grids*
(a) Power distribution networks for marine, ***(b)*** Distribution for data-centres, ***(c)*** Collectors for PV and wind generation, ***(d)*** MVDC distribution for bidirectional LVDC microgrids

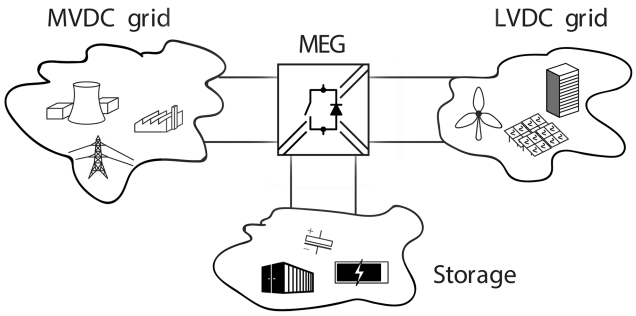

Fig. 2 *MEG provides galvanic isolation between future MVDC and LVDC grids, while integrating distributed ES, e.g. batteries and/or super-capacitors*

interface. Solutions based on the emerging concept of solid-state-transformer [21], using medium- or high-frequency transformers and thus enabling an isolated but very compact DC–DC conversion, seem adequate for bidirectional conversion for medium-voltage ratings and high power density.

Regarding the multiport topologies, converters based on multi-winding transformers offer the freedom to set the voltage adaptation ratio over a wide range, allowing grids of different voltages to be interfaced. In [22], the authors presented a topology derived from the reputed dual-active-bridge topology and supplemented by two additional ports. On the same principle, [23, 24] show triple-active-bridge structures in which the power flow is controlled by phase shift combined with the duty cycle. Multiple-active-bridge may be used in a multilevel structure such as presented in [25]. The voltage balancing is effective in a unidirectional way, but when it comes to the bi-directional converter, the control becomes very complex. Additionally, the limited operating range of these latter converters, in terms of soft switching has resulted in considerations towards resonant converters.

Relevant works on structures based on LLC converter extended to a multiport version are reported [26]. The operation of a three-winding MFT-based resonant converter with a single source port and two load ports is presented in [27] and demonstrates good load and cross-regulation. The operation with two synchronous source ports and one load port are experimented by the authors of [28]. The resonant tank can be either located on one port (for unidirectional flow) or split between all the ports in order to take advantage of bidirectionality.

MV voltage ranges can be achieved by using multi-level structures, either input-series-output-parallel (ISOP) [29] or input-parallel-output-series [30], to reduce voltage stresses on semiconductors. These structures have many advantages, as shown in [31]. The overall reliability of the system is enhanced by the redundancy of the key elements and the reduction of electrical and thermal stresses shared among the submodules.

Among these solutions, the power-electronics-traction-transformer (PETT) is a technology already tested at industry level [32, 33]. The PETT structure includes different conversion stages including an active-front-end which serves to regulate the voltage, an LLC resonant stage which allows voltage adaptation as well as galvanic isolation and a load side converter that controls the power. Even if this topology has been developed for AC traction, the structure can be adapted for DC–DC conversion with minor modification and the concept can be extended to a multiport converter, as proved in this work.

This paper presents a novel DC–DC–DC converter topology, Fig. 2 referred further as Multiport Energy Gateway (MEG). The converter is based on the combination of multiple identical submodules, each equipped with a three-winding MFT [34, 35]. The input-series side is connected to MVDC grid (MV port), while the output-parallel side is connected to the LVDC grid (LV port). The third port of each of the submodules is used to connect the same or different types of ES elements (ES port), depending on the desired dynamic of response. The tight voltage coupling provided by the LLC structure enables a good load regulation and stability while keeping the control structure simple. This allows the independent operation of each storage element and the use of a mix of batteries and super-capacitors improving the overall energy management [7].

This paper is organised as follows: The topology and its features are presented in Section 2. Section 3 describes the dynamics of the MEG converter and presents a control structure. Experimental and simulation results validating the principles presented are shown in Section 4, while Section 5 provides a summary and a conclusion.

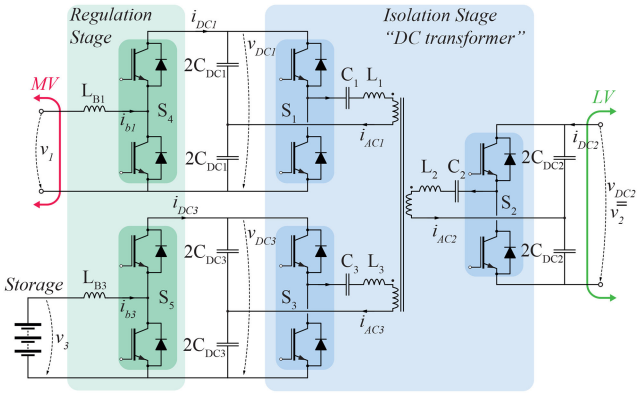

Fig. 3 *MEG submodule. It is a DC–DC–DC converter. Two terminals are dedicated to DC-grids and third one integrate storage elements. The backbone for a high efficient power conversion is the SRC based three-port DC transformer*

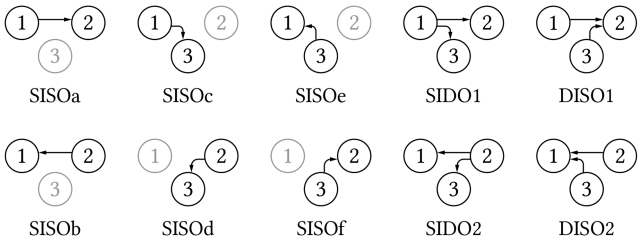

Fig. 4 *Modes of operation of the MEG converter*

Table 1 Operating modes

Mode	S_1	S_2	S_3	S_4	S_5
SISOa	active	passive	passive	boost	off
SISOb	passive	active	passive	buck	off
SISOc	active	passive	passive	boost	buck
SISOd	passive	active	passive	off	buck
SISOe	passive	passive	active	buck	boost
SISOf	passive	passive	active	off	boost
SIDO1	active	passive	passive	boost	buck
SIDO2	passive	active	passive	buck	buck
DISO1	active	passive	active	boost	boost
DISO2	passive	active	active	buck	boost

2 MEG converter topology

The MEG is made up of a number N_s of identical submodules, as depicted in Fig. 3. The core of each sub-module is a DC-transformer stage, which comprises a three-winding MFT combined with a resonant tank and three switching cells (S_1, S_2 and S_3). In order to benefit from full bi-directionality, the resonant tank is split among the three ports. The resonant frequency is the same for all active ports, which also implies a fixed switching frequency for all the cells (when switching signals are enabled) [27, 35]. It should be noted that the DC-transformer stage is only responsible for galvanic isolation and voltage adaptation; frequency control, duty-cycle control or phase-shift control are not considered at this stage [32, 36]. Since there are no closed-loop control features at the DC-transformer (or resonant stage in the following), each sub-module comprises two additional switching cells (S_4 and S_5) behaving as buck or boost converter, depending on the power flow direction. Both are controllable with the duty-cycle in order to regulate the output voltage and the power flow. This stage is further referenced as a regulation stage.

One key point of the MEG concept is its flexibility and ability to implement different application-level strategies. Based on the power flow direction, eight different modes of operation can be identified, c.f. Fig. 4, which are summarised in Table 1. Even though all the cases of power flow between the three ports are technically possible, the case where the storage is charged from the two grids and the case where the storage is discharged to the two grids are not taken in account, since they are of little practical relevance. In this sense, the power ratings considered for the ES port may be reduced compared to ratings of the main ports (MV port and LV port). For the sake of simplicity, the MV, LV and ES ports are referenced, at submodule level, as ports 1, 2 and 3, respectively.

2.1 Resonant stage

The resonant stage comprises a three-winding MFT with turn ratios $(n_1:n_2:n_3)$, which are set according to the nominal output voltages. The leakage inductance L_{σ_i} of each MFT port $i = 1, 2, 3$, and eventually additional external inductor to match the required value L_i, is combined to a capacitor C_i in order to make a resonant tank. The three resonant tanks have the same resonant frequency f_{res} which implies

$$2\pi f_{\text{res}} = \omega_{\text{res}} = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} = \frac{1}{\sqrt{L_3 C_3}} \tag{1}$$

This stage is driven by two-levels (bipolar) voltages so, in order to decrease the complexity and the number of semiconductors, half-bridges structures have been adopted for S_1, S_2 and S_3. The DC bus capacitance $C_{\text{DC}_{1,2,3}}$ is much bigger than the resonant capacitors, so the voltages generated by the active ports are considered as square-wave voltage sources. As mentioned earlier, the resonant stage is working in open loop, in a so-called DC-transformer operation. The switches of half-bridges $S_{1,2,3}$ are activated as a function of the

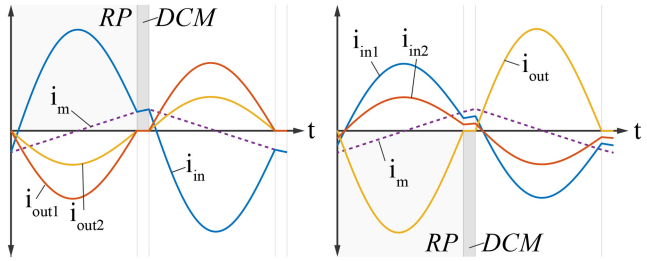

Fig. 5 *Typical resonant current waveforms in SIDO and DISO mode. In both modes, two main sub-intervals may be identified in the half switching-period. During the resonant pulse (RP), the input port(s) is/are supporting the output port(s) as well as the magnetising current. During the DCM, the passive rectifier on the load port(s) is not conducting and the magnetising current is provided by the input port(s). It is shared between the two active ports in DISO mode*

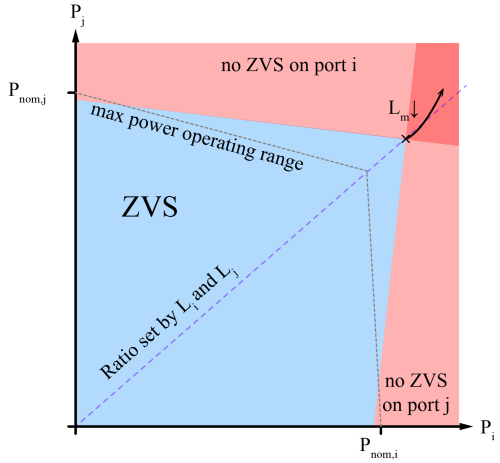

Fig. 6 *Operation range defined by P_i and P_j, and the ZVS operation area corresponding to a specific design (L_m, L_1, L_2, L_3). Reducing L_m increase the magnetising current and the ZVS area. However, increased magnetising current implies also increased conduction losses (increased RMS currents) and turn-off losses. This leaves the sizing of L_m, as well as the choice of the ratio L_i/L_j in order to fit at best the ZVS area with the maximal power operation region, subjects to further optimisation*

power flow direction: when a port is feeding power to one or both the other ports, it is actively switched at a fixed frequency f_{sw} and with a constant duty cycle of 50% [27, 32, 33, 35]. When a port is receiving power (load port) its semiconductor is not actively switched, and their freewheeling diodes are used as passive rectifiers. In order to benefit from soft switching, i.e. zero voltage switching (ZVS) on the primary side semiconductors [active insulated-gate bipolar transistor (IGBT)] and zero current switching (ZCS) on the secondary side (load port diode rectifier), the resonant stage is operated slightly below resonant frequency [35]. In this way, the circuit operates in discontinuous-conduction-mode (DCM), with representative waveforms in the rated operation being as depicted in Fig. 5. Two different main modes are considered: the single-input-dual-output (SIDO) mode when one port is actively switched and the other are rectifiers and the dual-input-single-output (DISO) mode when two ports are active and the third is a rectifier.

In SIDO mode, the two secondaries can be considered as in parallel. The circuit can be analysed using single-input-single-output LLC converter equivalents; equivalent resonant tanks are evaluated taking into account the turn ratios and the magnetising inductance and using T to Γ transformation introduced in [37]. For instance, the equivalent tank seen from the first port is

$$L_{\mathrm{equ}_1} = L_1 + \frac{L_{m_1} L'_2 L'_3}{L_{m_1} L'_2 + L_{m_1} L'_3 + L'_2 L'_3} \tag{2}$$

$$L'_{m_1} = \frac{L_{m_1}^2}{L_{m_1} L'_2 + L_{m_1} L'_3 + L'_2 L'_3} \tag{3}$$

with

$$L'_2 = \frac{n_1^2}{n_2^2} L_2 \text{ and } L'_3 = \frac{n_1^2}{n_3^2} L_3 . \tag{4}$$

The design methods for standard LLC converters, such as $k-Q$ criterion [38, 39], are applied to each of the equivalent circuits. This results for each port, in a set of optimal tank impedances, for which the tank RMS current is the smallest under the maximum load conditions, and a minimal value of the magnetising inductance in order to keep ZVS/ZCS operation under any rated load conditions:

$$L_{\mathrm{opt}_i} = \frac{R_{\mathrm{AC}_i}^2}{\omega_0^2 L_{m_i}} \tag{5}$$

$$L'_{m_i} \leq \frac{V_{\mathrm{DC}_i} T_{\mathrm{sw}}}{4 T_{\mathrm{d}i} I_{\mathrm{DC}_n} \pi} \tag{6}$$

with R_{AC_i} being the AC equivalent load (according to the first harmonic approximation [40]), corresponding to the nominal power P_{nom_i} of each port i, and $T_{\mathrm{d}i}$ the deadtime required by the semiconductors, which implies a minimal turn-off current [41].

In DISO mode, the sharing of the power injected by the two active ports i and j depends on the splitting of the resonant tank, i.e. on the ratio of the tank impedance [42]. In the ideal case where the DC-bus voltage v_{DC_i} equals exactly $(n_i/n_j)v_{\mathrm{DC}_j}$, the magnetising current i_{m} as well as the power p_i and p_j from the two active ports are shared as

$$\frac{p_i}{p_j} = \frac{i_{\mathrm{m}_i}}{(n_j/n_i) i_{\mathrm{m}_j}} = \frac{(n_i^2/n_j^2) L_j}{L_i} \text{ and } i_{\mathrm{m}} = i_{\mathrm{m}_i} + \frac{n_j}{n_i} i_{\mathrm{m}_j} \tag{7}$$

In other words, the ratio of the resonant tank defines the natural power-sharing in DISO mode, which makes it a design parameter to take in consideration according to the rated powers of each port. For instance, the sharing ratios between the ports 1 and 3 are given by

$$g_{13} = \frac{P_{\mathrm{nom}_1}}{P_{\mathrm{nom}_1} + P_{\mathrm{nom}_3}} = \frac{L'_3}{L_1 + L'_3} \tag{8}$$

$$g_{31} = \frac{P_{\mathrm{nom}_3}}{P_{\mathrm{nom}_1} + P_{\mathrm{nom}_3}} = \frac{L_1}{L_1 + L'_3} = 1 - g_{13} . \tag{9}$$

Any differential voltage Δv_{ij} between the two active ports, defined by

$$\Delta v_{ij} = v_{\mathrm{DC}_i} - \frac{n_i}{n_j} v_{\mathrm{DC}_j} \tag{10}$$

introduces a circulating current $i_{\mathrm{circ}_{ij}}$, which can lead to the loss of ZVS either on port i or j (see Fig. 6). This current is responsible for a circulating power from one active port to the other. In this sense, it is possible to deviate from the ratio set by $L_{i,j}$ and vary the part of the total power transmitted to the load from both active ports by acting on their DC-bus voltage v_{DC_i} and v_{DC_j} through the stages S_4 and S_5.

2.2 Regulation stages

In order to be able to control the DC voltages $v_{\mathrm{DC}_{1,2,3}}$, the ports 1 and 3 are equipped with additional regulation stages composed by the switching cells S_4 and S_5, operated at the frequencies f_{s4} and f_{s5}, respectively, and including the filtering inductors L_{b1} and L_{b3}. They

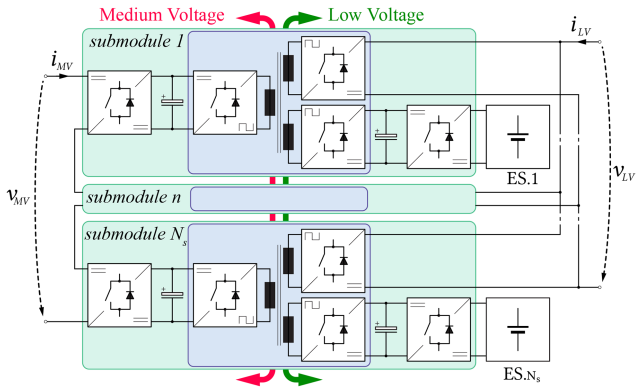

Fig. 7 *MEG: Multi-level ISOP combination of multiport-resonant-converters*

can be operated either as a buck (the upper switch is active and the lower switch is a passive diode) or as a boost converter (only the lower switch is active) depending on the power flow. The switching frequencies f_{s4} and f_{s5} can be different from f_{sw} and are subject to overall converter optimisation. Indeed, f_{s4} and f_{s5} can be adapted to the voltage/current ratings and the selected semiconductor technologies in order to minimise the losses, while f_{sw} is a result of a trade-off between the specifications of the three ports.

2.3 ISOP multilevel converter

To reach MV and high power ratings, a modular ISOP structure can be adopted for the MEG, as depicted in Fig. 7. A number N_s of submodules are connected in series on their port 1 (MV side), and connected in parallel on their port 2 (LV side). The series connection of the N_s buck/boost stages S_4 of the multiple submodules can be operated as a cascaded buck/boost structure with a common duty cycle D_1. Thanks to the ISOP structure and the fixed frequency operation of the inner resonant stage (DC transformer alike behaviour), the converter does not need any active balancing of the DC-bus voltages on the MV side [43]. A practical realisation will inherently produce some deviation of the components from the designed values, but as long as these are within certain margins, the balancing is maintained without active control action. It is also possible to discharge one of the storage elements while charging another one, as long as the power from/to those storage elements is smaller than the main power between the MV and LV sides.

The DC capacitors $C_{DC_{1,2,3}}$ are sized in order to fulfil voltage ripple specifications $\Delta V_{DC_{1,2,3}}$. C_{DC_1} is sized according to (11) where D_{MV} is the duty cycle in steady state and I_{DC_1} is given by P_1/V_{DC_1}. To decrease the voltage ripple on the LV side, the gate signal of the resonant stage of the multiple submodules can be shifted with a phase shift of $2\pi/N_s$[rad] (see Fig. 8*a*). Thanks to the interleaving the apparent frequency is multiplied by N_s and since the DC capacitors C_{DC_2} of the multiple submodules are connected in parallel, they can be reduced by N_s^2 (12). Similarly, C_{DC_3} is sized according to (13)

$$C_{DC_1} \geq \frac{I_{DC_1}(1-D_1)}{f_{swB_1}\Delta V_{DC_1}} \tag{11}$$

$$C_{DC_2} \geq \frac{I_{LV}}{N_s^2 2 f_{sw}\Delta V_{DC_2}} \tag{12}$$

$$C_{DC_3} \geq \frac{I_{DC_3}}{2 f_{sw}\Delta V_{DC_3}} \tag{13}$$

The inductors L_{b1} and L_{b3} are sized in order to fulfil current ripple specifications ΔI_{b_1} and ΔI_{b_3}. As depicted in Fig. 8*b*, interleaving can be introduced between the multiple submodules of the cascaded buck/boost stage of the MV port, in order to reduce the ripple of the current i_{b_1}. In steady state, depending on the duty-cycle, the voltage applied to L_{b1} varies between two levels that are consecutive fractions of the cumulative voltage $N_s \cdot V_{DC_1}$. Thus, L_{b1} may be given by (14). On the port 3, the buck/boost inductor is sized according to (15)

$$L_{b1} = \frac{(D_1 - (N_s - x/N_s))((N_s - x)V_{DC_1}) - V_{MV})}{f_{s4}\Delta I_{b_1}} \tag{14}$$

$$L_{b3} = \frac{V_3(1-D_3)}{f_{s5}\Delta I_{b_3}} \tag{15}$$

3 Modelling and control

This section describes the system modelling and the derivation of controllers for the proposed MEG concept. First, the dynamics of a single submodule is modelled. The simplification of resulting model eases its extension to the complete converter as well as the elaboration of a simple control scheme.

3.1 Modelling a single submodule

The plant modelling of a single-submodule depicted in Fig. 3 is firstly addressed. The currents i_{b1} and i_{b3}, which draw through the inductors L_{b1} and L_{b3}, are controlled inside a high bandwidth innermost loop acting on the duty cycles of S4 and S5 branches. Eventually, one of the DC-bus voltages, i.e. v_{DC_1}, is regulated by i_{b1} being the control action. This operation defines an outer (lower bandwidth) control loop. When ES is actively connected to the third terminal, its outer loop regulation should focus on the state of charge (instead of a tight regulation of v_{DC_3}); an EMS strategy would set the i_{b3} reference. From Table 1, this work explicitly addresses modes of operation SIDO1 and DISO1.

3.1.1 Current and voltage regulation at S4 and S5: Fig. 9 shows the model of both S4 and S5 stages. In principle, the ports 1 and 3 are considered independent from each other, with inductor currents and capacitor voltages being the state variables to be controlled [35]. For the innermost current controllers, duty-cycles D_1 and D_3 define the control actions. For regulation of DC-bus voltages, v_{DC_1} (and v_{DC_3} if apply), the control action is made by setting references to the innermost controllers. For the innermost controllers design, the system can be linearised around DC-bias operation points: V_{DC_1} and V_{DC_3} are assumed to be constant. For the outer controllers, the currents drawing the DC-transformer stage, i.e. i_1, i_3, are perturbations charging/discharging the local capacitor. In practice, both active terminals cannot be considered fully decoupled from each other, since the perturbation currents i_1, i_3 depend on the load connected at terminal 2, the dynamics of the DC-transformer and the operation mode (cf. Table 1). DC-transformer and operation modes are discussed in the next subsections, since a deep modelling of them allows for a more efficient overall MEG high-level controller strategy.

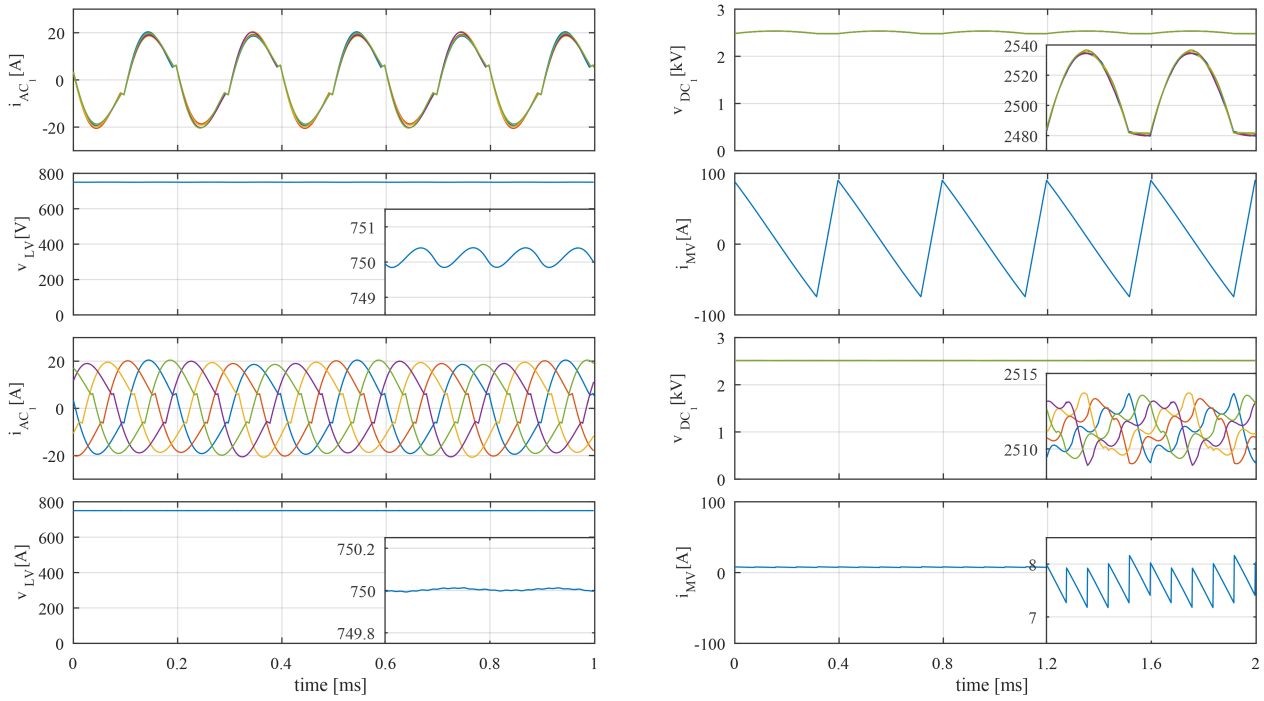

Fig. 8 *Effects of the interleaving for a MEG system with* $N_s = 5$

(a) Resonant currents and the output voltage, without (upper two plots) and with (lower two plots) interleaving of the resonant stages. The ripple on the output voltage is reduced thanks to the phase shift ($2\pi/N_s$) introduced between the submodules, ***(b)*** DC-bus voltages of the port 1 and the current through the MV port, without (upper plots) and with (lower plots) interleaving of the stacked buck/boost stage. The current ripple is clearly reduced while the effect on the DC voltage is also noticeable

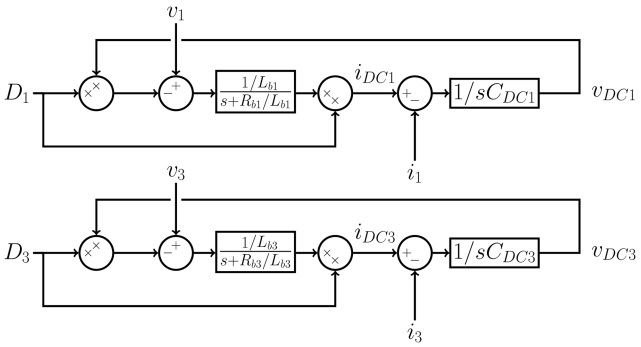

Fig. 9 *System dynamics block diagram for regulation at S4 and S5. Block diagram of the regulation stage. The control input are the duty-cycles* D_1 *and* D_3 *and both ports are independent. The output is the DC-bus voltages* v_{DC_1} *and* v_{E_3}*. The perturbations are the input voltage* v_1*, the storage voltage* v_3 *and the RMS value* i_1*,* i_3 *of the two resonant currents* i_{AC_1}*,* i_{AC_3}

3.1.2 DC transformer modelling: The physical model of the DC-transformer is depicted for DISO1 mode and SIDO1 mode in Figs. 10*a* and *b*, respectively. In both modes, the main voltage-to-current transfer function between the primary and secondary side, is defined as $Y_M(s)$; the differential-voltage-to-circulating-current transfer function is defined as $Y_C(s)$. The sharing ratios defined in (8) and (9) appear as gains. In principle, it is difficult to describe $Y_M(s)$ and evaluate it precisely over the complete frequency range, i.e. to express it as a transfer function [44]. However, regulation is well limited inside a region of the spectrum much smaller than the resonant frequency; i.e. voltage regulation is made in low band-bandwidth closed loops. Therefore, $Y_M(s) \simeq Y_M(0)$ and $Y_C(s) \simeq Y_C(0)$ are reasonable assumptions for the modelling. Calculation of resonant stages dc gains is reported in the literature [42, 45]. By definition, $Y_M(0)$ is a very high gain in the SRC base dc-transformer operated close to resonant frequency (load independent DC gain). The same approximation applies for the circulating current and $Y_C(s) \simeq Y_C(0)$ holds, following similar reason as above. These gains mostly depend on the MFT parameters and system losses [42].

3.1.3 Equivalent model for a single module: By carefully inspecting Fig. 10, the fact that $Y_M(0)$ is a high gain leads to a very important feature: the voltage difference Δv_M, defined by $g_{13}v'_{DC1} + g_{31}v'_{DC3} - v'_{DC2}$ in Fig. 10*a* and $v_{DC_1} - g_{23}v'_{DC2} - g_{32}v'_{DC3}$ in Fig. 10*a*, tends to zero. The same applies to $Y_C(9)$, which forces Δv_{13} and Δv_{23} to zero in steady-state. In other words, the input-voltage-to-output-voltage transfer function of the DC-transformer is well approximated by a unity gain (taking into account the turns ratios of the MFT). From these results, a simplified MEG model can be developed when taking into account that DC-bus capacitors are all connected in parallel (or through very low impedances): the system can be replaced by an equivalent single capacitor which, referred to the primary port, is given by

$$C_{out} \simeq C_{DC_1} + C'_{DC_2} + C'_{DC_3} \simeq C_{DC_1} + \frac{n_2^2}{n_1^2}C_{DC_2} + \frac{n_3^2}{n_1^2}C_{DC_3} \qquad (16)$$

The system can be simplified to an equivalent circuit and transfer function depicted in Fig. 11. In this case, the state variable that can be controlled are the output voltage (common to all DC-buses, taking in account the turn ratio), and the current injected/sinked by

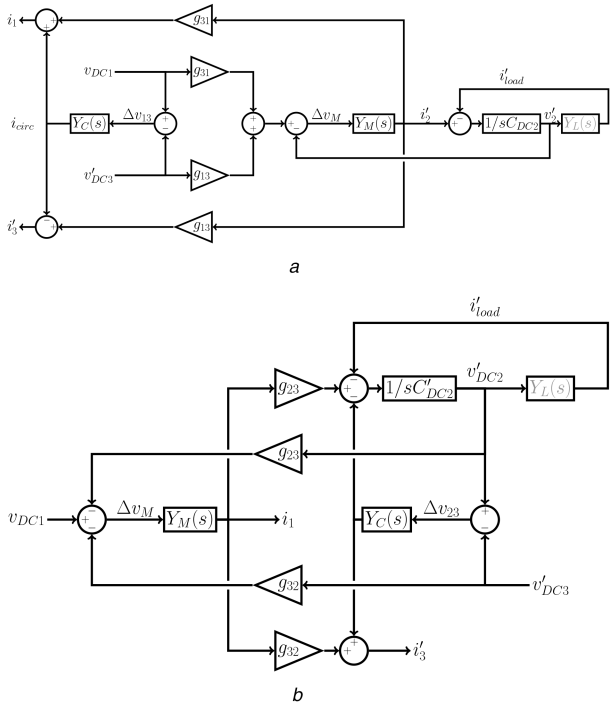

Fig. 10 *Modelling MEG operation modes*
(a) DISO1, ***(b)*** SIDO1

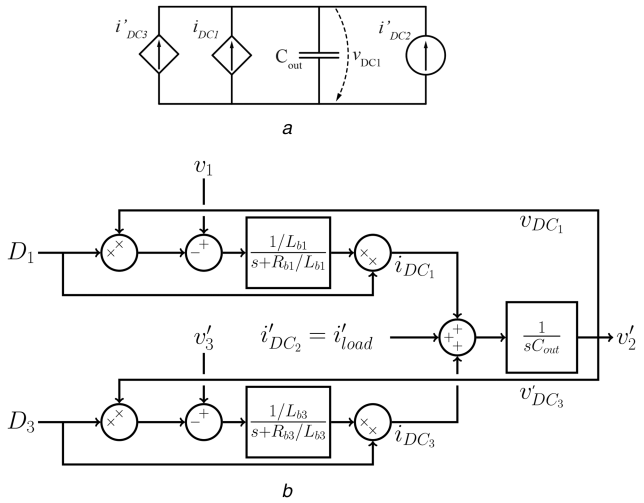

Fig. 11 *Single module equivalent models*
(a) Electric equivalent, ***(b)*** Plant transfer function

the ports 1 and 3 into/from C_{out}. The difference between DISO1 and SIDO1 modes is the direction of i_3 current (positive/negative for DISO1/SIDO1 mode). Clearly, this redefinition of the plant permits a more efficient outer-loop strategy for the proposed MEG concept. In other words, it is possible to use one degree of freedom to tightly regulate the voltage at the output terminal $v_2 = (n_2/n_1)v_{\text{out}}$, and another one to regulate the SOC of the ES element connected to terminal 3.

3.2 MEG control scheme

From previous approach, a simplified scheme is also feasible for the MEG complete converter depicted in Fig. 7. Since all the submodules, and their respective C_{out} are connected in parallel on the LV side, the plant can be seen as a single equivalent capacitor

$$C_{\text{tot}} = N_{\text{s}} C_{\text{out}} \tag{17}$$

The simplified equivalent circuit and plant are depicted in Fig. 12. The controllable state variables are the current through the series-connection of the terminal 1 of the N_{s} submodules, namely i_{MV}, the

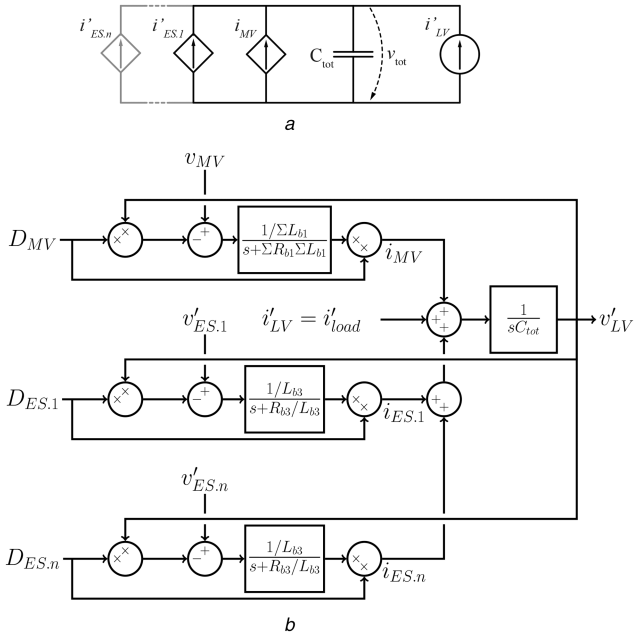

Fig. 12 *ISOP converter equivalent models*
(a) Electric equivalent, ***(b)*** Plant transfer function. The behaviour of the load (whether it is on the MV side or the LV side) is not known. In order to size regulators gains, a resistive load $R_{L,\text{nom}}$ is considered and thus $i'_{LV} \simeq v'_{LV}/R_{L,\text{nom}}$

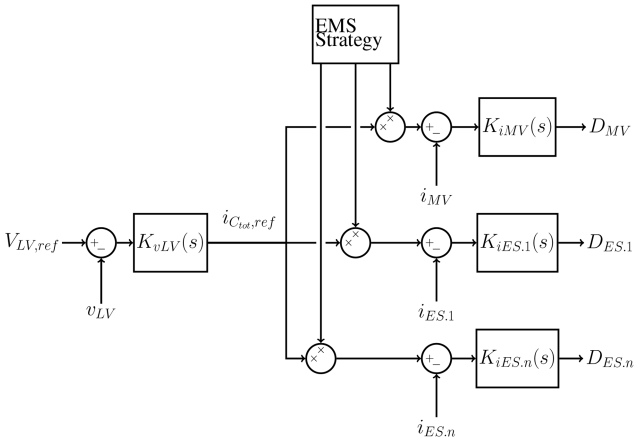

Fig. 13 *Proposed MEG control structure with one voltage regulator, one strategy function and* $(n + 1)$ *current regulators*

N_{s} currents $i_{\text{ES.1}-N\text{s}}$ from the storage elements and the voltage $v_{\text{tot}} = v'_{\text{LV}}$ on the equivalent capacitor C_{tot}. The same way as for a single submodule, this voltage can be regulated indirectly, with a slow voltage control loop $K_{v2}(s)$ through the $N_{\text{s}} + 1$ currents from/to the MV port and the storage ports. The output reference from the voltage controller $K_{v2}(s)$, namely the sum of the current references, has to be shared between the ports following a certain strategy. This sharing of the power to/from the MV grid and each storage element is responsibility of an upper application level energy management system (EMS) (State-of-charge control, optimised battery management etc.). Then, these currents can be regulated independently with higher bandwidth control loops $K_{i_{\text{MV}}}(s)$, $K_{i_{\text{ES.1}}}(s)$ to $K_{i_{\text{ES}\,.\,N\text{s}}}(s)$ and the duty-cycles D_{MV} and $D_{\text{ES.1}}$ to $D_{\text{ES}\,.\,N\text{s}}$ (c.f. Fig. 13).

3.3 Controllers tuning

All regulation strategies refer to dc-variables, so proportional integer (PI) regulators of the form

$$K(s) = \frac{k_p s + k_i}{s} \tag{18}$$

are employed. Internal model-based control is used to select the regulators parameters [46], with the aim to cancel the main pole of the plant with the zero of the PI regulator [47]. Firstly, the tuning of innermost current controllers is considered. An inductive filter of parameters L_B and R_B defines the plant. The R_B term should include an estimation of the switching operation losses [42, 48]. The tuning of the system is then

$$\begin{aligned} k_{p,i} &= \alpha_i L_B \\ k_{i,i} &= \alpha_i R_B \end{aligned} \tag{19}$$

with α_i being the theoretical bandwidth, which, according to the one-to-tenth rule, should not exceed $2\pi/10T_{\text{sw}}$.

For the voltage outer loop, the plant is a function of the total capacitance and the nominal load $R_{L,\text{nom}}$, i.e.

$$\begin{aligned} k_{p,v} &= \alpha_v C_{\text{out,tot}} \\ k_{i,v} &= \alpha_v / R_{L,\text{nom}} \end{aligned} \tag{20}$$

with α_v being the theoretical bandwidth, which, according to the one-to-tenth rule, should not exceed $1/10\alpha_i$. Following the same criterion, the current references from the EMS are set with similar dynamics as the outer loop.

4 Experimental and simulation results

In order to demonstrate the operation of the MEG converter, both simulation and experimental results are presented in this section. First experimental results from a low voltage prototype (200 V/3 kW) show the operation of a single submodule. Then, the operation of the complete converter is demonstrated through simulation with the example of a peak shaving converter for PV application (10 kV/0.5 MW).

4.1 Experimental setup

The low voltage setup (c.f. Fig. 14) consists in a complete sub-module and a storage element made of a super-capacitor with a capacitance around 2 F. The converter comprises a three-winding MFT with a 1:1:1 turn ratio, equipped with resonant tanks with the parameters presented in Table 2. The MFT is designed with a resonant frequency $f_{\text{res}} = 12\,\text{kHz}$ and is operated with a switching frequency $f_{\text{sw}} = 10\,\text{kHz}$. The five half-bridge converters S_{1-5} are made of PEB-4046 modules from Imperix [49] with IXYS MMIX1X200N60B3H1 IGBTs. In order to benefit from ZVS, the dead-times for all bridges are set to 1.6 µs, corresponding to their minimum value in low voltage condition increased by a certain margin. The regulation stage of ports 1 and 3 are equipped with inductors filters L_{b1} and L_{b3} both of 3 mH. The control is done using Imperix Boombox control platform. For the experiment, a resistive load is connected on the port 2, a DC voltage source is connected on the port 1 and the super-capacitor is connected on the port 3. The voltage on the load (output voltage) v_{DC_2} is actively regulated to be 200 V while the super-capacitor on the port 3 is charged and discharged between 100 and 150 V with a constant current reference. Oscilloscope measurements over the complete sequence are presented in Fig. 15 while a detailed view of the resonant currents over two switching periods are depicted for SISOa mode, SIDO1 mode and DISO1 mode respectively in Figs. 16*a*–*c*.

4.2 Full converter simulation

The simulated MEG converter has the parameters presented in Table 3. The application presented is the one depicted in Fig. 1*c*, where the LV side is the collection point of a PV park and the MV side is an MVDC grid.

The storage has to be sized in terms of power and energy to fulfil the application specifications, which for the case of partial shading implies capability to support the grid with certain P_{ES} during 10 s for instance. In terms of energy this would correspond

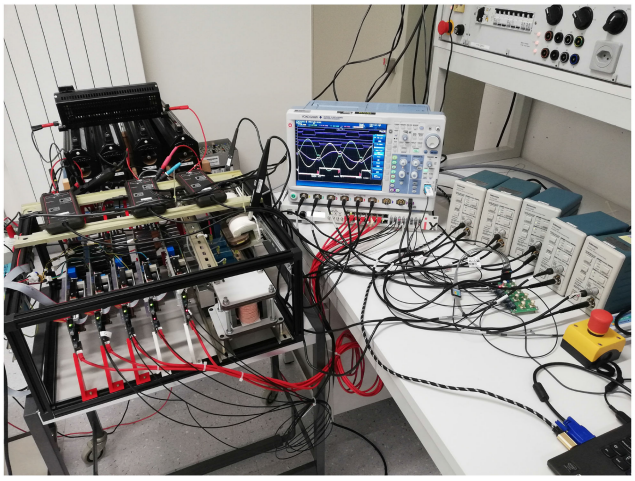

Fig. 14 *Low voltage prototype of one MEG submodule*

Table 2 LV prototype: passive components

Resonant tank	DC capacitors	
$L_1 = 70\,\mu\text{H}$	$C_1 = 2.5\,\mu\text{F}$	$C_{\text{DC}_1} = 748\,\mu\text{F}$
$L_2 = 35\,\mu\text{H}$	$C_2 = 5\,\mu\text{F}$	$C_{\text{DC}_2} = 1650\,\mu\text{F}$
$L_3 = 35\,\mu\text{H}$	$C_3 = 5\,\mu\text{F}$	$C_{\text{DC}_3} = 825\,\mu\text{F}$

to 280 Wh that can be stored at 100 V rated, 3 Ah battery modules or 80 F, 160 V rated ultra-capacitor modules. In the case of MEG, this is split between the N_s storage elements.

The number of MEG submodules the semiconductor technologies and the operating frequencies are closely linked and have to be designed coherently. The voltage on the MV side V_{MV} with selected semiconductor voltage class for port 1, defines the number of submodules. To be able to operate the converter in case of faults (e.g. with one submodule bypassed) the sum of possible DC voltages $V_{\text{DC}_{1_i}}$ of the $N_s - 1$ remaining submodules has to be higher than the MVDC grid voltage

$$V_{\text{DC}_1} \geq \frac{V_{\text{MV}}}{N_s - 1} \tag{21}$$

For the specified V_{MV} of 10 kV, one considers the use of the 4.5 kV IGBTs for S1 and S4 stages and the operation with 2.5 kV as the rated voltage for the V_{DC_1}. This implies that the MEG could be realised with $N_s = 5$ submodules. On port 2, semiconductors rated for 1.7 kV could be used, while on the port 3, 1.2 kV voltage class is sufficient (considering IGBT devices). The actual design of the storage components, or semiconductor devices are subject to further optimisation, which is not in the scope of this paper.

For the simulations, the switching frequencies are selected as shown in Table 4. The buck/boost inductors are sized accordingly to (14) and (15), resulting in $L_{b1} = 5\,\text{mH}$ and $L_{b3} = 3\,\text{mH}$. Following the design methodology presented in Section 2.1 for a ratio f_n of 0.95 and a magnetising inductor L_{m_1} of 10 mH, the passive components for the resonant tank and the different DC links are given in Table 5.

The control structure is implemented as presented in Fig. 13, with an EMS strategy aiming to use the storage elements to compensate any variation on the power provided by the LV port and minimise its impacts on the power injected on the MV side.

Numerous strategies could have been implemented in EMS block. One of them is the peak shaving application as demonstrated in Fig. 17. In this example, two storage elements ($\text{ES}_{1,2}$) are considered to be super-capacitors while the three others ($\text{ES}_{3,4,5}$) are batteries, with appropriate ratings. A detailed description is provided in the captions, and the simulated case demonstrate capabilities of MEG to effectively decouple the different ES technologies and utilise them effectively during dynamic response

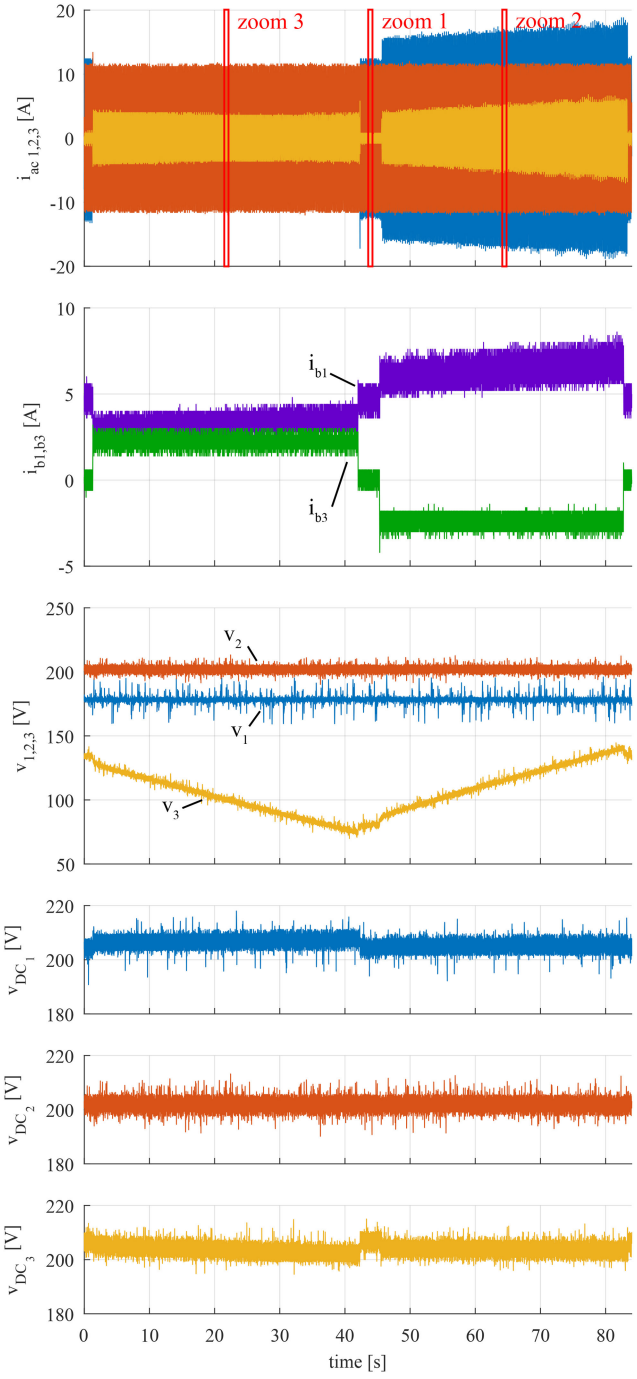

Fig. 15 *Operation of one submodule. From top to bottom: DC-transformer currents envelope, regulation stage current, grid side and storage voltage, DC-bus voltages. Between t = 2 and t = 42, the super-capacitor is discharged. The current i_{b3} is positive and the system is in DISO1 mode. Around t = 45, the port 3 is turned off, i_{b3} is zero and the system is in SISOa mode. Between t = 46 and t = 84, the super-capacitor is charged, i_{b3} is negative and the system is in SIDO1 mode. v_{DC2} is well regulated to 200 V while v_{DC_1} and v_{DC_3} are subject to some light variations due to cross-load regulation. Detailed view of the resonant current waveforms are shown in Fig. 16*

to grid changing conditions while providing an effective control of the output voltage and power delivered to the grid.

5 Conclusion

This paper presents the topology of a medium voltage fully-bidirectional multiport DC–DC–DC converter, referred to as MEG. It is based on the combination of multiple identical submodules, connected in series on the MV side and in parallel on the LV side. Each submodule comprises an open-loop operated resonant stage

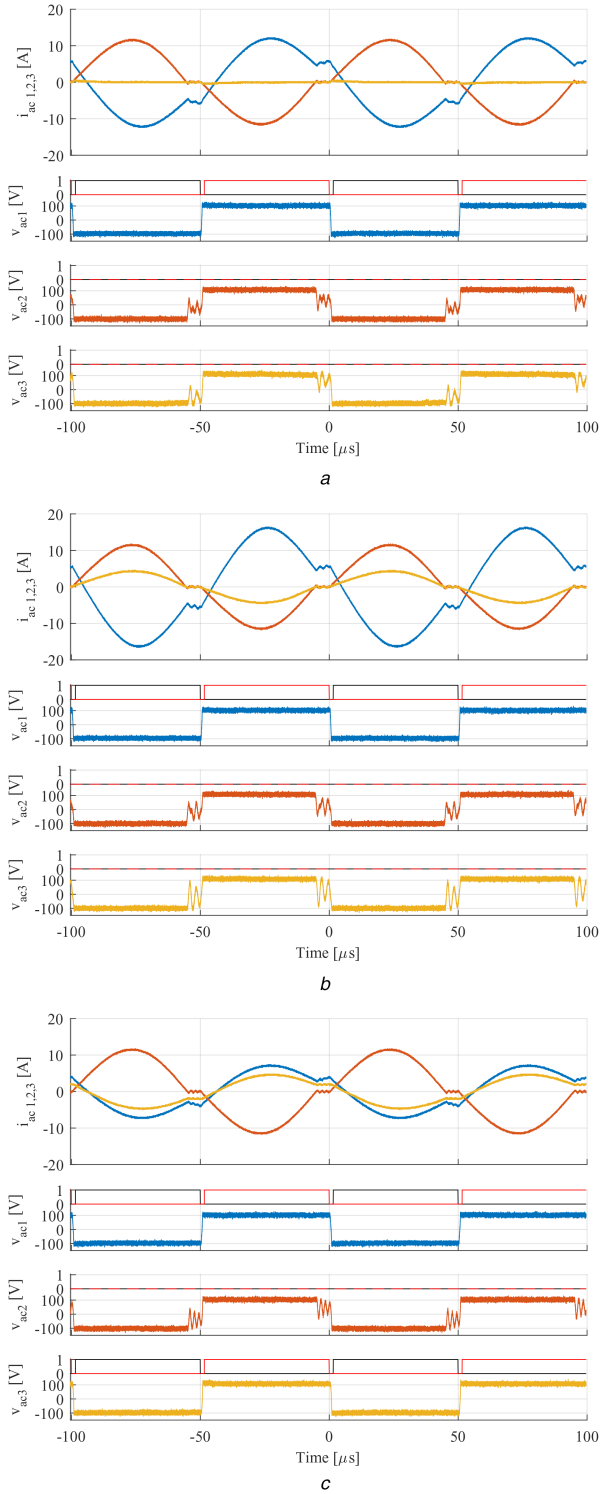

Fig. 16 *Resonant currents and AC voltages (port 1 in blue, port 2 in red and port 3 in yellow)*
(a) Zoom 1: SISOa mode, ***(b)*** Zoom 2: SIDO1 mode, ***(c)*** Zoom 3: DISO1 mode. For the active ports, the voltage changes polarity within the deadtime, and the switches benefit from ZVS at turn-on. During DCM interval, AC voltages of the passive ports (rectifiers) are subjects to some oscillations between the resonant inductor and the output capacitance of the diodes

(DC transformer), and an additional closed-loop operated regulation stage. In this way, the conversion functions, voltage adaptation, galvanic isolation and control, have been clearly separated between the different stages which allow for optimisation

Table 3 Power and voltage ratings at the converter level

Port	Rated power	Rated voltage
MV	$P_{MV} = 0.5\,MW$	$V_{MV} = 10\,kV \pm 20\%$
LV	$P_{LV} = 0.5\,MW$	$V_{LV} = 750\,V \pm 20\%$
ES	$P_{ES} = 100\,kW$	$V_{ES} = 450\,V \pm 33\%$

Table 4 MEG switching frequencies

Switches	Switching frequency
S_1,S_2,S_3	$f_{sw} = 5\,kHz$
S_4	$f_{s4} = 2.5\,kHz$
S_5	$f_{s5} = 10\,kHz$

Table 5 Passive components

Resonant tank		DC capacitors
$L_1 = 100\,\mu H$	$C_1 = 9.14\,\mu F$	$C_{DC_1} = 100\,\mu F$
$L_2 = 9\,\mu H$	$C_2 = 101.6\,\mu F$	$C_{DC_2} = 360\,\mu F$
$L_3 = 16.2\,\mu H$	$C_3 = 56.4\,\mu F$	$C_{DC_3} = 1\,mF$

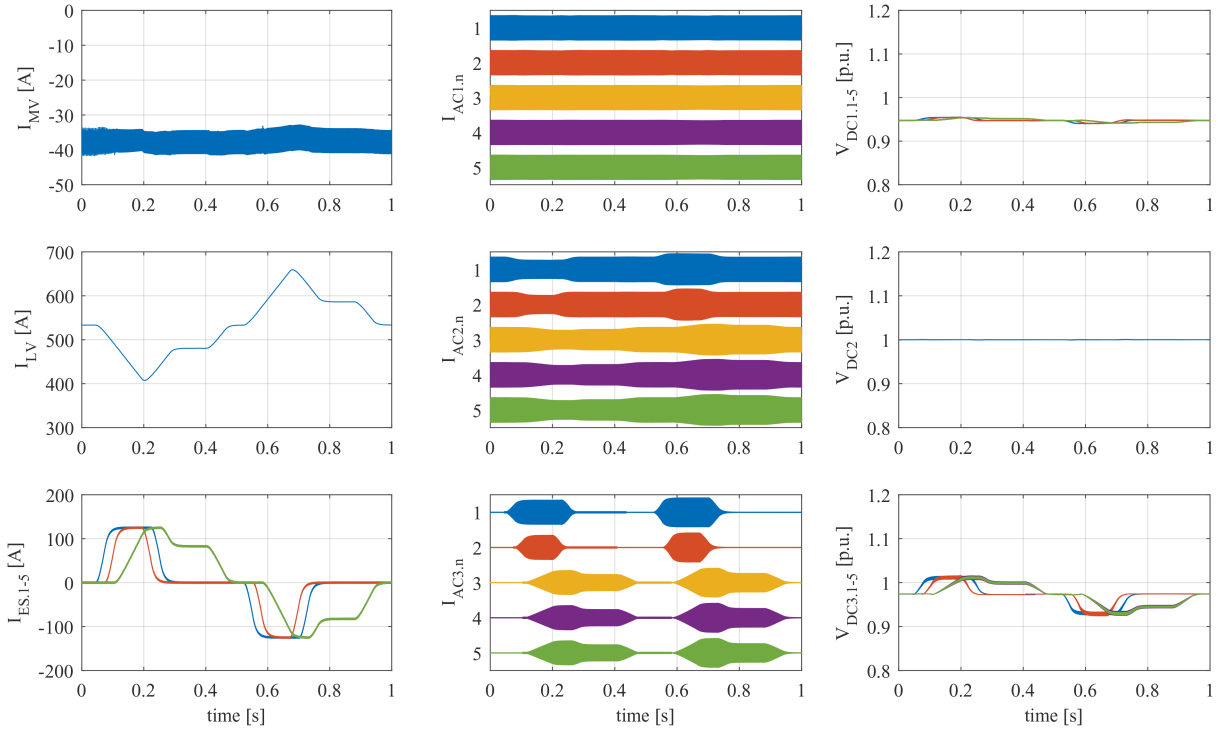

Fig. 17 *Simulation results: on the left hand side: The DC currents on the MV port, the LV port and the five ES ports. The current provided by the LV port is subject to variations which are compensated by the currents from ES ports in order to decrease the impact on the current injected on the MV side. In the middle: the envelopes of the resonant currents for the three ports MV, LV and ES. The ES ports are used independently which allows for optimised storage management strategy. On the right hand side: the DC-bus voltage of the five submodules and the cross-load regulation effects (in p.u.) for the three ports.* v_{DC2} *corresponds also to* v_{LV} *and is regulated to 750 V*

of each of them. The operating modes of the converter have been described and a simple control scheme is proposed, allowing for full bidirectionality and power flow control. The MEG is characterised with multiple auxiliary ports which are made available for the connection of LV storage elements that can be freely mixed in terms of technologies (ultra-capacitors or batteries) and thus, flexible and easily scalable grid supporting solutions can be realised.

Experimental results demonstrate the operation at the submodule level while the simulation results verify the operating principles and the use of the complete MEG converter. The simulation case is a peak shaving application, but the MEG is not limited to this alone: the presented topology of allows further extensions to the higher operating voltages by increasing the number of submodules connected in series (MFT insulation must be taken into account and will directly depend on the system operating voltage). To increase the rated power, paralleling multiple units at the submodule or the converter level is also possible. High flexibility and inherent simplicity are the main characteristics of the MEG, making it feasible enabling technology for the emerging MVDC applications.

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