Low Voltage Modular Multilevel Converter Submodule for Medium Voltage Applications

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Abstract

Modular multilevel converters have been subject to various research topics in the area of medium voltage conversion. The basic building block of all modular multilevel converters is the submodule, which despite being simple in terms of its topology, poses significant integration challenges when it comes to practical implementation. This paper provides an insight into the structure, design considerations and operation of the modular multilevel converter low voltage submodule for medium voltage applications. Special attention was paid to the submodule specific power and control parts, which were all experimentally tested, with all results being presented in the paper.

1 Introduction

Emergence of Medium Voltage (MV) DC grids creates the need for a highly flexible and efficient DC power source. One such possibility is presented in Fig. 1, where the conventional twelve pulse transformer (commonly used in combination with diode/thyristor rectifiers) is connected with two Modular Multilevel Converters (MMCs) having their DC terminals connected in series. Replacement of the diode/thyristor rectifiers with the MMCs enables the grid current controllability, fast and flexible DC voltage generation, able to counteract the short circuits across the converter DC terminals. Converter being developed is rated at 500 kVA and should be able to generate arbitrary voltage in the range of $\pm 10\,\text{kV}$ at its DC terminals.

So far, a number of MMC research prototypes have been reported in the literature, yet most of them developed as a Low Voltage (LV) prototypes [1]–[4], with rated power up to 45 kW [1]. Notable exception from academia of a 2 MW rated power MMC based AC/AC converter is presented in [5], whereas very few information from industry could be found. Integration of various technologies for an IGBT Submodule (SM) has been presented in [6], whereas [7] provides a
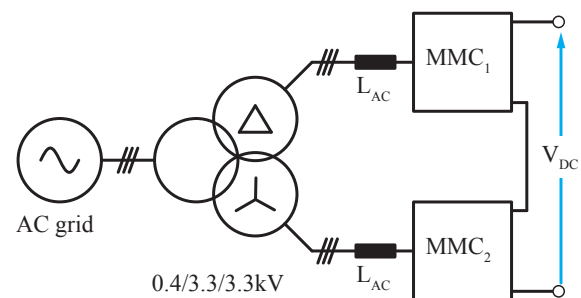

Fig. 1: Structure of the MMC based rectifier

thorough comparison between IGBT and IGCT semiconductor technologies in MMCs for AC/AC railway power supply applications, thus being valuable resource from the industry.

This paper presents the overall structure, design considerations and operation of the MMC SM for MV applications. Descriptions are accompanied by the experimental results, validating the correctness of the design procedure. SM is realized with LV semiconductors, and it could be used in any other MMC based topology, providing voltage and power ratings of the SM are not violated.

2   Submodule Structure

The use of MMC provides an opportunity to realize a highly flexible, bipolar DC source, given that a bipolar SMs are used [8]. Although various topologies of a bipolar SMs exist in the literature [9], developed SM is realized utilizing Full Bridge (FB) topology, mainly due to simplicity reasons. Despite simple in terms of its topology, practical implementation of MMC SM being used in MV application poses significant integration challenges, such as the need for an auxiliary power supply, proper insulation coordination, employment of internal protection, proper thermal design, current and voltage measurements, certain communication links with upper level controllers, etc.

Utilizing commercially available LV power components was the foundation for the converter design, and it was mainly driven by low cost design targets. Therefore, bipolar property of the submodule has been achieved with 1200 V IGBT H-bridge module, with a possibility of effortless mechanical reconfiguration to the unipolar structure. The choice of the 1200 V rated IGBT module and 5 kV DC voltage rating of a single MMC imposed the need for N=8 SMs per single MMC branch, with each SM average voltage being set as 625 V.

The structure of realized SM is shown in Fig. 2. It has several electronic circuits performing different functions, which are organized and split between two interconnected Printed Circuit Boards (PCBs): Power PCB and Control PCB, as described in details, hereafter.

3   Power PCB

Power PCB is a power processing part of the SM, hosting its main power components: IGBT H-bridge module and the bank of electrolytic capacitors. Apart from the key components, Power PCB also accommodates SM voltage and current measurement circuits, SM protection devices, capacitor balancing and discharge circuit, power terminals and board-to-board connectors with the Control PCB.

3.1   IGBT module

IGBT module from Semikron is rated at 1200 V/50 A, and features NTC temperature sensor [10]. By means of mechanical reconfiguration (HR in Fig. 2), also hosted at the Power PCB, it is possible to change the SM structure to unipolar, thus doubling its current capability to 100 A.

3.2   SM capacitor bank

Submodule capacitor bank was designed according to the permissible energy ripple within a MMC branch (determines the capacitance value), as well as according to the admissible AC current ripple per capacitor (determines the number of paralleled capacitors).

Series connection of two electrolytic capacitors within the SM is necessary as the SM rated voltage (625 V) is higher than the rated voltages of commercially available electrolytic capacitors (450 V in our case). Therefore, the SM capacitor
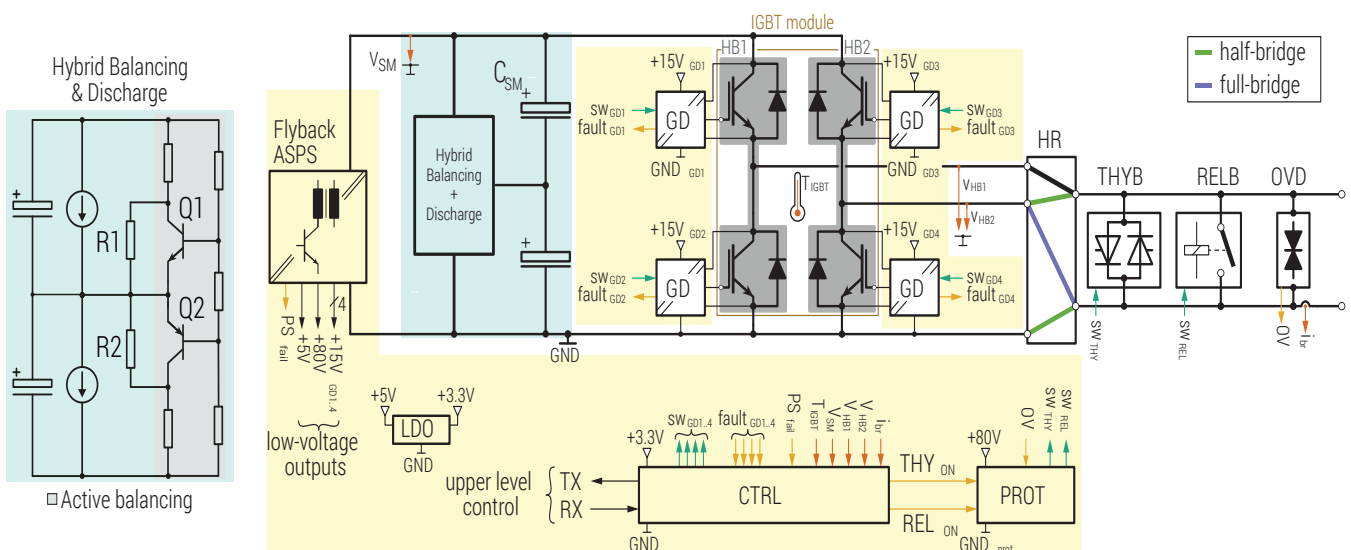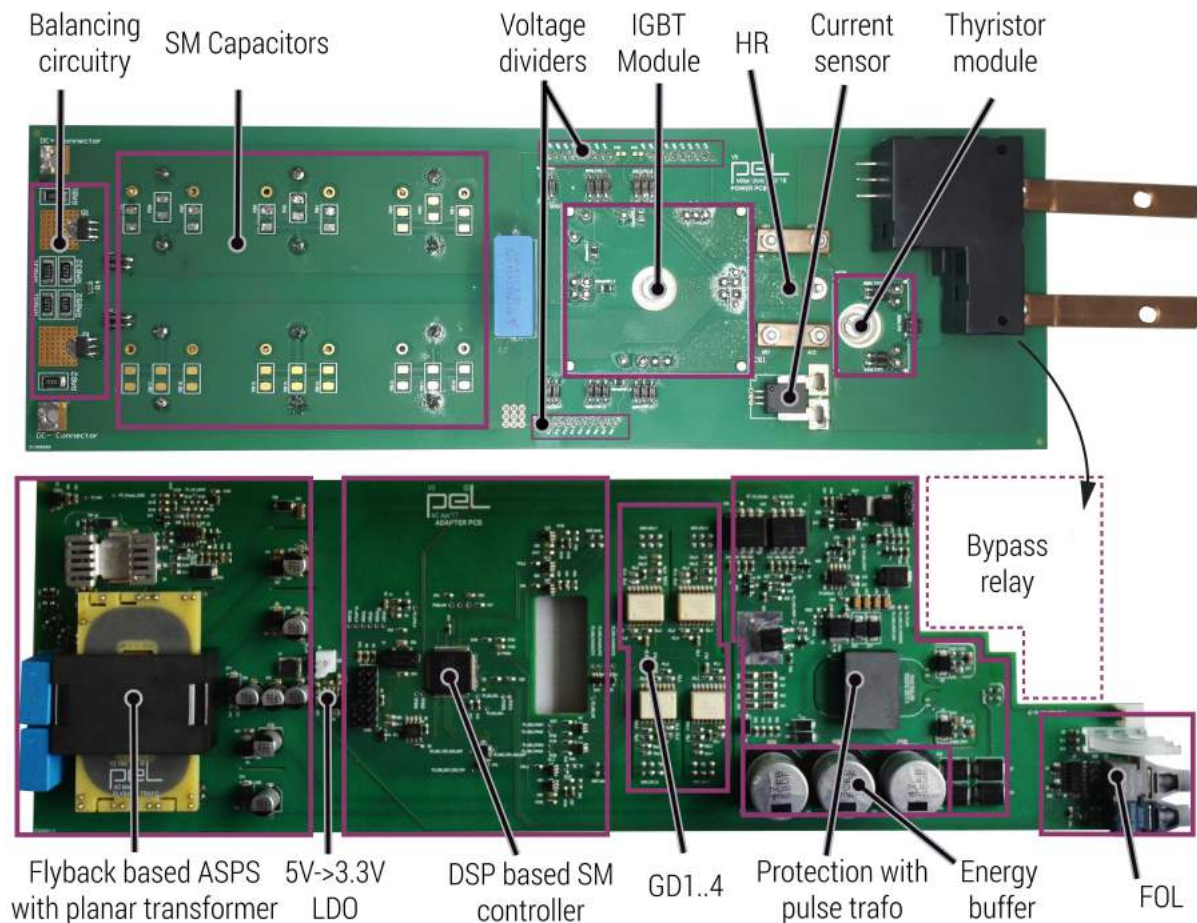

Fig. 2: MMC Submodule structure. Parts hosted at the Control PCB are labeled yellow.

Fig. 3: Developed MMC Submodule: Power PCB (Top), Control PCB (Bottom)

bank is realized as a parallel connection of three capacitor branches, each one of them consisting of a series connection of two 1.5 mF capacitors, giving the equivalent capacitance of C_{SM}= 2.25 mF. Employment of series connection of 450 V maximum rated capacitors within the SM, demands the insulation coordination being conducted for maximum expected SM voltage of V_{SMmax}=900 V. Furthermore, appropriate control and protective measures have to be taken in order to ensure that capacitor voltage does not exceed the limits. As expected, the problem of voltage sharing between such two capacitor groups arises, therefore hybrid balancing circuitry is utilized.

3.3 Hybrid balancing circuit

Initially, simple and well known passive balancing circuit was considered and implemented in the design. In order to maintain the voltage difference between the upper and the lower capacitor banks

of the SM within the range of ±7 V, three passive balancing resistors of $62\,k\Omega$ are mounted in parallel with each SM capacitor. Experiments (c.f. Fig. 4 (top)) have proven that this arrangement of resistors provides the balancing function, yet with the cost of prohibitively high power losses (30 W at V_{SM}=650 V).

Another approach was to consider hybrid balancing with the aim of reducing power losses, while preserving balancing performance. As shown in Fig. 2, it consists of Active Balancing (AB) circuit introduced in [11], reinforced with the two additional resistors, R1 and R2, in parallel with the transistors Q1 and Q2, respectively. Those two resistors aim to prevent over-voltages across the accompanied transistors, as well as to serve as a backup solution in case of fault of any of the transistors within the AB circuit. Under the faulty terms, additional resistors take over the role of passive balancing circuit.

Experiment with hybrid balancing was conducted
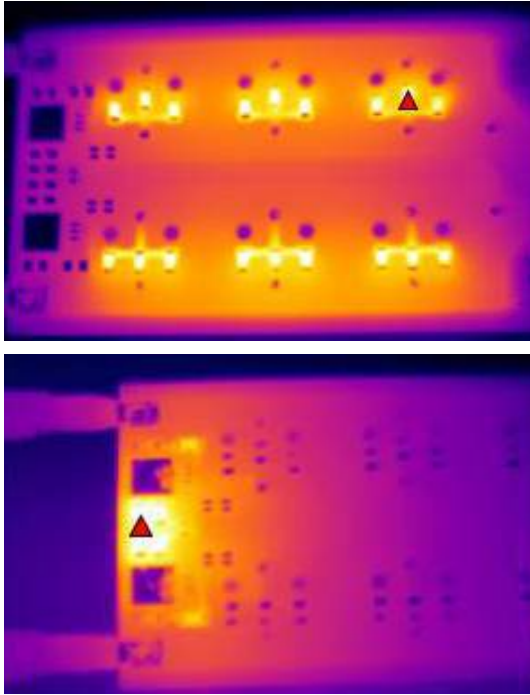
Fig. 4: Thermal images of the passive (top) and hybrid balancing (bottom)

(c.f. Fig. 4 (bottom)), and the power consumption was measured to be 4.7 W. Therefore, hybrid balancing shows great advantage over the passive balancing method in terms of significant power consumption reduction for the same balancing performance, without penalizing the circuit reliability and cost.

3.4 Voltage and current measurements

Voltage and current measurements within the SM are hosted at the Power PCB. Current sensing (i_{br} in Fig. 2) is realized with Allegro ACS759 Hall-effect-based linear current sensor with $100\,\mu\Omega$ internal resistance, having the performance optimized at 3.3 V. Measured current values are passed on to the SM's main controller.

Voltage measurements are performed at the three specific points within the SM: SM capacitor voltage (V_{SM} in Fig. 2), as well as the Half-Bridge (HB) voltages of the IGBT module with respect to SM ground (V_{HB1} and V_{HB2} in Fig. 2). Measurements are performed by means of resistive voltage dividers, and adjusted to match the 3.3 V range, suitable to the SM's main controller. HB voltage measurements are of particular importance to the SM's protection logic, as they provide feedback

information about the protection activation.

3.5 Protection devices

Submodule's protection consists of protection devices, situated between the SM's terminals, and protection logic that activates the devices, which is hosted at the Control PCB. Protection is realized by means of bypass thyristor module (THYB) and bypass relay (RELB), which bypass the SM in case of fault, as well as Over-Voltage Diodes (OVDs), aiming at over-voltage detection and protection activation.

4 Control PCB

Control logic of the SM is accommodated at the so-called Control PCB. Layout of the Control PCB is presented in Fig. 3, from which several mutually independent circuits can be identified: Auxiliary Submodule Power Supply (ASPS),SM's main controller, gate drivers' circuits, SM's protection logic and fiber-optic communication link (FOL). By means of board-to-board connectors, which provide both mechanical support and electrical connection, Control PCB is mounted on the top of the Power PCB.

4.1 Auxiliary Submodule Power Supply

In order to simplify insulation requirements in the surrounding of the SM, as well as due to the simplicity of implementation, a Flyback converter with multiple outputs, supplied from the SM's capacitor, was chosen as a solution for the ASPS. Its simplicity lies in the fact that a single switch controls multiple transformer's secondary outputs by means of cross-regulation. Flyback transformer is realized as a planar transformer with PCB integrated windings, and hosts seven secondary windings in total. Feedback voltage used in regulation is a +5 V output, which is further on regulated to +3.3 V by means of Linear Dropout Regulator (LDO), for the purpose of the SM's main controller supply. Another secondary output provides +15 V, used as a self-supply to the main Flyback PWM controller. Apart from this secondary, four +15 V secondaries with floating grounds supply the four IGBT gate drivers. Proper insulation coordination between upper and lower gate drivers was considered. Protection trigger
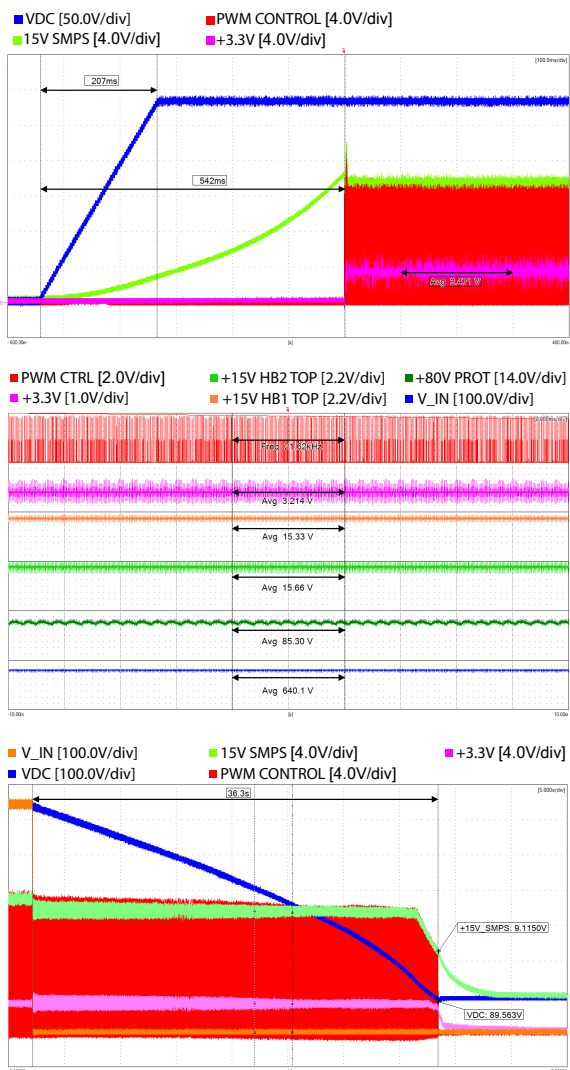
Fig. 5: Flyback based ASPS operation: startup (top), normal operation (middle), SM bypass and ASPS shutdown (bottom)

circuitry is powered by +80 V secondary output with floating ground. This voltage level was chosen so as to provide enough energy reserve within the protection trigger circuitry, utilizing relatively small storage capacitors. This energy reserve is of particular importance in case of ASPS fail, when the protection activation relies solely upon the energy reserve.

Fig. 5 presents the results of the experiments conducted to verify the ASPS functionality. Due to the fact that ASPS is internally supplied, SMs have to be passively charged, until the ASPS is activated. During charging of the MMC SMs from the AC side terminals, externally installed precharge resistors limit the inrush currents. During that period SMs are charged through their freewheeling diodes, until

each SM attains 290 V, which corresponds to the peak line voltage divided by the total number of SMs per phase leg. This voltage is sufficient to activate the Flyback based ASPS, which boots the SM's main controller and establishes communication with upper layer controller, bringing the MMC into operational state.

In order to emulate this process, the SM is connected to the controllable power supply, which attains 290 V within 200 ms, corresponding to the real charging conditions in the prototype under development. Fig. 5 (top) shows that it takes around 500 ms for the ASPS to start the normal operation. The same figure (middle) shows the normal ASPS operation, where the SM is connected to 650 V Direct Current (DC) power supply, which closely corresponds to its normal operating point. Finally, at bottom part of the figure the shutdown process of the ASPS is shown. SM is bypassed, therefore due to the consumption of the ASPS the SM capacitor is being discharged (voltage labeled as VDC in Fig. 5). Once the ASPS is turned-off resistors within the hybrid balancing circuit provide a slow discharge of the residual energy.

4.2 Main SM controller

SM controller is realized by means of TMS320F28069 Digital Signal Processor (DSP) . It handles multiple functions, such as: communication with upper level control (through Fiber Optic Link (FOL)), voltage and current measurements (V_{SM}, V_{HB1}, V_{HB2}, i_{br}), decentralized modulation through gate driver switching signals ($SW_{GD1..4}$), monitoring the SM condition (IGBT module temperature (T_{IGBT}), IGBT gate driver fault state (fault GD1..4), ACPS failure with PS_{fail}, etc). In case of fault on any of these devices, SM protection is activated and the SM is bypassed. Controller communication with the upper level control system is achieved through the FOL, where valuable information are exchanged, such as command signals, SM state-of-charge, etc.

4.3 Gate drivers

SM gate drivers are realized by means of Avago ACPL-332J optocouplers, ideally suited for driving IGBTs in a voltage range up to 1200 V and 150 A. Short circuit supervision along with desaturation detection is implemented, and feedback signals are provided to SM's main controller.
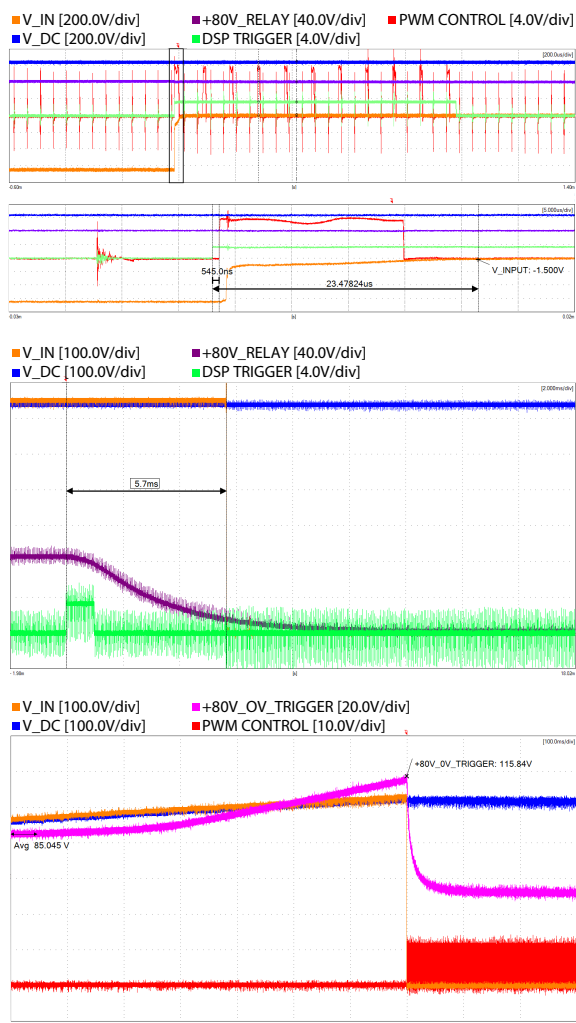
Fig. 6: SM protection test: bypass thyristor activation (top), bypass relay activation (middle), over-voltage detection (bottom)

4.4 SM Protection

Protection of the SM is realized by means of anti-parallel thyristors, providing the temporary bypass, and permanent bypass implemented with bi-stable relay. Once the faulty condition is detected within the SM, its main controller issues the command for protection activation. At first, bypass thyristor module is activated, and its primary role is to provide temporary path to the branch current until the relay closes its contacts, thus providing permanent bypass of the SM.

SM is also protected against an excessive voltages across its power terminals. It is realized utilizing transil OVDs, which go into the breakdown once the voltage across the SM's terminals exceeds V_{SMmax}=900 V. Over-voltage detection results in both bypass thyristor and relay activation.

Functionality of the SM protection has been thoroughly experimentally tested and three different scenarios are shown in Fig. 6.

In the first case, bypass thyristor has been triggered from the SM's main controller and it took 545 ns for the protection circuitry to fire its first thyristor turn-on pulse. It can be noticed from the Fig. 6 (top) that the thyristor bypassed the SM terminals 23 µs after the DSP command was issued. Two anti-parallel-connected thyristors are pulsed with 10 kHz (with 10 % duty cycle) signal, thus providing the path for either current direction.

Middle plot of Fig. 6 demonstrates the functionality of the bypass relay. It has been measured that the relay closes its contacts within 5.7 ms from the moment when the DSP command is issued. This confirms the need for the anti-parallel-connected thyristors as a fast, temporary bypass. Should the SM be unprotected for this amount of time, it would be exposed to the hazardous risks.

Finally, activation of the SM's protection in case of over-voltage detected at the terminals is demonstrated in the Fig. 6 (bottom). Down-scaled test has been carried out, where the voltage across the SM's terminals was gradually increased up to the point where it triggered the protection. In this case, SM's main controller did not issue any command, but the protection was activated owing to the breakdown of the transil OVD diodes, detected by the protection circuitry.

5 Power test

Finally, scaled down power test of the SM is conducted (limited due to ratings of the used power supplies). SM capacitor bank was connected to the constant DC power supply, whereas an inductive load was connected to its power terminals. This test aimed to verify the functionality of the SM's main controller, gate drivers, and IGBT module. Fig. 7 shows the pulse-width-modulated output voltage as well as the SM output current. Bipolar modulation is implemented, and test is conducted at SM rated voltage, with the switching frequency of 1 kHz. Even though the switching frequency was higher than the one intended for the SM regular operation, it was possible at the cost of reduced output current during the test.
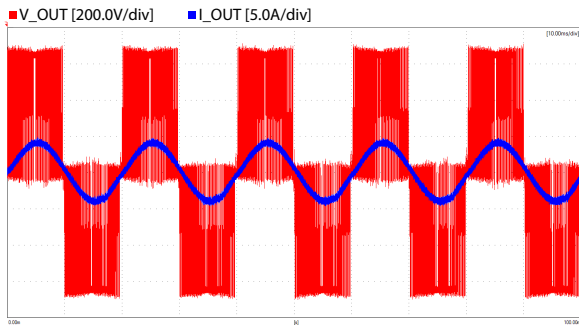
Fig. 7: Power test of the developed SM

6 Submodule integration

From the converter point of view, various analyses were conducted which influenced the SM design. Although their complexity and objectives exceed the scope of this paper, its worth mentioning it for the sake of completeness.

6.1 Thermal design

Proper SM evaluation in terms of the IGBT module and capacitor power losses has been conducted, considering real operating conditions. PLECS simulations were performed and apart from the fundamental AC current component, both DC and second harmonic circulating currents are considered. Apparent switching frequency of 3 kHz, corresponding to a SM switching frequency of $f_{sw_{SM}} = 250$ Hz was used in simulations, as presented in [12]. It has been shown that the worst operating condition in terms of IGBT power losses corresponds to the unity power factor with 58 W of losses, whereas in terms of capacitor losses it has been shown that the peak value of 5 W occurs at the zero power factor. Taking the former losses into consideration, along with the most critical ambient conditions, proper heatsink was chosen.

SM's enclosure, besides its mechanically protective and field shaping functions, has the role of providing the proper airflow path through the SM's heatsink and around the capacitors. Cabinet level cooling is conceived to be realized as forced air cooling with the airflow at the SM's outtake being 45 m³/h. FEM simulations have been carried out and verified the performance of the cooling system [12].

6.2 Insulation coordination

Necessary insulation clearance and creepage distances wihin the SM are determined in accordance with the UL 840 standard, whereas the insulation coordination at the converter level has been conducted considering safety standard IEC 61800-5-1.

Each SM is enclosed in an aluminum box, providing shielding, protection and shaping of the surrounding electric field at the corners below the critical levels, considering air insulation inside the cabinet. Its protruded front and back leads provide path to the air flow of the cooling system. Detailed analysis of the overall converter insulation has been conducted in [13], while the realized mechanical subsystems are shown in Fig. 8.

7 Conclusion

This paper presented the structure and design considerations of the LV MMC SM for MV applications. Although simple at the first glance, owing to the simple schematics of the power circuit, developing a reliable MMC SM requires a lot of engineering effort. Integration of various part, with different tasks being assigned to them, was demonstrated, showcasing the excellent and reliable operating performance of the constructed SM. Realized MMC platform allows for great flexibility in conducting various research activities, results of which will be reported in the near future.
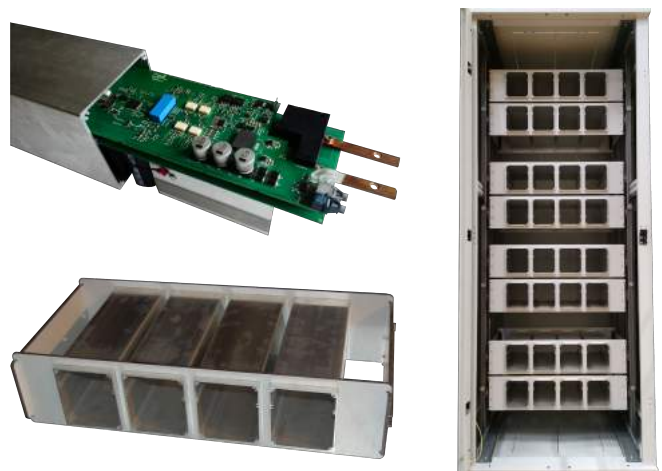

Fig. 8: SM with aluminum enclosure (top), SM's drawer (bottom), MMC cabinet (right)

Acknowledgment

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