Toward ultra-low power design methodology for frequency generation in the IoT design space

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The clock that stands still,
and points resolutely in one direction,
is certain of being right twice in the four and twenty hours.
While others may keep going continually,
and continually be going wrong.
— Lewis Carroll

To my family...

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Lausanne, 8th March 2019

Mathieu Coustans

Abstract

Today, the semiconductor industry is feeding our digital world with more and more data coming from compact embedded electronics that are monitoring our environment and feeding analytics for action. Interaction with our digital world is mostly achieved through Internet connectivity. The idea of the Internet of Things (IoT) extends the concept of a digital world into the physical world through these autonomous systems on a chip (SoC).

In a ubiquitous object with a small-form-factor, power is a significant concern. Device lifetime is a key. The most power-hungry functions, such as wireless radio operation, could be scheduled or made dependent upon other conditions. Most of these objects are battery operated, some harvest energy from their environments, or combine the two modes in case of energy sparsity. SoC should be in low-power mode when sleeping and energy-efficient when active. Once the SoC wakes up, it uses multiple clock sources to drive the processing, the memory, the sensor interface and the wireless connectivity. There are currently no solutions available that would meet all these requirements. Surveys estimate that clocking accounts for one-third of SoC power dissipation.

In this context, the objective of this research is to propose design methodologies for frequency generation. As highlighted earlier, the problem is broad, and therefore we review the metrics proposed in the literature and identify the trade-offs and Figures-of-merit (FoM). When addressing the production of circuits operated at a moderate inversion level, the process variability degrades the correlation between silicon and simulation results; the divot corner transistor effect was mitigated and modelled. The proposed design strategy relies on the use of self-biased circuits which benefit from enhanced robustness to process, supply, and temperature variation; this was combined with astute use of inversion level properties as well as merging functions reusing the same transistor.

Moreover, the proposed methodology can further extend to other domains such as SoC security with a random number generator leveraging the phase noise, in SoC signal chain fast locking phase-locked loops, and in SoC power chains with a 60mV cold-start function from a thermoelectric generator. This dissertation, case-studies, and results validate the design guidelines from which we manufactured eleven circuits.

Keywords : Low-power electronics, Internet of Things, wireless sensor networks, CMOS integrated circuits, CMOS variability, reference circuits, clocks, phase locked loops, energy harvesting, microprocessor chips, SRAM.

Résumé

Aujourd'hui, l'industrie des semi-conducteurs alimente notre monde numérique avec de plus en plus de données provenant de l'électronique embarquée compacte qui surveille notre environnement et alimentent les analyses. L'interaction avec notre monde numérique se fait principalement par la connectivité à Internet. L'idée de l'Internet des objets (IoT) étend le concept de monde numérique au monde physique grâce à ces systèmes autonomes sur puce (SoC).
Les objets connectés ont un facteur de forme réduit, et leurs consommations énergétiques est une préoccupation importante. La durée de vie de l'appareil est une clé. Les fonctions les plus gourmandes en énergie, telles que le fonctionnement de la radio sans fil, peut être cadencée ou agir de manière subordonnées à d'autres conditions. La plupart de ces objets sont alimenté par des batteries, certains récupèrent de l'énergie de leur environnement ou combinent les deux modes. Les SoC doivent être en mode basse consommation pendant le sommeil et éco-énergétiques en activité. Une fois que le SoC se réveille, il utilise plusieurs sources d'horloge pour piloter le traitement, la mémoire, l'interface du capteur et la connectivité sans fil. Il n'y a actuellement aucune solution disponible qui répondrait à toutes ces exigences. Les études estiment que la génération de fréquence compte pour un tiers de la dissipation de puissance des SoC.
Dans ce contexte, l'objectif de ces travaux est de proposer des méthodologies de conception pour la génération de fréquence. Comme souligné précédemment, le problème est vaste et nous passons donc en revue les métriques proposées dans la littérature et identifions les compromis et les figures de mérite (FoM). En ce qui concerne la production de circuits fonctionnant à un niveau d'inversion modéré, la variabilité du processus dégrade la corrélation entre les performances mesurées sur silicium et les résultats de la simulation. L'effet du transistor de coin/divot a été atténué et modélisé. La stratégie de conception proposée repose sur l'utilisation de circuits auto-polarisés qui bénéficient d'une robustesse accrue en termes de sensibilité aux variation de tension, température et de process; cela a été combiné à une utilisation astucieuse des propriétés de niveau d'inversion ainsi qu'à la fusion de fonctions réutilisant le même transistor.
De plus, la méthodologie proposée peut s'étendre à d'autres domaines tels que la sécurité SoC avec un générateur de nombres aléatoires exploitant le bruit de phase, dans les boucles à verrouillage de phase de chaînes de signaux SoC et dans les chaînes de puissance SoC avec une fonction de démarrage sans autre source d'énergie depuis 60 mV à partir d'un générateur thermoélectrique. Cette thèse, utilise des études de cas dont les résultats valident les directives de conception à partir desquelles nous avons fabriqué onze circuits.

Mots clés : Electronique basse consommation, Internet des objets, réseaux de capteurs sans fil, circuits intégrés CMOS, variabilité CMOS, circuits de référence, horloges, boucles à verrouillage de phase, récupération d'énergie, puces de microprocesseur, SRAM.

Riassunto

Oggi, l'industria dei semiconduttori alimenta il nostro mondo digitale con sempre più dati provenienti da componenti elettronici integrati compatti che monitorano il nostro ambiente e alimentano l'analisi per l'azione. L'interazione con il nostro mondo digitale è per lo più raggiunta attraverso la connettività Internet. L'idea di Internet of Things (IoT) estende il concetto di un mondo digitale nel mondo fisico attraverso questi sistemi autonomi su un chip (SoC).
In un oggetto onnipresente con un fattore di forma ridotto, il potere è una preoccupazione significativa. La durata del dispositivo è una chiave. Le funzioni più potenti, come le operazioni radio wireless, potrebbero essere programmate o rese dipendenti da altre condizioni. La maggior parte di questi oggetti funziona a batteria, alcuni raccolgono energia dai loro ambienti o combinano le due modalità in caso di scarsità di energia. SoC dovrebbe essere in modalità a basso consumo quando è inattivo e a risparmio energetico quando è attivo. Una volta che il SoC si attiva, utilizza più fonti di clock per gestire l'elaborazione, la memoria, l'interfaccia del sensore e la connettività wireless. Non ci sono attualmente soluzioni disponibili che soddisfino tutti questi requisiti. I sondaggi stimano che il cronometraggio conti per un terzo della dissipazione di energia dei SoC.
In questo contesto, l'obiettivo di questa ricerca è di proporre metodologie di progettazione per la generazione di frequenze. Come evidenziato in precedenza, il problema è ampio e pertanto esaminiamo le metriche proposte in letteratura e identifichiamo i trade-off e le cifre di merito (FoM). Quando si affronta la produzione di circuiti azionati a un moderato livello di inversione, la variabilità del processo degrada la correlazione tra i risultati del silicio e della simulazione; l'effetto transistor dell'angolo del divot è stato mitigato e modellato. La strategia di progettazione proposta si basa sull'uso di circuiti autoassistiti che traggono beneficio da una maggiore robustezza alle variazioni di processo, fornitura e temperatura; questo è stato combinato con l'uso astuto delle proprietà del livello di inversione e le funzioni di fusione che riutilizzano lo stesso transistor.
Inoltre, la metodologia proposta può estendersi ulteriormente ad altri domini come la sicurezza SoC con un generatore di numeri casuali che sfrutta il rumore di fase, nella catena dei segnali SoC, anelli bloccati in fase di blocco, e nelle catene elettriche SoC con una funzione di avviamento a freddo da 60mV da un generatore termoelettrico. Questa dissertazione, casi-studio e risultati convalidano le linee guida progettuali da cui abbiamo prodotto undici circuiti.

Parole chiave : Elettronica a basso consumo, Internet of Things, reti di sensori, circuiti integrati CMOS, variabilità CMOS, circuiti di riferimento, orologi, loop di blocco di fase, recupero di energia, chip a microprocessore, SRAM.

Contents

Introduction

The Web also is known as the World Wide Web and what is today known as the Internet, has drastically changed our lives. The way we communicate, the way information is shared, and accessible. In 1989, Tim Berners-Lee and Robert Cailliau at the CERN near Geneva initiated a hypertext system, also known as the World Wide Web [1]. “Web” and “Internet” often used without much distinction. However, the two are not the same. The Internet is the system of interconnected devices networks at the global scale [2]. While the World Wide Web is a global collection of documents, it is also known as the concept of Linked-data. For a graphical clarification, the iconography of Figure 1 shows the different layers composing what we call “the internet” exposing the key milestones of each layer.

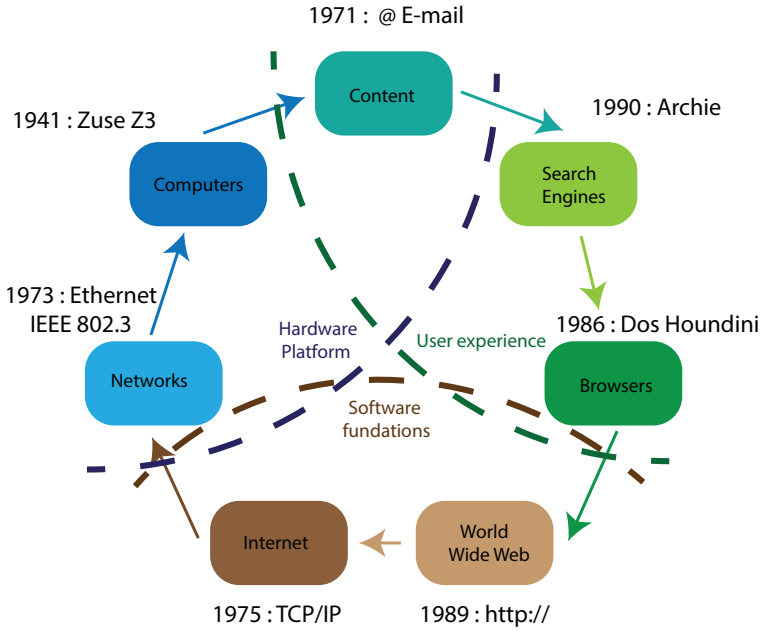


Figure 1: Internet, web, who’s who

Our user experience start-with a content that we could either provide or access, a usual content which existed on local networks for communication was the e-mail of Ray Tomlinson back in 1971 [3]. Ever since, we can access an incredible amount of media on the web, and use teleconferencing services. Then if we access either we got the link or we went through a

search engine with a milestone back in 1990 with Archie [4]. The graphical interface so called browser such as Dos Houdini [5] ease the access to users in general. The software foundations or the global lies world wide web as described back in 1989 by Tim Berners Lee and team at the CERN [1]. The Internet protocol, or Transmission Control Protocol/Internet Protocol TCP/IP was described in 1974 [2] using only four layer or the usual seventh of the "Open Systems Interconnection" or OSI model [6]. The TCP/IP rely and branch on networks more or less following the standard IEEE 802.3 for wire connectivity also known as Ethernet, and 802.x for many other standard access. The ever growing data transferred grew and still grows exponentially, and requires appropriate network communications to support its tremendous growth [7]. Figure 2 shows the traffic evolution in Petabytes per month since 1985. In 1990, 100GByte (GB) of data was transferred per day, whereas today, more than 20 years later, traffic has grown to 2 Exabytes (EB) per day, 20 million times more than 1990.

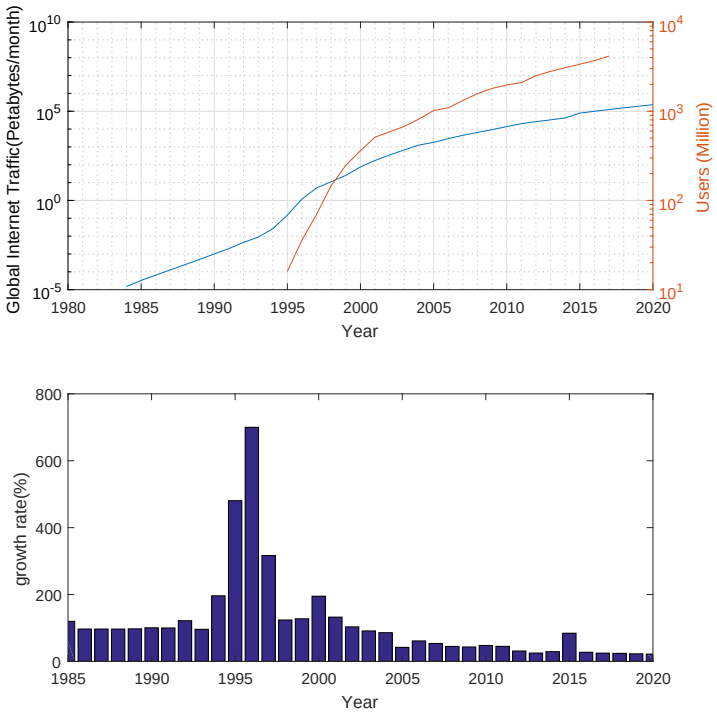


Figure 2: Total IP traffic and annual growth rate since 1985

The year 1995 was a year of high exposure for internet as a theme of the G7 meeting hosted by the European Commission in the European Parliament buildings in Brussels [8]. The momentum of the internet has kept its exponential increase with a growth rate of 20% ; this expanding trend is mainly attributed to the ubiquitous computing devices and machine to machine communications [7]. Adding the perspective of the increasing numbers of users which outreached more than half of the planet population pose some societal and environmental concerns.

The computing capability originally the Zuse had a tremendous evolution driving semiconductors devices toward ubiquitous computing. The Figure 3, provides a device evolution perspective. The transistor integration on as a monolithic device back in 1960, paved the way

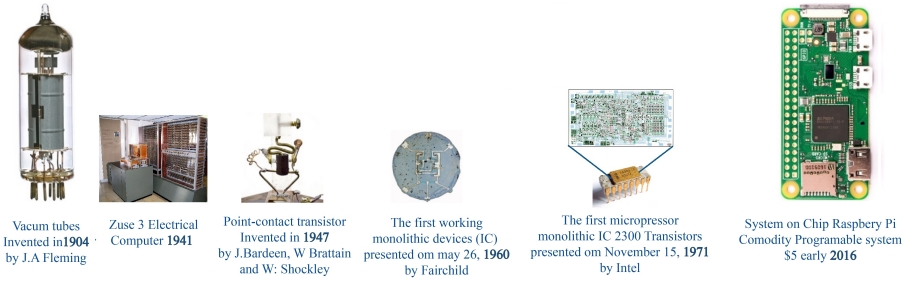
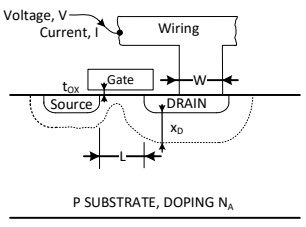


Figure 3: Devices evolution toward integrated system on chip

for the first commercial microprocessor [9]. The evolution of solid-state devices we really got in an era which enables such activities, computing devices capabilities of a personal computer except that it does not include a display such a device can run Unix and it got as affordable as 5$.

Observation of the device scaling from the Moore's law is the that the number of transistors in a dense integrated circuit doubles about every two years [10], Moore's prediction proved accurate for several decades, and has been used to guide long-term planning and to set targets for research and development in the semiconductor industry. The invention of dynamic random-access memory (DRAM) technology by Robert Dennard at IBM in 1967 [11], made it possible to fabricate single-transistor memory cells along with microprocessor paving the way for a further integration. The Figure 4 is extracted from [12]. It provides the impact of scaling on different parameters such as gate capacitance, supply voltage and current. It enables to calculate a delay time and power dissipation from a technology node to another. An important conclusion of the power consumption decreasing following the square law to the scaling factor. Another non proportional scaling is the power density which remain constant over the technology nodes. Delving into the device scaling number, the Figure 5, propose



Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, W, L	$\frac{1}{\lambda}$
Doping Concentration, N_A	λ
Voltage, V	$\frac{1}{\lambda}$
Current, I	$\frac{1}{\lambda}$
Capacitance, V	$\frac{1}{\lambda}$
Delay time/circuit, VC/I	$\frac{1}{\lambda}$
Power dissipation, VI	$\frac{1}{\lambda^2}$
Power density, VI/A	1

Figure 4: Devices classical scaling

as the sub-figure 5 (A) the original formulation of Moore law, which shows it's abscissa the technology node and years and the ordinate present the transistor per chip. Another curves propose the economic rationale of the cost per transistor which had made a tremendous drop as the number of transistor increase the price per transistor decrease. Since the two plots are in the logarithm scales and either strictly increasing or strictly decreasing. Therefore, for each new technology, the best number of components and the best price per component both develop exponentially there is a best number of components with the best per components price.

A further perspective in that figure is the diversification of computing platforms, ranging from the building-scale data centers to mm^3 computers. on the same figure (B), and (D), provides with a more detailed view on the so called Dennard scaling [12]. The sub-figure 5 (C), shows interesting number regarding the power density below 50 nm technology the plot is a projections at the maximum clock frequency, a proposed workaround is this multi-core parallelism. In (B), it shows static characteristics such as the supply voltage, and core transistors threshold voltage scaling along the nodes as well as the leakage current per gate length unit. Finally the sub figure (D), shows dynamic parameter scaling such as the propagation delay, and the subsequent energy dissipation. In general CMOS technology reached the point where technology

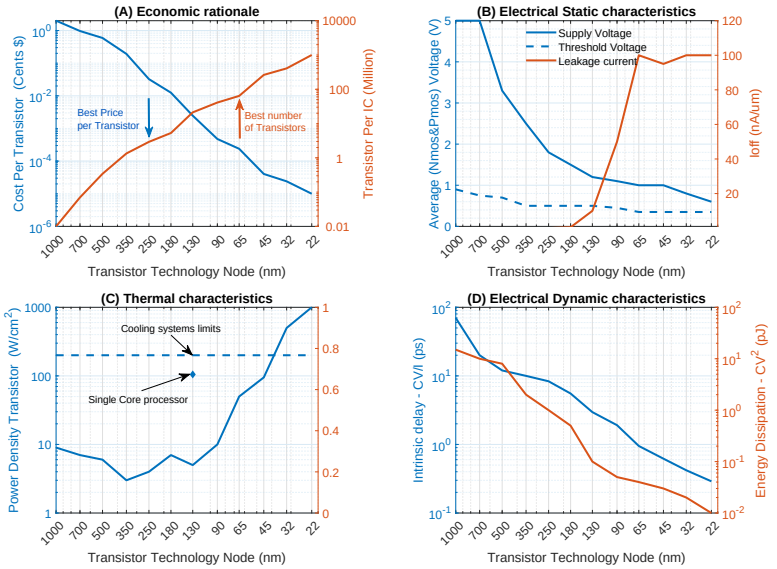


Figure 5: Scaling trends and Moore law

nodes could serve the needs, the evolution toward a three dimensional system in package using multiple die connecting each other are offering a lot of possibilities to integrate more functionality also known as the "more than Moore". The above data-set is mostly obtained extracting data from the public International Technology Road-map for Semiconductors (ITRS) data-sets and a few more publications [13, 14, 15, 16, 17, 18, 19, 20, 21, 22].

0.1 Internet of things design space and challenges

Internet of things on itself could be approached from many angles, the phrase "Internet of Things" was originally the title of a presentation of Kevin Ashton head of Auto-ID lab to Procter & Gamble (P&G) back in 1999 [23]. It is to some extents an extensive network of connected things. Where things could be computing devices, digital entities, mechanical machines, objects, or even people.

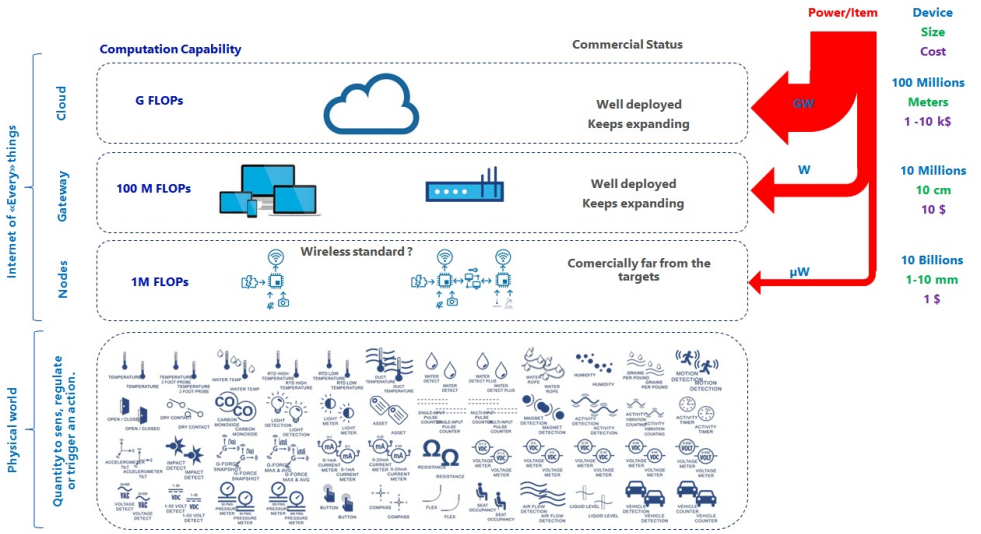


Figure 6: Top down requirements in the Internet of Things

The figure 6, propose a large variety of quantity that could be sensed, regulated or trigger an actuation. To do so, three to four layers are considered The Edge/Node, The gateways and the data-center/cloud. It could be regarded as between the gateway and the Cloud an additional layer named IT-Edge containing processing and analytics as most sensor nodes don't feature any. Order of magnitude is also provided regarding power per item, the number of devices, their size cost, and computational capability.

Data-centers have been designed to allow operational and capacity changes and expansions, and in conjunction with the fact that many of them run redundant power and cooling systems to provide better reliability, the energy consumption reported in 2012 worldwide is about 269 TeraWatts. Key players active in the IoT cloud Business have understood the need to harvest renewable energy and most have committed to do it. And some regulations [24, 25] are enforcing it.

When a network is considered, it implies an infrastructure which consumes energy. Therefore, this critical aspect linked to energy has to be considered at the system level. Managing power for the Internet of things is a challenging task because the devices must always be powered up and can be located anywhere, including harsh, remote environments. It is often impossible to run a wire to a device. CMOS technology is at the heart of many recent developments

in the design of integrated circuits. Moore's Law has served as the guiding principle for the semiconductor industry for several years. This trend is still moving forward as the state-of-the-art sub-100nm scaled CMOS technologies, for applications ranging from high-performance computing down to ultra-low-power mobile applications are developing. Circuit and system designers all around the globe are leveraging the large device density and processing power of modern technology toward new applications for more smart and interconnected world. System design with the system on chip (SoC) in the field of IoT, spans from data converters for sensor interfaces to radio and software applications. A small picture of the set of requirement is proposed in Figure 7, a single design point won't be enough to covers the span of applications.

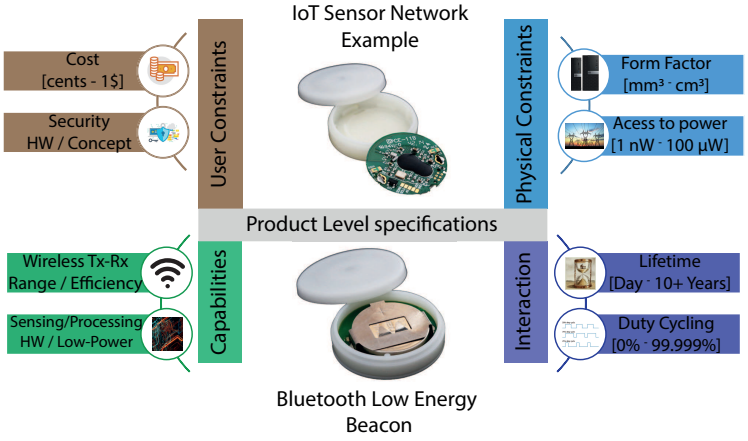


Figure 7: Challenges In the design of System On Chip for Internet of things

The set of challenges could be broader than shown in Figure 7, one can take the beacon as a System On Chip for Internet of things. Such technology is today at the edge of the proposed criterion's [26]. There is one particular observation which put into perspective two constraints being the processing capability and the access to power, and both scales together [27], given the level a performances obtained, one could think of a system which harvest its energy from the field where various sources are available as described per [28]. The paper includes the cost dimension, and denote that cheapest harvesting solution are incoming from the Radio-Frequency or magnetically coupled field, followed by the Photovoltaics (PV). The most potential if foreseen in the thermoelectric followed by the mechanical energy-harvesting, except that the maturity and cost of the part itself is not appropriate. Minimizing the need for raw material and thus the form factor is effective to cut down the cost of such energy-harvesting system. The lower end of the Figure 7 shows two set of constraints that are connected, that are the interaction and the capabilities of the system.

0.2 Thesis goal

Summarized in a single sentence the goal of this thesis would be: Find suitable frequencies generation architecture, design and implement of ultra-low-power and low voltage oscillator

and frequency synthesizers including power management extending the state of the art solutions for applications such as timekeeping, communication protocol clocking, and power conversion. These applications are taking place in most of the systems on chip nowadays.

Before, during and after the “Moore’s law” or “More Moore law” time remains an essential quantity. Alongside processor, memory/storage and analog/RF technologies, IC clocking count as the fourth dominant IC design technology. In the early years of this thesis, some work proposed industrial real-time-clock below 60 nA in its timekeeping mode. The Bluetooth® technology is mature and established short-range wireless connectivity to an internet gateway; the Bluetooth Special Interest Group report a 12% growth rate since 2010, and about one half the world population Bluetooth® parts. Indeed this wireless connectivity is one among many.

Nevertheless, it is one of the widely adopted duty-cycled radio, where a fully integrated sleep timer is used but needs to be as accurate as 500 ppm which is then over-precise in the context of EPCGen2 NFC RFID circuits. Foreseeing the explosion of connected devices with the Internet of Things where integrated circuit security had become one of the major concerns. A high entropy random number generator (RNGs) is an essential component of information security. They form the foundation for many cryptosystems. Jitter extraction based techniques got popular where a fully integrated oscillator sample a noisier one. Studying the phase noise bridge the accuracy performance and security requirements. The processing capability needs the system on a chip to provide flexible frequency generation as a commodity feature. The available solutions are power hungry and take a while to settle. Finally, the thermoelectric energy has a high energy density, but often the voltage is extremely low. Nevertheless, autonomous objects could be appealing if it opens a more moderate or zero maintenance need such as replacing a battery. The Internet of Things challenge the traditional design targets and require numerous functions operating at bottommost power and implement an energy-efficient mode so that in the long run, it keeps working without leaking information.

Challenges				Solu on	Implementa on	Chapter contribu on
Battery Life	Form Factor	Capabilities		Energy-Efficient operation (Vmin) coping with Variability	MCU core and Variability Monitoring	§2.2
Battery Life	Form Factor	Capabilities		Dual modes Active and Standby	Real-Time Clock	§3.2 + §3.4 + §4.4
Battery Life	Form Factor			Power management unit references	Bias references	§3.2 + §4.1
Battery Life	Form Factor	Capabilities		Dual modes Active and Standby	RC Timer	§3.2 + §3.3 + §4.2
Battery Life	Form Factor	Capabilities		Active-mode Processing clock flexibility	Phase Locked Loop	§4.5
Battery Life	Form Factor	Capabilities	Security	Energy Efficient prmitive for secured IC	Random Number Generator	§3.4 + §4.3
Battery Life				Ambiant energy extraction	Cold start Havester	§4.6

Figure 8: Covered challenges and contributions chapters

The Figure 8, shows in relation to the challenges presented in Figure 7, potential solutions where this had contributed with theoretical study, and potential implementations, and it is also pointed the chapter where this was addressed.

0.3 Thesis organization

The purpose of this thesis is to provide suitable frequencies generation architecture, which can easily be integrated into the IC design flow yet ultra-low-power and low voltage frequency

reference or flexible generator. In which, power management is a key concern for applications such as timekeeping, communication protocol clocking, and power conversion. Apart from the introduction, this dissertation is composed of an additional five chapters dedicated to the design analysis and methodology for clocking problems into System On Chip ICs with the following contributions:

• Chapter 1, provides the basis for comparison of fully integrated frequency reference given an application, it is proposed in a survey format. The same chapter also aims at providing an overview of the power management concerns of systems on a chip. The chapter includes some general aspects on the energy storage, a short par and the choice of the power conditioner.

• Chapter 2, introduce the foundation of our design methodology the physical based compact transistor models, which accurately represents our transistors along the design process. Variability of the divot transistor turns out to be essential, a device characterization is proposed and an applicable model exposed. Some techniques to mitigate the effect were proposed and evaluated. Besides the edge transistor and it's mismatch impact on the circuit, implementing high absolute value of the resistor is a crucial problem of low power design, we had put our focus on a few examples.

• Chapter 3, Propose design guidelines for self-biased error amplifier that could be used to generate frequency reference such as fully integrated RC and a resonator based. We reviewed a structure initially used in current reference, which variability was considered in Chapter 2. This leads us in proposing a sizing methodology that includes variability in the design target. Then we had built on top of the positive feedback adaptive biasing structure a self-biased amplifier and design guideline as a basis for fully integrated oscillator that which themselves are detailed afterward. The resonator based pierce oscillator is then reviewed, and a self-biased structure was proposed extending the common design steps that are included. Both circuits phase-noise analysis were somewhat simplified. Finally, after the need for improving the phase-noise, another set of function could require the opposite, and we proposed an entropy model for our random number generator. The design step is further presented in chapter 4 where we had particularly confirmed our guidelines with a case study and silicon results.

• Chapter 4, shows our cases studies that start with one example of the self-bias circuit the current reference, where we had reviewed available principle and proposed as a further option. After reviewing the static current reference, we had proposed one example of fully integrated and self-biased frequency reference. The phase noise analysis bridge our accurate timer case study with our random generator followed by the crystal (High-Q) based self-biased frequency references. We then combine our crystal oscillator reference and the fully integrated frequency reference to generate a flexible frequency that has a fast settling, to limit the sleep to active power consumption. The last case study covers the thermoelectric energy harvesting where the cold-start voltage is a key issue given that the thermoelectric generator (TEG) can hardly generate.

• Chapter 5, draws conclusions highlighting the contributions of this work and suggesting possible solutions that could be implemented in future works.

Overview

The unit for time is internationally the seconds. Since 1967, the second was defined by the cesium $\left({}^{133}Cs\right)$ atomic resonance which frequency reference is 9.192631770 GHz or transition between the two hyperfine levels of the ground state of the atom. This suggest that the evolution of the energy level of a system will always be downwards. Therefore at least one energy tank is required to define a time reference. Before and after the definition of the second, the pace of human activity has driven the need for precise time reference, whether it was for scheduling activities, for navigation [29] in which time synchronization to a reference time matters. Beyond these motivations, the clocks as we know are in fact including a frequency Standard also called frequency reference and a counting mechanism defining a local time. The specification and characterization of clocks and oscillators most of the standards focus on the oscillator stability metrics [30], [31] and measurements methods [32]. Systems On Chip (SoC) and their clocking is a crucial issue; time is one more input-output interface of our digital revolution [33]. In the context of the Internet of things, emerging from the mid-1990s with the smart-dust Integrated circuits [34]a fabulous effort on the processor, storage, analog, and Radio-Frequency (RF) technologies in this prospect of connecting every device to a network has been achieved.

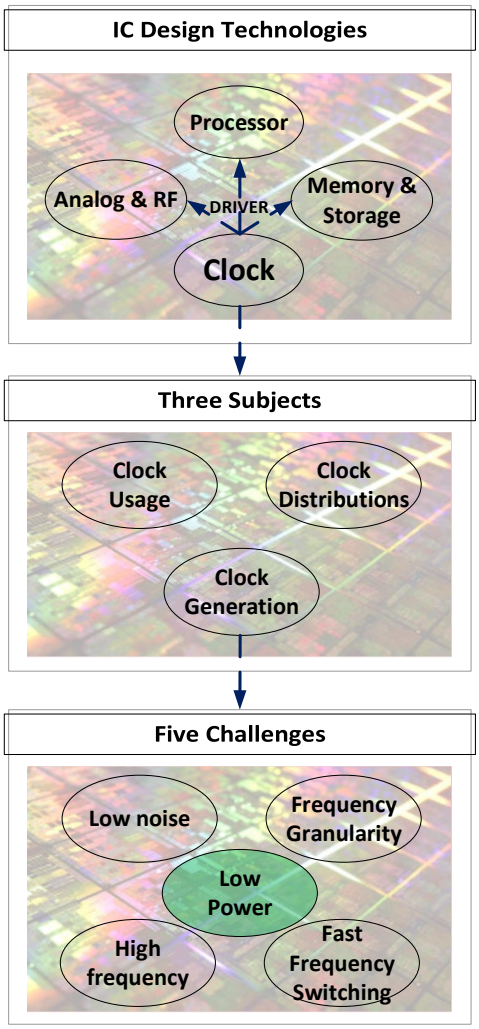


Figure 1.1: From the four Major IC design technologies to the challenges in clock generation

Among the four major IC design technologies depicted in the figure 1.1, clock technology is the driver of the three others. The contribution of Micro Electro Mechanical System (MEMS) used as resonator proposed a qualitative assessment [35], further continued in [36] and [37]. The figure 1.2 propose a radar plot as a summary of these statements.

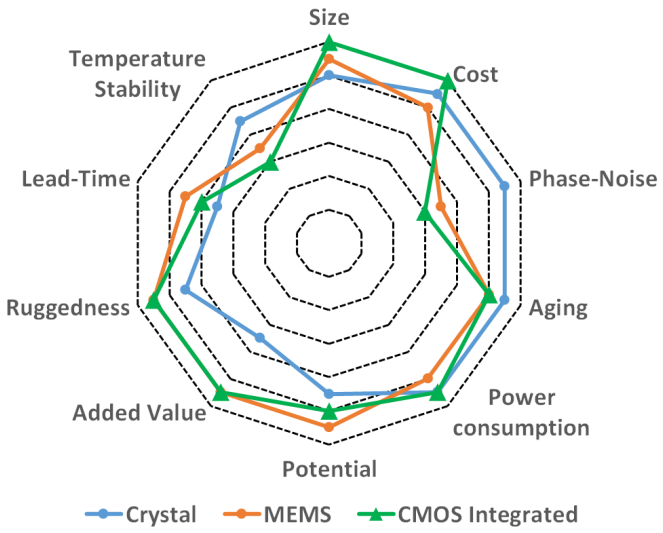


Figure 1.2: Qualitative assesment

As shown, the crystal oscillator (XO) typically achieve low-noise and low-power. Emerging technologies are generally inferior along these dimensions, but offer other benefits over quartz including smaller size and shorter lead-times. In the subject of clock generation the literature proposed a focus on fully integrated references, at a fixed frequency with constraints on power budget in the last decades, the application level also relaxed the requirements on clock technology.

1.1 Use case of frequency generation

The popular swarm model [38] of Jan Rabaey lightened this idea of wireless sensor nodes having an ultra low-power and thus slightly relaxed radio specifications. Since then, different wireless communication systems showing relaxed constraints on clocking techniques in relations to a different set of applications [39, 37]. The clock accuracy or directly the long-term frequency stability remains one of the central figure for most of the application. The increasing demand for high speed data transmission motivates the Figure 1.3 presenting the constraints on accuracy and data-rates.

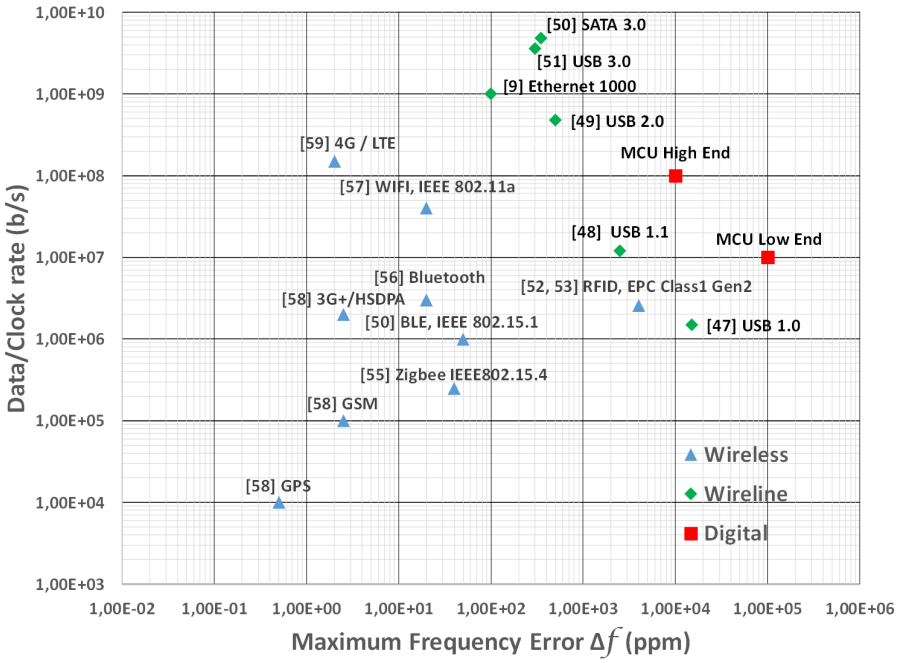


Figure 1.3: Clocking in digital, wireline and wireless standards requirements

Considering the case of digital micro- controller systems, an accuracy of around 1 % is in many cases sufficient. Some datasheets even report accuracies lower than ±10%, to some extent these precision are driven by the serial links to peripherals. In regards to communication systems, a higher accuracy is required. For low-speed USB 1.0, an accuracy of ±15 000 ppm and 1.1 or fully speed it gets to ± 2500 ppm [40, 41] the High-Speed USB 2.0 requires ± 500 ppm [42]. Another a few buses are proposing sub Giga-Hertz wireline communication requires even higher accuracies: the Serial-ATA [43] requires an accuracy of ± 350 ppm, the USB 3.0 requires ± 300 ppm [44], and the Ethernet require an enhanced accuracy of ± 100 ppm [36]. Meanwhile, the clock for the wireless interface requires a tighter clock accuracy specifications. The tight clock accuracy has mainly to do with the fact that the signal strength is much lower and that a lot of unwanted interferences are present. Accurate timing of the carrier frequency is of great importance in the case of narrow communication channels. An illustration of the consequence of such inaccuracy on the TX signal is proposed in Figure 1.4, it relates to the risk that receiver won't receive the signal in the receiver filter band correctly.

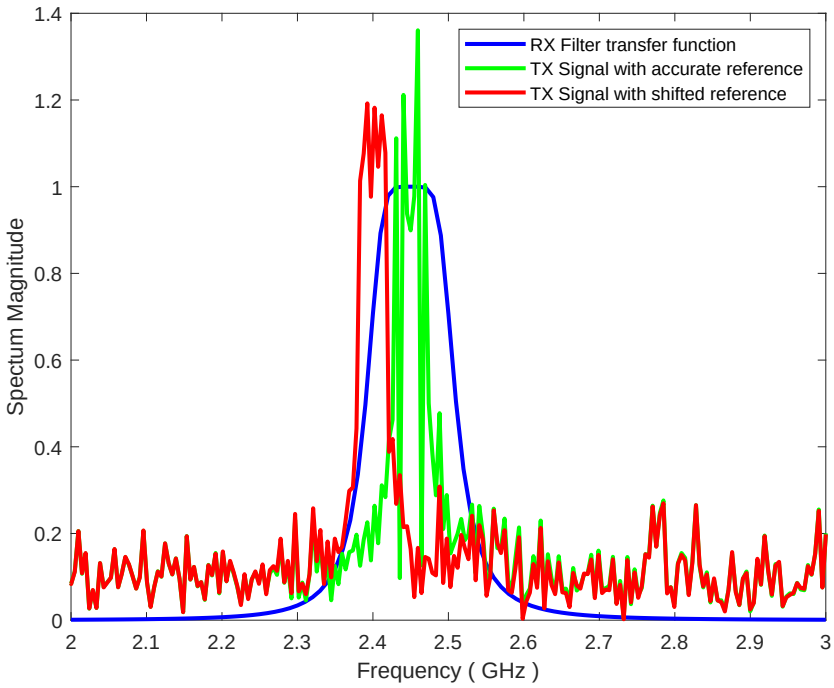


Figure 1.4: Effect of the carrier inaccuracy in a wireless standards requirements

Among the various wireless communication, the Radio Frequency IDentification (RFID) is quite an exception as shown in [45, 46] ± 3000 ppm would sustain a good communication. Already the Bluetooth low energy wireless communication layer [47] requires ± 50 ppm. for a lower data such as Zigbee the accuracy constraint gets to ± 40 ppm [48], and drop down to ± 20 ppm for a Bluetooth communication [49] as well as Wifi [50]. Our mobile handset application applications initially specified at ±2.5 ppm in [51] had slightly shifted their accuracy needs to ±1.5µs over 24hours [52] so a ±2.0 ppm. The ultimate reference accuracy constraints of ± 0.5 ppm remains as in [51] the GPS applications.

1.2 Oscillator metrics and benchmark

This section split into two categories, from more generic metrics that apply to any CMOS reference and those that are particular to CMOS Frequency reference. CMOS circuits itself classify with some parameters that are quite general. When exposed to environmental conditions semiconductor are also known as a sensitive material, a widespread use case is the temperature sensor, and therefore it raises the question of operating range and sensitivity. Similarly, some technology nodes handle relatively high supply voltage often used to drive actuator. Similarly, the CMOS devices have their breakdown voltage and are sensitivity to supply voltage. The effect such as piezoelectric, acceleration, irradiations properties, are not widely reported in light of the author background. Although when going to handheld equipment this could be of further research interest.

1.2.1 Metrics applicable to any CMOS references

Essentially benchmarking in CMOS comes along with the process scaling and the dramatic increase of developing an own foundry **Process Node** cost [53]. The CMOS processes are characterized by their minimum gate channel length other optional flavors like high voltage, low-leakage. Most of the semiconductor company turn from their process node to eventually use an external semiconductor manufacturer (foundry); this is why it comes into place the "**PPAC**" analysis; it stands for **Performance** which is the underlying reason to go for an integrated circuit. **Power consumption** which could be another one in the case of battery operated systems the Energy would replace such a metric. The **area** also called die size when it gets to complete integrated circuit. Finally, the **Cost** which is a very secretive metrics. These numbers were the primary variable of interest to any rational semiconductor company management for a make or buy decision. Essentially the Cost aspect is usually direct combination of the Process Node and the Area it takes to integrate the function. Somehow this cost notion gets hidden, a practical element of IC based on the direct cost of one Die directly relates to the die area as a large integrated circuit reduce the number of die per wafer $\left(N_{\frac{Die}{Wafer}}\right)$ as per Equation 1.1.

$$Die_{cost} = \frac{Wafer_{cost}}{N_{\frac{Die}{Wafer}} \cdot Die_{yeild}} \tag{1.1}$$

A further consideration for the final IC cost must be taken into accounts such as test and package cost and yield for example, and these could rule the rule, it is merely a common sense rule which justifies this for benchmarking fairly. A functional diagram description is proposed in Figure 1.5.

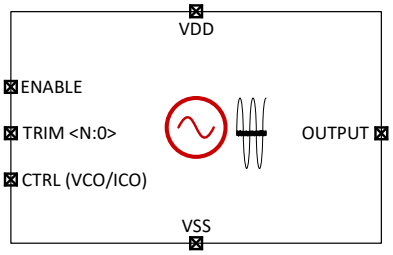


Figure 1.5: Functional description

Any fully integrated oscillator must get a supply voltage (VDD) pin and the ground pin (VSS) and the clock signal output pin (OUTPUT) this is going to be our considered **performance**. Every Integrated Circuit are processed over more than 100 steps, in which every step introduce their variability to the final performance. These worst case are also known as process corners. When addressing the CMOS reference whether it is a voltage, current, time or any reference, engineering nonidealities could be faced with both architectural tricks and on the top of that

implement, some are trimming such that the reference absolute value is well under control; this is proposed using some digital input (TRIM<N:0>) this could also be an analog signal. Finally, sometimes the oscillators are used in phase locked loops, or frequency locked loop and thus needs a control pin here named (CTRL). The supply rail itself define a first exciting metric which is the so-called **operating supply range** which tells us that the bloc is functional or in another word providing a clock or other reference. A further metrics called **supply voltage sensitivity**(ΔR_V) should then be mentioned, given a clear application or standard such as in the case of telecommunications the operating supply range is self-sufficient if the deviation of the reference value exceeds the tolerance it is then ground for considering the upper or lower bound. The usual definition of the sensitivity is given as per equation 1.2.

$$\Delta R_V = \max\left(\frac{\partial R}{\partial V}\right) \tag{1.2}$$

Another variable of interest to the reference is the behavior with temperature; the integrated circuit, typically exposed to environmental conditions such as temperature. The industrial range spans from -40°C to 85°C, while some consumer electronics would often require a lower standard and automotive or space higher. This call into existence **operating temperature range,** in which the reference will not collapse. Another quality assessment related to the temperature input stimuli is the **temperature sensitivity** (ΔR_T) is given by equation 1.3.

$$\Delta R_T = \max\left(\frac{\partial R}{\partial T}\right) \tag{1.3}$$

Note that as most of the local sensitivity methods, this involves taking the partial derivative of the output reference R concerning an input factor. Such local methods do not attempt to fully explore the input space since its one variable at a time. The Figure 1.6, proposes some common reference performance dependency observed as a function of the input stimulus. It's often encountered to see linear sensitivity which argues in the sense of reporting a single number being the slope of that linear curve. Nevertheless, other behaviors are met such as a bell shape or a reasonably close to zero variation coefficient around the nominal operating point, or a compound of this phenomenon. The reference variation is in part per million, percentage or equivalent unit.

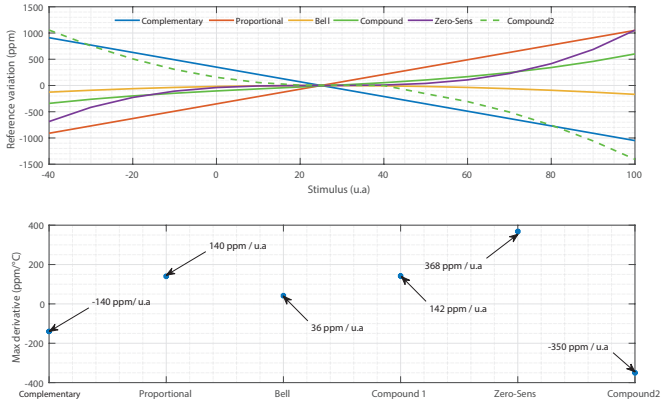


Figure 1.6: Local Sensitivities curvature the maximum of the first derivative and eventual pitfall

The underlying reason for reporting the maximum of the derivative comes across model abstraction principles when indicating a single number sensitive to a given input variable; the proportionality makes it easy to estimate the deviation. Such as per equation 1.4.

$$\Delta R_x = \max\left(\frac{\partial R}{\partial x}\right) \cdot x + R_0 \tag{1.4}$$

The input-sensitive variable considered is x. When taking a second look at the different curvatures, there is some physical observation that shows not to be linear and, therefore the equation 1.4 is not valid anymore. The compound behaviors which usually appears when some compensation strategy is applied, there could be a pitfall. Observing the green dashed line we could see a larger reference variation excursion than the purple curve corresponding to a so-called Zero-Sens curvature (due to its nearly flat behavior around the expected operating point). Nevertheless, the temperature coefficient is smaller than the so-called Zero-Sens curvature, a further observation by plugin the numbers in the equation 1.4, leads to ±26250 ppm of variation excursion from the reference which was ideally 0ppm, while the actual curvature shows ±1250 ppm. This call into existence the need for either providing the **curvature equation** and or the **boundaries**. The above definitions essentially apply to any circuit considering the standard environmental sensitivities such as Voltage and Temperature. A single-point trim is usually allowed to reduce the process spread; this covers the so-called PVT (Process, Voltage, Temperature) aspects. The particular parameter of a reference oscillator and the introduction of figures of merit is discussed in the next section.

1.2.2 Metrics and figure of merit particular to frequency references

This section introduces first the theoretical background to differentiate a harmonic oscillator and a relaxation oscillator, moving on with an abstract functional electrical schematic of both

oscillators, introducing then the notion of the quality factor of the tank. The representation of the signal enable a discussion on the stability of the frequency reference and finally address some possible figures of merit to compare them.

Harmonic, relaxation oscillator as Frequency reference

The differentiation between Harmonic and relaxation Oscillator requires to review the theory of the van der Pol Oscillator. From the early study on the concept of electrical oscillator [54] Balthasar Van Der Pol, proposed an equation describing self-sustaining oscillations in which energy is fed into small oscillations and removed from large oscillations given by equation 1.5.

$$\frac{\partial^2 y}{\partial^2 t} - \mu \cdot \frac{\partial y}{\partial t} \cdot \left(1 - y^2\right) + y = 0 \tag{1.5}$$

The parameter μ, is a scalar parameter indicating the nonlinearity and the strength of the damping. When $\mu = 0$, the equation reduces to the equation of simple harmonic motion such as suggest equation 1.6.

$$\frac{\partial^2 y}{\partial^2 t} - y = 0 \tag{1.6}$$

An illustration of the effect of the nonlinearity and the strength of the damping coefficient proposed for $\mu = 0.1$, and for $\mu = 5$, in Figure 1.7.

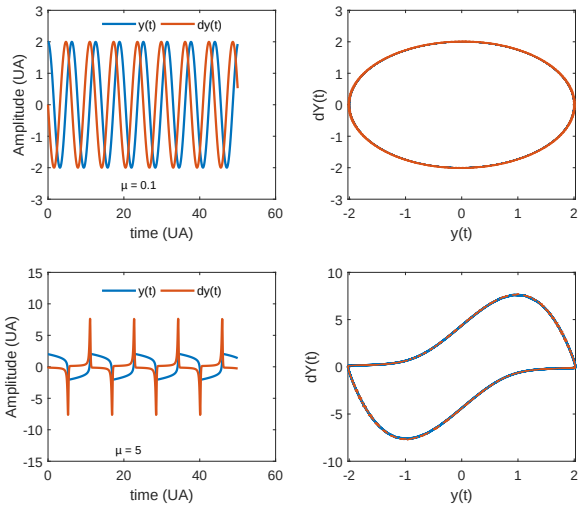


Figure 1.7: Time representation and Phase portraits of different van der Pol oscillator for $\mu = 0.1$ and $\mu = 5$

For low strength of the damping coefficient μ, the two state variables are continuously chang-

ing (energy exchange) as shown on the upper part of Figure 1.7. However for higher values of the damping coefficient μ, as reported on the lower part of Figure 1.7, the oscillator will move from a sine-wave (soft) behavior, where linear analysis hold. Towards a nonlinear or switched behavior oscillator. The terminology relaxation oscillator was used in [54] by Balthasar van der Pol to express the period of 'building up a tension in the continuous state and then suddenly relax by switching the discrete state' describe that switched oscillator. Linear analysis such as cannot using transfer functions cannot describe relaxation oscillators. It is therefore delicate to provide a mathematical model of the relaxation oscillators behavior. Figure 1.8 proposes an Insight on the implementation of a conventional fully integrated relaxation oscillator.

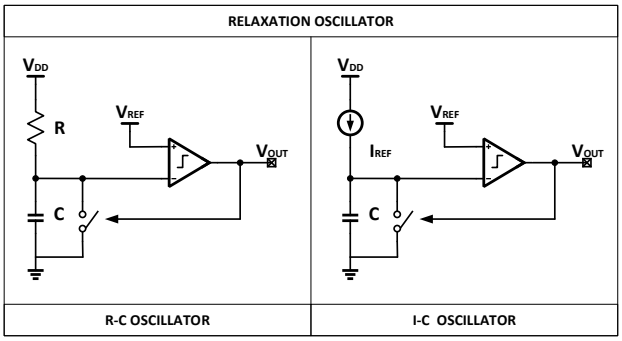


Figure 1.8: Abstract implementation of the relaxation oscillator using capacitive reservoir

Besides these abstract view on the implementation of relaxation oscillator numerous strategy to cope with non-ideality of each compound (resistor, capacitor, switch, voltage or current reference, or the comparator) get their contribution to the performance improvement or degradation. Some prior publication address the trade-off, [55] at block level in such implementation. A specific study on the impact of the comparator offset is proposed in [56] and [57]. Meanwhile, an additional control loop was introduced in [58], and a general formulation of the oscillator phase noise is addressed in [59]. Nevertheless, a relaxation oscillator can also use a resonator tank as shown in [60] and another abstract implementation as shown in Figure 1.9.

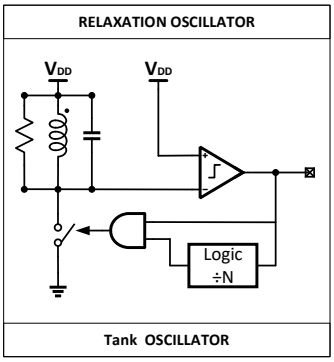


Figure 1.9: Abstract implementation of the relaxation oscillator using LC Tank

Such proposal paved the way for other pulsed oscillator topology and their analysis. The crystal resonator had the benefit of drastic current consumption savings [61, 62, 63]. Mentioning resonators, the **Quality factor** or **Q** factor is a parameter to characterize a two-pole system as shown in [37]. In the specific case of a resonator, gives us a relation as per equation 1.7. This equation relates the energy storage and the loss in a cycle of oscillation. This would apply to a simple reservoir either a coil or a capacitor.

$$Q = 2 \cdot \pi \cdot \frac{E_{STORED}}{E_{LOSS/CYCLE}} \tag{1.7}$$

A focus on the parallel resonant tank is proposed although several transformations can be applied to it to take into account another resonant mode. The Figure 1.10, describes the considered tank exited by a sine-wave as well as an amplifier and the tank as the feedback network.

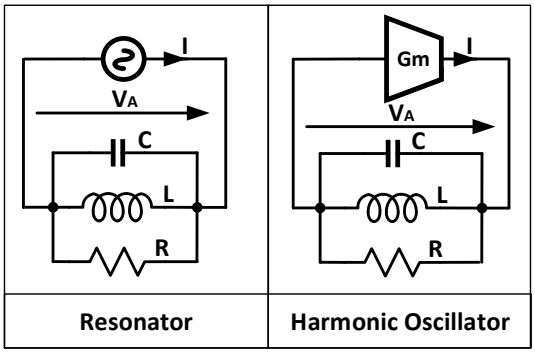


Figure 1.10: Diagram of an excited by a sine-wave resonator and a harmonic oscillator

Applying a sine-wave to the resonator the definition of equation 1.7, apply such as presented

in (1.8) ; which shows the relation between the electrical components and the quality factor.

$$Q = 2 \cdot \pi \cdot \frac{{}_0\int^{\frac{T}{4}} P(t) \cdot \partial t}{4 \cdot {}_0\int^{\frac{T}{4}} \frac{V_A^2}{R} \cdot \partial t} = 2 \cdot \pi \cdot \frac{\frac{C \cdot V_A^2}{2}}{\frac{V_A^2 \cdot \pi}{R \cdot \frac{1}{\sqrt{L \cdot C}}}} = R\sqrt{\frac{C}{L}} \tag{1.8}$$

For a further understanding of the quality factor, the following time domain differential equation (1.9) describes the evolution of the voltage v(t) over the capacitor over time. The canonical form of a passive two poles circuit was used for generalization.

$$\frac{\partial^2 v(t)}{\partial^2 t} + \frac{\partial v(t)}{\partial t} \cdot \omega_n \cdot \frac{1}{Q} + v(t) \cdot \omega_n^2 = 0 \tag{1.9}$$

The general solution to that differential equations is given by (1.10) :

$$v(t) = A \cdot e^{-\frac{\omega_n \cdot t}{2 \cdot Q}} \cdot e^{\frac{\sqrt{1-4 \cdot Q^2}}{2 \cdot Q} \cdot \omega_n \cdot t} + B \cdot e^{-\frac{\omega_n \cdot t}{2 \cdot Q}} \cdot e^{-\frac{\sqrt{1-4 \cdot Q^2}}{2 \cdot Q} \cdot \omega_n \cdot t} \tag{1.10}$$

As (1.10) is the general solution the constants A and B are the initial conditions of the network, those needs to be found in particular circuits topologies. Therefore a resonant second order network is proven to be entirely characterized by its Quality factor Q and natural frequency ω_n. The particular value of quality factor $Q = \frac{1}{2}$, involves a critically damped system, in other word, there will be no oscillations. As the Quality factor embed in one number the filtering characteristics and active dissipation it would as a consequence provide a good insight on the noise generation [64]. A negative Quality factor cannot exist for a passive resonator however it is theoretically applicable to both positive and negative sign. A higher quality factor than half would make an oscillator, but the higher, the better. Therefore if the oscillator implies a tank, it's a per-requisite to evaluate and provide the quality factor to the reader. When adding the active circuit, the differential equations are not the same for the parallel (1.11)

$$\frac{\partial^2 v(t)}{\partial^2 t} + \frac{\partial v(t)}{\partial t} \cdot \omega_n \cdot \frac{1}{Q_G} + v(t) \cdot \omega_n^2 = 0 \tag{1.11}$$

Solved as (1.12):

$$v(t) = A \cdot e^{-\frac{\omega_n \cdot t}{2 \cdot Q_G}} \cdot e^{\frac{\sqrt{1-4 \cdot Q_G^2}}{2 \cdot Q_G} \cdot \omega_n \cdot t} + B \cdot e^{-\frac{\omega_n \cdot t}{2 \cdot Q_G}} \cdot e^{-\frac{\sqrt{1-4 \cdot Q_G^2}}{2 \cdot Q_G} \cdot \omega_n \cdot t} \tag{1.12}$$

And the series network (1.13).

$$\frac{\partial^2 v(t)}{\partial^2 t} + \frac{\partial v(t)}{\partial t} \cdot \omega_n \cdot \frac{1}{Q_G} + v(t) \cdot \omega_n^2 \cdot \left(1 - \frac{1}{Q^2} + \frac{1}{Q \cdot Q_G}\right) = 0 \tag{1.13}$$

Solved as (1.14):

$$v(t) = A \cdot e^{-\frac{\omega_n \cdot t}{2 \cdot Q_G}} \cdot e^{\frac{\sqrt{1-4 \cdot Q_G^2 \cdot \left(1-\frac{1}{Q^2}+\frac{1}{Q \cdot Q_G}\right)}}{2 \cdot Q_G} \cdot \omega_n \cdot t} + B \cdot e^{-\frac{\omega_n \cdot t}{2 \cdot Q_G}} \cdot e^{-\frac{\sqrt{1-4 \cdot Q_G^2 \cdot \left(1-\frac{1}{Q^2}+\frac{1}{Q \cdot Q_G}\right)}}{2 \cdot Q_G} \cdot \omega_n \cdot t} \tag{1.14}$$

To obtain these reasonably simple expression, a workaround is to use the generalized quality factor (1.15).

$$Q_G = \left(\frac{1}{Q} - \sqrt{\frac{L}{C}} \cdot G\right)^{-1} \tag{1.15}$$

This expression does not include the loading effects which usually degrade the quality factor. Nevertheless consists of the impact of the amplifier where $G = \frac{V_A}{I}$ defines the transconductance. A generic solution of the above is rather straightforward, more important that some conclusions on the interest of this analysis the generalized quality factor Q_G, can be negative. The most important observation is that the instantaneous oscillation period depends on the stability of the amplitude. This highlight the motivation for an amplitude regulation mechanism in the harmonic oscillator that ensures stable amplitude of oscillation. The description of an electrical signal requires two variables, charges either seen from the flux (current) or potential (voltage) perspective and time. Fundamental components namely resistor, capacitor, and inductor form the building blocks of the entire electronic world. Their response to a stimulant depends on the number of charges involved in the process; this enables us to use that property for quantification and representation as an **Amplitude** for instance. The same components do not naturally recognize the concept of time but respect the physical principle of causality, and their inertia to a change in a flow or a potential of charge enables us to establish an order of sequence. The first harmonic of an oscillator expresses as (1.16),

$$v(t) = A(t) \cdot \sin\left(\phi(t)\right) \tag{1.16}$$

Where $A(t)$ is the instantaneous **Amplitude** of the oscillator signal and, $\phi(t)$ is the instantaneous phase of the oscillator signal. However, the oscillator is not necessarily providing a sinusoidal function but a periodic function with period $2 \cdot \pi$. The instantaneous **angular frequency** $\omega(t)$is given by the time derivative of the instantaneous phase $\omega(t) = \frac{\partial \phi(t)}{\partial t}$ and express in $\frac{rad}{sec}$ In an ideal non-modulated oscillator, the angular frequency is a constant $\omega_0 = 2 \cdot \pi \cdot f_0$ in which appears the **Nominal frequency** (f_0) of the oscillator. In a practical oscillator, fluctuation occurs in the evolution of phase and therefore in the nominal frequency includes both random and deterministic components. Separation of these components are usually made in the expression of the instantaneous phase $\phi(t)$ in (1.17), is implementing the constant mean angular frequency ω_0, the random phase fluctuation $\varphi(t)$, and systematic and

deterministic variations in the phase function $\psi(t)$.

$$\phi(t) = \omega_0 \cdot t + \varphi(t) + \psi(t) \tag{1.17}$$

The phase time function $T(t)$ that gives the evolution of time given by a clock that is run by the oscillator.

$$T(t) = t + \frac{\varphi(t)}{\omega_0} + \frac{\psi(t)}{\omega_0} \tag{1.18}$$

When neglecting the systematic and deterministic phase variations, the random instantaneous phase-time fluctuations reduces, the quantity remains unchanged under frequency multiplication and division of an oscillator output signal. It allows for easier comparison of frequency stability among oscillators having different nominal frequencies, this is often called the **Instantaneous Fractional Frequency** (1.19)**.**

$$\frac{\partial T(t)}{\partial t}_{\frac{\psi(t)}{\omega_0}=0} = \frac{\frac{\partial \varphi(t)}{\partial t}}{\omega_0} = \frac{\triangle f(t)}{f_0} \tag{1.19}$$

It can be thought of as the time difference between the corresponding zero-crossings of an oscillator, affected by phase fluctuation also known as **Jitter**, and those zero crossing would be compared with those of an ideal oscillator running at the same nominal frequency. An illustration of the jitter is proposed in Figure 1.11. The first waveform represent the Jitter-Free clock and the second waveform include Jitter. It is observed that the reference period could vary and **Cycle-To-Cycle Jitter** is a measure of the distance from the ideal period to the actual period, when averaging to N consecutive period, it define the **Long Term Jitter** or **Accumulated Jitter**, this average

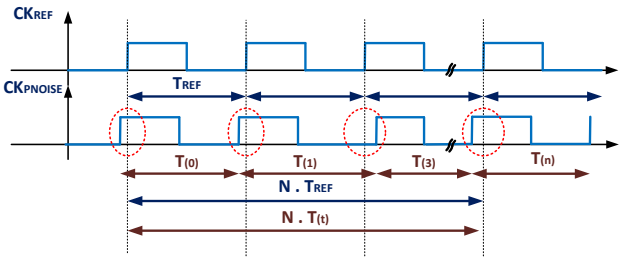


Figure 1.11: Jitter Definitions

Industry standard such as Joint Electron Device Engineering Council (JEDC) proposed the JEDS65B [31], it defines time domain measurement of the cycle to cycle jitter. The recommended measurement is a sample of 10 000 cycle on either rising or falling edge including

of consecutive cycle (from T[0] to T[10 000]), When observing the Figure 1.11, the proposed signals are digital pulsed wave and therefore embed a larger spectral content than the assumption on the fundamental which would be for a single sinus wave. When a signal is in the form of large signal pulse it is usually defined the Slew-Rate, as the change of voltage or current, or any other electrical quantity, per unit of time $SR = \frac{\partial q}{\partial t}$, as shown in Figure 1.12.

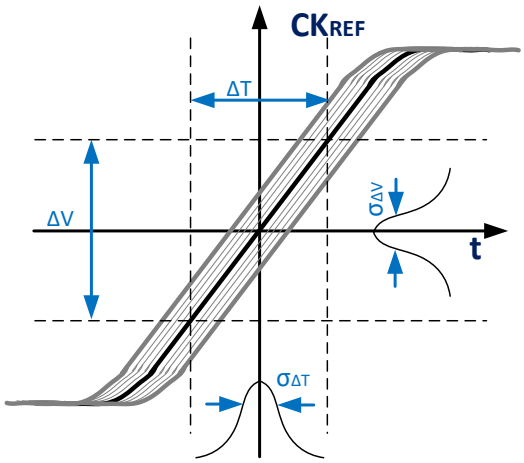


Figure 1.12: Relation of large signal and threshold crossing displacement.

In a systems where signals are continuous, an event is usually defined as a signal crossing a threshold in a particular direction. This recall the earlier zero crossing definition on the fundamental. The threshold crossings of the noiseless periodic signal are precisely evenly spaced. However, accounting for the noise each threshold crossing are slightly displaced and as consequence it converts additive noise into synchronous jitter as in equation 1.20.

$$J_c = \frac{\sigma_{qn}}{SR} \tag{1.20}$$

This connect the fact that amount in time (seconds) is determined by the amplitude of the noise and the slew-rate. Similar conclusions were proposed in [65]. In order to facilitate the theoretical modeling of oscillator phase noise, it is convenient to assume stationarity of the signal. Stationarity is such a mathematical property meaning that statistical parameters are time-independent. However, problems arise as the phase noise processes are strictly speaking non-stationary. Several IEEE standard defines the consideration given an application : [66, 67, 68, 69, 70, 71, 72, 73, 32, 74, 75, 76], the current project P2414 - IEEE Standard for Jitter and Phase Noise is trying to propose a harmonized but consistent approach, which is a real challenge in itself. The Allan variance is an IEEE recommended time-domain measure of frequency stability [77]. It offers a solution to overcome some of the problems involved in the use of the “classical” variance. The Allan variance the average is taken over an infinite number

of squared differences of two adjacent samples, whereas the classical variance, the average is taken over an infinite number of squared values of adjacent samples and therefore could diverge. The Allan Variance this express in (1.21), where $\tau = t_{i+1} - t_i$, which means that there is no dead time between the subsequent samples, and therefore the correlation between the subsequent samples is canceled.

$$ADEV = \frac{1}{2} \cdot E \left[\frac{1}{\tau} \cdot \int_{t_i - \frac{\tau}{2}}^{t_i + \frac{\tau}{2}} \frac{\triangle f(t_{i+1})}{f_0} \cdot \partial T - \left(\frac{1}{\tau} \cdot \int_{t_i - \frac{\tau}{2}}^{t_i + \frac{\tau}{2}} \frac{\triangle f(t_i)}{f_0} \cdot \partial T \right)^2 \right] \tag{1.21}$$

A typical representation is proposed in Figure 1.13. The blue points represents actual measurement of an actual fully-integrated oscillator, the usual averaging time should be selected in the range of $100\mu s$ to $100s$, objectively colored noise and low frequency noise starts to affect after 1 second observation it usually tend to a floor here about $2.8ppm$ voluntarily this graph was selected to shows the difficulty to asses any possible drift or other low frequency noise impact on the long term stability.

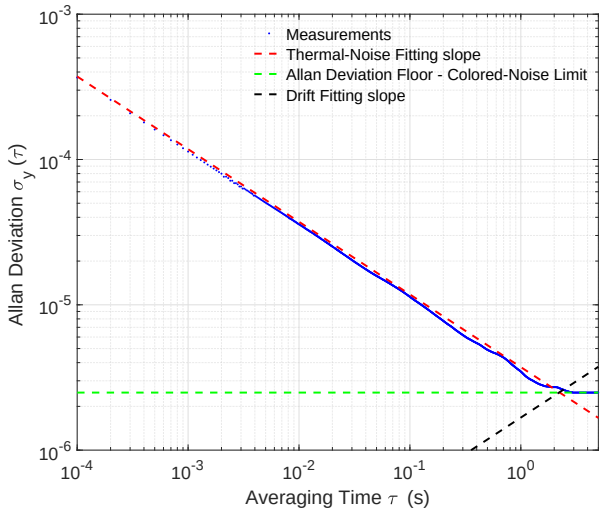


Figure 1.13: Typical Allan Deviation measurement

In some applications, such as the clock data recovery (CDR) in serial data transmission, or clock generation in ADC's, the time-domain measures of frequency stability are closer to the system performance, while for the wireless application usually consider the frequency domain measurements. Rarely but for completeness, the use of structure functions was first introduced by Lindsey and Chie [78] for oscillator phase noise analysis. The main advantage of Structure functions is to avoid the singularities which appear at low-frequencies in the case of colored noise sources. It could be seen as a mathematical unifying methodology. In light of this background, it is worth recalling the work of Sander Laurentius Johannes Gierkink Ph.D. thesis [79] exposing details on the mathematical background of **Frequency stability**, most of

the relationship between the time and frequency domain Fluctuations are summarized in Figure 1.14. Similar definitions could be found in [80, 81, 37, 39].

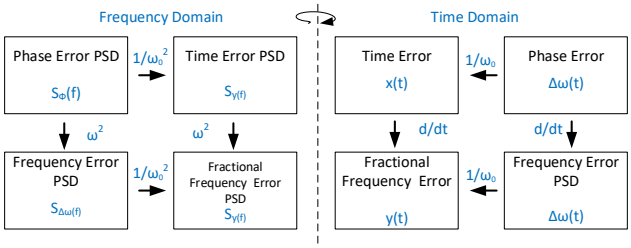


Figure 1.14: Typical Phase-Noise Spectrum and power law asymptote

Since the random phase fluctuation $\phi(t)$ is a random quantity, statistical parameters are needed for their description. For a convenient calculation of these parameters, the mathematics require that the random process underlying these functions has certain properties. Stationarity is such a mathematical property meaning that statistical parameters are time-independent. The auto-correlation function and the power spectral density of a process given by the Wiener-Khintchine theorem [82] leans on this property. The power spectral density (PSD) $S_{\phi(t)}$ of a random stationary signal $\phi(t)$ is defined as the Fourier transform of the random phase fluctuation. The auto-correlation function and power spectral density carry the same information about the random process, and therefore the variance of a random process $\phi(t)$ express as per Equation 1.22 :

$$\sigma = \int_0^\infty S_{\phi(t)}(f) \cdot \partial f = R_{\phi(t=0)} \tag{1.22}$$

However, problems arise when users apply the derived formulas to phase noise processes that are strictly speaking non-stationary. An example is the introduction of a lower cutoff frequency in the power spectral density description of 1/f noise, in relation with the observation time is a workaround [83]. Coming to the actual measurement of phase noise, is $\mathscr{L}(f)$in fact$\mathscr{L}(\Delta f)$where $\Delta f = f - f_0$ defining a frequency offset from the carrier, the following definition is used as (1.23) :

$$\mathscr{L}(\Delta f) = \frac{P_{SIDEBAND(f_0+f;1HzBW)}}{P_{Carrier}} \tag{1.23}$$

The Phase-Noise unit is $\frac{dBc}{Hz}$ meaning Decibel relative to the carrier per Hertz. In principle $P_{SIDEBAND(f_0+f;1HzBW)}$ is the measured power which imply a single-side band spectrum in a 1Hz interval or equivalently a 1Hz Bandwidth filter (RBW) at a frequency offset Δf from the carrier. The earlier assumption made in equation 1.17, assumes to work on the carrier

only, while the effect of both amplitude and phase noise is present in the noise spectrum. The power of the carrier is usually acceptable because it just introduces a small error and the entire signal power is much more difficult to measure, this error is negligible in most cases. When looking at the measured phase Noise such as presented in Figure 1.15. The noise spectrum can be divided into different sections similar to the Allan variance it could be recognized the power law [78].

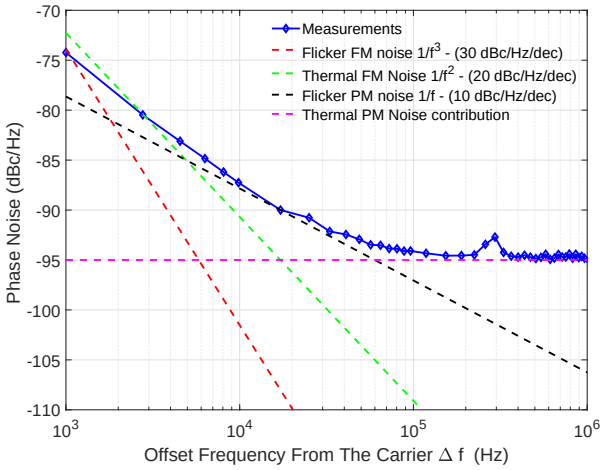


Figure 1.15: Typical Phase-Noise Spectrum and power law asymptote

In this figure, which corresponds well to a real phase noise spectrum, it could be observed the rather standard noise contributions :

- Flicker PM Noise : It relates to a resonance mechanism in the oscillator or non-linearity of the electronics.
- White FM Noise : It is usually an up-conversion of the white noise of the components in the oscillator circuit.
- Flicker FM Noise: It ordinarily refer to the colored noise of the components in the circuit that get up-converted by the oscillator, resulting in this type of phase noise.
- Random Walk FM: This noise has an even higher order $\frac{1}{f^{K_F}}$. It is difficult to measure since it is very close to the carrier, meaning that the observation time is infinite. It can be due to the physical environment sensitivities and therefore monitoring temperature, voltage usually helps to understand the phenomenon.

Throughout the years, different noise models were developed, that help to understand the mechanisms and origin behind such spectrum as presented in the Figure 1.15. It remains very often semi-empirical models [84, 85]. Besides these models some interesting fundamental

limitations were extracted in [59] for fully integrated relaxation (1.24) and ring oscillator (1.25).

$$\mathscr{L}_{min}(\Delta f) = 10 \cdot \log\left(\frac{3.1 \cdot k \cdot T}{P} \cdot \left(\frac{f_{osc}}{\Delta f}\right)^2\right) \tag{1.24}$$

$$\mathscr{L}_{min}(\Delta f) = 10 \cdot \log\left(\frac{7.33 \cdot k \cdot T}{P} \cdot \left(\frac{f_{osc}}{\Delta f}\right)^2\right) \tag{1.25}$$

An approach to quantify the phase noise of harmonic oscillator based on the property of the resonator and excess noise factor F of the circuit. Here considered as a long-channel saturated transistor in strong inversion making the $2 \cdot F = 1,33$ in (1.26).

$$\mathscr{L}_{min}(\Delta f) = 10 \cdot \log\left(\frac{1.33 \cdot k \cdot T}{P} \cdot \left(\frac{f_{osc}}{2 \cdot Q \cdot \Delta f}\right)^2\right) \tag{1.26}$$

Thus a comparison of the measured phase noise with these semi-empirical bound would be an important point of attraction. The latest (1.24) and (1.25), shows a closed form relation between the power. As for many circuits, Figures of Merit (FoM) has been defined. FoM takes several performances together as in one figure. In the meantime, A well-developed FoM makes sure that these effects cancel each other. Nevertheless, there are some optimized points where the circuits gets an optimal FoM and this does not prevent the circuit to be incompatible with certain system specifications given an application. With respect to phase noise the most common FoM was proposed as (1.27) in [86] at the Advances in Analog Circuit Design workshop in 1999.

$$FoM_{PN} = 10 \cdot \log\left(\frac{1}{P \cdot \mathscr{L}_{meas}(\Delta f)} \cdot \left(\frac{f_{osc}}{\Delta f}\right)^2\right) \tag{1.27}$$

The relation (1.27) use P as the power consumption expressed in milli-Watts, ideally the phase noise measurement are given in $\frac{dBc}{Hz}$, as long as the measurement is made in the $\frac{1}{f^2}$ region of the noise spectrum the FoM is not impacted. Any FoM lacking a closed relation between the included parameters would leave the reader clueless. Therefore presenting the FoM contributor separated and then combine in a single number makes more sense. Typically the Figure of merit presented in [36] as defined in (1.28) is an interesting proposal of including quantities without a close form relation in the figure of merit. Interestingly this figure of merit introduce the integrated jitter σ_j, expressed in pico-seconds and representing the integrated jitter between 12 kHz and 20 MHz band, which is approximately independent of the oscillator

frequency. Similarly to (1.27) P as the power consumption expressed in milli-Watts.

$$FoM_{J_CT} = 10 \cdot \log\left(\sigma_j \cdot \frac{\Delta f_T}{f_o} \cdot \frac{P}{6}\right) \tag{1.28}$$

From this figure of merit the reference [36] concludes that crystal oscillator, followed by MEMS and then CMOS implementation rank one after another with respect to this figure of merit. Possibly this figure of merit insert a bias when comparing CMOS implementation as the temperature accuracy is not clearly defined whether it is the deviation over a degree or over a span of temperature on one hand and on the other hand CMOS reference often imply active compensation techniques to achieve interesting temperature accuracy. Thus it is proposed to define a temperature figure of merit to be presented separately such as in equation 1.29, where the temperature sensitivity $\frac{\Delta f_T}{f_o}$, previously defined in (1.3) is expressed in $\frac{ppm}{°C}$.

$$FoM_T = 10 \cdot \log\left(P \cdot \frac{\Delta f_T}{f_o} \cdot 10^6\right) \tag{1.29}$$

Similarly supply voltage sensitivity FoM proposed in [37] could be presented separately. The relative frequency deviation $\frac{\Delta f_V}{f_o}$, expressed in ppm, divided by the relative supply voltage span $\Delta V_{rel} = \frac{2\cdot(V_{max}-V_{min})}{V_{max}+V_{min}} \cdot 100$ can then be used independently of the targeted technology.

$$FoM_V = 10 \cdot \log\left(\frac{\frac{\Delta f_V}{f_o}}{\Delta V_{rel}} \cdot 10^6\right) \tag{1.30}$$

The clock technology evolving with the duty-cycled system, themselves using frequency reference tend to need an instantaneous operational condition to limit the guard-band in the timers. A figure of merit could be defined for the settling time expressed in seconds.

$$FoM_{ST} = 10 \cdot \log\left(\frac{T_{settling}}{1s}\right) \tag{1.31}$$

More dimension could be added to the final comparison, the most important message is that to clearly understand the different trade-offs in the oscillator design space each figure of merit should be presented separately. the dB values sums and given a design space for instance a space optimizing for phase noise, voltage and temperature sensitivity and settling time, would combine as (1.32).

$$FoM_{PNVTST} = FoM_{PN} + FoM_V + FoM_T + FoM_{ST} \tag{1.32}$$

In the case of fully integrated references, the frequency reference signal tends to be full-swing,

and therefore a closed form relation between current consumption and frequency hold : $i = f_o \cdot C \cdot V$, the digital circuit had for decades used the **current consumption per hertz** $\left(\frac{A}{Hz}\right)$, as a key metric. Lately an interesting extension to account for the area was proposed in [87] with the **Normalized Area** defined as $A_{\blacksquare} = \frac{A}{L_{MIN}^2}$, a closed form relation could be demonstrated with power dissipation through the impedance and area relation, with technology scaling the passive could leverage advantage of narrow polysilicon patterns. In the Iot Design space, the requirements of the system might be dynamic. For example, the speed of the processor may scale depending on the incoming data and the speed of the charge pump may be dictated by changing load requirements. In this perspective it is rather important to consider the **Energy per Cycle** expressed in $\left(\frac{J}{cycle}\right)$ as proposed in [88], nevertheless, it should be ensured by design that the energy and frequency relation keeps their linear relation. A summary of the reviewed metrics is proposed in Table 1.1.

Table 1.1: Summary of the metrics for frequency references

Name	Symbol	Unit
Technology Node	L_{min}	nm
Area	A	mm^2
Reference Frequency	f_0	Hz
Nominal Current	I_{DD}	A
Quality Factor	Q	-
Supply Voltage Range	V_{DD}	V
Supply voltage sensitivity	Δf_V	$\frac{ppm}{V}$
Frequency for max voltage	$f_{V_{MAX}}$	Hz
Frequency for min voltage	$f_{V_{MIN}}$	Hz
Temperature Range	T	$°C$
Temperature sensitivity	Δf_T	$\frac{ppm}{°C}$
Frequency for max Temperature	$f_{T_{MAX}}$	Hz
Frequency for min Temperature	$f_{T_{MIN}}$	Hz
Settling Time	$T_{Settling}$	s
Integrated Jitter	J_{cc}	ps
Phase noise	$PN(\Delta f)$	$\frac{dBc}{\text{Hz}}$

Having reported the sensitivity elements it could be calculated individual figure of merit as in Table 1.2.

Table 1.2: Summary of the FoM for frequency references

Name	Symbol	Unit
Absolute accuracy	δ	ppm
Normalized Area	$A_{\blacksquare}$	-
Energy per Cycle	E_c	$\frac{J}{cycle}$
Current dissipation per Frequency	$I(f)$	$\frac{A}{Hz}$
Figure of Merit Power and Phase noise (1.27)	FOM_{PN}	dB
Figure of Merit Temperature (1.29)	FOM_T	dB
Figure of Merit Supply voltage (1.30)	FOM_V	dB
Figure of Merit Settling time (1.31)	FOM_{ST}	dB

According to the explored dimension it is worth combining them as in (1.32) for example, yet keeping the separated presentation.

1.2.3 Benchmarking frequency references

The metrics proposed in Table 1.1 and Table 1.2 were extracted from publications on fully integrated oscillator in a spreadsheet. The Frequency reference included in the spreadsheet are referenced by year, conference or journal, first author and Digital Object Identifier linking to the full paper version. The fully integrated can easily be sorted by their topology whether they are :

1. LC oscillators such as [89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 60, 101] where the most common challenge is to optimize for the Phase noise figure of merit in (1.27), some had reached the level of replacing the crystal in some serial link appliances [102, 103, 104] where the temperature and voltage sensitivity altogether are not affecting the clock accuracy. For LC resonator, the Quality factor is rarely reported making it difficult to compare to a physical boundary.

2. Relaxation oscillator some relatively early work [105, 106]. Frequency of such oscillator range in the MHz, and the stability assessment is reported in terms of Phase-Noise. Quite a few of them have challenged the power, frequency and frequency insensitivity trade off [107, 108, 109, 110, 56, 58, 111, 112, 113, 57, 114, 115, 116, 117] with some guideline presented in [55] finally the proposal in [118] fulfill the requirement of wireline Automotive Ethernet or CAN bus requirements. Another approach in [119, 120, 88, 121, 122] focused on the long term stability as wake-up timer, which requires low voltage, low power

3. Ring oscillator or frequency locked loop (FLL) form a third subgroup. The FLLs VCO is often taken as a ring oscillator [123, 124, 125] and tend to be used in some are rather simple [126] and robust due to self-biasing and first order passive temperature compensation techniques. A few more advanced FLLs includes advanced control system law and devices property to cope with the temperature and supply sensitivity [127, 128, 129, 130].

The overall benchmark explores a few dimensions, the first being power, and energy considerations. The second comes concerning the environmental sensitivities. As a measure of the long-term stability, the phase noise trade-off with the measured power. One more dimension taken into account is the area as a function of frequency, it provides an idea of the current status depending on the target frequency. With the collected data, more dimensions can be explored most of the paper above mentioned do not provide most of the measured information for settling-time in the case of the clock that is actuating a duty-cycled function it gives an idea of the guard-band that to consider on the timer side. Another interesting to report would have been absolute accuracy meaning measurement of the dispersion of trimmed samples over temperature at different voltage and corners which would enable the specification comparison to an application set as in proposed in Figure 1.3.

1.2.3.1 Comparisons of the power, and energy per cycle as a function of frequency

The Figure 1.16, provides an overview of power dissipation as a function of frequency for the collected papers.

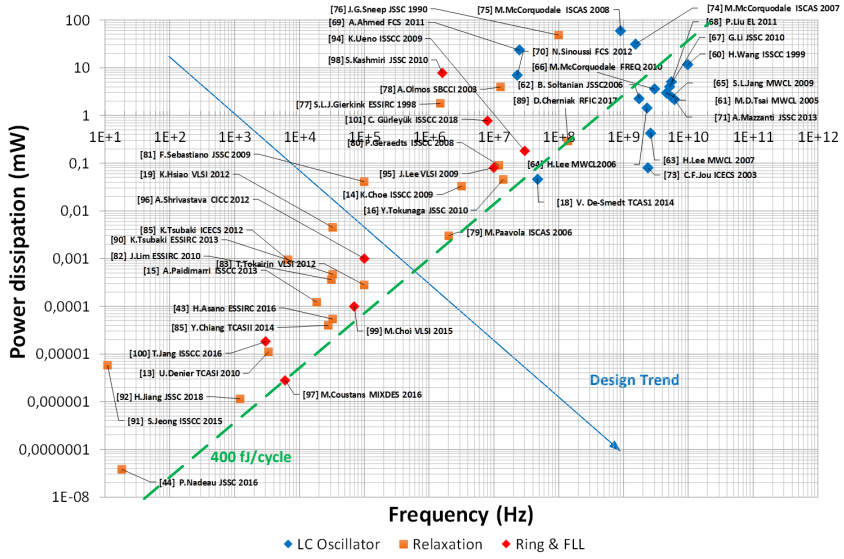


Figure 1.16: Power Dissipation as a function of Frequency

There are different trends to observe; one is the clear GHz range of LC oscillator and their high efficiency despite the higher absolute power consumption. The relaxation and ring oscillators are covering the same range of sub GHz. As shown in Figure 1.17, the energy per cycle of relaxation and ring oscillator tends to be comparable to LC oscillator in the recent years; there are still improvements needed to reach that level.

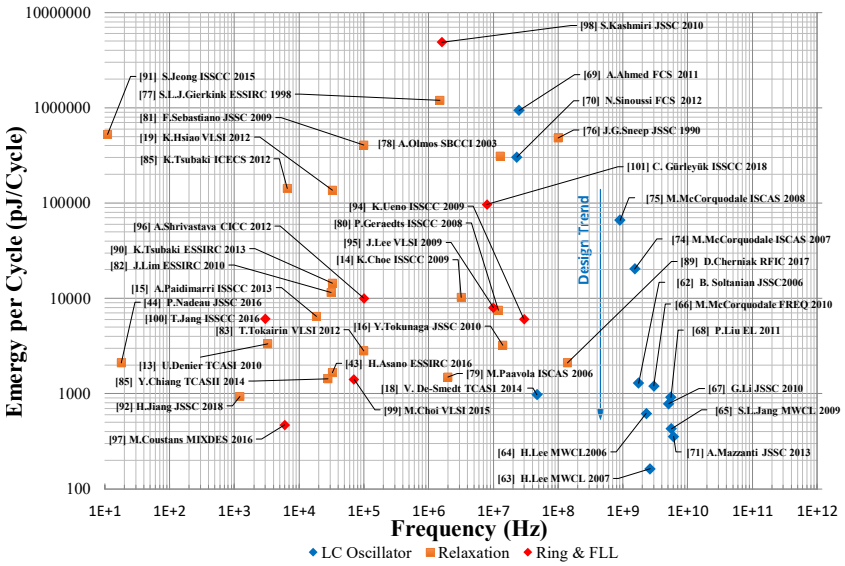


Figure 1.17: Energy Per Cycle as a function of Frequency

Another trend is to decrease the power consumption as much as possible. For that purpose, we could find sub hundred hertz reference timer and even sub Hz ranging in the pico-watt of power dissipation. Nevertheless, the environmental sensitivities observed in the next section are not necessarily performing well in this respect.

1.2.3.2 Comparisons of the Temperature and Line sensitivities as a function of power

The Figure 1.18, provides an overview of the temperature coefficient extracted as in (1.3) a function of dissipated power.

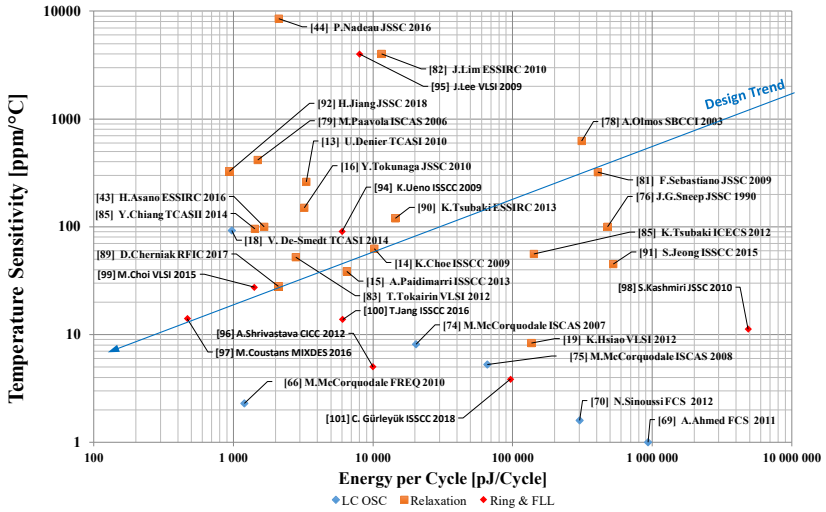


Figure 1.18: Temperature coefficient as a function of Frequency

The Figure 1.18, provides an overview of the supply sensitivity coefficient extracted as in (1.2), as a function of dissipated power. The collected papers shows an interesting aspect for LC oscillator the sensitivities are fairly weak.

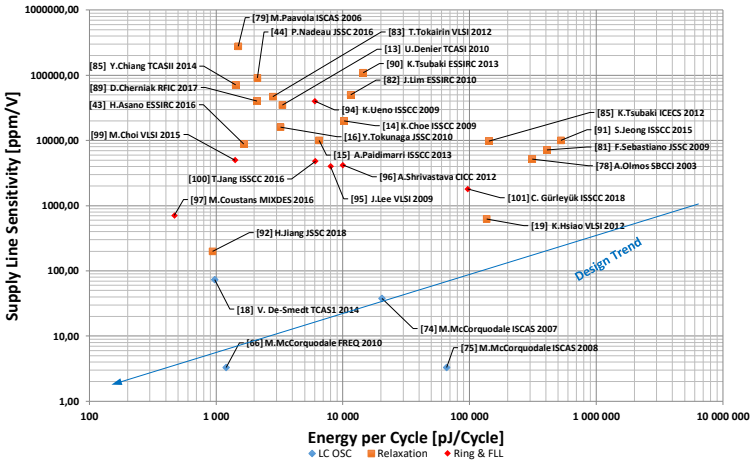


Figure 1.19: Line sensitivity coefficient as a function of Frequency

The collected papers show an exciting aspect for LC oscillator the sensitivities are relatively weak. But when this oscillator got out of harmonics behavior toward relaxation such as in [60], the environmental dependency got worse. Although a lot of compensation mechanisms are introduced, the ring oscillators and relaxation oscillator remain sensitive to the supply voltage. In battery operated systems the supply line would easily get 100mV perturbation leading to an

output frequency deviation of more than hundreds of ppm. And similarly for the temperature range.

1.2.3.3 Comparisons of the Power Phase-Noise Figure of merits

The Figure 1.20, propose the Figure of merit reported in (1.27) to observe the trade-off between the noise and power dissipated by the oscillator as a function of the oscillation frequency. To observe the trade-off between the noise and power dissipated by the oscillator as a function of the oscillation frequency. The figure of merit is often thought to minimize, but this one should be maximized. Maximizing this figure of merit translate into the compromise between the best accuracy traded for the lowest power.

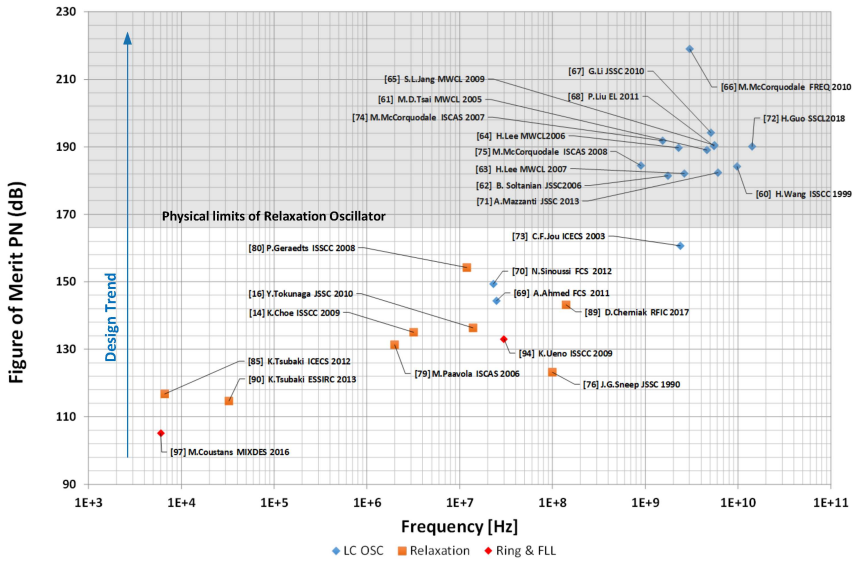


Figure 1.20: Figure of Merit Power and Phase Noise as a function of Frequency

The LC oscillator shows a superiority in this respect but it has to be counter balanced with the assumption found in [59], the maximum Figure of Merit can't reach higher than 169 dB for relaxation and ring oscillator. This area was made Grey in the Figure 1.20. The practical design did not reached yet such a level, the power invested in the buffer was not taken into account in [59]. One could also observe that low frequency and low power reference are rather far from that level.

1.3 Power management concerns

Looking back in the past decade consumer electronics served us with a smart-phone, which integrate most of the cited wireless and eventually USB wirelines technologies. The Figure , introduce to a survey from data collected from mass market available smart-phones. The

Figure 1.21 present in red the battery autonomy when the phone is turned in the sleep mode (dark red squares) and Active meaning wireless connectivity on (red dots). Essentially the Active mode power consumption did progress reaching more than one day active conversation or network.

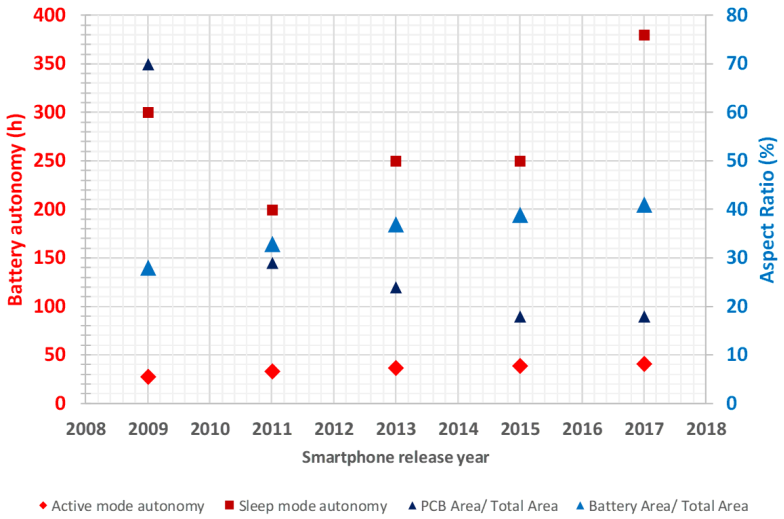


Figure 1.21: Smart Phone survey on the sleep mode to active mode autonomy and PCB and Battery area with respect to the total area.

An interesting trends on the sleep mode autonomy and printed circuit board (PCB) area as a ratio with the total could be correlated with the Dennard scaling, on one hand more leakage and therefore less sleep mode autonomy but a higher integration so a lower PCB footprint. both challenge kept being optimized toward less footprint and more autonomy. The ratio between the battery area and the total area had increased by 10 % and this comes along with the battery technology. A survey table is proposed in Table 1.3, some important parameter were collected from supplier datasheet.

Table 1.3: Summary of available battery storage performances

Technology	$ZnMnO_2$	$Li/Mn/O_2$	MnO_2	ZnO_2	Li Thin-Film	Supercap
Market denomination	AAA	CR2032	LR44	PR44	MEC102	GS130F
Picture						
Volume (cm^3)	3,8	1	0,5	0,5	0,25	0,5
Nominal Voltage (V)	1,5	3,0	1,5	1,4	4,1	2,75
Peak-current	300	20	10	10	5	30
Output resistance	0,3	10 - 40	1 - 5	2 - 8	15	0,02
Self-Discharge	5 years	10 years	5 years	weeks	10 years	1 week

The survey Table 1.3 propose originally the different chemistry going to the known commercial name and then an illustration. Smart phone is one of the most widely spread consumer electronics product, and could be considered as one of the wireless sensor nodes (WSN). Because of its general purpose and include a display it's autonomy drop significantly. According to some market research [131, 132], most of the connected object won't include a display and rather focus like WSN on machine to machine communication (M2M). In 2016 a tutorial article, a survey was made on available on the shelf parts for WSN [133].

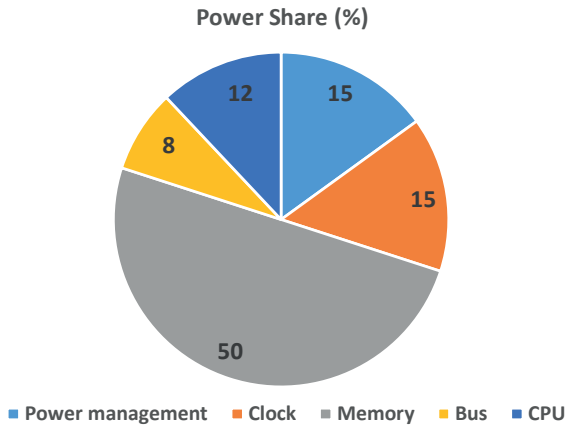


Figure 1.22: Wireless Sensor Network survey on Power Budget.

It provides that the power budget in a System On Chip (SoC) for implementation of a WsN, will consume roughly 15% in the clocking aspect very often consumption in a system bus and DC-DC shares also with the clocking. This comes to Duty-cycled operations, impose to have different functional modes.

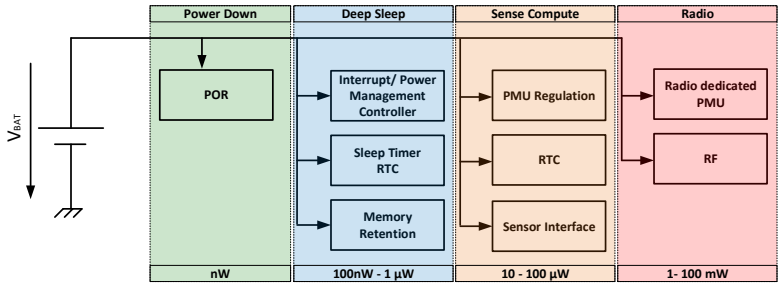


Figure 1.23: Wireless Sensor Network Typical Power Modes.

The Figure 1.23, propose different power modes including a deep sleep and two different active level one that include computing and another communication which in fact contains itself two

power modes one for the transmission and one for the reception. Simplifying to the extreme the proposed analysis in [134] on the duty-cycled radios for illustration purpose it is proposed a two level current profile as show in Figure 1.24, one active mode with a consumption I_{activ}, and last for a period noted T_{activ},. The second mode called sleep or standby comes with a consumption is noted I_{stdby}, and last for a period noted T_{stdby}.

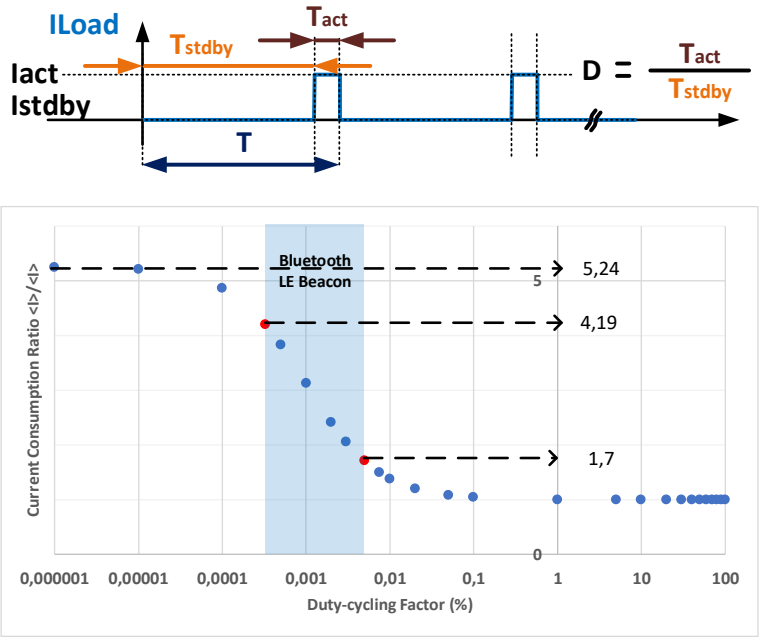


Figure 1.24: Illustration of the duty-cycled Wireless Sensor Network consumption profile with two Power Modes.

The average consumption could be expressed as Equation 1.33.

$$I_{avg} = \frac{1}{T}\int_0^T i(t)\cdot dt \sim I_{stdby}\cdot(1-D) + I_{activ}\cdot D \tag{1.33}$$

The numerical application presented here is a traditional Bluetooth low energy beacon is active 0,0003% up to 0,005%, the active mode dissipates tens of milliamps. Nevertheless, some commercial microcontrollers started to include extremely low sleep-mode including the real-time clock in the always-on power domain or deep-sleep as low as 420 nA and power down as little as 20 nA. Some other real-time clock proposed consumption as little as 60 nA. When having a PCB is involved those RTC modules as prove to be as little 1.5 mm^2. With these number, we can check the two asymptotes the sleep current ultimately reach 5,25 (420/80), and when it gets active, the current ratio is 1. Another observation in the case of Bluetooth low energy that the duty cycled operation using an external real-time clock will benefit from a factor 2 to 5 and further if the real-time clock consumes less. The complexity of the power

modes is indeed further complex; a typical consumed current profile of a wireless sensor node could be as illustrated in Figure 1.25, the particular case of a Zigbee transceiver presented in [135], is proposed.

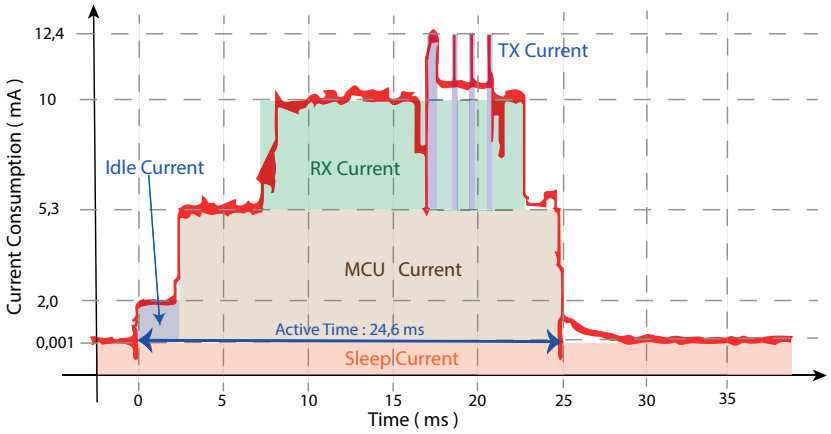


Figure 1.25: Wireless Sensor Network Current profile.

The measurement are the data-log taken from a power analyzer. This graph represents the current consumption from a 3V battery of a sensor node measure the temperature with a typical precision of 0.1°C and sending the result through the wireless standard IEEE 802.15.4. It includes the full system : microcontroller, radio, sensors and power management. The sleep current is 1µA, the microcontroller use up 5,299 mA and similarly for the radio, it consume 4,9 mA while active, in receive mode (RX) and 7,1 mA while transmitting (TX). It appears that the system wakes-up. Initially to an idle mode where an on-board capacitance get charged prior to turn on the chip (idle mode). Then the application of analog temperature sensing and some signal processing to ensure 0.1°C precision takes over. Having the information ready to be transmitted, it switch on the radio chip and perform radio calibration. The radio listen to channel waiting for beacon then receive, and treat information. In the same time the firmware prepare a IPv6 secured frame. The radio segment is a CSMA/CA (listen before talk). Can vary in length depending on the activity on the channel. Once it receive low level acknowledgment from parent, the radio switch the system back to deep sleep mode before the next wake-up. This cycle describe a transaction, the transaction last 24,6 ms. As a matter of fact when addressing the battery operated sensor nodes, the reservoir has a given capacity often stated in milli-Ampere per hour, another possible is to derive in terms of charge (Coulombs) deriving from the International System (SI) units Ampere and second. This lead to $1C = 3,6 \cdot mAh$. In that case with the current profile we have it barely make sense to discuss an average current but rather the energy a transaction takes. The transaction in Figure 1.25, last 24,6 ms and consume 192 µC. A CR2032 could for instance handle 4,5 million of them, the peak current is 25 times below the maximum the CR2032 cell could tolerate. Data-logging every quarter of an hour would lead to 35 040 transaction per year. The sleep-mode current is less than 1 transaction per year, thus an autonomy of 128 years would be expected. Nevertheless the battery technology limit it-self this autonomy through self-discharge over 10 years. Beside this limitation we can

observe in [135], that a DC-DC converter and LDOs were used. Seemingly the CR2032 cell could handle the energy consumption, current peaks. It raises the following question: “Is it worth spending a current overhead in biasing an LDO or a DC-DC ?”. Such a problem is not necessarily trivial and requires to describe some hypothesis. Besides many, more complex battery discharge models exist a simple premise of a linear discharge introduced in Figure 1.26, the model presented remains acceptable in most of the cases [136].

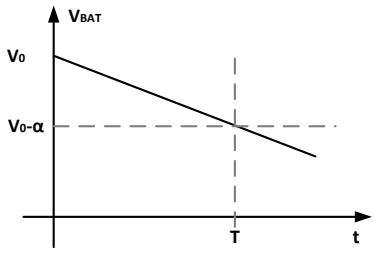


Figure 1.26: Battery Discharge model

The battery chemistry has a given capacity (given in Ampere per Hour: AH), and develop a voltage named V_o, when it degrades to a voltage $V_o - \alpha$, after a given time T, at which the capacitance of the battery is considered discharged. The load is assumed to behave as a logic load where the load current can express in a static component and a dynamic one. V_{reg}, is supposed to be the voltage at the load terminals. The load current is then express as Equation 1.34.

$$I_{load} = I_q + C \cdot F_{ck} \cdot V_{Reg}(t) \tag{1.34}$$

The battery to load connections are represented in Figure 1.27, these connection impact on the current drawn by the battery and the regulators forms a node. Nevertheless, the battery capacity gets

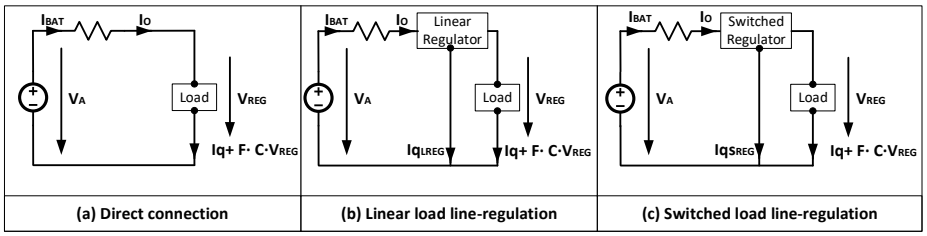


Figure 1.27: Battery to load connection (a) direct, (b) with a linear power converter regulator, (c) with a switched power converter regulator

When the scenario of direct connection is considered, the Equation 1.35, it directly related the battery current to the drained current of the load as in Equation 1.34, taking into account a linear degradation of the open voltage as per $V_0 - \frac{\alpha}{T} \cdot t$.

$$I_{Bat_{Direct}} = I_{LOAD} = I_q + C \cdot F_{ck} \cdot V_0 - \frac{\alpha}{T_{Bat_{Direct}}} \cdot t \tag{1.35}$$

Computing the integral of the load current (I_{LOAD}), we get the battery capacity when directly connected to the load. this capacity then express in $A \cdot h$.

$$C_{Bat_{Direct}} = \int_0^T I_{Bat_{Direct}} = T_{Bat_{Direct}} \cdot \left[I_q + C \cdot F_{ck} \cdot V_0 - \frac{\alpha}{2} \right] \tag{1.36}$$

Which provides us a direct relation between the discharge instant ($T_{Bat_{Direct}}$) and available battery characteristics from the battery datasheet such as the capacity ($C_{Bat_{Direct}}$) and open voltage (V_0) , the and some information's on the load current. For example the typical characteristics of a CR2032 cells are that V_0 is 3V originally, and decrease toward the discharge voltage of 2V which leads to $\alpha = 1$. Nevertheless the device quiescent and active current is not necessarily given, but could be estimated from estimations or more accurately with transistor level simulations.

$$T_{Bat_{Direct}} = \frac{C_{Bat_{Direct}}}{I_q + C \cdot F_{ck} \cdot V_0 - \frac{\alpha}{2}} \tag{1.37}$$

When connecting a linear regulator between the battery and the load, its equivalently as a node draining a quiescent current (I_{qLREG}), this current sums with the load current. Nevertheless, the regulated output voltage is now fixed and regulated (V_{REG}), although this is neglecting the output ripple voltage.

$$I_{Bat_{LREG}} = I_q + I_{qLREG} + C \cdot F_{ck} \cdot V_{REG} \tag{1.38}$$

Computing the current integral we get the battery capacity in Equation (1.39),

$$C_{Bat_{LREG}} = \int_0^T I_{Bat_{LREG}} = T_{Bat_{LREG}} \cdot \left[I_q + I_{qLREG} + C \cdot F_{ck} \cdot V_{REG} \right] \tag{1.39}$$

In the same manner, as the direct connection, it could be inverted to get a direct relation between the discharge instant ($T_{Bat_{LREG}}$). The dependency to the battery discharge now

disappear, nevertheless this assumes that the battery voltage is greater than the regulated voltage.

$$T_{Bat_{LREG}} = \frac{C_{Bat_{LREG}}}{I_q + I_{qLREG} + C \cdot F_{ck} \cdot V_{REG}} \tag{1.40}$$

Finally addressing the case of a switched mode regulator, it now introduce an efficiency (η) of the switching converter.

$$I_{Bat_{SREG}} = \frac{I_q + I_{qSLREG} + C \cdot F_{ck} \cdot V_{REG}}{\eta \cdot V_0 - \frac{\alpha}{T} \cdot t} \tag{1.41}$$

Computing the current integral we get the battery capacity in Equation (1.42).

$$C_{Bat_{SREG}} = \int_0^T I_{Bat_{SREG}} = \frac{I_q + I_{qSLREG} + C \cdot F_{ck} \cdot V_{REG}}{\eta} \cdot T_{Bat_{SREG}} \cdot [\ln(V_0 - \alpha) - \ln(V_0)] \tag{1.42}$$

Inverting the battery capacity relation a direct relation between the discharge instant ($T_{Bat_{SREG}}$). The dependency to the battery discharge is now included

$$T_{Bat_{SREG}} = \frac{C_{Bat_{LREG}}}{\frac{I_q + I_{qSLREG} + C \cdot F_{ck} \cdot V_{REG}}{\eta} \cdot [\ln(V_0 - \alpha) - \ln(V_0)]} \tag{1.43}$$

The equation 1.44 propose to investigate if the insertion of a linear regulator increase the global autonomy.

$$\triangle T = \frac{T_{Bat_{LREG}}}{T_{Bat_{Direct}}} \tag{1.44}$$

The first assumption made is that initially the battery capacity is the same, we assume that the linear regulator has a drop out voltage V_{do}.

$$\triangle T = \frac{I_q + C \cdot F_{ck} \cdot \left(V_0 - \frac{\alpha}{2}\right)}{I_q + I_{qLREG} + C \cdot F_{ck} \cdot (V_0 - V_{do})}$$

Formulating the autonomy gain hypothesis $T_{Bat_{LREG}} \geq T_{Bat_{Direct}}$ formulate as :

$$I_q + C \cdot F_{ck} \cdot \left(V_0 - \frac{\alpha}{2}\right) \geq I_q + I_{qLREG} + C \cdot F_{ck} \cdot (V_0 - V_{do})$$

Leading to the condition that the linear regulator wont provide a gain if the voltage drop is significant with respect to the battery end of life voltage (α),

$$V_{do} \geq \frac{\alpha}{2} + \frac{I_{qr}}{C \cdot F_{ck}} \tag{1.45}$$

As all the quantities in equation 1.45, are real and positive number, adding a voltage regulator would usually save battery life, nevertheless, conditions apply. The voltage drop between input and must be greater than half the end of life voltage. The equivalent capacitance and operating frequency assumes here a typical System on chip dynamic consumption under a bandgap voltage. The following numerical application is proposed. For instance it is quite a standard to find SoC with the following $V \cdot C \cdot F_{ck} = 1.2 \cdot C \cdot F_{ck} = 30\frac{\mu A}{MHz}$, this leads to use $C \cdot F_{ck} = 25\frac{\mu A}{MHz}$ the assumption is sim makes under a volt such MCU's run around 16 MHz making $C \cdot F_{ck} = 400\mu\frac{A}{V}$ for the quotient. Then it is proposed a sweep of the linear regulator quiescent current I_{qr} for the various battery reported in Table 1.3. is proposed.

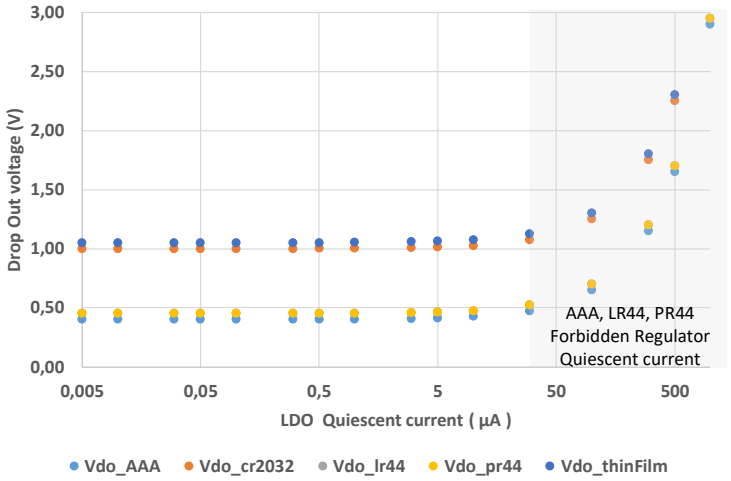


Figure 1.28: Constraints on the linear regulator quiescent current given a SoC typical load and battery chemistry

It could be observed that literature reports power management units that includes more than the linear regulator with a quiescent current well below $30\mu A$ [137, 138, 53, 135, 139, 122], which would be the corner case to reasonably remove the linear regulator between the battery

and the load. The efficiency of a linear regulator is described in (1.46).

$$\eta = \frac{V_{REG} \cdot I_{load}}{V_{BAT} \cdot I_{load} + I_{qLREG}} \tag{1.46}$$

Theoretically optimizing the voltage drop ($V_{BAT} - V_{REG}$), the efficiency would tend to 100%, in that perspective it was introduced in [140], the so called Efficiency Enhancement Factor (EEF) figure of merit provides a basis for comparison between LDOs and Switching converters. Nevertheless as discussed in [141], the reports for the peak efficiency are not necessarily covering the application constraints. Having observed the current profiles in Figure 1.25, raise the question of the regulator stability. Linear regulator are most of the time unconditionally stable, when optimizing the voltage drop some architectures so called Low Drop Out (LDO) regulator, their stability depend on the output load, some interesting work propose [142, 143] load unconditional stability. Switching converters are in general reasonable to stabilize but their settling time tend to be slower.

Similar calculation as (1.45) can be made to compare linear regulator and switched converters it can be observed as in (1.47). From this relation it could be extracted a condition on the switching regulator quiescent current.

$$I_{qSLREG} \leq I_q \cdot (\eta - 1) + C \cdot F_{ck} \cdot \left[\eta \cdot \left(V_0 - \frac{\alpha}{2} \right) - \ln\left(1 - \frac{\alpha}{V_0} \right) \right] \tag{1.47}$$

The various conditions and monotonic relation between the switched converter efficiency (η) and its quiescent current (I_{qSLREG}) is inversely proportional, thus introduce an implicit variable that makes the phenomenon non separable. Another approach would be to introduce a figure of merit related to a given synopsis. Typical IoT system on chip power modes were recalled in Figure 1.23. SoC architectures are designed so that energy-consuming blocks such as sensor interface, computing, and radio, spend the smallest possible time in active mode. Besides this improvement, the deep-sleep mode must be highly optimized and further reduce the delay to boot-up the active operation. In this regards, some control logic, time and another reference might be embedded, controlling environment interruption could also be important, and in any case to avoid collision or secure the communication channel a crypts primitive generating random number must be available. A simplified scenario is proposed in Figure 1.29.

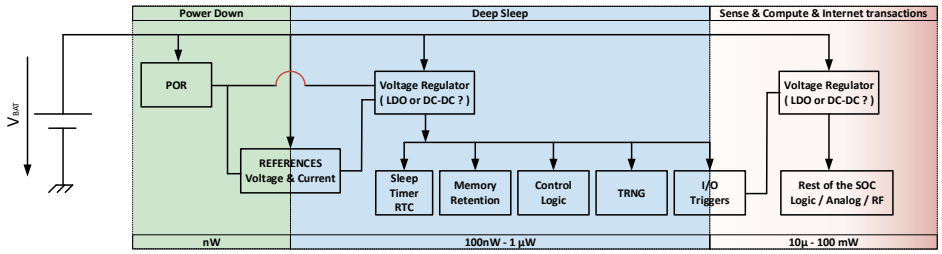


Figure 1.29: Illustration of the SoC Sleep mode and active mode.

It is hereafter proposed a metric that is to be adaptable to various scenario. As stated earlier the performances of interest among which silicon area, power consumption, bill of material cost. would and by giving a weight to each one, depending on the overall target performance the Equation (1.48) and (1.49) provides the first step of computation.

$$\langle I_{LDO} \rangle = I_{sleep} \cdot (1-D) + \left(I_{activ} + I_{qLDO}\right) \cdot D \tag{1.48}$$

$$\langle I_{SLREG} \rangle = I_{sleep} \cdot (1-D) + \left(I_{activ} \cdot \frac{1}{\eta} \cdot \frac{V_{REG}}{V_{BAT}} + I_{qSLREG}\right) \cdot D \tag{1.49}$$

This set enables us to define two separate figure of merit for LDO (1.50) and switched regulator (1.51).

$$FoM_{LDO} = wp \cdot \frac{\langle I_{LDO} \rangle}{\max(\langle I_{LDO} \rangle; \langle I_{SLREG} \rangle)} + wa \cdot \frac{{}^{A}SOC_{LDO}}{\max\left({}^{A}SOC_{LDO}; {}^{A}SOC_{DCDC}\right)} + w_{BOM} \cdot \frac{{}^{BOM}SOC_{LDO}}{\max\left({}^{BOM}SOC_{LDO}; {}^{BOM}SOC_{DCDC}\right)} \tag{1.50}$$

$$FoM_{DCDC} = wp \cdot \frac{\langle I_{SLREG} \rangle}{\max(\langle I_{LDO} \rangle; \langle I_{SLREG} \rangle)} + wa \cdot \frac{{}^{A}SOC_{LDO}}{\max\left({}^{A}SOC_{LDO}; {}^{A}SOC_{DCDC}\right)} + w_{BOM} \cdot \frac{{}^{BOM}SOC_{LDO}}{\max\left({}^{BOM}SOC_{LDO}; {}^{BOM}SOC_{DCDC}\right)} \tag{1.51}$$

The current consumption is considered at the level of the main supply source in Ampere. For the FoM, users must take care not to mix the units. These figure of merit could also be completed with more details information such as settling time, line regulation or other parameters which matters to the considered application. For instance, we here consider the main challenge is power consumption, thus the weighting coefficient (w_p) will have the highest weight. To have a faster reading, as we are looking for a relative improvement of a switched regulator with respect to a linear ($\delta\eta$), we could formulate the figure of merit as Equation 1.52.

$$\delta\eta = \frac{FoM_{LDO} - FoM_{DCDC}}{FoM_{LDO}} \tag{1.52}$$

A numerical application presented in Figure 1.30, provides us with constraints of BLE Beacons at a duty cycle of 0,04% of activity.

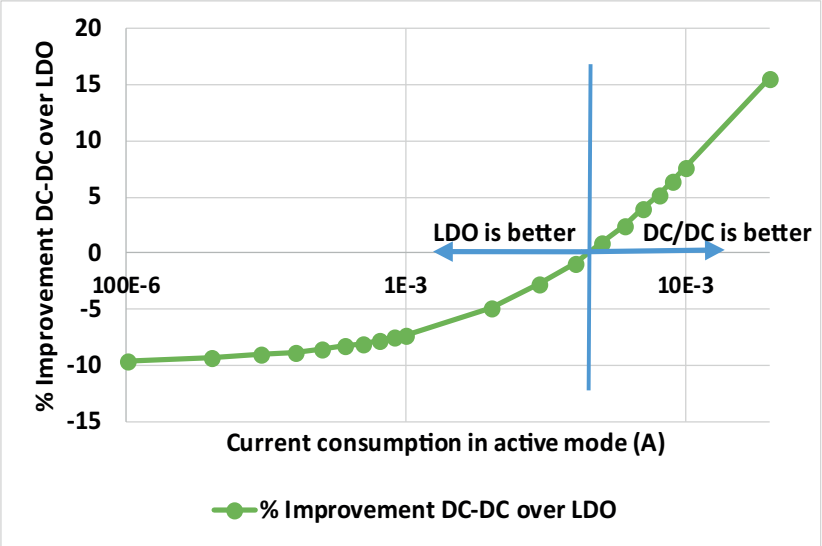


Figure 1.30: Illustration of the loss and gain analysis of using switched or linear regulator for a given load.

The entire SoC area was considered identical in both cases. The BoM can be used to also examine the onboard footprint as besides a decoupling capacitor that both linear and switched regulator might ask to be external; there would be either a coil or some capacitors for a switched regulator. The switched converter was considered to be 85%, and the quiescent current number picked from [133]. It shows us that for example the current profile of Figure 1.25, is having a corner use case in the processing phase and when the radio pulse starts a switched converter is worth having.

Process for Low-Power circuits

Over the years device and integrated circuit design interactions have fascinated both process development engineers and circuit designers. Challenges such as the variability, the power constraints, or the physical layout effects have been around for a long time. When this work started, it aimed to reach ultra-low-power consumption, the investigations made in relation to a 180nm Flash process. While designing one could observe repetitive structures and problems. The design of analog cells offers several degrees of freedom such as power, gain, noise, linearity, voltage swing, supply voltage, speed, and impedance. Several approaches have been proposed and are more or less structured but overall based on the $\frac{g_m}{I_D}$ methodology [144, 145, 146, 147, 148]. This figure is bridging a small signal quantity which is the transconductance, to a large signal quantity which is the drain current. As soon as either target, transconductance or drain current, is fixed, the other sizing parameters follow. These methodologies rely on an abstract view of semiconductor physics, the so called compact models. This chapter has three subsections. The first section 2.1, proposes a short recall on compact models and the essential parameters used for our derivations including their extraction procedure. Among these parameters, the digital design community reports variability as being critical [149, 150] and that variability is also known as local mismatch. Such a variability is critical to the repeatability of the logic gate delay [151]. This triggered some investigation into the causes due to a high interest being seen as a limitation of ring oscillators for fully integrated low-frequency and low-power yet accurate oscillators. The second section 2.2, presents the specific implication of the threshold voltage variability was part of our investigations and led to the implementation of a semi-empirical compact model by the research group of Professor Matthias Bucher at the Technical University of Crete, and notably, Nikolaos Makris and Nikolaos Mavredakis implemented the Verilog code used as an abstract view of the transistor models in the simulation tools. These models enabled the verification of the performances of the proposed circuits along the thesis. In the third section 2.3, as the low-power implies a low-current and thus the need for large resistor values, it provides a few insights into the implementation of large resistors.

2.1 Physics-based compact models

A semiconductor device model can assume different levels of abstraction. The most accurate representation is based on the detailed 3-dimensional (3D) geometrical and processing characteristics of the device structure. Such models are suitable for Technology CAD (TCAD). These simulators solve Poisson's, transport and continuity equations to find the electron and hole concentrations and derive the currents flowing in the structure given some contact and bias conditions. Such a structure can be observed in Figure 2.1.

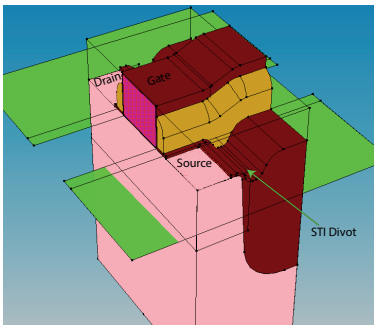


Figure 2.1: Three dimensional NMOS device structure including divot etch for simulation using Technology CAD tools

TCAD simulation is impractical for circuit simulation but could help due to the very complex and time-consuming solution needed for every single device. Mathematical models intended for circuit-level simulation that describe the current and charge behavior of semiconductor devices as a function of voltage, process, electrical, environment and geometry parameters are referred to as compact models [152]. Circuit-level models used in SPICE [153] describe a component relative to its terminals ; they are based on the physics of the device but are more abstract and also include some empirical approximations. In order to capture the full potential of semiconductor devices, compact models that can be used in Computer Assisted Design (CAD) tools are required to provide verification of results. Industry standards provide fittings related to observed electrical measurements related to the core effects.

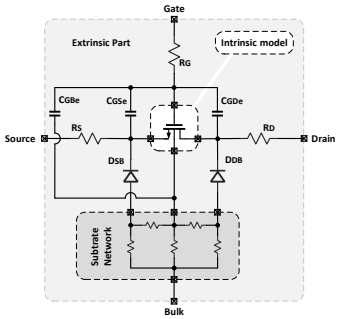


Figure 2.2: A MOSFET intrinsic element and the extrinsic elements

BSIM3 was selected as the industry-standard bulk MOSFET model in 1996 [154] although the threshold-voltage based formulation of the core model was found to be impractical to cover all biasing regions, in fact the core model or intrinsic part describes the behavior of a long-channel MOSFET. As shown in Figure 2.2 on top of this intrinsic model there are external passive and active devices to take into account. Nevertheless the core intrinsic model accounts for 10 % of the total formulation [155] of the BSIM model. Figure 2.3 shows that the implementation of the core model strategy is about having an external not necessarily physical coefficient to influence the fitting function. From BSIM4, the threshold-based approach was reconsidered due to some issues related to bias dependency asymmetry when drain source voltage is null. Leading to the implementation of a charge based model in the core model of the BSIM6 release [155].

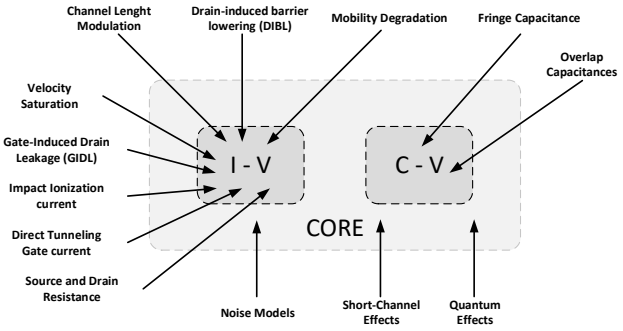


Figure 2.3: The core model and additional effects responsible for a compact's model's accuracy

The charge-based or charge sheet approach taken from the physical models is to derive equations based on the actual device physics and include as few parameters as possible into the model [156, 157]. For example, the evaluation of the drain current as explained in [158] is derived in the case of a charge -based physical model such as (2.1) which is a continuous equation based on physical quantities and bias conditions:

$$I_D = I_{SPEC_{\blacksquare}} \left(i_f - i_r \right) \tag{2.1}$$

In Equation 2.1, $I_{SPEC_{\blacksquare}}$ represents the specific current which embeds a scaling parameter, the mobility and sub-threshold slope dependencies, while the current i_f and i_r the reverse current make the drain current a superposition of two independent and symmetrical effects of the bias conditions at the drain and at the source.

$$i_f - i_r = \left(q_s^2 + q_s \right) - \left(q_d^2 + q_d \right) \tag{2.2}$$

Seen from Equation 2.1 the influence of the bias could seem unclear. When applying the

linearisation of the mobile inverted charge with the surface potential, there is a particular value of the surface potential that does not appear explicitly in the measurable characteristics of the transistor. For a particular value of the gate voltage, the inverted charge becomes zero. This particular value of the channel voltage is called pinch off voltage noted v_p [157].

$$v_p - v_s = 2 \cdot q_s + \ln(q_s) \tag{2.3}$$

$$v_p - v_d = 2 \cdot q_d + \ln(q_d) \tag{2.4}$$

The voltage bias condition with respect to the source voltage appears in (2.3) and with respect to the drain voltage in (2.4) which is practical for the implementation. From a designer's perspective, parametric simulation adds a long iterative process as a time overhead to achieve a given bias point, variability or AC performance,while compact models such as BSIM are broadening their numbers of parameters, as shown in Figure 2.4.

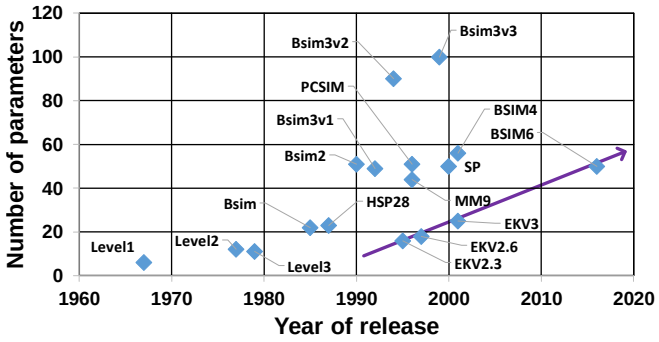


Figure 2.4: Number of DC model parameters as a function of the year of the introduction of the model

Significant growth of the parameter number can be noticed. The MOSFET model development based on semiconductor physics preserves a coherent charge-based framework. This framework ensures a limited number of parameters, while traditional compact modeling fosters the use of non physics based fitting parameters instead. Figure 2.4, considers a single transistor type and no scaling parameters. In the last BSIM3v3 this made it to 1000 for a single type transistor. Besides charge-based models are providing a reduced amount of parameters in simplified charge-based models and show that it could be used despite limiting the design framework to 10 parameters per device type. A summary of the used parameters and design recipe is presented in the next subsection.

2.1.1 Key parameters for low-power design

Over the years, low-power design and the $\frac{g_m}{I_D}$ methodology [144, 145, 146, 147, 148] have been applied to several structures for transistor level design of amplifiers. However, in some specific cases it could be interesting to have a direct relation between the drain current and the gate voltage approximation [159]. The Equation could be inverted although it's not a physics-based model but a good match with the interpolation function given in Equation 2.5.

$$I_D = I_{SPEC_{\blacksquare}} \cdot \frac{W}{L} \cdot \ln^2\left(1 + e^{\frac{V_p - V_s}{2 \cdot u_T}}\right) \tag{2.5}$$

The above equation stands for a saturated transistor meaning it only considers the forward inversion charge i_f. Doing so, we must introduce the inversion factor I_F as given in Equation 2.6.

$$I_F = \frac{I_D}{I_{SPEC_{\blacksquare}} \cdot \frac{W}{L}} \tag{2.6}$$

At present the only process parameter is the specific current $I_{SPEC_{\blacksquare}}$ which represents the specific current which embeds a scaling parameter, the mobility and sub-threshold slope dependencies. The knowledge of the targeted inversion factor I_F, the power budget which would fit the bloc specification and one technology parameter which is the specific current $I_{SPEC_{\blacksquare}}$ would provide a direct insight into the transistor sizing through its aspect ratio.

$$\frac{W}{L} = \frac{I_D}{I_{SPEC_{\blacksquare}} \cdot I_F} \tag{2.7}$$

It can also be observed the direct relation with the pinch off voltage V_p, which is very often approximated such as in Equation 2.8 as the sub-threshold slope factor n, is almost constant with respect to the channel voltage variation.

$$V_p = \frac{V_G - V_T}{n \cdot u_T} \tag{2.8}$$

An illustration of the above Equations is shown in Figure 2.5, which provides a plot of the Inversion Factor or Normalized Current as a function of the normalized pinch off voltage. The black curve represents the weak inversion or the sub-threshold approximation, while the red curve displays the Strong inversion or super-threshold approximation. The continuous form proposed in Equation 2.5 and then normalized to a specific current is shown in blue. The numerical solution of the EKV model is depicted by a black cross.

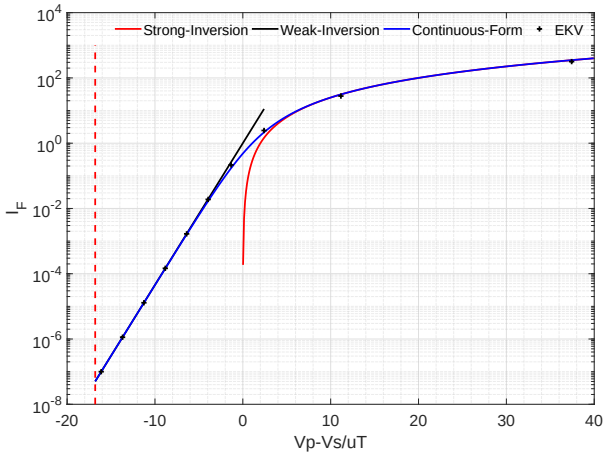


Figure 2.5: Static Id=f(Vg) characteristic

A few particular points can be observed in Figure 2.5. When $\frac{V_P - V_S}{u_T} = 0$, the singularity between the two regimes (Weak and Strong Inversion), approximation corresponds to the threshold voltage. When the gate voltage with respect to the bulk is null, this corresponds to the dashed red line, and this point correspond to the leakage current of the MOS device. The sub-threshold slope factor n can be directly observed as the slope of the black approximation. This shows how powerful the inversion factor $I_F$is as a concept to describe the behavior of an MOS Transistor. Having introduced the notion of inversion factor, it is presented as $\frac{g_m}{I_D}$ in Equation 2.9.

$$\frac{g_m}{I_D} = \frac{1}{n \cdot u_T} \cdot \frac{1}{\frac{1}{2} \cdot \sqrt{I_F + \frac{1}{4}}} \tag{2.9}$$

Besides bridging a small signal quantity, which is the transconductance, to the drain current, it is also a convenient relation to the inversion factor I_F. Equation 2.9 provides the inversion factor as in Equation 2.10.

$$I_F = \left(\frac{1}{n \cdot u_T \cdot \frac{g_m}{I_D}} - \frac{1}{2} \right)^2 - \frac{1}{4} \tag{2.10}$$

In recent years, with technology scaling, the velocity saturation coefficient λ_C was introduced to the $\frac{g_m}{I_D}$ figure [160].

$$\frac{g_m}{I_D} = \frac{\sqrt{(\lambda_C \cdot I_F + 1)^2 + 4 \cdot I_F} - 1}{I_F \cdot (\lambda_C (\lambda_C \cdot I_F - 1) + 2)} \tag{2.11}$$

The carrier's velocity varies linearly with the applied electric field as the mobility is consid-

ered as a constant parameter. However in a short channel MOS transistor, due to excessive collisions, their velocity saturates after a critical electrical field. There is observed in silicon a limit at $10^7 \frac{cm}{s}$ for both electrons and holes. These collisions lead to a saturation of the output current. This effect kicks in when the transistor channel is in strong inversion, when $I_F = \frac{1}{\lambda_C}$. Figure 2.6, is an illustration of the inversion level to which this effect kicks in as a function of process channel length. One can notice that below 100 nm channel process mosfet devices are highly prone to be degraded by carrier velocity saturation. The data-set is collected from various papers [160, 161, 162, 163].

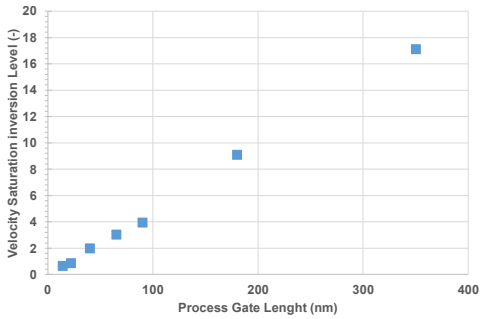


Figure 2.6: Inversion level $I_F = \frac{1}{\lambda_C}$ at which velocity saturation starts to influence as a function of process channel length.

Speaking of transistor saturation, the confusion can append between the velocity saturation and the saturation voltage also called pinch-off saturation. Both result in an overload of the drain current, nevertheless, the mechanism of voltage difference between the pinch-off point and the source remains constant even if the drain-source voltage increases, thus, the current flow clogs up and the transistor is said to be in saturation. The pinch-off saturation can be expressed as a function of the thermodynamic voltage u_T and the Inversion Factor, as in Equation 2.12.

$$V_{DSAT} = u_T \cdot \left(2 \cdot \sqrt{I_F + 4}\right) \tag{2.12}$$

Some blocks, and particularly current mirror, active-load and switches, find the pinch-off saturation region suitable. This operating region reduces the current error with the variation of the drain voltage and limits this error to a few percent. The output conductance g_{DS}, given in Equation 2.13, is part of the possible constraints that would be set in the case of transistor level design of amplifiers [164].

$$g_{DS} = \frac{I_D}{L \cdot V_A} \tag{2.13}$$

The above considered output conductance g_{DS}, relies on the bias conditions through the drain current V_A, the device sizing through it's length and a single process parameter V_A representing the early voltage. This condition is very often used to determine the length of the device, such as per Equation 2.14.

$$L = \frac{I_D}{g_{DS} \cdot V_A} \tag{2.14}$$

Having introduced the notion of transconductance in Equation 2.9, and output conductance in Equation 2.13, both actually apply into a small signal model for linear analysis statically ; it is given by Equation 2.13.

$$i_d = \frac{dI_D}{dV_G} \cdot v_g + \frac{dI_D}{dV_s} \cdot v_s + \frac{dI_D}{dV_D} \cdot v_d = gm \cdot v_g - n \cdot v_s + g_{DS} \cdot v_{ds} \tag{2.15}$$

This can then be represented as per Figure 2.7 with the transconductance and output conductance. One can observe in this figure the position of some capacitance are ignoring the junctions capacitance.

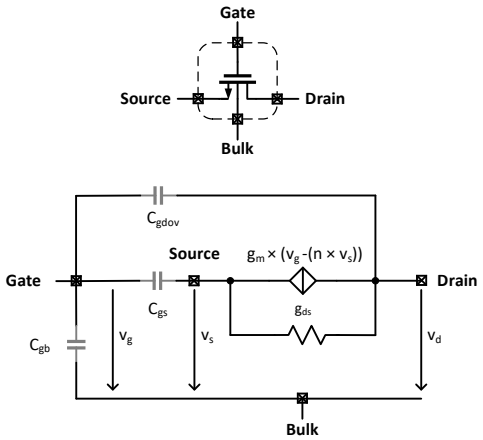


Figure 2.7: Simplified Equivalent small-signal model

I The capacitance C_{GS} is kept and expresses as Equation 2.16, with the assumption that in the saturation conditions, the reverse current is negligible compared to $\frac{1}{4}$, and thus the gate to drain capacitance C_{GD} is negligible.

$$C_{GS} = C_{OX} \cdot W \cdot L \cdot \frac{2}{3} \cdot \frac{\left(\sqrt{I_F + \frac{1}{4}} + 1\right) \cdot \left(\sqrt{I_F + \frac{1}{4}} - \frac{1}{2}\right)}{\left(\sqrt{I_F + \frac{1}{4}} + \frac{1}{2}\right)^2} \tag{2.16}$$

Nevertheless, the gate to bulk capacitance C_{GB} is kept as shown in Equation 2.17.

$$C_{GB} = C_{OX} \cdot W \cdot \frac{n-1}{n} \cdot (1 - C_{GS}) \tag{2.17}$$

The consideration of the overlap capacitance implies considering the gate to drain capacitance C_{GD} as in Equation 2.18.

$$C_{GD_{OV}} = W \cdot \left[C_{OX} \cdot W \cdot L \cdot \frac{2}{3} \cdot \left(1 - \frac{\left(\sqrt{I_F + \frac{1}{4}}\right)^2 + \left(\sqrt{I_F + \frac{1}{4}}\right) + \left(\frac{1}{2} \cdot \left(\sqrt{I_R + \frac{1}{4}}\right)\right)}{\left(\sqrt{I_F + \frac{1}{4}} + \sqrt{I_R + \frac{1}{4}}\right)^2} \right) \right] \tag{2.18}$$

An interesting part of these formulations is that these capacitance all rely on one single process parameter, the gate oxide capacitance C_{OX}, and then upon sizing and transistor inversion level. Having introduced the small signal model it is important to provide the transistor level linear analysis of intrinsic gain defined as the ratio of the transconductance to it's output capacitance, as per Equation 2.19, and the gain bandwidth product or Transit frequency which is defined as the frequency to which the transistor current gain becomes a unity, as per Equation 2.20.

$$A_i = \frac{g_m}{I_D} \cdot L \cdot V_A \tag{2.19}$$

$$F_T = \frac{g_m}{2 \cdot \pi \cdot (C_{GS} + C_{GB} + C_{GD})} \tag{2.20}$$

The above provides an almost complete picture of the transistor sizing trade-off, and this leaves us with the need to extract only 5 parameters that are depending on the technology node chosen. Table 2.1 provide this parameter list after introducing the minimal gate length which designates the technology node. Nevertheless, two second-order limitations were not accounted for yet, the Mismatch and the Noise in circuits. The intrinsic transistor noise is related to local random fluctuations of the carrier velocity or density. The propagation (amplification, attenuation, shaping) of these fluctuations in circuits depends on architecture, nevertheless the source can be modeled as spectral density of the drain current or gate voltage fluctuation, as shown in Figure 2.8.

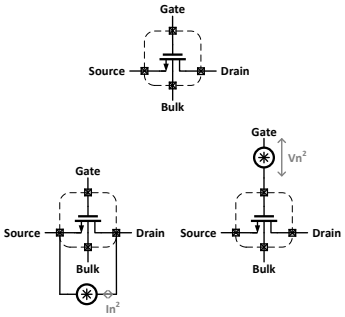


Figure 2.8: Intrinsic Noise Spectral density could be expressed as Current or Voltage fluctuation.

As every active dissipation process has called thermal or white noise, according to [165], the gate voltage thermal fluctuation spectral density could be approximated as per Equation 2.22, and the drain current thermal fluctuation spectral density could be approximated as per Equation 2.22.

$$I_n^2 = 4 \cdot k \cdot T \cdot G_n = 4 \cdot k \cdot T \cdot \gamma \cdot g_m \tag{2.21}$$

$$V_n^2 = \frac{I_n^2}{g_m^2} = 4 \cdot k \cdot T \cdot R_n = \gamma \cdot \frac{4 \cdot k \cdot T}{g_m} \tag{2.22}$$

Both spectral densities can refer to an equivalent noise resistance: R_n in the case of voltage fluctuation density, or a noise conductance in the case of current fluctuation density G_n. Both expressions are valid if the transistor operates in saturation, and both magnify the noise excess factor (2.24.) which takes into account the two partially correlated noise currents that are the channel noise and the induced gate noise [166]. This factor is purely depending on the inversion level so there is no further parameter to be extracted.

$$\gamma = n \cdot \frac{1}{1 + i_f} \cdot \left(\frac{1}{2} + \frac{2}{3} \cdot i_f \right) \tag{2.23}$$

When including the Flicker or colored noise process, the resistor R_n is reconsidered as Equation 2.24. Two more parameters are included the Flicker noise coefficient; K_F and the Flicker noise exponent A_F, which is an empirical model and often considered as an oversimplification. Nevertheless most of the standard simulation tools include it and the coefficient can be directly

picked-up from the device model card.

$$R_n = \frac{\gamma}{g_m} + \frac{\frac{K_F^{A_F}}{4 \cdot k \cdot T \cdot C_{ox}^2}}{W \cdot L \cdot f} \tag{2.24}$$

The voltage, and current processing blocks such as differential pair or current mirror [167] has limitation due to local mismatch. Mismatch and Noise are both fluctuations, however the mismatch happens from a local silicon area to another, while the noise is a time series. The mismatch affects both mobility and threshold voltage [168] such as expressed in Equation 2.25.

$$\triangle V_g = \triangle V_T - \frac{I_D}{g_m} \cdot \frac{\triangle \beta}{\beta} \tag{2.25}$$

Equation 2.25, can be derived to obtain the variance, it is interesting to note the bias dependency inserted with $\frac{I_D}{g_m}$

$$\triangle V_g = \sqrt{\sigma_{V_T}^2 + \left(\frac{I_D}{g_m} \cdot \sigma_\beta^2\right)} \tag{2.26}$$

$$\sigma_{V_T} = \frac{A_{V_T}}{\sqrt{W \cdot L}} \tag{2.27}$$

$$\sigma_\beta = \frac{A_\beta}{\sqrt{W \cdot L}} \tag{2.28}$$

These various observations show that there are only two independent variables for transistor level design : The first one is the inversion factor level and the second one is the transistor gate length. The most common transistor level design receipt [145, 146, 148] would actually lead to a choice of the inversion level and gate length. These choices come from a higher level of specification which applies to the considered architecture and applies at least two constraints on each transistor. The above form the basis of our methodology for the design of frequency references and references at large.

2.1.2 Hand-calculation parameter extraction methodology

Table 2.1 shows the process parameters used for hand-calculation presented in subsection 2.1.1.

Table 2.1: Summary of the process parameter to be extracted for transistor level sizing within the $\frac{g_m}{I_D}$ and sub-threshold design framework.

Name	Symbol	Unit
Technology Node	L_{min}	m
Specific Current	$I_{SPEC_{\blacksquare}}$	A
Threshold Voltage	V_T	V
Sub-threshold slope Factor	n	$-$
Early voltage	V_A	Vm
Gate voltage Oxide	C_{ox}	F
Threshold Voltage Mismatch	A_{V_T}	$\frac{mV}{\mu m^2}$
Mobility Mismatch	A_β	$\frac{\%}{\mu m^2}$

These parameters are extracted one after another. It is usual to extract them from a sign-off simulation. However, they could also be extracted from measurements. Since the threshold voltage and sub-threshold slope requires Pinch-off Voltage Characteristic swept over the gate voltage, the first step for extraction is then the Specific current. The Pinch-off Voltage Characteristic swept over the gate voltage is then simulated to obtain the Threshold voltage and slope factor. The early voltage is obtained by a simulation of the output characteristic. Finally, an AC simulation is made in order to extract the gate oxide capacitance.

2.1.2.1 Specific current extraction

The specific current could be extracted from the expression of the saturated drain current in strong inversion, given per Equation 2.29.

$$I_D = \frac{I_{SPEC_{\blacksquare}} \cdot \frac{W}{L}}{4 \cdot u_T^2} \cdot \left(V_p - V_s\right)^2 \tag{2.29}$$

It follows that the derivative of the current with respect to its source voltage corresponds to the square root of the specific current and some scaling parameter for the geometry aspect ratio of the device and thermodynamic voltage, as shown in Equation 2.30.

$$\frac{\partial \sqrt{I_D}}{\partial V_s} = \frac{\sqrt{I_{SPEC_{\blacksquare}} \cdot \frac{W}{L}}}{2 \cdot u_T} \tag{2.30}$$

How to extract the drain current as a function of a sweep of the source voltage in strong inversion and saturation is proposed in the schematic of Figure 2.9.

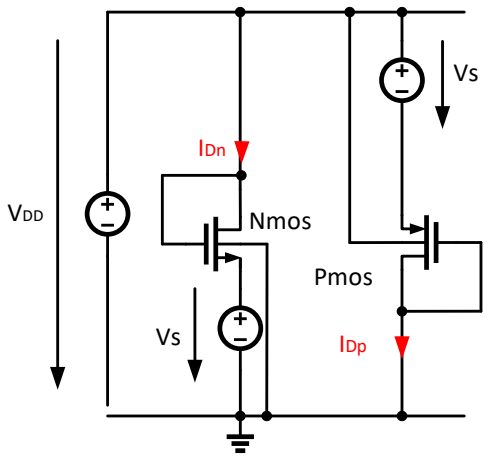


Figure 2.9: Circuit ensuring Strong inversion and saturation conditions while sweeping the transistor source voltage.

We can then observe the drain current as a function of the swept value of the source voltage. The figure presents the derivative of the drain current and it's derivative (slope) with respect to the swept source voltage. The practical aspect shows that the slope is not a constant and thus the specific current is taken for the maximal slope coefficient. According to the definition (2.30) the specific current is then given in Equation 2.31.

$$I_{SPEC_{\blacksquare}} = \left[2 \cdot u_T \cdot \max\left(\frac{\partial\sqrt{I_D}}{\partial V_s}\right)\right]^2 \tag{2.31}$$

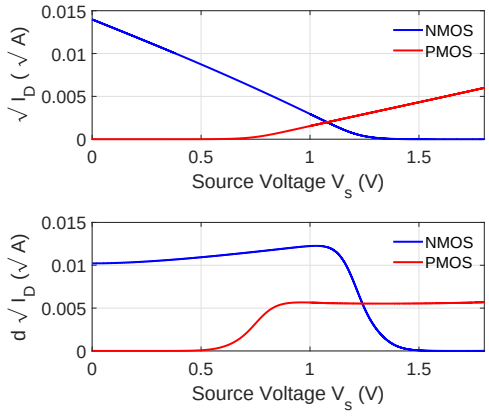


Figure 2.10: Intrinsic Noise Spectral density can be expressed as Current or Voltage fluctuation.

The specific current corresponds to a well defined operating point on the DC transfer char-

acteristics of an MOS transistor, right at the frontier between the weak and strong inversion. Thus, another extraction principle that could apply at circuit level is to compare a specific property of the respective modes of operation into a feedback loop. The proposed approach in [169] relies on the channel voltage property as per Equation 2.32.

$$v_{ch}(x, L, I_F) = 2 \cdot u_T \cdot \ln\left(e^{\sqrt{I_F}} - 1\right) - 2 \cdot u_T \cdot \ln\left(e^{\sqrt{I_F \cdot \left(1 - \frac{x}{L}\right)}} - 1\right) \tag{2.32}$$

Figure 2.11, presents plots of Equation 2.32. A possible way to measure physically the channel voltage is to split the transistor into a string having the same width but the length would be divided by their multiple. So, for instance, in Figure 2.11, our interest is to look at the quarter of channel length thus we split it into 4 transistors and plotted 3 tap voltage nodes.

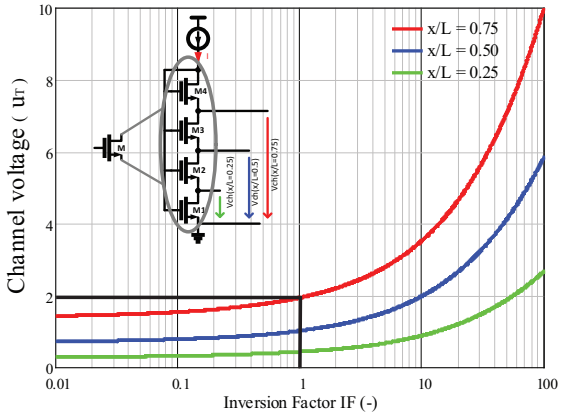


Figure 2.11: Channel Voltage as a function of the position and inversion level.

There is a remarkable value which is two thermodynamic voltages; this value is obtained for an inversion factor (e.g. level) of 1 at the transistor length tap $0,75 \cdot L$. Another important observation is that the various taps found themselves being parallel curves toward the weak inversion and strong inversion levels. This property could be leveraged to have a single operating point within a loop. The structure proposed in [169] is reported in Figure 2.12, and some further details and use-cases of the ratiometric design applied to analog techniques for neural network implementation were proposed in Pascal Heim's Ph.D Dissertation (appendix B).

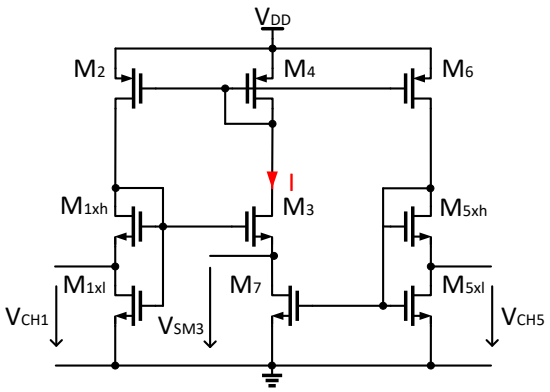


Figure 2.12: Specific Current Extractor Circuit.

This circuit technique extracts a current that is representative of the specific current. As a per-requisite, M1 should operate in weak inversion and M5 in i strong inversion. In order to keep a constant geometrical aspect ratio the current mirror formed by transistors M2 and M4 have an aspect ratio such that $\frac{W_{M4}}{L_{M4}} = \frac{W_{M2}}{L_{M2}} \cdot N$, and $\frac{W_{M8}}{L_{M8}} = \frac{W_{M4}}{L_{M4}} \cdot M$ where M and N are integers, and the current then scales with respect to the median branch current I. The source voltage of the transistor M3 equates with the channel voltage or transistor M1 $V_{SM3} = V_{CH1}$, by imposing $W_{M3} = W_{M1xh} \cdot N$. When imposing $L_{M7} = L_{M5xl} \cdot M$, the drain voltage of transistor M7 becomes $V_{SM7} = V_{CH5}$. Imposing a product $N \cdot M \geq 100$, would limit the sensitivity to the threshold voltage mismatch. The spice simulation offers the possibility to simulate ideal component and equation, therefore using "Current controlled current source to replace current mirror" and "Voltage controlled voltage source" to impose voltage one could think of re-using the above circuit technique to extract the specific current as shown in Figure 2.13. The same technique is applied for PMOS devices.

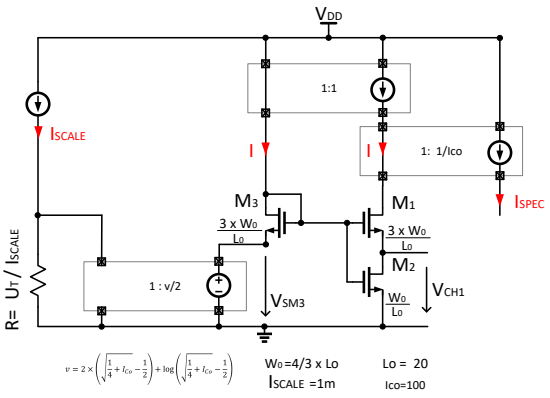


Figure 2.13: Specific Current Extractor using spice simulation.

Such a circuit is based on the physical properties of transistors M1, M2 and M3, however the

Matching issue of various current mirrors disappears and the inversion level of the branch M1, M2 is set by imposing the source voltage condition to M3. Both extraction techniques were used in the section 2.1.2.5, to crosscheck the obtained results.

2.1.2.2 Threshold voltage and sub-threshold slope

Having extracted the Specific current value, it is possible to extract the threshold voltage from the pinch-off voltage characteristic. As shown in Figure 2.1.2.5, one can observe the pinch-off voltage by imposing half the specific current biasing current and a diode connection. Additionally it is required to sweep of the gate voltage such as presented in [170] to obtain The Pinch-off Voltage Characteristic swept over the gate voltage : $V_P = f(V_G)$.

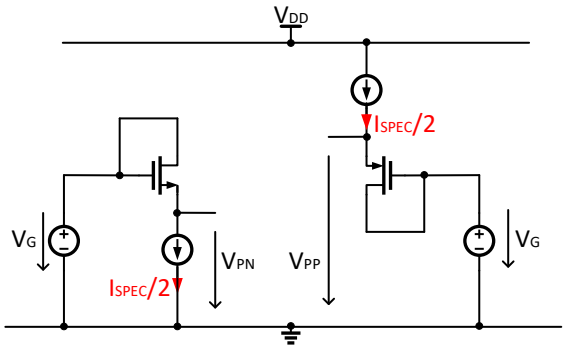


Figure 2.14: Specific Current Extractor using spice simulation.

An approximation of the pinch-off voltage proposed in Equation 2.8 considers that when the Pinch-off voltage cancels the gate voltage the threshold voltage $V_P = f(V_G)$.

$$\frac{V_G - V_T}{n \cdot u_T} = 0 \rightarrow V_G = V_T \tag{2.33}$$

The same Equation 2.34, shows that when deriving with respect to the gate voltage it provides directly the value of the inverse of the sub-threshold slope factor n.

$$\frac{\partial \frac{V_G - V_T}{n \cdot u_T}}{\partial V_G} = \frac{1}{n} \tag{2.34}$$

Figure 2.15, shows the simulated characteristics of the circuit presented in Figure 2.14. The first subplot is simply the $V_P = f(V_G)$ electrical simulation from which the threshold voltage extraction is straightforward. Normalizing the simulated pinch-off voltage to the thermodynamic voltage u_T, then, as suggested in Equation 2.34 plotting the inverse of the derivative

provides the sub-threshold slope factor n. We can see that the following is not constant and the maximum value is picked. The computed values above the threshold are not worth considering since this parameter translates the sub-threshold current slope of drain current as a function of the gate voltage.

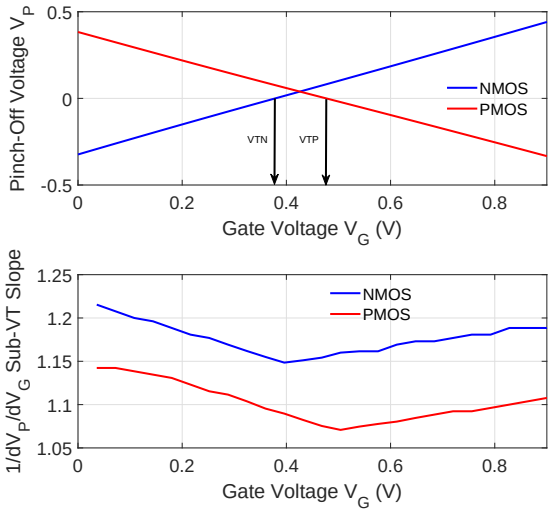


Figure 2.15: Electrical simulation of the pinch off characteristic $V_P = f(V_G)$

2.1.2.3 Output conductance and Early Voltage

The output conductance is measured as the output transistor characteristic; drain current as a function of the drain voltage for a given gate voltage, as shown in Figure 2.16.

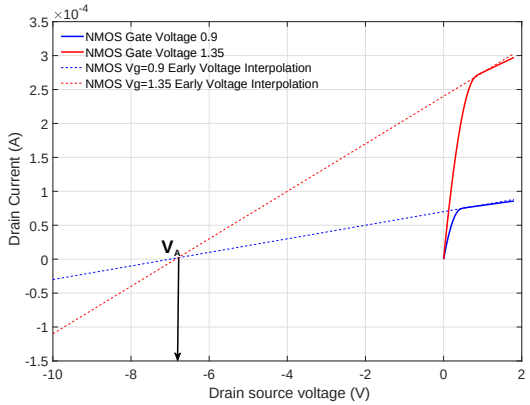


Figure 2.16: Electrical simulation of the Imaginary part of the gate current

A practical observation is that the fitting curves end up crossing the same point in abscissa. This point defines the Early Voltage, as can be observed in the figure. It naturally, from the

electrical measurements, gets defined as the drain current derivative with respect to the drain current, such as in Equation 2.35.

$$V_A = I_D \cdot \frac{\partial V_{DS}}{\partial I_D} \tag{2.35}$$

The extraction of this value requires a DC simulation such as shown in the schematic in Figure 2.17. Where it is imposed, there is an inversion level through the saturated diode of the current mirror for both PMOS and NMOS.

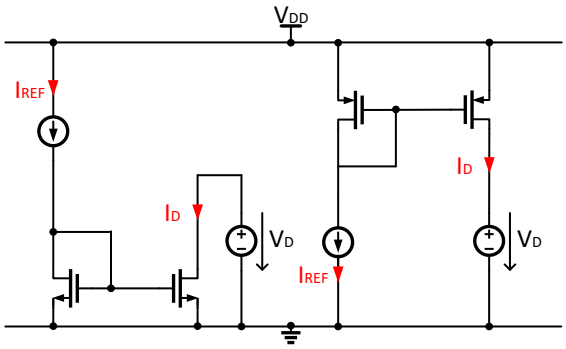


Figure 2.17: Electrical schematic for measuring output conductance imposing inversion level

From the compact model point of view there is no continuous definition that holds. A fitting function or approximation is proposed in [171] such that the output conductance is given per Equation 2.36.

$$gds = \frac{I_D}{V_A \cdot L} = \frac{I_F \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W}{L}}{V_A^{'} \cdot L} \tag{2.36}$$

This single parameter for modeling of the output conductance is quite relevant for covering most of the effect. Nevertheless while comparing the expression and an actual simulation, a characteristic discrepancy is observed when getting to strong inversion with inversion level.

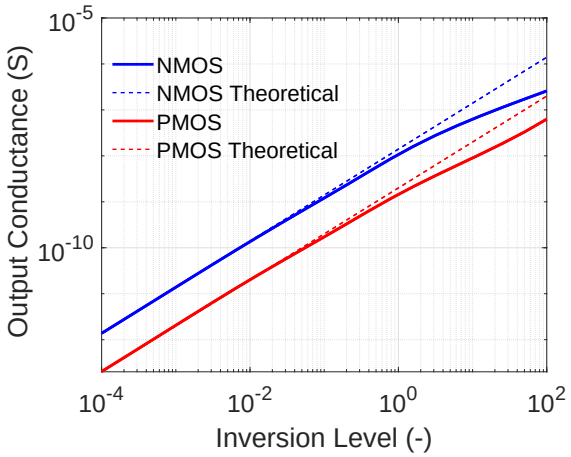


Figure 2.18: Theoretical output conductance as a function of the inversion level

This limitation could often lead to iteration between the simulator and hand-calculation evaluation, especially as the phenomenon is strengthening with the technology scaling such as observed in 28nm BULK in [171]. However for the weak to moderate inversion, the model remains a good fit, and considering the advance process limitation to bias in strong inversion, this model is satisfying.

2.1.2.4 Gate oxide capacitance

Capacitor impedance is usually defined in the sinusoidal regime such as the imaginary part of the impedance is $X_C = I_M\left(\frac{j}{C\cdot\omega}\right) = -\frac{j}{C\cdot\omega}$, thus imposing a sinusoidal voltage of unit amplitude on top of it's DC component, as shown in Figure 2.19. The measure of the gate capacitance value, is obtained as the imaginary part of current, and given that the pulsation is imposed to be $\omega = 1$ rad/s, the result is direct.

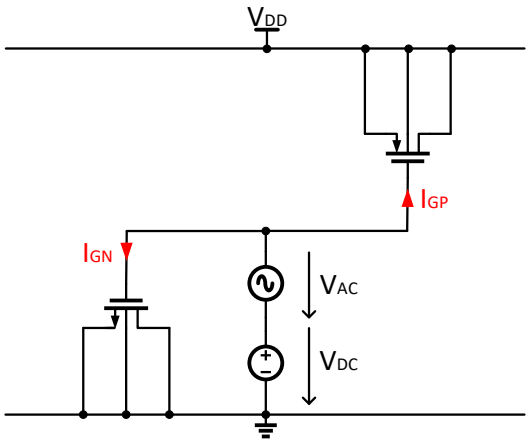


Figure 2.19: Electrical simulation or measurement schematic of the gate capacitance

The gate oxide capacitance must be extracted in strong inversion and saturation since the channel is pinched off and therefore the effective capacitance is not biased by other conduction.

$$C_{OX} = \lim_{abs(V_{Gx}-V_{Sx})\to V_T} I_M\left(\frac{\partial I_{Gx}}{\partial V_{Gx}}\right) \tag{2.37}$$

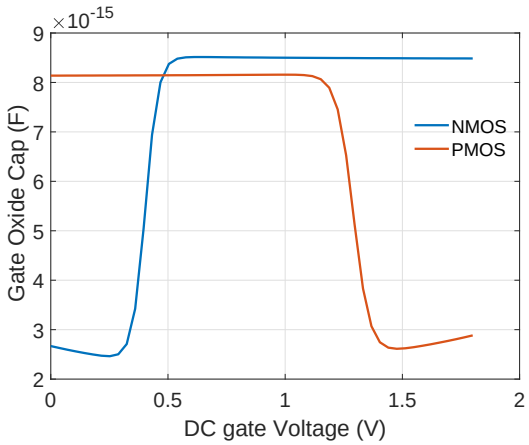


Figure 2.20: Electrical simulation of the gate capacitance

2.1.2.5 Application to various processes

The above parameter extraction techniques were applied to an available Design Kit using BSIM models for both submicron technology in Table 2.2.

Table 2.2: Summary of the process parameters to be extracted for transistor level sizing within the $\frac{g_m}{I_D}$ and sub-threshold design framework on the core device in submicron technology.

Name	Symbol	Unit	TSMC	TSMC	TSMC	TSMC
Technology Node	L_{min}	m	180	180	90	90
Device Type	P/N	core	Nmos	Pmos	Nmos	Pmos
Specific Current	I_{SPEC}■	nA	434	111,2	536,8	233,3
Threshold Voltage	V_T	mV	432,4	415,5	256,6	226,8
Subthreshold Slope Factor	n	–	1,23	1,27	1,14	1,09
Early Voltage	V_A	V	16,81	15,33	6,98	3,13
Gate Oxide Capacitance	C_{ox}	fF	8,88	8,79	12,00	11,33
Threshold Voltage Mismatch	A_{V_T}	$V\cdot\mu m$	5,10	5,49	3,50	2,59
Mobility Mismatch	A_β	$\%\cdot\mu m$	1,04	0,99	1,04	0,99

Applying the same extraction procedure to a deeply scaled process node we obtain the results summarized in Table 2.3.

Table 2.3: Summary of the process parameters to be extracted for transistor level sizing within the $\frac{g_m}{I_D}$ and sub-threshold design framework on the core device in deeply scaled technology.

Name	Symbol	Unit	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC
Technology Node	L_{min}	m	65	65	40	40	28	28
Device Type	P/N	core	Nmos	Pmos	Nmos	Pmos	Nmos	Pmos
Specific Current	I_{SPEC}■	nA	504,5	190	591,1	242,3	811,6	240,5
Threshold Voltage	V_T	mV	280,2	282,9	310,7	365,6	317,9	426,6
Subthreshold Slope Factor	n	–	1,10	1,07	1,16	1,10	1,07	1,074
Early Voltage	V_A	Vm	5,71	2,59	11,78	13,83	12,08	34,07
Gate Oxide Capacitance	C_{ox}	fF	12,88	12,09	14,48	12,68	17,89	19,33
Threshold Voltage Mismatch	A_{V_T}	$V \cdot \mu m$	2,1	2,2	1,01	1,06	1,02	1,03
Mobility Mismatch	A_β	$\% \cdot \mu m$	0,87	0,86	NA	NA	NA	NA

The above parameters consider long channel model with gate length of $1\mu m$, and assuming saturation which slightly biases the comparison of the parameters if used in their deeply scaled form where the short channel effects would appear. The above parameters form the basis of our methodology for the design of frequency references and references at large. Once these parameters are set, they actually provide a reliable instrument for an effective early-stage phase of the original design point.

2.2 Mismatch and corner-device conduction

Shallow Trench Isolation (STI) region structure is used in the state-of-the-art CMOS process as it is compliant for high-density applications such as SRAM and DRAM [172]. This is because it has near zero field encroachment, better planarity, latch-up immunity, and low junction capacitance [168]. However, STI has a disadvantage regarding device characteristics. The steep

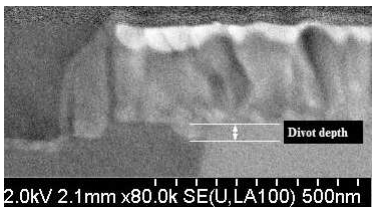


Figure 2.21: STI Corner / Divot transistor Scanning Electron Microscopy picture

slope of the silicon (Si) sidewall adjacent to an STI structure results in a "corner poly divot" that forms a "corner device." This can be observed in the Scanning Electron Microscopy shown in Figure 2.21. The corner device is enhanced in case of a flash process which introduces an additional etching step that produces a deeper STI divot. The fringing gate fields at the STI edge strengthen carrier inversion, thus creating a parallel conduction corner channel with a lower threshold voltage than that of the center channel, resulting in the so-called sub-threshold “hump.” The drain current as a function of the gate voltage usually observed in saturation are so-called “I-V characteristics.” An illustration of such an electrical signature is

shown in Figure 2.22. The drain current as a function of the gate voltage sweep from zero to drain voltage can be observed, and it's also convenient to look at the first derivative, which is the transconductance; it was normalized to the drain current, providing a figure of merit of the device.

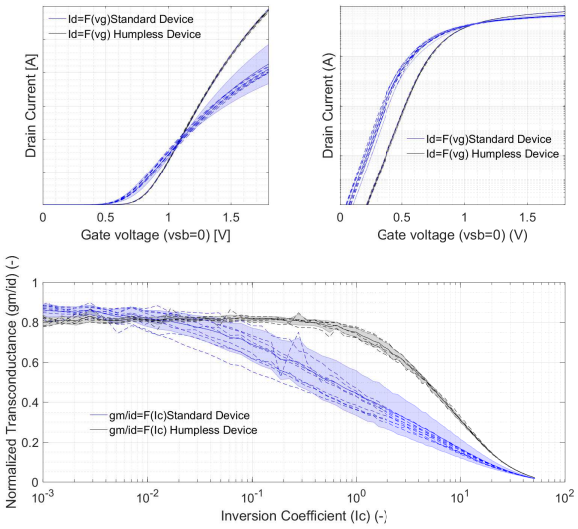


Figure 2.22: Electrical signature of STI Corner / Divot transistors

Such a sub-threshold hump characteristic increases standby currents [173] but also gate voltage mismatch, as can be observed in Figure 2.22. Various corner rounding, gate layout, and doping techniques have been used to minimize the effect, such as multi-finger [174], enclosed gate layout techniques [175, 176, 177], and some others have proposed doped devices. Improvement of hump effects with controlled Fermi level by changing doping concentration of gate-poly solutions was introduced in 2008 [178]. Such gate doping is in practice counter doping of a tiny part meaning that mask alignment and implantation angle are critical, as reported in [178, 177]. The mask alignment issue is due to enhanced diffusion of impurities in the polysilicon grains and joints; the control of the oppositely doped zone is unreliable and limits the minimum area that can be implanted, and hence the minimum width of a transistor. A corner over-doping procedure with additional spacers to align masks was proposed in [179], while a self-aligned corner doping was recently introduced and showed the advantageous effect on gate mismatch in circuits [180] as well as for low-frequency noise [181]. A study of sub-threshold CMOS edge conduction was extended from devices to circuits. The electrical DC characterization of the effect is presented in the section 2.2.1.1. It shows that the sub-threshold gate voltage mismatch blows-up drastically and current compact models are not able to catch the STI hump transistors effect on matching characteristics.

While processing devices that are significantly immune to the STI hump transistors, their matching characteristics improve. Although they improve, narrow transistors remain the more sensitive to the sub-threshold hump effect. The enclosed layout techniques do not scale much

but are of interest for large and long devices. The development of EKV3.02 enables the catching of the STI hump transistors effect and provides insight for designers on the variability of the produced circuit with better confidence in sign-off verification. The case of ring-oscillator is explored in section 2.2.2.1 to advocate for special care while selecting a technology for sub-threshold variability and hump effect. Some publications show the significance of an accurate initial delay or frequency [182, 183] in application with phase locked loop and time to digital conversion. The factor 8 observed on frequency variability is slightly higher than expected due to the long tail random process phenomenon. Although the model proposed by Equation 2.50 of the frequency model is quite simplified, it is in line with silicon measurements and simulations.

2.2.1 Comparison of gate voltage mismatch at device level and models

The measurements are carried out on a standard differential pair to make a comparative assessment of the gate voltage mismatch for standard, enclosed gate layout, and corner-doped transistors. The analysis of gate voltage mismatch requires an extraction method of the threshold voltage. Some would propose extrapolated Vth, others would recommend using conventional max gm method and drawn L and W. The most accurate way suggested in JDEC standard JESD28-A is the Vth extraction method based on fixed current; that current calculated by EKV specific current at inversion factor.

2.2.1.1 Compact model for the local mismatch

Originally, the modeling of matching effect was focused on the mismatch of mos capacitance [184]. At the time, precision analog filters could be realized by using a switched capacitor as a resistor equivalent. The accuracy of the filter is then decided by the matching of capacitors and not by the absolute value of any element. It was later extended to the NMOS capacitor and current sources [185]. It was later observed in PMOS and NMOS cases that the mismatch is inversely proportional to the square root of the area [186]. A further extension added spatial dependence to mismatch to describe local and global variations [187]. Having extended this Carrier fluctuation theory, the effect on precision circuits such as bandgap, analog to digital converter [167, 188, 189] demonstrated a fundamental interest at mismatch properties. The corner device effect was attempted in the release in 2011 of EKV3.0 [190]. The model attempts modeling of Mismatch accounting for the STI divot effect on the mismatch, with an extra set of 3 parameters. The parts of the channel that are on the sides of the channel are characterized by different properties concerning the middle and central part of the channel, forming this way some parallel devices to the main one. This device, having a lower pinch-off voltage (DPHIEDGE), thus lowers threshold voltage, and body effect coefficients (DGAMMAEDGE) make their appearance sooner in weak inversion. But, since their width is a portion of the whole device, in strong inversion they can hardly be noticed. This parallel combination forms a step-shaped curve in weak inversion, with the current in logarithmic scale. The summed width of the two edge devices is given to the WEDGE. Later an extension of BSIM6 showed accurate results [191]. Recently the EKV 3.02 was developed and is still at the step of a verilogA

model to account for the biasing dependence of mismatch coefficients for circuit design. This physics-based model is still under development and remains unpublished ; a brief description is provided in section 2.2.1.2. Figure 2.23 presents measured NMOS gate voltage mismatch of 25 sites across wafers, for standard silicon devices as well as transistors with improved immunity to the STI divot effect. Device dimensions cover the four geometry corners : Narrow-Short, Wide-Short, Narrow-Long, and Wide-Long. Simulation results obtained with EKV 3.0 and EKV 3.02 are shown in the same graphs. EKV 3.02 adds random dopant fluctuation of the parasitic edge transistors and thus nicely catches the hump effect on gate voltage mismatch in the sub-threshold. The coverage of geometry is also appreciable. Note that this is in general a quite challenging undertaking, due to the exponential behavior of drain current in weak inversion, combined with the strong geometry, and bias dependence of the edge conduction effect. Furthermore, the interaction among the mismatch of the center transistor and the edge conduction must also be kept in mind. The same simulation and measurement conditions are used for gate voltage mismatch of PMOS devices, shown in Figure 2.24.

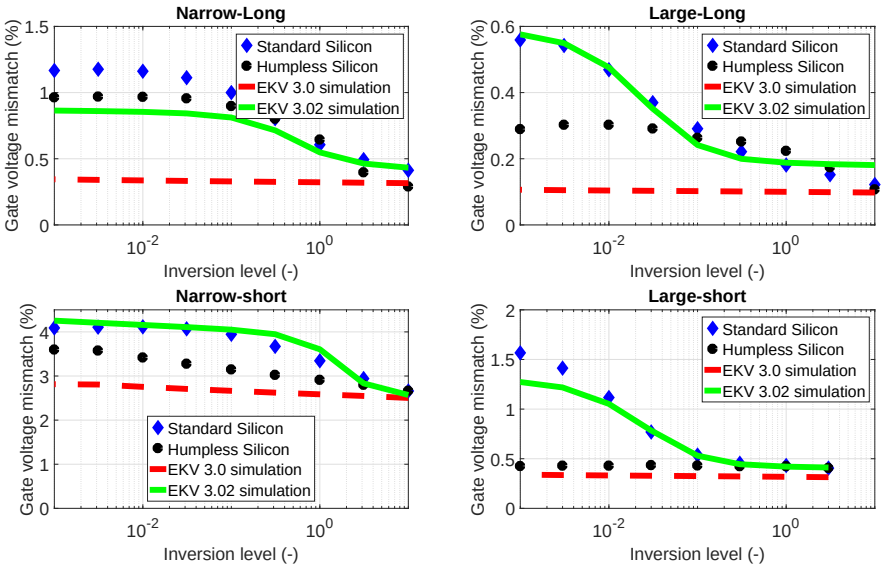


Figure 2.23: Relative degradation of gate voltage mismatch in weak inversion for NMOS transistors, both sensitive to STI divot and immune, together with simulation using charge-based compact models EKV3.0 and EKV3.02

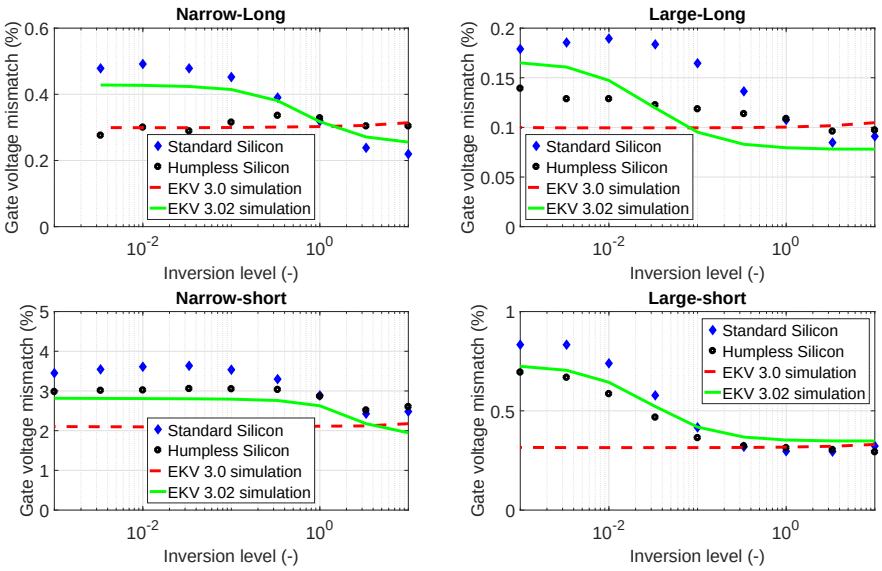


Figure 2.24: Relative degradation of gate voltage mismatch in weak inversion for PMOS transistors, both sensitive to STI divot and immune, together with simulation using charge-based compact models EKV3.0 and EKV3.02

For the PMOS devices, similar behavior as in the case of NMOS is observed, both in measurement and simulation. Figure 2.23 and 2.24 also provide a comparison of the gate voltage mismatch for standard and hump-less transistors. Figure 2.23 shows that corner-doped NMOSs have in general improved sub-threshold gate voltage mismatch characteristics, except for narrow and long transistors, which are of a particular interest when low current and sub-threshold is required. Figure 2.24 shows that hump-less PMOSs have an improved sub-threshold gate voltage mismatch, including for narrow and long devices.

2.2.1.2 EKV3.02 for circuit design

Recently the EKV 3.02 model [192] was developed to account for the bias-dependence of gate voltage mismatch degradation for circuit design. The charge-based EKV 3.0 code version was used as a basis for EKV 3.02. The code used in the present work is based on Verilog-A. It incorporates a statistical model that covers the variability of the edge-conductance effect. In every Monte-Carlo iteration, a deviation is added to targeted parameters in order to induce the statistical variability of the edge device. The variability of the hump transistor's body effect, γ_{EDGE} , is covered by

$$\Delta\gamma_{EDGE} = \frac{A\gamma_{EDGE}}{\sqrt{WL}}$$

where $A\gamma_{EDGE}$, is a statistical model parameter. The following equation is used in order to perform statistical deviation of the edge transistor's pinch-off voltage.

$$\Delta\delta\Phi_{EDGE} = A\delta\Phi_{EDGE} \cdot \sqrt{\left(\frac{\frac{P1_{EDGE}}{\sqrt{W}} + P2_{EDGE}}{\sqrt{L}}\right)^2 - \frac{std^2}{WL}}$$

$A\delta\Phi_{EDGE}$ is the statistically deviated parameter. $P1_{EDGE}$, and $P2_{EDGE}$, are used for the geometrical scaling and std is directly connected with the standard deviation of threshold voltage. This model will be applied to the circuit investigation made in the next subsection.

2.2.1.3 A comparative sub-threshold mismatch comparison of standard, enclosed gate layout and Corner doped device

In section 2.2.1.1, the bias dependency of different sizes of standard and corner doped devices was observed. One of the major goals of this section is the assessment of MOST with improved local mismatch performance in ultra low-current region. The presented results of local mismatch measurements on differential pairs of standard devices, enclosed gate layout and Hump-less PMOS and NMOS transistors, have been extracted at fixed current levels to ensure the biasing conditions for deep sub-threshold operation (e.g. IC=0.001). Mismatch has been measured on 52 sites of one wafer. Figure 2.25(a) presents the standard deviation of gate voltage mismatch of NMOS devices, based on measurements of standard, enclosed gate layout, and Hump-less devices, respectively. It can be observed that enclosed gate layout transistors (red triangle) and Hump-less transistors (black circle) have similar mismatch characteristics but cannot scale as much as conventional layout devices. The AVT lines show almost a factor 3 improvement of the gate voltage mismatch. Both Hump-less transistors and enclosed gate layout, have comparable gate voltage mismatch characteristics.

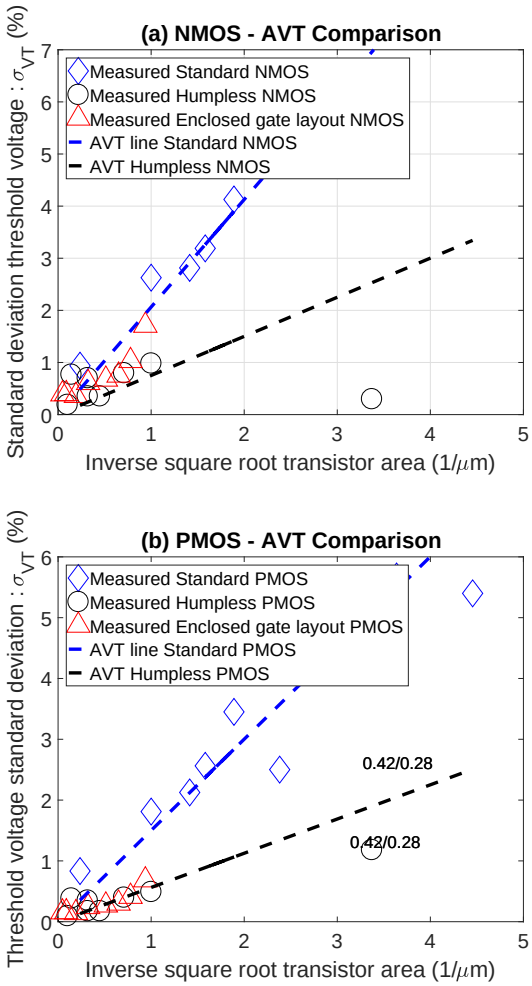


Figure 2.25: Comparative sub-threshold gate voltage mismatch standard deviation as a function of the Inverse square root of the NMOS gate area for standard, enclosed gate layout and Corner-doped transistors.

Although the selected layout for manufacturing of enclosed gate layout transistors cannot scale the gate area lower than a square micrometer, most of the benefits are obtained when transistor width is greater than a micrometer. Figure 2.25(b) presents the standard deviation of gate voltage mismatch of PMOS devices based on measurements of standard, enclosed gate layout, and Hump-less devices. It can be observed that enclosed gate layout transistors (red triangle) and Hump-less transistors (black circle) have similar mismatch characteristics but cannot scale as much as conventional layout devices either. While scaling the gate area, PMOS could encounter slightly better gate voltage mismatch performance, particularly in the case of narrow devices which is a favorable sizing for low current, low inversion level operation. The most benefits are obtained when transistor width is greater than a micrometer.

2.2.2 Circuit level investigations

2.2.2.1 The CMOS ring oscillator sensitivity to gate voltage mismatch

The most common building blocks of circuits encountered in integrated circuits are probably the CMOS inverters; many examples are provided in Fig.2.26.

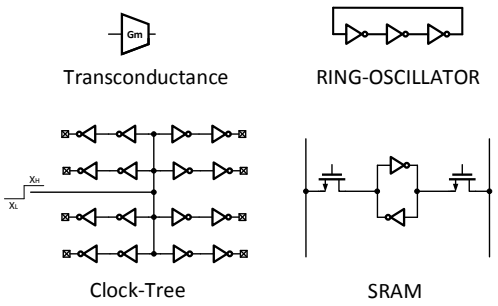


Figure 2.26: Circuits based on CMOS Inverter

Among the different circuits, frequency generation finds particular interest in the ring oscillator which is the most common process control and monitoring circuit available. Different strategies can be adopted depending on the objective of the measurement. In our context of local mismatch, the variation in transistor threshold voltage is the most influential contributor to the measured fluctuations in the frequency of ring oscillators. Thus, a quantitative model of CMOS Inverter as a building block of a ring oscillator is proposed. Some simplifying assumptions are introduced to extract a model of the CMOS inverter delay. The sub-threshold slope factor of PMOS and NMOS devices equal $n = n_p = n_n$ and similarly, the specific currents are the same $I_0 = I_{SPEC_{\blacksquare P}} \cdot \frac{W_P}{L_P} = I_{SPEC_{\blacksquare N}} \cdot \frac{W_N}{L_N}$, and can be realized by up-sizing of the PMOS transistor with respect to the NMOS transistor size.

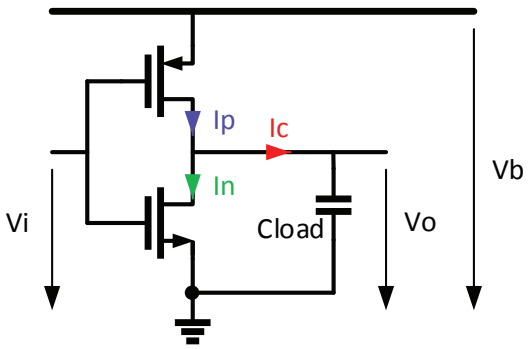


Figure 2.27: CMOS Inverter

The sub-threshold regimes equations of drain current normalized to specific current are

obtained in Equations (2.38) for the PMOS and (2.39) for the NMOS.

$$y_p(x_i, x_o, x_b) = \frac{I_p}{I_o} = e^{\frac{x_b - x_i}{n}} \cdot \left(1 - e^{x_o - x_b}\right) \tag{2.38}$$

$$y_n(x_i, x_o) = \frac{I_n}{I_o} = e^{\frac{x_i}{n}} \cdot \left(1 - e^{x_o}\right) \tag{2.39}$$

The output swing is derived by solving the Equation ob2.40, the swing is theoretically obtained when

$$y_n(x_i, x_o) = y_p(x_i, x_o, x_b) \tag{2.40}$$

Having derived, the swing, it appears clear that in theory above 200mV, the inverter with the same specific current shall not get a degraded swing, after a careful examination of Figure 2.28.

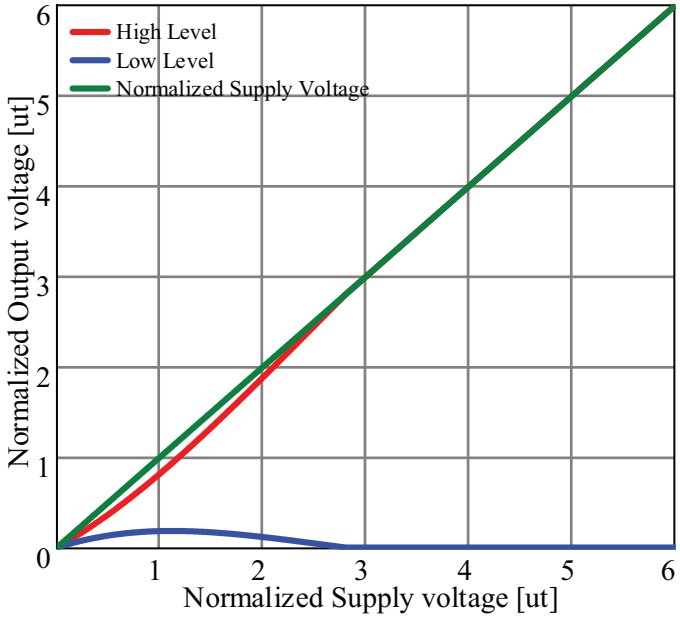


Figure 2.28: CMOS Inverter output swing

Thus, the ultimate parameter limiting speed is the load capacitor, as exposed in Figure 2.27. The normalized current charging or discharging of the capacitor, C_{load}, is expressed as per 2.41. It is assumed that the C_{load} represents the total capacitive load against the reference terminal (either ground or supply). The above load capacitance neglects the gate overlap

capacitance of the transistor.

$$y_c(x_i, x_o) = \frac{I_c}{I_o} = y_p(x_i, x_o, x_b) - y_n(x_i, x_o) \tag{2.41}$$

Additionally

$$y_c(x_i, x_o) = y_p(x_i, x_o, x_b) - y_n(x_i, x_o) \tag{2.42}$$

Since the capacitance voltage current relation could be written as in Equation 2.43, we keep the notation presented in Figure 2.27.

$$I_c(t) = C_{load} \cdot \frac{\partial V_o}{\partial t} \tag{2.43}$$

which provides a solution to the output voltage expression through Equation 2.43.

$$\frac{\partial V_o}{\partial t} = \frac{1}{C_{load}} \cdot I_c(t) \Leftrightarrow V_o(t) = V_o(0) + \frac{1}{C_{load}} \cdot_0 \int^T I_c(t) \tag{2.44}$$

Thus, this fulfills our normalization of the voltage to the thermodynamic u_T such as the input voltage $x_i = \frac{V_i}{u_T}$, of the currents to the specific current I_o such as the pmos current $y_p = \frac{I_p}{I_o}$. We can the characteristic time defined as per Equation 2.45. The output load capacitor C_{load} is integrated into the characteristic time.

$$T_o = \frac{C_{load} \cdot u_T}{I_o} \tag{2.45}$$

Thus, we can use a normalized time, which is the time normalized to a characteristic time as per Equation 2.46.

$$\tau = \frac{t}{T_o} \tag{2.46}$$

The equation can then be used for variable change in Equation 2.47.

$$x_o(\tau) = x_o(\tau) + \int_0^\tau y_c(x_i, x_o)\, \partial\tau \tag{2.47}$$

Equation 2.47, has no closed form solution known to date. Various models were proposed along the years, including the switching delay models such as [193, 194]. Some others based on RC delay models [195] lead to binned solutions depending on various supply and threshold voltage conditions. A common application of the CMOS inverter in digital circuits is to regenerate the clock three levels where they get cascaded ; this inserts a delay and the delay variability has been shown to be critical in [196] . Another interesting bloc is the ring-oscillator which is made of a cascaded chain of inverters with an odd number and the last output is fed back as the first input of the chain. Cascading CMOS inverters, as presented in Figure 2.29, show the propagation delays over the chain; the transitions become standard after a few stages. In a technical report of Prof. Vittoz [197], it was demonstrated using the linearized charge model, that the total amount of charge per stage is either due to the cross-conduction current, or to the transition between two states converging to a constant gap between those values. Therefore, it was demonstrated that the ring oscillator including five stages or more could be modeled.

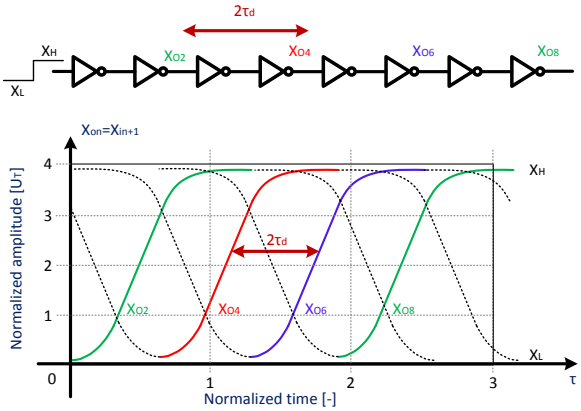


Figure 2.29: CMOS Inverter chain

The normalized standard delay time τ_d, can then be defined as per Equation 2.48. The normalized standard delay time only depends on supply voltage and sub-threshold slope and the threshold voltage. A similar proposition with a binned version of the current was also proposed in [198, 199, 200]. Nevertheless, Equation 2.48, proposes an approximation from the charge linearisation:

$$\tau_d = \frac{T_d}{T_o} = \frac{C_{eq} \cdot V_{DD}}{I_{DPON}} = \begin{cases} \frac{C_{eq} \cdot V_{DD}}{I_0 \cdot e^{\frac{-V_T+(n-1)\cdot V_S}{n \cdot u_T}} \cdot e^{\frac{-V_{DD}}{n \cdot u_T}}} & Weak-Inversion \\ \frac{C_{eq} \cdot V_{DD}}{I_0 \cdot \ln\left(1+e^{\frac{V_{DD}-V_T}{n \cdot u_T}}\right)} & Continious-interpolation \\ \frac{C_{eq} \cdot V_{DD}}{\frac{I_0}{4 \cdot n \cdot u_T^2} \cdot \left(\frac{V_{DD}-V_T}{n}\right)^2} & Strong-Inversion \end{cases} \quad (2.48)$$

When the ring-oscillator is made of a cascaded chain of inverters with an odd number and the last output is fed back, the output frequency is obtained as 2.49.

$$F_{out} = \frac{1}{2 \cdot N \cdot \tau_d} \tag{2.49}$$

That can be expended in Equation 2.50 and simplified since the source to bulk voltage could be here considered nulled:

$$F_{out} = \begin{cases} \dfrac{1}{2 \cdot N \cdot \dfrac{C_{eq} \cdot V_{DD}}{I_s \cdot e^{\frac{-V_T}{n \cdot u_T}} \cdot e^{\frac{-V_{DD}}{n \cdot u_T}}}} & Weak - Inversion \\ \dfrac{1}{2 \cdot N \cdot \dfrac{C_{eq} \cdot V_{DD}}{I_s \cdot \ln\left(1 + e^{\frac{V_{DD} - V_T}{n \cdot u_T}}\right)}} & Continious - interpolation \\ \dfrac{1}{2 \cdot N \cdot \dfrac{C_{eq} \cdot V_{DD}}{\frac{I_0}{4 \cdot n \cdot u_T^2} \cdot \left(\frac{V_{DD} - V_T}{n}\right)^2}} & Strong - Inversion \end{cases} \tag{2.50}$$

The above proposition for validity range was compared to a post-layout extracted simulation given a simple 5 stage ring-oscillator in a 180nm process where the PMOS was over-sized to equate the specific current of an NMOS transistor such as $I_{SPEC_{\blacksquare P}} \cdot \frac{W_P}{L_P} = I_{SPEC_{\blacksquare N}} \cdot \frac{W_N}{L_N} = 554,4nA$. Meanwhile the sub-threshold slope $n_n n_p 1.22$, and threshold voltage $V_{TN} V_{TP} 366mV$ were comparable. And finally the post layout extracted input capacitance is $C_{eq} 5fF$; Plotted in Figure 2.30 is the asymptotic value of the Frequency based on Equation 2.50 as well as a Spice simulation result using the EKV 3.02 model.

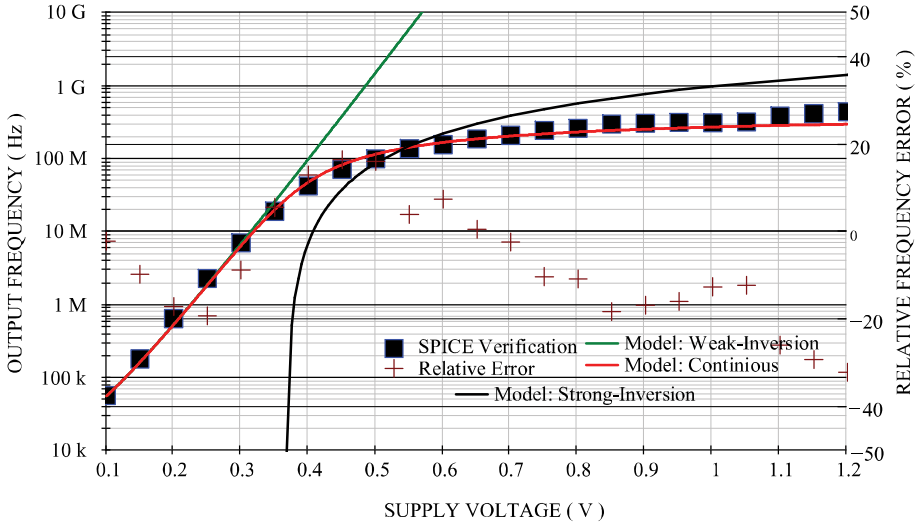


Figure 2.30: CMOS Ring-oscillator Post Layout Simulation Verification

For the weak inversion asymptote, a good matching between Equation 2.50 and the Spice simulation result is observed. Meanwhile the strong inversion asymptote is relatively misaligned. Based on the earlier work presented in [159, 201, 157], it is proposed to compare the continuous interpolation with the Spice simulation results, which turns out to be as precise as ±20% of relative variation to the Spice simulation which provides a numerical solution to Equation 2.47 covering from weak to strong inversion level. This relative error provides a good coverage and an accuracy which is comparable to ±20% [199]. The mathematical model is reasonably simple with only seven parameters to describe the circuit and the process. The process parameters includes the threshold voltage V_T , the specific current $I_0 = I_{SPEC_{\blacksquare P}} \cdot \frac{W_P}{L_P}$, it's scaling parameter $\frac{W_P}{L_P}$, the mobility β as well as the thermodynamic voltage u_T, and sub-threshold slope factor n, themselves contained in the specific current $I_{SPEC_{\blacksquare P}} = 2 \cdot n \cdot \beta \cdot u_T^2$. The output frequency is a monotonic relation that is strictly increasing and could be differentiated. It is commonly admitted that the threshold voltage V_T fluctuations, and mobility fluctuations contained in the scaled specific current I_0, are owing to the random dopant fluctuation [202, 203], which probability density function is very close to normal with an eventual positive skewness. It is a reasonable assumption that the fluctuations due to mobility fluctuation σ_β as well as those owing to sub-threshold slope σ_n are negligible in weak inversion [204, 205, 206, 145, 207, 156, 208, 148]. If a Random Variable (RV) V_T, obeys a standard normal distribution, then it's realization $Y = e^{V_T}$, obeys a log-normal distribution [209, 210]. The two fluctuations are assumed to be independent of each other, and one could derive the probabilistic central moments associated, such as Equation 2.51, for the first central moment μ_{VT-LN}, and Equation 2.52, for the second central moment σ_{VT-LN}.

$$\mu_{VT-LN} = e^{\mu_{VT-N} + \frac{\sigma^2_{VT-N}}{2}} \tag{2.51}$$

$$\sigma_{VT-LN} = \sqrt{\left(e^{\sigma^2_{VT-N}} - 1\right) \cdot e^{2 \cdot \mu_{VT-N} + \sigma^2_{VT-N}}} \tag{2.52}$$

which finally feeds Equation 2.50, which output is a probable realization of the output frequency with a probable realization of the threshold voltage $V_T = \mu_{VT-LN} \pm 3 \cdot \sigma_{VT-LN}$. However, this defines, mathematically speaking, the probability moments.

Circuit designers are interested in the standard deviation quantity because it provides a direct relation to the parametric yield (% of the performing integrated circuits). In order to achieve a parametric yield of 99.87%, for a normal distribution this corresponds to three standard deviations (3σ). Some high-quality standards achieve a parametric yield of 99.9999999 % which then corresponds to six standard deviations (6σ). There exists a sort of a rule of thumb proposed in [211, 212] such that : $3\sigma_{VT-LN} \rightarrow e^3 \sigma_{VT-N} = 20.1\sigma_{VT-N}$, and $6\sigma_{VT-LN} \rightarrow e^6 \sigma_{VT-N} = 403.4\sigma_{VT-LN}$, which illustrate that besides targeting a parametric yield of 99.87%, the log-normal or compound distribution comes with a larger second central moment. Hence, a

single gate would demand an unfeasibly large design margin to fulfill the specification of some application either in the digital or analog domain [182, 183, 199, 211, 213, 196]. It is interesting to note that the ring-oscillator is a self-timed circuit, which means the fluctuation would rather accumulate [183, 182] than average and scales inversely proportional to the number of observations$\left(1/\sqrt{N_{obs}}\right)$ which the open loop delay line will, as reported in [211]. The snag effects are that some parts might fail to start oscillating for long ring oscillators or propagate multiple transitions that might collapse, as the condition reported in [214]. In the moderate inversion region, the distribution is somewhat intermediate between strong and weak inversion, and hence it is neither perfectly Gaussian nor log-normal and the combination of 3 random variables makes it even less clear, as all of these have their own third central moments, also known as skewness.

Having introduced the hump effect electrical signature and its impact on variability in section 2.2.1.1, and presented a model for frequency estimation of a ring oscillator in Equation 2.50l, a ring oscillator made of 10005 inverters was measured at the wafer level. This ring oscillator can be observed at the top left of the die picture in Figure 2.31.

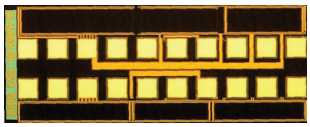


Figure 2.31: CMOS Ring-oscillator test module die picture

The measurements reported in Figure 2.32 are the results of 52 sites. The wafer map reports the local frequency on each die, biased in sub-threshold (0.4 V), on a standard and a Hump-less wafer for a 180nm CMOS technology. The frequency is normalized to the median of the observations. It can be observed that frequency varies as much as ±80% for the standard wafer, while variation is reduced drastically to ±10% for the Hump-less wafer. The frequency variability map does not show particular gradients.

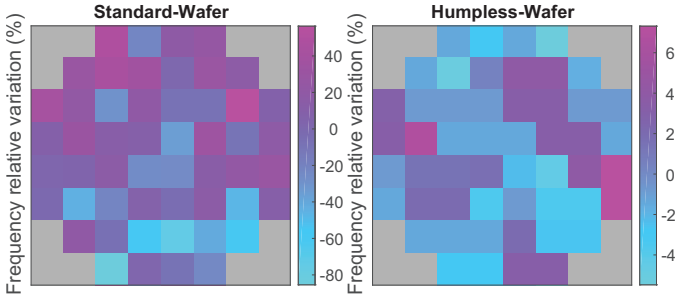


Figure 2.32: CMOS Ring-oscillator sub-threshold regime measure of the wafer frequency variability normalized to the median of a standard wafer

The same measurements reported in Figure 2.32 are now presented in histogram form in Figure 2.33, which also presents the results of circuit-level analytical expression based on

primary parameters (blue), EKV 3.02 simulation results (yellow), and the silicon results (red), for the standard wafer. The Monte-Carlo simulation using EKV 3.02 covers properly the observed frequency variability on the standard wafer. The circuit-level analysis based on primary parameters is in reasonable agreement with these results but requires more samples than measurements and simulation to properly cover the frequency spread across the wafer. This can be attributed to the fact that the slope factor and specific current variability are not taken into account in the circuit-level analysis.

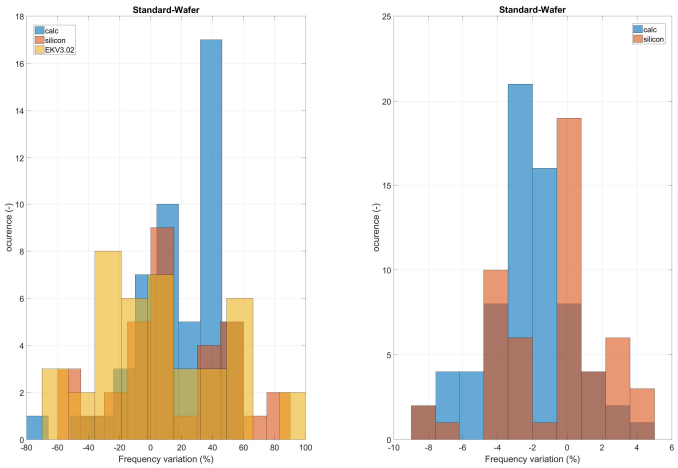


Figure 2.33: CMOS Ring-oscillator sub-threshold regime histogram of the frequency variability normalized to the median of a standard wafer

The variability is a particularly important concern for VLSI circuits such as microcontrollers [196, 195, 210, 211] where, practically, some are about quantifying the margins required [196, 195, 210, 211, 215] and other techniques [213, 196, 211, 215] propose the adjustment of the bulk-bias, or the supply voltage or the frequency or all of them. Among various techniques ring-oscillators provides an interesting signature of the corner conditions since they are highly sensitive to the threshold voltage which itself is sensitive to the temperature. The low power and low complexity CoolRISC [216] microcontroller was taken as a test case for sub-threshold design in which four PVT sensors were integrated into the corners of the die, as presented in Figure 2.34.

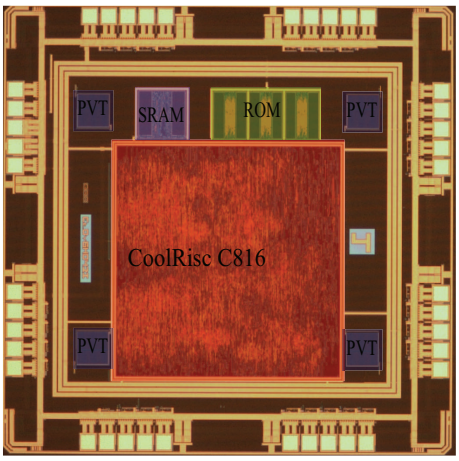


Figure 2.34: Integrated CoolRISC microcontroller along with SRAM, ROM and ring oscillator for sensing PVT conditions

The considered PVT sensor is a compact digital bloc including 18 different ring oscillators. The distinction between these oscillators is the way the logic gates realizing the inverter function are combined or their fan out. The various cross combinations could lead to more than 18. A report proposed in [196] shows different delay conditions in sub-threshold given a logic gate type and fan-out. These can be powered with the same supply voltage of the core logic and with a counter logic one can deduce the PVT conditions. For our study we have simply considered 3 of these ring oscillators which are made of CMOS inverters and an enabled nand gate, as presented in Figure 2.35.

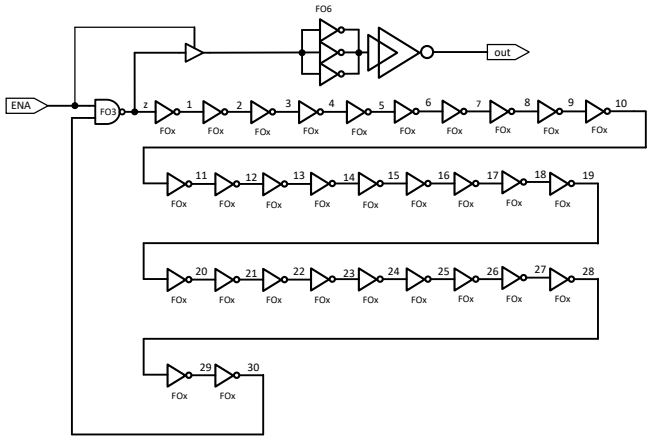


Figure 2.35: Ring oscillator schematic for sensing PVT conditions

The considered ring-oscillator in a 180nm process consisting of 31 stages with low leakage transistors such that the sub-threshold slope $n_n n_p 1.22$, and threshold voltage $V_{TN} V_{TP} 533mV$ were comparable and the specific current was also adjusted such that $I_{SPEC_{\blacksquare P,N}} = I_{SPEC_{\blacksquare N}} \cdot W =$

$453nA \cdot W$. We consider here 3 drives. Input capacitance C_{eq} was extracted in each of them. A probe card was not available to proceed with wafer-level measurement. 44 circuits were measured at 3 supply voltages [0.4V, 0.6V, 0.8V] and 3 temperatures [Cold : -40°C, Ambient : 25°C, Hot : 85°C]. Figure 2.36 presents the measurement results of the three ring oscillator's absolute variation $\frac{F_{out}.[i]-\langle F_{out}\rangle}{\langle F_{out}\rangle} \cdot \sqrt{W \cdot L} \cdot 100$ which is representative of the relative variability in percentage of the average value and normalized to the area of the logic gates. These measurements are presented for 25°.

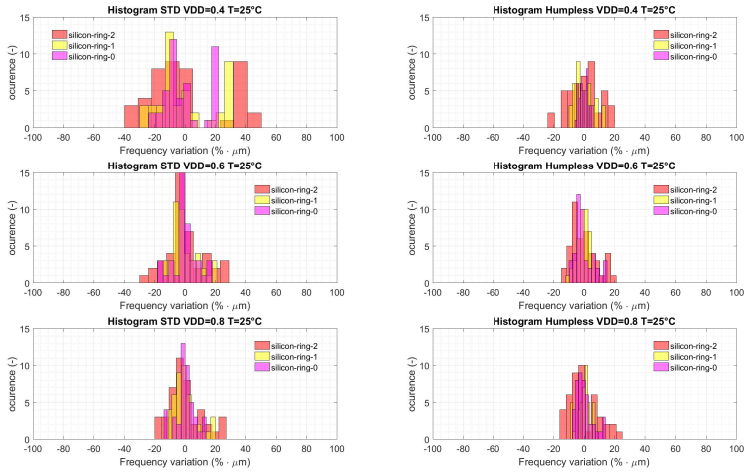


Figure 2.36: Ring-oscillator normalized relative variability

At first sight it appears that there is a variability reduction which was then quantified in Figure 2.37.

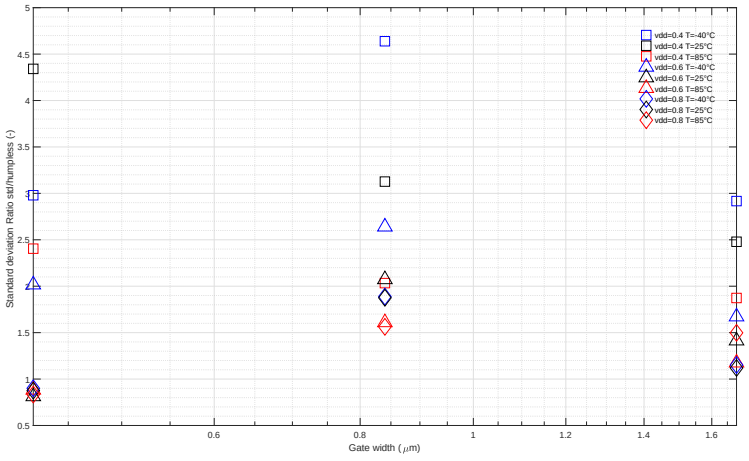


Figure 2.37: Ring-oscillator normalized relative variability

The results show interesting information in relation to the biasing voltage, where approaching a moderate to strong inversion level does not provide as much improvement as could be observed in the weak inversion domain. Another interesting approach is that the benefits reduce with a gate area increasing, specifically for a large device, which is well aligned with the transistor properties reported in Figure 2.24 and Figure 2.23. Another interesting element is the sensitivity increase at cold temperature, which confirms the observations on this effect up to date and shows the efficiency of our technique to mitigate it.

2.2.2.2 The CMOS 6T SRAM sensitivity to gate voltage mismatch

Static Random Access Memory (SRAM) is one of the most fundamental memory technologies today, for long ago digital systems integrates various gates, logic, memory but SRAM remains one of the main challenge. A VLSI circuit microcontroller is a good test candidate. Due to it's low power and low complexity, the CoolRISC [216] was taken as an example and the results are presented in [180]. The 6T SRAM configuration often known as the CMOS standard SRAM cell has the desirable properties of low power dissipation, high switching speed, and good noise margin [217]. The typical cells schematic is given in Figure 2.38.

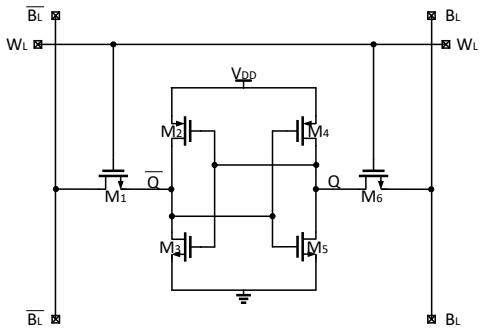


Figure 2.38: The 6 Transistor SRAM Schematic

The SRAM margin is one of the most challenging problems for low-voltage design. Circuit design techniques and architectures can mitigate that, but normal SRAMs are problematic with low voltage or near-threshold digital design [218, 219]. An analysis of the minimum power dissipation in relation to the signal to noise ratio was proposed in [220], extended with the variability limits in [167] and further in [189]. The transistor mismatch is also a concern to digital designers; one transistor could be stronger or weaker, thereby causing failures when writing or reading due to an increase in the transistor variability when the devices are operated in subthreshold. Nonetheless, precision is affected but the notion of Matching energy was introduced in [187] such that the mismatch is a voltage error signal on the gate of the MOS Transistor. The definition of such energy is given in Equation 2.53.

$$E_\sigma = C_{OX_\blacksquare} \cdot A_{V_T}^2 \tag{2.53}$$

In order to be processed, the signal energy must be significantly larger than the random mismatch energy mentioned above. In a digital circuit, e.g. flip-flop, an energy overdrive of 10 is usually considered [188, 189, 180]. Considering a constant size and process node, the lower the standard deviation of the gate voltage threshold, the lower the energy to overcome. As this figure is taken into account, energy is inversely proportional to frequency. Therefore, at a high frequency this would limit the operating voltage. In [180], we integrated a CoolRisc MCU core [216] alongside the memories (SRAM and ROM). Figure 2.34 shows our integration. The typical memory test is known as MARCH-C [221]. which consists of a finite sequence of march elements. A march element is a finite sequence of read and write operations applied to every cell in memory in either increasing or decreasing address order; the liveliness of the data is checked. On one hand the average consumption while running the MARCH-C is reported. On the other hand, after a memory reset and no further activities into the memory, the average consumption measures the leakage current contribution. It is commonly accepted that the RAM decoder contributes half the access time [222] as well as a significant fraction of the total dynamic power. Although the logic function of a decoder is reasonably simple, the function is often composed of a large fan in AND Logic gate and then driving the global to local word-line requires a large fan-out. Although there have been rare attempts to model this analytically such as in [222], traditional optimization uses the logical effort method [223]. Thus, the dynamic current of a read or write of a word usually gets dominated by the decoder while the static leakage is usually dominated by the memory point array. Recalling the behavior observed in Figure 2.22, the problem of leakage current could be addressed and is expected to reduce by a decade in a process in which sensitivity to the hump effect reduces. Figure 2.34 shows the die picture of the considered array of which the average measured leakage current of a batch of 21 sample measurements is presented in Figure 2.39. The measurements are proposed for two supply voltages, one at a weak inversion level or sub-threshold $0,4V$ and another well above the threshold $1,8V$ for both wafer standard and less sensitive to the hump effect in the industrial temperature range. In any case the lowered sensitivity to the hump effect enables gaining a decade on the leakage current.

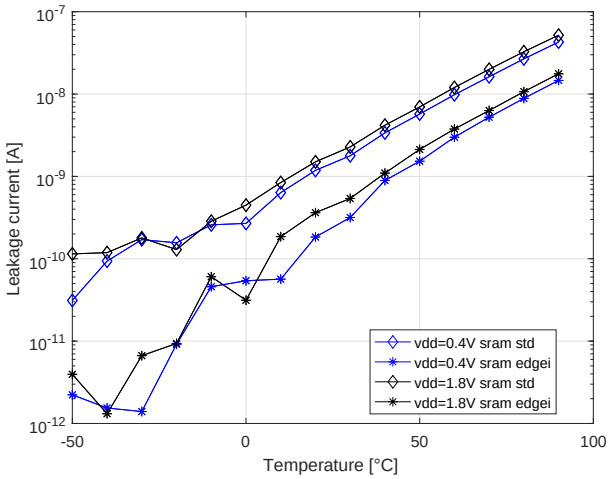


Figure 2.39: The Leakage current of a 6 Transistor SRAM array of 256 bytes along with the decoder

The next measurement step was the average. The dynamic current consumption, results are shown in Figure 2.40 and the measurement is taken at 125kHz Frequency.

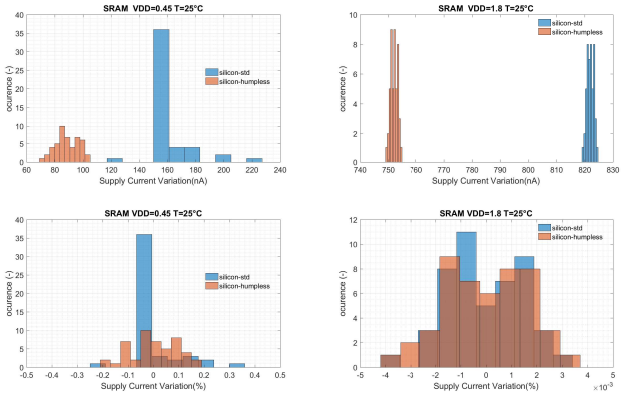


Figure 2.40: Average consumption current of a 6 Transistor SRAM array of 256 bytes along with the decoder during read and write instruction

It is shown that the current consumption reduces and the sub-threshold variability of the consumed current as well. The original objective to reduce the dynamic consumption is expressed in Equation 2.53. However, the current consumption including the decoder is well above the mismatch energy and the total value of current saving is somewhat attributed to a slightly higher threshold voltage reducing the consequence of the leakage current induced by the corner devices. When checking the liveliness of the data in ram we have observed the possibility to decrease the minimal operating voltage which would provide the benefit of reducing system on chip power consumption with efficient and agile power conditioners.

2.2.2.3 The CMOS current reference sensitivity to gate voltage mismatch

The current reference presented in [224] is a sort of standard for micro power level; a typical cells schematic is given in Figure 2.41. Once having defined the schematic it is recalled that the PMOS transistors M_{P1} and M_{P2} must operate in the strong inversion levels (greater than 10) and the NMOS transistors M_{N1} and M_{N2} must operate in the weak inversion levels (below 0.1). It is then important to note the difference in terms of aspect ratio set on the transistor M_{N1} which introduces a structural offset. One more hypothesis is made that all transistors operate in saturation, thus Equation 2.54.

$$I_D = I_{d1} = I_{d2} = \frac{u_T}{R} \cdot \ln(N) \tag{2.54}$$

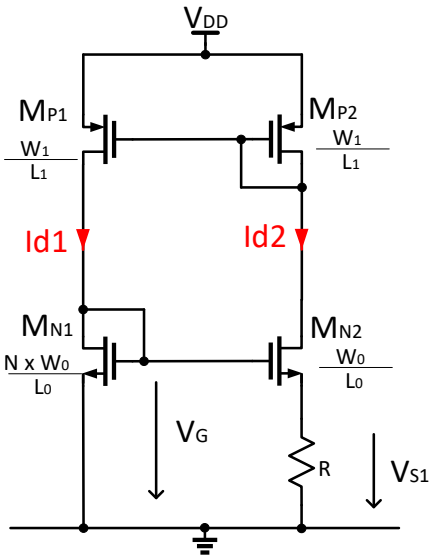


Figure 2.41: The PTAT current reference transistor level schematic

It is noteworthy that when the current level reduces to a few nano-amperes, it gets difficult to bias the transistor in strong inversion recalling. From equation 2.6 one can obtain $I_D = I_F \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W}{L}$, this imposes to use a long transistor. In order to keep a reasonable area, the width should be kept as small as possible. As seen in Figure 2.23 and Figure 2.24, the narrow and long devices hardly suffer from the threshold voltage variability increase in sub-threshold, with a factor 3 of increase. In order to address the circuit matching errors the mismatch between transistors M_{N1} and M_{N2} was first included in the study then between transistors

M_{P1} and M_{P2} and finally we introduced the resistance error.

$$I_{PTAT0} = I_{d1} = I_{d2} = \frac{u_T}{R} \cdot \ln(N) \tag{2.55}$$

In circuits such as RFID Inlay [225], the constraints on die size are shown in Figure 2.42. In a typical RFID inlay the current source cannot take too much space. In addition to some standard logic for the communication, the non volatile memory and the energy harvesting, power-management functions are usually integrated. The references and particularly the current reference requires large resistances.

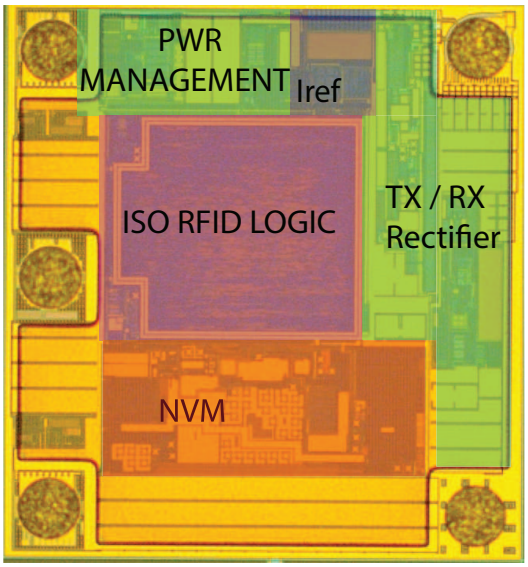


Figure 2.42: Die picture of an integrated PTAT into an RFID inlay

The resistor integration creates a first problem. A second problem is due to the use of narrow and long transistors which suffer from the corner divot transistor also called the Hump-effect. Considering the effect of the mismatch between transistors M_{N1} and M_{N2} it is worth recalling that the two devices must operate at a weak inversion level or sub-threshold, thus, according to (2.26) the main concern is the threshold voltage mismatch. The contribution of the current mirror made of the PMOS transistors M_{P1} and M_{P2} is neglected in the first place. The drain current derives from the sub-threshold relation as per Equation 2.56 for M_{N1}, and 2.56 for M_{N2}.

$$I_{D1} = I_{SPEC_{\blacksquare}} \cdot e^{\left(\frac{-V_{T01}}{n \cdot u_T} + \frac{V_G}{n \cdot u_T}\right)} \Leftrightarrow V_{T01} = V_G - n \cdot u_T \cdot \ln\left(\frac{I_{D1}}{I_{SPEC_{\blacksquare}} \cdot N \cdot \frac{W_0}{L_0}}\right) \tag{2.56}$$

$$I_{D2} = I_{SPEC_{\blacksquare}} \cdot e^{\left(\frac{-V_{T02}}{n \cdot u_T} + \frac{V_G}{n \cdot u_T} - \frac{-V_{S2}}{u_T}\right)} \Leftrightarrow V_{T02} = V_G - n \cdot u_T \cdot \ln\left(\frac{I_{D2}}{I_{SPEC_{\blacksquare}} \cdot \frac{W_0}{L_0}}\right) - n \cdot u_T \cdot V_{S2} \quad (2.57)$$

Equation 2.58 is obtained under consideration that the the sub-threshold slope factor coefficient n is unity, which then provides a direct relation of the mosfets threshold mismatch δV_T between the two NMOS transistors M_{N2} and M_{N1}. That depends only on the thermodynamic voltage u_T, and the aspect ratio N.

$$\delta V_T = V_{T01} - V_{T02} = -u_T \cdot \ln\left(\frac{\frac{1}{N}}{N^{u_T}}\right) \quad (2.58)$$

The relation between the drain current could then be expressed as 2.59.

$$I_{d2} = \frac{u_T \cdot \ln(N)}{R} - \frac{\delta V_T}{n \cdot R} \quad (2.59)$$

Thus, the error due to the mismatch of the source coupled comparator operating in the sub-threshold region is defined in Equation 2.60.

$$\varepsilon_1 = \frac{\delta V_T}{n \cdot u_T \cdot \ln(N)} \quad (2.60)$$

This contribution of random gate voltage fluctuation of transistors M_{N2} and M_{N1} could be minimized when enlarging the aspect ratio N. As a consequence, a structural offset is inserted. Having a too large structural offset is a penalty on the area since both are proportional for the same current level. Considering then the effect of the current mismatch between transistors M_{P1} and M_{P2}, knowing that the inversion level must be strong and recalling (2.26), the mobility fluctuations are then dominating such that the error is defined as per Equation 2.61.

$$\varepsilon_2 = \frac{\delta\beta}{\beta_0} = \frac{\beta_{P1} - \beta_{P2}}{\beta_P} \quad (2.61)$$

Finally the resistor mismatch contribution is obtained as per Equation 2.62. This consideration defines the unit segment that would be chained to achieve a large resistance.

$$\varepsilon_R = \frac{\delta R}{R_0} \quad (2.62)$$

A final cumulative error expression is obtained in Equation 2.63.

$$I_{PTAT} = I_{PTAT0} \cdot (1 + \varepsilon_1 + \varepsilon_2 + \varepsilon_R) \tag{2.63}$$

In the considered process the error contribution on the resistive element is measured separately and leads to $\varepsilon_R = 0.7\%$, the mobility mismatch error is considered as $\varepsilon_2 = 0.216\%$. Finally the VT error without hump effect is considered as $\varepsilon_1 = 10.5\%$, thus a total cumulated error of $\varepsilon_{tot} = \varepsilon_1 + \varepsilon_2 + \varepsilon_R = 11.416\%$ was expected with a major contribution expected from the source coupled comparator formed by the transistors M_{N1} and M_{N2} and operated in the sub-threshold region.

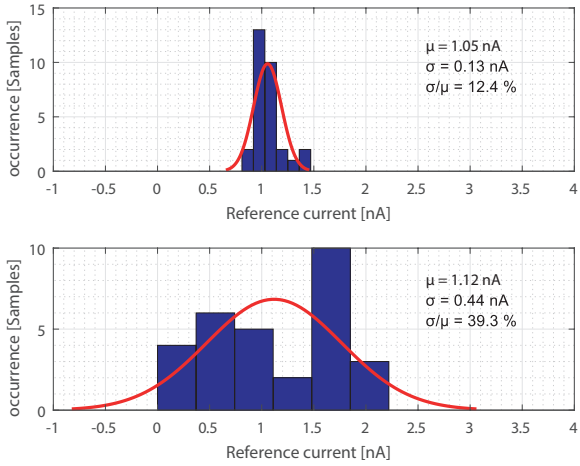


Figure 2.43: Measurement of the current reference with the hump effect (bottom) and with the corrected process (top) at room temperature.

The measurements presented in [180], are shown in Figure 2.43.It shows the measurements of two batches of 21 dies from a lot in a typical specification range after the electrical test. The presented measurements were made at room temperature. The bottom graph shows a current reference of a standard wafer which is affected by the hump effect. The same circuit was tested after a different process route which reduced the hump effect sensitivity, which measurements are reported by the top graph, and shows a reduction of 3,2 times the dispersion of the reference current after handling the trimming procedure. There is still 2% more than expected dispersion of the reference over the 21 samples, which is consistent with the variability reported in Figure 2.23.

This section provides a brief summary of the effect of the parasitic corner devices effect from the transistor level toward very large scale integration, and a reference circuit that motivates the interest to account for the effect of local mismatch when operating at low inversion level. Having observed that the corner dopant segregation was impacting the mismatch, it turns

out that the corner dopant segregation was also observed by others [208, 226] as an impactful issue for the low frequency noise variability from one die to another. We have collaborated on various test structures at device level on the variability of the low frequency noise which results are reported in [175, 227]. The low frequency noise may result in a degraded allan deviation as discussed in Figure 1.13, and in particular adding a long term drift. This has stimulated further investigations that require some more integrated circuit fabrication and measurement of the large batch, which falls outside of the scope of this work.

2.3 High resistor implementations

When the low voltage and low-power electronics challenge started decades ago. It was evolving in parallel with the main trend of high performance computers. This main trend was consuming milliwatts, while the wearable time keeping unit known as the electronic crystal watch was designed to consume power in the micro-watt range [228, 229] so that it fit the constraints of a battery operated system. The CMOS current mirror had sorted the issue of having several $M\Omega$ resistors with each and every transistor biasing the circuit, as illustrated in Figure 2.44.

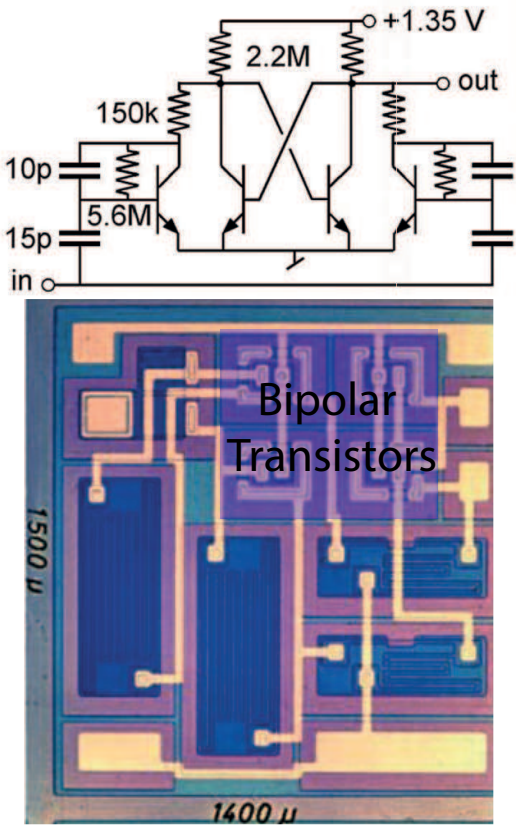


Figure 2.44: Bipolar relaxation oscillator operating in the micro-watt range

The high resistor implementation in the order of a few $M\Omega$ actually occupy most of the silicon area and have large dimensions. This challenge remains on open problem, from both ends; the process and circuit design. A generic passive solution has not been reported to our knowledge. Looking further into frequency reference [229] the use of polydiodes was proposed in order to achieve high-resistor values. However, a statement of limitation could be extracted from [229] about the temperature coefficient, which is dramatically large.

2.3.1 Highly resistive polysilicon and polysilicon diodes

Implementing could look simple in the first place the resistance is defined such that, advantageously, the semiconductor materials are not actual metallic conductors and their sheet resistance is often expressed such that the conductivity ρ, the conductor length l, and the section s, combines to express the sheet resistance such that $R = \rho \cdot \frac{l}{s}$, and the conductor line is assumed to be a parallelepiped of a constant height of which we can adjust the width and length. The minimal equal width and length form a square that is then used as a measurement unit. Typical values in a 180nm process for the sheet resistance is summarized in Table 2.4.

Table 2.4: Summary of the typical capacitance values in a 180 nm Flash process

Resistor type	-	N-Diff	P-Diff	N-Well	P-Well	N+-Poly	P+-Poly	HighRes-Poly
Resistor Sheet Density	$\frac{\Omega}{\blacksquare}$	85	95	950	316	365	110	5 325

The sheet resistor value and it's relative variation with temperature is an important parameter to take into account. Since there are no built-in currents in silicon, one needs to apply a voltage to a resistive element to get a current,.The bandgap voltage or a structural offset could be well controlled over voltage and temperature, thus it is interesting to look into the resistance thermal dependency and how it influences the reference performances. The relative temperature variations of the listed resistor types is shown in Figure 2.45.

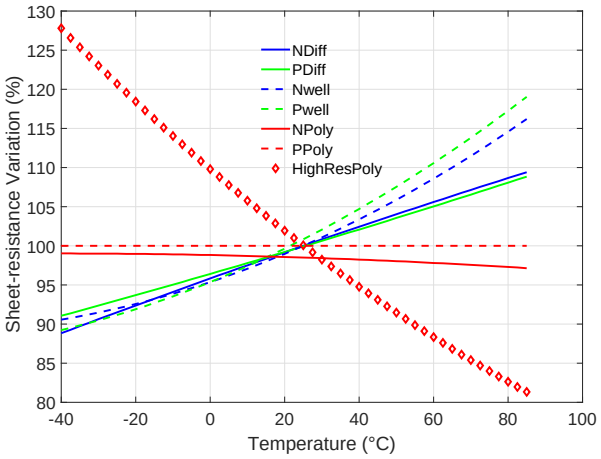


Figure 2.45: Bipolar relaxation oscillator operating in the micro-watt range

The polydiodes have interesting properties to integrate hundreds of mega-ohms in a single digit μm^2,area [230, 231]. The highly integrated resistor advantage comes with the drawback of a temperature variation being extremely important, as shown in the Figure 2.46.

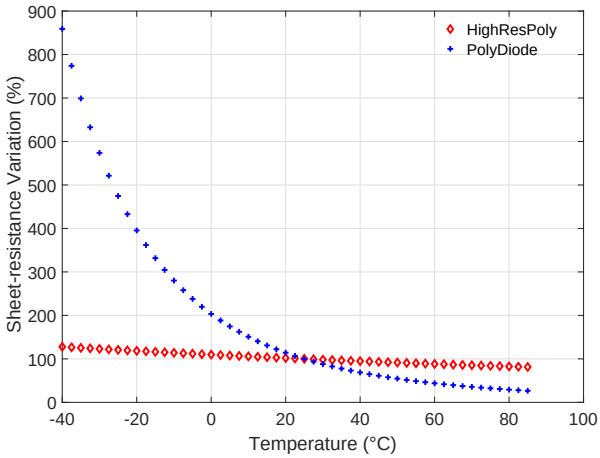


Figure 2.46: Comparison of the sheet resistance of polydiodes

These diodes also introduce a source of noise (either shot noise, flicker or low frequency noise) as discussed in [232]. Such effects are usually not part of models . Thus, cautious attention should be paid when using such a device; typically the absolute value of the resistance should not have a direct impact on the performance targeted.

2.3.2 Active resistors

The passive device resistance sheet remains a challenging problem to integrate nano-power functions within a reasonable area. The following section proposes a few possible implementations of active resistors.

2.3.2.1 Linear operation of a MOS transistor

There is a linear segment in the transistor drain current as a function of the drain source voltage characteristic shown in Figure 2.16. Thus operating in strong inversion and ensuring conduction mode (the drain source voltage is below the pinch-off saturation voltage) we could write the relation between the drain current, the pinch-off voltage and the source and drain voltage as per Equation 2.65.

$$I_D = \frac{I_{SPEC_\blacksquare} \cdot \frac{W}{L}}{u_T^2} \cdot \left(V_p - \frac{V_D + V_s}{2} \right) \cdot V_{DS} \tag{2.64}$$

Since the output conductance is defined by the drain current divided by the drain source

voltage, one could equally get the output conductance of resistance:

$$G_{DS} = \frac{I_D}{V_{DS}} = 2 \cdot \beta_{\blacksquare} \cdot \frac{W}{L} \cdot \left(V_G + V_T - n \cdot \frac{V_D + V_s}{2} \right) \tag{2.65}$$

When considering a zero threshold voltage device, also known as a native device which, as the name clearly states, is a transistor whose threshold is zero and it is possible to use it in a grounded source configuration. This simplifies Equation 2.65, into Equation 2.66.

$$G_{DS} = \frac{I_D}{V_{DS}} = 2 \cdot \beta_{\blacksquare} \cdot \frac{W}{L} \cdot \left(V_G - n \cdot \frac{V_D}{2} \right) \tag{2.66}$$

This conductance is valid when the gate voltage is greater than the pinch-off saturation voltage. Meanwhile the drain voltage should be lower than the pinch-off saturation voltage.

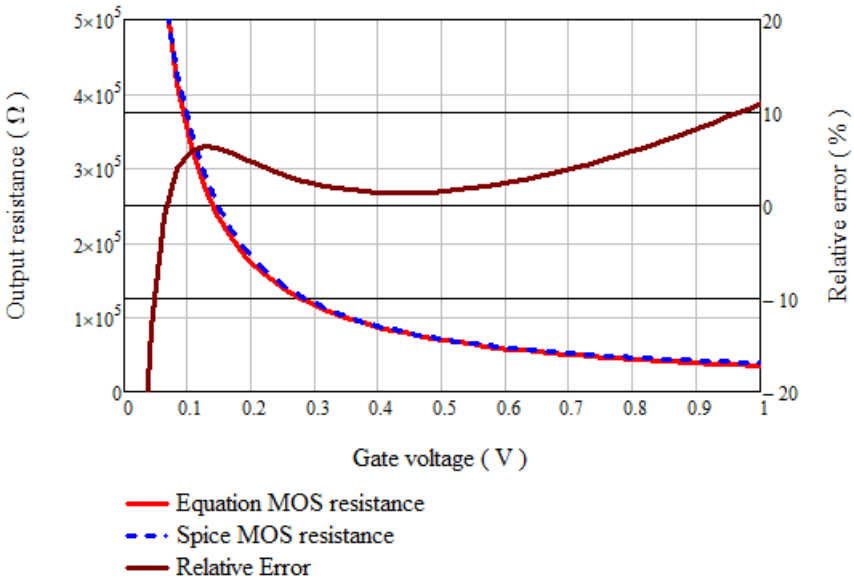


Figure 2.47: Proposed Clamp solution for gate control voltage below saturation voltage

Figure 2.47 shows the effect of the proposed additional resistance in order to clamp the impedance seen if a too high resistor provides a non linear curvature of the equivalent resistance at a gate voltage below the saturation voltage.

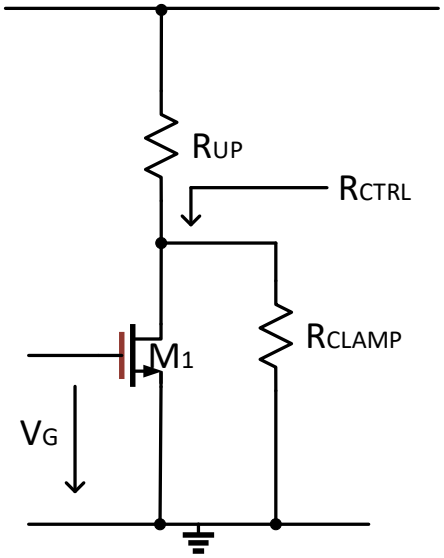


Figure 2.48: Proposed Clamp solution for gate control voltage below saturation voltage

Figure 2.48 shows a typical implementation of the clamping resistance for linearisation of the mosfet resistor when the gate voltage drops down the saturation voltage.

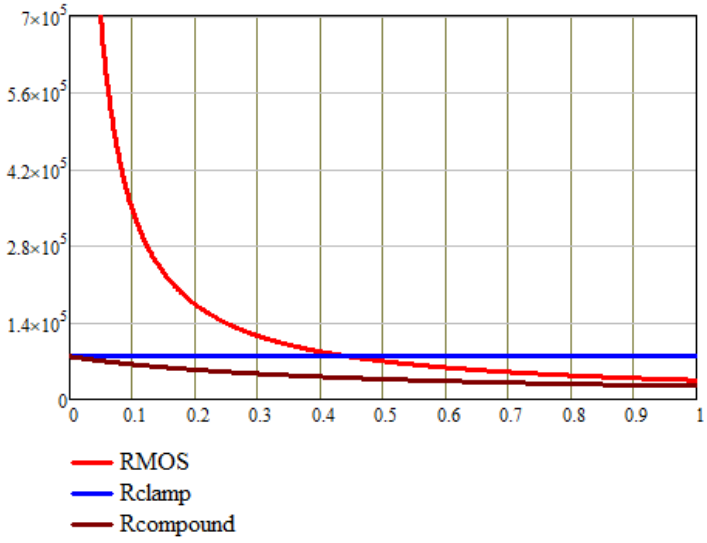


Figure 2.49: Proposed Clamp solution for gate control voltage below saturation voltage

This would typically apply in the case of a voltage controlled RC oscillator where the resistance is the control element.

2.3.2.2 Active resistor to impose a DC bias with a high impedance

The capacitive coupled amplifier such as the AC coupled inverter presented in [233], needs to impose a voltage, nevertheless, this should be a high impedance node in order to filter out the transient signal from the injected bias. The Figure 2.50 propose an implementation.

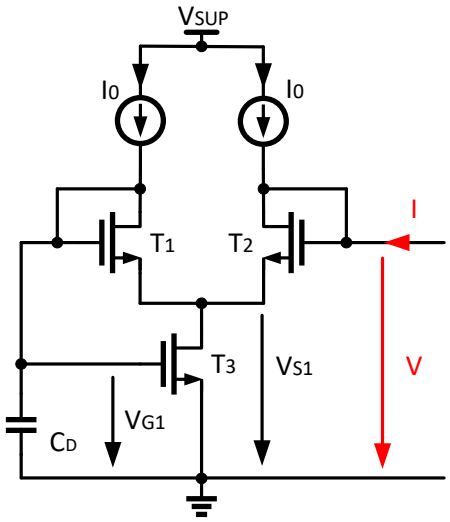


Figure 2.50: ADC-Biasing circuit for Class A-B Amplifier

It is assumed that all transistors operate in sub-threshold and are saturated and we can write a system of equations for the current relation in the circuit. The transistors are considered in to be in sub-threshold and saturated. which imposes that the drain current of the transistor T1 expresses as Equation 2.67.

$$I_0 = I_{SPEC_{\blacksquare}} \cdot \frac{W_1}{L_1} \cdot e^{-\frac{V_{T0}}{n-u_T}} \cdot e^{\frac{V_{G1}}{n-u_T}} \cdot e^{-\frac{V_{S1}}{u_T}} \tag{2.67}$$

The transistors are considered to be in sub-threshold and saturated, which imposes that the drain current of the transistor T2 expresses as Equation 2.68.

$$I + I_0 = I_{SPEC_{\blacksquare}} \cdot \frac{W_2}{L_2} \cdot e^{-\frac{V_{T0}}{n-u_T}} \cdot e^{\frac{V}{n-u_T}} \cdot e^{-\frac{V_{S1}}{u_T}} \tag{2.68}$$

The transistors are considered to be in sub-threshold and saturated.,which imposes that the

drain current of the transistor T3 expresses as Equation 2.69.

$$I + 2 \cdot I_0 = I_{SPEC_{\blacksquare}} \cdot \frac{W_3}{L_3} \cdot e^{-\frac{V_{T0}}{n-u_T}} \cdot e^{\frac{V_{G1}}{n-u_T}} \tag{2.69}$$

It could be isolated from the transistor T3 that: $e^{\frac{V_{G1}}{n-u_T}} = \frac{I+2\cdot I_0}{I_{SPEC_{\blacksquare}} \cdot \frac{W_3}{L_3} \cdot e^{-\frac{V_{T0}}{n-u_T}}}$ and from the transistor T1 that: $e^{-\frac{V_{s1}}{u_T}} = \frac{I+2\cdot I_0}{I_{SPEC_{\blacksquare}} \cdot \frac{W_3}{L_3} \cdot e^{-\frac{V_{T0}}{n-u_T}}}$. Injecting these two relations into the relation of transistor T2 it is obtained from Equation 2.70.

$$e^{\frac{V}{n-u_T}} = (I + I_0) \cdot \left(\frac{I + 2 \cdot I_0}{I_0} \right) \cdot \left(\frac{I_0 \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W_1}{L_1} \cdot e^{-\frac{V_{T0}}{n-u_T}}}{I_{SPEC_{\blacksquare}} \cdot \frac{W_2}{L_2} \cdot e^{-\frac{V_{T0}}{n-u_T}} \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W_3}{L_3} \cdot e^{-\frac{V_{T0}}{n-u_T}}} \right) \tag{2.70}$$

Equation 2.70 proposes a direct relation between our voltage V and current I defined in Figure 2.50. Let us assume the notation $i = \frac{I}{I_o}$ this defines the normalized output current to the biasing current as per Equation 2.71.

$$e^{\frac{V}{n-u_T}} = (i + 1) \cdot (i + 2) \cdot \left(\frac{I_0 \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W_1}{L_1} \cdot e^{-\frac{V_{T0}}{n-u_T}}}{I_{SPEC_{\blacksquare}} \cdot \frac{W_2}{L_2} \cdot e^{-\frac{V_{T0}}{n-u_T}} \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W_3}{L_3} \cdot e^{-\frac{V_{T0}}{n-u_T}}} \right) \tag{2.71}$$

The geometry and biasing current term could be simplified in a sign coefficient $A = \frac{I_{SPEC_{\blacksquare}} \cdot \frac{W_2}{L_2} \cdot e^{-\frac{V_{T0}}{n-u_T}} \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W_3}{L_3} \cdot e^{-\frac{V_{T0}}{n-u_T}}}{I_0 \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W_1}{L_1} \cdot e^{-\frac{V_{T0}}{n-u_T}}}$ then solving the following Equation 2.72.

$$i^2 + 3 \cdot i + 2 - A \cdot e^{\frac{V}{n-u_T}} = 0 \tag{2.72}$$

Results in (2.73) show that replacing $i = \frac{I}{I_o}$ provides a direct relation between the output voltage and current.

$$I = \frac{I_o}{2} \cdot \left(-3 + \sqrt{4 \cdot A \cdot e^{\frac{V}{n-u_T}}} \right) \tag{2.73}$$

Ideally there should not be a direct current derived from the load and thus Equation 2.73

cancels, which implies the solution as per Equation 2.74.

$$V = n \cdot u_T \cdot \ln\left(\frac{2}{A}\right) \tag{2.74}$$

2.3.3 Switched capacitors

The switched capacitor implementation of a resistor was motivated to replace the resistors by capacitors and switches in filters [234, 235, 236] in which the absolute fluctuation (aka mismatch) was studied in [184]. The simplest form of switched capacitor implementation of a resistor is presented in Figure 2.75.

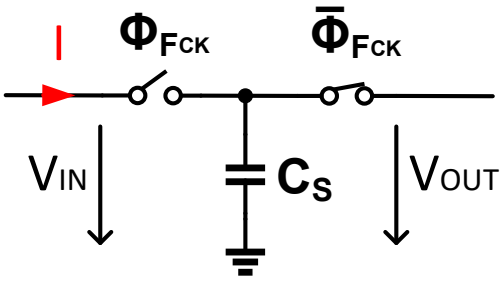


Figure 2.51: Schematic of a Switched-Capacitor emulation of a resistor

The equivalent resistance can be expressed through the charge analysis. This analysis expresses the input charges $q_{in} = C_s \cdot V_{in}$ and the output charge flow $q_{out} = C_s \cdot V_{out}$, integrating the charge flow provides the current $I = f_{ck} \cdot (V_{in} - V_{out}) \cdot C_S$, thus the equivalent impedance is given in Equation 2.75.

.

$$R = \frac{(V_{in} - V_{out})}{I} = \frac{1}{f_{ck} \cdot C_S} \tag{2.75}$$

Some typical capacitance density values for a 180nm CMOS Flash process are shown in Table 2.5.

Table 2.5: Summary of the typical capacitance values in a 180 nm Flash process

Capacitor type	-	MIM	Dual Poly	NMOS	PMOS
Capacitor Density	$\frac{fF}{\mu m^2}$	1,5	2,24	8,7	9,7
1pF Capacitor Area	μm^2	666,7	446,4	114,9	103,1

A numerical application for typical integration of a $1pF$ to $10pF$ capacitance, is given in Figure 2.52.

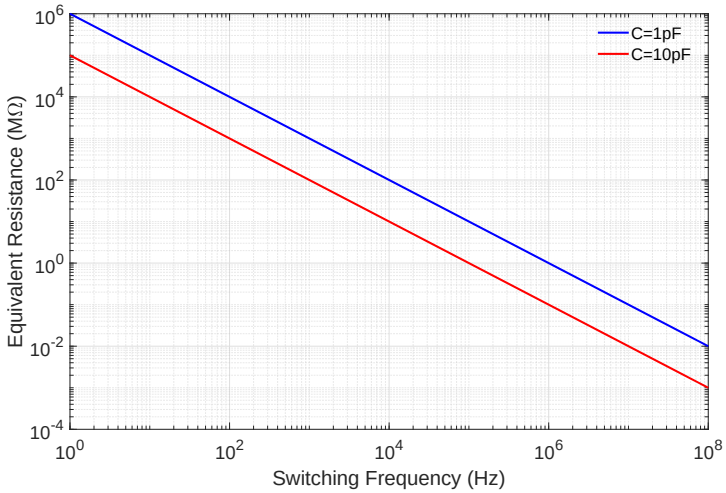


Figure 2.52: Numerical evaluation of a Switched-Capacitor emulation of a resistor

Figure 2.52 shows a typical equivalent resistance for such capacitance with respect to the switching frequency. It shows that for frequency in the KHz range and capacitance ranging between 1pF and 10pF the equivalent resistor could range from $1M\Omega$ to $100M\Omega$. Nevertheless such a solution requires the oscillator to have reasonable absolute accuracy and to provide an array for trimming the absolute capacitance value.

Structured design methodology for reference building blocks

Mobile and ubiquitous applications have driven a paradigm shift from high-performance computers toward fully integrated systems. Their common feature is power reduction in order to be sustainably battery-powered. For example, the marine chronometer was a mature technology, already a century old, when Swiss interest in precision watchmaking gave rise to the electronic crystal-based marine chronometer such as the one invented by Warren Marrisson in 1928. At a scale of 1.5 dm^3, it could be considered a rather large object with a power consumption greater than 100 mW [229]. Marine chronometers of this kind shown in Figure 3.1 solved one of the key navigational problems of that century [237], and precise timekeeping in general provided a solution for system synchronization. In this context, synchronization means there is a reference somewhere within the system [238].

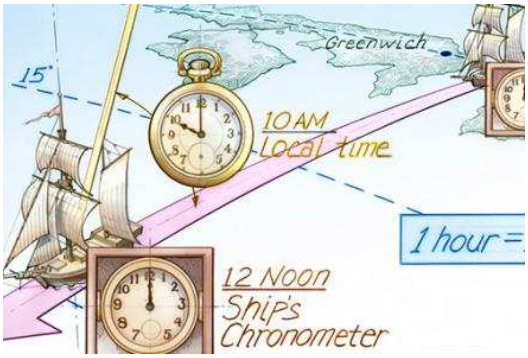


Figure 3.1: The longitude problem.

Among the fundamental research on low-power analog circuits that leverage sub-threshold properties, the mercury button cell battery specification is an example of a nominal-voltage solution that consumes only 1.35 V [224]. This led to the use of systems that could be integrated into a monolithic circuit, the capacity of which ensured a lifetime of more than one year. This meant that the power consumption of a typical wristwatch had to be no more than 10 μW, which is four orders of magnitude lower than that of marine chronometers. Such constraints apply to the general consumer-electronics market, whether the device be a watch or any other wearable or ubiquitous computer, all of which have microcontrollers as a common

feature [239, 240]. The key technology for miniaturization is process scaling [10, 12, 241, 242], which reduced the silicon area, increased computational capability and lowered power consumption. However, later deep-sub-micron technologies suffered from increased leakage, but fully depleted silicon-on-insulator technologies enabled leakage to be reduced and integrated circuits to operate with supply voltages below 0.5 V in CMOS 1 μm in a fully depleted silicon-on-insulator process [243, 244]. Promising research outcomes to achieve near-threshold logic and systems have been published [245, 246, 247, 248, 249, 250], where the near-threshold logic paradigm [248] consists of a gain in power and thermal dissipation at the cost of architectural parallelism such as pipeline or replicating functions to ensure a given performance. This paradigm has been driven essentially by size and power-constrained systems such as body implants for medical purposes [251], or environmental or industrial process monitoring at the core of Industry 4.0 [34, 38]. For aggressive miniaturization of computing platforms, ultra-low power consumption is one of the most challenging constraints resulting from the form factor of the system. Regarding the application layer, energy harvesting is one approach to complement battery-operated systems [252], and it is a domain where the frequency reference plays a key role [253, 254]. Finally, as these devices are intended to be interconnected in addition to improving the communication layer [255], a security concept is needed, which requires certain building blocks to ensure chip security. One such component is a random number generator, which is somehow a noise entropy extractor that, over the years, has moved into the time domain [256] and relies on signal jitter.

In this chapter, a structured methodology is proposed to approach the design of self-biased current and frequency references. CMOS technology itself provides neither a current nor a time reference, although, in a given process, the frequency, supply voltage and intrinsic capacitance define a frequency as reviewed in Section 2.2.2.1, where the effect of a STI divot corner device on frequency variability is addressed. This also shows that a ring oscillator could be considered a dipole in terms of $I-V$ characteristics. This chapter is organized into five sections. Section 3.1 reviews selected near-threshold design challenges for analog circuits and connects them with the self-biased circuits addressed in Section 3.2. This was motivated originally by the current reference, and then the principle was translated to frequency references. For the design of a self-biased methodology, Section 3.3 proposes a fully integrated RC timer. The use of a self-biased circuit is also translated into a revisited resonator-based Pierce oscillator in Section 3.4. Section 3.5 discusses the potential of leveraging the phase noise of a self-biased oscillator to generate random numbers, and a stochastic model is proposed in this context.

3.1 Voltage scaling and design point in near-threshold-region challenges

Although sub-threshold design often refers to $V_{DD} = V_T$, it really applies to any application where the supply voltage is less than the sum of $V_{DD} = V_{TP} + V_{TN}$. Let us consider basic CMOS structures such as the common source amplifier stage in Figure 3.2(A), the common gate configuration in Figure 3.2(B), and the common drain amplifier, also known as the follower configuration, in Figure 3.2(C).

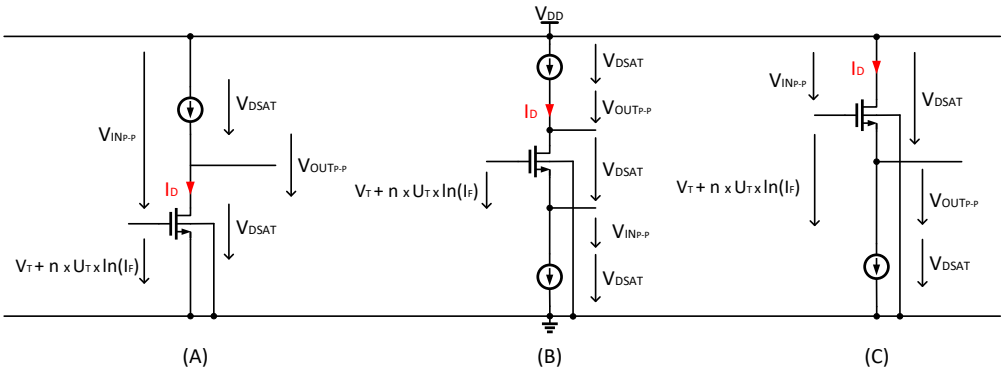


Figure 3.2: Basic CMOS structures.

One can observe the need for the current biasing to operate in a saturated state, and this implies a drain to source voltage, where saturation $V_{DSAT} \sim 0.15$ V is independent of the threshold voltage scaling. Sub-threshold design then refers to a supply voltage of $V_{DD} = 0.5$ V or less when the typical transistor threshold values are $V_T = 250$ mV. In this condition, one can observe that, of the above three configurations, only the common source has the potential to operate down to $V_{DD} = 0.5$ V. For mature CMOS nodes such as $L_{MIN} = 350$ nm down to $L_{MIN} = 110$ nm, when threshold voltage values are $V_T = 600$ mV with a supply voltage of $V_{DD} = 1.2$ V, the supply voltage means that these circuits fall into the category sub-threshold designs and the designer must seriously consider sub-threshold problems such as susceptibility to noise and process variations. Having introduced the notion of an inversion factor, the term $\frac{g_m}{I_D}$ in Equation 2.9 bridges a small signal quantity, which is the trans-conductance, to the drain current. It is also a convenient relation to the inversion factor I_F, although the strong signal dynamic should be considered to ensure functionality. A power penalty factor (Γ) was introduced in a tutorial lecture of Peter Kinget [257] at the European Solid State Circuit Conference 2013, and this metric can be applied to the voltage processing block such as amplifiers because the acceptable signal swing reduces the supply voltage more than proportionally. This compression is illustrated in Figure 3.3, which shows the effect of scaling the supply voltage, whereas the saturation voltage does not scale.

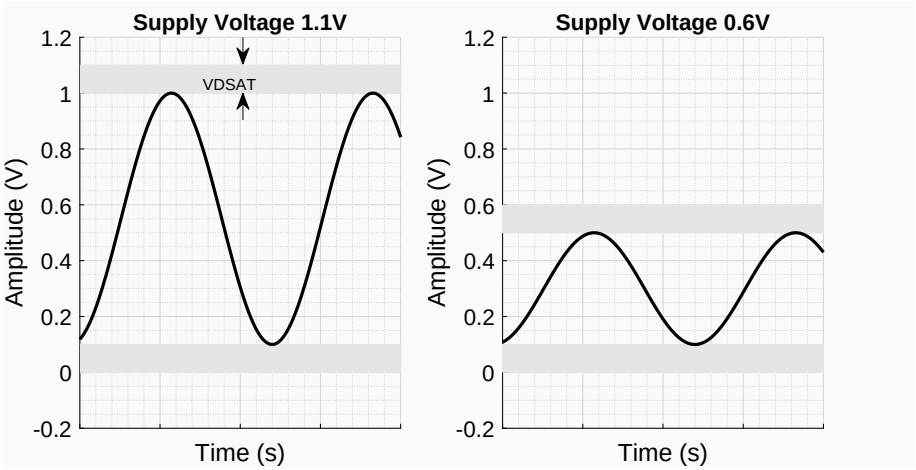


Figure 3.3: Amplitude scaling and power penalty factor.

The power penalty factor is $\left(\Gamma_p = 1 + \frac{2 \cdot V_{DSAT}}{VDD - 2 \cdot V_{DSAT}}\right)$ for a sine wave, assuming that it remains in a non-saturated amplification region as shown in Figure 3.3. Nevertheless this further reduces the signal amplitude with respect to noise. In this context, the minimum power of a single-pole Class B amplifier power limitation was extended in [257] from [258], as follows:

$$P \geq 8 \cdot k \cdot T \cdot f_{ck} \cdot \frac{V_s}{V_n} \cdot \Gamma_p \tag{3.1}$$

Class B amplifiers have a considerable advantage over Class A amplifiers in that no current flows through the transistors when they are in their quiescent state, and therefore no power is dissipated in the output drive. It can be observed that the power penalty factor in Figure 3.4 for supply voltage scaling down to $V_{DD} = 0.5$ V is already more than twice the power $(\Gamma = 2,5)$.

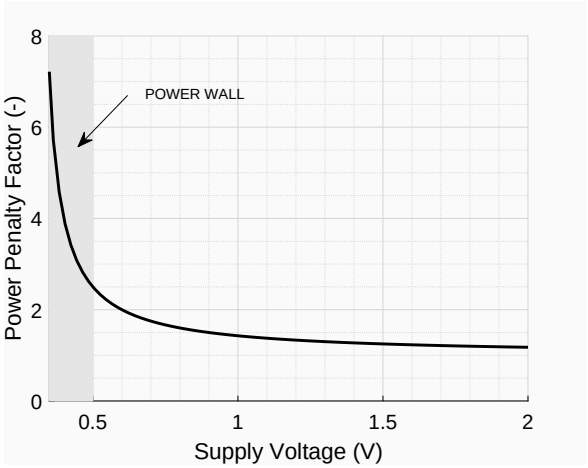


Figure 3.4: Power penalty factor as a function of supply voltage.

Extensive use of fully differential circuits leverages their properties of a high swing supply and substrate insensitivity, which are essential to low-voltage design for which the common-mode

rejection is even more important. The design of aggressively scaled supply voltage analog blocks gave rise to various techniques to cope with supply voltages reduced to $V_{DD} = 0.5$ V such as VCO-based quantizers for sensor interfaces [259, 260] or for more asynchronous event-driven sampling or continuous-in-time and discrete-in-amplitude acquisition chains [261]. It is worth noting that these techniques rely on time-based circuits or require precise external frequency references.

3.2 Design guidelines for self-biased amplifiers

The discussion in Section 2.3 of implementation of high resistor values shows that, to reduce passives, one could use current biasing, although silicon does not include a current reference. However, semiconductor physics provides us with the highly stable quantity of bandgap energy [262]. The reference voltage has proved to be extremely important in many applications such as analog-to-digital conversion and the reverse, as well as power management in general [263]. Owing to the limitations of battery-operated circuits down to 0.85 V and for operating in the near-threshold regime, we cannot use the bandgap voltage, which is higher than the battery end-of-life voltage. Another extraction principle that could apply at the circuit level is to compare two devices in terms of a specific property and a rather general property, such as the $I-V$ curves of various dipoles. As illustrated in Figure 3.5, one could observe a few typical curves such as the resistor in blue, a diode in red or an NMOS transistor in saturation in black. Operating points are highlighted in green.

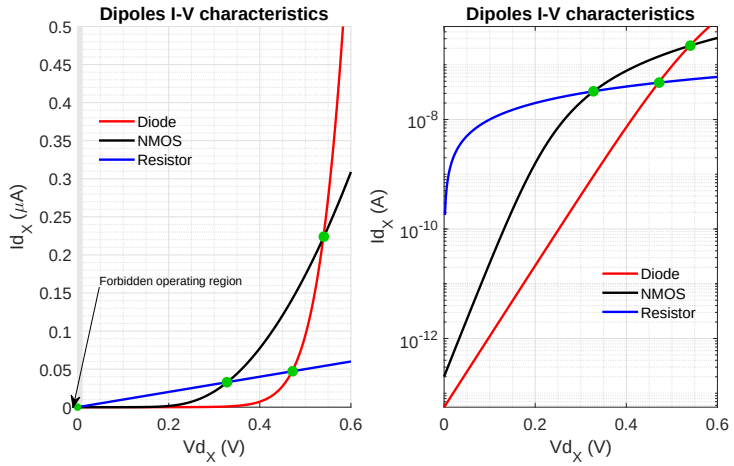


Figure 3.5: $I-V$ device characteristics and operating points.

Recalling the modeling results discussed in Section 2.1, the MOSFET can also be operated in weak-inversion mode, where the drain current varies exponentially with respect to the gate voltage, which mimics the diode characteristic. The above curves can cross into a named forbidden operating region, which is the zero-current, zero-voltage region, where the circuit has not started. In principle, a circuit does not require external bias if it has the capability to start. In that case, it is equal to the voltage and current of two dipoles. Figure 3.6 shows a

schematic of an ideal voltage-controlled voltage source and voltage-controlled current source, which in principle would find the operating point of two dipoles. The operating point is found as soon as the current is balanced to obtain equal voltages at the dipole terminals.

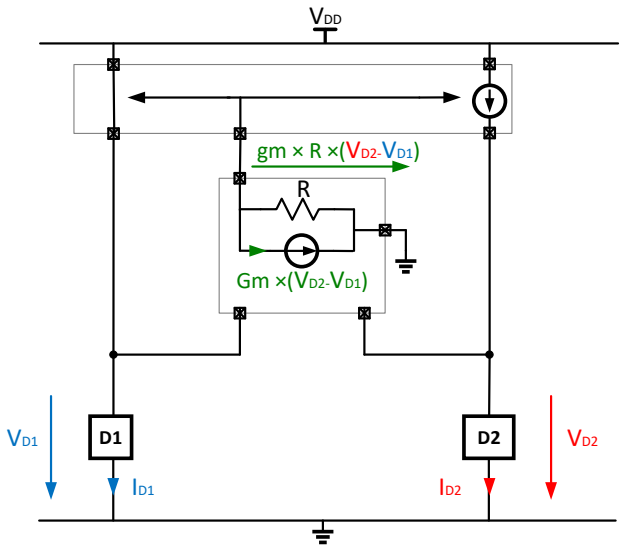


Figure 3.6: Schematic of a voltage-following current mirror.

The concept of a voltage-following current mirror was first proposed in [264]. That bipolar implementation called for adding a common collector voltage follower between the two collectors of the current mirror. This introduced a systematic offset because the voltage follower is then forward-biased, which has proved to reduce sensitivity to the power supply rail. In addition, the temperature effect is dependent on the two $I-V$ device characteristics effect, which should find a new operating point at each temperature. A direct application of this principle to generate a current reference is proposed in [265], which turns out to be proportional to absolute temperature and practically insensitive to supply variation effects. This earlier circuit intuition was first exposed by Th. J. Van Kessel, and R. Van de Plassche in an article entitled "Integrated Linear Basic Circuits" in the Philips Technical Review of 1971. The weak inversion level or sub-threshold behavior of a MOSFET transistor close to bipolar transistor current reference was proposed in [224] earlier than the bipolar structure proposed in [265]. Another analysis of this structure in strong inversion was proposed in [266]. The structure proposed in [224, 265, 266] is self-biased but nevertheless resulted in a positive feedback loop that imposes a structural offset. A rather general scheme is presented in Figure 3.6, which refers to [224, 265, 266] and implements a current reference by using a source-coupled comparator discussed in more detail in Section 3.2.1. However, note that the source-coupled comparator circuit imposes a structural offset in the feedback loop so that the circuit is stable. The adaptive biasing amplifier proposed in [267] decouples the positive feedback loop and the actual differential stage, the design method of which is detailed in

Section 3.2.2 .

3.2.1 Design guidelines for the source-coupled comparator

Figure 3.7 proposes an implementation of a source-coupled comparator that tends to equate the voltage sources of M1 and M2 by adjusting the current I_{REF}. This implements a voltage follower current mirror (VFCM), where the current mirror formed by M3, M4 tends to equate the current of the structural offset imposed by the imbalance (N:1) with an offset seen from the source of M2.

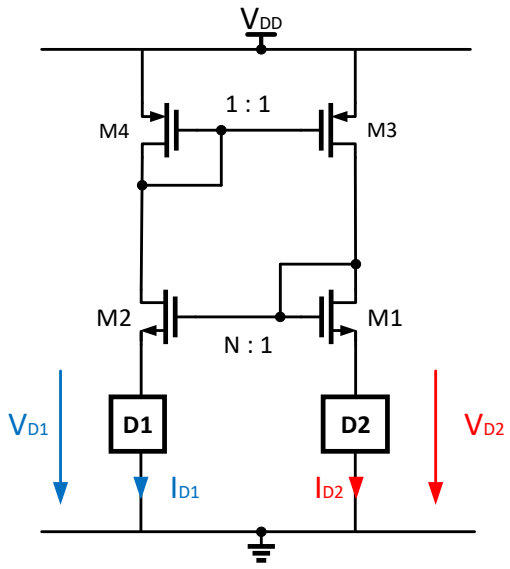


Figure 3.7: Self-biased source-coupled comparator.

This translates into a few relationships, and the current mirror imposes the following relation:

$$I_{D1} = I_{D2} = I_{REF} \tag{3.2}$$

The channel voltage conditions of transistors M3 and M4 are

$$V_{P_{M4}} - V_{S_{M4}} = V_{P_{M3}} - V_{S_{M3}} \tag{3.3}$$

and the channel voltage conditions of transistors M1 and M2 are

$$V_{P_{M1}} - V_{S_{M1}} = V_{P_{M2}} - V_{S_{M2}} \tag{3.4}$$

It is important to mention that the circuit in Figure 3.7 does not show a start-up circuit because of a positive feedback. Combining Eqs. (3.2), (3.3), and (3.4), we determined the source voltage of transistor M2 as

$$V_{S_{M2}} = \left[V_{P_{M2}} - V_{P_{M1}}\right] + V_{S_{M1}} \tag{3.5}$$

This property can make the circuits unstable. The easiest remedy is to insert an imbalance between the sizes of transistors M1 and M2. Equation 3.5 presents the difference in pinch-off voltage between transistors M1 and M2, both highlighted in the schematic shown in Figure 3.8.

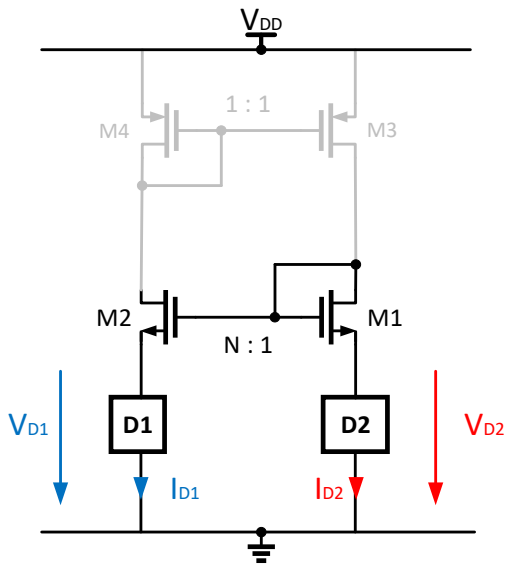


Figure 3.8: Self-biased source-coupled comparator: Comparator sizing.

A simplifying assumption is to set the source voltage of transistor M1 to zero such that $V_{S_{M1}} = 0$, and thus simplify Eq. 3.5. The numerical solution reusing the complete EKV formulation as per Eq. 2.3 describes the pinch-off voltage (particularly the gate voltage, to which the inverted charge becomes zero) with respect to the source voltage as shown in Figure 3.9 in red. This figure shows the normalized value of the source voltage of transistor M2 with respect to thermodynamic voltage such as $\upsilon_{S_{Ms}} = \frac{V_{S_{M2}}}{u_T}$. The imbalance chosen for Figure 3.9 is to have transistor M2 be oversized by a factor of $N = 20$ with respect to transistor M1. The source voltage of transistor M1 would have the impact of an offset if a voltage is applied to that terminal.

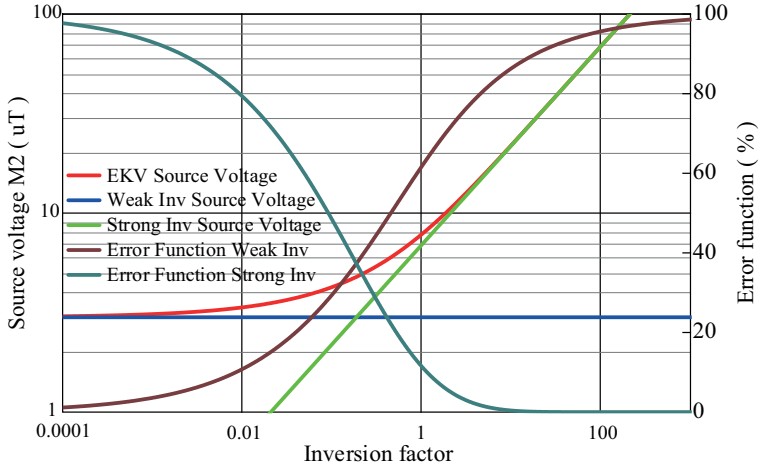


Figure 3.9: Self-biased source-coupled comparator source voltage developed at a given imbalance.

Using the generic solution, we could check the particular solution of the weak-inversion level as per Eq. 3.6 as proposed in [224] and the strong-inversion level as per Eq. 3.7 as proposed in [265].

$$V_{S_{M2}} = u_T \cdot ln(N) + V_{S_{M1}} \tag{3.6}$$

$$V_{S_{M2}} = 2 \cdot \sqrt{I_{F2}} \cdot ln\left(1 - \frac{1}{\sqrt{N}}\right) + V_{S_{M1}} \tag{3.7}$$

The error plot in Figure 3.9 suggests designing a weak inversion with a coefficient of less than 0.01 and a strong inversion with a coefficient of greater than 15 such that using one asymptote or the other yields an error below 10% relative to the EKV fitting function. The error due to the mismatch of the source-coupled comparator operating in the subthreshold region is defined in Eq. 2.60. Thus, our first step is to select a structural offset value as defined here:

$$\delta V_T = n \cdot u_T \cdot ln(N) \tag{3.8}$$

The overall impact on the value of the current is given as 2.63. Knowing the contribution of each value *a priori* provides enough constraints to size transistor M1. A second step is to account for the cumulative variability spread compliance as presented in Eq. 3.9.

$$\sigma_{V_T} = \varepsilon_1 \cdot \delta V_T \tag{3.9}$$

Given the above constraint for variability spread, we have

$$W_{M1} \cdot L_{M1} = \left(\frac{A_{V_T}}{3 \cdot \sigma_{V_T}} \right)^2 \tag{3.10}$$

The aspect ratio is then set given an inversion level of $\left(I_F \ll 10^{-3}\right)$ below one milli as discussed in Figure 3.9, which leads to

$$\frac{W_{M1}}{L_{M1}} = \frac{I_{REF}}{I_{SPEC_{\blacksquare}} \cdot \frac{I_F}{N}} \tag{3.11}$$

Combining Eq. (3.11) and (3.10) provides a direct expression for setting the width :

$$W_{M1} = \sqrt{(W_M \cdot L_M) \cdot \frac{W_M}{L_M}} \tag{3.12}$$

and combining Eq. 3.11 and 3.10 provides a direct expression for setting the gate length :

$$L_{M1} = \frac{(W_M \cdot L_M)}{\sqrt{(W_M \cdot L_M) \cdot \frac{W_M}{L_M}}} \tag{3.13}$$

Transistor M2 is N times larger, which could be implemented as a multiple finger or multiple instances :

$$\frac{W_{M2}}{L_{M2}} = \frac{N \cdot W_{M1}}{L_{M1}} \tag{3.14}$$

3.2.1.1 Source-coupled comparator feedback loop and stability conditions

As described in [266], a small signal analysis opens the loop at a gate voltage of M2 by injecting a voltage and takes it back on the drain and gate of M1 as shown in Figure 3.10(a). The equivalent small signal schematic of this analysis is shown in Figure 3.10(b).

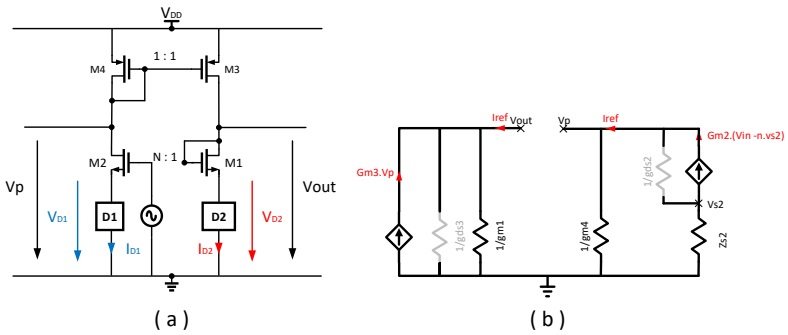


Figure 3.10: Self-biased source-coupled comparator: Stability analysis.

The transfer function is obtained as follows, assuming the output conductance is much lower than the transconductance $g_{m_{Mx}} \gg g_{ds_{Mx}}$, which provides the loop gain as follows:

$$A_{loop} = \frac{V_{g_{M1}}}{V_{d_{M2}}} = \frac{g_{m_{M3}}}{g_{m_{M1}}} \cdot \frac{\frac{1}{g_{m_{M4}}}}{\frac{1}{g_{m_{M2}}} + n \cdot Z_{S_{M2}}} \tag{3.15}$$

For a stable operation of the circuit, the feedback gain must be less than 1. Hence this suggests that N, the size ratio of M2 and Ml, should be greater than 1 to ensure the stability of the circuit. In practice, a ratio of 8 is often considered at the edge because, in the sub-threshold regime, it ensures that an offset voltage of $V_{S_{M2}} \geq 2 \cdot u_T$ is greater than twice the thermodynamic voltage, thus maintaining a reasonable comparator reference level. A following small signal analysis is the power supply rejection ratio according to the schematic presented in Figure 3.11.

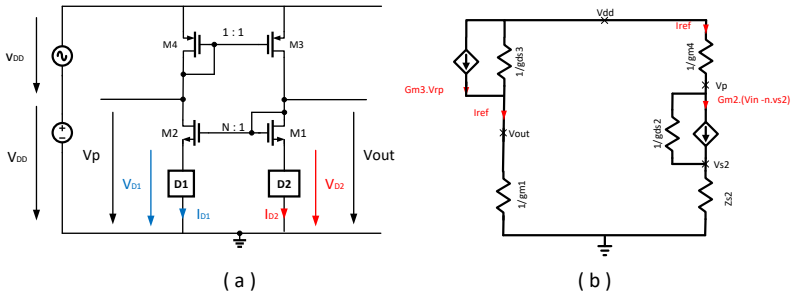


Figure 3.11: Self-biased source-coupled comparator: Supply rejection analysis.

The supply rejection could be approximated as in Eq. 3.16, which is mostly dependent on the P-channel length modulation and yields the same results as a standard current mirror.

$$PSRR = \frac{I_{ref}}{V_{DD}} = g_{ds_{M3}} \tag{3.16}$$

The last highlighted design part of the schematic is shown in Figure 3.12.

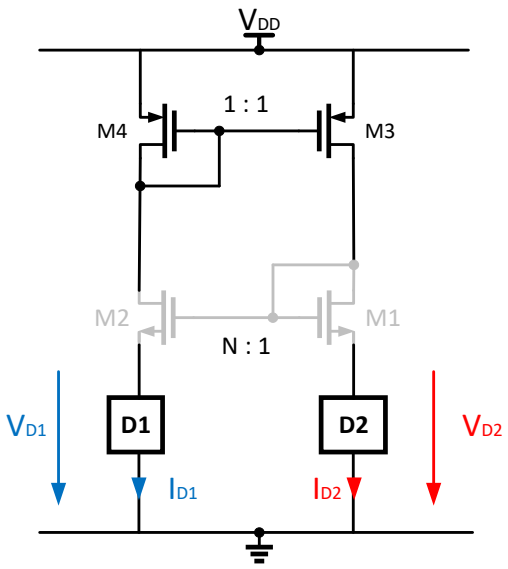


Figure 3.12: Self-biased source coupled comparator: Current mirror sizing.

According to

$$\frac{W_{M3}}{L_{M3}} = \frac{W_{M4}}{L_{M4}} = \frac{I_{REF}}{I_{SPEC_{\blacksquare}} \cdot I_F} \tag{3.17}$$

we need to address two requirements, one of which is the output conductance 3.18

$$L_{M3} = L_{M4} = \frac{I_F \cdot I_{SPEC_{\blacksquare}} \cdot \frac{W_{M3}}{L_{M3}}}{V_A' \cdot gds} \tag{3.18}$$

At the same time, the overall impact on the value of the current is given as 2.63, but a similar analysis could be performed in the other case

$$W_{M3} \cdot L_{M3} = W_{M4} \cdot L_{M4} = \left(\frac{A_\beta}{3 \cdot \sigma_\beta}\right)^2 \tag{3.19}$$

Combining Eqs. 3.17 and 3.19 provides a direct expression for setting the width:

$$W_{M3,4} = \sqrt{\left(W_{M3,4} \cdot L_{M3,4}\right) \cdot \frac{W_{M3,4}}{L_{M3,4}}} \tag{3.20}$$

Combining Eqs. 3.17 and 3.19 provides a direct expression for setting the gate length determined by Eq. 3.21:

$$L_{M3,4} = \frac{\left(W_{M3,4} \cdot L_{M3,4}\right)}{\sqrt{\left(W_{M3,4} \cdot L_{M3,4}\right) \cdot \frac{W_{M3,4}}{L_{M3,4}}}} \tag{3.21}$$

This computed gate length must be coherent with Eq. 3.18, and we select the maximum of the two. This sizing methodology was applied in Sections 4.1 and 4.5.

3.2.1.2 Source-coupled comparator: Large signal consideration

The large signal consideration of the source-coupled comparator is important to determine limits of circuit operation, given the structural sizing methodology proposed above. Equation 3.22 expresses the headroom limit of the circuit:

$$V_{DD} \geq \begin{cases} V_{D1} + V_{T_{M2}} + V_{DSAT_{M2}} + V_{T_{M4}} + V_{DSAT_{M4}} \\ V_{D2} + V_{T_{M1}} + V_{DSAT_{M1}} + V_{T_{M3}} + V_{DSAT_{M3}} \end{cases} \tag{3.22}$$

The large-signal limitation essentially takes into account the saturation thresholds and voltages of the transistors. Taking into account a 180 nm process and its parameters reported in Table 2.2 and assuming a low inversion operating point at the saturation limit yields

$$V_{DD} \sim\geq V_{DX} + 550\text{mV} \tag{3.23}$$

The forward design approach to this design equation would be to impose the dipole voltage of V_{DX} for a given technology and supply voltage. A backward design approach would be to take a voltage optimum of the V_{DX} dipole to minimize noise, for example, and define a minimum supply voltage. Equation 3.23 does not take temperature variations into account because they impact primarily the threshold voltage, which is sensitive to about 2 mV/K for a variation of 50 K around ambient temperature and would impose a margin of 100 mV . This makes it difficult to use and would put it at the operating limit below a power supply of 1 V. As indicated in Section 3.1, reducing the supply voltage yields substantial energy savings.

However, it becomes impossible to stack transistors that do not have a decrease in threshold voltages and saturation. Therefore, the results presented in Section 3.2.2.5, using a "self-biased OTA" structure, are recommended for power supply conditions below 1 V.

3.2.2 Design guidelines for self-biased OTA

Self-biased OTA could be considered self-biasing circuits as soon as dipoles D1 and D2 find a DC operating point so that the amplifier equates voltages V_{D1} and V_{D2}. If one operating point exists, the fixed biasing current used in [267] is not mandatory.

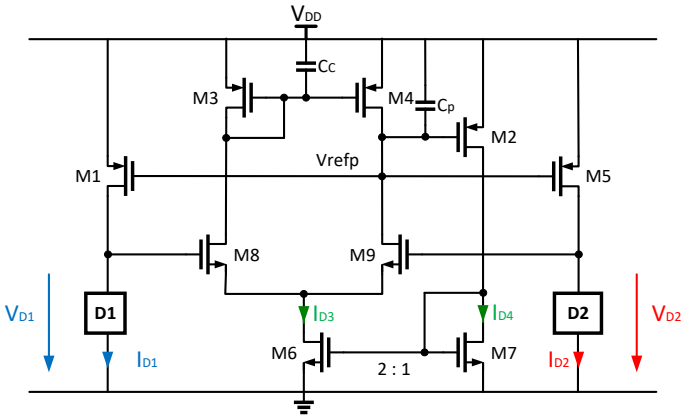


Figure 3.13: Self-biased amplifier schematic.

The biasing current in the OTA has to be chosen carefully because it generates an overhead power consumption with respect to the structure presented in Figure 3.7. However, it provides the advantage of whether to impose a structural offset. The total current consumption is expressed as follows:

$$I_{TOT} = I_{D1} + I_{D2} + I_{D3} + I_{D4} \tag{3.24}$$

which can express the OTA consumption. This equation unfortunately does not show that the OTA contains three current branches.

$$I_{OTA} = I_{D3} + I_{D4} \tag{3.25}$$

It is important to match PMOS transistors identified M_1, M_5, M_2, M_3, and M_4 in Figure 3.13. As we intend to equate currents such that $I_{D1} = I_{D2}$, we define the corresponding transistor to be $\frac{W}{L}_{M_1} = \frac{W}{L}_{M_5}$. If we now define a factor of, say, B to be a fraction of the current consumption

$I_{D1} = I_{D2}$ to bias the OTA, it yields $\frac{W}{L}_{M_1,M_5} = B \cdot \frac{W}{L}_{M_2,M_3,M_4}$. The total consumption could now be simplified as Equation. 3.26.

$$I_{TOT} = \left[\frac{3}{B} + 2\right] \cdot I_{D1} \tag{3.26}$$

3.2.2.1 Setting the bias

Figure 3.15 highlights transistor M_6, which handles the tail bias current of the differential pair and must be saturated.

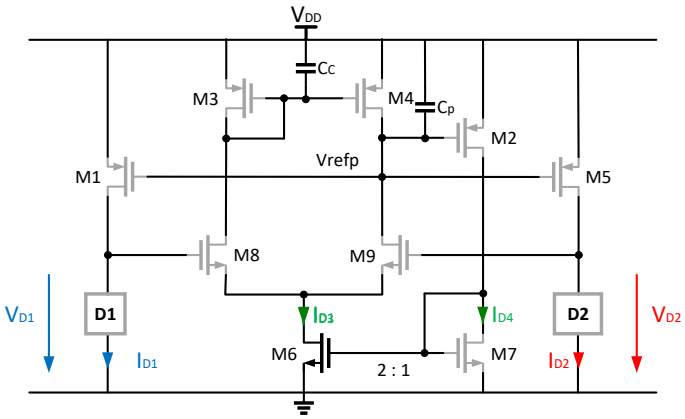


Figure 3.14: Self-biased amplifier: Tail bias transistor sizing.

Considering the above Equation 3.24, yield to Equation 3.27.

$$I_{M6} = \frac{2}{B} \cdot I_{D1,D2} \tag{3.27}$$

Thus, to design an efficient circuitry, the biasing circuit should operate mainly in moderate inversion. Assuming $V_{DSAT_{M7}} \sim 250$ mV allows us to use Eq. 2.12 to determine the inversion factor of transistor M7 as follows:

$$I_{F_{M6}} = \left[\frac{1}{2} \cdot \left(\frac{V_{DSAT_{M7}}}{u_T} - 4\right)\right]^2 \tag{3.28}$$

where $I_{F_{M6}}$. A small inversion factor reduces the stability to temperature because the primary parameters such as threshold and mobility variation sensitivity are close to the absolute value. This in fact sets the following aspect ratio:

$$\frac{W_{M7}}{L_{M7}} = \frac{I_{D_{M7}}}{I_{F_{M7}} \cdot I_{SPECN_{\blacksquare}}} \tag{3.29}$$

3.2.2.2 Sizing the differential pair

Figure 3.15 highlights transistors M_6 and M_7 that form the differential pair. The structure operates in a closed loop with a negative feedback loop. Therefore the aim is to create a balanced voltage with no voltage difference at the input or a so-called virtual ground.

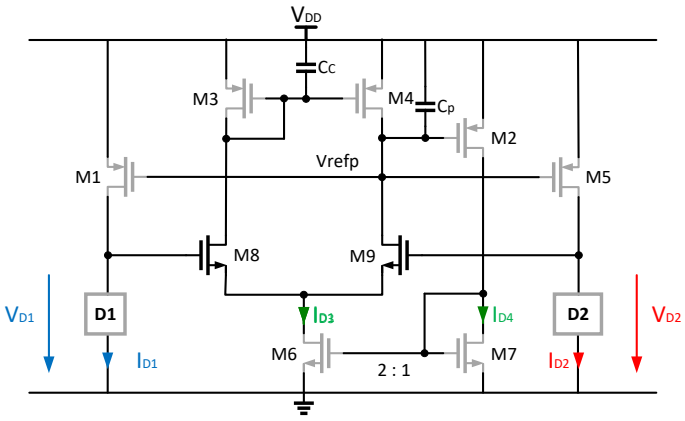


Figure 3.15: Self-biased amplifier: Input differential pair sizing.

The sizes of transistors M_6 and M_7 are known. The next focus point is the differential pair, which is formed by transistors M_8 and M_9 and will mainly contribute to the gain and bandwidth of the OTA through its transconductance. In order to maximize its efficiency, it must operate in deep weak-inversion: $I_{F_{M9,M8}} < 1.10^{-4}$. This is a good starting point, and can be adjusted in a later design verification. Transconductance is determined as follows:

$$gm_{M9,M8} = I_{Bias} \cdot \frac{1}{n \cdot u_T} \cdot \frac{1}{1+\sqrt{1+4 \cdot I_{F_{M9,M8}}}} = 2 \cdot \pi \cdot GBW \cdot \left(C_{GS_{M1}} + C_{GS_{M2}} + C_{GS_{M5}} + C_p\right) \quad (3.30)$$

This in fact sets the following aspect ratio:

$$\frac{W_{M9,M8}}{L_{M9,M8}} = \frac{I_{D_{M7}}}{I_{F_{M9,M8}} \cdot I_{SPECN_{\blacksquare}}} \quad (3.31)$$

3.2.2.3 Sizing the top current mirror

The last block to design is the active load formed by a current mirror operating in a moderate to strong inversion and saturation regime. This leads to an inversion factor greater than 1 $\left(I_{F_{M1,M5,M2,M3,M4}} \geq 1\right)$. Figure 3.16 highlights these transistors. To understand the constraints in the case of a current-controlled dynamic charge, it is important to know the topology and to regulate a current mirror to determine which source will be sensitive to the ripple. Thus, setting the gain of the OTA to $A_V = 100$, the amplitude of the ripples will be attenuated by 100.

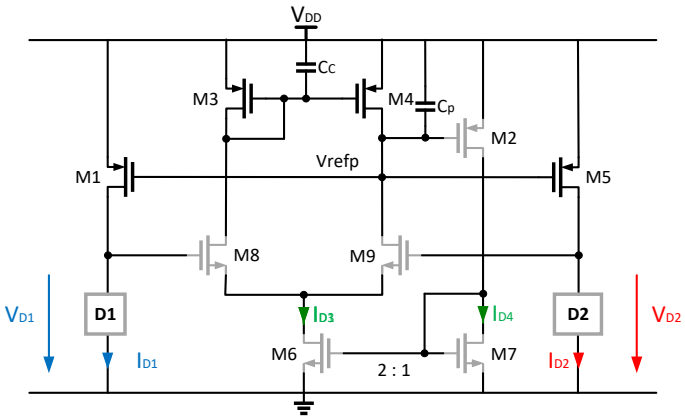


Figure 3.16: Self-biased amplifier: Active load and current mirror sizing constraints.

The amplifier open-loop gain is defined in Eq. 3.32, with the differential pair transconductance and impedance at its output.

$$A_V = g_{ms_{M8,M9}} \cdot R_{out} \tag{3.32}$$

In our OTA, output resistance (R_{out}), is formed by the resistance seen from and combined in parallel as

$$R_{out} = \frac{R_{DW} \cdot R_{UP}}{R_{DW} + R_{UP}} \sim \frac{1}{g_{ds_{M3,M4}}} \tag{3.33}$$

$$R_{UP} = \frac{1}{g_{ds_{M3,M4}}} \tag{3.34}$$

$$R_{DW} = \frac{1}{g_{ds_{M8,M9}}} \cdot \left(1 + \frac{1}{g_{ds_{M7}}} \cdot g_{ms_{M8,M9}}\right) \sim \frac{1}{g_{ds_{M8,M9}}} \tag{3.35}$$

The main contributors to the output resistance (R_{out}) are the active load transistors M_3 and M_4. Thus the sizing constraint using Eq. 2.14 to determine the gate lengths of transistors M_3 and M_4 is

$$L_{M3,M4} = \frac{I_{D_{M3,M4}} \cdot R_{out}}{2 \cdot V_{A_{PMOS}}} \tag{3.36}$$

Equation 3.37 provides the required aspect ratio :

$$\frac{W}{L}_{M3,M4} = \frac{\frac{I_{D_{M3,M4}}}{2}}{I_{F_{M3,M4}} \cdot \frac{I_{D_{M7}}}{I_{F_{M9,M8}} \cdot I_{SPECP_{\blacksquare}}}} \tag{3.37}$$

3.2.2.4 Adaptive biasing a positive feedback loop and stability conditions

Figure 3.17 shows the ratio between transistors M_6 and M_7 to be a factor 2, as highlighted in [267].

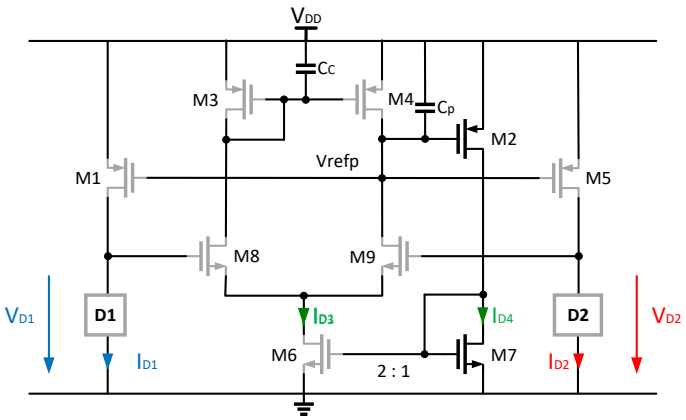


Figure 3.17: Self-biased amplifier: Positive feedback loop stability analysis.

A cautious analysis of the positive feedback was proposed in [need citation here]. The phase margin of this circuit is adjusted by the capacitor C_p, the value of which is determined by the following stability analysis. In the context of a self-biased band gap, it was proposed in [268] that an analysis be performed in agreement with our breakdown into two loops for this system. The positive feedback loop is made on the biasing part of the OTA realized by M_2, M_6 and M_7 and but also contributes to the open loop gain. Figure 3.18 proposes the location to open the loop such that we obtain the positive feedback open-loop gain and the closed-loop feed.

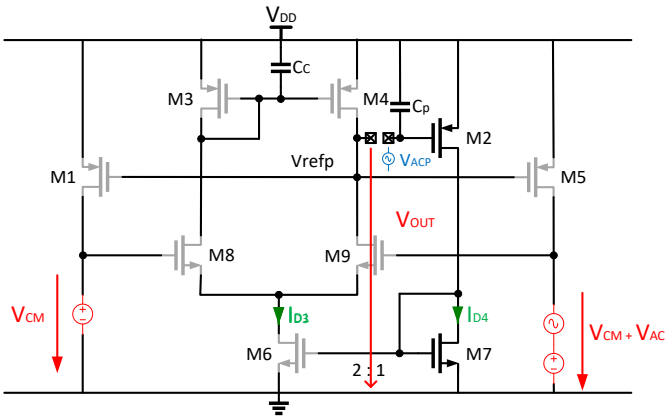


Figure 3.18: Self-biased amplifier: Positive feedback loop stability verification.

Equation 3.38 express positive feedback loop gain.

$$K_{V_p} = \frac{V_{out}}{V_{AC}} = \frac{C_P}{C_C} \cdot \frac{g_{m_{M8}}}{g_{m_{M4}}} \cdot \frac{g_{m_{M5}}}{g_{m_{M6}}} \cdot \frac{g_{m_{M7}}}{g_{m_{M9}} + g_{m_{M8}}} \tag{3.38}$$

The second loop stabilizes the circuit, providing a negative feedback loop. The open loop gain is expressed as

$$K_{V_n} = \frac{V_{out}}{V_{AC_P}} = \frac{g_{m_{M8}} \cdot g_{m_{M1}} Z_{D1}}{g_{ds_{M4}}} \tag{3.39}$$

The gain bandwidth product of the OTA should be chosen to be approximately 1/10 of the oscillating frequency in order to keep the topology stable. The dominant pole of the topology is governed by the capacitor C_C, the value of which is determined by

$$C_C \geq \frac{g_{m_{M8}} \cdot 10}{2 \cdot \pi \cdot F_{osc}} \tag{3.40}$$

Moreover, the dominant pole of the system is derived as follows :

$$F_{p1} = \frac{g_{ds_{M4}}}{2 \cdot \pi \cdot C_C} \tag{3.41}$$

In addition, a first non-dominant pole of the system is derived with

$$F_{p2} = \frac{g_{m_{M8}} \cdot g_{m_{M1}} Z_{D1}}{2 \cdot \pi \cdot C_P} \tag{3.42}$$

and the gain bandwidth of the system is derived with

$$GBW = K_{V_n} \cdot F_{p1} = \frac{g_{m_{M8}} \cdot g_{m_{M1}} Z_{D1}}{2 \cdot \pi \cdot C_C} \tag{3.43}$$

This leads to a pole-splitting condition while adjusting capacitor C_p with respect to capacitor C_C or vice versa. A condition can be established such that

$$C_C \geq C_P \cdot \frac{g_{m_{M8}}}{g_{m_{M4}}} \cdot \frac{g_{m_{M5}}}{g_{m_{M6}}} \cdot \frac{g_{m_{M7}}}{g_{m_{M9}} + g_{m_{M8}}} \tag{3.44}$$

To illustrate the above derivation, let us examine the negative and positive feedback gains with a variation of capacitance C_C, while considering a fixed value of $C_P = 1pF$ as shown in Figure 3.19(a). The phase margin and gain-bandwidth products were also extracted from simulations and are shown in Figure 3.19(b).

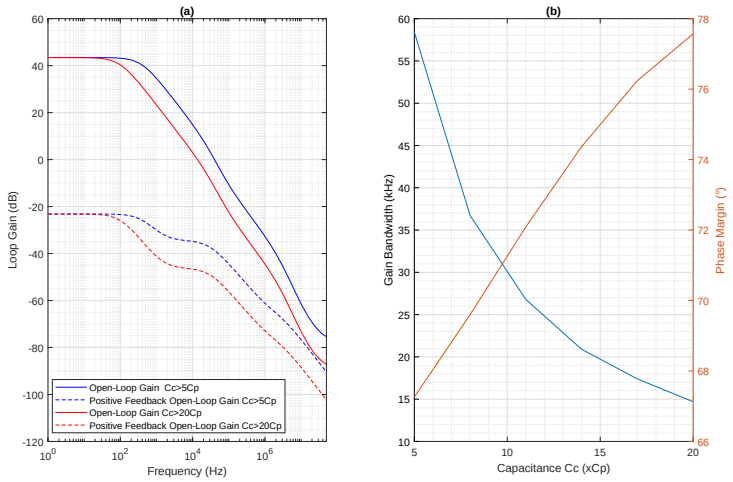


Figure 3.19: Self-biased amplifier : Positive feedback loop stability. Pole-splitting verification.

As expected and shown, GBW decreases with increasing capacitance C_C, which in turn increases the phase margin.

3.2.2.5 Self-biased OTA large signal consideration

The large signal consideration of the self-biased OTA is important to determine the operational limits of the circuit, given the structural sizing methodology proposed above. Equation 3.45

expresses the headroom limit of the circuit :

$$V_{DD} \geq \max \begin{cases} V_{D1} + V_{DSAT_{M4}} \\ V_{T_{M6}} + \left(V_{D1} - V_{T_{M6}}\right) + V_{DSAT_{M4}} \end{cases} \tag{3.45}$$

Essentially it takes into account the fact that transistors are operating in the saturation region and that the dipole voltage sets the input range of the amplifier. Given 180 nm node parameters in Table 2.2, an approximation of the minimal supply voltage is

$$V_{DD} \sim\geq V_{DX} + 200\text{mV} \tag{3.46}$$

This structure could support a larger voltage scaling than the structure reported in Section 3.2.1.2.

3.2.3 Outcomes of the guidelines

An analysis has been performed that, though not exhaustive, highlights each of the main topology properties and design guidelines that are applicable to designing self-biased circuits. As each circuit is specific for each case, further effects are solved approximately with verification methods based on transistor level models. These design guidelines would benefit greatly from a methodology perspective to produce a specification-compliant design and reduce the time spent analyzing the corner case by initially checking the corner case parameter extracted in the framework as proposed in Table 2.2.

3.3 Design guidelines for a fully integrated RC reference oscillator

The background on duty-cycling and time tracking in IoT was discussed in Section 1.1. This work also provides a study of the variability of ring oscillator frequency in Section 2.2.2.1. This chapter extends the contributions proposed in [269] and [270], where the thermal compensation strategy of Section 3.3.3 was first presented. Accurate knowledge of the physics behind a performance is often the correct way to achieve the expected performance through a system-level approach. As proposed above in Section 3.2, we need to know the dipole under consideration. Thus it is proposed to take another look at the $I-V$ relation of the ring oscillator as in Section 3.3.1. The loop conditions are proposed in Section 3.3.2. The thermocompensation mechanism is recalled in Section 3.3.3. Section 3.3.4 conclude s the case on a fully integrated RC reference oscillator.

3.3.1 Ring-oscillator amplitude estimation

Figure 3.20 shows that, each time a PMOS charges the output capacitor, the supply voltage is pulled down and PMOS acts as a diode as long it is saturated.

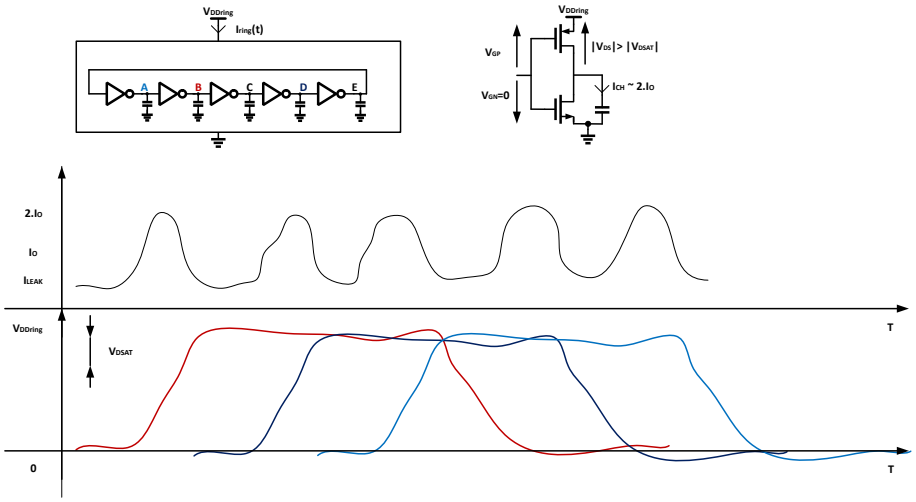


Figure 3.20: Schematic of the inverter in transition

It is worth mentioning that no direct current would punch through PMOS–NMOS if the ring oscillator voltage is close to the threshold voltage. Equation 3.47 estimates the ring-oscillator voltage:

$$V_{RING} \sim \begin{cases} V_{T0} + 2 \cdot n \cdot u_T \cdot \sqrt{I_F} & strong inversion \\ V_{T0} & Moderate - Inversion \\ V_{T0} + n \cdot u_T \cdot \ln(I_F) & weak inversion. \end{cases} \tag{3.47}$$

As shown in Figure 3.20, the channel current when charging the capacitance is twice the bias current. Thus one could estimate the inversion level and deduce the size of the ring oscillator inverter as follows:

$$I_F \sim \frac{I_{CH}}{I_{SPEC_{\blacksquare P}} \cdot \frac{W_P}{L_P}} = \frac{2 \cdot I_0}{I_{SPEC_{\blacksquare P}} \cdot \frac{W_P}{L_P}}. \tag{3.48}$$

3.3.2 Proposed architecture self-biased RC oscillator

The circuit shown in Figure 3.21 consists of a feedback loop containing two dipoles: a resistor and a ring oscillator.

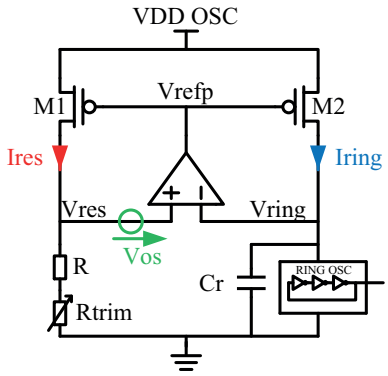


Figure 3.21: Architecture of the proposed RC oscillator

The current mirror balances the DC current flowing in the resistor and the dynamic current supplied to a ring oscillator comprising an odd number of CMOS inverters. The current mirror in fact imposes the following relation:

$$I_{Ring} = I_{Res} \tag{3.49}$$

As mentioned above, the current flowing in the resistor is given by

$$I_{Res} = \frac{V_{Res}}{R} \tag{3.50}$$

As the dynamic current supplied to a ring oscillator comprises an odd number of CMOS inverters, it can be expressed analytically as

$$I_{Ring} = F_{osc} \times C_{eq} \times V_{ring} \tag{3.51}$$

The OTA feedback loop then imposes the following condition on the voltage:

$$V_{Ring} = V_{Res} + V_{os} \tag{3.52}$$

which leads to a beat frequency expressed as

$$F_{osc} = \frac{1}{R \times C_{eq}} \times (1 - \frac{V_{os}}{V_{Ring}}) \tag{3.53}$$

This oscillator is then intrinsically dependent on an RC product. It is potentially possible to reduce the input-referred offset of the amplifier V_{os} in order that its influence on the output frequency is negligible. Section 3.3.3 proposed a thermocompensation mechanism taking advantage of this offset value. As a matter of fact, the oscillation frequency relies on absolute values, which could be trimmed in production, as the capacitance is defined by the inverter gate input capacitance itself.

3.3.3 Temperature behavior

The thermal behavior of this circuit is expected to be fairly dominated by variations of the thermal coefficient of the passive elements R and C. The MOS capacitance temperature coefficient is $-7300\,ppm/°C$, which is too high to achieve a stable oscillation frequency over temperature. For the resistor, it is a tradeoff between high resistivity and thermal behavior. As shown in Figure 2.45, a high resistivity polyresistor is a reasonable choice, but the thermal coefficient of $-1950\,ppm/°C$ is also too high to achieve a stable oscillation frequency for a time reference. To get a complete picture of the thermal dependency, we considered that each element in Eq. 3.54 is subject to temperature drift, the corresponding first-order relative temperature coefficient of the oscillation frequency.

$$T_C = \frac{1}{F_{osc}} \times \frac{\partial}{\partial T} F_{osc} = -T_{CRes} - T_{CCeq} + \frac{1}{V_{ring} + V_{os}} \times (T_{CVos} - T_{CVring} \frac{V_{os}}{V_{ring}}), \quad (3.54)$$

where the temperature coefficients R and C are expressed in $ppm/°C$ and temp coefficients of OTA offset voltage and ring oscillator voltage are expressed in $\mu V/°C$ in the designed OTA. The above result shows that a first-order compensation of the temperature drift can be achieved under specific conditions on the offset voltage. Thus a second-order calibration can be obtained with no additional current branch or circuitry to compensate for the thermal behavior. For a perfectly matched load, there remain two uncorrelated phenomena: random mismatch on the threshold voltage and the geometrical ratio. It could be easily proved that

$$V_{os} = \sqrt{n \cdot u_T \cdot \ln\left[\left(e^{\sqrt{IC}} - 1\right) \cdot \frac{\Delta \frac{W}{L}}{\frac{W}{L}}\right]^2 + \Delta V_T^2}. \quad (3.55)$$

Figure 3.22 shows the structure implementing a structural mismatch element introduced in the differential pair with variable sizes of transistors M8 and M9.

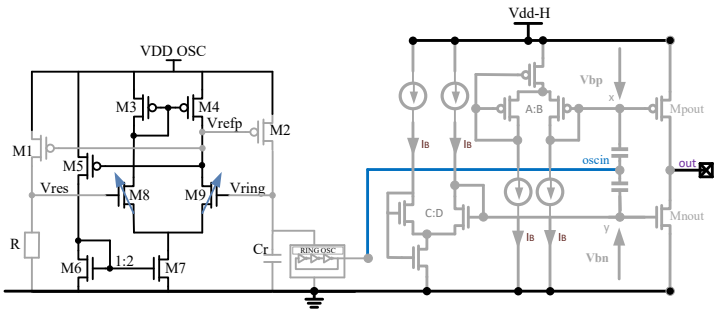


Figure 3.22: Transistor-level implementation of the RC oscillator

The structural offset was implemented in a binary weighted fashion (M8.i, M9.i) including W, which is between 0 and 31 times more than the other side of the differential pair. Figure 3.23, shows the transistor level implementation.

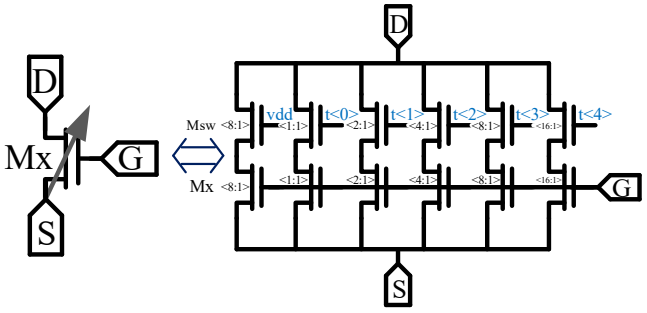


Figure 3.23: Transistor-level implementation of the differential pair.

The effectiveness was verified, and the silicon results are provided in Section 4.2.1.2.

3.3.4 Amplitude selection in self-biased resistor-capacitor frequency reference

Generating a clock-signal, i.e. an alternating digital signal with stable and controlled frequency, is generally done in two steps as depicted in Figure 3.24.

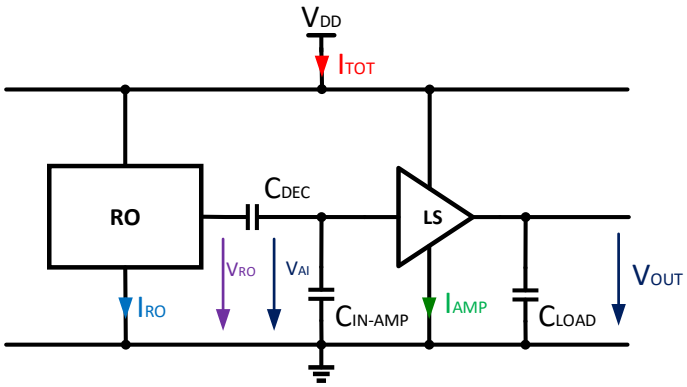


Figure 3.24: Architecture diagram for amplitude tradeoff

1. Oscillator function (RO): Generates a first signal that is alternating, has a stable frequency but is rarely compliant with the digital specification of a signal.

2. Clock amplifier function (LS): Amplifies and limits ("level-shifts") the first signal to make it compliant with the digital specification of a signal.

Both consume current and therefore power. The attempt to minimize the power consumed by the former usually comes at the cost of increased power consumption in the latter. We want to minimize the overall consumption under certain conditions. As shown in Eq. 3.51, reducing the oscillator's output-signal amplitude reduces its current-consumption, but increases the clock-amplifier's noise contribution according to the results presented in Figure 1.12. For the CMOS ring oscillator, Eq. 1.25 presents the fundamental limitations of the phase noise extracted from [59] based on the linearized empirical models presented in [84, 85]. Considering subthreshold jitter, Ref. [271] proposes the jitter model of a CMOS ring oscillator in subthreshold as follows:

$$\sigma_{jro} = \sqrt{\frac{q}{f_o^2 \cdot \sum C_{node} \cdot V_{ring}} \cdot \left[1 + e^{\frac{V_{ring}}{2 \cdot u_T}}\right]}. \tag{3.56}$$

Figure 3.25 visualizes the contributions to the jitter in a particular case at 32,768 kHz in a five-stage ring oscillator and a level sifter compatible with 1.8 V CMOS logic.

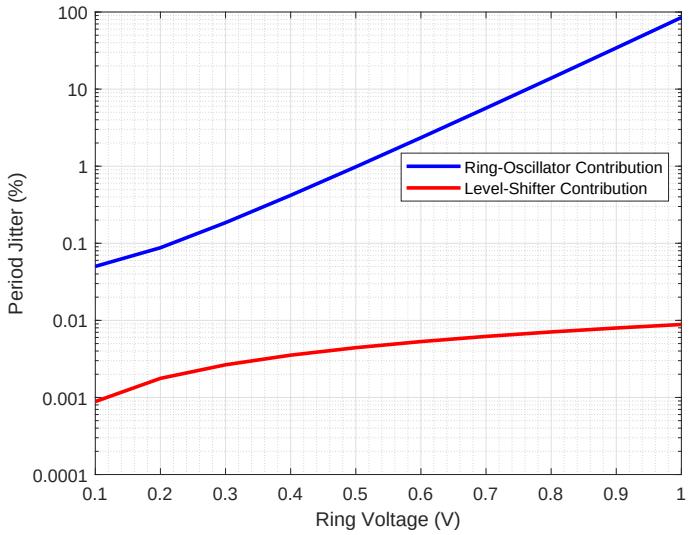


Figure 3.25: Tradeoff between the ring oscillator voltage and the period jitter

For the level shifter, a Class A-B amplifier structure is presented in Figure 3.26.

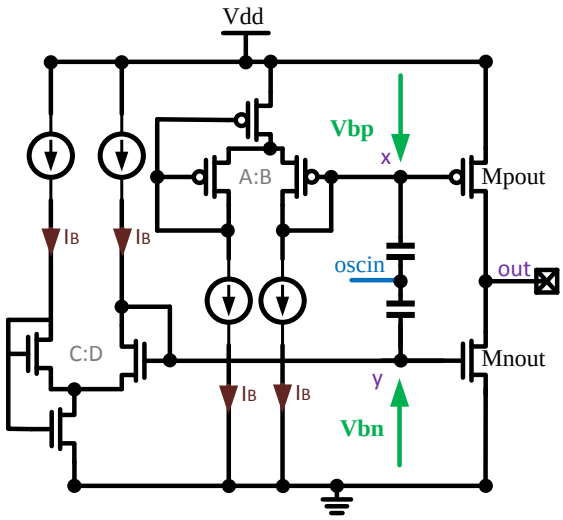


Figure 3.26: Clock extraction class-AB amplifier

The noise contribution of the RC oscillator and its level converter is shown in Figure 3.25. The contribution of the level converter shown in Figure 1.12 is negligible compared to that of the oscillator. In fact, the optimization is based on the phase noise criterion of the oscillator itself for a given amplitude as well as the total consumption presented in Figure 3.27.

The overall oscillator structure consumption can be estimated from Eq. 3.26, whereas the level

sifter amplifier shown in Figure 3.26 as presented in [233] consumes $I_{LS} = 5 \cdot I_B$. In principle, the output transistor imposes the current mirrored from the transconductor for voltages V_{Bp} and V_{Bn}. When the input voltage tends to zero, the amplifier enters the region where the PMOS charges the output capacitor, the supply voltage is reduced and the PMOS acts as a diode with an average current of $I_P = 2 \cdot I_B$. Conversely, the NMOS reduces the output voltage such that the output stabilizes at $V_{out} = \frac{V_{DD}}{2}$. Figure 3.27 shows the trade-off between the amplitude of the ring oscillator and its power consumption as well as that of the level sifter.

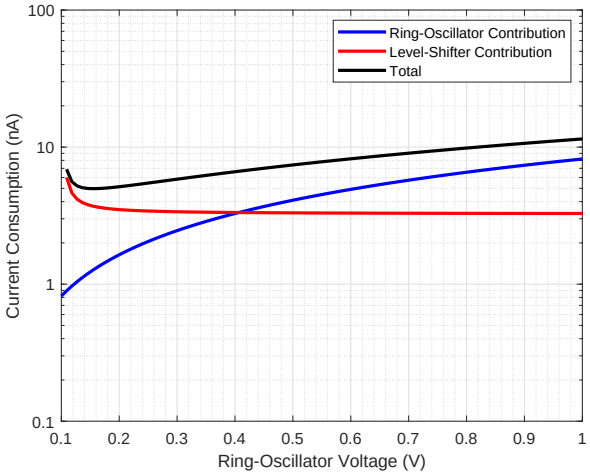


Figure 3.27: Trade-off between the ring oscillator voltage and the total power consumption

The example is numerical but could be applied to any frequency and ring oscillator size. Nevertheless it reveals a sweet spot in amplitude ranging from $V_{RING} = [0.3 - 0.4]\ V$, where the ring oscillator amplitude enables savings with respect to the level-sifter consumption.

3.4 Design guidelines for resonator-based frequency reference

In this section we introduce the background of the Pierce oscillator, which has proved to be suitable for low-power appliances. As shown by Eq. 1.14, the amplitude regulation and frequency stability have a direct relation. Therefore we also exploited this property and altered the structure to realize an ultra-low-power, self-biased, amplitude-regulated crystal oscillator. We will first revisit the principles behind the Pierce oscillator and the amplitude regulation in Section 3.4.1, then analyze the phase noise in Section 3.4.2, and finally examine the regular design steps in Section 3.4.3. Further design steps are expressed in the context of a real-time clock module that proposes a novel self-biased crystal oscillator in Section 4.4, which includes measurements and validations.

3.4.1 Revisiting the Pierce oscillator and amplitude regulation

A crystal resonator is a resonant circuit with some motional attenuation, as modeled by series resistors on RLC circuits in Figure 3.28b. This motional resistor in the case of a 32.768 kHz

crystal would range between 20 k and 100 k under vacuum conditions. The assembly of the crystal and the chip in the same package requires an additional test under atmospheric pressure, thus causing the motional resistor (ESR) to surge as high as 1 M. Therefore, such oscillators should implement a mode that cancel such a high motional resistor. We consider the series resonant circuit to be a current mode resonator.

The active circuit provides an impedance of $Z_c(j\omega)$ to the resonator. As the circuit is nonlinear, the voltage across the motional branch may be distorted, but the current flowing through the motional branch will be sinusoidal due to the high-Q and the subsequent filtering action of the resonator. Therefore, the energy exchange between the active circuit and the motional branch of the resonator takes place only at the fundamental frequency. Thus a first-harmonic model could be sufficient, and the impedance of the active circuit can be defined.

A linear analysis of the Pierce oscillator was also performed, the schematic of which is shown in Figure 3.28a. This schematic illustrates a general case with impedances Z_1, Z_2, and Z_3 that represent the capacitances and their parasitics.

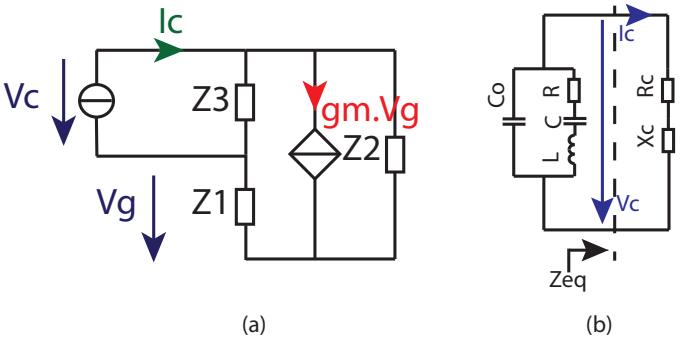


Figure 3.28: Pierce oscillator

The lossless expression will account for the impedances $Z_1 = C_1 + j \cdot G_1$, $Z_2 = C_2 + j \cdot G_2$, and $Z_3 = C_3 + j \cdot G_3$ as pure capacitance, and considers $Z_1 = C_1$, $Z_2 = C_2$, and $Z_3 = C_3$, as shown in Figure 3.29. Thus it provides the simplified algebraic expression of the impedance derived from Equations 3.57 to 3.58.

$$Z_c(j\omega) = \frac{Vc}{Ic}. \tag{3.57}$$

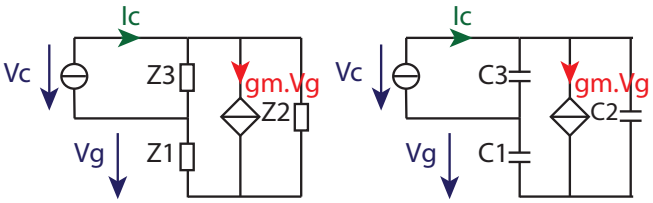


Figure 3.29: Pierce oscillator small signal lossless model

$$Z_c(j\omega) = \frac{G_m + j\omega(C_1 + C_2)}{\omega^2 \cdot (C_1 \cdot C_2 + C_1 \cdot C_3 + C_2 \cdot C_3) - j\omega \cdot G_m \cdot C_3}. \tag{3.58}$$

Note that the above input impedance of the Pierce oscillator is an interesting bi-linear impedance $Z_C(\omega, gm)$, which can be presented in its complex form $Z_C(\omega, gm) = Re\left[Z_C(j\omega)\right] + j \cdot Im\left[Z_C(j\omega)\right]$ and extracted such that the real part is given in Eq. 3.59 and its imaginary part in Eq. 3.60. These depend on load capacitances C_1, C_2, the case of parallel capacitance C_3, and the trans-conductance elements gm.

$$Re\left[Z_C(j\omega)\right] = R_c = -\frac{g_m \cdot C_1 \cdot C_2}{\omega^2 \cdot (C_1 \cdot C_2 + C_1 \cdot C_3 + C_2 \cdot C_3) + (g_m \cdot C_3)^2}, \tag{3.59}$$

$$Im\left[Z_C(j\omega)\right] = X_c = -\frac{g_m^2 \cdot C_3 + \omega^2 \cdot (C_1 \cdot C_2 + C_1 \cdot C_3 + C_2 \cdot C_3) \cdot (C_2 + C_1)}{\omega \cdot \left[\omega^2 \cdot (C_1 \cdot C_2 + C_1 \cdot C_3 + C_2 \cdot C_3) + (g_m \cdot C_3)^2\right]}. \tag{3.60}$$

Figure 3.30 shows the polar plot of the impedance equivalent to the Pierce oscillator input, where the abscissa represents real part of the impedance and the ordinate represents the real part of the Pierce oscillator input impedance. The locus is drawn at a fixed frequency or pulsation ω, yet their an implicit variable is the oscillator transconductance gm.

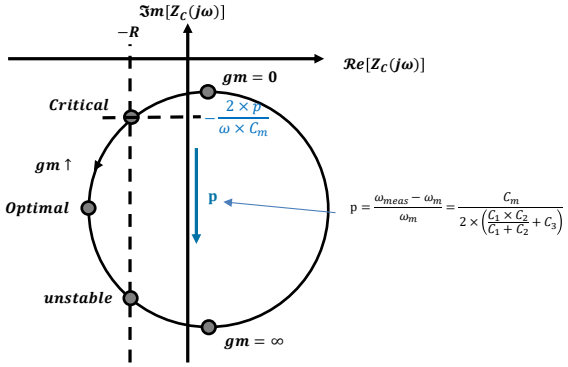


Figure 3.30: Resonator and circuit modeling

The locus finds interesting operating regimes when the circuit is not started. Hypothetically there is no transconductance and the input impedance is positive, whereas by increasing the transconductance, we find a first operating point, called the critical operating point, where the input impedance of the Pierce oscillator cancels the motional resistance of the resonator

such that it continues to oscillate. The condition on the transconductance is

$$G_{mcrit} \sim \frac{\omega \cdot C_m}{Q \cdot p_c^2} \cdot \frac{(C_1 + C_2)^2}{4 \cdot C_1 \cdot C_2}. \tag{3.61}$$

of the locus impose an optimal value for the transconductance defined as :

$$G_{mopt} \sim \frac{\omega \cdot (C_1 \cdot C_2 + C_1 \cdot C_3 + C_2 \cdot C_3)}{C_3}. \tag{3.62}$$

This usually defines an upper boundary for the transconductance, after which the input resistance decays and finds one more operating point, called the maximum transconductance, as in Eq. 3.63. Further increasing the transconductance will simply degrade the oscillator circuit input equivalent impedance to a point that it could not oscillate.

$$G_{mmax} \sim \frac{\omega \cdot C_m \cdot C_1 \cdot C_2 \cdot Q}{C_3^2}. \tag{3.63}$$

This analysis does not account for the losses and thus this number will rather underestimate the transconductance needed. Nevertheless accounting for the losses does not provide an analytical solution. Figure 3.31 shows a summary of potential CMOS implementations of a transconductance, as well as the supply voltage required.

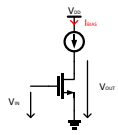
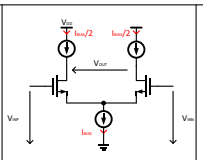
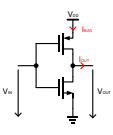
			
	Common Source	Differential Amplifier	CMOS INVERTER
Equivalent trans-conductance weak-inversion	$g_{eq} = \frac{i}{V} = g_m \sim \frac{I_{bias}}{n \times u_T}$	$g_{eq} = \frac{i}{V} = g_m \sim \frac{I_{bias}}{2 \times n \times u_T}$	$g_{eq} = \frac{i}{V} = g_{mp} + g_{mn} \sim \frac{2 \times I_{bias}}{n \times u_T}$
Headroom voltage	$\Delta V_{min} = V_{th} + V_{DSAT}$	$\Delta V_{min} = V_{th} + V_{DSAT}$	$\Delta V_{min} = u_T \cdot \ln(n \cdot \lvert A_v \rvert)$

Figure 3.31: CMOS Implementation of a transconductor

As shown in Figure 3.31, a fundamental property of the weak-inversion regime is the direct relationship between transconductance and the quiescent current for a common source amplifier:

$$I_q = n \cdot U_T \cdot g_{ms}. \tag{3.64}$$

Therefore, optimizing current consumption requires, on the one hand, minimizing the capacitance and the oscillation amplitude such that the current consumption will linearly decrease. On the other hand, a further reduction of the transconductance optimizes the quiescent current as shown. Extracting the highest transconductance from an architectural perspective is the current recycling technique, where a CMOS inverter naturally forgoes any overhead because PMOS and NMOS currents are shared and transconductance accumulates. To obtain a similar carrier mobility, we adjusted this value by increasing the PMOS two to three times more significantly than the NMOS will enable us to double the value of gm for the same invested current. This technique was used in [272]. It is important to note that the selection of the capacitances pushes or pulls the XO frequency. The pulling factor is given by Eq. 3.65, which defines the relative error with respect to the resonance tone:

$$p_c = \frac{\omega_0 - \omega_m}{\omega_m} = \frac{C_m}{2 \cdot \left(C_3 + \frac{C_1 \cdot C_2}{C_1 + C_2}\right)}. \tag{3.65}$$

It depends on the motional capacitance C_m, the case capacitance C_3, and the load capacitances C_1 and C_2, which can be adjusted by reducing the dynamic power consumption and trading power consumption for frequency accuracy. One could define the series association of the capacitances $C_1$and C_2 as $C_s = \frac{C_1 \cdot C_2}{C_1 + C_2}$. As a consequence, crystal fork initial laser trimming is required in order to adjust the central frequency crystal tuning fork specification to benefit from a ppm-level accuracy. Section 3.4.3.3 presents our numerical results of the case study further described in Section 4.4.

Figure 3.32 proposes an amplitude-regulated crystal oscillator proposed in [229], based on the original publication of [224]. It is interesting to note that the core oscillator and amplitude regulation concept stayed stable, but the post-amplifier structure was modified to a biased CMOS inverter from one publication to another. The CMOS inverter biasing scheme presented in Figure 3.32 differs from the scheme presented in [229], but is conceptually similar and detailed in Section 2.50.

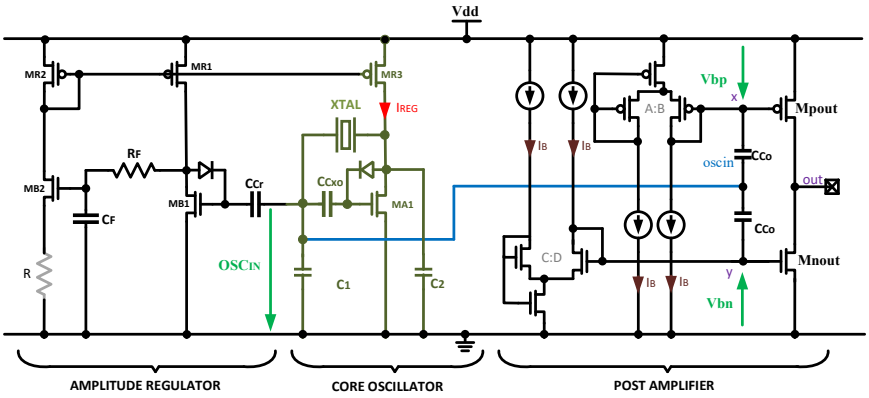


Figure 3.32: Amplitude-regulated crystal oscillator [229]

As the oscillation grows, it is usually limited first by the nonlinear transfer function of the active device, as illustrated in (3.66):

$$\frac{I_D}{I_{spec}} = e^{\frac{v_g - v_t + |v_{oscin}| \cdot \sin(\omega t)}{u_T}}. \tag{3.66}$$

The DC component of the drain current is obtained by averaging (3.66) over one period:

$$\langle \frac{I_D}{I_{spec}} \rangle = e^{\frac{v_g - v_t}{u_T}} \times \frac{1}{2\pi} \int_{-\pi}^{\pi} e^{\frac{|v_{oscin}|}{nu_T} \cdot sin(\omega t)} . d\omega t \tag{3.67}$$

This analytically leads to a tabulated function called the modified Bessel function of order 0:

$$\left\langle \frac{I_D}{I_{spec}} \right\rangle = e^{\frac{v_g - v_t}{u_T}} \times \left\{ 1 + \frac{v_1^2}{2^2} + \frac{v_1^4}{2^2 \cdot 4^2} + \frac{v_1^6}{2^2 \cdot 4^2 \cdot 6^2} + \ldots \right\} \tag{3.68}$$

These properties are reused in the basic amplitude regulation (PMOS version) of the original publication as presented in [224]. The transistor MR1 is saturated by construction, and we operated this transistor in weak inversion. For the above-mentioned calculation to be valid for its distortion, we filtered out the harmonics content using the following RC filter. Thus to express the drain current flowing in MR2 on average, we need to change only one variable $\theta = \omega \cdot t$:

$$\langle I_{DMR2} \rangle = \frac{S_{MR2}}{S_{MR1}} \cdot \frac{S_{MB2}}{S_{MB1}} \cdot I_{DMR1} \cdot \frac{1}{2\pi} \cdot \int_{-\pi}^{\pi} e^{\frac{|U_{MR1}|}{u_T} \cdot sin(\theta)} . d\theta. \tag{3.69}$$

We can recognize that the 0-order modified Bessel function the solution is tabulated. Equating $\langle I_{D1} \rangle$ to I_{D3} leads to

$$I_0(x) = \frac{1}{2\pi} \int_{-\pi}^{\pi} e^{\frac{U_1}{nu_T} sin?(\theta)} .d\theta = \frac{S_{MR2}}{S_{MR1}} \times \frac{S_{MB2}}{S_{MB1}}. \tag{3.70}$$

The Bessel tabulation is as follows :

$x = \frac{\lvert U_{g_{T1}} \rvert}{nu_T}$	$I_0(x)$	$\lvert U_{g_{T1}} \rvert$
1	1.26	31 mV
2.5	3.29	85 mV
3	4.88	94 mV
3.5	7.37	110 mV
4	11.3	125 mV
4.5	17	141 mV
5	27	156 mV

A standard amplitude-regulated XO is presented in Figure 3.32 as reported in [224]. Nonlinearity induced a drop in VG at MR1 sensed by MR2. During startup, the bias current $\frac{U_T}{R_b} \cdot \ln(K)$ in Eq. 3.71 decreases as the oscillator amplitude settles over time in accordance with $\frac{\ln(IBO(x))}{\ln(K)}$ in Eq. 3.71, where $x = \frac{\hat{V_{osc}}}{n \cdot U_T}$, $\hat{V_{osc}}$ is the peak amplitude, which is regulated. The term K is the aspect ratio between transistors MR2 and MR1 as shown in Figure 3.32, and IBO is the 0-order modified Bessel function, which is a tabulated function of x. Note that this circuit complexity (only four transistors, one diode, two resistors, two capacitors) impose the amplitude regulation level by the aspect ratio between transistors MR2 and MR1.

$$I_{D_{MB1}} = \frac{U_T}{R_b} \cdot \ln(K) - \frac{\ln\left(IBO\left(\frac{\hat{V_{osc}}}{n \cdot U_T}\right)\right)}{\ln(K)}. \tag{3.71}$$

As shown in Figure 3.33, the crystal oscillator and the amplitude regulator find their operating point such that for a given current, the peak amplitude is regulated.

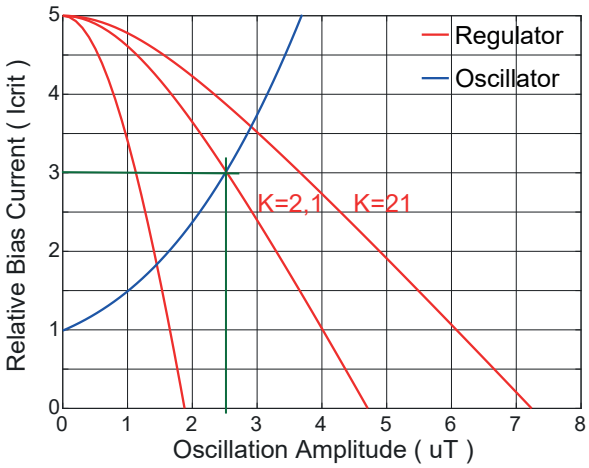


Figure 3.33: Amplitude regulator and oscillator characteristic coupling

The DC current is obtained by Eq. 3.72, which could be of particular interest in the start-up sequence.

$$I_o = \frac{u_T \times \ln(\frac{S_{MR2}}{S_{MR1}} \times \frac{S_{MB2}}{S_{MB1}})}{R}. \tag{3.72}$$

As we need to provide current at the start-up, this could be sized in order to sustain a start-up condition. Note that, when the oscillation is sustained, the source voltage tends to zero, so there is no direct current injected, which is also advantageous because it cuts its own consumption.

3.4.2 Analysis of the phase noise

An oscillator based on a high-Q resonator has two sources of thermal noise as shown in Figure 3.34.

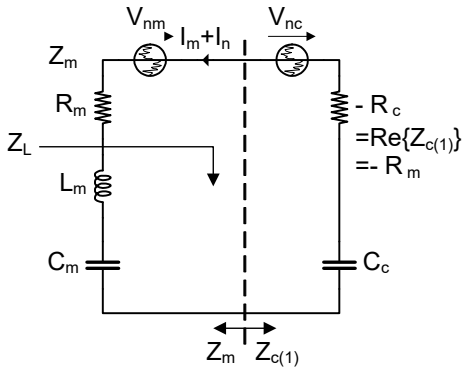


Figure 3.34: Resonator and circuit modeling

One noise source is the motional resistance of the resonator, whose thermal noise voltage PSD is given by

$$S_{VNM} = 4 \cdot k \cdot T \cdot R_M. \tag{3.73}$$

The second is the noise coming from the active circuit. This noise has a voltage PSD of

$$S_{VNM} = 4 \cdot k \cdot T \cdot R_M \cdot \gamma, \tag{3.74}$$

where γ is the noise excess factor and depends on the bias current flowing through the active circuit. The impedance seen by the total noise voltage source with a PSD is

$$S_{VN} = 4 \cdot k \cdot T \cdot R_M \cdot (1+\gamma). \tag{3.75}$$

The impedance seen by the total voltage noise source towards the output at frequencies close to the frequency of oscillation ω_0 is

$$Z_L = 2 \cdot j \cdot Q_m \cdot R_m \cdot \frac{\omega - \omega_0}{\omega_m} = 2 \cdot j \cdot Q_m \cdot R_m \cdot \frac{\Delta\omega}{\omega_m}, \tag{3.76}$$

where $Q_m = (\omega_m L_m)/R_m = 1/(\omega_m R_m C_m)$ is the quality factor of the motional branch. Therefore, the noise current PSD in this loop is $4kTR_m(1+\gamma)/\left|Z_L^2\right|$. The phase noise is obtained by normalizing this noise PSD to the square of the RMS value of the motional current. The phase noise is then given by

$$\mathscr{L}(\Delta\omega) = \frac{1}{2} \cdot \frac{S_{I_n^2}}{(|I_m| \cdot \sqrt{2})^2} = \frac{(1+\gamma) \cdot k \cdot T \cdot \omega^2}{Q_m^2 \cdot R_m \cdot |I_m|^2 \cdot (\Delta\omega)^2}. \tag{3.77}$$

The factor 0.5 is due to the fact that the noise is equally divided between noise in the amplitude and noise in the phase. The thermal noise thus varies inversely with the square of the offset frequency $\Delta\omega$, exhibiting a -20 dB slope as illustrated in Figure 3.35. The flicker noise of the circuit arises from the up-conversion of the noise at DC due to the inherent non-linearity of the transistor. This phenomenon is best described by using the impulse sensitivity function theory by Hajimiri *et al.* [273]. The expression for flicker noise is

$$\mathscr{L}(\Delta\omega) = \frac{1}{2} \cdot \frac{\overline{\Gamma}^2 \cdot K_{fi}}{(C_c V_{C_C})^2 (\Delta\omega)^3} \cdot \left(\frac{C_m}{C_c}\right)^2, \tag{3.78}$$

where $\overline{\Gamma}$ is the average value of the impulse sensitivity function (ISF). The flicker noise thus varies inversely with the cube of the offset frequency $\Delta\omega$, exhibiting a -30 dB slope with respect to the frequency offset. This is well illustrated in Figure 3.35.

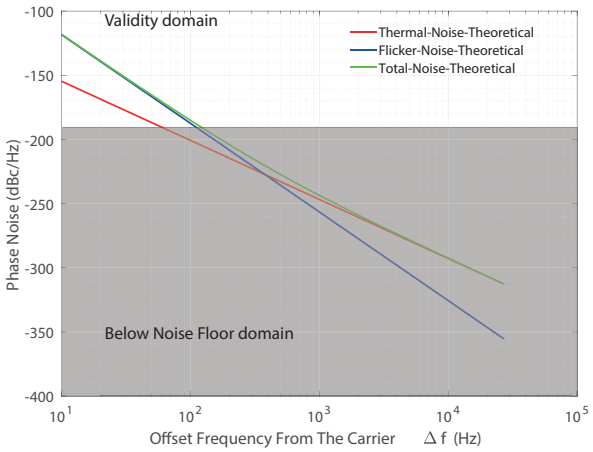


Figure 3.35: Numerical application of the Hajimiri *et al.* [273] phase noise model

An important note for the Pierce oscillator flicker noise is to consider the motional capacitance C_m and the oscillator input capacitance C_c that will form the corner frequency offset contribution. This phase noise theoretical analysis is confronted with our measurement results in Section 4.4.1.4.

3.4.3 Crystal-oscillator design steps

The design methodology for the Pierce oscillator has been proposed in multiple scientific articles [224, 274, 275, 229, 276, 277, 61] and books [278] and has proved be suitable for low-power appliances. This motivated us to recall the generally agreed design steps while inserting our assertions implemented and verified in Section 4.4.

3.4.3.1 Resonator selection

The choice is often limited by the available components at vendors. Nevertheless there are a few criteria that would support the selection. An obvious requirement is the desired frequency of oscillation. Another highly important aspect is their temperature dependence. An interesting observation is that the cut angle and the temperature dependency slope have nearly the same angle [279]. For the original electronic wristwatch, watchmakers considered using a plain bar of crystal with a large resonator oscillating at 8 kHz [229]. Soon thereafter, the low-frequency crystal resonator was optimized in terms of size with resonators oscillating in flexural mode (possibly in the form of a tuning fork). The temperature performance of a tuning fork is poor compared to a high-frequency crystal, which can use a thickness-resonant mode of either shearing or expansion, called the ZT or AT cut.

The resonator is modeled by series resistors on RLC circuits as presented in Figure 3.28b. It is rare to have the value of each component. Nevertheless the series resistance or quality factor (Q) and parallel capacitance already provide a good starting point.

3.4.3.2 Calculating the minimum start-up time

The longest start-up time of an oscillator corresponds to starting from complete rest, with oscillation building up from noise only. As we will consider here only the very beginning of the build-up, the system could be considered fully linear. The results are derived from [280]. The first important relation describes the evolution with time of the variance of the voltage across a resonant circuit (tank) as the square of the RMS value:

$$V^2(t) = 2 \cdot k \cdot T \cdot \left(1 - \frac{G_n}{G_p}\right) \cdot G_p \cdot \left(1 + \gamma\right) \times \int_0^t h^2(t).dt \tag{3.79}$$

where k is the Boltzmann constant, T the temperature, G_n the active part (oscillator) negative conductance, G_p the resonator conductance, $h(t)$ the impulse response of the system and γ the noise factor of the transconductance. After integration, this translates into

$$V^2(t) = \frac{2 \cdot k \cdot T \cdot (1+\gamma)}{C} \cdot \left[1 - e^{\frac{\sqrt{\frac{L}{C}} \cdot (G_p - G_n)}{\sqrt{L \cdot C}} t} \cdot (1 - \frac{\frac{\sqrt{\frac{L}{C}} \cdot (G_p - G_n)}{\sqrt{L \cdot C}}}{2 \times \frac{1}{\sqrt{L \cdot C}} - \left(\frac{\frac{\sqrt{\frac{L}{C}} \cdot (G_p - G_n)}{\sqrt{L \cdot C}}}{2} \right)^2} \cdot \sin\left(\frac{1}{\sqrt{L \cdot C}} - \left(\frac{\frac{\sqrt{\frac{L}{C}} \cdot (G_p - G_n)}{\sqrt{L \cdot C}}}{2} \right) \right) \right] \tag{3.80}$$

We can identify a few parameters to simplify, such as the resonant pulsation $\omega_o = \frac{1}{\sqrt{LC}}$, the resonant impedance $Z_o = \sqrt{\frac{L}{C}}$, the quality factor $Q = \frac{1}{Z_o \times (G_p - G_n)}$, and the bandwidth $B = \frac{\omega_o}{Q}$. We could then define the half bandwidth geometric distance such as $\omega_1^2 = \omega_o^2 - \left(\frac{B}{2}\right)^2$, which could then be simplified as follows:

$$V^2(t) = \frac{2 \cdot k \cdot T \cdot (1+\gamma)}{C} \cdot \left| 1 - e^{-Bt} \times \left(1 - \frac{B}{2\omega_1} \times \sin\left(\omega_1 t\right) \right)^2 \right| \tag{3.81}$$

A small quality factor ($Q < \frac{1}{2}$) will tend to have $\sin(\omega_1 t)$ being hyperbolic sinusoid. As we are focusing on crystal oscillators, we expect greater than half-quality factor. Considering the system after a very few pulses $\omega_o t \gg 1$, it could be simplified to

$$V^2(t) = \frac{2 \cdot k \cdot T \cdot (1+\gamma)}{C} \cdot e^{-Bt} \tag{3.82}$$

Therefore we can extract the linear regime start-up time to reach an oscillation amplitude of "V_1", for instance as given by

$$t \sim \frac{2 \cdot Q}{\omega_o \cdot \left(\frac{G_n}{G_p} - 1\right)} \cdot \ln\left(V_1 \cdot \sqrt{\frac{C}{k \cdot T \cdot (1+\gamma)}}\right) \tag{3.83}$$

where γ is the thermal noise excess factor

$$\gamma = \begin{matrix} \frac{n}{2} & Weakinversionsaturation \\ \frac{2n}{3} & Stronginversionsaturation \end{matrix} \tag{3.84}$$

This estimation is quite pessimistic because the start-up of the oscillator is not only dependent on its own noise. As the inductance is in the milli Henry range, one could argue that the oscillation envelope expansion time is constant if it can be determined by $t \sim 3 \cdot \tau$, where τ is the time constant $\tau = \frac{2}{L_m \cdot |R_m|}$ and the inductor is derived from $L = \frac{1}{C \cdot \omega^2}$.

The term CM7V-T1A has a mechanical time constant close to 300 ms, whereas the DS26 crystal has a mechanical time constant close to 750 ms. This calculation was performed on different crystals on the market, and we observed that, the higher the quality factor, the longer it takes for this expansion to stabilize. It takes a longer period to cancel the oscillation, so it is necessary to accumulate more energy in the first place.

3.4.3.3 Circuit capacitances calculation of pulling and series resonant frequency

The values of C_1 and C_2 essentially control the amount of frequency pulling (p_C) by the circuit. If the frequency pulling is increased, the frequency of oscillation moves away from the intrinsic mechanical resonant frequency of the resonator and becomes more dependent on the sustaining circuit. Conversely, if the frequency pulling is decreased, the critical transconductance to start the oscillation G_{mcrit} is increased, resulting in an increase of power consumption according to Equation 3.61. Knowing C_m, C_1, C_2 and C_3, and the coupling factor K_M, the frequency pulling at the critical condition for oscillation can be calculated by Equation 3.61.

$$p_C = \frac{C_m}{2 \cdot (C_s + C_3)} + \frac{C_m}{2 \cdot (C_s + C_3)} \cdot \left(1 - \sqrt{\frac{1}{K_M^2}}\right) \sim \frac{C_m}{2\,(C_s + C_3)} \tag{3.85}$$

The coupling factor K_M between the circuit and the resonator is recalled in Equation. 3.86 and is due to the presence of the compound parallel capacitance C_3.

$$K_M = \frac{\frac{Q \cdot C_m}{C_3}}{2 \cdot \left(1 + \frac{C_3}{C_s}\right)} \tag{3.86}$$

Knowing the specified frequency of a stable oscillation f_s, which is the exact (series) resonant frequency, the pulled frequency f_p at which the circuit and the resonator oscillate is

$$f_p = f_s \cdot (1 - p_c) \tag{3.87}$$

The impedance locus is shown in Figure 3.36. It reports the evolution of the imaginary part of the oscillator input impedance as a function of its real part, whereas the implicit variable is the transconductance swept from 1 nS to 10 µS.

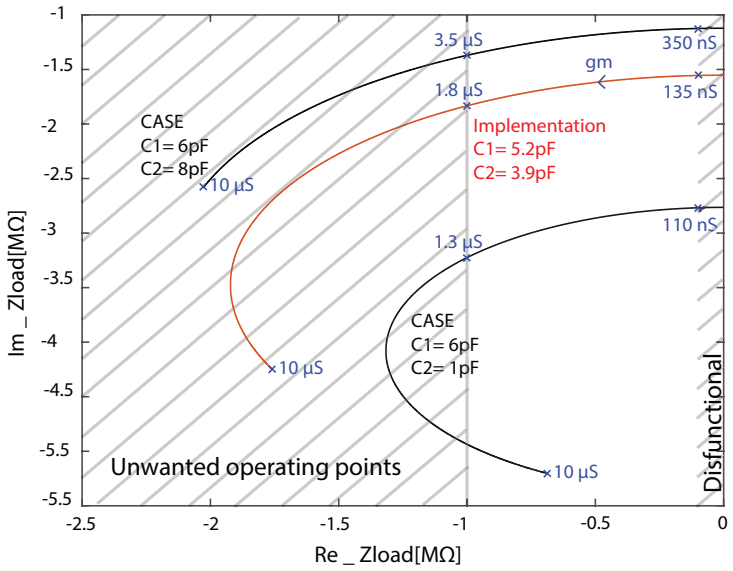


Figure 3.36: Resonator and circuit impedance locus for various load conditions

This impedance locus is proposed for load capacitance values ranging from 1 to 8 pF. The impedance locus shows that the load capacitor could be selected in the range from 3 to 6 pF and by ensuring an M negative resistance while increasing the transconductance. It is taken as a complementary design step in which we optimize pulling in order to reduce the critical transconductance with respect to traditional design methodology.

3.4.3.4 Calculation of the critical transconductance

Figure 3.30 illustrates the position of the critical input impedance and the transconductance for which the oscillation starts, whereas Equation 3.61 provides an analytical method for determining this transconductance. The implementation of transconductance by a CMOS inverter minimizes the necessary current. This structure reuses the same current to achieve two additional transconductances, one with PMOS and the other with NMOS, as presented in [272]. The CMOS inverter will draw a current of a hyperbolic sine wave, which reduces the conduction angle and has more of a Dirac function. By reducing the amplitude, the

inverter has to drive over a wider conduction angle to reach the same peak current. This could be observed in Figure 3.37, where three cases are presented, one of which represents the implanted case oscillating at about $3 \cdot U_T$ within the range from $1 \cdot U_T$ to $5 \cdot U_T$.

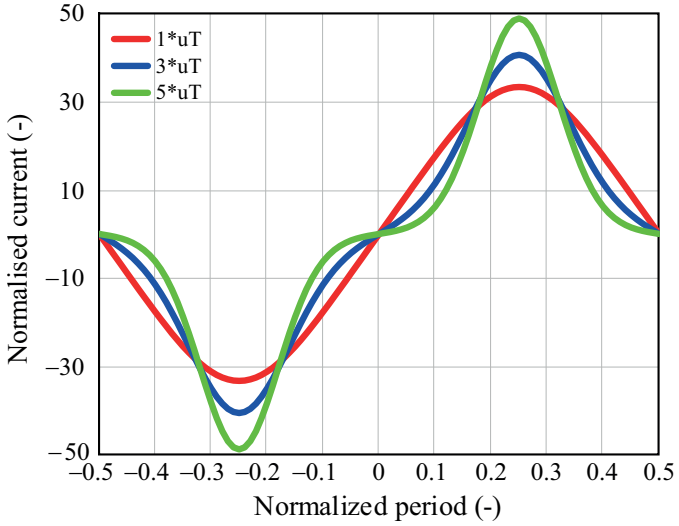


Figure 3.37: Normalized current in a CMOS inverter over a normalized period.

This means that the efficiency of the CMOS inverter will decrease to achieve an efficiency comparable to that of a standard common source amplifier. Thus the advantage presented in Equation. 3.88, would not hold.

$$I_{qcsa} = n \cdot U_T \cdot g_{ms} \neq I_{qCMOSINV} = n \cdot U_T \cdot \frac{g_{ms}}{2}. \tag{3.88}$$

For this reason, structural changes are proposed in Section 3.4.3.5.

3.4.3.5 Proposed structural changes

To benefit from the simplicity of amplitude regulation, the four core transistors MR1, MR2, MB2, and MB3 are kept. Also included was the filter made of Rf, Cf that must be effective at least one decade lower than the oscillation tone. Finally, the resistor RB is also kept to set the start-up current. Additionally, as presented in Figure 3.38, an aspect ratio “A” between transistors MB1 and MR1 is inserted to save current in that control loop. The minimum supply voltage can be reduced as the amplifier current branch is folded from the control part. It enables the use of a CMOS inverter and minimizes the quiescent current as complementary transconductance sums up as presented in [272].

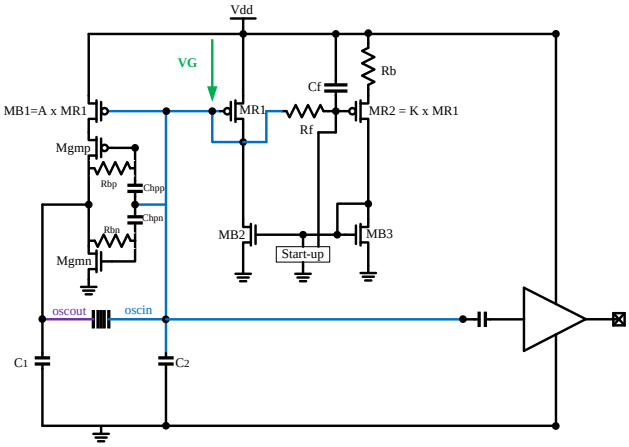


Figure 3.38: Proposed Self-biased, low amplitude regulated CMOS XO.

At low oscillation amplitudes, the CMOS inverter current characteristics shown in Figure 3.37 are flattened. To overcome this, a gate connection of MB1 is proposed, and the subthreshold slope is ideally 60 mV/decade. When the “oscin” signal peak is at its lowest value, it will inject one current decade more than fixed by the operating point and adequately clamp the right amount of charge required to maintain amplitude. The continuous drain current and CMOS current were implemented and can be observed in Figure 3.39. The consumption of this branch is MB1 drain current (red).

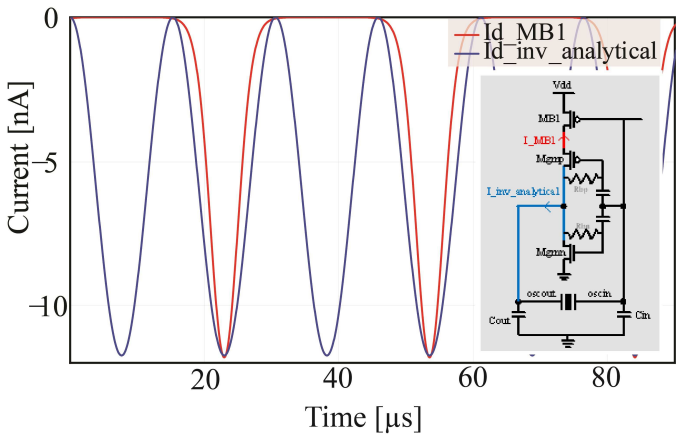


Figure 3.39: Theoretical drain current waveform in MB11 and drive current.

An additional contribution of MB1 to the system is to improve the supply rejection ratio as reported in [272]. The circuit formed by MR1, MR2, MB2, and MB3 is known to be proportional to absolute temperature (PTAT) when MR1 and MR2 are operated at a subthreshold. Therefore, power consumption concerning temperature is expected to be proportional. The generated reference current can be reused to bias the post-amplifier, which will extract the signal from

the “oscin” node, whereby the oscillation amplitude voltage is as low as 80 mV to 1 V. The reason to do so is to avoid harmonic distortion at the output of the CMOS inverter. To extract the low-voltage clock reference efficiently, a class AB amplifier is used. As for single quiescent current, two transconductances will either push or pull the signal. The class-AB amplifier is biased in order to bias the amplifier transistors Mpout and Mnout in the sub-threshold and keep the node at a relatively high impedance node as presented in [233]. The implementation of this class-AB amplifier is proposed in Figure 3.26. It requires one voltage biasing at high impedance so that it would adequately bias the transistors “Mpout” and “Mnout.” Using differential pairs biased in sub-threshold and sized to lower than the transconductance leads to a reasonable output impedance at the node, as proposed in Section Figure 2.50. The voltage shifts Vbn and Vbp are the structural offsets imposed by the transistors aspect ratio of A : B for the PMOS device, and C : D for the NMOS device.

3.4.3.6 Amplitude selection in harmonic oscillator

Generating a clock-signal, i.e. an alternating digital signal with stable and controlled frequency, is generally done in two steps as depicted in Figure 3.40.

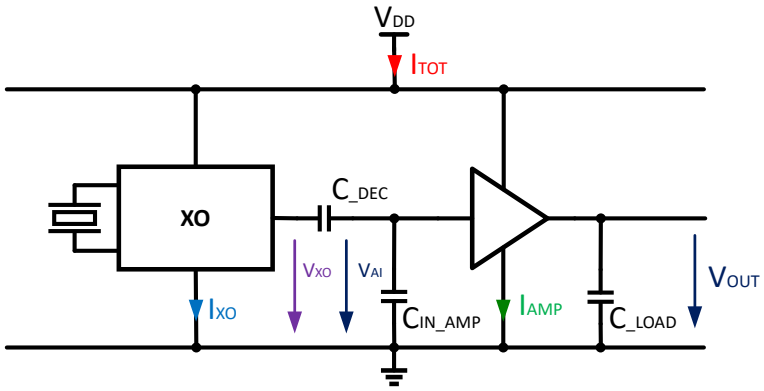


Figure 3.40: Crystal oscillator amplitude trade-off

1. Oscillator function (XO): Generate a first signal that is alternating, has a stable frequency but is rarely compliant with the digital specification of a signal.
2. The coupling between the first harmonic of the crystal oscillator and the amplifier could be highly critical.
3. Clock amplifier function (LS): Amplifying and limiting (“level-shifting”) the first signal make it compliant with the digital specification of a signal.

Both consume current and therefore power. The attempt to minimize power consumed by the former usually comes at the cost of increased the power consumption of the latter. One wants to minimize the overall-consumption under certain conditions. As presented in Figure 3.25, the buffer jitter contribution is expected to dominate. According to Equation 3.90, a too

small oscillation amplitude value (V_{XO}) may result in an unacceptable level of phase noise. However, the energy of oscillation is also proportional to the oscillation amplitude (V_{XO}). Thus, according to noise around the frequency of oscillation, if the oscillation amplitude is too large, the power dissipated in the resonator can exceed the acceptable limit, resulting in excessive aging or even breaking of the resonator:

$$P_m = \frac{\omega}{QE_m} = (1 + \frac{C_3}{C_2})^2 \cdot |V_{XO}|^2 \cdot \frac{\omega^2 C_1^2 R_m}{2}. \tag{3.89}$$

Moreover, a large oscillation amplitude requires a large value of supply voltage to maintain the active transistor in saturation in order to avoid additional losses and a degradation of frequency stability.

$$S_\phi = \frac{(1+\gamma)\, k \cdot T \cdot \omega^2}{2 \cdot Q \cdot P_m \cdot \triangle\omega^2} = \frac{(1+\gamma)\, k \cdot T \cdot \omega^2}{2 \cdot Q \cdot (1 + \frac{C_3}{C_2})^2 \cdot |V_1|^2 \cdot \frac{\omega^2 C_1^2 R_m}{2} \cdot \triangle\omega^2}. \tag{3.90}$$

Maintaining a low amplitude ensures a low transistor complexity oscillation amplitude regulation circuit consisting of four transistors (two PMOS, two NMOS) and one RC first-order filter as presented in [224]. This circuit takes subtle advantage of the subthreshold properties. Figure 3.41 proposes an estimation of the power consumption as a function of the amplitude normalized to thermodynamic voltage (UT). The required stabilized quiescent current is added to sustain a transconductance of 135 nS, corresponding to the loading capacitance to an 80 k motional resistor, which is the worst-case motional resistor for the resonator considered here.

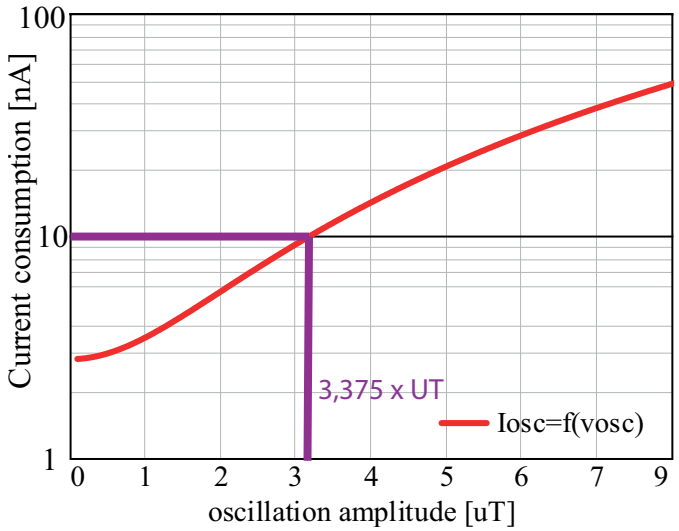


Figure 3.41: Consumption model as a function of oscillation amplitude

With load capacitances of C1=5.2 pF and C2=3.9 pF, respectively, it is reasonable to select an amplitude of 3 thermodynamic voltage (UT) leading to a power consumption below 10 nA, on top of which the 2 nA of the buffer presented in Section 3.3.4 was added, thus an amplitude of 74 mV ensures a total consumption of 10 nA. Verification, measurements and analyses are provided in Section 4.4.

3.5 Leveraging phase noise for robust random number generation

As mentioned in the introduction, high-entropy random number generators (RNGs) are an essential component of information security. They form the foundation for many cryptosystems. Jitter extraction-based techniques became popular, whereas a fully integrated oscillator samples a noisier one. True random number generators (TRNGs) are devices that extract entropy from a physically random phenomenon. They generate random numbers, which are ideally unpredictable. The concept of unpredictability cannot be estimated by using statistical tests. Entropy can only be assessed by modeling the noise source and the extraction mechanism to estimate Shannon's entropy per output bit [281, 282]. These models are mandatory when targeting certifications such as the AIS31 PTG.2 [282]. The NIST SP 800-90B standard is also highly encouraging to provide such a model. Figure 3.42 describes the requirements of the classical approach. Minimum certification in the US and Europe would suggest that one can use a stochastic model to prove the last grade and evaluate online both entropy source and post-processed bit stream, where various canary logics apply.

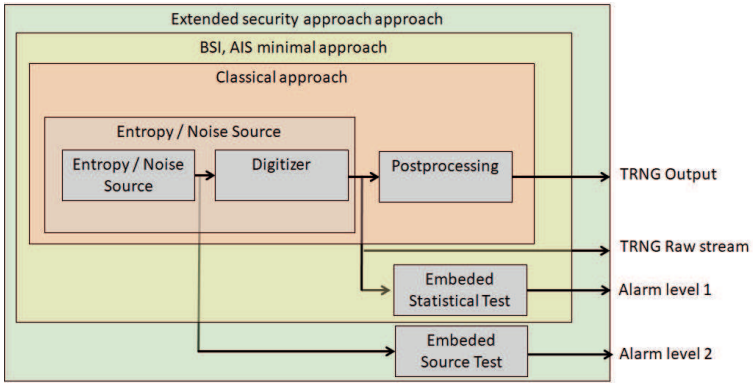


Figure 3.42: Random Number Generator : Design grade and recommandations

Many TRNGs exist, but TRNGs with simple extraction mechanisms with an independent physical entropy source [283, 281, 284, 282] are usually well-suited for certification processes. Others are not scalable [285], or burdensome to model accurately [286, 287]. Self-timed rings (STR) are oscillators in which events (electrical transitions) propagate without colliding, thanks to a handshake request/acknowledgment protocol. They can be used to generate multi-phased signals with a sub-gate delay phase resolution [288, 289]. In classical ring oscillators, the phase resolution is limited by the propagation delay of one stage because only one event propagates in the ring. Conversely, STRs allow phase differences that are fractions of the propagation

delay of one ring stage because several events evolve simultaneously in the ring. The phase resolution ($\Delta\phi$) in the time domain is then expressed as

$$\Delta\phi = \frac{T}{2 \cdot L} \tag{3.91}$$

where L is the stage number and T the STR period. The contribution [290, 291] proposes a random number generator that would lower the gate complexity with respect to [288, 289]. It still consists of STRs and another oscillator. The STRNG architecture is depicted in Figure 3.43.

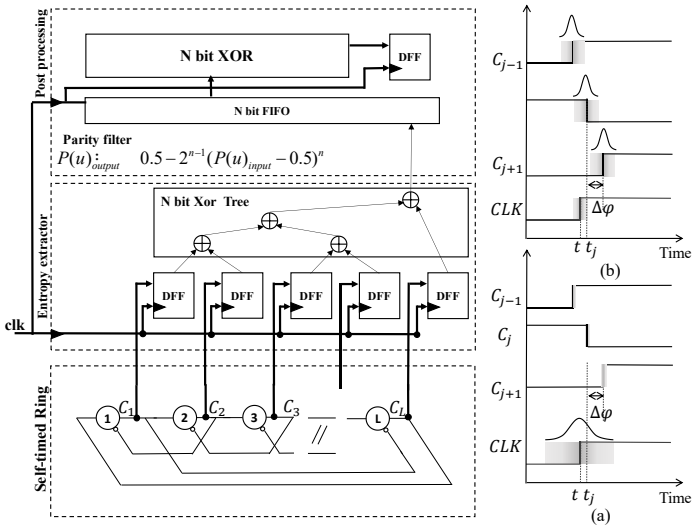


Figure 3.43: STRNG architecture. (a) Proposed sampling clock jitter extraction. (b) Extraction of the phase resolution error

The STR is initialized with N events, where N is a co-prime with L number of stages. In this configuration, it provides L phases corresponding to the signals C_1 to C_L having the same period T, a constant phase difference $\Delta\phi$ and are evenly distributed over half an oscillation period of the STR. These signals are subject to jitter variations that follow a normal distribution with a standard deviation of σ_{STR}. Each signal C_i (with $i \in [1..L]$) is sampled in a flip-flop by a clock. The sampling clock is also a jittered signal having a normal distribution with a standard deviation of σ_{samp}. Whatever the exact sampling instant t, there exists an integer j such that $|t - t_j| \leq \frac{\Delta\phi}{2}$, where t_j is the switching moment of signal C_j. The sampling produces a random bit stream if σ_{STR} is greater than the phase resolution $\Delta\phi$ and/or σ_{samp} is greater than $\Delta\phi$. Increasing σ_{STR} and/or σ_{samp} favors a lower area and lower consumption thanks to a lower stage number L. In this work, we consider that STRs are in an evenly spaced propagation mode, guaranteeing a constant phase difference over the ring. This is done by appropriately selecting the number of events at reset time.

In [14] and [18], a stochastic model is proposed for STRNGs, allowing us to compute a lower

bound for entropy per output bit H_m given in Eq. 3.5, where P_u is the probability to sample a value "u" at 0 or 1 at the TRNG output.

$$H_m = -P_u \cdot \log_2(P_u) - (1 - P_u) \cdot \log_2(1 - P_u)$$

This probability uses the function $\varphi(x) = \frac{1}{\sqrt{2 \cdot \pi}} \int_{-\infty}^{x} e^{-\frac{t^2}{2}} . dt$, $x \in \mathbb{R}$, the cumulative distribution function of which is a Gaussian law.

In [14] and [18] the probability is computed with the jitter magnitude and the STR parameters as follows:

$$P_0 = 1 - 2\varphi\left(-\frac{T_{STR}}{4 \cdot L \cdot \sigma_{STR}}\right) - 2\varphi\left(\frac{T_{STR}}{4 \cdot L \cdot \sigma_{STR}}\right)^2.$$

Conversely, no hypothesis on the STR jitter is required when the entropy lower bound is only computed with the sampling jitter as follows:

$$P_0 = \varphi\left(-\frac{T_{STR}}{4 \cdot L \cdot \sigma_{samp}}\right) \cdot \left(1 - \varphi\left(\frac{T_{STR}}{4 \cdot L \cdot \sigma_{samp}}\right)\right)$$

Both models can be used independently because the STR jitter and the sampling clock jitter are uncorrelated, but both contribute to the extracted entropy. Both Shannon's lower bounds of entropy per output bit H_m are represented in Figure 3.44, which confirms the relevance of such an approach even with only a few stages, making possible a TRNG with a low gate count. Note that this model yields a lower bound that does not reach the maximal entropy ($H_m = 1$) in this case. Thanks to these models, it is possible to quickly estimate the minimum entropy that can be extracted by the TRNG. Lowering the supply voltage, especially with subthreshold voltages, increases the sampling clock and STR jitters, allowing TRNG implementation with a few stages. Moreover, the subthreshold approach drastically reduces the power consumption per output bit.

Finally, if required, the entropy can be enhanced with a parity filter as depicted in Figure 3.43. This was combined with the sampling mechanism to mitigate the bias of the random number. This parity filter compresses the bit stream and therefore reduces the data rate. By setting the entropy lower bound close to 1, the TRNG bit stream can be considered unpredictable.

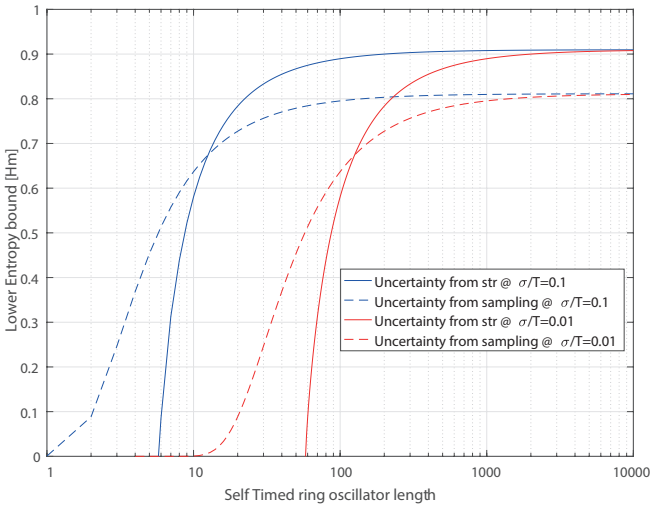


Figure 3.44: Shannon lower entropy bound according to the length of the STRO.

Case Studies

The circuits principles, relies on the use of self-biased circuits with an astute use of the inversion level properties as well as merge transistors that could be reused to ensure more than one functions. The chapter is divided in Subsection. The first Sub-section 4.1 propose a review of Self-biased current-reference using strong inversion and linear region transistor operation for reducing the size of nA level current references, reaching the nA references comes with the issue of handling non dynamic start-up due to their potential failure in large scale production but yes manage to avoid any overhead in operation. As a result we had proposed a higher order compensated nA level current reference including a non dynamic start-up without a quiescent current consumption. The second Sub-section 4.2 discuss a fully integrated timer circuit presented in [269, 270]. The third sub-section 4.3 propose a random number generator which was exposed in [290] and .The forth sub-section 4.4 on which it is presented an ultra-low power crystal oscillator as shown in [292, 293]. The fifth sub-section 4.5 which had targeted a fast locking time, we had reused the timer architecture for the voltage controlled oscillator and our low power crystal oscillator. The last sub-section differ as the fist from timing circuit toward a more power-management discussing on thermoelectric energy-harvesting circuit and particularly it's cold-start function 4.6, the particularity of thermoelectric energy-harvesting is that although the available power density is important it requires an important conditioning as the voltage starts from very few milli-volts. The challenge of power conversion without any external power than the thermoelectrogenerator is then pushed back from the power converter circuits to the switching frequency generation part, which we had contributed to propose a structure that take advantage of process and low power ring-oscillator.

4.1 Self-biased current-reference

One of the direct application of the methodology presented in the sub-section 3.2.1. The case study apply to a current reference where the objective was set to a current of 1nA. We had implemented the reference circuit of [224], where one of the dipole is a resistor, as discussed earlier this resistor tends to be large for low current, thus we had also studied two other topology proposed in the literature [294, 295, 296], where the resistor is implemented as a mosfet in strong-inversion and linear region. The resistor case study is discussed in

sub-section 4.1.3, it confront our analytical method, simulation, and silicon validation. The implementation presented in the paper of Oguey [294], was part of our case study is discussed in sub-section 4.1.3. The implementation presented in the paper of Galenao [296], was also subject to our case study, and it is discussed in sub-section 4.1.4, it confront our analytical approach, with simulation, and silicon validation. We finally brought up another method based on the discussion of sub-section 2.3.2.1, by using a native device it is naturally in strong inversion and one could find a structure that ensure saturation. The circuits were all realized in a 180nm CMOS flash process, the die picture is proposed in Figure 4.1. For ultra low power applications, one would like to reduce the bias current to nA range. The topology presented in [224], would require a value for the resistance R in the range of 100M - 1G Ohm, leading to a huge area of silicon, as well as being very dependent of PVT (+/- 25% variation for polysilicon resistors). Reviewing the MOSFET used in linear region enable an highly integrated circuit that only consists of MOS transistors, which this test die illustrated.

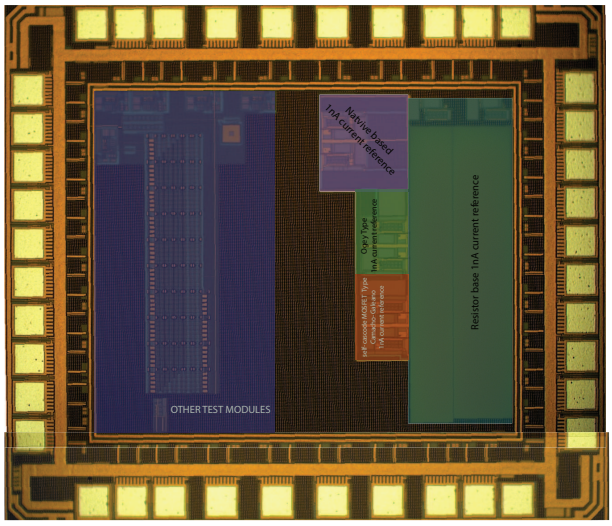


Figure 4.1: Die Picture of the realized current references in 180nm CMOS flash process

Two current mirror ratio were integrated for the source coupled comparative the transistor imbalance of the aspect ratio between transistors M_4 and M_5 in Figure 4.3, was set to 10, and 21 leading to a reference voltage of 59.87 mV, and 79.16 mV respectively. We applied the guidelines (flow) presented in Figure 4.2 for sizing the whole structure.

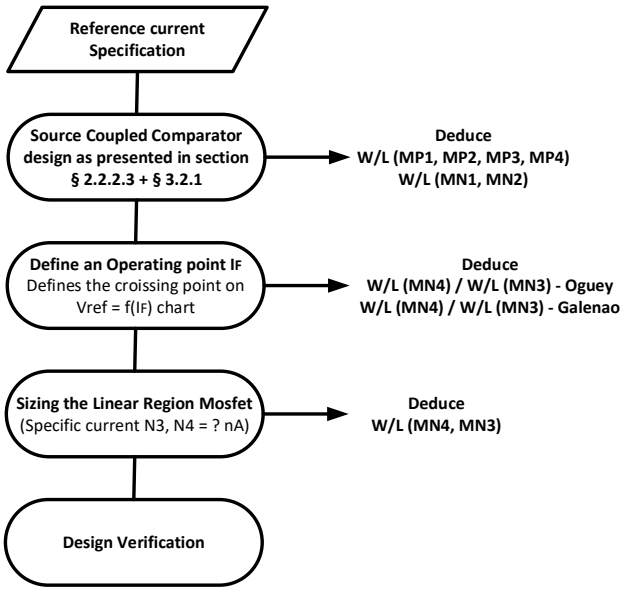


Figure 4.2: Procedural design guidelines for current reference

The first specification of current reference impose a part on the design point. Then it was applied the source coupled current mirror design procedure and finally we size the linear region mosfets by imposing an operating point and sizing accordingly as shown in sub-section 4.1.3 and in sub-section 4.1.4.

4.1.1 A Start-up Circuitry without a quiescent current.

As reviewed in sub-section 3.2, the operating point where current and voltage are null could be a stable solution. Therefore there is the need to have start-up circuits which ensure the start-up and then the proper function of the circuit. It is commonly proposed techniques called dynamic and static start-up circuits. One of the key issue with dynamic start-up is that they might not be able to detect a dysfunctional state and therefore keep the circuit stuck where current and voltage are null. In this perspective we have proposed a rather simple circuit that ensure the start-up as proposed in Figure 4.3.

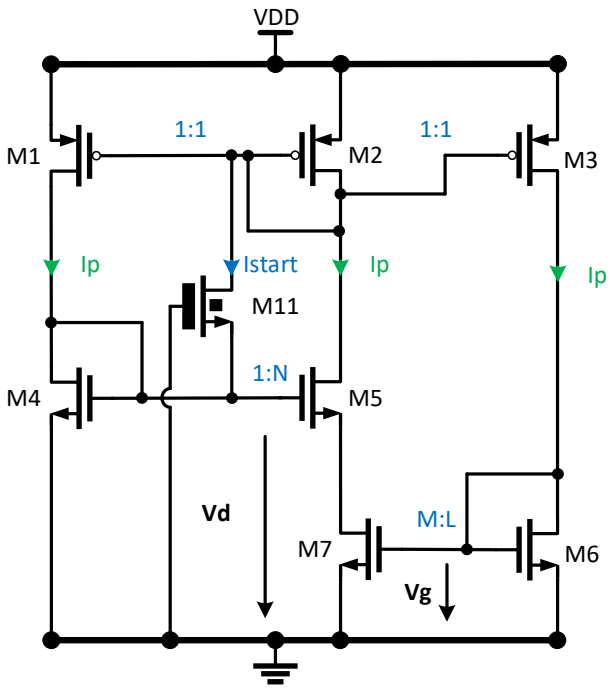


Figure 4.3: Proposed single transistor start-up circuitry without a quiescent current

The circuit takes advantage of a "Zero-Vt" or "Native" mosfet M_{11}, which as the name tells have the property to have it's threshold voltage close to zero, this mean the device is in strong inversion even with a gate source voltage at zero. We had connected the source to the gate of transistors M_4 and M_5 which operate in sub-theshold when the reference find it's operating point. Thus we can assume a voltage in the range of $V_{G_{M5,M4}} \in [0.2-0.4]V$, which makes a negative gate to source voltage and thus make the transistor blocked. A potential issue with this is that the short-cut between the two gate voltage could lead into some long time constant to recover a stable state. The Figure 4.4, propose a potential improvement in which the transistor M_{11} is now sensing the reference quantity in the same way and in Figure 4.3, where the leakage would stop for the same reason.

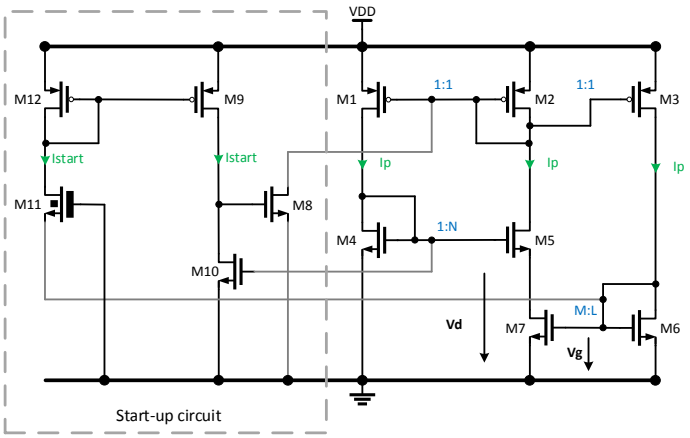


Figure 4.4: Proposed dual level transistor start-up circuitry without a quiescent current

On the top of that, The leakage generated impose a start-up current onto the drain of M_9, and M_{10} that generate a voltage to the gate of transistor M_8 leading to draw current from the gate of transistor M_1, the gate of transistor M_4 and M_7 shall converge to a stable operating point. As a consequence M_{10} starts to conduct and the gate voltage of transistor M_8 drop down to ground level which open the start-up loop. While the negative gate source voltage of M_{11} impose a negligible leakage current to the circuit. This leakage quantified in 2 digit pA number over the temperature range. Both principle were used in circuits and will not be represented.

4.1.2 The Resistive Proportional To Absolute Temperature (PTAT) current reference

A reference circuit of [224], we have applied the methodology exposed in sub-section 3.7, in order to size the core transistors namely M_{P1}, M_{P2}, M_{P3}, M_{P4}, M_{N1}, and M_{N2}. These form a source coupled comparator. As we had Zero Threshold, transistors available we had self cascoded the source coupled comparator with transistors M_{NAT1}, and M_{NAT2}. The transistors M_{N1}, and M_{N2} are fixed size enclosed gate layout transistors.

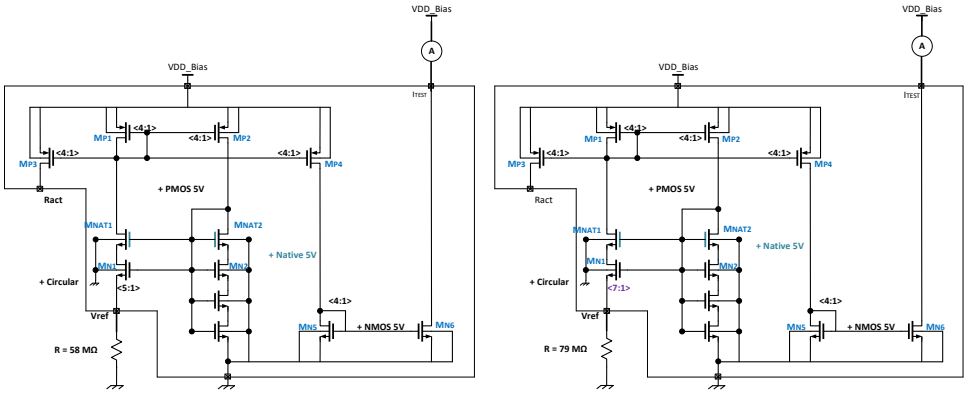


Figure 4.5: Standard current reference schematic and sizing

The choice to use these devices was guided by the results presented in Section 2.2.2.3 on variability of gate voltage mismatch at weak inversion level. The Figure 4.5 shows the schematic.

4.1.3 The strong inversion and linear "Oguey" current reference

The circuit proposed in [294], proposed among the first all-MOS circuit technique for very-low-voltage proportional-to-absolute temperature (PTAT) current references. It kept named as its author The Oguey current reference in the literature. The circuit is shown in Figure 4.6.

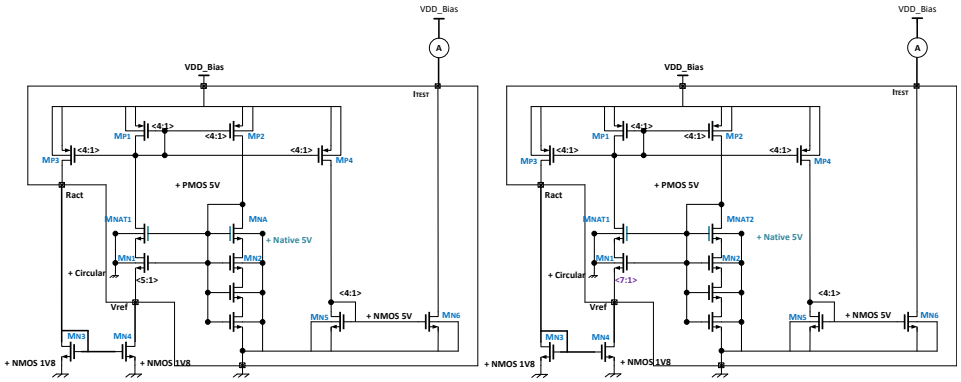


Figure 4.6: "Oguey" current reference schematic and sizing

This topology is based on the source-coupled comparator structure which has been detailed in in the sub-section 3.2.14Instead of using a resistor at the source of the transistor connected to V_{ref}, is a SAMOSET in linear region instead of a resistor, namely M_{N4}. It is paired in current mirror structure with bias transistor M_{N3}. Another branch is hence required, and PMOS transistor M_{P3}, which distributes a current in that branch equal to the one flowing in each of the source-coupled comparator branches. This current I_{ref} can then be used to bias another circuit. It is generated at the drain of M_{P4}. The following table 4.1 summarize the above assertion .

Table 4.1: Target operating points for the Oguey structure

Transistor	Regime	Remark
M_{N1}, M_{N2}	Weak inversion / Saturation	$N_0 = \frac{\frac{W_{M_{N2}}}{L_{M_{N2}}}}{\frac{W_{M_{N1}}}{L_{M_{N1}}}}$
M_{P1}, M_{P2}, M_{P3}, M_{P4}	Strong inversion / Saturation	-
M_{N3}	Strong inversion / Saturation	$A_0 = \frac{\frac{W_{M_{N4}}}{L_{M_{N4}}}}{\frac{W_{M_{N3}}}{L_{M_{N3}}}}$
M_{N4}	Strong inversion / Linear-region	-

It is paired in current mirror structure with bias transistor M_{N3} a which . Another branch is hence required, and PMOS transistor M_{P3}, distributes a current in that branch equal to the one flowing in each of source-coupled comparator branches. This current I_{REF}, can then be used to bias another circuit. It is generated at the drain of M_{P4}. The next part of this sub-section will be to determine the relation $V_{ref} = f(I_F)$.

I_F represent the inversion coefficient of transistor M_{N4}. It is by definition equal It is by definition equal to $I_f = \max(i_{f4}; i_{r4})$. i_{f4}, and i_{r4} are defined as forward and reverse normalized current of transistor M_{N4}. The reference current can be defined as per Equation 4.1.

$$I_{ref} = I_{SPECN_{\blacksquare}} \cdot \frac{W_{M_{N4}}}{L_{M_{N4}}} \cdot (i_{f4} - i_{r4}) \tag{4.1}$$

The specific current of transistor M_{N4} is $I_{SPECN_{\blacksquare}} \cdot \frac{W_{M_{N4}}}{L_{M_{N4}}}$, as defined in section 2.1, it is first expressed in Equation the pinch-off Voltage for the transistor M_{N4} in Equation 4.2, and then it is derived the drain source voltage of transistor M_{N1} in Equation 4.3.

$$\frac{V_{PM3,M_4}}{u_T} = 2 \cdot q(i_{f4}) + \ln(q(i_{f4})) \tag{4.2}$$

$$\frac{V_{ref}}{u_T} = 2 \cdot q(i_{f4}) + \ln(q(i_{f4})) - 2 \cdot q(i_{r4}) + \ln(q(i_{r4})) \tag{4.3}$$

As ekv function is continuous, and strictly increasing with $i_{f,r}$, and this inversion level is a real and positive number. Thus the function is bijective. A Bijective function finds a particularly interesting property for a given i_{fx} and a given i_{fy}, if their respective pinch-off voltage are equal $2 \cdot q(i_{fx}) + \ln(q(i_{fx})) = 2 \cdot q(i_{fy}) + \ln(q(i_{fy}))$, then their inversion level as well $i_{fx} = i_{fy}$. The inversion level is set to be equal on both transistor M4, M3 imposing : $2 \cdot q(i_{fM4}) + \ln(q(i_{fM4})) = 2 \cdot q(i_{fM3}) + \ln(q(i_{fM3}))$. Hence, we can deduce the reference current as per

Equation 4.4.

$$i_{fM3} = i_{fM4} = \frac{I_{ref}}{I_{spec_{M3}}} = i_{fM4} - \frac{I_{ref}}{I_{spec_{M4}}} \tag{4.4}$$

The reverse current is expected to be smaller than the forward current $i_{r4} < i_{f4}$. As shown in Equation $I_C = \max(i_{f4}; i_{r4})$ It is deduced that the inversion level is set by the forward current as per Equation 4.5.

$$I_F = i_{f4} \tag{4.5}$$

We had expressed accordingly the reverse current as per Equation 4.6.

$$i_{r4} = I_F \cdot (1 - \frac{I_{SPECM3}}{I_{SPECM4}}) \tag{4.6}$$

The Figure 4.7, propose an the of $V_{ref} = f(I_F)$ for Transistor M_{N4}.

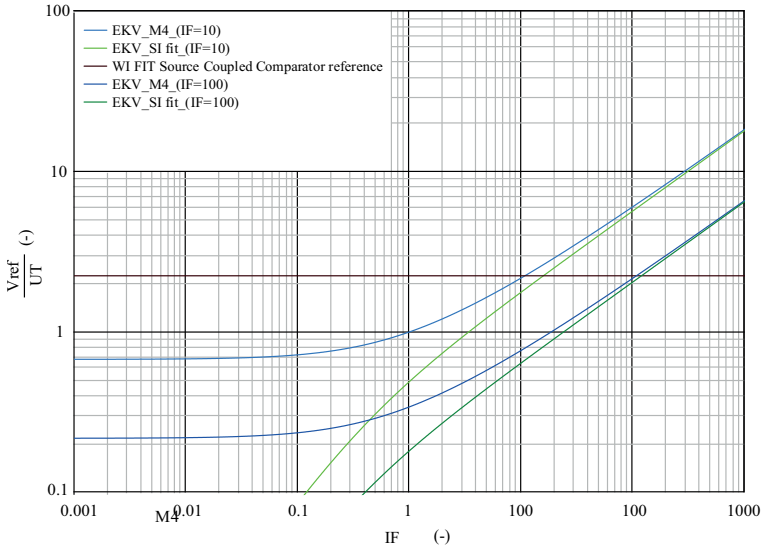


Figure 4.7: $V_{ref} = f(I_F)$ for TransistorM_{N4} in Oguey's structure

The Figure 4.7, is plotted for the case $N_0 = \frac{\frac{W_{M_{N2}}}{L_{M_{N2}}}}{\frac{W_{M_{N1}}}{L_{M_{N1}}}} = 10$, which set $V_{ref} \sim 2.3 \cdot 3u_T$. which appears as a black line. The blue lines correspond to the voltage imposed by the current mirror formed by M_{N3}, and M_{N4}. The green ones while assuming purely strong inversion component. The intersection determines the operating point of the circuit. The choice for the corresponding

IC can be arbitrary chosen by changing $A_0 = \frac{\frac{W_{M_{N4}}}{L_{M_{N4}}}}{\frac{W_{M_{N3}}}{L_{M_{N3}}}}$ of the transistors M_{N3}, and M_{N4}. For this topology, a value of 10 has been chosen. It's actually a trade-off, as it has to be high enough to put N4 in mid - strong inversion, and yet keep a decent sizing. Of course IC = 100 would have been preferable, but it would have required an aspect ratio of the transistor M_{N4} such that $\frac{W_{M_{N4}}}{L_{M_{N4}}} = \frac{1}{50000}$ for 1nA reference current, which is not reasonable. One could notice from the Figure 4.7, that the strong inversion model would apply for the large inversion coefficient it is thus in these corner case it worth considering EKV model for such design procedure. At this point, it is now possible to determine the sizing of the different transistors of the Oguey topology are given in Table 4.2. As a comparison to the proposed schematic in Figure 4.6, the

Table 4.2: Calculated sizing from denormalized operating points for the Oguey topology

Transistor	Sizing (W/L), N0 = 10	Sizing (W/L), N0 = 21	Target IC
M_{P1}, M_{P2}, M_{P3}, M_{P4}	(2.4u /24u)	(2.4u /24u)	10
M_{N1}	(9.4u /2u)	(9.4u /2u)	0.1
M_{N2}	10*(9.4u /2u)	21*(9.4u /2u)	0.01
M_{N3}	(500n/2480u)	(500n/2205u)	10
M_{N4}	(500n/1240u)	(500n/1365u)	10

transistor M_{N1}, M_{N2} are in fact not sized according to the above calculation, it was selected a circular transistor device designed on purpose for the 1nA current reference with improved electrical parameters such as threshold voltage, mobility and their variability aspects due to the observed phenomenon in Section 2.2.2.3.

4.1.4 The self-cascode transistor

The circuit proposed in [295, 296], proposed a new all-MOS circuit technique for very-low-voltage proportional-to-absolute temperature (PTAT) current references. It allows both strong supply scaling by the use of MOS sub-threshold techniques and area scaling through an all-MOS implementation. It could be noticed that this one also propose to replace the resistor of [224], by a linear operation MOS transistor.

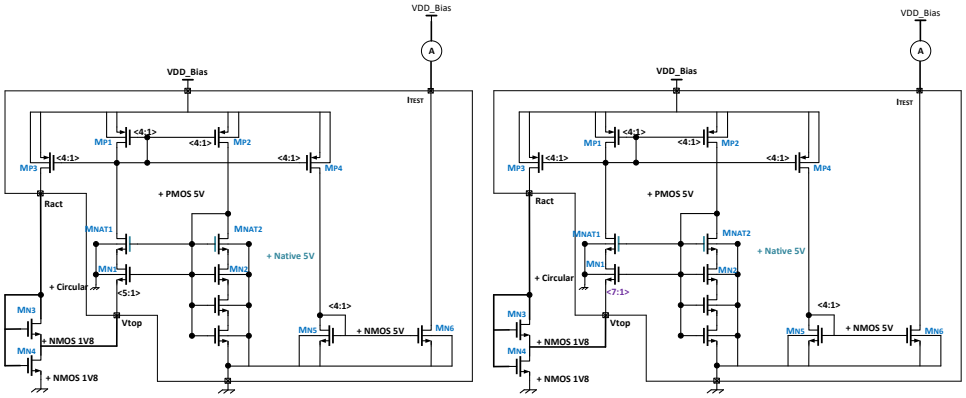


Figure 4.8: Self-Cascode current reference schematic and sizing

Instead of using a resistor at the source of M_{N1}, a MOSFET in linear region is used, namely M_{N4}. It is paired in a self-cascode structure with bias transistor M_{N3}. Another branch is hence required, and PMOS transistor M_{P3} distributes a current in that branch equal to the one flowing in each of branches of the source coupled comparator. This current I_{ref} can then be used to bias another circuit. It is generated at the drain of M_{P4} . One can notice here, that the current going through the transistor in linear region is equal to $2 \cdot I_{ref}$. The Table propose a summary of the Target operating conditions of the self-cascode structure 4.3. The next part of

Table 4.3: Operating points of the self-cascode structure

Transistor	Regime	Remark
M_{N2}, M_{N1}	Weak inversion / Saturation	$N_0 = \frac{\frac{W_{M_{N2}}}{L_{M_{N2}}}}{\frac{W_{M_{N1}}}{L_{M_{N1}}}}$
M_{P1}, M_{P2}, M_{P3}, M_{P4}	Strong inversion / Saturation	-
M_{N3}	Weak inversion / Saturation	$A_0 = \frac{\frac{W_{M_{N3}}}{L_{M_{N3}}}}{\frac{W_{M_{N4}}}{L_{M_{N4}}}}$
M_{N4}	Weak inversion / Linear region	-

aim at the determination of the inversion coefficient of transistor M_{N4}. It is by definition equal to $I_{F_{M_{N4}}} = \max(i_{f4}; i_{r4})$. The variable i_{f4}, and i_{r4} are defined as the normalized reverse and forward inversion current in EKV formalism. The whole reasoning proposed in the sub-section 4.1.3 apply and in this case the reverse current of transistor M_{N4} is given as per Equation 4.7

$$i_{rM4} = 1 - \left[\frac{I_{sM3}(1+N1)}{I_{s_{M3}} + N1 \cdot (I_{s_{M3}} + I_{s_{M4}})} \right] \tag{4.7}$$

$N1$ is defined as $\frac{\frac{W_{M3}}{L_{M3}}}{\frac{W_{M1}}{L_{M1}}} =$, we imposed $N1 = 1$ for this case study. From now on, we have as $\frac{W_{M3}}{L_{M3}} = \frac{W_{M1}}{L_{M1}}$ in the determination of the operating point $V_{ref} = f(I_F)$ as presented in Figure 4.9,

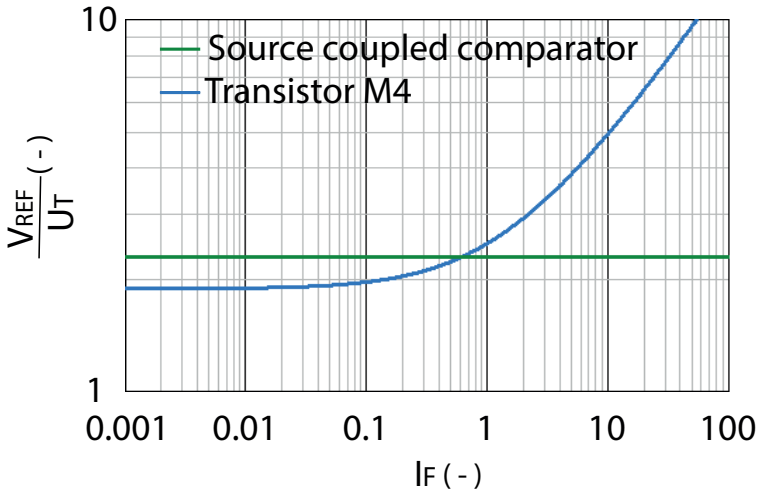


Figure 4.9: $V_{ref} = f(I_F)$ for Transistor M_{N4} in Self-cascode structure

I_F represent the inversion coefficient of transistor M_{N4}. The crossing point between the source coupled comparator reference voltage reference and transistor by choosing a ratio $A_0 = \frac{\frac{W_{M_{N3}}}{L_{M_{N3}}}}{\frac{W_{M_{N4}}}{L_{M_{N4}}}}$. The value of the reference current is set by choosing a specific value for specific current of either N3 or N4. At this point, it is now possible to determine the sizing of the different transistors of the self-cascode transistor topology given in Table 4.4. As a comparison to the

Table 4.4: Calculated sizing from denormalized operating points for the self-cascode transistor topology

Transistor	Sizing (W/L), N0 = 10	Sizing (W/L), N0 = 21	Target IC
M_{P1}, M_{P2}, M_{P3}, M_{P4}	(2.4u /24u)	(2.4u /24u)	10
M_{N1}	(9.4u /2u)	(9.4u /2u)	0.1
M_{N2}	10*(9.4u /2u)	21*(9.4u /2u)	0.01
M_{N3}	(500n/24.3u)	(500n/13.1u)	10
M_{N4}	(500n/72.9u)	(500n/78.6u)	10

proposed schematic in Figure 4.6, the transistor M_{N1}, M_{N2} are in fact not sized according to the above calculation, it was selected a circular transistor device designed on purpose for the 1nA current reference with improved electrical parameters such as threshold voltage, mobility and their variability aspects due to the observed phenomenon in Section 2.2.2.3. The self-biased source coupled comparator sizing remains the same as Oguey's topology, and it can be noticed the length of transistors M_{N3} and M_{N4}, used to create the MOSFET in linear region, are way shorter than in the Oguey's topology, which improves the total area

4.1.5 Proposed current reference

We proposed the circuit shown in Figure 4.10.

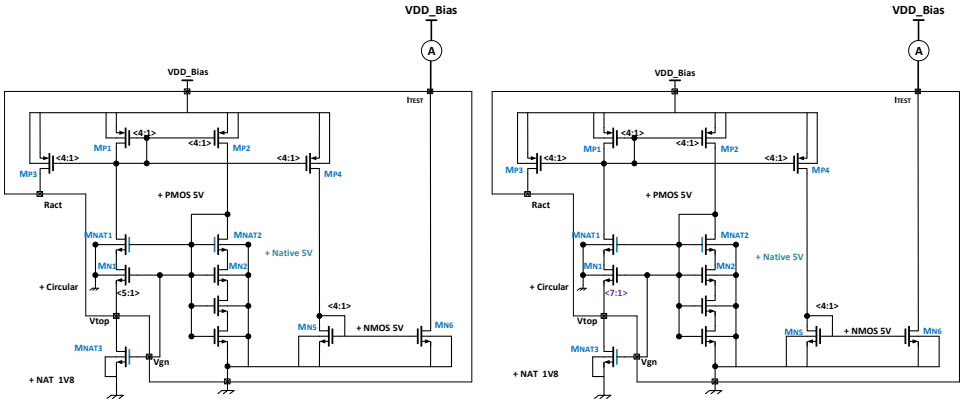


Figure 4.10: Proposed 1nA current Reference using Native conductance operated in strong inversion and conduction

The simplicity of [224], was kept and the strong inversion and conduction mode operation MOS transistor had simply benefit of the advantage of existing Zero-Threshold, also called Native transistor, which by nature of the self biased source coupled comparator would find a stable reference voltage to apply on the conductance. This high resistor technique was presented in the subsection 2.3.2.1. It is preferred to operate in week inversion so that the transistor M7 is by construction in conduction mode ($V_D < V_{Dsat}$) meaning the reverse current is not null. Thus the drain current express as $I_D = I_{Spec} \cdot (I_F - I_R)$. Considering that the text-book strong inversion approximation of the normalized channel voltage as per Equation 4.8.

$$V_p - V_{s,d} = 2 \cdot \sqrt{i_{f,r}} \tag{4.8}$$

The denormalized drain current is given of transistor M_{NAT3}, is obtained Equation 4.9.

$$I_D = \frac{I_{Spec}}{u_T^2} \cdot \left[V_p - \left(\frac{V_d + V_s}{2} \right) \right] \cdot V_{ds} \tag{4.9}$$

The approximation of the pinch-off voltage is given by Equation 4.10.

$$V_p = \frac{V_g - V_T}{n} = 2 \cdot u_T \cdot \ln\left(e^{\sqrt{I_F}-1} \right) \tag{4.10}$$

The V-I characteristic of device M_{NAT3}, could formally be expressed as Equation 4.11.

$$g_{ds} = \frac{I_D}{V_{ds}} = \frac{2 \cdot \beta_{\blacksquare} \cdot \frac{W_{M_{NAT3,}}}{L_{M_{NAT3,}}}}{1} \cdot \left[\left(V_g - V_T \right) - n \cdot \left(\frac{V_d + V_s}{2} \right) \right] \tag{4.11}$$

Which was fitted as Equation 4.12, to touch-up the fitting with respect to the EKV model.

$$g_{ds} = \frac{2 \cdot \beta_{\blacksquare} \cdot \frac{W_{M_{NAT3,}}}{L_{M_{NAT3,}}}}{1.06} \cdot \left[\left(V_g - V_T \right) - n \cdot \left(\frac{V_d + V_s}{2} \right) \right] \tag{4.12}$$

Finally it is important to note that in the case where the designer would like to use this source it is de-facto a fraction of the specific current which is taken as reference. The Figure 4.11 propose a sense of the error involved and the improved fitting.

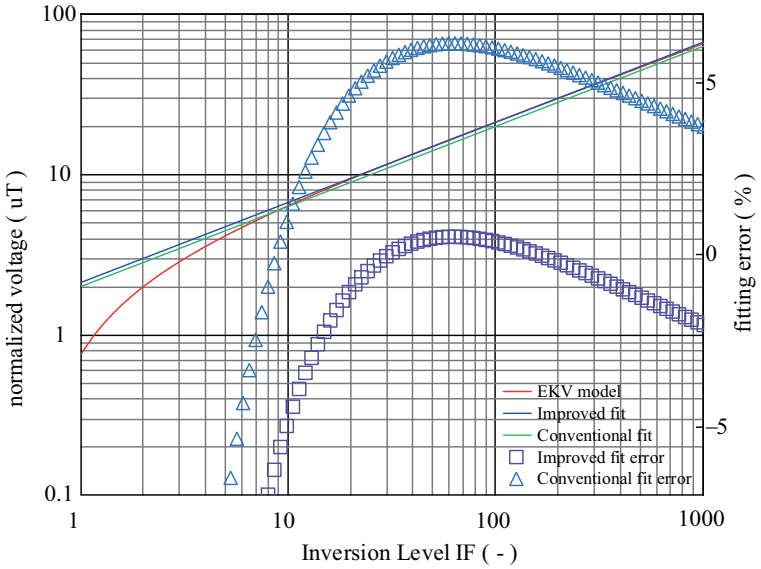


Figure 4.11: Improved strong-inversion and conduction region fitting with respect to EKV complete model

It is then taken some assumption for the study of the structure temperature behavior. The threshold voltage vary with the coefficient a : $V_T = V_{TT0} + a \cdot T$, while the mobility vary with the coefficient b : $\beta = \beta_{T0} + b \cdot T$, the gate voltage with the coefficient d : $V_G = V_{G_{T0}} + d \cdot T$, finally the drain voltage with the coefficient e :$V_D = V_{D_{T0}} + e \cdot T$. The relative variation of the conductance with respect to the temperature express as per Equation 4.13

$$\frac{\frac{\partial g_{ds}}{\partial T}}{g_{ds}} = \frac{1}{T} \cdot \left[\frac{b}{\beta} + \frac{a - d + \frac{n \cdot e}{2}}{V_{T_{T0}} - V_{g_{T0}}} \right] \tag{4.13}$$

It's interesting to note that regular Mobility and Threshold compensation is in the place. Usually this Zero Temp coefficient is not so easy and so well defined technologically. In our case we introduce also d temp coefficient of gate voltage and e temp coefficient of the drain voltage as parameters which could compensate each others.

The gate voltage of transistors M_{N1}, and transistor M_{N2} vary to absolute temperature. This enable a second order temperature compensation the results are discussed in sub-section 4.1.6.

4.1.6 Self-biased current references results and discussion

The Figure 4.12 shows the measurement and simulation of the exposed structure originally using a resistor of [224], as well as the all transistor implementation detailed in the sub-section 4.1.3, and in sub-section 4.1.4.

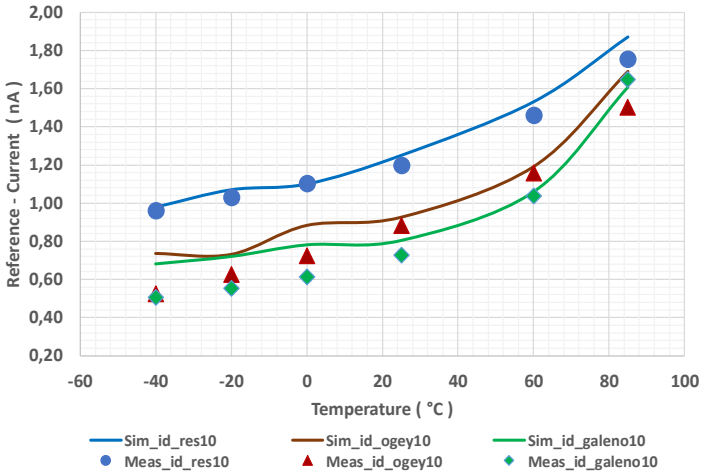


Figure 4.12: Standard, Oguey, and self-cascode current references, correlation of measurement result with simulation results.

The measurement point are the average of 20 measured typical dies packaged in ceramic package. The behavior over temperature is shown at 1.2V supply voltage but is not highly impacted at both 0.8V and 1.6V. For practical reasons a fine trimming was not implemented, the reference were measure for the typical corner trimming code. it could be observed that our design guideline for the current reference at 25°C are 20% accurate which is reasonable considering the component deviation and no fine trimming available. The relative variation over the temperature range of [-40°C ; 85°C], is [-25% ; +100%]. Moving to the proposed all transistors current reference using the output conductance of a native transistor as proposed in sub-section 4.1.5. The Figure 4.13 present its measurement results as well as a correlation with simulation results. One could observe a good match with the proposed design guidelines.

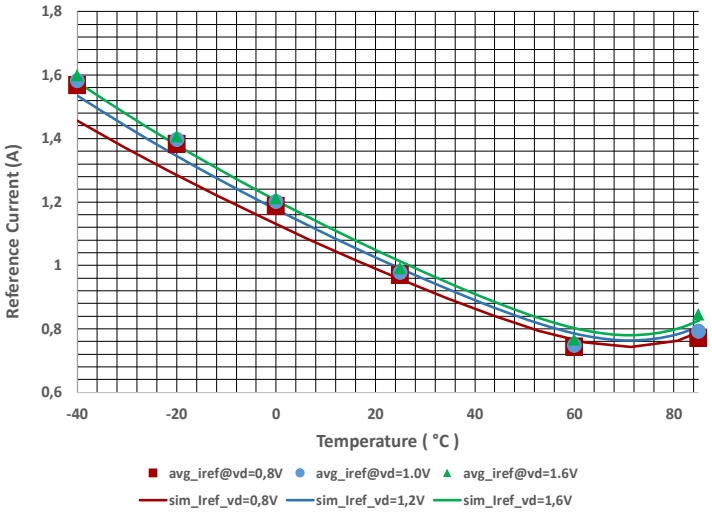


Figure 4.13: Proposed current reference, correlation of measurement result with simulation results.

The behavior over temperature is shown at three supply voltage (0.8V, 1.2V, and 1.6V). A fine trimming was implemented, the trimming code is in that case about half the dynamic of the trimmer (8/15). One could observe that the target current at 25°C is perfectly matched with the structured design approach. The relative variation over the temperature range of [-40°C ; 85°C], is [+60% ; -20%], the temperature compensation mechanism is effective, even though precise measure were not taken to drive the gate to further reduce the temperature dependency.

4.2 A Fully integrated Frequency Reference

As discussed in section 1.1, power consumption is a critical element in the design of microcontrollers, compact wireless systems, and time keeping applications. Implementation of sleep or even deep sleep modes in such applications is enabled by duty-cycling and keeping track of the time. This standby mode is a key concern for the internet of things. Hence, it is vital to maintain accuracy while at the same time reducing power consumption to ensure proper time keeping or reference clock. For accurate time keeping, crystal oscillators are the conventional choice due to their excellent temperature and frequency stability. However, they require an external element which drives up the system footprint and cost. Based on the methodology presented in section 3.2, it is proposed in the Figure 3.22, a schematic of the proposed topology. It was kept the formalism of an RC oscillator even though recently some studies had proposed to approach the problem as a resistor locked loop [123, 124, 127, 125, 128, 129, 130]. The formalism of Frequency Locked Loops makes it possible to introduce advanced control system law and devices property to cope with the temperature and supply sensitivity. Even though the proposed approach in [126, 270] remain rather simple and robust due to self-biasing and first order passive temperature compensation techniques. An accurate knowledge of the physics behind a performance is often the correct way to achieve the expected performance through a

system level approach. The proposed nA range oscillator is implemented in 180nm CMOS Flash process is shown in Figure 4.14.

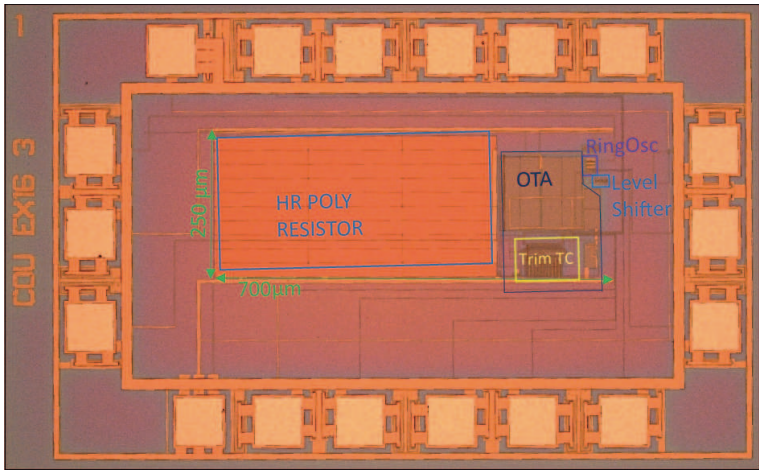


Figure 4.14: Die Picture of the realized current references in 180nm CMOS flash process

The surface of the block is 0.175 mm^2, which is comparable or lower than other published result, in order to get rid of the technology node we had normalized the area results to the minimal square gate length feature in the given process. Since one can realize resistor, capacitor and transistor out of polysilicon this normalization makes relatively sense as their density scale as well. The Figure 4.15 represent the normalized area comparisons of the fully integrated frequency generator as a function of their Frequency.

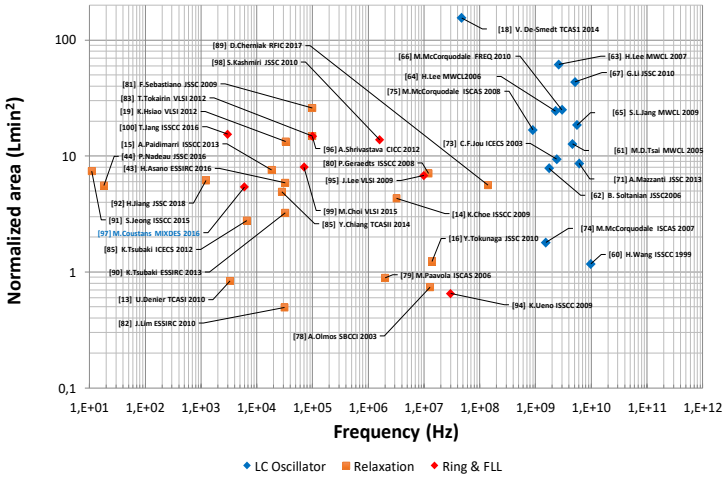


Figure 4.15: Normalized oscillator area with respect to the output Frequency

The main contributor to the area is in our case is the polysilicon resistor with its 400 $M\Omega$, this case study describe the basic results one can obtain. Several tricks on the resistor implementa-

tion can be applied with respect to the publication [126, 270].

4.2.1 Fully integrated Frequency Reference Measurements

This section provides the silicon measurement of 20 typical samples packaged in ceramic.

4.2.1.1 Power consumption temperature and supply voltage sensitivity

The figure 4.16, propose a measurement of the integrated reference current consumption over the temperature from [-40°C - 85°C].

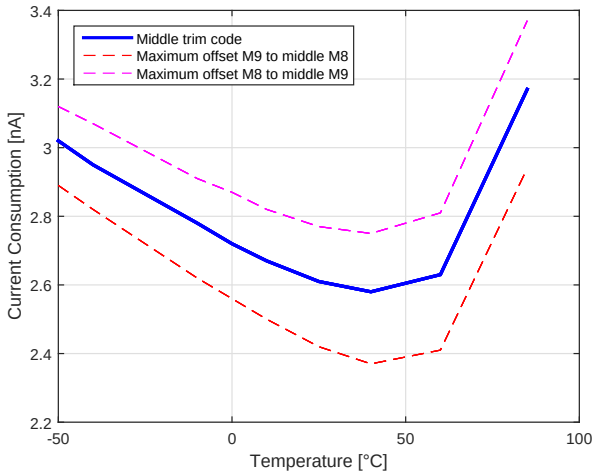


Figure 4.16: Current-Consumption over the temperature range [-40°C - 85°C]

The measured current is below 3.2nA over the temperature range, which is a remarkable single digit nA power consumption. This is obtained at the supply voltage of 0.8V which makes 3.2nW consumption at a frequency of 6500 Hz, leading to a 394 fJ/cycle which was rounded to 400 fJ/cycle this remains fairly constant over the supply range while most other structure would turn into a 10x degradation over the same supply range as best reported in [88].

4.2.1.2 Temperature dependency

In order to demonstrate the effective temperature calibration discussed in Sub-section 3.3, each trimming code was swept over temperature. It is presented Figure 4.17 the typical behavior without any imbalance as the bold line. The maximum imbalance of the transistor M9 with respect to M8 in red and the maximum imbalance of the transistor M8 with respect to M9 in purple. It was applied ±80mV offset to the middle range of M9 with respect to M8. The different measurement results are presented following this convention.

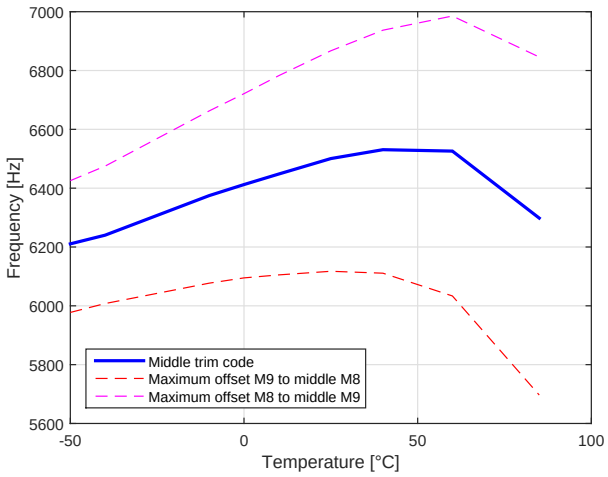


Figure 4.17: Measured frequency over the temperature range [-40°C - 85°C]

The calibrated imbalance has been selected as seven additional unity area of the differential pair in order to get that temperature coefficient. The thermal coefficient is extracted as ±7ppm/°C in the temperature defined in usual human wearable electronics of [-40°C - 85°C]. A more exact formulation of that coefficient would be a second order polynomial function as the curve shape is parabola is given as per Equation 4.14.

$$F(T) = -0.0484T^2 + 3.0314T + 6446.5 \tag{4.14}$$

The derivative of Equation 4.14, provides us with two extreme and remain well-below ±7ppm/°C. The supply voltage Frequency variation is presented in Figure 4.18.

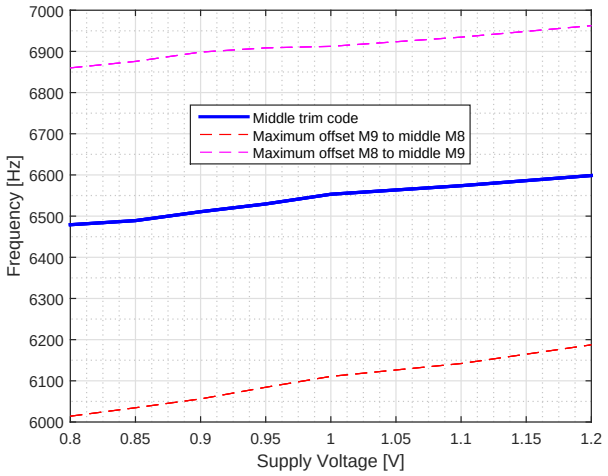


Figure 4.18: Measured frequency over the supply voltage range [0.8V - 1.2V]

This oscillator has a dependency of 0.071 %/V over the operating range 0.8V-1.2V, it is important to note that this result is achieved without any voltage conditioner or regulator in between the power source and the supply pin of the oscillator. A dynamic test was also applied representative of an IR drop and had shown no clock stops down 0.5 V supply, the frequency recovery was lower than 30 μs.

4.2.1.3 Phase noise, Jitter and Allan variance stability assessment.

Most of the above results were presented in two international contributions in [269] and [270], where the emphasis was mode on fully embedded RTC or timer. The Allan deviation presented in Figure 4.20 was not presented so far. The Figure 4.19 propose the jitter distribution. The Jitter measurement were performed using a universal frequency Counter, with 12 digits/s and 20 ps resolution. The JDEC standard JESD65B suggest the following definition. It's measured every interval time or frequency, it is recommended to take a large number of samples and more precisely suggested to take 10'000 cycle as a reasonable sample size. It was accordingly measure every interval between rising edges, and it was logged 10'000 measures these measure being already the results of several measurements. Then it was decided to post-process as period jitter as the measure was intended to measure a long term accuracy. A second reference would not deviate more than 12 PPM correspond to one second per day. A minute reference would not exceed 720 PPM et cetera.

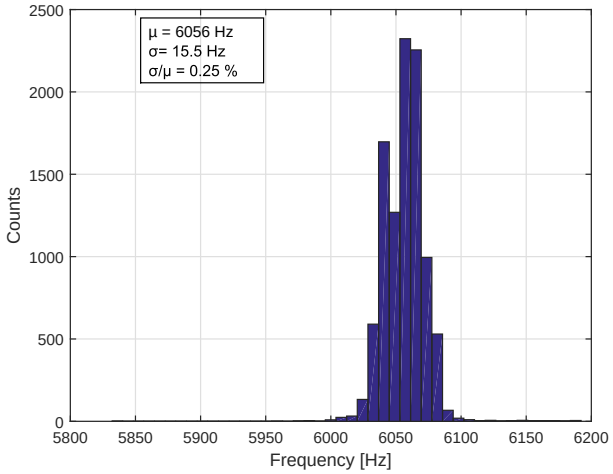


Figure 4.19: Jitter measurements according to JDEC standard JESD65B

The measured deviation is 2500 PPM accordingly this reference could not be itself more accurate than 4 minute a day, 2 hour a month et cetera if the effect is cumulative. In the case of an IoT sensor time stamp it would fit into most of the state of the art appliances especially IoT nodes including time synchronization with the network. Nevertheless the Figure 4.20 provides us with the Allan deviation measurement of the long term stability which also tells us on the cumulative limits of these effects.

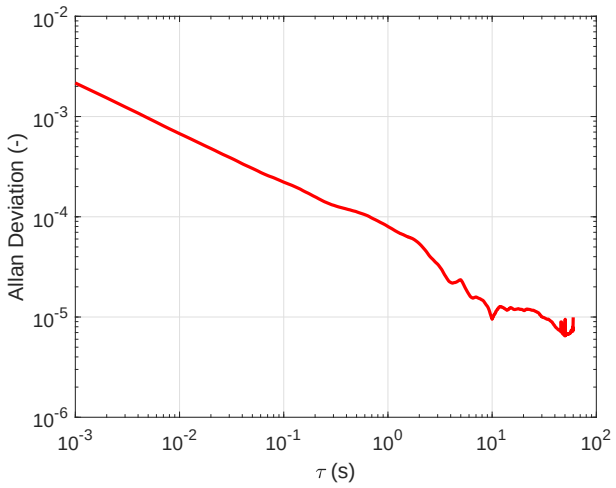


Figure 4.20: Allan Deviation measurements from counter acquired data

It is measured a 100 part per million (ppm) error accumulated in a second. A longer observation will reduce the error toward a plateau at 10 ppm, which level is comparable to a crystal if the sleep period are longer than 10 seconds. The output signal was digital and it's frequency in the kHz range which lead the third harmonic at 21 kHz, thus phase-noise measurement were not considered as most of the benchmark compare with the phase noise at a MHz Offset frequency.

4.3 A 30pJ/bit Self-timed oscillator Based True Random Number Generator

The case study of a true random number generator was introduced in sub-section 3.5. The fully integrated Frequency reference had aimed at an opposite goal to make a frequency generator with low-jitter and low-phase-noise level. The subsection 4.3.2, review some more transistor level aspect on the random number generator. And the sub-section 4.3.2, propose some measurement results and benchmark .

4.3.1 Random Number Generator Architecture

The presented analysis in Figure 3.44 propose a stochastic model of the Shannon's lower bounds of entropy per output bit. Where the clock sampling clock is considered to be way noisier than the self-timed ring oscillator. The fact that we use the C-gate cells partially helps due to the non accumulative behavior of that self-timed ring oscillator [297, 298]. As discussed in [299, 59] the period jitter of a ring oscillator could be increase with a series resistance in between stage. The use of a post-processing imply a data compression, in this case with a parity filter. It suppose independent input bits which increases the entropy rate per output bit but lowers the bit-rate. The Equation 4.15, provides the stochastic model at the output data-flow given the input.

$$P(u)_{OUT} = 0.5 - 2^{n-1} \cdot (P(u)_{in} - 0.5)^n \tag{4.15}$$

It is found from Abacus that a 2^{nd} order filter would be good enough given a 9 stage self-timed ring-oscillator and an uncertainty of 0.1% on the sampling clock generator, which the oscillator presented in sub-section 4.2, was even greater. The Figure 4.21, shows the random number generator architecture and the design steps.

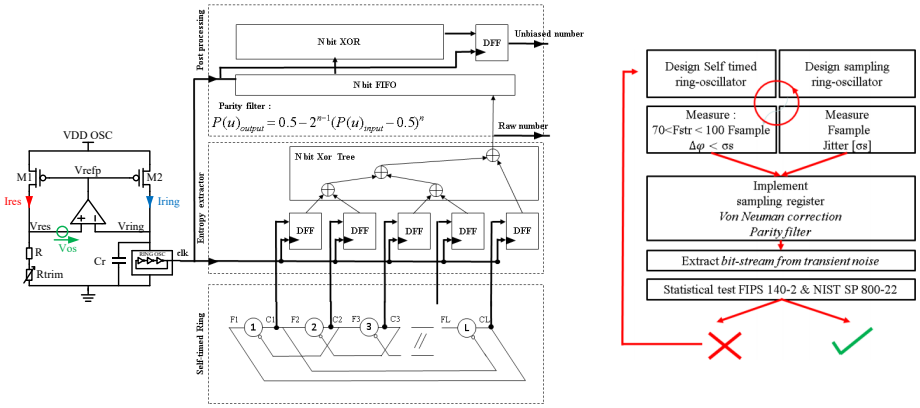


Figure 4.21: Random Number generator Architecture and design guidelines tree

It was ensured to have a lower phase resolution than the sampling jitter and a frequency ratio between 70 and 100 for decorrelation of the two instantaneous phase [298]. The verification at transistor-level were showing compliance to the expected randomness test. One strong hypothesis was made in both case that the noise would mostly be white and thus a Gaussian distribution, while considering sub-threshold some observation of a non Gaussian distribution were made [208, 181]. In this prospect the ring oscillator was made out of resistor which white noise is a know source and could be characterized as discussed in [299, 59].

4.3.2 Random Number Generator experimental results and analysis

The Figure 4.22, shows the random number generator test die integrated in a 180 nm CMOS Flash process node.

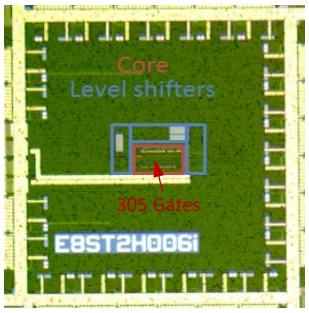


Figure 4.22: Random Number generator Die Picture

This generator is quite compact with 305 NAND2 equivalent gate surface. The Figure 4.23, shows the measurement of jitter of the two oscillators while sweeping the voltage. It could be observed that both are mostly Gaussian and increases their spread with decreasing the voltage.

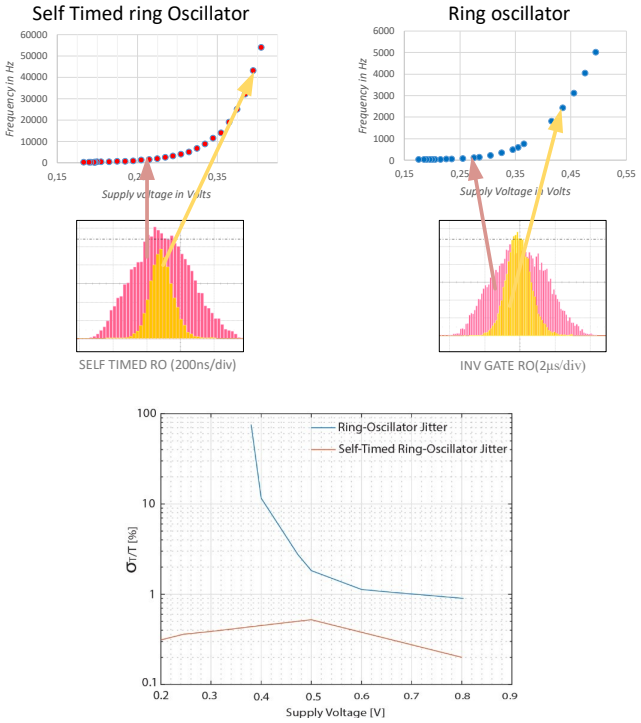


Figure 4.23: Random Number generator jitter measurements

A qualitative measure of the randomness is the period variance normalized to the period $\left(\frac{\sigma_T}{T}\right)$. The Figure 4.24, propose a summary of the measured performances of the random number generator.

T° stream		-40°C	25°C	+80°C
f_samp (Hz)		530	546	935
σ_samp (µs)		2.3	3.6	2.8
Δφ (µs)		1.29	1.23	0.64
σ_samp / Δφ		1,78	2.92	4.38
f_stro/ f_samp		81	82	93
Parity post processing	FIPS 140-1	PASS	PASS	PASS
	FIPS 140-2	PASS	PASS	PASS
	NIST SP 800-22	PASS	PASS	PASS
	E (pJ/bit)	29.9	29.6	19.1

Figure 4.24: Random Number generator Summary of the performances over temperature

The sampling clock jitter is managed to be kept higher than phase resolution and it is kept greater than 80 frequency ratio between the self-timed ring oscillator. It ensure a random output data-flow with respect to NIST SP800-22 standard and this is happens with an energy consumption below 30 pJ/bit. The Figure 4.25, propose a comparisons to recent paper on random number generator.

	This work	K. Yang JSSC 2016	Q. Tang CICC 2014	C. Tokunaga JSSC 2008
Technology	180 nm	180 nm	65 nm	130nm
Area [gate]	305	697	4166	3500
Entropy source	Jitter in oscillator	Jitter in oscillator	Jitter in oscillator	Metastability
Operating conditions	1V – 1.8V	0.8V – 1.2V	0.8V – 1.2V	N/A
	-40° - 80°	-40° - 120°	N/A	
Bit rate [kb/s]	0.5	180	2000	200
Latency [cylce]	1	N/A	N/A	N/A
Efficiency [pJ/bit]	30	21	66	5000
NIST SP 800-22	ALL	ALL	ALL	5/15

Figure 4.25: Random Number generator comparison to recent papers

The comparison with published generator shows a quite efficient principle with a lower complexity but a low data-rate. A further bench-marking is proposed in Figure 4.26. The requirements for a random number generator could be broad. Initial challenge was to see what could be obtained from nA level power consumption. For instance the requirements in a RFID use case from are rather the area and power to improve, rather than the quality of the random number itself, since it is most of the time used in an anti-collision mechanism.

Figure 4.26: Random Number generator Benchmarks

Besides energy efficiency with consumption below 100 pJ/Bit, it in fact reach a 10 nW power consumption which is far below other proposal, with an extremely low gate complexity below 500 gates. The data rate could be improved reusing these design guidelines for a higher throughput In that case seed for the EPC-Gen2 RFID anti-collision mechanism, such a throughput 500 bits/s is enough.

4.4 Crystal oscillator use in a Real-Time-Clock.

Time-keeping units based on a 32.768 kHz crystal oscillator (XO) stand as a favorite, low-power and cost effective solution. Ubiquitous computing devices lie at the heart of the connected objects revolution and influence the way we connect. Keeping track of the flow of time is key [33]. Most Systems On Chip have integrated XO with a frequency error based on the combining

of an integrated silicon oscillator and an on-board resonator. These parts are quite sensitive to environmental variations such as temperature, light, moisture and stray capacitance. For some applications, further miniaturization, tighter accuracy, and power consumption are required. Literature has reported on a significant amount of work in the area [61, 300, 301, 272, 224, 63]. RTC was shown in [63] to be a key management block in the scheduling of precise wake-up at user predefined intervals. Timekeeping appliances are used in a wide variety of applications such as metering, smart-building, medicine, in wearable devices and automotive products. An RTC is also a key component of secured systems with time synchronized to a trusted platform preventing replay attacks. However, power consumption remains the key issue. A low power, compact and cheap RTC is a crucial component of time-keeping devices. From a power perspective, the circuit must feature an ultra-low power 32.768 kHz XO, a power management unit including a current reference, a voltage regulator handling high loads of Non Volatile Memory, a read or write cycle and I2C transactions. Additionally, a trickle charger and a voltage switch over complete the power management unit. Digital functions include essential RTC functions (second, minutes, hours, day month, years et cætera), event detection, and memory for application programmability. Some security features such as Unique Identifier (UID) and passwords are implemented. The RTC module power consumption was isolated into three parts: power-management, digital circuitry, and the crystal oscillator (see the block diagram depicted in Figure 4.27-(a). Most commercial real-time clocks run their crystal oscillator with amplitude regulation at 400 mV and load capacitances in the order of 6pF leading to 170 nA of current consumption. Some more advanced techniques report commercially available 60nA crystal oscillators [302], which is still higher than the whole consumption of the proposed RTC module. The current consumption breakdown is presented in Figure 4.27-(c), as a pie chart. A crystal oscillator and power management are the main contributors.

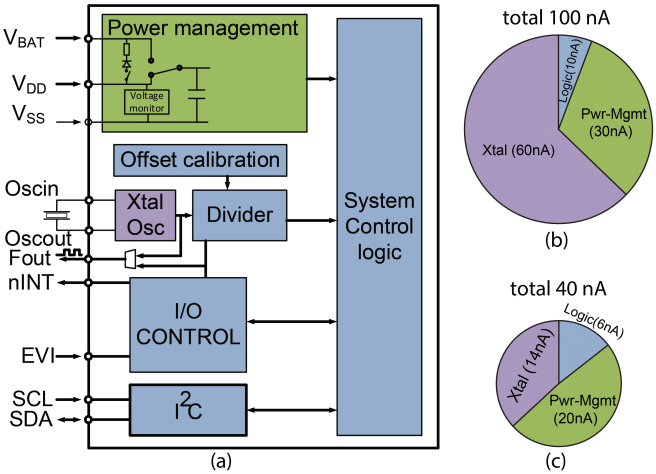


Figure 4.27: Example real-time clock module architecture and power budget

This work focused on optimizing crystal oscillator power consumption leveraging self-biased circuit and voltage-scaling technique. The main advantages and limitations were introduced in the Sub-section 3.4.

4.4.1 Crystal oscillator experimental results and analysis

The circuit die photo is shown Figure 4.28. It is integrated into a 180 nm CMOS Flash process and measures 1.182 × 0.72 mm2. It is a flip-chip bonded using gold studs on the bottom layer of a miniature 3.2 × 1.5 mm2 ceramic package containing 8 IOs in addition to the two internal XTAL leads and a test IO used in the wafer level test. The latter is assembled attached to its side on the second level of the package.

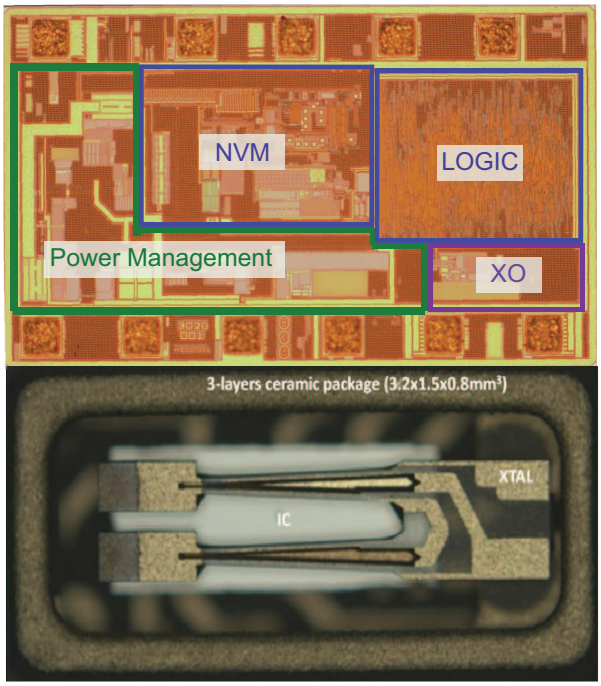


Figure 4.28: Die and package micro-photo

Finally, after laser-trimming of the XTAL, a metal lid is reflow-soldered on the third level to seal the package at low pressure, below 0.1mbar. The vacuum is made to maximize the resonator quality factor. It is important to note that motional dissipation scales with the square weight of the quality factor [63]. Parts are then individually calibrated in large batches before the compensation parameters are stored in the on-chip nonvolatile memory.

4.4.1.1 Power consumption and oscillation amplitude validation.

Measured amplitude and current over a voltage supply sweep from 0.6V to 1.2V are presented in Figure 4.29. These measurements were performed on a batch of standard DILS chips and not a CM7 ceramic-sealed package. Two crystals available on the market with different quality factors for CM7 were used in the vacuum-packaged solutions. The quality factors are 30 838 for CM7 and 90 000 for AB38T. As these measurements were made out of a batch, an average value was plotted, and its standard deviation is highlighted with a shaded plot. The first observation is that the oscillation amplitude is well controlled. Based on the calculation of the 0-order

modified Bessel function (5), an amplitude of 80 mV close to 3 UT was expected. Measurement shows an amplitude between 75mV and 120 mV, so +/-25 % amplitude with 3 variations. It is worth mentioning that the low motional resistor (loss) induced a higher amplitude. In the Fig. 10, the current consumption of the same batch is reported for the crystal resonator as a function of the supply voltage. The mean value is the solid line, and the shaded bar represents the 3 variability of the lot which is +/-14 %. The CM7 resonator consumes 14nA at 1V.

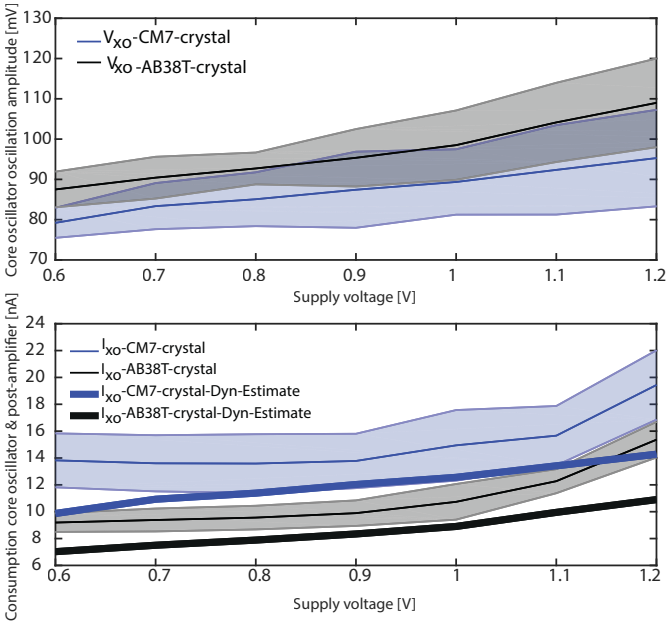


Figure 4.29: Power consumption as a function of supply voltage

When encapsulating the resonator and IC in the same package, the current consumption reported in Figure 4.29 reduced by 5nA. Alternatively, using a crystal resonator of a higher quality factor gave the same results. The dynamic power consumption estimation was reported in Figure 4.29. An overhead is attributed to the post-amplifier for 1.5 nA up to 4nA over PVT variations. This means at room temperature that the core oscillator bias is less than 1nA, which means attaining lower power consumption will rely on optimizing the load capacitors as well as the resonator itself.

4.4.1.2 Supply voltage dependency

The frequency deviation concerning the supply voltage is reported in Figure 4.30. The measurements were entirely spreading from +/- 15ppm; a trend was extracted as 2.1ppm/V above the measurement reports a restricted supply range 0.5 to1.3V as the on-chip regulator regulates the supply voltage to 1.1 V. The frequency deviation concerning the supply voltage is reported in Figure 4.30. The measurements were entirely spreading from +/- 15ppm; a trend was extracted as 2.1ppm/V above the measurement reports a restricted supply range 0.5 to 1.3V as the on-chip regulator regulates the supply voltage to 1.1 V.

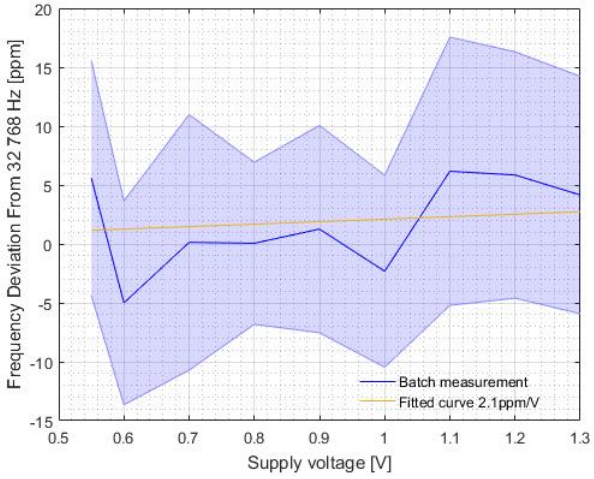


Figure 4.30: Frequency deviation as a function of supply voltage

4.4.1.3 Temperature dependency

The frequency deviation concerning temperature is reported in Figure 4.31. It is highly correlated to the resonator curve fitting provided by the supplier of the CM7V-T1A resonator which correspond to $\frac{\Delta F_0}{\Delta T} = -0.035 \cdot (T - T_o)^2$.

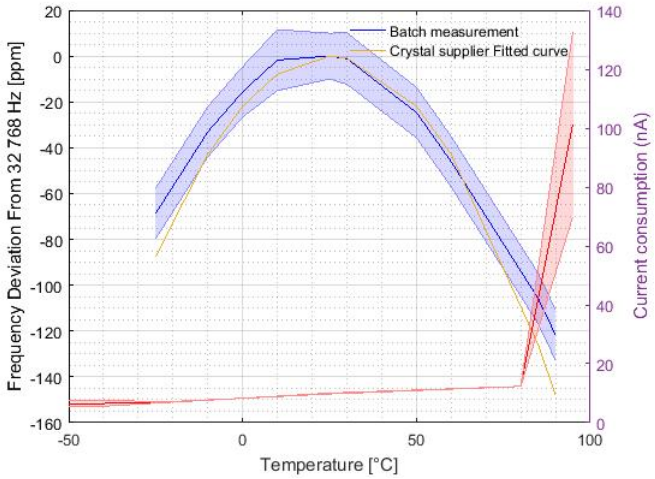


Figure 4.31: Frequency deviation and current consumption as a function of temperature

The Frequency deviation concerning temperature was as expected the contribution comes mostly from the tuning for dependence to the temperature. The current consumption is PTAT up to 80°C, and further increase due to leakages. One can derive the dependency due to

capacitance as per Equation 4.16.

$$\frac{\Delta\omega}{\omega} = \frac{C_m}{2 \cdot C_0} \cdot \frac{C_L}{C_0} \cdot \frac{1}{1 + \frac{C_L}{C_0}} \cdot \frac{\triangle C_L}{C_L} \sim \frac{1}{1000} \cdot \frac{\triangle C_L}{C_L} \tag{4.16}$$

Which can provide an insight in the variation of the measurement with respect to the fitting function of the crystal.

4.4.1.4 Phase noise, Jitter and Allan variance stability assessment.

The Figure 4.32 extend the analysis proposed in sub-section 3.4.2 with measurement results. The result correspond to the prediction of pss and pnoise verification where the cyclostationary contribution of the level shifter, which is due to the limited current charging the output capacitance.

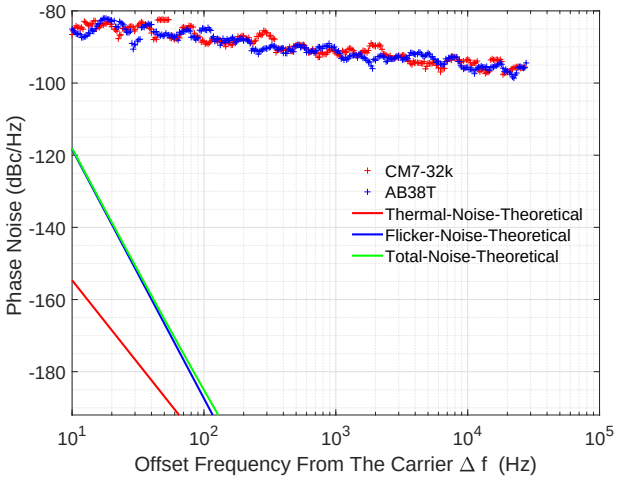


Figure 4.32: Phase Noise Measurement and comparison

Further measurement are proposed in the Figure 4.33. The purpose of these measurements was to check different crystal which Quality factor and related properties varies.

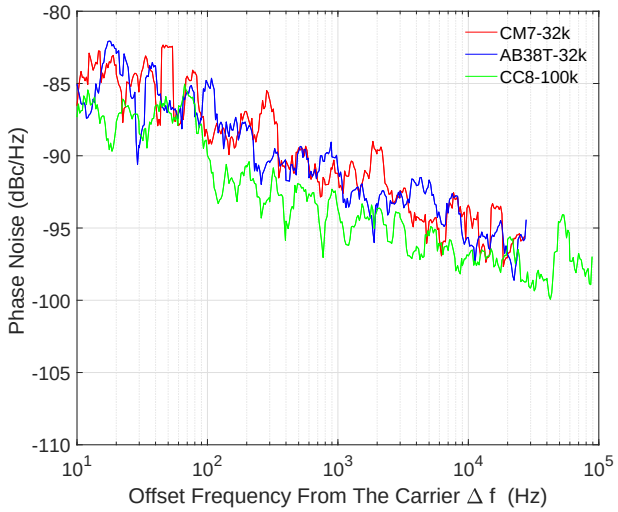


Figure 4.33: Phase Noise Measurement and comparison

It also propose a different frequency which is upper and include a higher quality factor. These measurement are all well aligned and confirms the phase noise contribution comes from the level shifter function. the Figure 4.34. The measurement shows the Allan Variance.

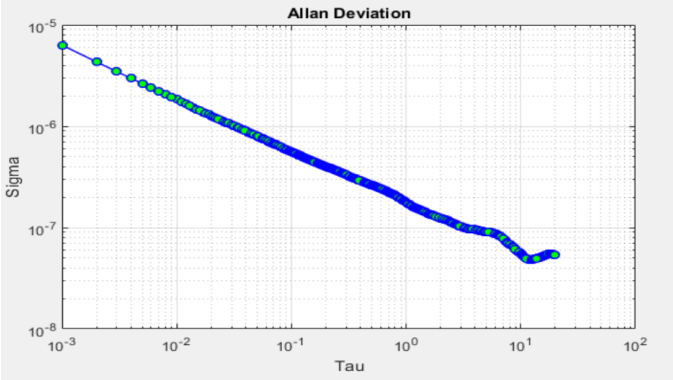


Figure 4.34: Phase Noise Measurement and comparison

It is measured a 0.2 part per million (ppm) error accumulated in a second. A longer observation will reduce the error toward a plateau at 0.06 ppm, which level is ensuring a good performance for time keeping unit.

A new XO architecture with a transistor level functional merge and a power injection mechanism added to the resonator allowed for energy savings to be achieved by reducing resonator load capacitances and oscillation amplitude. This paper proposes a 10nA at a 1V self-biased amplitude-regulated COS XO, leveraging voltage scaling down three thermodynamic voltage levels for extremely low power consumption. This consumption pushes the limits of dynamic

current consumption in the considered node. Table 4.33, Attempt benchmark with other reported crystal oscillators supplied at 1V, embedded or not in real-time clock modules.

Parameters	This work	K. Hsiao ISSCC 2014	D. Ruffieux ISSCC 2016	A. Shrivastava JSSC 2016	W. Thommen ESSCIRC 1999	D. Yoon JSSC 2016
Process [nm]	180	28	350	130	2000	180
XO Area [mm²]	0.035	0.03	N/A	0.0625	N/A	0.3
Normalized XO Area [■. 10^6]	1.06	42,8	N/A	3.7	N/A	9,25
XO type	XO	XO	DTCXO	XO	XO	XO
Frequency [Hz]	32 768	32 768	32 768	32 768	32 768	32 768
Crystal Quality factor Q [-]	30 838	N/A	30 838	90 000	33 729	N/A
Temperature range [°C]	-40 – 85	-20 – 80	-40 – 85	0 – 80	N/A	-20 – 80
Temperature drift over range[ppm]	120	48.8	5	150	N/A	140
Supply voltage range [V]	0.4 – 5.5	0.15 – 0.5	-	0.3 – 0.9	1.2 – 0.9	0.3 – 0.8
Supply voltage drift [ppm/V]	2.1	66	N/A	7	N/A	N/A
Jitter [ns]	40	1000	N/A	80	N/A	N/A
Amplitude [mV]	90	N/A	N/A	230	100	100
Core-Osc Current @1V [nA]	10	140	16	500	22	11
Current sensitivity to supply [nA/V]	25	160	N/A	913	N/A	43.6
Start-up time [µs]	144 – 1000	N/A	N/A	N/A	N/A	1000 – 3000

Table 4.5: Table benchmark of RTC XO modules

As the crystal quality factor is not provided to guarantee the architecture dependency and transistor level complexity, the XO area was normalized to the minimum feature size. Before normalization, the size is comparable to a 28nm XO [61] including load caps, thanks to a low transistor count. The power consumption is comparable to [63] in the same operating conditions. Nevertheless, the crystal quality factor is not reported for every XO. The frequency performance of the crystal is maintained through commercial temperatures ranging from –40 to 85°C at a 100ppm tolerance. Stability metrics of peak to peak jitter was measured which would be compatible with a fully digital thermos compensation through pulse inhibition. Finally, the start-up time was improved and compared to [63].

4.5 Phase locked Loop use in battery operated system on chip.

Active Electrostatic digitizer is getting popular input human-machine interface devices following a similar path as miles are with information and communication technologies (ICT) such as a computer, and tablets. These active digitizer are implicitly having transactions between the display and the digitizer. Protocols in place are requesting few different accurate frequency in phase with reference [303, 304, 305]. The technology under investigation uses 2 PLL dedicated to the ES reception and transmission communication. One generates a 4MHz clock signal for both RX and TX. The second could be either be 950 kHz, and other frequencies for TX only. Both PLLs generate frequency clocks from a 32.7768 kHz time reference. Format selection is controllable by CPU through the logic by protocol selection data decoded by the logic. The transaction follows a pattern which wakes up the PLLs and put these into an idle mode and back to sleep such as to the one proposed in Figure 4.35.

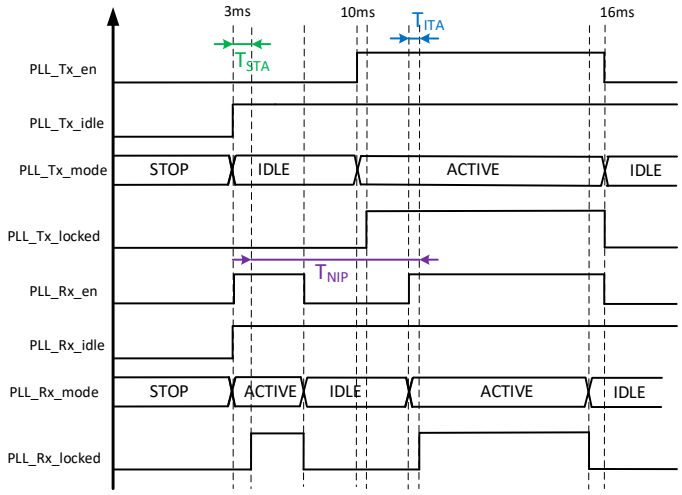


Figure 4.35: Phase locked Loops transaction level timing diagram

The diagram, includes some numbers about timescale. It is noteworthy that there is a pause in the order of magnitude of 10 ms (TNIP), The time from “STOP” to “ACTIVE” mode (TSTA) is considered longer than the time from “IDLE” to “ACTIVE” mode (TITA). As shown in [306], it is necessary to reduce the consumption in the transient mode from hibernate to active mode and reversely. When timescale between two active events are in greater than settling time of the overall function it is of interest to evaluate potential gain with first order macro-models for power consumption such as [307]. In the system the frequency reference is set from a 32.768 kHz crystal oscillator. The device also defines the constraints of a battery operated the device operating at low voltage (0.9V), and require a high efficiency such function should target sub 1.5uA/MHz. And finally achieve a sub 30 reference cycle to lock.

4.5.1 Phase locked Loop architecture guidelines and analysis

Frequency synthesis using the 32.768 kHz crystal oscillator was mandatory due to the synchronous process for data modulation and demodulation with this reference. Using charge-pump phase-locked-loop (CP-PLL) imposing a Type II PLL was then considered. and a second order filter a good trade-off between accuracy and settling time, an analysis of the linearized PLL model is proposed in the Figure 4.36.

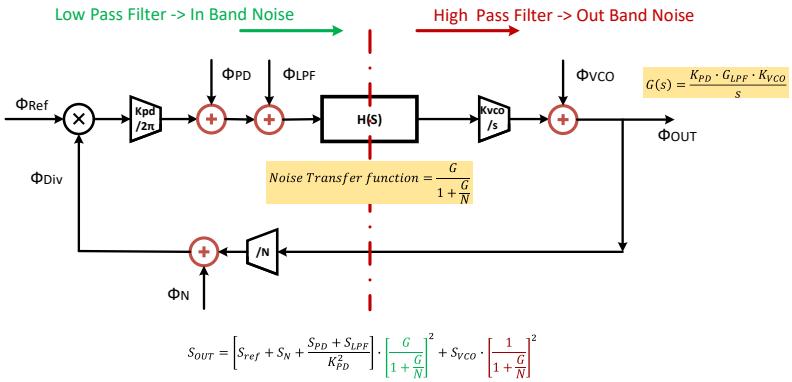


Figure 4.36: Linear model of a Type-II PLL including In-Band Noise and Out-band Noise contributors

The small signal transfer function is given by Equation 4.17.

$$\frac{\Phi_{DIV}}{\Phi_{REF}} = \frac{N \cdot K_{loop} \cdot (s + \frac{1}{R_z C_z})}{R_z \cdot C_p \cdot s^3 + (\frac{C_z + C_p}{C_z}) \cdot s^2 + K_{loop} \cdot s + \frac{K_{loop}}{R_z \cdot C_z}} \tag{4.17}$$

With the static loop gain defined per Equation 4.18, is composed of charge pump gain (K_D), basically current, the VCO linearized gain (K_{vco}), the resistor filter parameter (R_z), and the feedback divider parameter (N).

$$K_{loop} = \frac{K_D \cdot K_{vco} \cdot R_z}{N} \tag{4.18}$$

As most of the high order systems it could be simplified as a second order system as per Equation 4.19.

$$TF(s) = \frac{K \cdot \omega_n^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \tag{4.19}$$

Where the natural pulsation is identified as per Equation 4.20, and the damping factor as per Equation 4.21.

$$\omega_n = \sqrt{\frac{K_D \cdot K_{vco}}{N \cdot C_z}} \tag{4.20}$$

$$\zeta = \frac{\omega_n}{2} \cdot R_z \cdot C_z = \frac{1}{2} \cdot \sqrt{\frac{K_D \cdot K_{vco} \cdot R_z}{N} R_z \cdot C_z} \tag{4.21}$$

When the damping factor (ζ) is comprised in the range 0 to 1 then the lock time could be estimated as per Equation 4.22.

$$t_{lock} = -\frac{\ln(\frac{\epsilon_{tol}}{\Delta_F} \cdot \sqrt{1-\zeta^2})}{\zeta \cdot \omega_n} \tag{4.22}$$

This modeling is not taking into account the pull-in time which is out of the scope of this analysis. It is noteworthy that it is a widely discussed topic which accounts for the non-linearity of the phase detector and cycles slipping in [308, 309], and would model more accurately the system dynamics and it is the time from an unlock to a lock state. Most of the investigations assumes a sinusoidal phase detector which does not hold in case of the tri-state Phase-Frequency detector. In this following it is provided some definitions, then assumption taken to estimate the Pull in time and finally a more elaborated mathematical approach where it was introduced a continuous function for the Type-II tri-state Phase-Frequency Detector (PFD) and a numerical solution of the linear locking conditions.

- **Pull in range :** describe the PLL dynamic state (acquisition mode) it's the range within which a PLL will always become locked through the acquisition process. PLL is initially unlocked, it will acquire lock if a reference frequency within the pull in range is applied if the reference frequency is outside the pull in range PLL will not be able to lock onto the reference signal. The pull-in range for the PLLs using PFD as the phase detector is infinite. In practice, the pull-in range corresponds to the range frequency VCO can generate. The pull-in range for this type PLL is infinite Because any loop filter cascaded with the PFD behaves as a real integrator when both flip-flops of the PFD are in the 0 state, which means it has a pole at s=0. Hence, the DC gain of all loop filters is infinite and the pull-in range also becomes infinite

- **Pull-in Time :** PLL dynamic state (acquisition mode), reach the locked state (also called steady state) within a time which is by definition not null and equal to the Pull-in time.

- **Locking conditions :** The locked state (also called steady state), the signal's phase space must satisfy the following conditions. The phase error $\phi_e(t)$ is constant. The frequency error is zero. Mathematically it can be expressed as the first derivative or the phase error $\phi_e(t)$, with respect to time that cancel as per Equation 4.23.

  $$\frac{\partial \phi_e(t)}{\partial t} = 0 \tag{4.23}$$

  Thus it ensure that the frequency error is null as phase is integral of the frequency. and phase error is constant as the derivative of a constant is null. As the phase error is the

input of the loop it means that equivalent linear or non linear model time dependent must be found in order to establish the differential equation that would model the dynamic of the loop. For the tri-state PLL it is Initially assumed that:

1. the input reference frequency is ω_{ref}.
2. The output frequency of VCO is center frequency ω_0.
3. A uni-polar supply used in PFD, so it's output voltage is: vdd/2.
4. As a consequence, the frequency offset is : $\Delta\omega = \omega_{ref} - \omega_0$.

In order to get locked, the VCO must create an output frequency that is offset from the center frequency: $N \cdot \Delta\omega$. Thus the input voltage is increased by $\frac{N \cdot \Delta\omega}{K_{vco}}$. The outputs of Phase-Frequency Detector are toggling between 0 and VDD which on average is a saw-tooth signal. Due to the reference frequency is higher than bandwidth of the loop filter create an average output of the Phase-Frequency Detector outputs. Therefore, the pull-in time is the time for the square wave charging the capacitor of loop filter such that the input voltage of VCO is equal to $\frac{N \cdot \Delta\omega}{K_{vco}}$. In case of damping coefficient the loop filter could be approximated as 1st order and dead time, so capacitor charge can be estimated with the general first order solution as per Equation 4.24.

$$\frac{N \cdot \Delta\omega}{K_{vco}} = \frac{vdd}{2} \cdot (1 - e^{\frac{T_p}{\tau}}) \tag{4.24}$$

Thus solving this condition the pull-in time is written as per Equation 4.25.

$$T_p = \tau \cdot \ln\left(\frac{\frac{vdd \cdot K_{vco}}{2 \cdot N}}{\frac{vdd \cdot K_{vco}}{2 \cdot N} - \Delta\omega}\right) \tag{4.25}$$

Equation 4.26, provide a first estimation, the time constant τ, must be estimated as a matter of fact that the filter time constant is a tenth of the reference frequency (For a 32.768 kHz reference, we would assume a cut of frequency F_c of the filter at 3.2768 kHz.

$$\tau = \frac{1}{2 \cdot \pi \cdot F_c} = 4.8570 \cdot 10^{-6}\,(rad/s) \tag{4.26}$$

It is important to note that, the Pull-in Time denote for Frequency acquisition on top of that there is another dynamics to account for which is linear dynamics (small signal) and denotes for the phase acquisition. An example on the critical case of a 950 kHz PLL From a 32.768 kHz with a VCO gain of 0.181 MHz/V, 8Khz/trim bit and 3.268Khz Bandwidth supplied under

1,05V is provided. The below Figure 4.37 shows, the Pull-in time summed with the Lock-in time (black) representatives of Frequency and Phase acquisition respectively. The blue line is representative of Pull-in time.

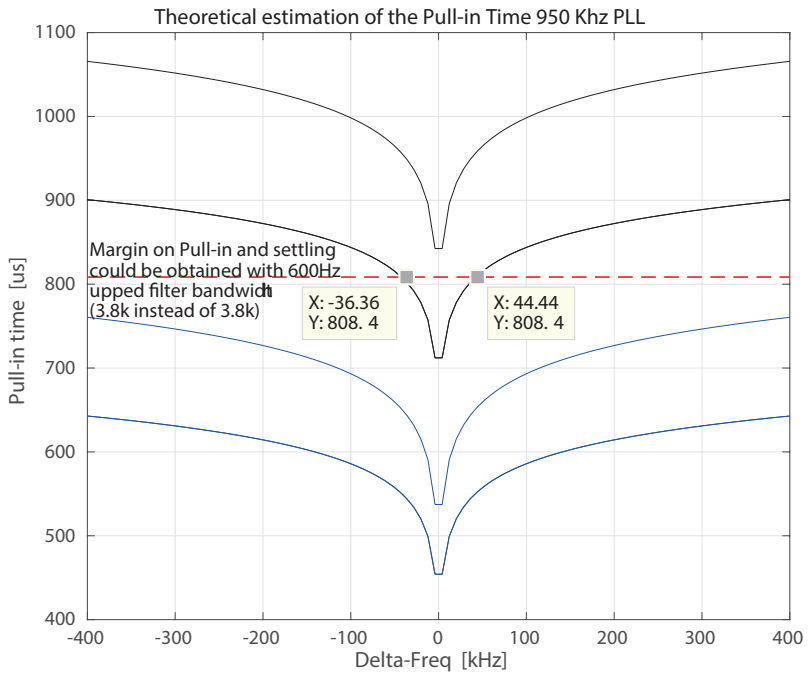


Figure 4.37: Calculated CP-PLL Type 2 third order pull-in time with continuous interpolation of the Phase Frequency Detector

The red dashed line represent the specification with a subtraction of the power management and initialization sequence needs. It could be seen that the pre-charge to Vdd/2 as a positive effect which must lead to a Frequency acquisition phase below the start-up time specification. The filter bandwidth was extended by 600 Hz such that the start-up time specification is achievable. It is important to note that a range of +/- 50 kHz is then allowed as the initial frequency offset of the VCO. An empirical approach in [310], compares to Equation 4.22. The reduced settling time of third and second order are de-normalized to a 3.2 kHz bandwidth, and as the system order is 3, the damping coefficient is approximated as in [310], the optimum settling time behavior is obtained for a 50° Phase margin or 0.5 damping. The phase locked loop block diagram is proposed in Figure 4.38

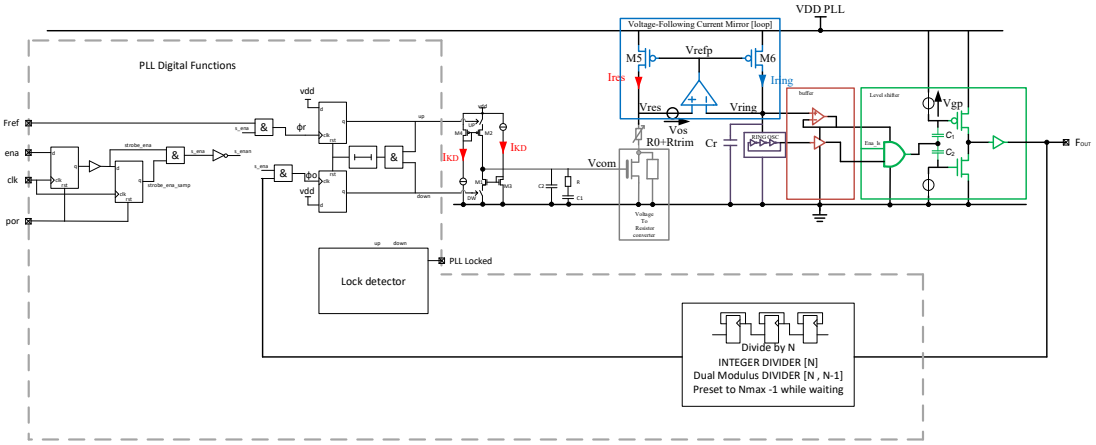


Figure 4.38: Simplified Architecture of the PLL

On top of that we had implemented a filter presetting as introduced in [311] ensure that our trimmed VCO is in the acceptable frequency range before the locking operation is released in order to assure a linear-mode settling operation shown in Figure 4.37. The phase locked loop was integrated in a 180 nm process.

Frequency offset boundary were set by analysis to be+/- 50 kHz. The original center trimming code was found 30 kHz above the expected center Frequency.

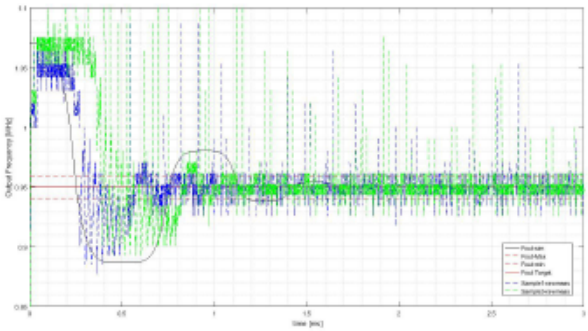


Figure 4.39: Frequency measurement of the presetted PLL Locking sequence (un-trimmed)

The Figure 4.39, propose an acquisition of the output Frequency sampled every 10μs. There are some glitches due to the instrumentation.

The measurement of two samples are proposed (green and blue) lines. The target in terms of mean an peak to peak jitter is proposed in the red lines. Finally the envelope linear model including a non linear Phase Frequency Detector and the same VCO offset propose a numerical results plotted in black line. The two samples output frequency and their prediction matched quite accurately. The average typical lock time after trimming is 900µs which represents 30 cycle making a near failed specification.

The average typical lock time after trimming is 600μs, which represents 20 cycle, the average current consumption was 1.15uA/MHz in active mode, While the idle mode consumption was reduced to 200nA, enabling energy savings at system level.

4.6 Thermoelectric Energy Harvesting

Chasing any overhead consumption is critical in the ultra-low power circuit, although func-tionally, it is expected to fulfill the same function. An industrial grade energy harvester circuit for the solar or thermoelectric source would include functions such as power-on-reset, max-imum power point tracking DC-DC converter, battery charger and peripherals for regular operation (oscillator, bias, custom logic. . .) as shown fig1. All these different blocks have to be co-designed to maximize efficiency over different power ranges. There is a situation where the short term and long term and short term storage are empty which is called “cold-start” as the system must start without any stored energy but harvest it from the environment. Which is the problem addressed in this section. The Figure 4.40 present an energy harvester circuit from DC renewable source.

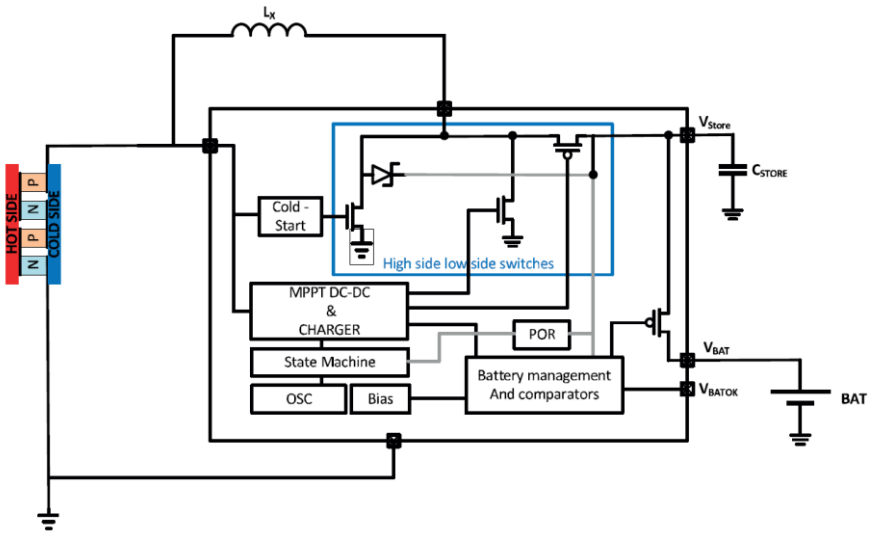


Figure 4.40: DC source Harvesting Integrated Circuit block diagram

The thermoelectric energy is a potential candidate in quite a few applications from wearable electronics where 2K difference assume a great thermal assembly to the industrial application where it could be up to 10 Kelvin thermal gradient. Bi2Te3 thermoelectric generator (TEG), is in production and produce approximately 28 mV/K/cm2. A reasonable size and thermal packaging requires the electronics to start with a few thermodynamics voltages. In the Joule thief principle presented in [312], it was demonstrated operation sub-thermodynamics voltage. This approach uses a voltage transformer as a magnetic which is bulky, relatively expensive and specific to a power range [313]. Therefore a striving need for a solution that keeps using efficient over a wide range of input power a DC-DC boost including its maximum power point tracking and get kick-started with voltage as low as 2uT (60mV) was is investigated in this paper from the theoretical basis to the results of implementations and discussion. Theoretical background Any charge pump or DC-DC converter tend to be modeled as shown in Figure 4.41 The equivalent circuit of a charge pump with N stages.

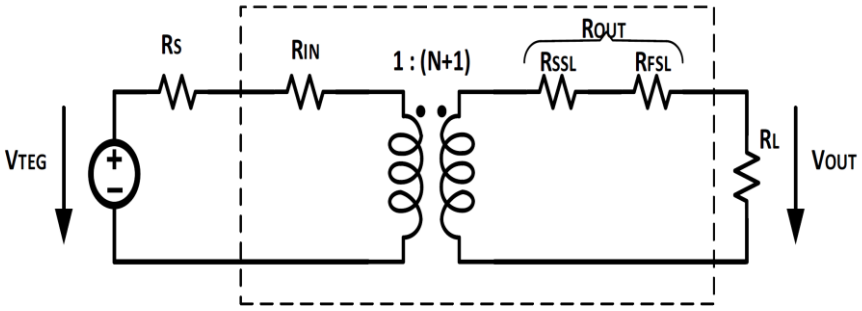


Figure 4.41: Equivalent circuit of a charge pump with N stages

From the above equivalent model, recalled from [314], the available input power could be

derived by Equation 4.27.

$$P_{in} = \frac{V_{TEG}.R_{IN}}{(R_S + R_{IN})^2} \tag{4.27}$$

Thus, Maximum Power Point (MPP) transfer would occur for $R_S = R_{IN}$, which would be the function of Maximum Power Point tracking. At cold start the maximum voltage would be defined by the size of the harvester and its temperature g radient. Thus, the goal is not to track the Maximum Power Point but maintain a harvester voltage as high as possible. In this context, the key challenge in an ultra-low-voltage step-up converter is to start-up an oscillator in the tens of mV range [315, 316]. Although inductive boost converters are advantageous, with respect to capacitive converters, for their efficiency [314], the gate drivers require at least 600mV for startup and to sustain a few μA [317]. As a consequence a charge-pump is needed to start-up the system. Fig 4.42 shows three different architectures with the same cold start intention.

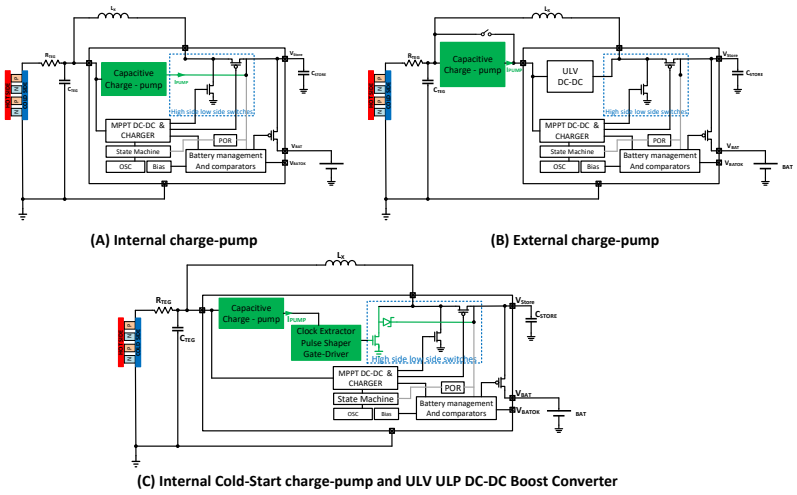


Figure 4.42: Comparison (a) Internal charge-pump charging the short term storage directly, (b) External charge-pump supporting the present cold start circuit of an on-the-shelf component, (c) Internal charge-pump supporting an optimized DC-DC driver

Some commutation cells tend to be efficient, reducing either the slow switching losses or the fast switching, where the output resistor is inversely proportional to the switching frequency and a flying capacitance, as proposed in Equation (4.28).

$$R_{OUT_{FSL}} \propto \frac{1}{k \cdot F \cdot C} \tag{4.28}$$

The factor k, can be larger than one in multi-phase converter or bi-linear switched capacitor cells thus reducing the output impedance and causing a voltage drop across the switches in

one phase and another. This leads to the conclusion that the losses are mostly due to the conduction losses also known as slow switching losses, as proposed in Equation (4.29).

$$R_{OUT_{SSL}} \propto \frac{1}{2 \cdot g_m} \tag{4.29}$$

Moreover, the output resistor [314], is given by Equation (4.30).

$$R_{OUT} \propto \sqrt{R^2_{OUT_{SSL}} + R^2_{OUT_{FSL}}} \tag{4.30}$$

The work of [254], demonstrated that a standard fully integrated ring oscillator cannot start below 36mV at room temperature. Given this supply range, the conduction losses will dominate if the oscillator starts. The conduction loss $\frac{1}{g_m}$, is in the order of magnitude of the $G\Omega$, which would require dramatically high load impedance.

In Fig 4.45 (a) it is thaught to build-up a voltage that would directly supply the inductive converter while (b) proposes a companion circuit that would sustain the cold-start function. Finally, Figure 4.45 (c) proposes an optimization of the cold-start charge-pump and gate driver. Equation (4.31), proposes a rational approximation of the output resistor needed for the charge-pump.

$$R_{OUT_{CP}} \propto \frac{1}{10} \cdot \frac{V_{out}}{I_{out}} \tag{4.31}$$

Case (a), requires a Harvester ICs 1.3V to trigger the power-on reset and 3 μA to sustain the start-up, leading to a charge-pump output impedance of 43 $k\Omega$. The same consumption applies for 0.3V output voltage for case (b) leading to a charge-pump output impedance of 15 $k\Omega$. Case (c), represents another way to tackle the cold-start challenge with an optimized gate driver for delivering 600mV and 5nA; as a consequence 12 $M\Omega$ is required as charge-pump output impedance. With respect to the converter using magnetically coupled coils such as [318, 319], the proposed inductive boost converter actuation starts up without any extra external coil.

At a voltage supply below a 100mV, the ratio of ON current to OFF current in an inverter is very low due to deep-sub-threshold transistor conduction. Also, the DC gain further reduces [320]. Under this condition, a ring oscillator barely satisfies oscillation criteria with many stages, and generates low clock frequency. In opposition to the stacked inverters in [320], the technique proposed in [321, 322] is the so-called Dynamic Threshold MOSfet (DTMOS) and addresses the problem at device level. A ring oscillator implementation shows minimal supply voltage close to the theoretical bound in post layout simulation [323]. Taking into account the theoretical comparison shown in [253] one would rather select a Dickson topology.

However, as shown in Figure. 4.43, when taking into account the overhead consumption of sustaining the oscillator itself the circuit would in theory not start-up before 120mV.

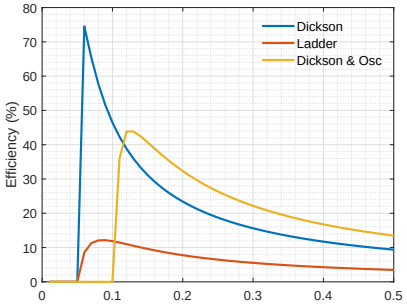


Figure 4.43: Theoretical comparison of the Ladder and Dickson topology conversion efficiency in the sub 0.5V range.

Although it's low voltage efficiency is limited, the ladder step-up cell could be implemented based on CMOS inverters [324]. Which justifies a self-oscillating ladder topology to assure the cold-start sequence, [325]. When a sustainable operating point is reached the function is disabled.

4.6.0.1 Operation principle

The actuation of a DC-DC converter for a low voltage power source designated 2 in the Figure 4.44, wherein the converter operates in discontinuous mode and comprises an inductor designated Lx in the Figure 4.44. The discontinuous mode imply that the current across the inductor cancels earlier than the switching period. The inductor connects to the power source providing an input voltage (Vin) to be converted, a switch designated 11 in the Figure 4.44, this switch is controlled by a controller designated 10 in the Figure 4.44, the switch have a switching cycle period T, and a diode element designated 12 in the Figure 4.44, connected to the inductor (LX) and connected to the switch. These elements are arranged to provide an output voltage (Vout). The method comprises the steps:

1. Building-up voltage in a self-oscillating charge-pump, designated 3a in Figure 4.44, comprising an array of interconnected ring oscillators (RO_1 - RO_N). The input voltage (V_{in}) is provided at a connection node of the first ring oscillator (RO_1) and the second ring oscillator (RO_2), at the last ring oscillator (RO_N), the voltage (X_N) is the result of the accumulated built-up voltage of the self oscillating charge-pump, designated 3a in Figure. 4.44.

2. The amplifier, designated 3b in Figure. 4.44, Generate a clock signal, which is obtained based on the output of the array of ring oscillators (RO_1 - RO_N) of the self-oscillating charge-pump, designated 3a in Figure. 4.44.

3. The clock signal feed then the pulse generator, designated 3c in Figure. 4.44. The converted a pulse signal control the switch, designated 11 in Figure. 4.44.

4. When the pulse signal is high, the switch conduce, during a first period Tn to obtain a current build-up (I_L) in the inductor (L_X).

5. When the pulse signal is low, the switch open during a second period Tp. This induce a decreasing current (I_L) in the inductor (L_X). This induce to boost the voltage which is transferred through the diode element, designated 12 in Figure 4.44, to provide an output voltage (V_{out}).

6. Inactivating the DC-DC converter, designated 1 in Figure. 4.44, once the current in the inductor (L_X) is zero so that no current enters or leaves the DC-DC converter, until the end of the switching cycle period T of the switch, designated 11 in Figure. 4.44. The duty cycle d = Tn/T between the first period Tn when the switch is conducting and the period T decreases when the input voltage (V_{in}) decreases until delay reaches a saturation point, keeping the duty cycle at a constant level so that the pulse signal cannot increase further.

The original implementation of the ladder converter proposed in [324], was improved in [325] reducing overhead due to the driving circuits with the self self-oscillating charge-pump. The bottleneck in lowering the supply voltage is double, one part is the converter losses degrades with a lower input voltage. A second one is the fact that ring oscillator can not sustain oscillation, an intrinsic limit is related to the threshold voltage.

As presented in Figure 2.30. The Frequency evaluation with respect to supply voltage is ±20% accurate with respect to the simulations. The V_T contribution on the minimum supply voltage motivates the use of the DTMOS connection [323]. The clock extractor was implemented as a class A-B amplifier; since both inputs are small signal with a DC-biasing, makes the structure a natural choice.

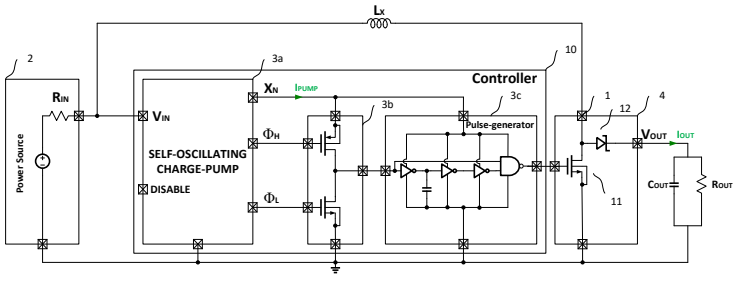


Figure 4.44: DC source Harvesting Integrated Circuit block diagram

The Figure 4.45 present Further details on the implementation of the Self-oscillating charge-pump, based on the work presented in [253] the ladder topology was found interesting in the below capacitance arrangements.

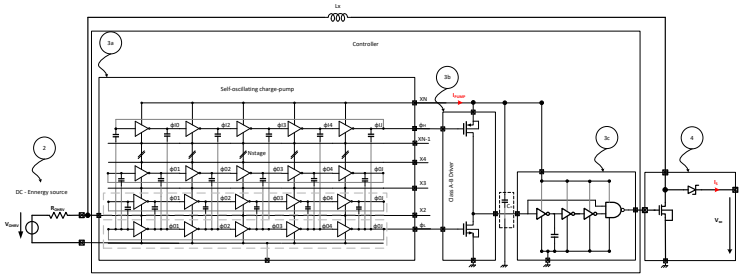


Figure 4.45: DC source Harvesting Integrated Circuit block diagram

Then a fully digital implementation of the switch was proposed based on inverter in [324] which was then proposed in the cascade of odd-stage such that the structure would self-oscillate in [325].

4.6.0.2 Measurements and discussion

The Figure 4.46 present the integrated die picture in a 180nm Process. Where the cold-start function occupies 0.418 mm^2.

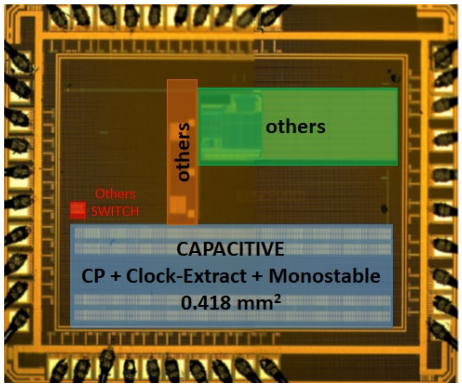


Figure 4.46: DC source Harvesting Integrated Circuit Die picture

The Figure 4.47 present the probed voltage taken from an integrated follower in the test die the yellow signal is the base ring-oscillator frequency supplied by the energy harvested (green trace) at 80mV. The function generate a 600mV DC voltage (blue) as well as a control pulse for the inductive converter (red).

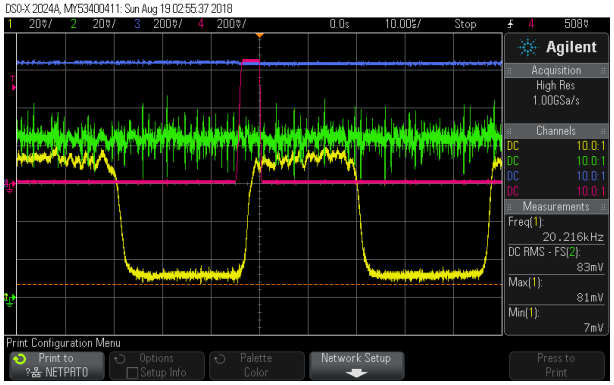


Figure 4.47: Transient verification of the base ring-oscillator frequency (yellow) under 80mV supply voltage (green) generating a dc output voltage (blue) and pulse (red) of 600mV amplitude to drive the DC-DC switch.

The Figure 4.48 present the output voltage of the self-oscillating charge-pump as a function of the temperature. The measurement proposed in the Figure 4.48 confirm the expected operation.

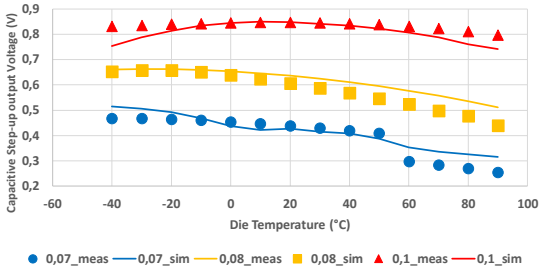


Figure 4.48: Capacitive self-oscillating charge-pump function output voltage as function of the temperature

The charge-pump is loaded by the pulse generator and maintain a voltage close to 0.5V in order to drive the boost gate. As shown in the Figure 4.49 the inductive boost output voltage as function of the temperature with an open load condition.

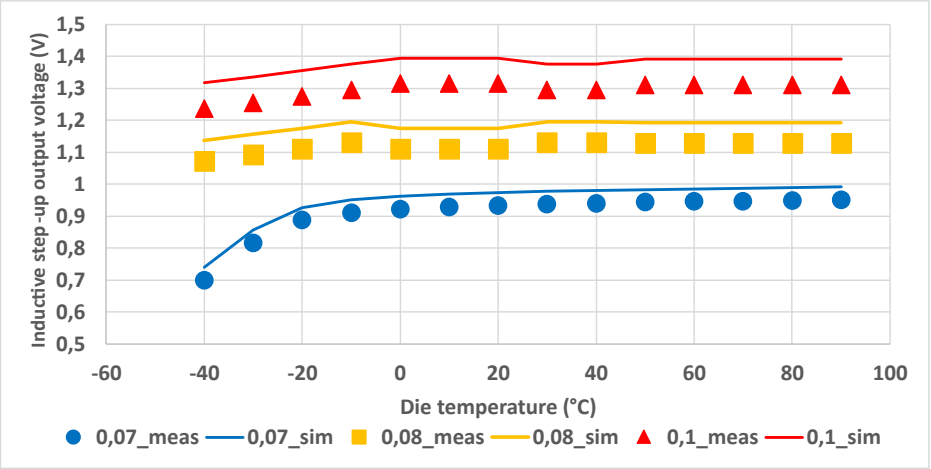


Figure 4.49: Inductive no load output voltage of the inductive start-up as function of the temperature

This results shows that despite the low voltage obtained from the capacitive boost at 70mV input and hot temperature the inductive boost ensure a functional 1V delivery. Over the load it was observed a hard decrease from 50 μA load current. Most of standard harvesting ICs would require 10 μA to start-up their own internal sustain boost converter. Thus our proposal would extend most of the available thermoelectric harvesting ICs if a companion chip interface was planned.

A benchmark with reported circuits for thermoelectric generator cold-start is proposed in the Figure 4.50.

	Hardware	Start-up	Output
Ref	Process node (nm)	Voltage (mV)	Voltage (V)
	Passives	Time (ms)	Current (µA)
Hao-Yen Tang	65 nm	50 mV	1.2 V
VLSI 2012	4 Off chip Coil	10 ms	70 µA
J. Göppert	130 nm	70 mV	1.25 V
ESSIRC 2015	Nothing off chip	1500 ms	12 µA
S. Bose	180 nm	57 mV	0.8 V
ISCAS 2018	Nothing off chip	135 ms	0.005 µA
This Work	**180 nm**	**60 mV**	**1.2 V**
	1 Off chip Pwr Coil	**150 ms**	**20 µA**

Figure 4.50: Benchmark of the reported thermoelectric generator cold-start circuits

The proposed techniques shows 3mV higher start-up voltage, slower performances but a way higher output current, which is mandatory to comply the need of extended range cold-start function.

The Figure 4.51 present a demonstration board including a thermoelectric generator, the circuit for energy harvesting and some circuits to drive a thin LCD screen, where a test pattern will be blinked.

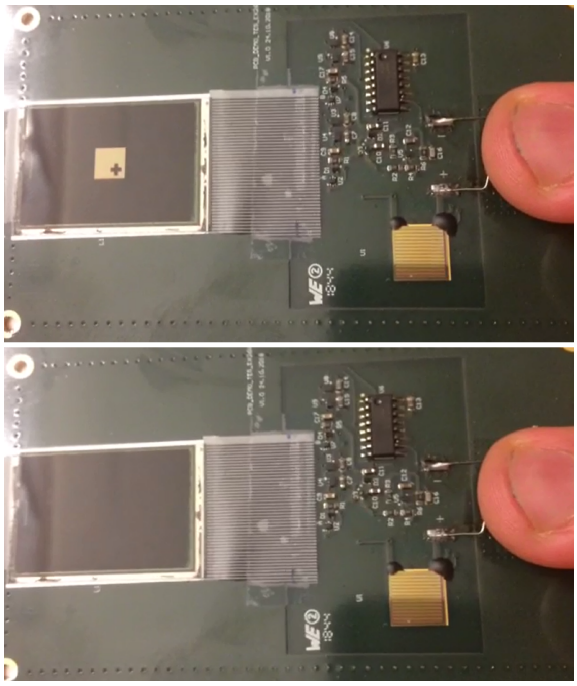


Figure 4.51: Operating demonstration

The LCD could be modeled by a 400pF capacitance and it's driver as a $2M\Omega$ restive load that must be supplied under 1V, thus consume $500\,nA$. We had proposed to use 81 cells of the capacitive charge-pump which provide 7nA each in order to supply such load and proves our cell to be capable to run an application.

Conclusion

5.1 Results

Millimeter-scale wireless sensors not only bring new applications in many applications such as wearable and infrastructure sensors or human machine interfaces, but also add performance-enhancing intelligence to old, expensive, and difficult to replace infrastructures. The main goal of this research was to find suitable frequencies generation architecture, design and implement of ultra-low-power and low voltage oscillator and frequency synthesizers including power management extending the state of the art solutions for applications such as timekeeping, communication protocol clocking, and power conversion. These emerging IoT platforms tend to incorporate energy source, energy storage, sensing and communication into a miniaturized system. Miniature size, autonomous operation, low manufacturing cost and efficient wireless communication are the challenging specifications that should be met for wide spread of these miniature sensors. Harvesting ambient energy for powering up durable and long-life wireless motes is a very hot topic today.

However, as harvested energy is intermittent and highly depends on the environmental conditions, an energy storage device such as a rechargeable battery should be used for reliable operation of electronic circuits. In addition, as the energy provided by the energy harvesting source should be able to supply the set of electronics functions, the power budget of those functions is therefore the most important design factor in realization of autonomous motes. The basic components of such a system are quite well known, starting from harvesting energy from environment, charging a rechargeable battery using harvested energy and powering up the electronic circuit for energy management, sensing and communication. The main focus of this manuscript is realization of frequency references. In this thesis, it was shown that IoT is a broad application field where the clocking plays a key role and particularly foster the need for energy efficient circuits.

In this thesis we have proposed a structured design approach as an efficient way to design and optimize a wide range of analog circuits. It is shown that each circuit can be partitioned into basic analog structures, whose sizing in the circuit environment demands less effort. At the same time, the level of the basic analog structures is the only abstraction level where the design trade-offs can be found and where it can be confirmed whether the design parameters

can be improved or have to be relaxed. The proposed procedural analog design scenarios consist in

1. Circuit partitioning, derivation of the building blocks and specifications for predefined procedural design sequence.
2. The basic analog structures are designed in transconductance-load-bias structure order since it allows the correct propagation of the design specifications, the determination and verification of parameters' bounds, as well as the local optimization loops.
3. In the cases where certain specifications cannot be achieved because of the technology limits or the necessary design trade-offs, topology variants are proposed as an elegant solution.
4. It consists in replacing the basic analog structure that affects the design parameter in question by its topology variant modified in such a way to improve the required performance.

The work had particularly emphases the use of self-biased structure due to their robustness, when a single operating point is desired which is the case of CMOS references. In this thesis we have proposed various CMOS reference block that provide either current, voltage or frequency in an efficient manner.

5.2 Outlook

Size of a sensor is typically limited by battery, antenna and energy harvesting source. Millimeter-scale sensors are now feasible thanks to major breakthroughs in developing energy harvesting sources, energy storage devices, wireless transceivers, sensing platform and last but not least, Circuit design innovations [38, 133, 251]. Nowadays, energy-efficient circuits have made it feasible to realize fully functional sensors that consume only a few hundreds of nA, yet energy harvesting face the industrial cost effectiveness challenge with respect to primary cells.

In the domain of frequency generation with the obtained results one could think of :

1. Improved absolute accuracy of Resistor locked loop for silicon based frequency reference.
2. Self-oscillating relaxation resonator based oscillator with low jitter
3. Sub 0.5V Time based signal processing.
4. Generating the communication carrier directly from the frequency reference. A report of 2018 [326] had shown some feasibility in the context of Bluetooth low-energy.
5. Flexible Frequency generation.
6. High density resistor with high stability over the temperature and bias conditions.

The thermoelectric energy harvesting on its sides seems more limited by the volume of Bi2Te3 available for the production of such modules in high volume. Some research on the chemical, flexible replacements could potentially bring new challenge into that domain.

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Research Submissions

Patents

[1] **M. Coustans**, M. Dellea, and L. Plavec, "Cellule elementaire et pompes de charges comprenant une telle cellule elementaire" EP 18 17 57 44 – Submitted to EPO June 04, 2018

[2] **M. Coustans**, L. Rossi, and Y. Godat, "A dc-dc converter for a low voltage power source" EP 18 20 60 16 – Submitted to EPO November 13, 2018

Journal Papers

[3] **M. Coustans**, F. Krummenacher, and M. Kayal "A survey of fully integrated frequency references" Preprint submitted to Microelectronics Journal December 28, 2018

Research Publications

Patents

[1] **M. Coustans**, L. Rossi, and Y. Godat, "Self-polarized quartz oscillator circuit" US2018342982 (A1), EP3407486 (A1), JP2018198423 (A), KR20180128843 (A).

Books

[2] **M. Coustans** and C. Dehollain, Power management for Internet of Things, Tutorials in Circuits and Systems. River Publishers, 2018.

Journal Papers

[3] **M. Coustans**, F. Krummenacher, C. Terrier, and M. Kayal, "A 400 fJ Per-Cycle Frequency Reference for Internet of Things," IInternational Journal of Microelectronics and Computer Science, vol. 7, pp. 8–13, 2016.

Conference Papers

[4] **M. Coustans**, F. Krummenacher, M. Kayal, and C. Terrier, "A nA crystal - Less oscillator for internet of things," in Proceedings of the 23rd International Conference Mixed Design of Integrated Circuits and Systems, MIXDES 2016, 2016, pp. 136–139.

[5] M. Bucher, **M. Coustans**, et al., "Variability of Low Frequency Noise and mismatch in enclosed-gate and standard nMOSFETs," in 2017 International Conference of Microelectronic Test Structures (ICMTS), 2017, pp. 1–4.

[6] **M. Coustans,** M. Bucher, et al., "Variability of Low Frequency Noise and mismatch in CORNER DOPED and standard CMOS technology," in 2017 International Conference on Noise and Fluctuations (ICNF), 2017, pp. 1–4.

[7] **M. Coustans,** D. Gauthey, S. Rota, A. Acovic, P. Habas, and R. Meyer, "Hump-effect impact on subthreshold VLSI circuit," in 2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2017, pp. 1–3.

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[9] **M. Coustans,** C. Terrier, T. Eberhardt, S. Salgado, A. Cherkaoui, and L. Fesquet, "Subthreshold logic for low-area and energy efficient true random number generator," in 2018 IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS), 2018, pp. 1–3.

[10] **M. Coustans,** F. Krummenacher, L. Rossi, M. Dellea, Y. Godat, Y. Sierro, S. DallaPiazza, and M. Kayal, "A 32kHz Crystal Oscillator Leveraging Voltage Scaling in an Ultra-Low Power 40nA Real-Time Clock," in 2018 31st IEEE International System-on-Chip Conference (SOCC), 2018, vol. 1, no. c, pp. 308–313.