Characterization and Modeling of Gigarad-TID-induced Drain Leakage Current of 28-nm Bulk MOSFETs

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***Abstract*—This paper characterizes and models the effects of total ionizing dose (TID) up to 1 Grad(SiO_2) on the drain leakage current of *n*MOSFETs fabricated with a commercial 28-nm bulk CMOS process. Experimental comparisons among individual *n*MOSFETs of various sizes provide insight into the TID-induced lateral parasitic devices, which contribute the most to the significant increase up to four orders of magnitude in the drain leakage current. We introduce a semi-empirical physics-based approach using only three parameters to model the parallel parasitic and total drain leakage current as a function of TID. Taking into account the gate independence of the drain leakage current at high TID levels, we model the lateral parasitic device as a gateless charge-controlled device by using the simplified charge-based EKV MOSFET model. This approach enables us to extract the equivalent density of trapped charges related to the shallow trench isolation oxides. The adopted simplified EKV MOSFET model indicates the weak inversion operation of the lateral parasitic devices.**

***Index Terms*—Charge-controlled, drain leakage current, gateless, parasitic leakage current, parasitic device, physics-based modeling, shallow trench isolation, STI, total ionizing dose, TID, trapped charges, 28-nm bulk MOSFETs, weak inversion**

I. Introduction

THE forthcoming high-luminosity Large Hadron Collider (HL-LHC) at CERN is anticipated to experience an unprecedented radiation level up to 1 Grad(SiO_2) of total ionizing dose (TID) and $10^{16}\mathrm{neutrons/cm^2}$ of hadron fluence over ten years of operation [1]. To ensure long-term reliable performance, the HL-LHC will require highly improved tracking systems with higher bandwidth and more radiation-tolerant front-end (FE) electronics [2], [3]. The aggressive downscaling of CMOS technologies brings a higher operation speed and an extended circuit functionality [4], [5]. Moreover, the introduced ultrascaled gate oxides suppress the relevant TID-induced charge buildup and reduce the susceptibility to TID effects [**?**], [6]. However, at ultrahigh TID levels, effects on parasitic oxides, such as shallow trench isolation (STI) oxides and spacer oxides, often dominate the radiation response of nanoscale CMOS technologies [7], [8]. With the perspective of using ultrascaled CMOS technologies in future radiation-tolerant tracking systems, we have been characterizing the radiation tolerance of a commercial 28-nm bulk CMOS process up to 1 Grad(SiO_2) of TID [9], [10] and modeling the observed effects for supporting radiation-tolerant circuit designs [11]. Static measurements on our 28-nm bulk MOSFETs demonstrate an improved radiation tolerance at the switched-on region, whereas

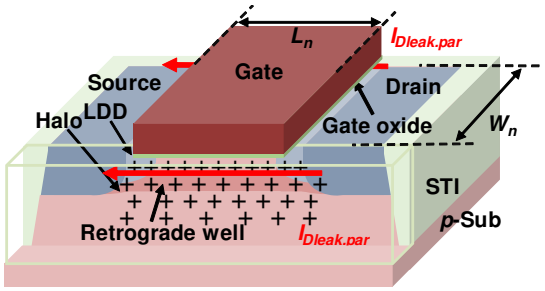

Fig. 1. Three-dimensional schematic illustration of an irradiated *n*MOSFET illustrating the formation of two lateral parasitic devices. The main *n*MOSFET is surrounded by the shallow-trench isolation (STI) structure, as shown in light green. The front face of the STI structure is represented by the light-green frame to make the channel doping profile and the STI-related trapped-charge distribution (+ markers) visible.

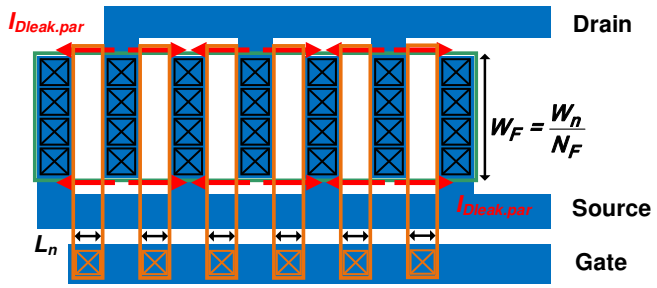

Fig. 2. Layout of an irradiated multi-finger *n*MOSFET illustrating the scaling property of the total parallel parasitic drain-to-source leakage current with two times the number of fingers. The total width of the multi-finger *n*MOSFET W_n is the width per finger W_F times the number of fingers N_F.

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most of the irradiated *n*-type MOSFETs undergo a significant increase in the drain leakage current [9], [10]. To characterize these effects, we have introduced the simplified charge-based EKV MOSFET model in [11] to describe the large- and small-signal characteristics. We are currently developing physics-based models of TID effects on bulk MOSFETs that can ultimately be implemented into the BSIM6 compact model for the design of radiation-tolerant circuits. Among all the various effects of TID on bulk MOSFETs, the significant increase of the drain leakage current observed for *n*-type MOSFETs is certainly the most important to model. Most of the other effects such as threshold voltage shift can be compensated by proper circuit biasing techniques. This work therefore focuses on modeling the TID-induced drain leakage current by means of a gateless charge-controlled model similar to the simplified charge-based EKV MOSFET model.

The significant increase in the drain leakage current is mainly attributed to the radiation-induced charge trapping in relatively thick STI oxides. For an *n*MOSFET, trapped holes in STI oxides can invert the *p*-type substrate along the STI sidewalls and open two parallel parasitic leakage paths [12]–[15]. This allows two parallel leakage components to flow from drain to source, even when the main *n*MOSFET is switched off, as shown in Fig. 1. The situation becomes even worse for a multi-finger *n*MOSFET because the total parasitic drain-to-source leakage current scales with the number of fingers [16], as shown in Fig. 2. This radiation-induced leakage current questions the main advantage of nanoscale CMOS technologies—i.e., low power consumption [17]. In contrast, for a *p*MOSFET, trapped holes in STI oxides tend to accumulate electrons at the surface of the *n*-type substrate and prevent the formation of *p*-type channels. Therefore, the drain leakage current of the irradiated *p*MOSFETs is not an issue, as shown in [10].

This paper characterizes and models in detail the effects of TID up to 1 Grad(SiO_2) on the drain leakage current of *n*MOSFETs. To our knowledge, no publication has been devoted from the perspective of both experiment and modelling to the impact of such high TID levels on the drain leakage current of this commercial 28-nm bulk CMOS process. We propose a semi-empirical physics-based approach with only three parameters to model the parallel parasitic and total drain leakage current as a function of TID. The lateral parasitic device has been investigated using TCAD device simulations [18]–[20], compact models [21], or a combination of these two approaches [15], [22]. However, these models involve complex device structures and intensive analytical computations. We aim at a simpler approach for evaluating the TID-induced drain leakage current. Taking into account the gate independence of the drain leakage current at high TID levels, we propose modelling the lateral parasitic device as a gateless charge-controlled device by using the simplified charge-based EKV MOSFET model.

II. Experimental details

Test chips with a matrix of individual MOSFETs were fabricated with a commercial 28-nm bulk CMOS technology, which allows the width per finger W_F from 100 nm to 3 µm and the length L_n from 30 nm to 1 µm. We explore standard single-finger and multi-finger *n*MOSFETs of various sizes for identifying the dominant components of drain leakage current at different TID levels and the favorable device geometry for radiation-tolerant applications. Each chip has only one transistor of each size. However, a brief comparison of the same size of transistors on different chips demonstrates the repeatability of our measurement results. Enclosed-layout transistors are often used for isolating the effects of TID on STI oxides [7], [8]. However, the strict design rules of this commercial 28-nm bulk CMOS process exclude such special structures.

Chips were irradiated at CERN's in-house 10-keV X-ray irradiation system (Seifert RP149) at room temperature (300 K). Reference [7] shows that the conducting bias condition $V_{GB} = V_{DS} = V_{DD}$ is the real worst-bias case for commercial 65-nm bulk *n*MOSFETs from the same foundry, where V_{GB} is the gate-to-bulk voltage, V_{DS} is the drain-to-source voltage, and V_{DD} is the nominal voltage supply. This is different from the historical worst-bias case—i.e., the switched-on bias condition $V_{GB} = V_{DD}$ and $V_{DS} = 0$ [23]. Nevertheless, these two bias conditions induce no big difference in the drain leakage current of our 28-nm bulk MOSFETs [24]. Moreover, in most analog circuits and particularly the analog FE electronics, MOSFETs are biased in saturation with a nonzero V_{DS} except the switches working at a zero V_{DS}. To reproduce as closely as possible the realistic bias condition, we used the conducting bias condition.

Single-finger and multi-finger *n*MOSFETs were irradiated up to 1 Grad(SiO_2) with steps of 0, 0.5, 1, 5, 10, 50, 100, 200, 400, 600, 800, and 1000 Mrad at a dose rate of 8.82 Mrad/h(SiO_2) and 10 Mrad/h(SiO_2), respectively. These two dose rates are quite similar and make no big difference in terms of TID effects on our 28-nm bulk MOSFETs. Immediately after each TID step, static measurements were performed with the Keithley 4200-SCS Parameter Analyzer. As oxide-trapped charges anneal with time [25], we chose a voltage step of 25 mV as a suitable compromise between limiting the measurement duration and providing a sufficient measurement resolution. Reference [10] shows the relatively slow oxide-trapped charge annealing at room temperature for our 28-nm bulk MOSFETs. This allows us to neglect the annealing effects that happened during less than one hour of measurements. More measurement details can be found in [9], [10].

III. Characterization of the drain leakage current

Fig. 3 plots the drain current I_D of single-finger (a-c) and multi-finger (d-f) *n*MOSFETs measured in saturation ($V_{DS} = 1.1$ V) versus the overdrive voltage $V_{GB} - V_{T0}$ with respect to TID up to 1 Grad(SiO_2), where the threshold voltage V_{T0} is extracted as the intercept of the linear extrapolation at the maximum slope of $\sqrt{I_D}$-V_{GB} curves at the V_{GB} axis. Both single-finger and multi-finger *n*MOSFETs demonstrate a substantial increase in the drain leakage current.

Furthermore, the drain leakage current of single-finger *n*MOSFETs presents a width independence and a length dependence. At high TID levels, single-finger *n*MOSFETs of the same length ($L_n = 1$ µm), as shown in Fig. 3a and Fig. 3b,

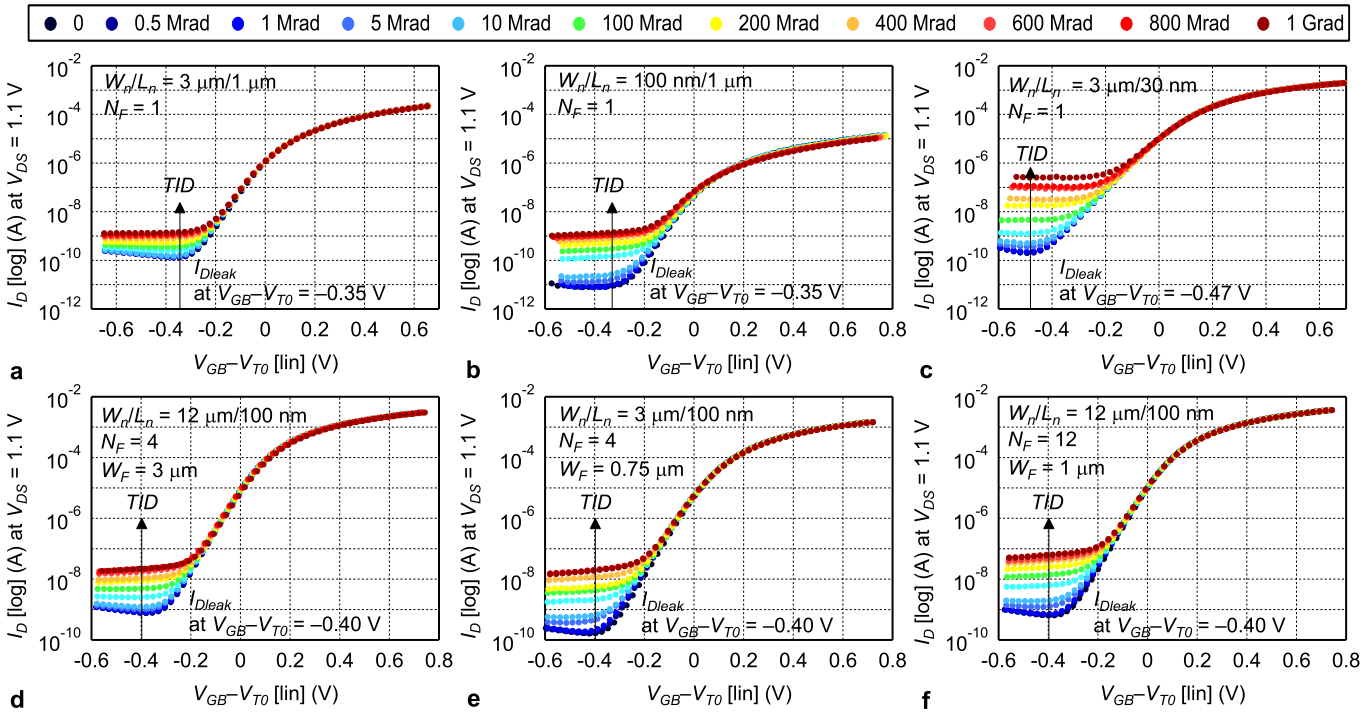


Fig. 3. Drain current I_D of single-finger (a-c) and multi-finger (d-f) nMOSFETs measured in saturation ($V_{DS} = 1.1$ V) versus overdrive voltage $V_{GB} - V_{T0}$ with respect to the total ionizing dose TID. V_{T0} is the threshold voltage extracted as the intercept of the linear extrapolation at the maximum slope of $\sqrt{I_D}$-V_{GB} curves at the V_{GB} axis. The vertical arrow lines point out the location where the drain leakage current I_{Dleak} is extracted.

exhibit a close amount of drain leakage current. However, those of the same width ($W_n = 3\,\mu$m) but different lengths, as shown in Fig. 3a and Fig. 3c, display different values of drain leakage current. This width independence and length dependence jointly indicate the dominant contribution of the lateral parasitic devices.

In addition to the gate length dependence, the drain leakage current is also proportional to the number of fingers. At high TID levels, multi-finger nMOSFETs of the same gate length and the same number of fingers ($L_n = 100$ nm and $N_F = 4$), as shown in Fig. 3d and Fig. 3e, present almost the same amount of drain leakage current. However, those of the same device geometry ($W_n/L_n = 12\,\mu\text{m}/100\,\text{nm}$), as shown in Fig. 3d and Fig. 3f, have the drain leakage current proportional to the number of fingers. This scalability with the number of fingers confirms the primary contribution of the lateral parasitic devices.

Even though the increase in the drain leakage current slows down at relatively high TID levels, we do not see the rebound effects of interface-trapped charges [12]. For the tested 28-nm bulk nMOSFETs, trapped holes in STI oxides therefore play a more important role than charges trapped at silicon/STI interfaces.

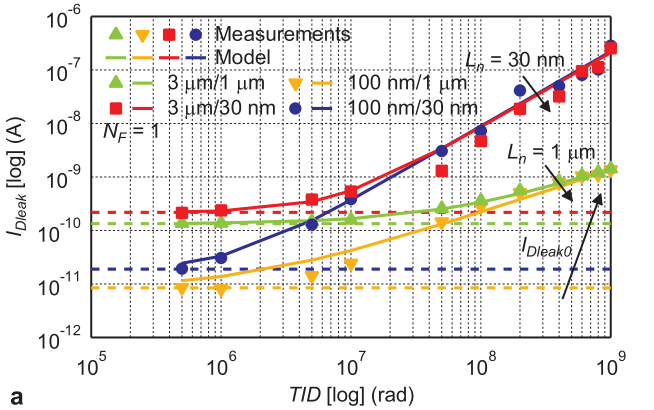
IV. Modeling of the Drain Leakage Current

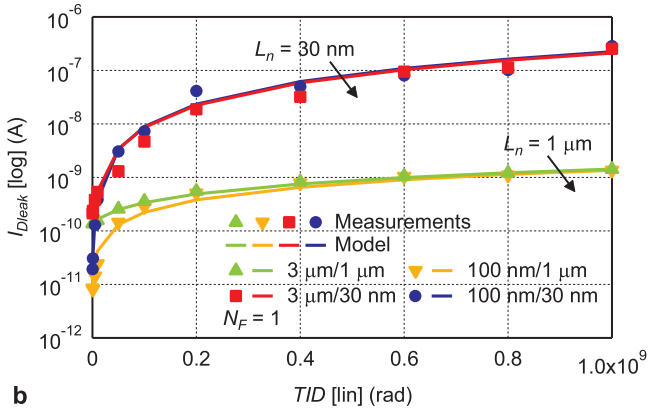
This work mainly studies single-finger nMOSFETs at the four corners of the W_n versus L_n plot, the multi-finger nMOSFET with $W_n = 3\,\mu$m and $N_F = 4$, and those with $W_n = 12\,\mu$m and N_F =4, 6, 8, and 12. The total drain leakage current I_{Dleak} is extracted at a constant $V_{GB} - V_{T0}$ from the transfer characteristics. Fig. 4a and Fig. 5a plot the extracted I_{Dleak} of single-finger and multi-finger nMOSFETs as closed markers, respectively. The tested nMOSFETs of the same gate length and the same number of fingers exhibit a close amount of I_{Dleak}. This confirms the width independence, the length dependence, and the dependence on the number of fingers, demonstrating the main contribution of the lateral parasitic devices. The log-lin plots with closed markers in Fig. 4b and Fig. 5b show that the significant increase in I_{Dleak} mostly happens before 200 Mrad of TID. Afterwards, the increase tends to slow down. This might be due to the saturation effect of STI-related trapped charges [26].

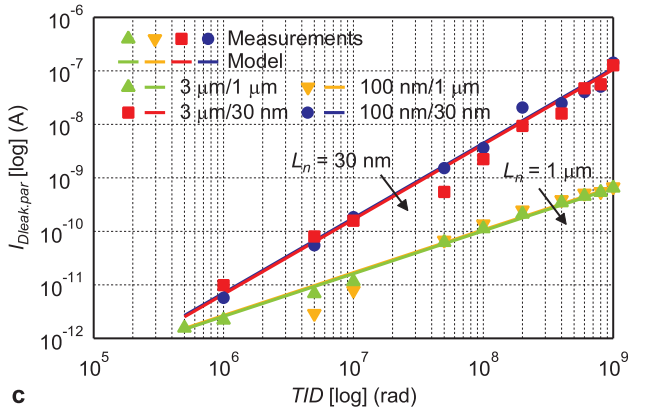
I_{Dleak} comes from the main nMOSFET ($I_{Dleak.main}$) and the lateral parasitic devices ($2N_F I_{Dleak.par}$):

$$I_{Dleak} = I_{Dleak.main} + 2N_F I_{Dleak.par}. \quad (1)$$

The drain leakage current of the main nMOSFET $I_{Dleak.main}$ is mainly composed of the drain-to-gate tunneling current, the gate-induced drain leakage current, and the subthreshold current [27]. These leakage components are as a function of the threshold voltage V_{T0}, which is among the most TID-sensitive device parameters. Plotting I_D versus $V_{GB} - V_{T0}$ isolates the effects of the TID-induced V_{T0} shift. I_{Dleak} extracted at a constant $V_{GB} - V_{T0}$ with respect to TID therefore has almost the same contribution from the main nMOSFET. In addition, the substantial increase in I_{Dleak} is mostly the contribution of the lateral devices, which allows us to assume a constant $I_{Dleak.main}$, as confirmed by the plateau at low TID levels ($<\sim$1 Mrad) in Fig. 4a and Fig. 5a. Prior to irradiation, neither the oxide-trapped charge density from the semiconductor processing nor







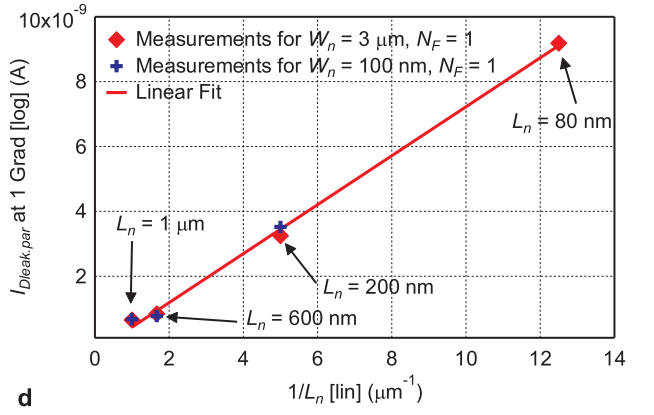
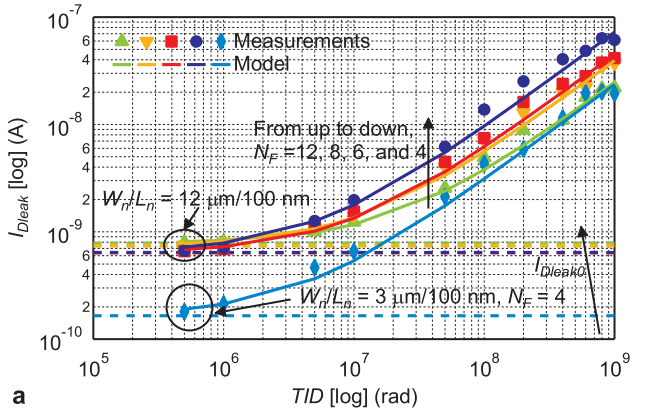
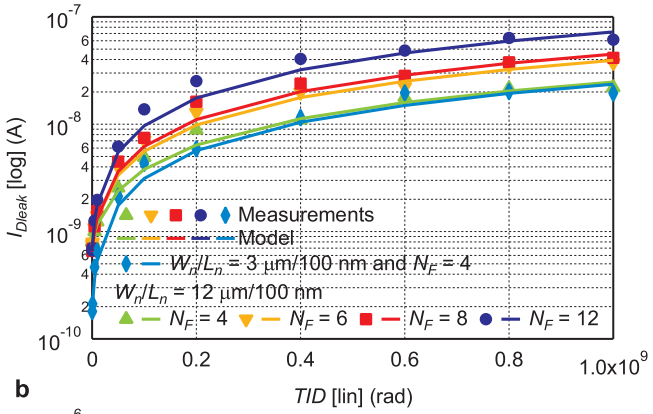
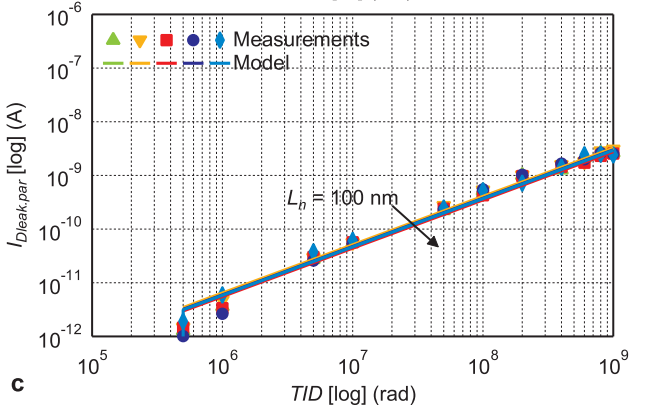


Fig. 4. Model validation of the total drain leakage current I_{Dleak} of single-finger *n*MOSFETs in log-log scale (a) and log-lin scale (b) versus the total ionizing dose *TID*; (c) model validation of the average parasitic drain-to-source leakage current $I_{Dleak.par}$ versus *TID*; (d) average parasitic drain-to-source leakage current at 1 Grad of TID versus L_n.







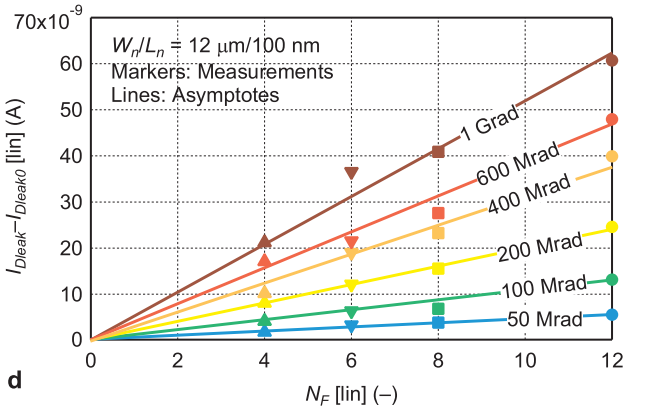


Fig. 5. Model validation of the total drain leakage current I_{Dleak} of multi-finger *n*MOSFETs in log-log scale (a) and log-lin scale (b) versus the total ionizing dose *TID*; (c) model validation of the average parasitic drain-to-source leakage current $I_{Dleak.par}$ versus *TID*; (d) total parasitic leakage current $I_{Dleak} - I_{Dleak0}$ of multi-finger *n*MOSFETs of the same size versus the number of fingers N_F.

TABLE I
MODEL PARAMETERS FOR THE DRAIN-TO-SOURCE LEAKAGE CURRENT

W_n/L_n	N_F	I_{Dleak0} (A)	k	TID_{crit} (Mrad)
3 µm/1 µm	1	1.34×10^{-10}	0.8	58.6
100 nm/1 µm	1	8.47×10^{-12}	0.8	1.78
3 µm/30 nm	1	2.17×10^{-10}	1.4	7.35
100 nm/30 nm	1	1.90×10^{-11}	1.4	1.24
3 µm/100 nm	4	1.65×10^{-10}	0.9	4.10
12 µm/100 nm	4	7.84×10^{-10}	0.9	22.4
12 µm/100 nm	6	7.37×10^{-10}	0.9	12.3
12 µm/100 nm	8	6.37×10^{-10}	0.9	8.95
12 µm/100 nm	12	6.42×10^{-10}	0.9	5.29

the fringing field from the gate bias is high enough to induce the parasitic leakage paths in parallel with the main channel or a total parasitic drain-to-source leakage current comparable to $I_{Dleak.main}$ [28]. This allows us to neglect the parallel parasitic drain-to-source leakage current before irradiation.

Therefore, the pre-irradiation drain leakage current I_{Dleak0}, as plotted by dashed lines in Fig. 4a and Fig. 5a, measures $I_{Dleak.main}$. Solving (1) gives the average parasitic drain-to-source leakage current $I_{Dleak.par}$:

$$I_{Dleak.par} = \frac{I_{Dleak} - I_{Dleak0}}{2N_F}. \tag{2}$$

Closed markers in Fig. 4c and Fig. 5c exhibit a significant increase in $I_{Dleak.par}$. Moreover, the lateral parasitic devices in parallel with the main *n*MOSFETs of the same gate length have almost the same contribution to I_{Dleak}. $I_{Dleak.par}$ of long-channel parasitic devices is actually linearly dependent on $1/L_n$, as shown in Fig. 4d. The shortest gate length $L_n = 30\,\mathrm{nm}$ falls beyond the linear fit due to short-channel effects. The linearity in Fig. 5d evidences the scaling property of the total parasitic drain-to-source leakage current with the number of fingers.

Considering the constant $I_{Dleak.main}$ at all TID steps and the linear relation between I_{Dleak} and TID in log-log scale at high TID levels, as shown in Fig. 4a and Fig. 5a, we propose a simple semi-empirical physics-based model for the total drain leakage current I_{Dleak}:

$$I_{Dleak} = I_{Dleak0}\left[1 + \left(\frac{TID}{TID_{crit}}\right)^k\right], \tag{3}$$

where TID_{crit} is the critical total dose at which the lateral parasitic devices contribute the same amount of current as the main *n*MOSFET and k is the slope of the log-log plot at relatively high TID levels calculated by $(\log_{10} I_{Dleak2.par} - \log_{10} I_{Dleak1.par})/(\log_{10} TID_2 - \log_{10} TID_1)$ with two sets of data $I_{Dleak1.par}(TID_1)$ and $I_{Dleak2.par}(TID_2)$. Solving (2) and (3) produces the model for the parallel parasitic drain-to-source leakage current $I_{Dleak.par}$:

$$I_{Dleak.par} = \frac{I_{Dleak0}}{2N_F}\left(\frac{TID}{TID_{crit}}\right)^k. \tag{4}$$

Fitting (3) with measurement results determines the values of TID_{crit} and k. Together with I_{Dleak0}, model parameters are listed in Table I. The power k is the same for *n*MOSFETs of the same length, whereas the pre-irradiation drain leakage

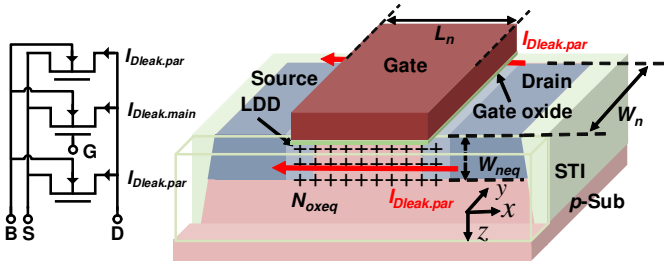


Fig. 6. Equivalent circuit of an irradiated *n*MOSFET with two gate-independent lateral parasitic devices (left) and three-dimensional schematic illustration of the irradiated *n*MOSFET with two parallel parasitic leakage paths formed by uniformly distributed trapped charges related to shallow trench isolation (STI) oxides (right).

current I_{Dleak0} and the critical total dose TID_{crit} depend on the device geometry and the number of fingers. Model results are plotted as solid lines in Fig. 4 and Fig. 5. Using only three parameters, the proposed semi-empirical physics-based model demonstrates good agreement with measurement results. This efficiency makes it a practical method of evaluating the parallel parasitic and total drain leakage current with respect to TID. TID_{crit} indicates the TID level, above which the lateral parasitic devices contribute the most to the total drain leakage current I_{Dleak}. Recent measurements show the independence of the parallel parasitic drain-to-source leakage current $I_{Dleak.par}$ on the applied V_{DS} during irradiation. This demonstrates the promising use of this model in accurately predicting the drain leakage current of *n*MOSFETs working across the whole range of V_{DS} from zero to V_{DD}. By extracting the corresponding values of three model parameters, we can apply this model easily to alternative CMOS technologies.

V. MODELING THE LATERAL PARASITIC DEVICE AS A GATELESS CHARGE-CONTROLLED DEVICE

A. Equivalent structure for the lateral parasitic device

At high TID levels, the drain current at low values of overdrive voltage is independent of the gate bias, as shown in Fig. 3. This weak or negligible gate control is one distinctive feature of the lateral parasitic device. It is the STI-related trapped charges that modify the surface potential of the edge channel and control the mobile charge density of the lateral parasitic device. This motivates us to model the lateral parasitic device as a gateless charge-controlled device, as shown by the equivalent circuit in Fig. 6. Since this lateral parasitic device has no gate control and is fully controlled by STI-related trapped charges, we name it as *n*-*Q*FET.

The applied bias and the dynamic charge movement during irradiation make the electrical condition inside the device complex. This results in a non-uniform charge buildup related to STI oxides [18], [19]. Moreover, the complex channel doping engineering has been widely used in modern CMOS technologies, including the retrograde well for preventing the latch-up effect, the threshold voltage adjustment by ion implant at the surface, the lightly-doped drain (LDD) for suppressing the hot carrier degradation, and the halo implant for inhibiting the punchthrough effect [29]. This leads to a non-uniform doping profile [15], [18], as illustrated in Fig. 1. Both aspects

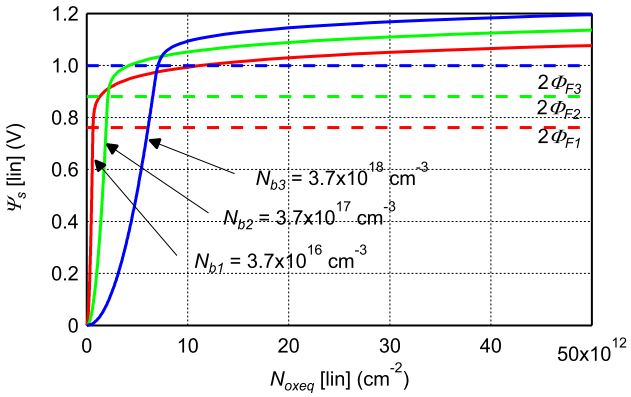


Fig. 7. Surface potential Ψ_s versus the equivalent density of STI-related trapped charges per unit area N_{oxeq}.

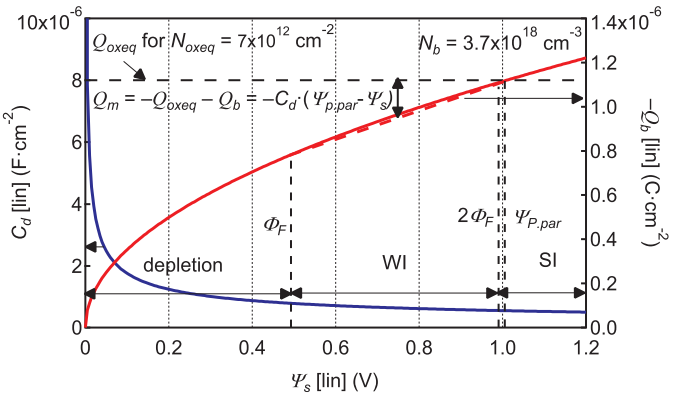


Fig. 8. Linearization of the mobile charge density Q_m with respect to the surface potential Ψ_s.

influence the electrical characteristics of the lateral parasitic *n*-*Q*FET.

To simplify the modeling task, we introduce an equivalent structure for the lateral parasitic *n*-*Q*FET, as illustrated in Fig. 6. It has a uniform channel doping concentration (N_b) that is the same as the main channel. It also has an equivalent STI-related trapped-charge density $Q_{oxeq} = qN_{oxeq}$ that models the complex charge distribution:

$$Q_{oxeq} = \frac{\int_0^{W_{n.par}} \int_0^{L_{n.par}} Q_{ox}(x,y)dxdy}{W_{neq}L_{neq}}, \tag{5}$$

where $Q_{ox}(x,y)$ is the local STI-related trapped-charge density, $W_{n.par}$ is the local width, $L_{n.par}$ is the local length, W_{neq} is the equivalent channel width, and L_{neq} is the equivalent channel length. The equivalent STI-related trapped-charge density Q_{oxeq} is uniform over a certain width W_{neq} and a certain length L_{neq}. $I_{Dleak.par}$ is assumed above the bottom of source and drain extensions. It is then straightforward to assume L_{neq} equal to the gate length of the main channel L_n and W_{neq} equal to the junction depth of source and drain extensions X_j, where L_n and X_j are two known parameters.

B. Utilization of the simplified EKV MOSFET model

The simplified EKV MOSFET model is able to fully describe large- and small-signal characteristics over a wide range of bias from weak via moderate to strong inversion with only four parameters—i.e., the slope factor n, the specific current I_{spec}, the velocity saturation parameter λ_c, and the threshold voltage V_{T0}. References [11], [30], [31] have verified the applicability of this model for this commercial 28-nm bulk CMOS process. Since the gateless charge-controlled concept involves no gate voltage or gate oxide capacitance, we need to modify the simplified EKV MOSFET model for the lateral parasitic *n*-*Q*FET.

Solving the Gauss's law and the Poisson's equation gives the relation between the local silicon charge density Q_{si} and the surface potential Ψ_s:

$$Q_{si} = -\Gamma_{b.par}\sqrt{U_T}\sqrt{\exp\frac{-2\Phi_F - V_{ch}}{U_T}\left(\exp\frac{\Psi_s}{U_T} - 1\right) + \frac{\Psi_s}{U_T}}, \tag{6}$$

where $\Gamma_{b.par} = \sqrt{2q\epsilon_{si}N_b}$ is defined as the substrate modulation factor, q is the elementary charge, ϵ_{si} is the silicon permittivity, $U_T = kT/q$ is the thermal voltage, k is the Boltzmann constant, T is the temperature, $\Phi_F = U_T \ln(N_b/n_i)$ is the Fermi potential, n_i is the intrinsic carrier concentration, V_{ch} is the channel voltage equal to V_S at source and V_D at drain, and V_S and V_D are the source and drain voltages, respectively. Note that in [32], the substrate modulation factor is defined as $\Gamma_b = \sqrt{2q\epsilon_{si}N_b}/C_{ox}$ that links $\Gamma_{b.par}$ by $\Gamma_{b.par} = \Gamma_b C_{ox}$, where C_{ox} is the gate oxide capacitance.

The charge neutrality condition provides the key bridge between STI-related trapped-charge density and total silicon charge density:

$$Q_{oxeq} = -Q_{si}. \tag{7}$$

Solving (6) and (7) gives the link between Q_{oxeq} and Ψ_s. Fig. 7 shows that for a higher channel doping concentration, a higher STI-related trapped-charge density is needed to switch on the lateral parasitic *n*-*Q*FET. Since $N_b = 3.7 \times 10^{18}\text{cm}^{-3}$ and $\Phi_F = 0.5\,\text{V}$ for our 28-nm bulk *n*MOSFETs, N_{oxeq} needs to be higher than $4.94 \times 10^{12}\text{cm}^{-2}$ to bias the lateral parasitic *n*-*Q*FET in weak inversion ($\Phi_F < \Psi_s < 2\Phi_F$) and $7.06 \times 10^{12}\text{cm}^{-2}$ in strong inversion ($\Psi_s \geq 2\Phi_F$). Therefore, we expect that advanced bulk CMOS technologies, which have a higher channel doping concentration, can withstand a much higher TID before having enough STI-related trapped charges to switch on the lateral parasitic *n*-*Q*FET.

The charge-sheet approximation gives the expression of depletion charge density $Q_b = -\Gamma_{b.par}\sqrt{\Psi_s}$. The differentiation of Q_b versus Ψ_s gives the depletion capacitance $C_d = \Gamma_{b.par}/(2\sqrt{\Psi_s})$. As shown in Fig. 8, C_d slightly depends on Ψ_s in inversion operation. This enables us to linearize the depletion charge density Q_b, as shown by the approximated red dashed line in Fig. 8. The length of the vertical double-arrowheaded line in Fig. 8 represents the mobile charge density $Q_m = -Q_{oxeq} - Q_b$ that can be linearized in inversion region as

$$Q_m = -C_d(\Psi_{P.par} - \Psi_s), \tag{8}$$

where $\Psi_{P.par}$ is the pinch-off potential. Once Ψ_s reaches $\Psi_{P.par}$, Q_m becomes 0 and Q_b equals to $-Q_{oxeq}$, which gives the expression of $\Psi_{P.par}$: $\Psi_{P.par} = Q_{oxeq}^2/\Gamma_{b.par}^2$. Note that in [32],

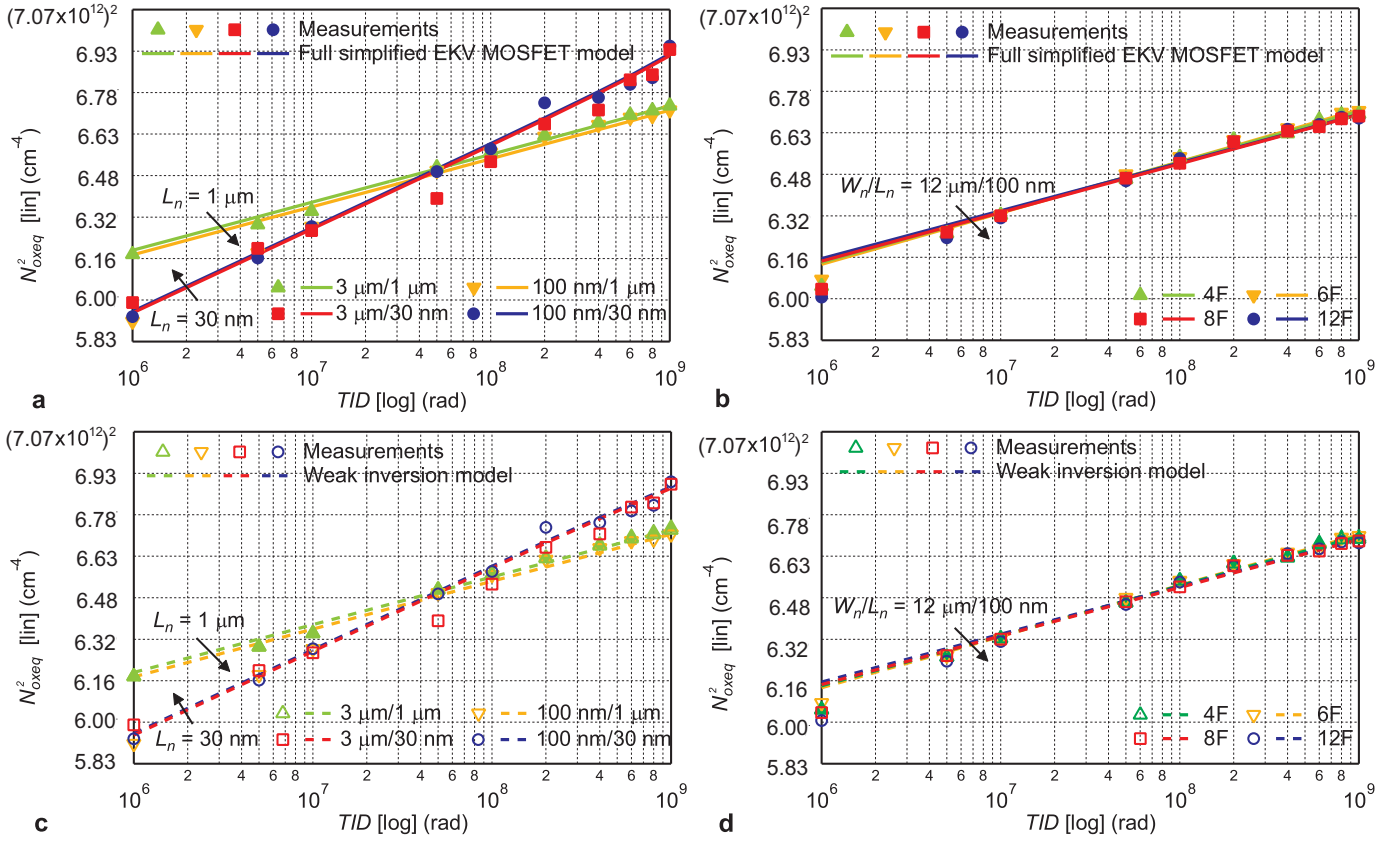


Fig. 9. Square of the extracted (markers) and modeled (lines) equivalent density of STI-related trapped charges per unit area N^2_{oxeq} versus the total ionizing dose (*TID*) in lin-log scale for single-finger (ac) and multi-finger (bd) *n*MOSFETs. (a) and (b) correspond to the full simplified EKV MOSFET model, whereas (c) and (d) correspond to the weak inversion approximation.

the slope factor n is defined as $n = 1 + \Gamma_b/(2\sqrt{\Psi_s})$ that links the depletion capacitance C_d by $C_d = C_{ox}(n-1)$.

Subtracting Q_b from Q_{si} gives the expression of Q_m:

$$Q_m = -\Gamma_{b.par}\sqrt{U_T} \left[\sqrt{\exp\frac{-2\Phi_F - V_{ch}}{U_T}\left(\exp\frac{\Psi_s}{U_T} - 1\right) + \frac{\Psi_s}{U_T}} - \sqrt{\frac{\Psi_s}{U_T}}\right]. \quad (9)$$

Under the flatband condition, Ψ_s and Q_m equal to zero. Combining (8) and (9) and following the steps from (3.40) to (3.48) in [32] with the redefined parameters, we obtain the charge-voltage relation:

$$v_{p.par} - v_{s,d} = 2q_{s,d} + \ln q_{s,d}, \quad (10)$$

where $q_s = Q_{iS}/Q_{spec.par}$ is the normalized mobile charge density at source, $q_d = Q_{iD}/Q_{spec.par}$ is the normalized mobile charge density at drain, Q_{iS} and Q_{iD} are the mobile charge densities at source and drain, respectively, $Q_{spec.par} = -2C_dU_T$ is the specific charge, $v_{p.par} = V_{P.par}/U_T$ is the normalized pinch-off voltage, $V_{P.par} = Q^2_{oxeq}/\Gamma^2_{b.par} - 2\Phi_F - (\ln 2)U_T$ is the pinch-off voltage, $v_s = V_S/U_T$ is the normalized channel voltage at source, and $v_d = V_D/U_T$ is the normalized channel voltage at drain.

Adopting the drift-diffusion model $I_D = -\mu_n(W_{neq}/L_n)\int_{V_S}^{V_D} Q_m dV_{ch}$, we obtain the charge-current relation:

$$i_{f,r} = q^2_{s,d} + q_{s,d}, \quad (11)$$

where $i_f = I_F/I_{spec.par}$ is the normalized forward current, $i_r = I_R/I_{spec.par}$ is the normalized reverse current, I_F and I_R are the forward and reverse currents, respectively, $I_{spec.par} = 2\mu_nC_dU^2_TW_{neq}/L_n$ is the specific current, and μ_n is the low-field electron mobility that is assumed equal to that of the main *n*MOSFET. The parallel parasitic drain-to-source leakage current $I_{Dleak.par}$ is the difference between the forward current I_F and the reverse current I_R. Since the reverse current I_R is negligible in saturation, combining (10) and (11) and neglecting I_R leads to the current-voltage relation:

$$v_{p.par} - v_s = \sqrt{1 + 4i_{dleak.par}} + \ln\left(\sqrt{1 + 4i_{dleak.par}} - 1\right) - (1 + \ln 2), \quad (12)$$

where $i_{dleak.par} = I_{Dleak.par}/I_{spec.par}$ is the normalized parasitic leakage current. Taking into account the velocity saturation (VS) effect, the current-voltage relation for short-channel parasitic *n*-*Q*FETs becomes [33]:

$$v_{p.par} - v_s = \sqrt{(1 + \lambda_c i_{dleak.par})^2 + 4i_{dleak.par}} + \ln\left[\sqrt{(1 + \lambda_c i_{dleak.par})^2 + 4i_{dleak.par}} - 1\right] - (1 + \ln 2), \quad (13)$$

where $\lambda_c = L_{sat}/L_n$ is the VS parameter and L_{sat} corresponds to the section of the channel where the carrier drift velocity saturates. L_{sat} is assumed equal to that of the main *n*MOSFET.

The proposed charge-controlled concept is similar to the work of Zebrev et al. [34]. However, the work of Zebrev

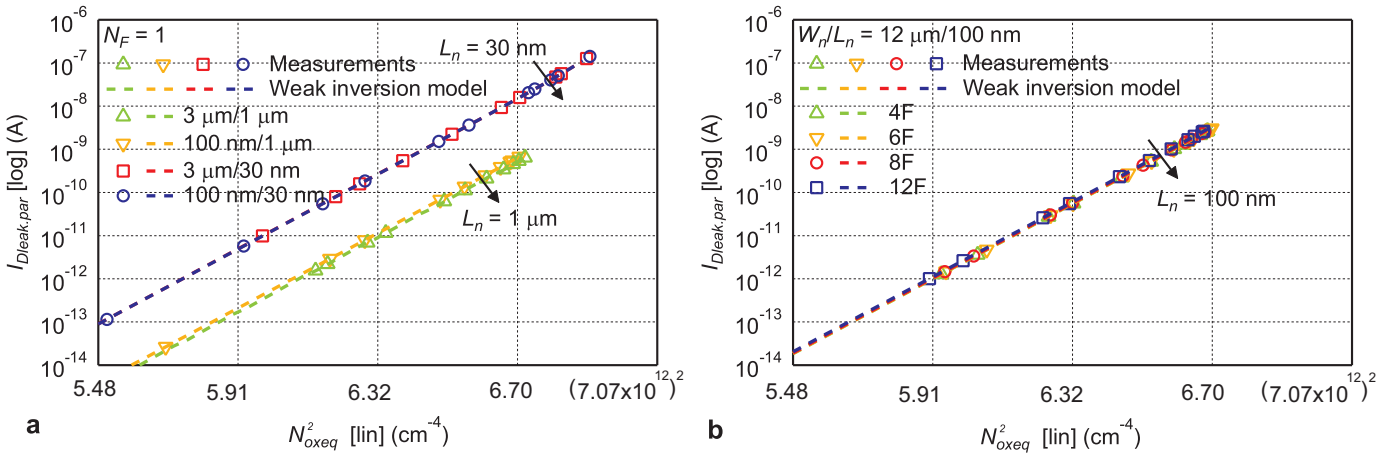


Fig. 10. Extracted and modelled parasitic drain-to-source leakage current $I_{Dleak.par}$ of single-finger (a) and multi-finger *n*MOSFETs (b) versus the square of the density of STI-related trapped charges N^2_{oxeq}.

et al. focuses on the inter-device parasitic leakage current underneath the STI oxide between the *n*-well of a *p*MOSFET and the source/drain of the nearby *n*MOSFET, whereas our work focuses on the intra-device parasitic leakage current along the STI sidewalls in parallel with the main *n*-type channel. Moreover, the work of Zebrev et al. is limited to the linear operation and validated at low TID levels (krad), whereas our approach is able to cover the parallel parasitic drain-to-source leakage current from linear to saturation and extends to rather high TID levels up to 1 Grad.

C. Extraction of the equivalent density of STI-related trapped charges

Solving (2) with (12) or (13), we extract the equivalent density of STI-related trapped charges N_{oxeq} from measurement results. Combining (4) with (12) or (13), we obtain the N_{oxeq} predicted by the proposed models. The square of the extracted and modeled N_{oxeq} are plotted as closed markers and solid lines in Fig. 9a and Fig. 9b, respectively. Model results are in good agreement with the extraction. The lateral parasitic *n*-*Q*FETs of the same length have the same amount of STI-related trapped charges, which is consistent with their close amount of parallel parasitic drain-to-source leakage current.

D. Weak inversion approximation

As mentioned in Section V-B, N_{oxeq} needs to be higher than $7.06 \times 10^{12}\text{cm}^{-2}$ for Ψ_s to be higher than $2\Phi_F$ and to bias the parasitic *n*-*Q*FET in strong inversion. However, as shown in Fig. 9a and Fig. 9b, the highest value of N_{oxeq} is around $6.95\times10^{12}\text{cm}^{-2}$. This meets our intuition that even after 1 Grad(SiO_2) of TID, the lateral parasitic *n*-*Q*FET still works in weak inversion and might eventually enter the moderate inversion. Therefore, we consider only the weak inversion operation for an approximated solution to the equivalent density of STI-related trapped charges.

Now we focus on the logarithmic term of (10): $v_{p.par} - v_s = \ln q_s$. Substituting the normalized variables with the absolute values brings back to the original expression: $Q_m/(-2C_dU_T) = \exp[(V_{P.par} - V)/U_T]$. Introducing it into the drift-diffusion model gives

$$I_{Dleak.par} = \frac{2\mu_n C_d U_T W_{neq}}{L_n} \int_{V_S}^{V_D} \exp \frac{V_{P.par} - V_{ch}}{U_T} dV_{ch}. \quad (14)$$

Solving the integral gives the parallel parasitic drain-to-source leakage current in weak inversion $I_{Dleak.par}$:

$$I_{Dleak.par} = I_{spec.par} \left(\exp \frac{V_{P.par} - V_S}{U_T} - \exp \frac{V_{P.par} - V_D}{U_T} \right). \quad (15)$$

Since $V_D > V_{P.par}$ in saturation, $I_{Dleak.par}$ is finally modeled as:

$$I_{Dleak.par} = I_{spec.par} \exp \frac{V_{P.par} - V_S}{U_T}. \quad (16)$$

Combining (4) and (16), replacing $V_{P.par}$ with $Q^2_{oxeq}/\Gamma^2_{b.par} - 2\Phi_F - (\ln 2)U_T$, and including the VS parameter λ_c, we obtain the approximated solution for STI-related trapped-charge density:

$$Q^2_{oxeq} = \Gamma^2_{b.par} U_T \left[\ln \left(\frac{(2+\lambda_c) I_{Dleak0}}{2 I_{spec.par}} \right) + k \ln \left(\frac{TID}{TID_{crit}} \right) + \frac{2\Phi_F}{U_T} + \ln 2 \right]. \quad (17)$$

Setting λ_c to zero leads to the long-channel model.

The square of the extracted and modeled N_{oxeq} using the weak inversion approximation are plotted as open markers and dashed lines in Fig. 9c and Fig. 9d, respectively. The weak inversion approximation presents almost the same results as the full simplified EKV MOSFET model, except the slight mismatch at ultra-high TID levels where the lateral parasitic *n*-*Q*FET approaches the moderate inversion. In addition, the straight lines fit the relation of $Q^2_{oxeq} \propto k \ln(TID/TID_{crit})$ in (17). The weak inversion model is therefore a very good approximation for the parallel parasitic drain-to-source leakage current.

Replacing all defined terms in (16) with the full expressions provides a direct link between the parallel parasitic drain-

to-source leakage current $I_{Dleak.par}$ and the channel doping concentration N_b:

$$I_{Dleak.par} \propto \exp \frac{Q_{oxeq}^2}{2q\epsilon_{si}N_bU_T}. \quad (18)$$

The parallel parasitic drain-to-source leakage current $I_{Dleak.par}$ increases exponentially with the square of STI-related trapped-charge density Q_{oxeq}^2, as shown by the straight lines in the log-lin plots in Fig. 10. For a higher channel doping concentration N_b, the lateral parasitic *n*-*Q*FET needs a higher Q_{oxeq} to reach the same amount of $I_{Dleak.par}$. Advanced CMOS technologies with a higher channel doping concentration is therefore advantageous in terms of radiation-induced static power consumption.

VI. Conclusion

This paper characterizes and models the effects of total ionizing dose (TID) up to 1 Grad(SiO_2) on the drain leakage current of *n*MOSFETs fabricated with a commercial 28-nm bulk CMOS process. Static measurements demonstrate a significant increase up to four orders of magnitude in the drain leakage current. At high TID levels, the drain leakage current is independent of the width but dependent on the length and the number of fingers, indicating the dominant contribution of the TID-induced lateral parasitic devices.

We model the parallel parasitic and total drain leakage current as a function of TID with a semi-empirical physics-based approach. Using only three parameters, model results have good agreement with measurements. One of those three parameters is the critical total dose that is defined as the TID, above which the parallel parasitic drain-to-source leakage current dominates the total drain leakage current. This model provides a practical way of predicting the parallel parasitic drain-to-source leakage current.

Owing to the gate independence of the drain leakage current at high TID levels, we model the lateral parasitic device as a gateless device that is fully controlled by STI-related trapped charges. The simplified charge-based EKV MOSFET model indicates that even at 1 Grad, the STI-related trapped-charge density is not high enough to bias the lateral parasitic device in strong inversion. The weak inversion approximation gives a direct link between the STI-related trapped-charge density and the parallel parasitic drain-to-source leakage current, indicating the advantage of a higher channel doping concentration in termas of radiation-induced static power consumption.

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