ReRAM From Material Study to CMOS Co-integration

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Life is not easy for any of us. But what of that?
We must have perseverance and above all confidence in ourselves. We must believe that we
are gifted for something and that this must be attained.
— Marie Curie

To my parents… Simin and Aliakbar

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Abstract

The revolution of information-technology owes to silicon-based complementary-metal-oxide (CMOS) technology. However, CMOS technology approaches its physical limitation hardening the further progress of memory devices as well as computing paradigm requiring great speed, low power dissipation and high efficiency at elevated density feature. Among the emerging technology, resistive random access memory (ReRAM) based on transition-metal oxide is one of the most promising candidates to meet these requirements. The scalability, simplicity and CMOS compatibility of metal-oxide based ReRAM enable the realization of fully operational high-density memory devices that can be also implemented with robust CMOS technology to boost computing system functionality. The present dissertation provides an examination of the ReRAM, based on transition-metal oxide as a viable alternative for non-volatile multi-level data storage from proper material selection to heterogeneous implementation with conventional CMOS technologies.

In this thesis, we present a practical consideration regarding the ReRAM-CMOS co-integration using tungsten (W) as the ReRAM electrode. W is one of the most promising material to be used as ReRAM electrode for its CMOS-compatibility with the prospect of device integration, scalability, and low-power consumption. However, W has multiple oxide phases that influence profoundly the ReRAM electrical performances. First, we have studied comprehensively the stand-alone W-based ReRAM properties to have an in-depth understanding of the effect of W electrode on ReRAM performances. We have controlled the effect of W oxidation through the insertion of the interfacial layer. The precise modulation of resistance states has been achieved through the adjustment of pulse input parameters and the incorporation of W in switching. Notable improvements in endurance, power consumption, resistance state stabilization, cycle-to-cycle, and device-to-device variability are reported. Switching kinetics and conductive nano-filament (CNF) evolution is studied in details to understand the microscopic effect of the interface modifications.

We also proposed a technique for the nm-scale heterogeneous ReRAM-CMOS co-integration based on using W via from CMOS 180 nm technology. The co-integrated stacks show self-limiting behavior with an operating current less than 1 mA. The process optimization and stack engineering have been carried out to obtain high device functionality. The results of the best performed integrated (W/Al_2O_3 (3 nm)/HfO_2 (5 nm)/TiN) ReRAM were further supported by HRTEM-EDX microstructural characterization and electrical performance simulation.

Moreover, we have studied the potential of high ion conductive CGO and YSZ thin films to be used as the ReRAM switching layer. Both materials exhibited stable switching performance and great endurance. The formation of multi-filament for CGO and single-filament for YSZ have been proposed as the switching mechanism supported by the electrical characterization. The further scaling process optimization and stack engineering have been performed on the CGO-based ReRAM. For the first time, the outstanding electrical characteristics have been achieved for the (Pt/CGO (14 nm) /Al (3 nm) /TiN), including operating voltage of (-2 to 1 V) at 150 μA, high endurance of 10^5 with the 100 μs pulse width and the capability of multi-level switching by the careful pulse programming operation.

Key words: ReRAM, Tungsten, Via, Oxidation, Time-dependency, Aluminum oxide, Barrier layer, Titanium, Aluminum, Oxygen scavenging layer, Interface engineering, Resistive switching, CMOS technology, Co-integration, Post-processing, Chip-scale, Yttrium stabilized zirconia, Gadolinium doped ceria, Multi-level switching, Ion-conducting, Resistance modulation

Résumé

La révolution des technologies de l'information repose sur la technologie dite CMOS, pour complementary metal oxide semiconductor (métal-oxyde-semiconducteur complémentaire). Cependant, la technologie CMOS approche de ses limites physiques, ce qui complique la poursuite du développement de composants de mémoire ainsi qu'un paradigme de puissance de calcul qui nécessite une vitesse élevée, une faible dissipation d'énergie et un rendement élevé à densité de composants élevés. Parmi les technologies émergentes, les mémoires vives résistives (ReRAM pour Resistive Random Access Memory), basées sur les oxydes de métaux de transition, sont l'un des candidats les plus prometteurs pour satisfaire ces exigences. La facilité de miniaturisation, la simplicité, la compatibilité avec les procédés CMOS et la topologie sans transistor des ReRAM basées sur des combinaisons métal-oxyde permettent la réalisation de composants de mémoire de haute densité, complètement opérationnels, qui peuvent également être implémentés en combinaison avec la technologie CMOS, bien établie, afin d'améliorer les performances des systèmes de calcul. Le présent travail fourni un examen des dispositifs de type ReRAM basés sur des combinaisons métal de transition-oxyde en tant qu'alternative viable pour le stockage de données non-volatile multi-niveaux, du choix des matériaux à l'implémentation hétérogène avec les techniques CMOS conventionnelles.

Dans cette thèse, nous présentons une réalisation pratique concernant la co-intégration des procédés ReRAM et CMOS employant le tungstène (W) comme électrode des cellules de ReRAM. W est l'un des matériaux les plus prometteurs pour l'électrode des cellules de ReRAM, grâce à sa compatibilité avec les procédés CMOS et les perspectives d'intégration, de miniaturisation et de faible consommation d'énergie qu'elle ouvre. Cependant, l'oxyde de W peut exister dans plusieurs phases qui influencent en profondeur les performances électriques des cellules de ReRAM. En premier lieu, nous avons étudié en détail les propriétés des cellules isolées de ReRAM à base de W pour obtenir une compréhension profonde des effets de l'électrode de W sur les performances des ReRAM. Nous avons contrôlé les effets de l'oxydation de W grâce à l'insertion d'une couche interfaciale. La modulation précise des différents états résistifs a pu être obtenue grâce à l'ajustement des paramètres des impulsions d'écriture et par l'incorporation de W dans le processus de bascule de résistance (switching). Nous présentons des améliorations notables en termes d'endurance, de consommation d'énergie, de stabilité des états résistifs, et de variabilité cycle-à-cycle et cellule-à-cellule. La cinétique du switching et l'évolution des nano-filaments conducteurs (NFC) sont étudiées en détail dans le but de comprendre les effets microscopiques des modifications de l'interface.

Nous proposons également une technique pour la co-intégration hétérogène ReRAM-CMOS à l'échelle du nm, basée sur l'utilisation d'interconnections verticales (via) à base de W, issues la technologie CMOS 180 nm. Les composants co-intégrés présentent un comportement auto-limité en courant, avec un courant limite inférieur à 1 mA. Des performances élevées des composants ont pu être obtenues grâce à l'optimisation du procédé et au design des cellules. Parmi les différents types de composants fabriqués, les cellules ReRAM (W/Al_2O_3 (3 nm)/HfO_2 (5 nm)/TiN) sont les plus performantes, ce qui est corroboré par la caractérisation microstructurale au HRTEM-EDX et par des simulations des performances électriques.
De plus, nous avons étudié le potentiel des couches minces de CGO et YSZ, deux matériaux à conduction ionique élevée, comme couche active des cellules de ReRAM. Les deux matériaux possèdent des performances de switching stables et une bonne endurance. Nous proposons la formation de multi-filaments pour le CGO et d'un filament unique pour le YSZ comme mécanismes de switching; cette hypothèse est corroborée par la caractérisation électrique des cellules. Nous avons procédé à l'optimisation du design et à la miniaturisation des cellules ReRAM à base de CGO. Pour la première fois, d'excellentes caractéristiques électriques ont pu être obtenues pour les cellules de type (Pt/CGO (14 nm)/Al (3 nm)/TiN), incluant un voltage opérationnel de -2 V à 1 V pour un courant de 150 μA, une endurance élevée de 10^5 cycles pour une largeur d'impulsion de 100 μs, et la possibilité d'un switching multi-niveaux par la programmation bien choisie des impulsions.

Mots clefs : ReRAM, tungstène, via, oxydation, dépendance en temps, oxyde d'aluminium, couche-barrière, titane, aluminium, couche de récupération d'oxygène, ingénierie des interfaces, bascule de résistance, technologie CMOS, co-intégration, post-processing, échelle du composant, zircone stabilisée à l'yttrium, oxyde de cerium dopé au gadolinium, switching multi-niveaux, conduction ionique, modulation de résistance.

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1 Introduction

The rapid growth of data infrastructure over the last 40 years has changed the different aspect of our lives dramatically. Particularly important is the latest generation of processor and microelectronic devices, i.e. a paper-thin computer/telephone, digital cameras, global positioning system (GPS) with an accuracy in the range of a few feet and the autonomous cars with the capability of communication to the other cars. These technologies demand high speed, low power dissipation, low cost and high efficiency while being small and reliable. However, CMOS technology with the physical scaling limitations and consequent high power dissipations can not anymore meet these requirements. Thus, the new technology for nano-devices seeks to a supplement and/or a replacement for CMOS leading to the new approaches of memory and logic technologies improvement [13]. Memory technologies are mainly categorized into two main groups of "volatile" and "non-volatile". Unlike the volatile memories, non-volatile memories have the capability to hold saved data even if the power is turned off. Static random access memory (SRAM) and dynamic random access memory (DRAM) are the volatile and FLASH is the non-volatile memory which are used as cashes, main memory and solid-state drive in computer systems respectively. The comparison between the functionality of conventional memories is schematically shown in Figure1.1. SRAM on the top of the pyramid performs with high read/write speed of 1 ns and great endurance of >10^{16} cycles. It consists of 6 transistor and suffers from non-volatility, small device density due to the large cell area of 24-140 F^2 (F is the feature size of the lithography used for patterning the cell), low capacity storage and high cost [14].

Going down the pyramid, DRAM consists of a cell capacitor in series with a transistor (1T1C) for the data storage in which logic "1" and logic "o" are attributed to the presence and absence of the charge in storage node. It has large device density capability (cell area: $24F^2$) and performs with excellent endurance (>10^{16}) and reasonable speed of 10 ns while it requires power for the data retention. The main limiting factor of DRAM scalability is the cell capacitor. NAND Flash memory with the feature of non-volatility are scaling ahead to DRAM in terms of scalability as well as storage capacity which is placed at the bottom of this pyramid. However,

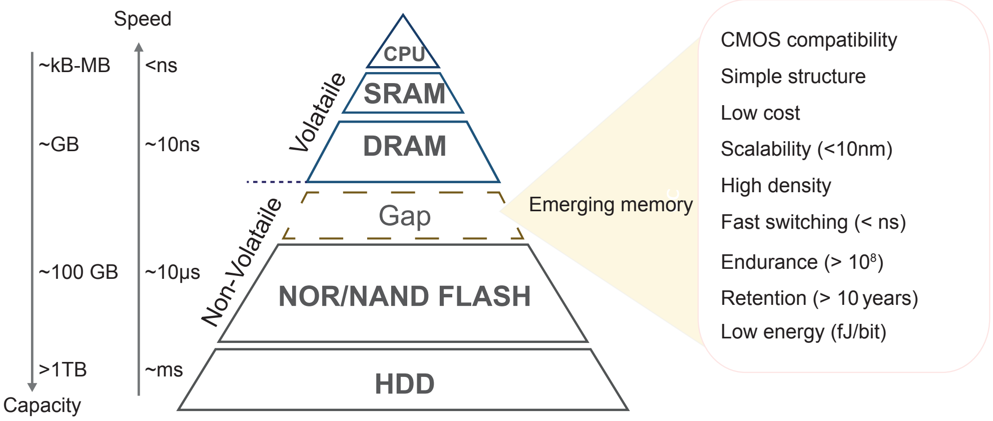

Speed
~kB-MB
~GB
~100 GB
>1TB
Capacity
<ns
~10ns
~10μs
~ms
CPU
SRAM
DRAM
Gap
NOR/NAND FLASH
HDD
Volataile
Non-Volataile
Emerging memory
CMOS compatibility
Simple structure
Low cost
Scalability (<10nm)
High density
Fast switching (< ns)
Endurance (> 10⁸)
Retention (> 10 years)
Low energy (fJ/bit)

Figure 1.1 – The current mainstream memory hierarchy; SRAM and DRAM are the volatile memories which are served as cache and main memory in computer systems while Flash is the non-volatile memory used as the solid state drive. Adopted from [1]

the scalability of the Flash is approaching its physical limitations (>10 nm) due to the high current leakage in the floating gate layer [14].

Emerging non volatile memory (NVM) technology with nano-store architecture is an alternative solution to combine the advantage of mainstream memories while avoiding their drawbacks filling the gap between FLASH and DRAM in the memory hierarchy. Among various types of emerging memory technologies, resistance switching random access memories (RRAM) have made remarkable improvement in the past decade and offer the possibility of higher areal density, scalability and greater performance. In particular, the RRAM category of Redox-based RAM (ReRAM) has progressed significantly in the past two years from fundamental understanding to technological development of working prototype chips searching for the ideal metrics of having an endurance of 10^8 cycles, data retention of >10 years, low bit error with the sufficient resistance window, low power dissipation with operating voltage of <3 V, current range of mA-nA, fast switching speed in range of ns and energy consumption of fJ/bit. Furthermore, the hybrid integration of ReRAM with CMOS circuitry can combine the advantage of high yield and mature circuit functionality of CMOS, with the high-density feature of ReRAMs [15–17]. ReRAM as a passive circuit element with the active CMOS circuitry also meet the requirements for other applications such as neuromorphic computing circuit [18], reconfigurable logic [7] and analogue computations [19] applications. However, it is still crucial to correlate the design concept of ReRAM with electrical performance improvement, switching mechanism understanding, material processing and CMOS-integration.

In this context, the present thesis covers the material selection for ReRAM around the central concept of heterogeneous ReRAM-CMOS co-integration. First, we have extensively studied the impact of W electrode on different aspect of ReRAM properties on the stand-alone substrate (Chapter 3). Next, We have ascertained a technique for the hybrid integration of nm-scale W-based ReRAM on the foundry-produced CMOS 180 nm technology chip. In the first approach, self-align and mask-free WO_x switching layer is formed on the top of W via and in the second approach, HfO_2 as the most well-established switching layer is employed (Chapter 4). Finally, we have studied the fast ion conducting thin films, i.e. gadolinium doped cerium oxide (CGO) and yttrium stabilized zirconium oxide (YSZ), as promising materials with the potential of offering forming-less and low-power switching behavior (Chapter 5). These are indeed the main requirements of ReRAM implementation on the BEoL of CMOS circuitry. The results and discussion are provided in the format of paper manuscripts.

2 State-of-the-art

The emerging memories are two terminal devices that can store data by switching between a high resistance state (HRS or Off-state) and a low resistance state (LRS or on-state) by applying electrical stimuli. Among different types of studied emerging memories, spin torque transfer magnetic resistive random access memory (STT-MRAM) [20], phase change random access memory (PRAM) [21], ferroelectric random access memory (FRAM) [22] and resistive random access memory (ReRAM) [6] are the most promising candidates towards the ideal memory characteristics, i.e. operation speed (< ns), retention (> 10 years), write/read endurance ($> 10^8$ cycles), scalability (< 10 nm) and energy consumption (fJ/bit) [20]. The characteristics of these memories are strongly dependent on the employed material that are showing different switching mechanism. The main characteristics of conventional and emerging memories are listed in Table 2.1.

Table 2.1 – The mainstream and emerging memory technology devices characteristics. Adopted from [11]

Type	Mainstream memories				Emerging memories			
	SRAM	DRAM	Flash		STT-RAM	PCRAM	FRAM	ReRAM
			NOR	NAND				
Cell element	6T	1T1C	1T	1T	1(2)T1R	1T1R/1D1R	1T1C	1T1R/1D1R
Cell Area	$>100\,F^2$	$6\,F^2$	$10\,F^2$	$<4\,F^2$ (3D)	$6\sim 20\,F^2$	$4\sim 20\,F^2$	$22\,F^2$	$< 4\,F^2$(if 3D)
Multi-bit	1	1	2	3	1	2	1	2
Voltage	<1 V	<1 V	>10 V	>10 V	<2 V	<3 V	1.1-3.3 V	<3 V
Read time	~ 1 ns	~ 10 ns	~ 50 ns	~ 10 μ s	<10 ns	<10 ns	~40 ns	< 10 ns
Write time	~ 1 ns	~ 10 ns	10 μs-1 ms	100 μs-1 ms	<5 ns	<5 ns	~65 ns	<5 ns
Retention	N/A	~ 64 ms	>10 y	>10 y	>10 y	>10 y	10 y	>10 y
Endurance	$>10^{16}$	$>10^{16}$	$>10^5$	$>10^4$	$>10^{15}$	$>10^9$	10^{14}	$>10^6\sim 10^{12}$
Write energy (J/bit)	~ fJ	~ 10 fJ	~ 100 pJ	~ 10 fJ	~ 0.1 pJ	~ 10 pJ	~ 10 fJ	~ 0.1 pJ
Cell	Latch	Main memory	Storage	Storage	Storage	Storage	Storage	Storage/main memory

F: feature size of the lithography. The energy estimation is on cell-level (not array-level).

The conventional memory technology, i.e. SRAM, DRAM and Flash memory performances are based on charge storage mechanism which is the main limiting factor for device scaling (< 10 nm). Th charges are stored in the dielectric layer of DRAM and in the floating gate of the FLASH. However, the emerging memory performances are not based on the charge storage leading to scalability below 10 nm along with higher reliability and larger noise margin. STT-MRAM can store data according to the electron spin orientation in which LRS is attributed to the parallel spin configuration while HRS is the anti-parallel ones. Low operating voltage, high speed and unlimited endurance are the main features of STT-MRAM [20]. In FRAM, switching relies on different polarization states of a ferroelectric material e.g lead zirconate titanate (PZT) [22]. PRAM switches between two different phases of crystalline (LRS) and amorphous (HRS) through the current induced Joule heating [21]. The most common material for PRAM is chalcogenide GeS_2 (GST) which is widely used for CD and DVDs. The main PRAM issues are high operating current which limits the high device density integration and reduces its reliability. ReRAM in principle covers all type of memory which can show two distinct non-volatile resistance states by applying an electric field. In the next section, the details of the ReRAM specifications and switching mechanism will be described.

2.1 Resistive random access memory (ReRAM)

The concept of the resistive switching (RS) is dated back to the early 1960s. Hickmott [23] has observed a low frequency negative resistance in the wide variety of thin film, i.e SiO_x, Ta_2O_3, TiO_2 and Al_2O_3 in a capacitor-like structure and later, it has been proposed [24] to use this concept for NVM devices. However, the further progress of the RS phenomenon has delayed for 30 years due to the more successful development and robustness of transistor based memories. Nevertheless, the improved capacity of metal oxide thin film processing and characterization during these years, as well as, scaling trend limitation following Moor's law, raised backed the attention to RS as an alternative solution in the early 2000s. A.Beck et al [25] and S.Q. Liu et al. [26] have reported a reliable performance of resistance switching in perovskite-type oxides such as Cr-doped $SrZrO_3$ and $Pr_0.7Ca_0.3MnO_3$ using 500 nm CMOS technology process for NVM applications. These findings have increased the interests of RS field for both research-level and application-oriented goals dramatically and various range of materials have been investigated for ReRAM. Ma et al. [27] have proposed the organic-based ReRAM. Samsung electronic presented the first successful integration of a binary metal oxide, NiO_x-based ReRAM array in 180 nm CMOS technology with the operating voltage (<3 V), endurance of 10^6 and reading cycle of 10^{12} [28]. Hewlett-Packard research laboratory [7, 29] has developed circuit design concept and hybrid co-integration of ReRAM as the fourth passive circuit element based on the memristor theory previously proposed by L.Chua [30]. Recently, numerous studies have been carried out to understand the physics of RS mechanism in binary metal oxide, to address the technical issues for ReRAM commercialization and using it for other applications than memory including, neuromorphic computing systems [18, 31], reconfigurable logic [7] and analogue computations [19]. The main focus of this work is on the oxide-based ReRAMs, thus, further mentioning of ReRAM only refers to oxide-based ReRAM (OxRAM).

2.2 The principle of resistive switching in ReRAM

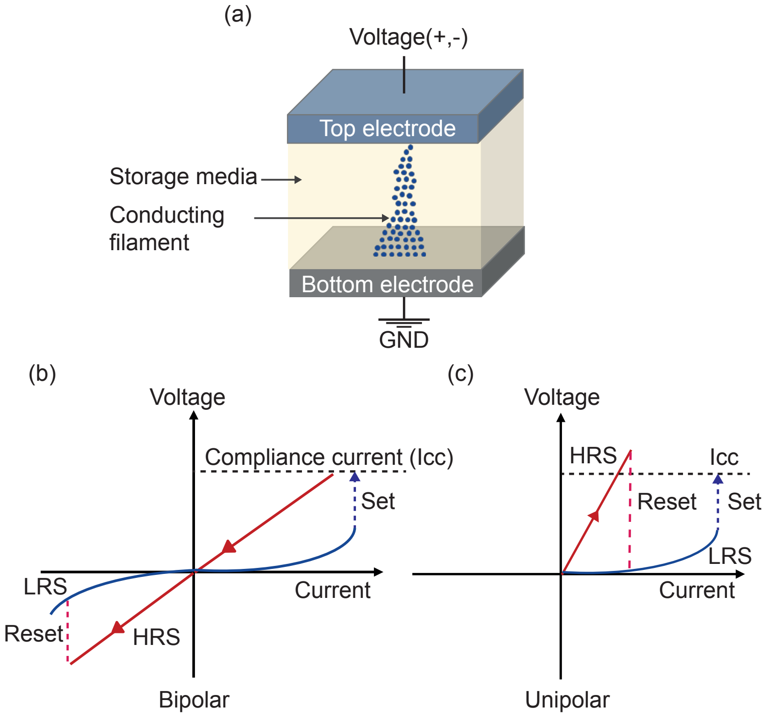

(a)
Voltage(+,-)
Top electrode
Storage media
Conducting filament
Bottom electrode
GND
(b)
Voltage
Compliance current (Icc)
Set
LRS
Current
Reset
HRS
Bipolar
(c)
Voltage
HRS
Icc
Reset
Set
LRS
Current
Unipolar

Figure 2.1 – (a) The schematic of ReRAM structure which is an insulator/semiconductor layer between two electrodes. (b) The bipolar switching modes and (c) the unipolar switching mode.

ReRAM is consist of an insulator/semiconductor layer (switching layer) which is placed between two electrodes as shown in Figure 2.1(a). The memory principle depends on resistive switching between at least two different resistance states of LRS and HRS through an application of suitable stimuli. The switching from HRS to LRS is called *Set* process and the reverse switching from LRS to HRS is called *Reset* process. A fresh ReRAM cell shows quite high initial resistance state and a pretreatment is required to trigger the switching which is called *forming* operation. Forming is a soft break down in the oxide layer which results in the creation of a conductive filament (CF) [32]. The consecutive Set and Reset operation is due to the creation and rupture of such CF. In both Set and forming operation, the current needs to be limited by applying a compliance current (I_{CC}) to avoid the hard break down. Normally, the I_{cc} is provided by an external parameter analyzer in 1R configuration or by a transistor/diode in 1T(D)1R configurations. The ReRAM switching modes can be mainly categorized as bipolar and unipolar. The schematic of I-V characteristics of both switching modes is demonstrated in

Figure 2.1(a,b). In bipolar switching (Figure 2.1(a)), the Set and Reset occur at different voltage polarities while in unipolar switching, the switching is dependent on the voltage amplitude and both Set and Reset happen at the same voltage polarity. The switching modes are not the intrinsic property of the oxide materials but also dependent on the electrodes and their electrode/oxide interface properties. However, it has been proved that in both unipolar and bipolar modes, oxygen migration/diffusion plays a critical role in resistance switching [33]. Numerous experimental and theoretical studies have been attempted to explain the physics of switching mechanism. Mostly, when the electrodes are noble and identical such as Ru or Pt, the switching mode is unipolar while using an oxidizable electrode with low work function such as Al, Ti and W, results in bipolar switching [15]. Figure 2.2 schematically explains the unified resistive switching model for both unipolar and bipolar presented by Yu et al. [2].

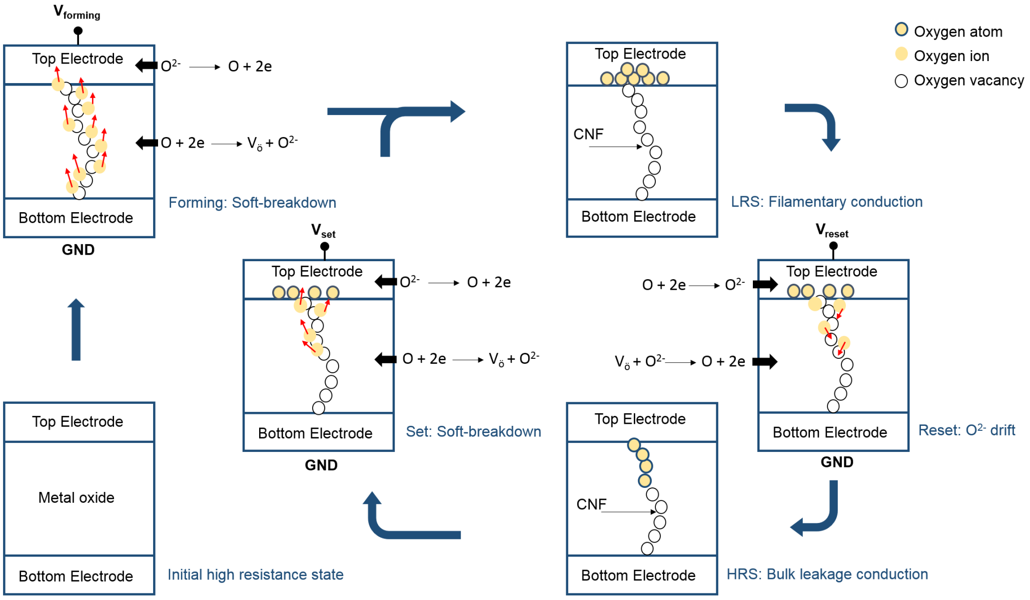

$V_{forming}$
Top Electrode
O^{2-} → O + 2e
O + 2e → $V_{ö}$ + O^{2-}
Bottom Electrode
GND
Forming: Soft-breakdown
Top Electrode
CNF
Bottom Electrode
LRS: Filamentary conduction
Oxygen atom
Oxygen ion
Oxygen vacancy
V_{set}
Top Electrode
O^{2-} → O + 2e
O + 2e → $V_{ö}$ + O^{2-}
Bottom Electrode
GND
Set: Soft-breakdown
V_{reset}
O + 2e → O^{2-}
$V_{ö}$ + O^{2-} → O + 2e
Top Electrode
Bottom Electrode
GND
Reset: O^{2-} drift
Top Electrode
Metal oxide
Bottom Electrode
Initial high resistance state
Top Electrode
CNF
Bottom Electrode
HRS: Bulk leakage conduction

Figure 2.2 – Schematic of switching process in metal-oxide based ReRAMs. Adopted from [2]

During the forming, by applying a positive voltage bias on top electrode, the oxygen ions are pushed towards the TE interface, leaving back the oxygen vacancies in the bulk oxide. When the TE is noble, oxygen ions are discharged while in case of an oxidizable electrode (oxygen reservoir layer), a thin layer of TE metal-oxide is formed at the interface. Thus, the CF made of oxygen vacancies enables the current flow and the memory is at LRS. During the Reset process, the oxygen ions are moved back to the bulk oxide or recombine with the oxygen vacancies resulting in the CF rupture and HRS. In unipolar mode, the oxygen movement is due to the Joule heating and high current is required to provide sufficient thermal energy while in bipolar, the ion drifts are attributed to both the reverse voltage polarity and thermal energy.

During the switching, the dynamic of CF is attributed to mixed of ionic-electronic conduc-

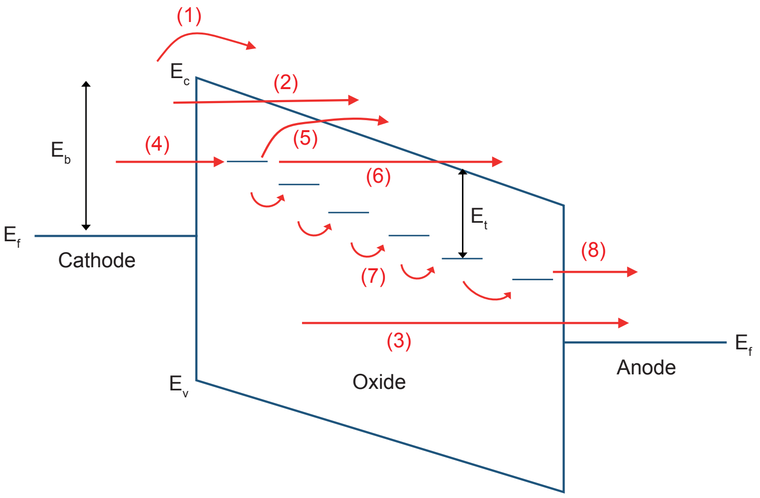


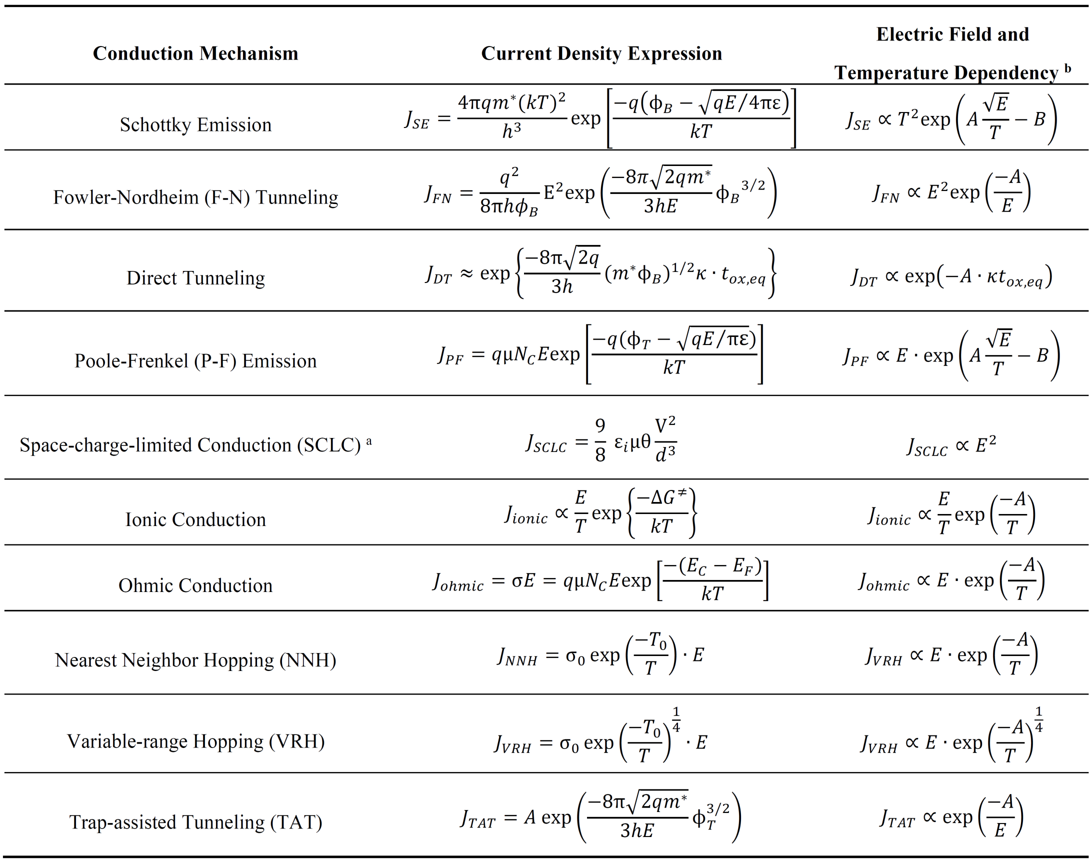
Figure 2.3 – Possible electronic conduction mechanism in the metal-oxide films between two electrodes. (1) Schottky emission. (2) Fowler-Nordheim (F-N) tunneling in which the electron tunnels into the conduction band. (3) Direct tunneling from one electrode to another electrode when the oxide is sufficiently thin. (4) Electron injection into trap states when the oxide posses enough number of traps. (5) Poole-Frenkel (P-F) emission from trap to conduction band. (6) Direct tunneling from trap to conduction band similar to the F-N tunneling (7) Electron hopping from trap to the adjacent trap/s. (8) Tunneling from trap to anode. Adopted from [2]

tions and it is crucial to identify the conduction mechanism to enhance device performance, uniformity and data retentions. There are many factors that can influence the type of conduction mechanism such as, oxide properties (dielectric constant, band gap, trap energy level, trap density, carrier mobility, etc), processing conditions (temperature, ion bombardments, deposition technique, etc), electrodes and electrode/interface properties. Among the typical conduction mechanism, the electrode-limited mechanisms are Schottky emission, Fowler-Nordheim (F-N) tunneling, direct tunneling and the bulk-limited conduction mechanisms are Poole-Frenkel (P-F) emission, ohmic conduction, space-charge-limited conduction (SCLC), ionic conduction, hopping conduction, and trap-assisted tunneling (TAT) [34]. The possible electron paths in an oxide layer between two electrodes are schematically shown in Figure 2.3. Below, the principle of each conduction mechanism is explained briefly and the corresponding equations and field/temperature dependency are presented in Table 2.2.

Schottky emission happens when a thermally induced flow of electrons can overcome the oxide barrier potential. This is the most common conduction mechanism of oxide especially at high operating temperature [34].

F-N and direct tunneling are the emission of electrons induced by high electric field. When the oxide thickness is sufficiently low (< 3 nm), direct tunneling occurs while for thicker oxide, F-N is more dominant conduction mechanism [35].

Table 2.2 – Expression and field/temperature dependency of typical conduction mechanism in dielectric film. J_{SE}: current density, T: temperature, m* (m°): effective mass, k: Boltzmann's constant, h: Planck's constant, E: electric field, ϕ_b: junction barrier height, ε: Dielectric permittivity, α: constant, μ: charge carrier mobility, ϕ_T: depth of traps potential well, θ: ratio of free and shallow trapped charge, d: oxide thickness, N_C: density of states in conduction band, ν: Debye frequency, r: jump distance, ΔG: activation energy, σ: electrical conductivity, E_C: conduction band, E_F: Fermi-energy level, σ_0: electrical conductivity, A and B: constant. [a] Just for the high field, low filed follows ohm's law. Adopted from [12]



Conduction Mechanism	**Current Density Expression**	**Electric Field and Temperature Dependency** [b]
Schottky Emission	$J_{SE} = \frac{4\pi q m^*(kT)^2}{h^3}\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon}\right)}{kT}\right]$	$J_{SE} \propto T^2\exp\left(A\frac{\sqrt{E}}{T} - B\right)$
Fowler-Nordheim (F-N) Tunneling	$J_{FN} = \frac{q^2}{8\pi h\phi_B}\mathrm{E}^2\exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE}{\phi_B}^{3/2}\right)$	$J_{FN} \propto E^2\exp\left(\frac{-A}{E}\right)$
Direct Tunneling	$J_{DT} \approx \exp\left\{\frac{-8\pi\sqrt{2q}}{3h}(m^*\phi_B)^{1/2}\kappa \cdot t_{ox,eq}\right\}$	$J_{DT} \propto \exp(-A \cdot \kappa t_{ox,eq})$
Poole-Frenkel (P-F) Emission	$J_{PF} = q\mu N_C E\exp\left[\frac{-q(\phi_T - \sqrt{qE/\pi\varepsilon})}{kT}\right]$	$J_{PF} \propto E \cdot \exp\left(A\frac{\sqrt{E}}{T} - B\right)$
Space-charge-limited Conduction (SCLC) [a]	$J_{SCLC} = \frac{9}{8}\,\varepsilon_i\mu\theta\frac{\mathrm{V}^2}{d^3}$	$J_{SCLC} \propto E^2$
Ionic Conduction	$J_{ionic} \propto \frac{E}{T}\exp\left\{\frac{-\Delta G^{\neq}}{kT}\right\}$	$J_{ionic} \propto \frac{E}{T}\exp\left(\frac{-A}{T}\right)$
Ohmic Conduction	$J_{ohmic} = \sigma E = q\mu N_C E\exp\left[\frac{-(E_C - E_F)}{kT}\right]$	$J_{ohmic} \propto E \cdot \exp\left(\frac{-A}{T}\right)$
Nearest Neighbor Hopping (NNH)	$J_{NNH} = \sigma_0\exp\left(\frac{-T_0}{T}\right) \cdot E$	$J_{VRH} \propto E \cdot \exp\left(\frac{-A}{T}\right)$
Variable-range Hopping (VRH)	$J_{VRH} = \sigma_0\exp\left(\frac{-T_0}{T}\right)^{\frac{1}{4}} \cdot E$	$J_{VRH} \propto E \cdot \exp\left(\frac{-A}{T}\right)^{\frac{1}{4}}$
Trap-assisted Tunneling (TAT)	$J_{TAT} = A\exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE}\phi_T^{3/2}\right)$	$J_{TAT} \propto \exp\left(\frac{-A}{E}\right)$

P-F emission happens when the electrons that are trapped in the localized states of oxide achieve enough thermal energy to get out of the traps and move to the conduction band. The electric field reduces the electron Coulombic barrier height and increases the chance of P-F emission.

SCLC mechanism is determined with three main sections; low-field region which corresponds to thermally generated electrons in the oxide and is ascribed by the ohms law ($I \propto V^1$). The child's square region ($I \propto V^2$) at high electric field, when the density of emitted electrons from the electrodes exceeds the equilibrium electron density. This follows by steep current jump in the high-field region when all the traps are filled by the electrons and the resistance changes which is known as trap-filled SCLC part. SCLC is a dominant mechanism when the electrodes have low work function that can inject high number of electrons as well as enough traps are available in the oxide layer for the electron transitions [36].

Ionic conduction is attributed to the drift of ions through the available defects in the oxides by applying an electric field. The current density of ions is dependent on the ions drift velocity [37].

Ohmic conduction which is related to the motion of mobile electrons in the conduction band of the oxide and the current density is linearly proportional to the electric field .

Hopping conduction is when the electrons hop from one trap to the adjacent/further traps through tunneling effect. The trap hopping is strongly dependent on the trap energy and for further traps hopping is also dependent on the temperature [34].

TAT is traps assisted electron tunneling from one electrode to another one's. Despite F-N and direct tunneling in which the electrons are transferred through a single step tunneling, TAT, is a two-steps tunneling process. First, the injected electrons from cathode get trapped in the localized sites of the oxide and subsequently they get out of the traps and emitted to anode [38].

2.3 Thin films for ReRAM

Among different types of thin films that have been proposed for the switching layer, metal-oxide and in particular binary metal-oxides have drawn a great attention due to their simple processing and thermal stability. WO_x [39, 40] and CuO_x [41] are the most CMOS compatible oxides which can be formed through thermal oxidation of W or Cu vias from CMOS periphery. HfO_x [42], AlO_x [43], NiO_x [28], TiO_x [29] and TaO_x [5] are the most well-studied ones. Various deposition techniques including rapid thermal processing (RTP), plasma oxidation, reactive sputtering, chemical vapor deposition (CVD), pulsed laser deposition (PLD) and atomic layer deposition (ALD) are used as the deposition methods. Among all, ALD is the ideal method due to its uniformity and coverage at ultra-thin film scale. In this work, we mainly focus on HfO_x, AlO_x, WO_x, CeO_x-based and ZrO_x-based thin films for the ReRAM switching layers.

HfO_2 is a high-k dielectric material which has been widely used as a gate insulator in CMOS technology. HfO_2 is the most common material for ReRAM which its resistive switching properties have been extensively developed through structural modification, interface engineering and thermal annealing. HfO_2 does not have any stable sub-stoichiometric oxide forms [44] and the crystalline structure is both temperature and thickness dependent [45]. It has been reported that the ALD deposited HfO_2 with the thickness of (< 10 nm) at 200 °C has an amorphous structure suitable for the resistive switching material [45]. Excellent bipolar switching with the speed of (< 10 ns), retention of 10 years, endurance of ($> 10^6$ cycles), multi-bit storage, large resistance window of (R_{OFF}/R_{ON}= 100) and high device yield has been reported in 1T1R configuration of HfO_2-based ReRAM stacks [46].

Al_2O_3 is one the pioneering binary oxide for ReRAM that has very similar characteristics to HfO_2. It has an electron affinity (χ) of 1.25 ev, dielectric constant (ε) of 9 and the Gibbs free energy (ΔG) of -1582 kJ/mol [47]. Al_2O_3 has a robust oxide phase which does not form any stable sub-stoichiometric oxides and it has relatively large oxygen vacancy formation energy of 7 ev and large bad gap of ~ 8.9 eV [45,47]. Thus, the vacancy migration is strongly prohibited in Al_2O_3 which results in low current leakage, high LRS (~ MΩ) and more reliable performance during switching [43]. The low power consumption of Al_2O_3 enables the realization of ultra large-scale crossbar array memory without the need for selector devices [48]. The AlO_x-based ReRAM switching characteristics including resistance ratio of 10^6, operation speed of < 10 ns and endurance of 10^4 have been reported [43,49]. Recently, due to the strong oxygen immunity of Al_2O_3, it has been extensively used as a barrier layer with other oxides to improve switching uniformity and read disturb problems [47,50–52].

WO_x is an attractive oxide due to its CMOS compatibility, simple and low-cost processing [53]. In the conventional CMOS technology, W is the material of choice for nm-scale vertical interconnectors between the metal layers. Self-align WO_x switching layer can be formed on top of the W vias through thermal/plasma oxidation of W surfaces in which W is served as the ReRAM bottom electrode and it defines the effective size of the memory cell [39,54]. However, despite of other metal-oxides, WO_x has low pristine resistance state which limits the memory resistance window and increases the power consumption. WO_x has a variety of stable sub-stoichiometric oxide phases with different resistance states including WO_2, $WO_{2.72}$ ($W_{18}O_{49}$), $WO_{2.90}$ ($W_{20}O_{58}$), $WO_{2.96}$ ($W_{50}O_{148}$) and WO_3 [55], that are given in the equations 3.1-2.5.

$$W(s) + O_2(g) \rightleftarrows WO_2(s) \tag{2.1}$$

$$\frac{18}{49}W(s) + O_2(g) \rightleftarrows \frac{18}{49}WO_{2.72}(s) \tag{2.2}$$

$$\frac{20}{58}W(s) + O_2(g) \rightleftarrows \frac{20}{58}WO_{2.90}(s) \tag{2.3}$$

$$\frac{50}{158}W(s) + O_2(g) \rightleftarrows \frac{50}{158}WO_{2.96}(s) \tag{2.4}$$

$$\frac{2}{3}W(s) + O_2(g) \rightleftarrows \frac{2}{3}WO_3(s) \tag{2.5}$$

Each of these oxide reactions is ascribed to a specific free energy of formation (ΔG_f) that defines the thermodynamic stable condition of W oxidation ranging from -550 Kjmol^{-1} to -750 Kjmol^{-1} [55]. Depending on the energy provided to the W electrode during the oxidation, it transforms with sequential and spontaneous oxidations from the meta-stable WO_2 to the most thermodynamical stable WO_3 showing the different level of resistivity. Some of the best switching properties of WO_x-based ReRAM are reported in [53, 56, 57] showing the forming-free switching with the endurance of 10^8, resistance window of 10^4 and switching speed of (< 300 ns).

CeO_2 (ceria) is a well-known oxide for its mixed ionic-electronic conduction properties showing a great potential for ReRAM devices. Table 2.3 is an overview of the CeO_x-based ReRAM characteristics. In most of them, the switching mechanism is based on the formation/rupture of CF, made of oxygen vacancies. The main feature of CeO_2 is the coexistence and reversible valance states transitions between Ce^{3+} and Ce^{4+} which results in rapid formation and annihilation of oxygen vacancies through reduction/oxidations reactions.

Table 2.3 – Review of CeO_x-based ReRAM devices characteristics. "SR":Self-Rectifying, "less": Forming-less operation, "HRS": High Resistance State, "LRS": Low Resistance State, "DC": Direct current, "AC": Alternating current. "-":Not reported

Year	Ref.	Structure	Oxide thickness (nm)	Forming (V)	Set/ Reset(V)	HRS/LRS	I_{set} (mA)	Endurance(cycle)	Retention (s)
2005	[58]	$La_{0.67}Ca_{0.33}MnO_3$-CeO-Ag	80	-	4/ -4	10^5	10 (SR)	-	-
2008	[59]	Pt-CeO-Pt	180	9	4/ 1	10^4	5	-	10^4
2009	[60]	Pt-CeO-Al	40	8	0.6/ -1.5	10^2	5	-	10^5
	[61]	Al-CeO-Pt	40	less	0.6/ -1.5	4×10^2	20 (SR)	250	10^5
2011	[62]	TiN-Si-CeO-W	20	2.8	3/ -2.2	10	1	50	-
2012	[63]	Pt-CeO-TiN	50	-3.2	-1.1/ 2.2	10^2	1	10^4 (AC)	10^4
	[64]	NSTO-CeO-RM	175	-	-2/ 2.2	10^2	10	-	3.6×10^2
	[65]	W-CeO-Si-TiN	20	3	3/-3	10	1	50	-
	[65]	W-CeO-TiN	20	7.2	3/ -3	2	5	50	-
	[66]	Au-CeO-ITO	-	-	3/ -3	4	50	8×10^3 (AC)	-
	[67]	TaN-CeO-Ru	20	-	2/ -3	10^4	0.5	10^3 (DC)	10^6
2013	[68]	Au-CeO (cubes)-Au	162	-	2/ -2	10^4	60	200	2×10^3
	[69]	SnO_2-$Ce_{(1-x)}Co_xO$-Au	-	-	2.2/ -2.2	10^3	50	50	10^9
	[70]	In-Nb:$SrTiO_3$-CeO/ZnO-Ag	10/100	-	2/ -3	10^3	5	50	10^3
2014	[71]	Pt-CeO-TiN	20	less	-3/ 2	10^3	1	200	10^4
			30	less	-2/ 2	10^4	1	200	10^4
			40	less	-1/ 2	10^5	1	200	10^4
	[72]	$La_{0.5}Sr_{0.5}CoO_3$-CeO-Ag	80	-	4/ -4	-	0.1	-	-
	[73]	Au-CeO-Nb:$SrTiO_3$	-	-	1.8/ -4	5×10^4	1	200	10^4
	[74]	Pt-$La_{0.7}(Sr_{0.1}Ca_{0.9})MnO_3$-CeO	-	-	4/ -4	10^2	1	-	-
2015	[75]	ITO-CeO-CeO_x-Ti-TiN	15-6/8	2	2/ -2	2×10^2	0.5	10^5 (DC)	10^4
	[76]	Au-CeO-Al	13	3	-1.2/1.2	10^3	10	10^5 (AC)	10^5
	[77]	Pt-CeO-TaN	15	-	1.3/-0.8	10^4	1	500	10^4
2016	[78]	Pt-CeO-Al-CeO-Ti	3-1-2	-	2/ -2	10^2	10	10^4 (DC)	10^5
	[79]	Pt-CeO-Ti-CeO-TaN	6-1-6	-8	1.3/-1	10^2	5	10^4 (DC)	10^4
2017	[80]	Pt-CeO-Cu	3.4	10	10/ -10	4	10^{-3}	-	-
	[81]	Pt-$Ce_{0.9}Gd_{0.1}O_x$/Er_2O_3-Cu	3.4	-	200/ -200	15	10^{-4}	-	-
	[4]	Pt-$Ce_{(1-x)}Gd_xO_x$-Pt	500	-	10/ -10	2×10^2	10^{-4}	50	-

However, using a single switching layer of CeO_2 mainly suffers from high power consumption and in many cases, the forming voltage is not reported and no long endurance over short pulses have been conducted. Several attempts have been carried out to enhance the CeO_2-based ReRAMs performances using UV treatment [3], doping [4] and interface engineering through deposition of metal buffer layer, for instance Al, Ti and Si [62, 78, 79]. Younis et al. [3] have studied the resistive switching characteristics of 5 % Gd-doped CeO_2 (CGO) in which they could achieve better resistance window of 10^4, lower operating voltage of (-2, 2 V) and the endurance of 10^4 by means of UV irradiations (Figure 2.4 (a)). However, the operating current stayed at the high range of 10 mA.

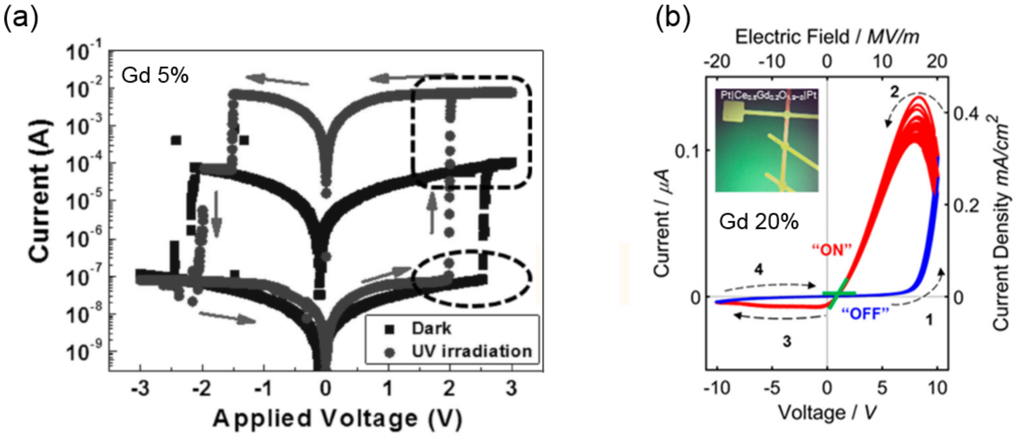


Figure 2.4 – I-V characteristics of (a) FTO/ CeO_x:Gd (10 %)/ Au ReRAM in semi-logarithmic scale under dark condition and under UV irradiation [3] and (b) Pt/ $Ce_{0.8}$ $Gd_{0.2}$ $O_{1.9-\delta}$ / Pt cross bar devices [4].

Furthermore, doping of CeO_2 with Gd have been reported to increase the concentration of oxygen vacancies as well as the ion mobility. Schmitt et al. [4] have investigated the effect of Gd dopant content on the oxygen vacancy configuration, referred as "free" versus "clustered", and on the final ReRAM performances. The highest ion conductivity is a trade-off between the vacancy concentration and how free they can migrate. They have achieved the maximum ion conductivity with 20% Gd which coincides with the highest resistance window at low operating current of 0.1 μA , see Figure 2.4(b). Nevertheless, high oxide thickness of 500 nm with high operating voltage of (-10, 10 V) are the features that are needed to be further optimized.

ZrO_2 (zirconia) is expected to show similar behavior to HfO_2, while the number of studies on ZrO_2-based ReRAM are so limited. The switching characteristics of ZrO_2-based ReRAM are listed in Table 2.4 in which the resistance window of 10^6, operation speed of (<10 ns) and endurance of 10^4 are the best-reported results [82]. The main issues of ZrO_2-based ReRAM are high forming and Set/Reset voltages [83, 84] that can be modified by doping with lower valance dopant such as yttrium (Y). Yttrium stabilized zirconia (YSZ) as a well-known ion conducting material has higher concentration of oxygen vacancy leading to smaller forming voltage. While encouraging results have been published, further studies are needed in order to confirm the potential of YSZ thin films to be used as a switching layer in ReRAM devices. In particular, the film thickness has to be further decreased as YSZ should retain its properties even at ultra-low thickness.

Table 2.4 – Review of ZrO_2-based ReRAM devices. "SR":Self-Rectifying, "less": Forming-less operation, "HRS": High Resistance State, "LRS": Low Resistance State, "DC": Direct current, "AC": Alternating current. "-":Not reported

Year	Ref.	Structure	Oxide thickness (nm)	Forming (V)	Set/ Reset (V)	HRS/LRS	I_{set} (mA)	Endurance (cycle)	Retention (s)
2010	[83]	Ti-ZrO-Pt	40	8	0.7/ -1.5	100	10 (SR)	10^3 (AC)	10^7
2011	[85]	Cu-ZrO-Pt	20	less	4.43/ -2	10^4	1	2.5×10^3	10^4
	[86]	W-YSZ-$Pr_{0.7}Ca_{0.3}MnO_3$-Pt	10	less	3/ -5	10^4	10^{-3} (SR)	200 (AC)	10^5
2014	[87]	Cu-ZrO-TaN	-	less	1.5/ 0.5	10^5	0.1	-	10^4
	[88]	Ti-ZrO-Pt	100	-	1.2/ -1.7	100	5	100	-
	[89]	Nb:$SrTiO_3$-YSZ-Pt	80	-	3/ -3	10^5	10	35 (AC)	10^3
	[90]	Au-YSZ-TiN	12	-3	3/ -2	100	10 (SR)	100	-
2015	[84]	Pt-ZrO-TiN	14	7-8	2-6/ 1-4	15	1	9×10^3	-
	[91]	Si-ZrO-Pt	5	-	-8/ 8	-	4×10^{-5}	-	-
2016	[92]	Au-Zr-YSZ-TiN-Ti	40	-5.5	-3.5/ 5.5	10^3	100 (SR)	10^3 (AC)	-
	[93]	Sb-YSZ-Zr-Au	40	-	-8.5/ 4.5	10^4	0.5	-	-

2.4 Chip-level ReRAM-CMOS co-integration

Concerning shrinking down obstacle in the CMOS technology, the hybrid integration of ReRAM with the CMOS circuitry opens up an opportunity to take the advantage of high yield and mature circuit functionality of CMOS with the high density feature of ReRAMs [15–17]. In addition, the integration of ReRAM as a passive circuit element with the active CMOS circuitry meet the requirements for neuromorphic computing circuit [18], reconfigurable logic [7] and analogue computations [19] applications. In the conventional CMOS-ReRAM co-integration (ex:1T1R configuration), ReRAM is integrated in the CMOS periphery required the costly hybrid technology [5], while integration of ReRAM on the foundry-produced CMOS dies can reduce the fabrication cost and increases the accessibility particularly for the research purposes. The manufacturing process for ReRAM briefly consists of BE/switching layer/TE deposited between the metal layers of CMOS as shown in Figure 2.5.

Different memory elements designs which have been proposed for ReRAM-CMOS integration are depicted in Figure 2.6. Figure 2.6(a) presents simple MIM ReRAM stacking deposited on the CMOS vias and followed by fabrication of the second vias on the ReRAM top electrode [5]. In Figure 2.6(b), the metallic via acts as a bottom electrode for ReRAM and the area of via beneath the oxide layer can be regarded as an effective memory size. Reducing via diameter scales down the ReRAM size [94]. This design results in reliable and low cost process. In Figure 2.6(c), via is used as the memory BE and a self-align oxide layer is formed through oxidation of the metallic via surface leading to simpler process compared to switching layer deposition and patterning [39, 40]. However, in this case, material oxide choices become limited. Figure 2.6(d)

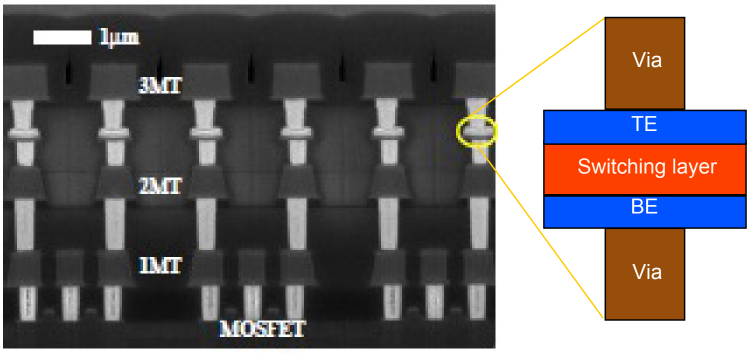


Figure 2.5 – TEM cross section micrograph of fully integrated ReRAM array in 180 nm technology [5]. the corresponding technology consists of the Al metal layers that are connected through the W vias. ReRAM stack consists of BE/switching layer / TE is embedded in the CMOS periphery.

shows concave structure for ReRAM [95] in which the memory element size can be reduced by reducing the concave area. Figure 2.6(e) is the cross-bar array structure where the oxide layer deposited all around on top of the CMOS chips and the memory size is defined by the width of TE or BE wires [96].

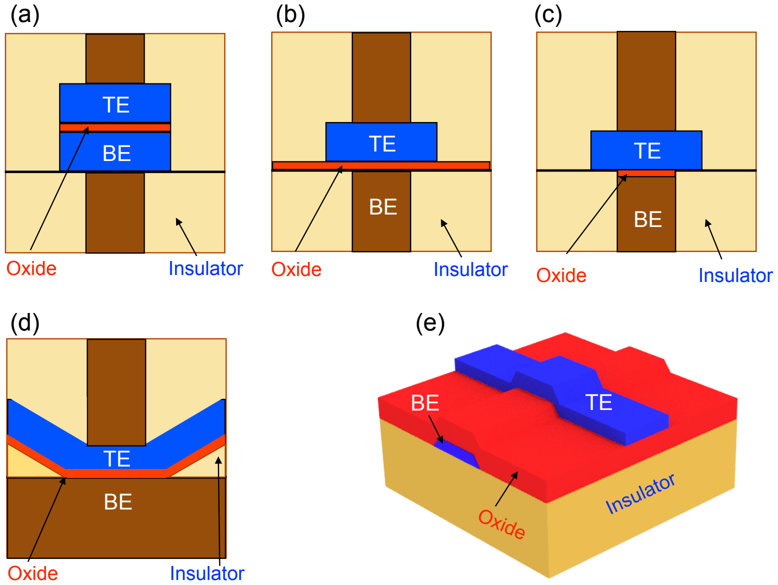


Figure 2.6 – (a) Typical MIM ReRAM structure in which all the memory parts are deposited between the CMOS metal layers. (b) The ReRAM elements on the metallic vias where via act as memory BE. (c) The via surface oxidation to form self-align switching layer. In both (b) and (c), the effective size of the ReRAM is defined by the size of CMOS via. (d) ReRAM with concave structure cell. (e) The cross-bar structure with BE and TE wires and the blanket switching layer. The width of electrode wires determines the effective size of memory array. Adopted from [6]

Recently, there has been an increasing amount of studies on embedding ReRAM on the back end of line (BEoL) of the foundry-produced CMOS chips [7–9, 40, 97]. In 2009, Xia et al. [7] reported successful 2D hybrid ReRAM integration on top of the foundry-produced CMOS 500 nm technology chip with the FPGA-like functionality using nano imprint lithography (NIL) technique. However, their process for building the memristor crossbars requires several steps of polishing and UV radiation to planarize the respective surface which makes it a complex and expensive embedding technique, see Figure 2.7(a-c). The electrical characteristics (Figure 2.7(d)) reveals a small resistance ratio of (HRS/LRS: 40 kΩ/ 20 kΩ) with the relative high operating voltage of (-4 to 10 V). They have also fabricated a stand-alone ReRAM with the same cross-sectional junction geometry which switches with the resistance ratio of 10^3 and the operating voltage of (-2 to 2 V). The significant difference between ReRAM performances on the Si wafer and in the CMOS periphery exhibits the profound impact of CMOS post-processing on the final device performance.

In 2016, Sandrini et al. [8], proposed the MMC-based (Metal to Metal Capacitor) integration prototype with the dedicated CMOS 180 nm circuitry. Although, they simplified the integration technique, the device performance was unstable. The local field enhancement caused by the shape of MMC structure is the main reason behind device instability. Moreover, they have

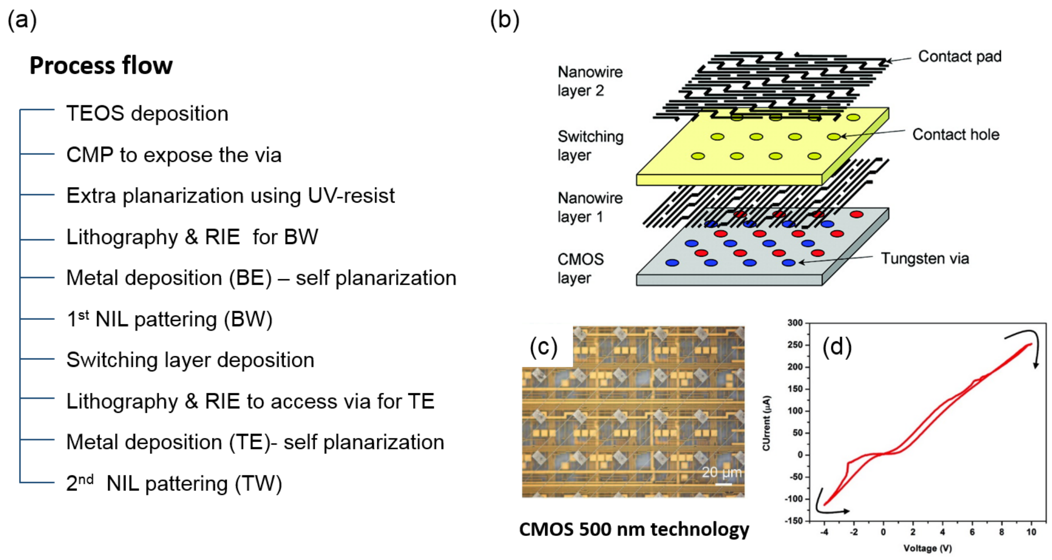

(a)
Process flow
TEOS deposition
CMP to expose the via
Extra planarization using UV-resist
Lithography & RIE for BW
Metal deposition (BE) – self planarization
1st NIL pattering (BW)
Switching layer deposition
Lithography & RIE to access via for TE
Metal deposition (TE)- self planarization
2nd NIL pattering (TW)
(b)
Nanowire layer 2
Switching layer
Nanowire layer 1
CMOS layer
Contact pad
Contact hole
Tungsten via
(c)
20 µm
CMOS 500 nm technology
(d)
CUrrent (µA)
300
250
200
150
100
50
0
-50
-100
-150
Voltage (V)
-4
-2
0
2
4
6
8
10

Figure 2.7 – (a) Process flow of the cross-bar array ReRAM-CMOS integration. (b) Schematic illustration of the memristor-CMOS hybrid architecture. W vias (red and blue) from the CMOS periphery are employed as the area interface between the transistors and the memristor. The red vias are connected to the memory BE wires while the blue vias are dedicated to the TE wires. The crossbar array memory consists of switching material which is sandwiched between TE and BE nano-wires. (C) An optical micrograph of the hybrid ReRAM arrays on CMOS 500 nm technology. (d) I-V characteristics of a hybrid memristor from a two-wires measurement [7].

proposed to use the metal layers from the CMOS which limits the choice of electrodes. The device geometry, as well as the integrated ReRAM performances are presented in Figure 2.8(a). It can be observed that the memory switches with low operating voltage of (-1 to 1.5 V) but at the high operating current of 10 mA. No endurance cycling has been reported.

Later 2016, we have reported [40] a W-based technique to co-integrate ReRAM with 180 nm fully finished CMOS chips. W/WO$_x$/TiN was fabricated through the mask-free thermal oxidation of W vias at 400 ∘C inside the CMOS chips. Employing CMOS's W via as BE avoids the need for an extra CMOS compatible BE deposition and patterning. nm-scale feature of vias defines the effective size of the final device. Finally, W is a low-work function metal that with the appropriate material combination can be used as high carrier injection cathode for the electronic switching mechanism rather than ionic one which reduce the power consumption and improves the reliability issue [98].

Chakrabarti et al. [9] in 2017 extended the Xia et al. [7] 2D planar prototype and reported the first reconfigurable chip level 3D CMOl hybrid circuits. However, the complexity of the process due to the e-beam lithography, CMP, and polarization steps is still remaining. They lowered

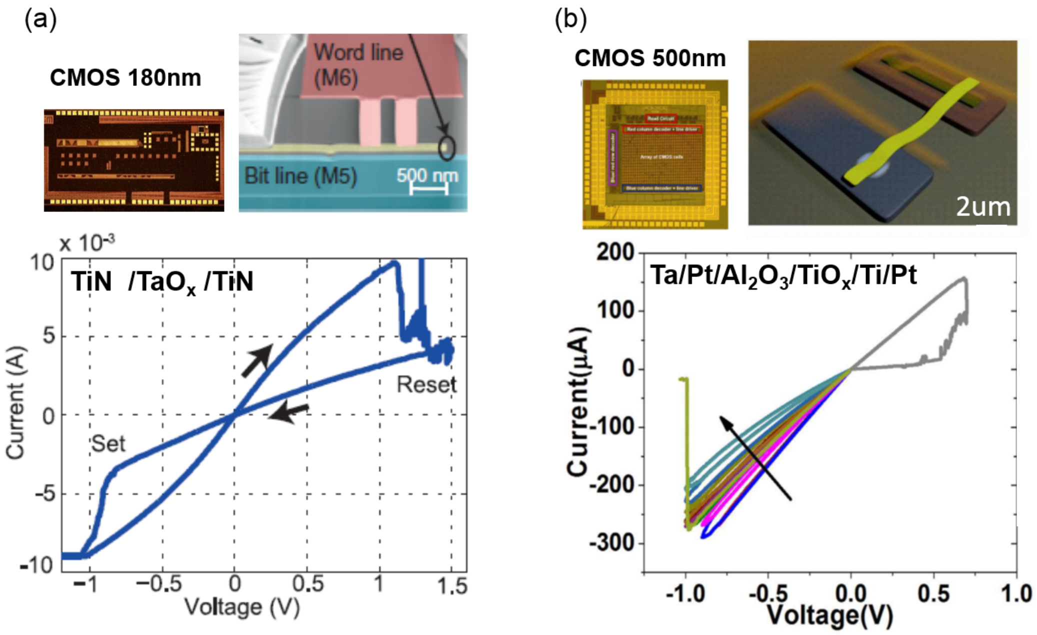


Figure 2.8 – (a) MMC hybrid ReRAM devices on CMOS 180 nm technology presented by [8]. (b) Reconfigurable chip level 3D CMOl/ReRAM hybrid proposed by Chakrabarti et al. [9].

the operating voltage down to (-1 to 0.8 V) with 150 μA but at the cost of low resistance window particularly in Reset. The electrical characteristics as well as the device geometry of the hybrid ReRAM/CMOS devices are presented in Figure 2.8(b).

3 W-based stand-alone ReRAM

In this chapter, the impact of W electrode on ReRAM performance has been investigated. We have engineered the W electrode interface with an in-depth understanding of W electrochemical properties targeting the better control on ReRAM switching properties. To achieve an insight understanding of W electrode properties and its impact on ReRAM performances, the well-established materials, i.e. HfO_2 *and Pt were utilized as the switching layer and inert electrode, respectively. The study has been performed on the stand-alone cross-point memory cells avoiding the complication arise from the material and processing issues. First, W has been studied as top electrode to avoid the effect of processing on W properties and oxidation (Section 3.1). The results are presented in the format of paper that is submitted for the publication. Furthermore, the multi-storage capability of* $(Pt/HfO_2/Ti/W)$ *has been also carefully investigated by tunning the resistance states with the Reset pulse voltage (Section 3.2). Finally, we have studied W as the bottom electrode for better simulation of CMOS configuration. In order to minimize the processing effect on W, both electrodes have been patterned by shadow mask (Section 3.3). The output of the studies is published as IEEE Xplore (DOI: 10.1109/PRIME.2018.8430371)*

3.1 Switching kinetics control of W-based ReRAM cells in transient operation by interface engineering

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Authors contribution: ES conceived the research, developed the fabrication process, produced the samples, participated in the electrical and material characterization, data analysis and wrote the manuscript. CG was involved in the paper preparation, proposed the switching conduction mechanism, participated in the electrical characterization and data analysis and wrote the manuscript. MH performed the material characterization, analyzed the corresponding data and revised the manuscript. MR contributed in the device fabrication and statistical electrical measurements. CR supervised the theoretical part and revised the manuscript. YL supervised the research and revised the manuscript.

Switching kinetics control of W-based ReRAM cells in transient operation by interface engineering

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Abstract

Tungsten is one of the most promising material to be used as ReRAM electrode for its low work function and CMOS-compatibility with the prospect of device integration, scalability, and low-power consumption. However, W has multiple oxidation states which affect the device reliability due to the formation of semi-stable oxides at the switching layer/electrode (HfO_2/W) interface. In this study, we have modulated the tungsten chemical interaction through the insertion of Al_2O_3 or Ti interfacial layers. The time-dependent switching kinetics is investigated in a transient Set/Reset operation. We have observed that the compact stoichiometric ALD-deposited Al_2O_3 barrier layer prevents completely W oxidation, resulting in a sharp current transient in the Reset operation. While, the use of a sputtered Ti buffer layer allows a partial W oxidation, defining a tunable HRS by pulse rise time control. Notable improvements in endurance, power consumption, resistance state stabilization, cycle-to-cycle and device-to-device variability are reported. Moreover, switching kinetics and conductive nano-filament (CNF) evolution is studied in details to understand the microscopic effect of the interface modifications. The tunability of multi-HRS states by pulse timing control in Pt/HfO_2/Ti/W is indeed in the interest of network and brain-inspired computing applications, adding a degree of freedom in the modulation of its resistance.

Introduction

The recent advancement of resistive-switching random access memories (ReRAM) in material functionality [99] , switching kinetics analysis [100, 101] , design and fabrication processing [102–104] is raising the prospect of developing these devices as a promising replacement to the NAND-type flash memories. Simple structure, great scalability, high device density and CMOS-compatibility are the key features of ReRAMs for many different applications such as neuromorphic computing system and FPGA-like functionality [82, 105, 106] . A ReRAM cell is a two terminal device whose memory principle depends on resistive switching between at least two different resistance states through an application of suitable stimuli, i.e. a low resistance state (LRS) and a high resistance state (HRS). In bipolar ReRAM, the change from HRS to LRS (Set process) is driven by a proper voltage, while the reverse operation from LRS to HRS (Reset process) occurs at the opposite polarity. The ReRAM basic structure consists of a metal-insulator-metal (MIM) stack, in which an insulator layer responsible for resistive switching is sandwiched between two electrodes. For the metal-oxide based bipolar ReRAMs, HfO_2 [103, 107] , TaO_x [108, 109] and TiO_2 [110–112] are among the most studied and preferred switching layers. For the electrodes, an asymmetrical configuration is employed, where one is an oxidizing electrode with a low work function (W, Ta, Ti and Hf) and the other has rather higher work function and lower chemical reactivity (Pt, TiN, ...) [113–116] . The most common resistive switching mechanism in metal-oxide is a filamentary type [117] , which is defined by the generation and annihilation/rupture of the conductive nano filament (CNF) along the path from one electrode to the other. In valance change memory (VCM), the CNF is made of the sub-stoichiometric oxide with high density of oxygen vacancies ($V_{\ddot{O}}$, following the $kr\ddot{o}ger - vink$ notation [118]). These $V_{\ddot{O}}$ are created by the migration of the O^{2-} ions towards the electrodes by the application of a voltage, which introduces a valance change of the metal in the metal-oxide layer (initial forming process). In the following repetitive Set and Reset operation, the created CNF is partially formed/ruptured. Therefore, improving methods that can control the oxygen ion migration at the atomic scale is an essential and fundamental requirement for the further optimization and engineering of ReRAM devices. Extensive studies with different approaches have been carried out to control the ion migration and corresponding switching operation. They can be mainly categorized as: material engineering [47, 115, 119, 120] and electrical stimulation control of devices [121–123] . Regarding the material engineering, interface modification is mostly proposed using oxygen barrier layers, e.g. Al_2O_3, and oxygen scavenging electrodes, e.g. Ti. It has been shown that these additional layers can strongly influence switching dynamics in both forming [124–126] and Reset operations [115] . In case of electrical stimulation parameters, local temperature and electrical field- the driving forces of ion migration- can be controlled by the device voltage/current amplitude [123, 127–129] . One needs to take into account that these two approaches are strongly correlated, meaning that modulation of the device performance through any specific electrical parameters has to be consistent with the electrodes/oxide electrochemical properties. Appropriate criteria are requested in order to select suitable materials. Gou et al proposed to calculate the energy required for the formation of oxygen vacancy defects (E_{vo}) in an oxide layer for different ohmic metal cap [44, 130]. Another approach is to evaluate the exchange ability of the different ohmic electrodes using the oxidation reactivity of metals by the Gibbs free energy (ΔG) [131] . Among the common ohmic electrodes, tungsten as the most CMOS compatible material [40] has interesting and special oxidation properties. Note that W is used as the material of choice in numerous back end of line (BEoL) processes for vertical vias between adjacent layers in the metal stacks. When W is exposed to an oxidizing environment, it can develop large variety of oxide forms, WO_2, $WO_{2.72}$ ($W_{18}O_{49}$), $WO_{2.90}$ ($W_{20}O_{58}$), $WO_{2.96}$ ($W_{50}O_{148}$) and WO_3 [55] . Each of these oxide reactions is ascribed to a specific free energy of formation (ΔG_f) that defines the thermodynamic stable condition of W oxidation. Depending on the energy provided to the W electrode during the ReRAM operation, it transforms with sequential and spontaneous oxidations from the meta-stable WO_2 to the most thermodynamical stable WO_3. However, an elaborative study on the effect of WO_x physical properties on the control of the switching kinetics is still missing.

In this study, the time-dependent switching kinetics of W-based ReRAMs is investigated in transient Set/Reset operation. For the ReRAM stacks, Pt is employed as an inert electrode and HfO_2 as oxide switching material. In order to analyze the pure W oxidation properties on switching, ($Pt/HfO_2/W$) devices are fabricated and tested, where W acts as both electrode and oxygen exchange layer. Then, the effect of W oxidation is modulated by the insertion of Al_2O_3 and Ti. The presence of Al_2O_3, prepared by atomic layer deposition (ALD) with high uniformity and strong oxygen immunity [47, 120], prevents the W electrode remote scavenging at the HfO_2/W interface. On the other hand, in case of Ti buffer layer incorporation, W electrode partially contributes in switching kinetics by diffusing/penetrating through sputtered Ti film. We have observed that the incorporation of both Ti and W in the switching kinetics enables a gradual Reset operation via pulse time programming. Our finding suggests that the Reset kinetics can be controlled precisely through time modulation by involving two ohmic electrodes with different oxidation rates.

Results and discussion

Electrical characterization and response comparison

Three stacks of ReRAM have been fabricated, ($Pt/HfO_2/W$), ($Pt/HfO_2/Al_2O_3/W$) and (Pt/HfO_2 $/Ti/W$) , in which the HfO_2 and Al_2O_3 are deposited by ALD and the rest are sputter-deposited. The structure is defined based on the conventional photo-lithography process (see method section), as shown in Figure 3.23.

The DC electrical characterizations of the stacks are reported in Figure 3.2(a-c). A positive voltage sweep from 0 V to 7 V with a current compliance (I_{cc}) of 1 mA is applied to form the initial conductive nano filaments (CNF) in the switching layer. The same I_{cc} value for all three stacks is applied to have a correct performance comparison. The extracted forming voltages for ($Pt/HfO_2/W$), ($Pt/HfO_2/Al_2O_3/W$) and ($Pt/HfO_2/Ti/W$) ReRAMs are 3.25 V, 5.65 V and 2.57 V respectively (SI 1). During the DC measurement, the voltage is swept from 0 V → -1.5 V → 0 V → 3 V → 0 V on the W top electrode while Pt bottom electrode is grounded. All the devices show a bipolar switching behavior, with Set in positive and Reset in negative polarity. For the ($Pt/HfO_2/W$) Set (cycle in Figure 3.2(a)), a positive voltage of 2.8 V is required, while for the Reset operation, the memory switches from LRS to HRS showing two intermediate steps at -0.9 V and -1.5 V with a high overshoot current. Reset current overshoot is caused due to

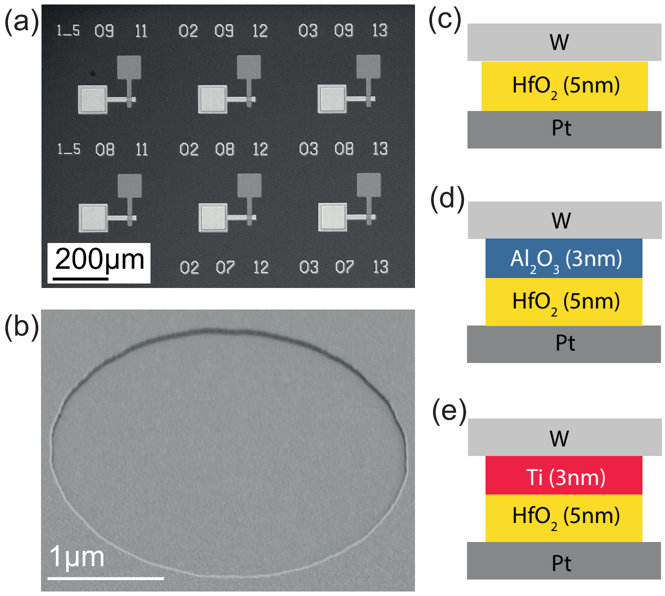

Figure 3.1 – (a) Optical image of the fabricated devices and (b) SEM micrograph on active device area (via) with the dimension of 3 μm. Schematic structure for (c) (Pt/HfO$_2$/W), (d) (Pt/HfO$_2$/Al$_2$O$_3$/W) and (e) (Pt/HfO$_2$/Ti/W).

the large value of the V$_{Set}$ that makes the fast current rising (in range of few μs) before the current limiting tool can overcome the voltage drop across the circuits [132]. Moreover, this device tends to show high current fluctuation through the Set operation before the abrupt Set occurs. To address such a behavior, the effect of W electrode at the HfO$_2$/W interface has to be considered, for its complex correlation with oxygen. During Set, before the formation of a CNF, there is a stochastic creation of V$_{\ddot{O}}$ due to sequential and spontaneous W oxidations, which are not sufficient to trigger the complete Set. The Reset current overshoot and the fluctuations in Set operation decrease the device reliability and cause a fast degradation in device performances. The insertion of an additive layer between W and HfO$_2$ modulates the W contributions, defining different switching kinetics to tune the electrical functionality. (Pt/HfO$_2$/Al$_2$O$_3$/W) in Figure 3.2(b) switches from HRS to LRS with positive Set voltage of $\sim$ 2 V. By applying a reverse voltage polarity, the LRS retains its level until -0.9 V when the first deep Reset occurs and the HRS value remains unchanged until -1.5 V. Country to the (Pt/HfO$_2$/W) samples, no current fluctuation is observed in the Set operation and the Reset overshoot current is reduced significantly. In Figure 3.2(c), (Pt/HfO$_2$/Ti/W) sample switches to LRS at $\sim$ 1 V while it stays till -0.4 V and gradually switches back to HRS at higher applied voltages. The current is uniform and stable through the ReRAM operation and the maximum Reset current is equal to I$_{cc}$.

In order to quantify the effects of Al$_2$O$_3$ and Ti, extensive statistical analyses are conducted. The calculated device to device (D2D) variabilities on 5 devices per stack are available in SI

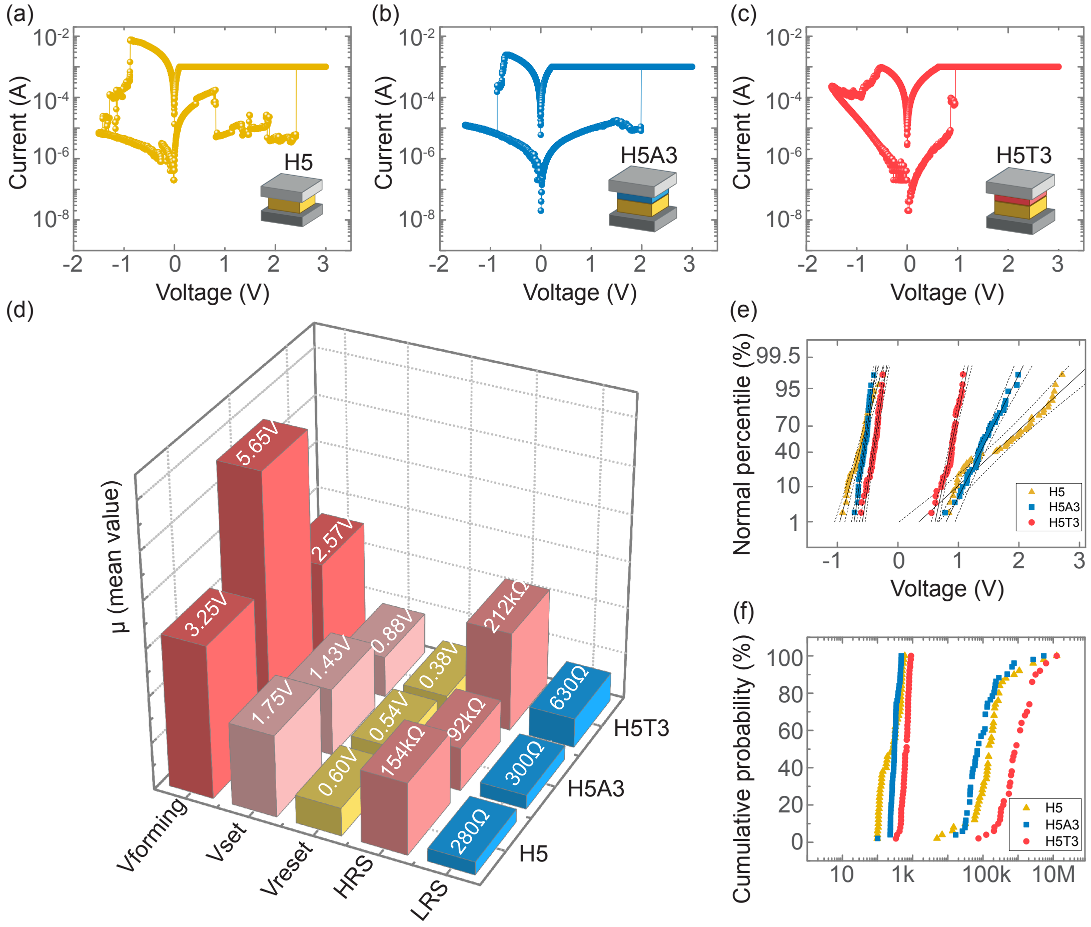

Figure 3.2 – DC bipolar I-V switching curve obtained from (a) H5: (Pt/HfO_2/W), (b) H5A3: (Pt/HfO_2/Al_2O_3/W) and (c) H5T3: (Pt/HfO_2/Ti/W). (d) Statistical mean value analysis 3D plot of $V_{forming}$, V_{Set}, V_{Reset}, HRS and LRS over 100 cycles for H5, H5A3 and H5T3. Cumulative distribution of (e) V_{Set}/ V_{Reset} with standard deviation fit in gray dash line and (f) HRS /LRS for H5, H5A3 and H5T3 measured at V_{read} = 0.25 V

2. Regarding the cycle to cycle (C2C) variability, the mean value (μ) and normal standard deviation (σ) of $V_{forming}$, V_{Set}, V_{Reset}, HRS and LRS are evaluated over 100 cycles per each stack. The μ values are graphically shown in Figure 3.2(d) and σ values are presented in SI 3. The comparison between (Pt/HfO_2/W) and (Pt/HfO_2/Al_2O_3/W) shows that the insertion of Al_2O_3 increases forming voltage from 3.25 V to 5.65 V, originated by the barrier properties of Al_2O_3 [120] . Moreover, ALD deposited Al_2O_3 film has stronger chemical bonding, compared to the HfO_2 film [120, 133]. This results in lower vacancy concentration in Al_2O_3 rather than in HfO_2. In Reset with the negative bias, the small number of $V_{\ddot{O}}$ in the Al_2O_3 are efficiently recombined resulting in lower Reset voltage (-0.54 V) compared to (Pt/HfO_2/W) (-0.60 V). Due to the partial rupture of CNF at HfO_2/Al_2O_3 interfaces, lower energy is needed to recreate the filaments during the Set process. Recorded Set voltage, 1.43 V, is 20% lower than

(Pt/HfO_2/W), 1.75 V. The LRS value remains higher in (Pt/HfO_2/Al_2O_3/W) (300 Ω) compared to the (Pt/HfO_2/W) (280 Ω) and the HRS is lower (92 kΩ) with respect to (Pt/HfO_2/W) (154 kΩ) in agreement with the CNF formation/rupture dynamics (see conduction mechanism section). Considering the Ti insertion, (Pt/HfO_2/Ti/W) shows the lowest forming voltage of 2.57 V. According to the ab-initio calculation reported by Chen et al [134], based on Eq.3.1, cap metal (M) scavenging ability can influence $V_{forming}$.

$$\mathrm{M(bulk)} + \mathrm{HfO_2} \longrightarrow \mathrm{MOx} + \mathrm{HfO_x} + \mathrm{Vox} \tag{3.1}$$

The energy levels required to create the WO_x and TiO_x with 25% oxygen atomic percentage are 7 eV and 1 eV respectively [134]. This indicates that Ti has much stronger thermodynamic ability to draw oxygen out of HfO_2 compared to W electrode and creates more $V_{\ddot{O}}$ leading to lower $V_{forming}$. The more efficient oxygen exchange of Ti during the Set/Reset results in smaller V_{Set}/V_{Reset} (0.88 V/-0.38 V). During the Reset operation, fast TiO_x reduction with high O^{2-} mobility inside the HfO_2 layer results in large filament gap formation and deep HRS value of 212 kΩ, which is extensively explained in conduction mechanism section. The cumulative distributions of V_{Set}/V_{Reset} and LRS/HRS for three samples are plotted in Figure 3.2(e,f) respectively. In all cases, the variations of the V_{Reset} is smaller compared to V_{Set}. It is evident that the insertion of Al_2O_3 or Ti layer at the HfO_2/W interface improves both switching voltage and resistance uniformities. HRS and LRS data retentions of both (Pt/HfO_2/Al_2O_3/W) and (Pt/HfO_2/Ti/W) devices at room temperature are presented in Figure 3.3(a,b) proving the non-volatility of the memories by the absence of resistance drifts.

In order to elaborate the role of W in switching kinetics after the electrode-oxide interface engineering by insertion of the two different layers, a comprehensive electrical characterization is required. For this purpose, pulse measurements have been carried out on the three different stacks, in which the switching is controlled by consecutive positive (Set) and negative (Reset) pulses with programmable amplitude and width. The reading is performed by a voltage ramp from 200 mV to 250 mV. The (Pt/HfO_2/W) endurance degrades after 150 cycles (SI 4) and no controllable switching is achieved by pulses with width ≤ 1ms. This underlines the importance of the HfO_2/W interface engineering. The pulse endurance characteristics of (Pt/HfO_2/Al_2O_3/W) and (Pt/HfO_2/Ti/W) over 10^4 are presented in Figure 3.3(c,d) respectively. In order to prolong ReRAM endurance lifetime, it is important to optimize appropriate Set/Reset pulse conditions [135]. For both devices, Reset/Set voltage pulses of -2 V/2.5 V with a slope of 20 % are applied. The pulse width and I_{cc} for (Pt/HfO_2/Al_2O_3/W) and (Pt/HfO_2/Ti/W) are adjusted to (1 ms, 1 mA) and (5 μs, 500 μA) respectively. No degradation is observed for both devices after 10^4 cycling. (Pt/HfO_2/Al_2O_3/W) (Figure 3.3(c)) switches with HRS variation between 100 kΩ to 10 MΩ and uniform LRS of 2 kΩ, while (Pt/HfO_2/Ti/W) (Figure 3.3(d)) cycles with more stable HRS (~ 10 MΩ) and LRS value of 3 kΩ in agreement with their DC

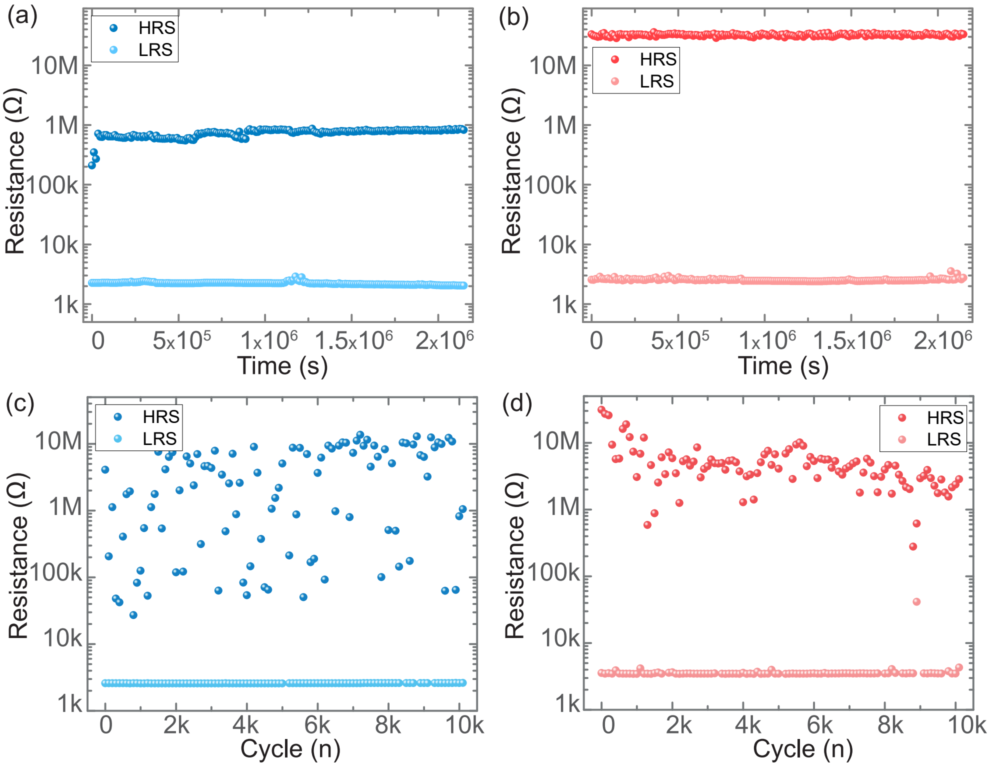

Figure 3.3 – HRS and LRS data retention at room temperature (a) (Pt/HfO_2/Al_2O_3/W) devices and (b) (Pt/HfO_2/Ti/W)devices, reading performed every 2 min. 10^4 pulse endurance of (c) (Pt/HfO_2/Al_2O_3/W) device (V_{Set}/ V_{Reset} = -2 V/2.5 V, I_{cc}= 1 mA, Pulse width = 1 ms and Pulse slope = 20 %) and (d) (Pt/HfO_2/Ti/W) device (V_{Set}/ V_{Reset} = -2 V/2.5 V, I_{cc}= 500 μA, Pulse width = 5 μs and Pulse slope = 20 %).

performance characteristics. It is evident that (Pt/HfO_2/Ti/W) is capable to switch with much faster pulses and higher HRS uniformity.

Pulse time effect on the resistance states of (Pt/HfO_2/Al_2O_3/W) and (Pt/HfO_2/Ti/W) are further investigated by stimuli with different pulse width (5, 10, 50, 100, 500 and 1000 μs) and different pulse slopes (10 % to 50 %). Several consecutive endurance tests are performed, changing the pulse width and slope in order to cover all the possible combinations. Width is varied every 100 cycles whereas slope is changed every 600 cycles. Figure 3.4 reports the HRS and LRS mean values and standard deviations for each set of data (100 cycles) per each slope. An overview of these measurements is available in the SI 5. To define a single factor including the impact of both pulse width (W_p) and slope (S_p) information, the rise time (t_r) is introduced, i.e. $t_r = W_p \times S_p$ and the resistance state dependence by rise time is displayed. In (Pt/HfO_2/Al_2O_3/W) (Figure 3.4(a)), LRS is recorded as 2 kΩ without any significant change depending on rise time. Regarding HRS, with very steep pulse slope (< 20 %) or the extended ones (≥40 %), the device performance is attenuated with higher number of resistance failure.

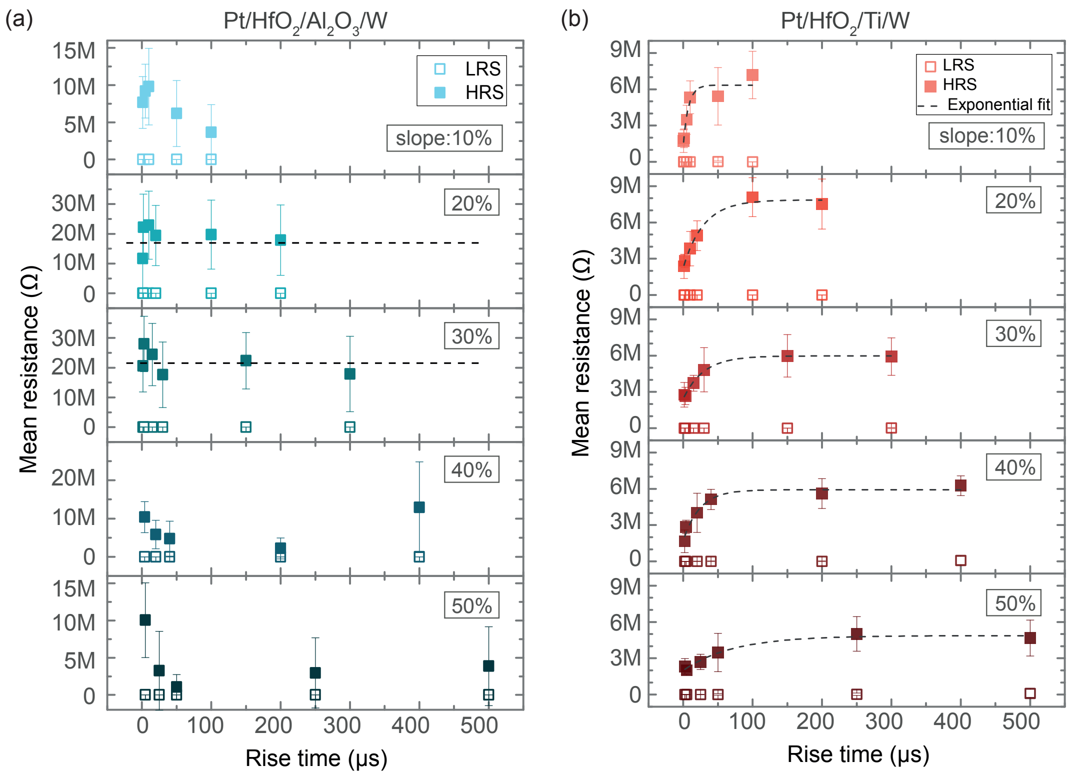

Figure 3.4 – (Pt/HfO$_2$/Al$_2$O$_3$/W) (a) and (Pt/HfO$_2$/Ti/W) (b) mean values and standard deviations on 100 consecutive pulse cycles for different pulse widths and slopes; V$_{Set}$ is fixed at 2.5 V, V$_{Reset}$ at -2 V and I$_{cc}$ at 1 mA.

With the pulse slopes of 20% and 30%, the devices perform with better resistance states uniformity and HRS does not change with respect to the rise time. A different behaviour is notable for (Pt/HfO$_2$/Ti/W) (Figure 3.4(b)). LRS remains constant at ~ 2 kΩ, while HRS increases by increasing the rise time. Distinct HRS states are achievable by the precise tuning of the rise time factor and analytically a log curve fits the HRS versus the rise time. The tunability of multi-HRS states by pulse timing control makes the devices a good candidate for neural network and brain-inspired computing applications, adding a degree of freedom in the modulation of its resistance. The gradual HRS change has not been observed in devices without W electrode ((Pt/HfO$_2$/Ti/TiN) - SI 6), suggesting that the W plays a crucial role in the device electrical response.

This is further supported by the current measurements for different pulse timing presented in Figure 3.5. The current that flows through the circuit is evaluated by the insertion of a series resistance using the oscilloscope (more details in methods). The complete inhibition of W in the case of (Pt/HfO$_2$/Al$_2$O$_3$/W) (Figure 3.5(a)) determines an abrupt current variation, which does not depend on the applied energy since the filament rupture point is strongly confined. Whereas, in case of (Pt/HfO$_2$/Ti/W) stack, a gradual current variation and a reduced final HRS

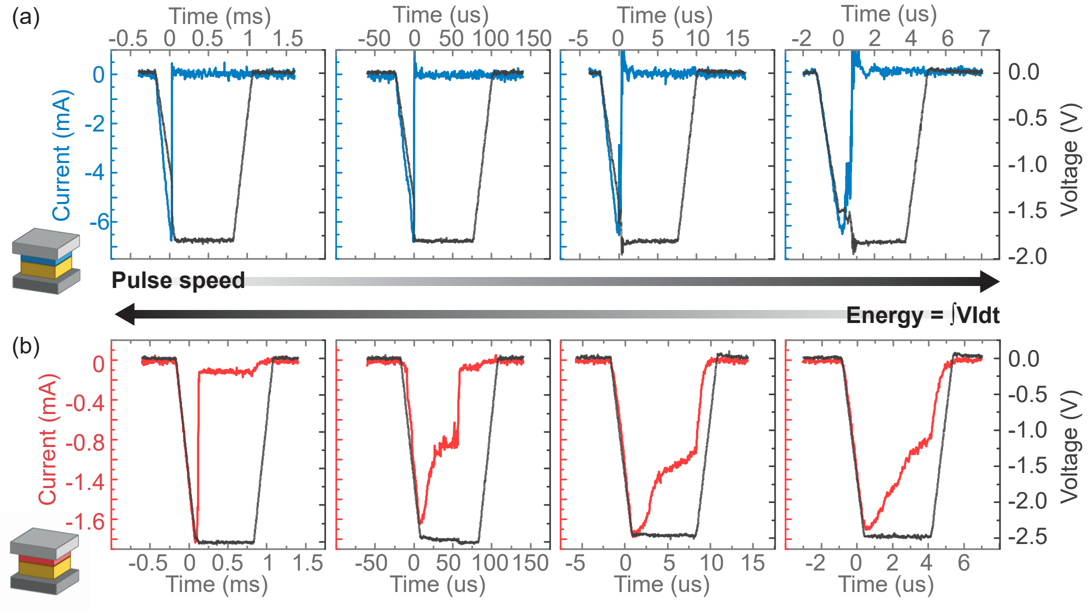

Figure 3.5 – Current evaluation during Reset pulse operation depending on pulse timing. The (Pt/HfO_2/Al_2O_3/W) and (Pt/HfO_2/Ti/W) device responses are presented in (a) and (b) respectively for 1 ms, 100 μs, 10 μs and 5 μs pulse widths and 20% slope. The applied voltages are targeted considering the series resistaces used to measure the current (R = 50 Ω for (Pt/HfO_2/Al_2O_3/W) and R = 1 kΩ for (Pt/HfO_2/Ti/W)).

are notable when the pulse rise time decreases (Figure 3.5(b))).

The Set characteristics of this device are also evaluated using two quantified parameters, (i) switching time and (ii) Set voltage (inset Figure 3.6). The switching time is defined as the time interval between the pulse start and the moment when abrupt change in current is visible and the Set voltage is evaluated as the V value in correspondence of the current change. The dependence of switching time and Set voltage on the rise time are reported in Figure 3.6(a,b). The required voltage to complete the Set operation does not change with respect to the rise time while the switching time linearly increases with the rise time. The trends confirm that the Set operation is a snap process driven by the applied voltage, which starts when enough energy for ion motion is provided across the oxide layer. When the filament is formed, the I_{cc} controls the size growth of the CNF, limiting internal temperature and electric field. This voltage dependency makes the Set process less suitable to be used for gradual resistance control over pulse time.

Conduction mechanism

The variation in CNF dynamic and oxygen exchange phenomenology in different stacks are inspected, to understand the Reset dynamics. When W is directly in contact with HfO_2 oxide

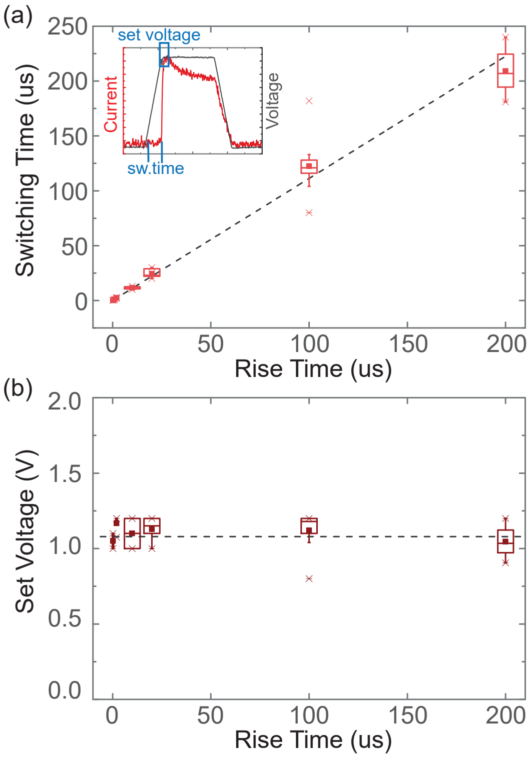

Figure 3.6 – Switching time (a) and voltage (b) versus rise time during Set operation for (Pt/HfO_2/Ti/W) stack. For all the measurement the V_{Set} is fixed at 2.5 V, the V_{Reset} at -2 V and I_{cc} at 500 uA.

layer, by applying a positive voltage, O^{2-} ions migrate towards the HfO_2/W interface and create a thin WO_x layer on the electrode side and an oxygen-deficient area at the oxide layer. The oxygen deficient layer in the oxide acts as the initial points for the conductive filament formation. However, since W oxidation reaction does not reach its steady state as fast as other active metal such as Ti and Hf [136, 137] , a large number of vacancies accumulate in the active layer leading to possible multi-filament formation/rupture. This causes CTC variability and fast device degradation as shown in Figure 3.2. Upon sufficient delivery of O^{2-} and thermal energy, W reaches to its stable oxide state (WO_3) and the reduction reaction is not thermodynamically favorable. The creation of a stable WO_x compound traps the oxygen and partially blocks the exchange at the interface. This results in low switching speed and high energy requirement in Reset operation. In this context, the insertion of an additive layer between W and HfO_x partially or completely inhibits the metal-active oxide layer interaction and affects the filament dynamics and the conduction mechanism. The switching mechanism for both (Pt/HfO_2/Al_2O_3/W) and (Pt/HfO_2/Ti/W) have been investigated.

Concerning the insertion of a barrier layer, Al_2O_3 has been selected due to its high potential barrier, low oxygen diffusion coefficient and high reduction energy [47, 138] . The comparison between the Gibbs free energies (ΔG) of Al_2O_3 and HfO_2 (-1582 kJ/mol and -1010 kJ/mol

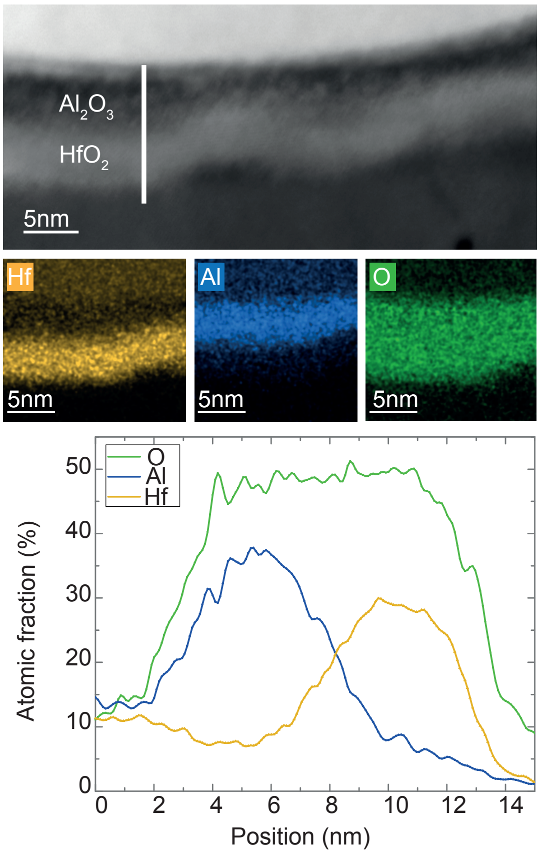

Figure 3.7 – HRTEM-EDX cross-sectional images of the ALD deposited HfO_2 (5nm) / Al_2O_3 (3nm) bilayer in the memory stack. Distribution of the aluminum (Al), hafnium(HF) and oxygen (O) composition along the entire line-scan are plotted.

respectively) [139] clearly shows that HfO_2 has higher number of weak oxo-ligand bounds which facilitate the creation of $V_{\ddot{O}}$. This is based on the assumption that both oxides are stoichiometric and amorphous, as it is proved by the TEM-EDX analyses presented in Figure 4.21. Once the O^{2-} ions are created inside the oxides, the movement is highly hindered in the Al_2O_3 layer, due to the lower oxygen diffusion coefficient [140, 141] . The result of forming process is the formation of an asymmetric filament, where the maximum $V_{\ddot{O}}$ density is concentrated in the BE/HfO_2 interface while the interface between HfO_2/Al_2O_3 acts as constriction point for filament rupture and creation (Figure 3.8(a)). In order to investigate in details the filament dynamic during the Reset, the IV curves have been fitted in $ln(|I|)$ - $1/|V|$ scales, revealing a good accordance with the Trap-Assisted Tunneling (TAT) transport mechanism (SI 7). In this model, the current density is defined by:

$$J_{TAT} = A\,exp\left[\frac{-8\pi\sqrt{2qm^*}}{3hE}\,\phi_T^{3/2}\right] \tag{3.2}$$

where A is a constant, q is the elementary charge, m^* is the effective mass, h is the Plank constant, E is the electric field and ϕ_T is the energy value of the traps with respect to the conduction band of Al_2O_3. It is assumed that during the Reset, the carrier drift is mediated by defects-generated trap states in proximity to the HfO_2/Al_2O_3 interface. The confined density of $V_{\ddot{O}}$ in the Al_2O_3, allows the movement of a small number of ions to easily break/rebuild the filament, leading to a sharp change in current during Reset. The main consequence of the sharp Reset is an attenuated control on HRS over time which is shown in Figure 3.4(a). The Al_2O_3 constriction in CNF shape and dynamics affects the resistance states: LRS increases due to the reduced filament diameter, while HRS does not reach a deep value compared to (Pt/HfO_2/Ti/W), due to the partial filament rupture at the confined point(Figure 3.2(f)).

The use of Ti as an oxygen reservoir layer is due to the low energy required for oxygen extraction, as quantified by its ΔG value of -883.3 kJ/mol [142] . The forming provides sufficient energy to thermodynamically activate the oxidation reactions at the HfO_2/Ti interface. Ti oxidation process determines an increase of the $V_{\ddot{O}}$ density in HfO_2 close to the Ti layer, which initiates the filament formation. At the HfO_2/Ti interface, a thin TiO_x layer is formed. Therefore, it is expected the formation of a conic-shape filament with a $V_{\ddot{O}}$ concentration gradient from the HfO_2/Ti interface to the Pt/HfO_2 one (Figure 3.8(b)). The efficient oxygen exchange at HfO_2/Ti and the high $V_{\ddot{O}}$ concentration in the oxide layer enhance the HRS/LRS window and resistance states stability (Figure 3.3(d)). Due to the less reactive nature of the BE material in comparison to Ti, the Pt/HfO_2 junction can be modeled as Schottky-like contact. When a negative voltage is applied and the Reset occurs, the migration of the O^{2-} towards the BE interface forms the Schottky barrier. A confirmation of the accuracy of Schottky model in experimental I-V curves description is given by the data fits reported in SI 7, following the equation:

$$J_{SD} = \frac{4\pi q m^{*}(kT)^{2}}{h^{3}}\, exp\left[\frac{-q(\Phi_B - \sqrt{qE \backslash 4\pi\epsilon})}{kT}\right] \tag{3.3}$$

where ϵ is the oxide permittivity, k is the Boltzmann constant, T is the temperature and ϕ_B is the barrier height. Applying a negative voltage, increases the Schottky barrier at the Pt/HfO_2 interface which results in a gradual change of the current through the device [113] .

Finally, to confirm the role of partial interaction of W through Ti buffer layer, the surface morphology of the samples has been analyzed using atomic force microscopy (AFM). The AFM map on Pt/HfO_2(5nm)/Ti(3nm) (Figure 3.8(c)) reveals that the peak to peak roughness of the surface is about 3-4 nm, which is basically transfered from Pt BE (SI 8). The surface roughness is in the same range as the Ti layer thickness which can result in pinholes allowing W penetration. One should notice the difference between the deposition techniques used for the insertion of two inter-layers. In the case of Al_2O_3, the oxide acts as a dominant layer to control the switching properties, due to the conformal coverage of ALD deposited films. In fact, after the first 10 ALD deposition cycles, the Al_2O_3 reaches the nominal layer growth resulting in a dense and conformal layer [143], which completely prevents the interaction of W with the HfO_2 layer. While the Ti layer is sputtered at room temperature and this defines a film with

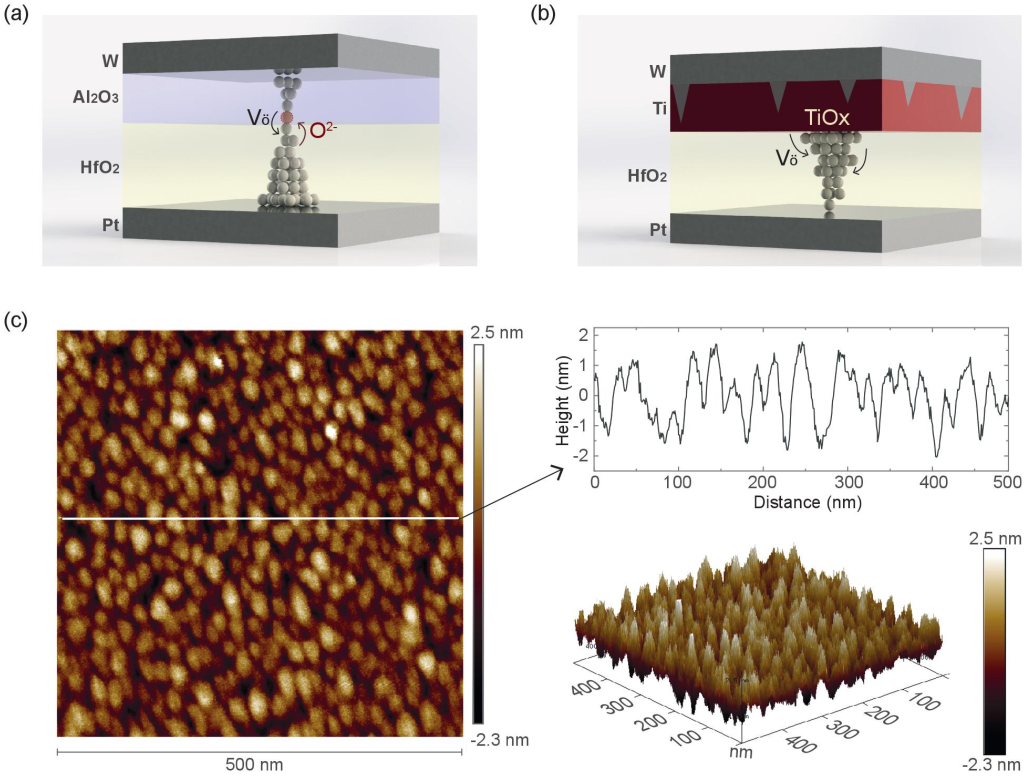

Figure 3.8 – Conduction mechanism schematic for (Pt/HfO_2/Al_2O_3/W) (a) and (Pt/ HfO_2/Ti/W) (b) devices. (c) The AFM maps for the evaluation of the surface morphology.

lower density and less coverage in comparison with the ALD technique. Therefore, the role of W is not completely inhibited by the presence of the buffer layer. The main consequence of W partial interaction with HfO_2 is visible in the pulse measurement results of Figure 3.4(b). When the Reset pulse operation is fast, a lower energy is provided to the sample and TiO_x has more tendency to be reduced, since it has lower oxygen affinity than WO_x. As soon as the pulse timing is long enough to provide sufficiently high energy, W starts to be reduced at the interface. The diffusion of ions in the oxide layer is progressively increased by the W sequential reduction. The released oxygen ions can drift under the effect of the electric field and break the CNF at the Pt/HfO_2 interface. The process reaches a saturation point when Ti and W are completely reduced.

Conclusion

In this work, an extensive study on W-based metal oxide ReRAM is presented, focusing on the HfO_2/W interactions responsible for resistive switching behavior. W has sequential oxidation properties which are involved in the switching kinetics. We have modulated the W interaction during switching by interface engineering. It has been shown that the insertion of a compact

ALD deposited high-barrier oxide layer (i.e. Al_2O_3) completely inhibits W contact with HfO_2. Al_2O_3 low oxygen mobility and strong Al-O bonding immune W oxidation and define an asymmetrical confined CNF, where a few number of ions is able to break/rebuilt the filament, resulting in a sharp change in current during Reset operation. The sharp current change limits the control of HRS by the pulse time. It has been shown that the incorporation of sputtered oxygen scavenging Ti layer partially prevents W interactions with HfO_2. Since the Ti thickness is in the same range of surface roughness, W comes into contact with HfO_2 through the Ti layer pinholes meaning that both W and Ti with different oxidation properties contribute to the switching. Ti has fast oxygen exchange properties while W has sequential oxidation that needs more energy to reach its steady state. This was observed by the change of Reset kinetics over pulse time. Consequently, we are able to achieve HRS multi-states by pulse timing control. In addition, remarkable improvements in power consumption optimization, HRS and LRS stabilization, C2C and D2D variability reduction, endurance and retention have been reported for both (Pt/HfO_2/Al_2O_3/W) and (Pt/HfO_2/Ti/W) stacks. These findings make (Pt/HfO_2/Ti/W) memory attractive for neural network applications and spike-inspired circuits where one can modulate different HRS by both pulse voltage amplitude and rise time.

Methods

Device fabrication

The fabrication process starts with a thermal growth of 500 nm SiO_x on standard 4" Si wafer. Then a 5 nm Ti adhesion layer and 125 nm Pt BE are sputtered by a Pfeiffer Spider 600. Through standard photo-lithographic processes, the BE is coated and patterned. After, the BE is dry etched by STS Multiplex ICP. Thereafter a 100 nm thick low thermal oxide (LTO) by LPCVD at 425°C is deposited as a passivation layer. Subsequently, to define ReRAM active area, VIAs with different sizes of 1, 2, 3, 5 and 10 μm are patterned by photo-lithographic processes and BHF wet etching. The HfO_2 active layer (5 nm) and the Al_2O_3 barrier (3 nm) are deposited by atomic layer deposition (ALD) at 200°C, while the Ti oxygen scavanger is deposited by sputtering at room temperature. A 56 nm W TE film is sputtered by an Alliance-Concept DP 650 with a final 15 nm TiN cap deposition to avoid oxidation. Finally, the TE is patterned by photolithography and dry etched using an optimized recipe to reduce the physical damages of the switching layer.

Electrical Characterization.

The device electrical characterization is performed trough a two-point contact with grounded BE and biased TE by an Agilent B1500 parameter analyser. Two different setups are used for voltage ramp measurements (DC) and pulse measurements (pulse width ≤ 1ms)(SI 9). In DC mode, the I_{cc} limitation is performed by the internal tool of the parameter analyser, while during pulse measurements an external transistor is introduced. The transistor goal is to efficiently control the current limit, reducing the initial current overshoot, which is one of the causes of fast degradation of device performances. In order to evaluate the current trend during the pulses, the voltage drop across a series resistance is measured using the oscilloscope. The value of the resistance is chosen properly for each device as a compromise between the noise reduction and the avoidance of interference on the Set process.

Acknowledgment

The authors thank Dr.J. Sandrini for his help on pulse programming and device fabrication advises and Dr.T. Lagrange for transmission electron microscopy imaging and the EPFL center of electron microscopy (CIME) for their technical helps. The authors acknowledge the staff of the center of micro-nano technology of EPFL, for providing technical advices in the device fabrication.

Supplementary Information

Switching kinetics control of W-based ReRAM cells in transient operation by interface engineering

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Forming phenomenology

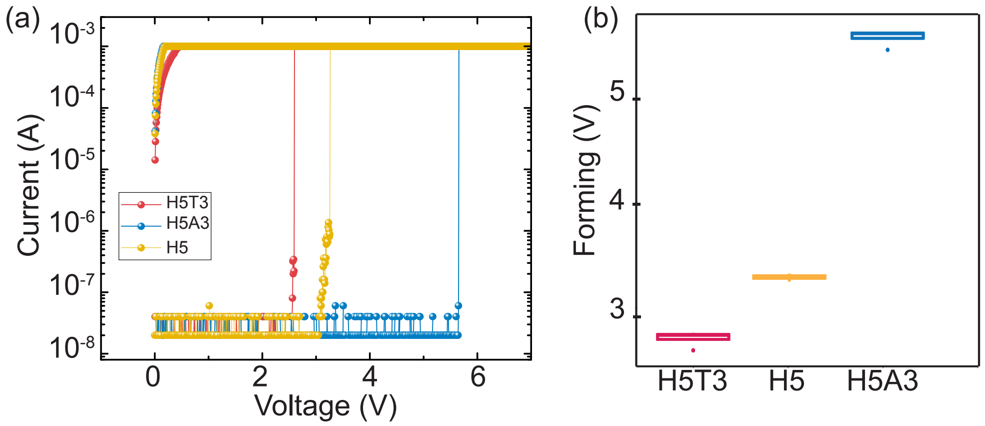

Figure 3.9 – (a) Forming I-V characteristics of H5T3: Pt/HfO_2/Ti/W, H5: Pt/HfO_2/W and H5A3: Pt/HfO_2/Al_2O_3/W. (b) Device-to-device (DTD) variation of the forming voltage comparisons between 3 different stacks of H5T3, H5 and H5A3. The statistical analysis are carried out over 5 devices per each stack.

Figure 3.9(a) shows the forming operations of the three stacks. The forming voltage extracted from the IV curves of Figure 3.9(a) are 2.57 V for H5T3, 3.25 V for H5 and 5.65 V for H5A3. The comparison between H5 and H5A3 reveals that, with insertion of thin Al_2O_3 barrier layer, the cell requires higher energy for the formation of $V_{\ddot{O}}$. The effect of Al_2O_3 in $V_{\ddot{O}}$ reductions is evident in the abrupt forming current jump with the lower transient of 6×10^{-8} A, compared to the gradual current increase in the H5 cell. In case of the H5T3 cell, the insertion of 3 nm of high oxygen scavenging Ti layer increases the pristine density of the $V_{\ddot{O}}$ in HfO_2 and lowers the forming voltage. As shown in Figure 3.9(b), there is only slight device-to-device (DTD) forming voltage variations for each stack and no clear trend in forming variability improvement is observed between the stacks.

D2D variability analysis

D2D performance variability are demonstrated in Figure 3.10(a,b). The trends that were explained from C2C in the paper Figure 3.2 for the insertion of Al_2O_3 and Ti compare to H5 for the V_{reset} and V_{set} reduction with performance uniformity enhancement are consistent with the D2D variation graphs. This confirms that the main switching parameter variation is attributed to the CNF geometry alteration caused by the intrinsic material properties of each stack and is not induced by our processing techniques.

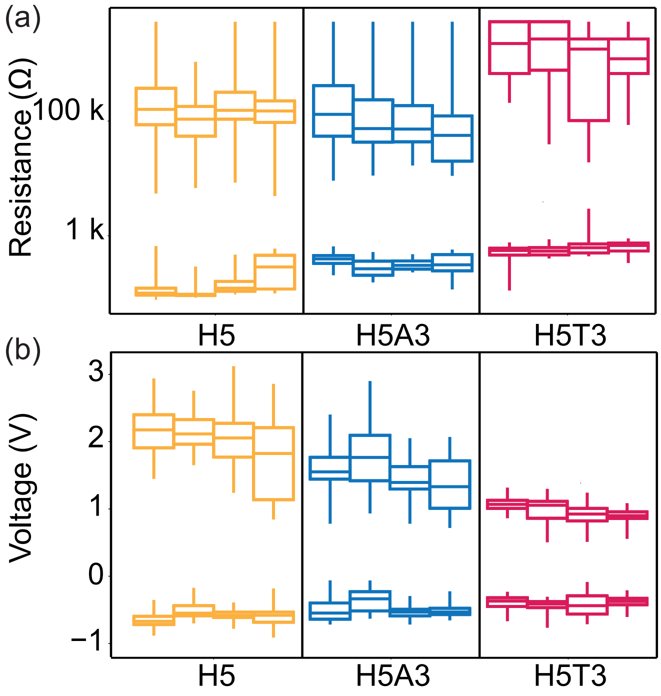

Figure 3.10 – Device-to-device distributions of (a) HRS and LRS and (b) V_{reset} and V_{set} for the H5, H5A3 and H5T3 ReRAMs. For the boxplots, the horizontal line within the box represents the median value while the upper and lower lines of the box show the first and the third quartile respectively.The statistical analysis are carried out over 4 devices per each stack.

C2C mean and standard deviation table

Table 3.1 – Cyle-to-cyle variability comparisons of H5, H5A3 and H5T3 ReRAM devices.

		H5	**H5A3**	**H5T3**
Interface		-	Al_2O_3 3nm	Ti 3 nm
V_{set} (V)	μ	1.75	1.43	0.88
	σ	0.60	0.27	0.11
V_{reset} (V)	μ	0.60	0.54	0.38
	σ	0.15	0.07	0.08
HRS (kΩ)	μ	154.26	92.56	212
	σ	97.76	70.25	160
LRS (kΩ)	μ	0.28	0.30	0.63
	σ	0.2	0.07	0.13

Pulse endurance characteristics of Pt/HfO$_2$/W device

The endurance and bit error rate measurements of the Pt/HfO$_2$/W device is demonstrated in Figure 3.11. The test is carried out with the optimized -2 V reset pulse, 3 V set pulse, 1.969 V gate voltage, 1 ms pulse width and 20 % pulse slope. Reading is performed every 10 cycles. The device shows the HRS failure after 150 cycles. For the BER, The resistance value for the LRS and HRS failure are defined as 10 kΩ and 100 kΩ respectively.

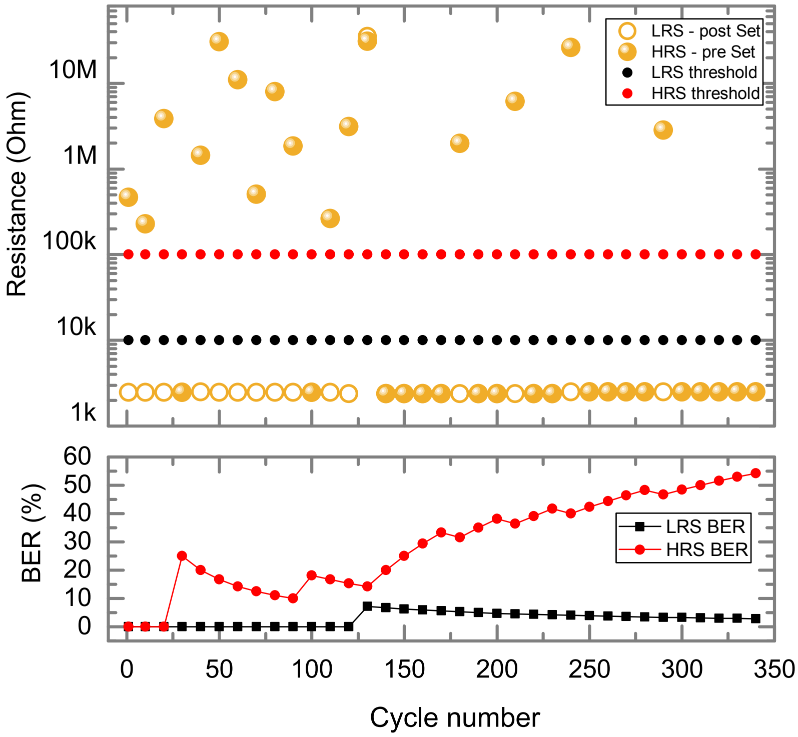

Figure 3.11 – Endurance and BER characteristics of Pt/HfO$_2$/W device.

Slope and Pulse width variation analysis on Pt/HfO$_2$/Ti/W devices

The influence of the slope and pulse width on the resistance states for the Pt/HfO$_2$/Ti/W devices are presented in Figure 3.12(a). For the measurement, the reset voltage is fixed at -2.5 V, the set voltage at 2.5 V and the gate voltage at 1.969 V. The slope value varies every 600 cycles with values of 10%, 20%, 30%, 40% and 50%, while the pulse width, color coded in the image, changes every 100 cycles with values of 5μs, 10μs, 50μs, 100μs, 500μs, 1 ms. Reading is performed every 5 cycles. The LRS magnification is represented in Figure 3.12(a). LRS does not show dependency to pulse width and pulse slope.

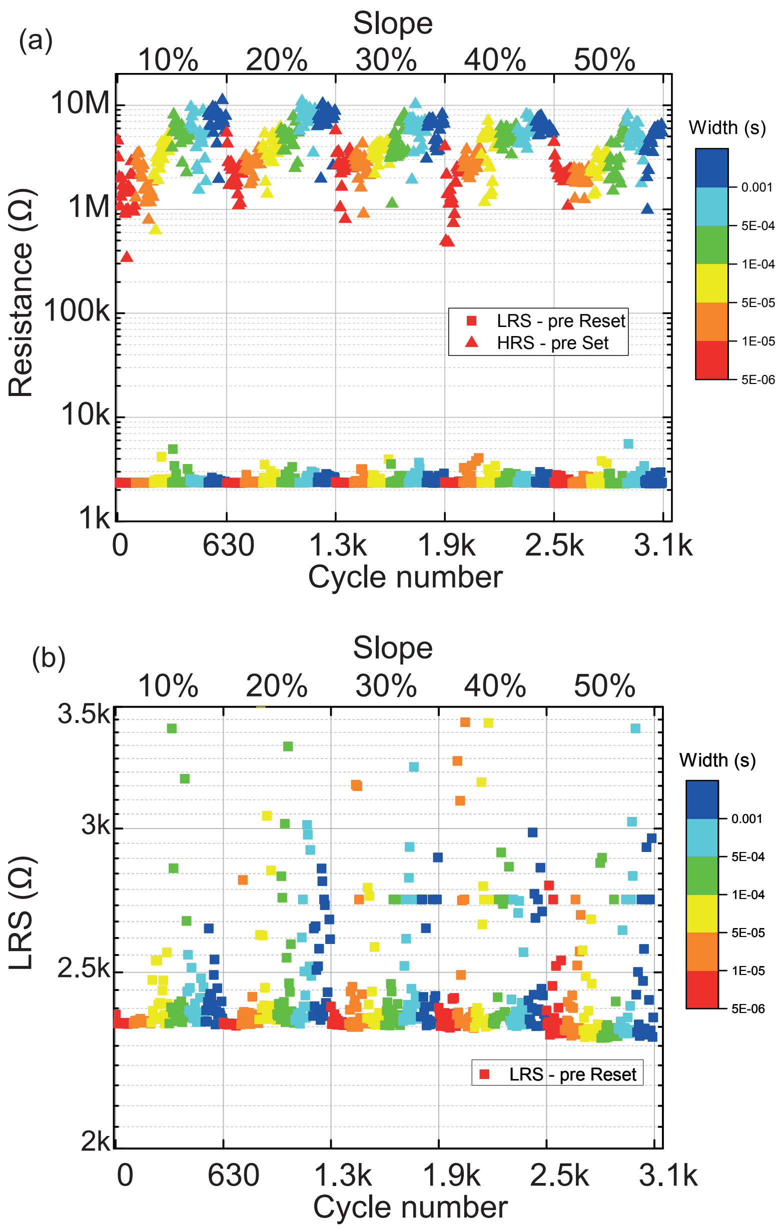

Figure 3.12 – (a) An overview of the slope and pulse width variations influence on the memory resistance states with -2 V reset pulse, 2.5 set pulse, 1.969 V gate voltage. The slope value varies every 600 cycles from 10% to 50%, while the pulse width changes every 100 cycles from 5μs to 1 ms. Reading is performed every 5 cycles. (b) Magnification of the LRS versus pulse width and slopes.

Resistance dependence of Pt/HfO_2/Ti/TiN on pulse timing control

The dependence of HRS on the pulse timing is not observed in Pt/HfO_2/Ti/TiN devices, in which W is not present. Figure 3.13 presents five consecutive endurances (2000 cycles per test), obtained by changing the pulse width from 100 μs to 100 ns with the constant pulse slope of 20%. HRS does not vary with respect to the pulse width.

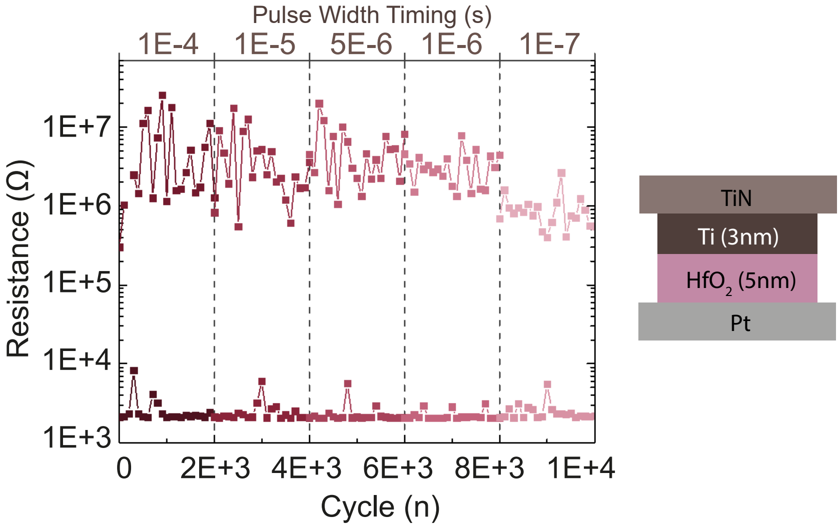

Figure 3.13 – Influence of the pulse width on Pt/HfO_2/Ti/TiN devices. The pulse width changes every 2000 cycles with the values of 100 μs, 10 μs, 5 μs, 1 μs, 0.1 μs.

Conduction mechanism Fits (TAT and SD)

The Pt/HfO_2/Ti/W reset behaviour is properly described by Schottky transport mechanism, while the set is Ohmic. The fit for both regimes are performed on 50 consecutive DC cycles in $ln(I)$-$\sqrt(V)$ and $ln(I)$-$ln(V)$ scales respectively. The result for the first 20 cycles are reported in Figure 3.14 and Figure 3.15. The same procedure is carried on the Pt/HfO_2/Al_2O_3/W device, revealing good accordance with Trap Assisted Tunneling (TAT) and Ohmic transport mechanisms (Figure 3.16 and Figure 3.17).

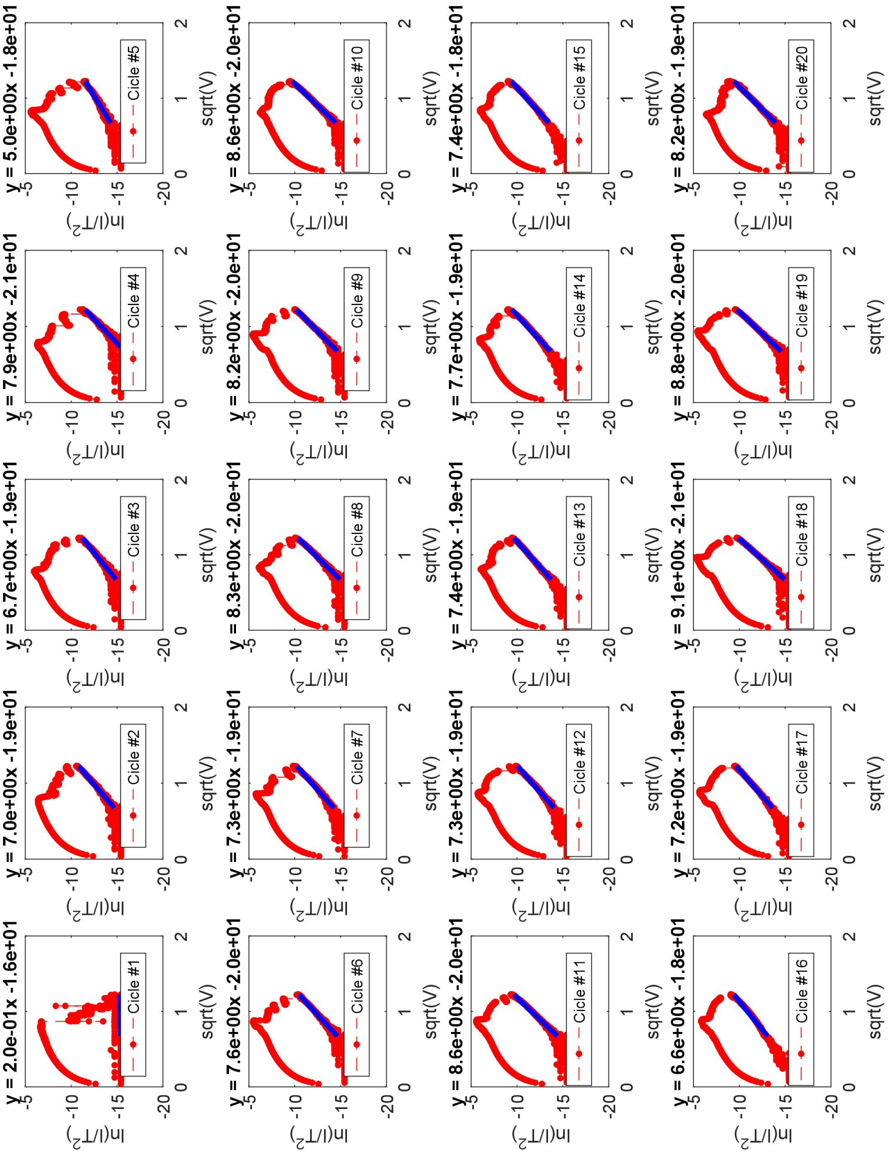

Figure 3.14 – I-V characteristic for 20 consecutive reset half-cycles in $ln(I)$-$\sqrt(V)$ scale and linear fits. The best fit parameters for each cycle are reported on top of each box.

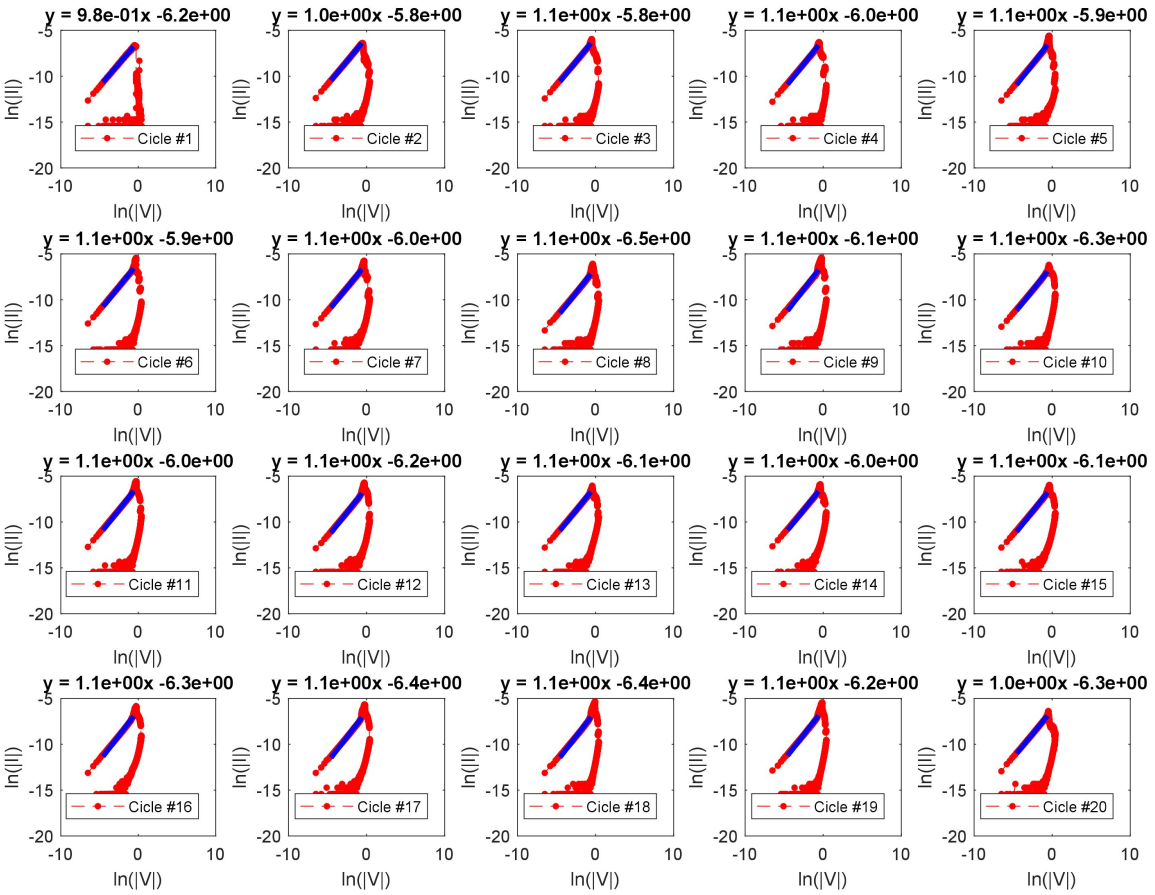

Figure 3.15 – I-V characteristic for 20 consecutive reset half-cycles in $ln(I)$-$ln(V)$ scale and linear fits. The best fit parameters for each cycle are reported on top of each box.

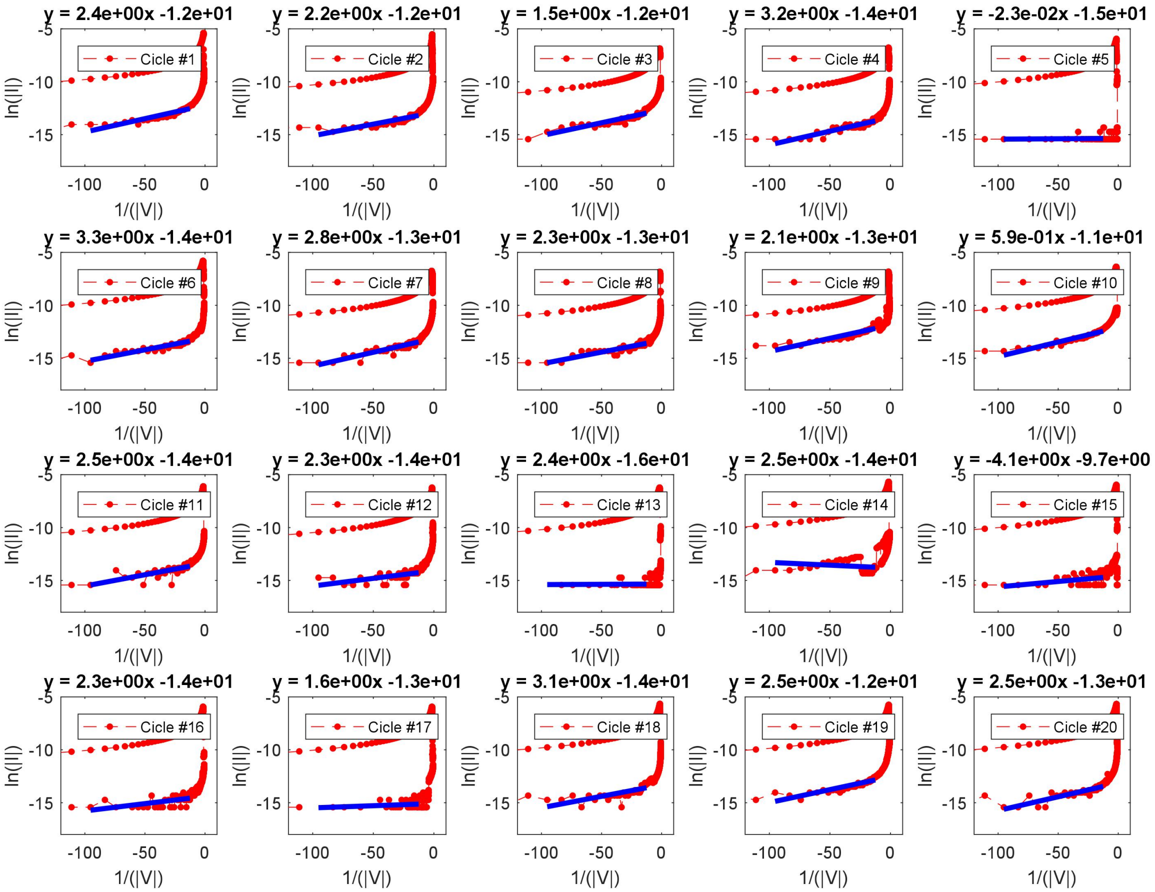

Figure 3.16 – I-V characteristic for 20 consecutive reset half-cycles in $ln(I)$-$1/(V)$ scale and linear fits. The best fit parameters for each cycle are reported on top of each box.

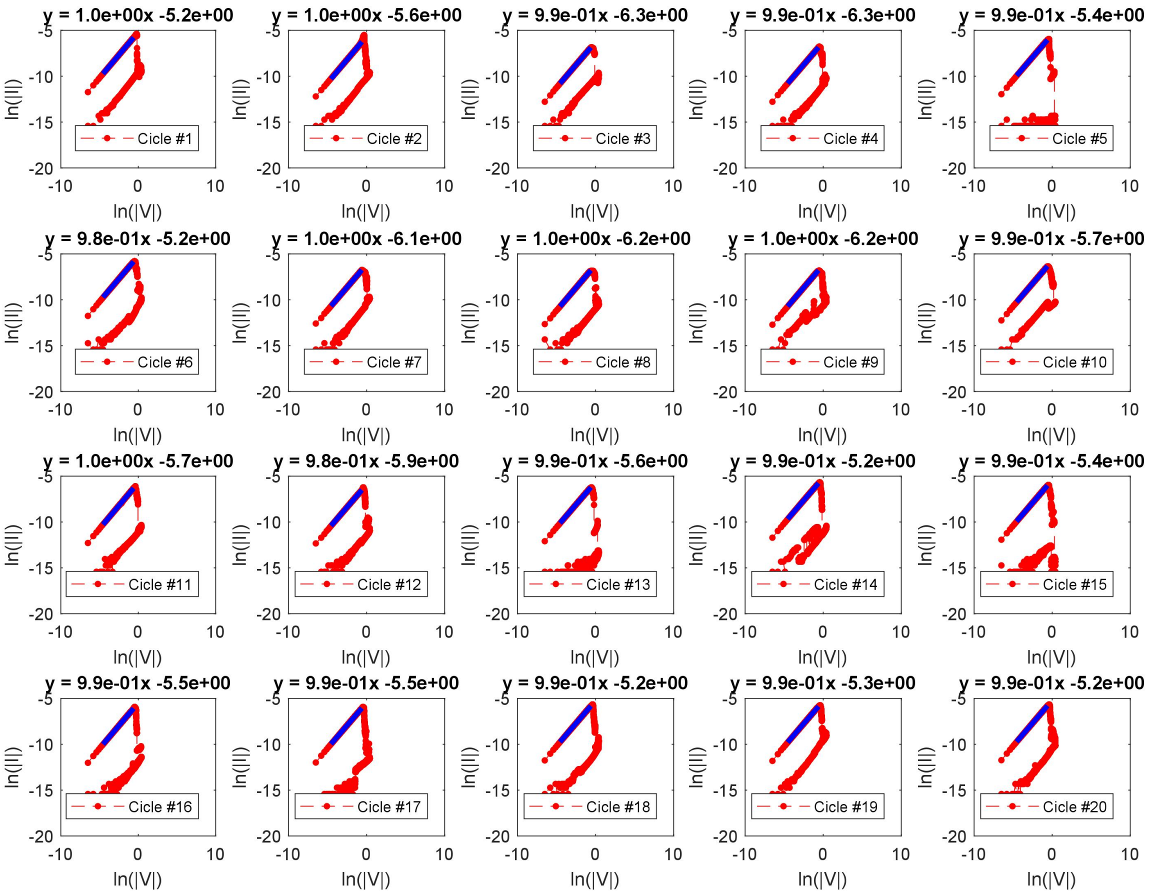

Figure 3.17 – I-V characteristic for 20 consecutive reset half-cycles in $ln(I)$-$ln(V)$ scale and linear fits. The best fit parameters for each cycle are reported on top of each box.

AFM surface analysis of the Pt, Pt/HfOx/Ti and Pt/HfO_2/AlOx surfaces

AFM map analysis of the Pt, Pt/HfO_2/Ti and Pt/HfO_2/Al_2O_3 surfaces are demonstrated in Figure 3.18(a,b,c) respectively. It is observed that the morphology of the Pt surface is transfered to the both Ti and Al_2O_3 surfaces.

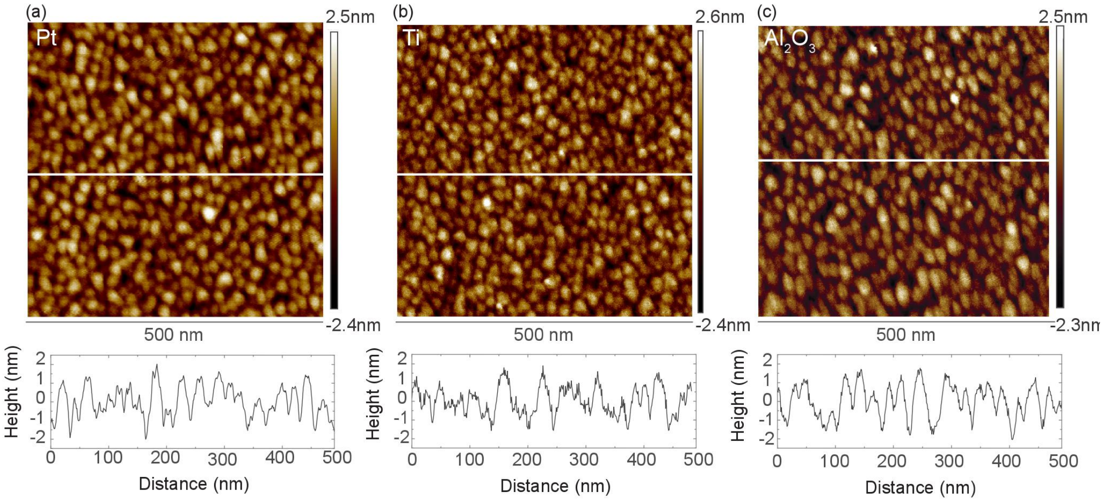

Figure 3.18 – surface morphology AFM maps for the (a) Pt, (b) Pt/HfO_2/Ti and (c) Pt/HfO_2/Al_2O_3. The scale is 500 nm.

Electrical measurement setup

Figure 3.19 presents the different setups used during the electrical characterization. In Figure 3.19(b,c) the value of the V_{gate} is modulated to obtain current compliance values from 150 μA to 500 μA. The values for the series resistance in Figure 3.19(c) are:

- 1 kΩ for the Pt/HfO_2/Ti/W devices;

- 50 Ω for the Pt/HfO_2/Al_2O_3/W devices.

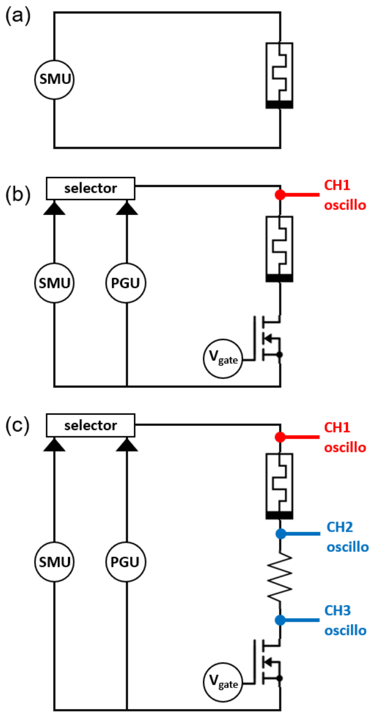
(a)
SMU
(b)
selector
CH1
oscillo
SMU
PGU
V_{gate}
(c)
selector
CH1
oscillo
CH2
oscillo
SMU
PGU
CH3
oscillo
V_{gate}

Figure 3.19 – Schematic for electrical characterization configuration for: (a) DC measurement in voltage sweep, (b) pulse measurement for endurance and pulse variation tests, (c) current evaluation during pulse measurements.

3.2 Multi-bit ReRAM operation through the voltage control

The electrical modulation of CNF to achieve the reliable multiple resistance states is highly desired to store more informations for many different applications such as neuromorphic computing systems. Multi resistances states can be obtained by changing either the Reset pulse width or pulse amplitude [144]. However, tunning the distinct resistances states is strongly limited by the stochastic behavior of the CNF specially in the memory with large resistance window (>10^3) [145]. The multi-level switching capability of (Pt/HfO_2/Ti/W) ReRAM by varying Reset pulse widths have been carefully investigated. The dual contribution of W and Ti with different oxidation rates results in multi-level control of resistance states in transient operation. In this section the precise control of the resistance levels by changing the Reset pulse voltage is studied.

The influence of Reset pulse voltage on the resistance states of (Pt/HfO_2/Ti/W) ReRAM is shown in Figure 3.20(a, b). The measurement is carried out with the Set pulse voltage of 2.5 V, I_{cc} of 500 μA (V_{gate}: 1.969), pulse width of 5 μs and the slope of 20 %. The Reset pulse varies from -2 V to -1.6 V (step of 0.05) every 200 cycles. It is evident that by reducing the Reset pulse voltage, the HRS decreases gradually while LRS remains constant. Higher Reset voltage contains more energy for the CNF rupture results in bigger resistance value. Figure 3.20(c) shows the resistance cumulative distribution over 200 cycles at different Reset pulses of -1.6 V to -2 V (step:0.05) in which 8 distinguishable resistance states are achieved. At smaller Reset voltage ranges (-1.6 to -1.8), the resistance levels are completely splitted while for the larger Reset pulses, the resistance uniformity is reduced. Higher Reset pulse amplitude provides larger driving force during Reset process which results in uncontrollable rupture of CNF due to the Joule heating and more HRS variations [146]. Device-to-device multi-resistance states variability versus Reset pulses is demonstrated in Figure 3.20(d). The HRS values are consistent with the corresponding HRS from cycle-to-cycle cumulative distributions (Figure 3.20(c)) meaning that the resistance fluctuation is attributed to the stochastic nature of CNF during Reset and not the processing. For the boxplots, the horizontal line within the box represents the median value while the upper and lower lines of the box show the first and the third quartile respectively. The statistical analysis are carried out over 4 devices with 200 cycles per each Reset pulse value.

Figure 3.21(a) is the schematic of pulse programming operation for the multi-resistance levels retention measurement. The multilevel resistance retentions of (Pt/HfO_2/Ti/W) devices are obtained by modulating the Reset pulse voltage from -1.4 V to -2 V (step: 0.1 V). The test is carried out with the fixed value of V_{set}: 2.5 V, I_{cc} of 500 μA (V_{gate}: 1.969), pulse width of 5 μs and the slope of 20 %. After each pulse programming operation, the read is performed at 250 mV every 2 min. No resistance levels degradations are observed for 120 min which reveals the stability, reliability and non-volatility of (Pt/HfO_2/Ti/W) devices for multi-level operations through changing the amplitude of Reset pulses.

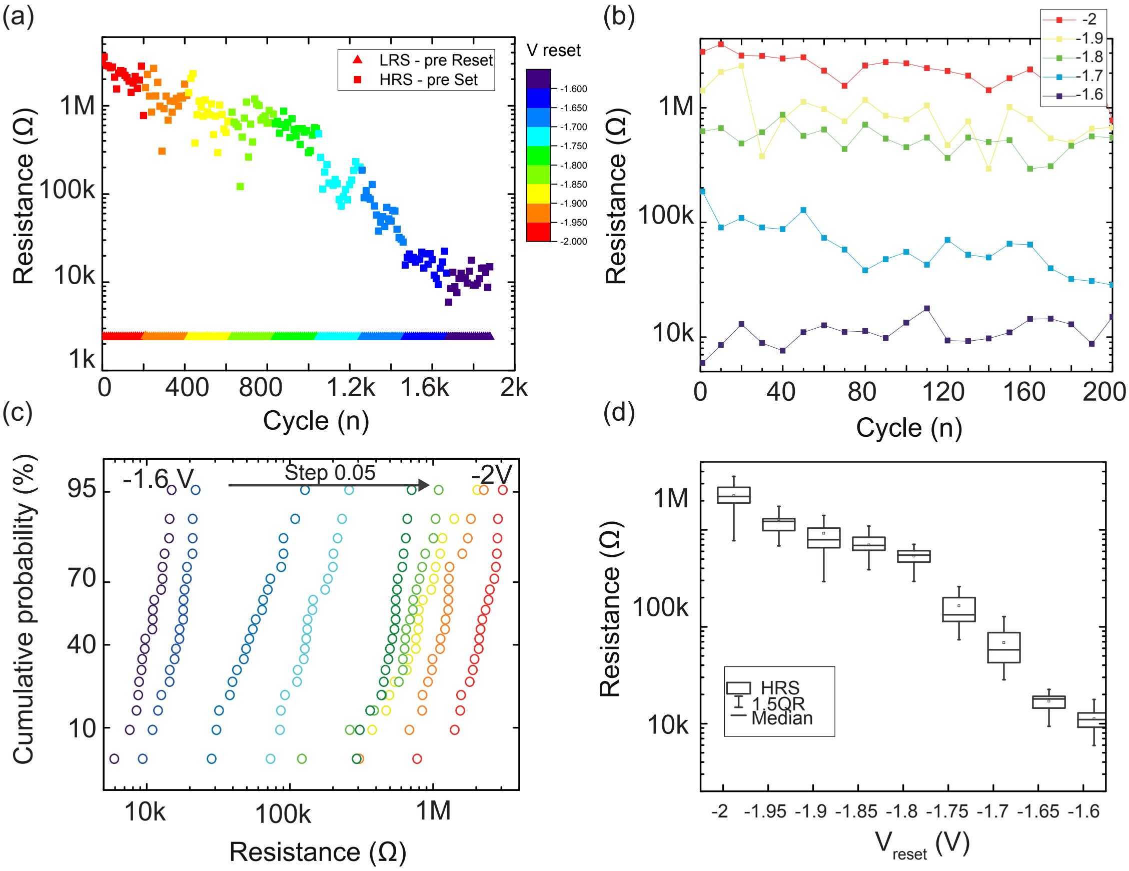

Figure 3.20 – (a) The effect of Reset pulse voltage variations on the (Pt/HfO$_2$/Ti/W) ReRAM resistance states. (b) Consecutive endurance measurement over 200 cycles for different Reset pulses of -2 V to -1.6 V (step :0.1). (c) Resistance cumulative distributions obtained from 200 consecutive AC cycles with different Reset pulse values of -2 V to -1.6 V (step: 0.05). Device-to-device distributions of the HRS resistances in 200 AC switching cycles. The statistical analysis are carried out over 4 devices per each test. The test is carried out with the fixed value of V$_{set}$: 2.5 V, I$_{cc}$ of 500 μA (V$_{gate}$: 1.969), pulse width of 5 μs and the slope of 20 %.

Finally, the switching speed for the Set and Reset operations of (Pt/HfO$_2$/Ti/W) ReRAM is investigated using the 1 kΩ resistor in series with the control transistor (Figure 3.19(c)) and the current is evaluated through the voltage drop across the resistor. For the actual switching speed measurement, the device has to be programmed with sufficiently short pulses. Using the standard slope of 20% with nm-scale pulse width (< 50 ns) results in pulse shape deformation due to our setup SPGU limitations in creating fast pulses. For this measurement, the optimized pulse parameters are 1.3 V, -2 V, I$_{cc}$ of 500 μA, pulse width of 1μs and the slope of 1% in which the pulses are not distorted. The results for both Set and Reset current transient are demonstrated in Figure 3.22(a,b) revealing the switching time of 80 ns and 100 ns, respectively. The switching time is defined as the time interval between the pulse start and the moment when an abrupt change in current is visible (Figure 3.22(c,d)).

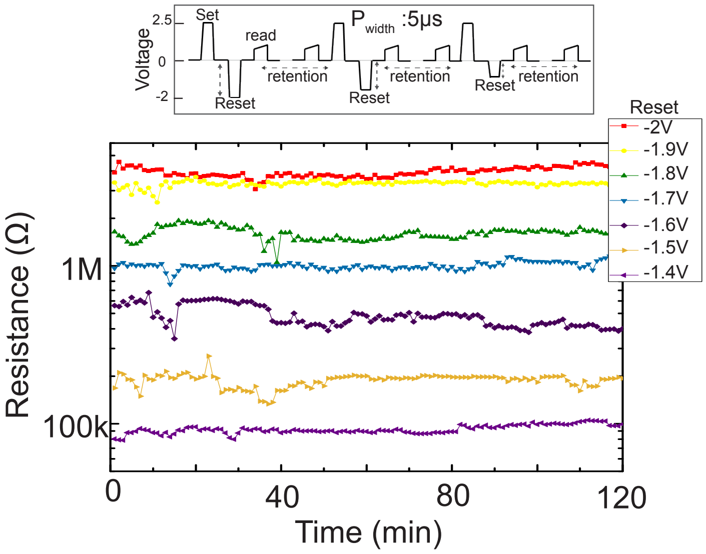

Figure 3.21 – (a) The pulse programming operation for the retention measurement. The test is carried out with the fixed value of V_{set}: 2.5 V, I_{cc} of 500 μA (V_{gate}: 1.969), pulse width of 5 μs and the slope of 20 % with the varied Reset pulse values of -2 V to -1.4 V (step 0.1). The read is performed every 2 min. (b) Retention characteristics of (Pt/HfO$_2$/Ti/W) for 120 min at room temperature results in 7 different HRS levels obtained by controlling the Reset pulse values.

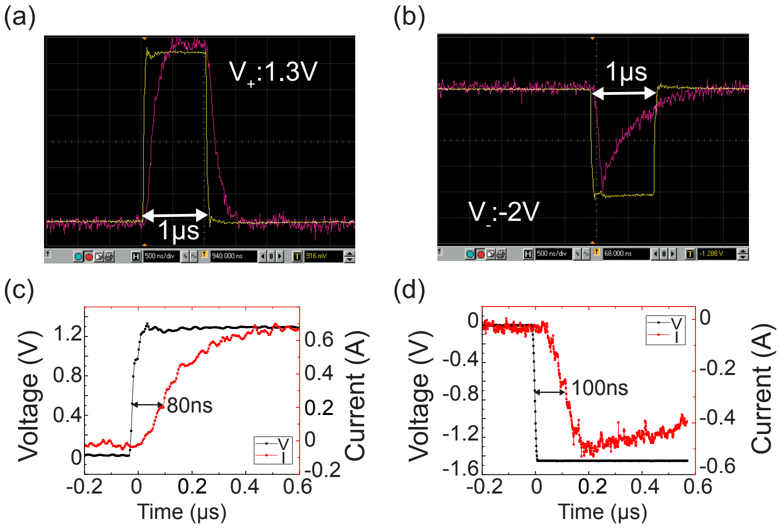

Figure 3.22 – Current transient behavior of the (Pt/HfO$_2$/Ti/W) ReRAM devices with a (a) Positive set pulse value of 1.3 V and (b) negative reset pulse value of -2 V. The optimized test parameters to measure the switching speeds are, pulse width of 1 μs, slope of 1 % and I_{cc} of 500 μA. The magnified (a) Set transient operation with the switching speed of ~ 80 ns and (b) Reset transient operation with the sweeting speed of ~ 100 ns.

3.3 The key impact of incorporated Al_2O_3 barrier layer on W-based ReRAM switching performance

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Authors contribution: ES developed the fabrication process by the early supports from JS, produced the samples, performed the electrical measurement, analyzed data and wrote the manuscript. CG was involved in the conduction mechanism explanation, performed the corresponding calculations and revised the manuscript. YL supervised the research and revised the manuscript.

The key impact of incorporated Al_2O_3 barrier layer on W-based ReRAM switching performance

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Abstract

In this article, we inspected the bipolar resistive switching behavior of W-based ReRAMs, using HfO_2 as switching layer. We have shown that the switching properties can be significantly enhanced by incorporating an Al_2O_3 layer as a barrier layer. It stabilizes the resistance states and lowers the operating current. Al_2O_3 acts as an oxygen scavenging blocking layer at W sides, results in the filament path constriction at the Al_2O_3/HfO_2 interface. This leads to the more controllable Reset operation and consecutively the HRS properties improvement. This allows the $W/Al_2O_3/HfO_2/Pt$ to switch at 10 times lower operating current of 100 μA and 2 times higher memory window compared to the $W/HfO_2/Pt$ stacks. The LRS conduction of devices with the barrier layer is in perfect agreement with the Poole-Frenkel model.

Introduction

Resistive random access memory (ReRAM) in the past decays has drawn great attention with the prospects of creating a replacement for both embedded storage memory and mass memory applications [6]. Typical ReRAM cells consist of a simple metal-insulator-metal structure, in which the electrical resistance can switch between two resistance states, high resistance state (HRS) and the low resistance state (LRS). Simple structure, great scalability, high device density and CMOS-compatibility are the key features of the ReRAMs for many different applications. For successful embedding of ReRAM in any demands, the main concerns are still to control the device variation and reduce the power consumption [114]. Among different high-k dielectric materials, HfO_2 [147], Al_2O_3 [120], TiO_2 [47] are the most mature candidates for the resistive switching devices in which the resistance levels are controlled by the formation and destruction of the conductive nano filament (CNF) path. The main performance variations are due to the limited control on such nano-scale conductive path. To improve the switching uniformity and device performances, different solutions have been proposed, such as insertion of the oxygen reservoir to facilitate the ion migrations [134], stacking a barrier layer between the oxide layer and electrode to suppress the operating current down to 1 μA [148], proper selection of the electrodes with respect to the work function and electronegativity to control the interface resistance and the switching performances [149]. Moreover, several other advanced processing techniques like, doping, nano-crystals implanting in the switching layer, operating condition adjustment and annealing at different atmosphere and temperature were carried out to reduce the switching variations [150] [151]. These massive efforts prove that it is still challenging to realize a simple, time and cost effective way to improve device stability along with the CMOS-compatible stack selection that can be applied directly for the relevant applications.

In this article, we have carefully investigated the role of ultra thin Al_2O_3 barrier layer on the switching variability enhancement of the $W/Al_2O_3/HfO_2/Pt$ ReRAM devices. Using W as the electrode is beneficial, since, it is one of the widely accepted material in the microelectronic devices. In our previous study [40], we have applied nano-scale W inter-connectors inside the CMOS technology to integrate nano-scale, self-align WO_x-based ReRAMs. Due to the CMOS thermal budget, WO_x is not the best candidate to provide stable switching performances with the W electrodes. We have designed W-based ReRAMs using HfO_2 as a switching layer and Al_2O_3 as a barrier layer. We demonstrated that the insertion of 3 nm Al_2O_3 at the W/HfO_2 interface can provide enough asymmetry barrier potential to (i) reduce the operating current, (ii) improve the resistance window and (iii) control the variability of operating voltage and HRS. Finally, the switching mechanism for the $W/Al_2O_3/HfO_2/Pt$ is well explained by the Poole-Frenkel mechanism. These studies are highly valuable for the further co-integration of the similar stack on the W via surface of the CMOS periphery.

Device description

Figure 3.23(a) is the schematic representation of the ReRAM cells fabrication. In this process, both bottom electrode (BE) and top electrode (TE) are deposited through a shadow mask membrane. Shadow mask prevents the probable reactive ion etching (RIE) electrode damaging such as ion bombardment, radiation-induces bonding changes and charge buildup. The Si-based shadow masks are fabricated using the conventional photolithography and deep reactive ion etching (DRIE) followed by the grinding to obtain the membrane with the thickness of 300 μm. For the ReRAM devices, 100 mm Si/SiO_x wafer substrate is used. The BE of W (100 nm) is sputtered at room temperature with the 15 nm of TiN as an adhesion layer. Afterwards, 100 nm of low temperature oxide (LTO) is grown using LPCVD technique at 425 °C to isolate the ReRAM cells and to define the active device area. The LTO passivation layer is patterned via photolithography and BHF wet etching to create the cylinder-shape active area with the diameter of 800 nm, 2 μm, 3 μm, 5 μm and 10 μm. Then the wafer is diced into the small chips of 1x1 cm^2 as shown in Figure 3.23(b). Next, the amorphous ALD HfO_2 and Al_2O_3 are deposited as the resistive switching layer (RS) materials. Finally a 100 nm Pt (TE) was sputter-deposited to complete the cell structure. In this paper, we have analyzed two main stacks that are referred as H5 and A3H5 within the text. Table.3.2 summarizes the samples specifications.

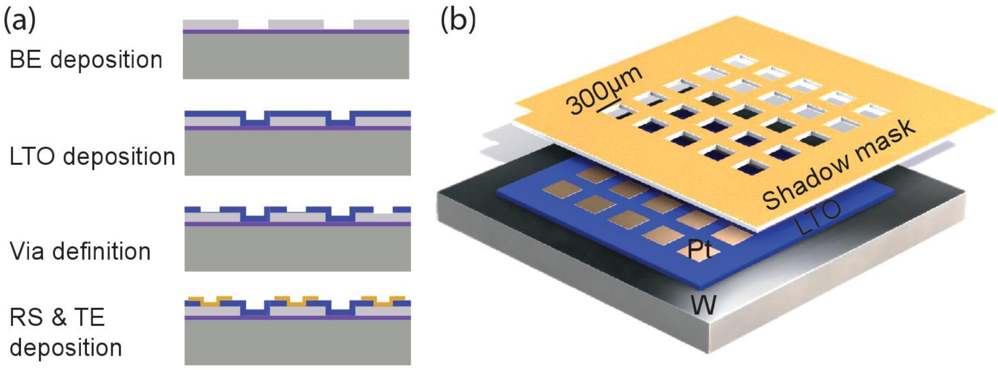

Figure 3.23 – (a) Schematic representation of the stand-alone ReRAM fabrication process flow and (b) final device stack.

Table 3.2 – Samples specification

Sample ID	Stack
H5	W 100 nm (BE)/HfO_2 5 nm/ Pt 100 nm (TE)
A3H5	W 100 nm (BE)/Al_2O_3 3 nm/ HfO_2 5 nm/ Pt 100 nm (TE)

Forming phenomenology

To qualify the impact of stack material engineering on the $V_{\ddot{O}}$ formation energy, we investigated the forming and breakdown operation for the both H5 and A3H5 ReRAM cells by applying the voltage ramp to the TE while the BE is grounded. During the forming operation, the negative voltage sweep from 0 V to -7 V is applied and the current is limited using the Agilent B1500 parameter analyzer to avoid the hard breakdown in the dielectric layers. The memories were able to switch appropriately with the negative forming operations. The breakdown voltage is obtained from the positive voltage sweep from 0 V to 12 V with no current limitation. Figure 5.4(a, b) show the SEM micrograph of ReRAM cells after employing the forming voltage (V_f) and breakdown voltage (V_{BD}) respectively. For the V_{BD} with no current elimination, the memory active area goes under massive physical damages due to the Joule heating as explained by Lu et al. [152] while for the regular forming operation with the current compliance, there are only few blow-off zones that caused due to the current overshoots problems with the parameter analyzer limitations. As shown in Figure 5.4(c), there is a higher gap between the (V_{BD}, $|V_f|$) of the A3H5 samples compared to the H5 samples. A3H5 cells are formed at -6.3 V with the I_{cc} of 100 μA and the forming voltage of -4.5 V with the I_{cc} of 2 mA is achieved for the H5 cells. Moreover, the forming leakage current (pointed in Figure 5.4(d)), for the A3H5 (3×10^{-7} A) is 10 times less than the one for the H5 (2.5×10^{-6} A). It is evident that the insertion of the tunnel barrier Al_2O_3 at the W/HfO_2 interfaces immunes the HfO_2 from the interactions with the W. Lower density of the vacancy at one interface results in a better conductive path confinement with asymmetrical geometry that can facilitate the conductive filament destruction at lower operating voltage and current. This effect is further discussed in the next sections.

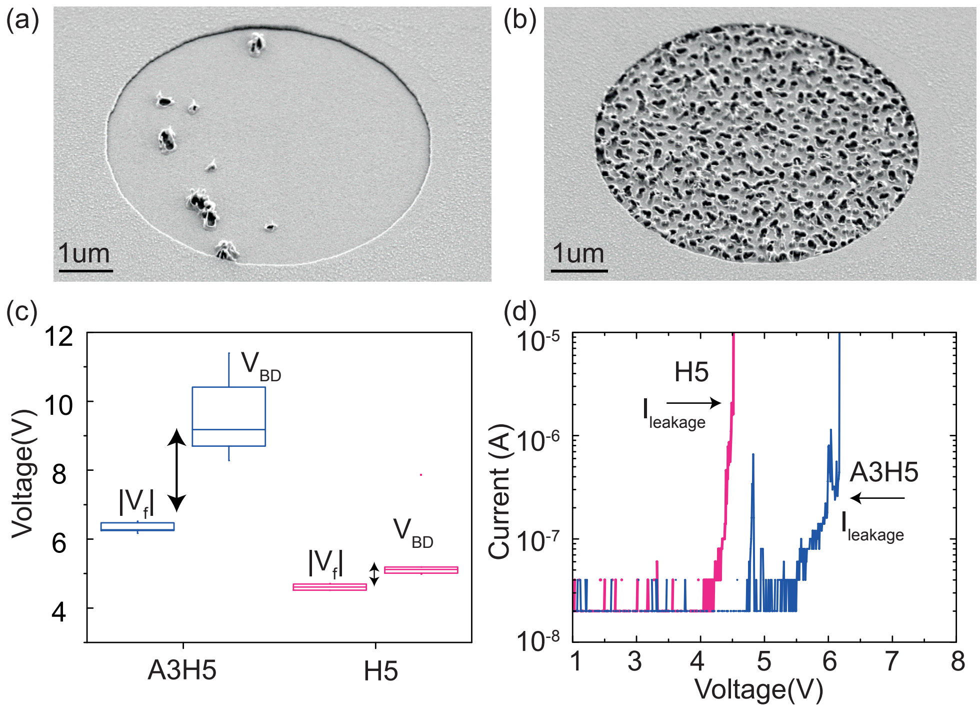

Figure 3.24 – SEM micrograph of the same stack after (a) soft forming operation with the negative bias and (b)breakdown operation with the positive applied voltage. (c) V_{BD} and V_f parameters comparison for the H5 and A3H5 cells. (d) I-|V| Forming behavior obtained from the H5 and A3H5 cells.

Switching characteristics

Figure 3.25 and Figure 3.26 show the typical DC bipolar resistive switching I-V curve and resistance variations from cycle to cycle of 5 μm H5 and A3H5 cells at room temperature. The voltage was swept from 0 V→ -1.5 V → 0 V → 2 V→ 0 V on the TE while the BE is kept grounded. During the Set operation, the I_{cc} of 2 mA and 100 μA are applied on the H5 and A3H5 cells respectively. From the DC characteristics of H5, it can be seen that the devices switched to the LRS of 300 Ω at the negative Set voltage of -1 V with 2 mA and in the positive voltage region, the LRS retained up till -2 V and gradually switched back to the HRS of 10 kΩ. It should be noted that the switching performance of the H5 stack for I_{cc} of 100 μA is strongly attenuated. Therefore, we had to progressively increase the current limit until 2 mA to get more stable and distinguishable resistance levels. For the A3H5 cells, in the negative voltage region, the cell switched to the LRS of 1 kΩ at the Set voltage of -1.1 V and far smaller operating current of 100 μA and the positive Reset associates with several intermediate jumps from LRS of 1 kΩ to the HRS of 100 kΩ. In the Reset part, the first sudden jump occurs at the Reset voltage of 0.9 V and another two obvious resistance intermediates states are visible before reaching 2 V. To assess the cycle-to-cycle stability and reproducibility of both H5 and A3H5 devices, the DC endurance test was conducted as demonstrated in Figure 3.27. The resistance values of both H5 and A3H5 were calculated at the reading voltage of 0.25 V. For the H5 cells, the memory shows very stable HRS and LRS for 50 cycles, and after that, there is an obvious degradation of HRS from 30 k to 3 k which stabilizes again over contentious cycling. This degradation is expected to be due to the incomplete Reset at the W/ HfO_2 interface.

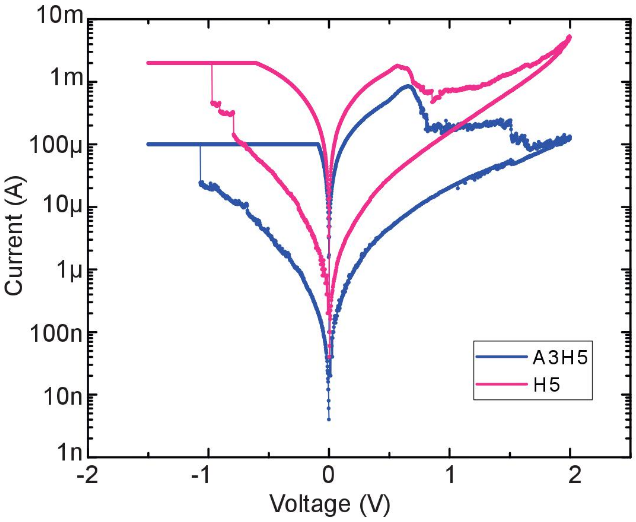

Figure 3.25 – DC bipolar resistive switching I-V curves of the H5 device (W/ HfO_2 (5 nm)/ Pt) and the A3H5 device (W/ Al_2O_3 (3 nm)/ HfO_2 (5 nm)/ Pt) cells with the negative Set operation and positive Reset operation.

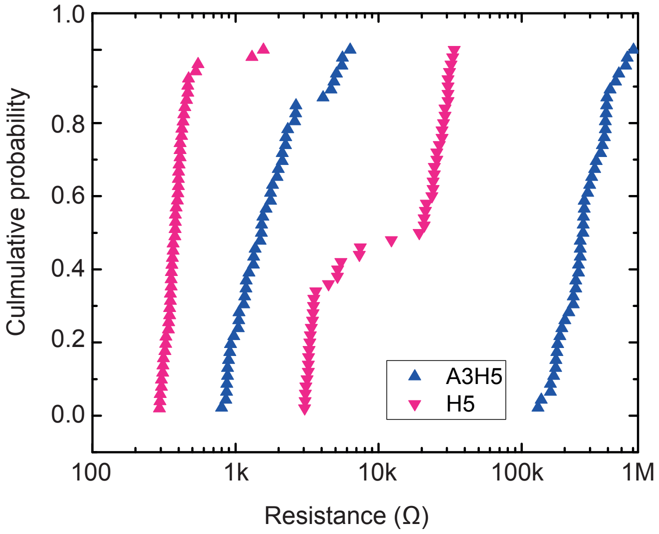

Figure 3.26 – Cumulative probability distribution of LRS and HRS for both H5 and A3H5 devices measured under DC read voltage of 0.25 V.

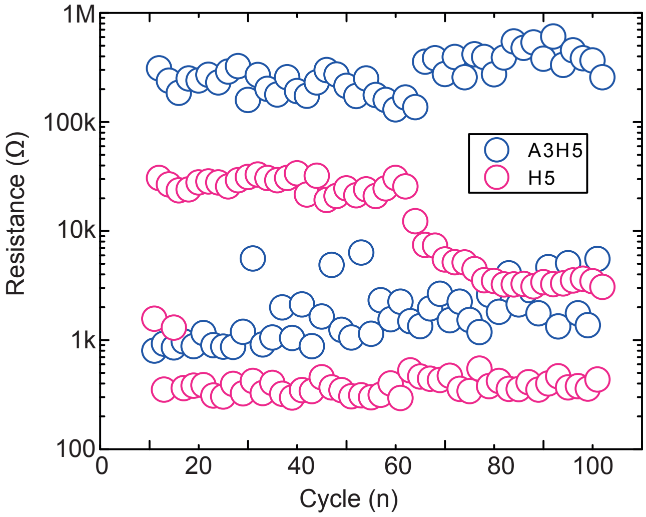

Figure 3.27 – Endurance characteristics of H5 and A3H5 devices under 100 DC consecutive cycling.

During the Set operation, the negative bias on the Pt TE pushes the oxygen ions towards the W electrode. W is known as the electrode material with several non-stoichiometric level of oxidation [153]. When W encounters the oxygen ions in the Set step, it starts to extract more oxygen ions to grow the thin layer of non-stoichiometric conductive WO_x at the W/HfO_2 interface and make the HfO_2 more deficient and form the thicker filaments. In order ro reduce the formed WO_x to return the oxygen ions back to the HfO_2 layer and break the filaments at the Reset part, higher bias voltage (>2 V) is required which makes it unfavorable for the electronic devices. The A3H5 device demonstrates stable switching over 100 cycles by maintaining a resistance window of 10^2, which can accomplish the requirement of ReRAM applications. Moreover, both HRS and LRS states are distinctly separated without any explicit degradation. The excellent cycling uniformity and reduced operating current in A3H5 is related to the insertion of Al_2O_3 at the W interface which has much higher oxygen scavenging immunity compare to the HfO_2 [120]. Al_2O_3 immunity reduces the random formation of the $[V_{\ddot{O}}]$ at Al_2O_3 induced by the W electrode which narrows down the filament path at the Al_2O_3/HfO_2 interface that can be easily ruptured with the lower power consumption. The switching parameters variation of different A3H5 and H5 devices are shown in Figure 3.28 (a,b). It is noticeable that improved switching characteristics are achieved in A3H5 stacks. The ON and OFF resistance window and the resistance stability from device-to-device is much higher compared to the H5 stacks while the operating voltage is decreased.

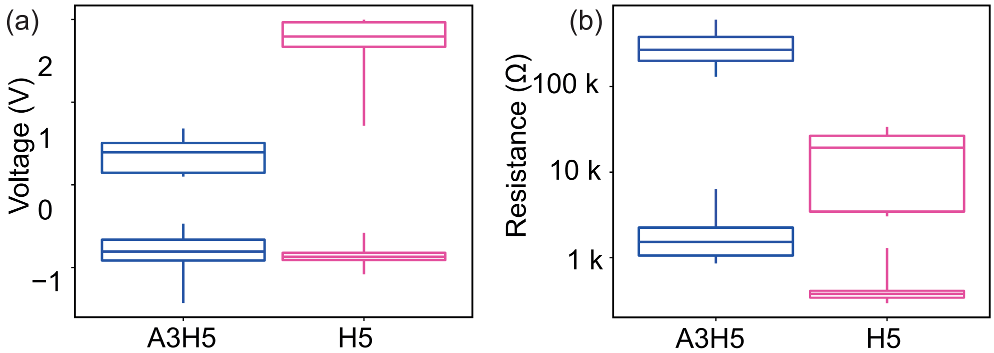

Figure 3.28 – Voltage (a) and Resistance (b) variation, comparison between H5 and A3H5. The statistical analysis have been carried out on 5 devices for each stack.

Conduction mechanism

The switching conduction mechanism of the A3H5 stack has been investigated to have a better insight on the device switching properties. Figure 3.29(b) exhibits the conductive filament dynamic in the presence of the Al_2O_3 barrier layer. The different oxygen affinity of the two oxides determines the formation of an asymmetric filament, where the interface Al_2O_3/HfO_2 acts as a constriction zone for conductive filament rupture and formation in Reset/Set operations. It is assumed that the presence of the Al_2O_3 increases the barrier potential at the W interface which results in even lower vacancy accumulation at W/Al_2O_3 compared to the HfO_2/Pt interface. The confined filament profile improves the stability of the resistance states, particularly the HRS. The narrow filament formation inside the Al_2O_3 layer is attributed to the break of Al-O bonds and the creation of $V_{\ddot{O}}$ interstitial defects [120]. Due to the very low self diffusion of $V_{\ddot{O}}$ in amorphous Al_2O_3 deposited via ALD, the defects are confined inside the barrier layer, playing a crucial role in the conduction transport mechanism responsible for the Reset of A3H5 cells. A trap-led mechanism, as the Poole-Frenkel is proposed. In this model, the current density is defined by:

$$J_{PF} = q\mu N_C E\, exp\left[\frac{-q(\Phi_T - \sqrt{qE\backslash\pi\epsilon})}{kT}\right]$$

where μ is the mobility of electrons, N_C is the state density in conduction band and Φ_T is the potential well of the traps. Trapped electrons, thermally excited by the electric field, drift inside the oxide layer by passing from a localized trap state to the adjacent ones (Fig.3.29 (c)).

In order to verify the accuracy of Poole-Frenkel conduction mechanism, the positive part of IV characteristic is plotted in $ln(I/V)$-$\sqrt{V}$ and a linear fit of data between 0.2 V and 1.5 V is performed (Figure 3.29(a)). The calculations have been carried out on 45 consecutive cycles, revealing that the Poole-Frenkel mechanism correctly describes the electron transport of the device. The dimension of the potential well of the traps (Φ_T) has been extracted by the intercept of the linear fit, resulting in 1.29±0.03 eV. The traps in Al_2O_3 lower the energy required for the electron motions. This impact is visible in the steep Reset current changes for A3H5 devices.

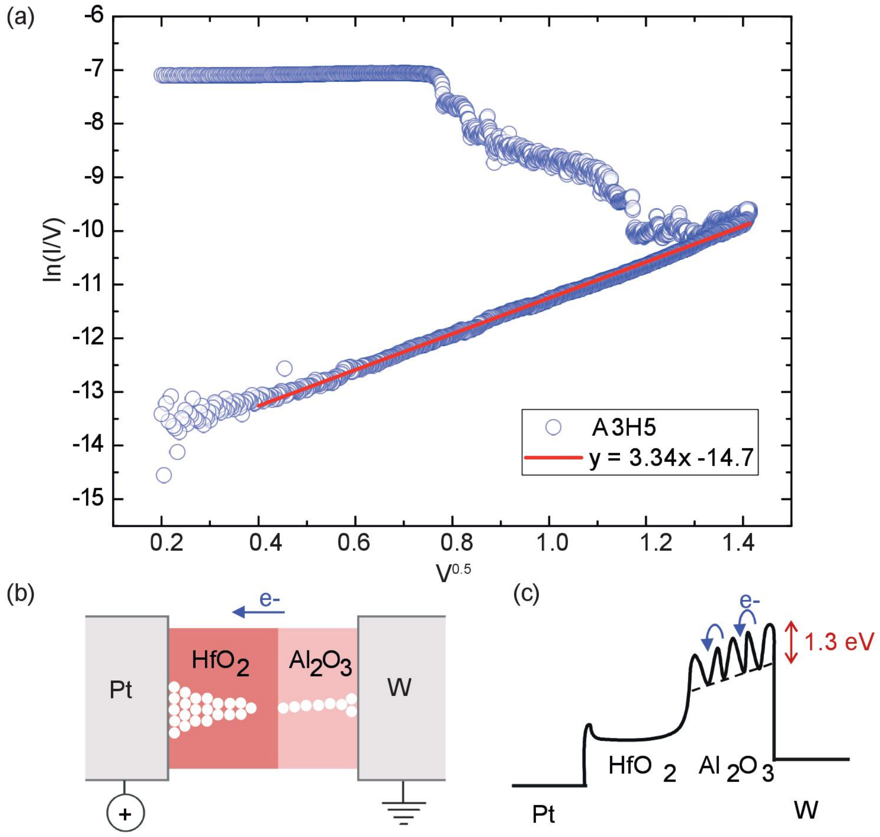

Figure 3.29 – (a) Linear fit on the Reset I-V characteristic of A3H5 in $ln(I/V)$-$\sqrt{V}$ scale; (b) Scheme of the conductive filament dynamic during Reset; (c) energetic band diagram for the Poole-Frenkel conductive mechanism.

Conclusion

In this study, we have studied the bipolar switching properties of HfO_2-based ReRAM using the W as the bottom electrode. We have ascertained the variability improvement of the resistance switching in the Al_2O_3/HfO_2 bilayers with W interface barrier engineering by insertion of an ultra thin 3 nm of Al_2O_3. Al_2O_3 acts as an oxygen scavenging blocking layer at W sides, results in the filament path constriction at the Al_2O_3/HfO_2 interface. This leads to the more controllable Reset operation and consecutively the HRS properties improvement. This allows the A3H5 to switch at 10 times lower operating current of 100 μA and 2 times higher memory window compared to the H5 stacks. The conduction mechanism of the A3H5 device is perfectly explained by the Poole-Frenkel model. This study provides valuable insights in the application of the similar stack for the 1T1R CMOS-ReRAM co integration.

4 ReRAM CMOS co-integration

In this chapter, detailed nanofabrication process of chip-scale heterogeneous ReRAM-CMOS integration, as well as, a carrier wafer for the delicate chip handling and post-processing were extensively studied. The first approach was based on thermal oxidation of W via proposing a self-align and mask-free formation of WO_x *switching layer (Section 4.1). The results are published in IEEE Xplore (DOI:10.1109/PRIME.2016.7519497). However,* WO_x *requires delicate oxidation process to obtain a stable performance, thus, in the second phase, we have employed* HfO_2 *as a well-established switching layer (Section 4.2). Furthermore, the impact of* Al_2O_3 *barrier layer on the performance of integrated ReRAM has been thoroughly investigated by means of TEM material characterization, electrical analysis and device simulation. The output of this part has been submitted for the publication.*

4.1 Chip-Level CMOS Co-Integration of ReRAM-Based Non-Volatile Memories

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Authors contribution: ES conceived the research, developed the fabrication process, produced the samples, performed the electrical and material characterization, data analysis and wrote the manuscript. JS was involved in the electrical characterization and revised the manuscript. BA revised the manuscript. TD designed the CMOS chips. MH contributed in material characterization and revised the manuscript. YL supervised the research and revised the manuscript.

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Abstract

This work reports a technique to fabricate ReRAM crossbar arrays co-integrated with fully finished 180 nm CMOS technology chips. The proposed integration method enables low-cost ReRAM-CMOS integration and allows the rapid prototyping of complete memory systems. We propose to use W plugs, already present as vias in CMOS technology, as the ReRAM bottom electrodes. The resistance switching layer, WO_x, is obtained by the mask-free rapid thermal oxidation of the W plug surface. With this method, we are able to fabricate 280 nm non-volatile memory devices without any additional high-resolution lithography. The integrated memory devices operate at 300 μA, with a high resistance state of 0.6 MΩ and low resistance state of 4 kΩ. The electrical characteristics confirm the possibility to integrated non-volatile memories on the back-end-of-the-line of standard CMOS chips, enabling low-cost integration of the memory components with the CMOS driving circuitry.

Introduction

Resistive random access memories (ReRAMs) are very promising candidates for the next generation non-volatile data storage devices, potentially offering an alternative to the widely used silicon-based flash memories [6]. The main advantages of ReRAMs include high switching speed [154], low operating voltage [155], high endurance [6], ease of fabrication, high scalability [156] and compatibility with CMOS technology [155]. In addition to the above mentioned characteristics, ReRAMs are very attractive because they can be fabricated with low thermal budget processes. This characteristic allows the fabrication of ReRAMs in the back-end-of-line (BEoL) of standard CMOS technology. It is then possible to fabricate the memory devices directly above the CMOS driving circuitry, allowing the realization of extremely compact memory systems [157] [158].

Recently, different hybrid ReRAM-CMOS technologies have been presented [159] mostly by few company fabrication facilities. As a main common feature, these solutions consist into the fabrication of the ReRAM devices by processing an entire wafer. Although this method allows a precise control on the process parameters, a high yield and the fabrication of a large number of devices per batch, it has the disadvantage of a limited accessibility. It is indeed extremely difficult to fabricate a ReRAM-CMOS integrated prototype because of the limited number of ReRAM hybrid processes and their high cost.

In this paper, we present a chip level ReRAM-CMOS co-integration method. The proposed integration solution relies on the post-processing of a standard CMOS chip, thus it does not require a dedicated CMOS foundry, and allows the realization of 280 nm ReRAM without any additional high resolution lithography. These two characteristics enable low-cost ReRAM integration and a rapid prototyping capability. First, we show the fabrication process and the electrical characteristics of WO_x-based ReRAMs. The cells, fabricated on standard Si wafer substrates, are used in order to test the WO_x switching material. Second, we present a wafer reconstruction technique to embed the CMOS chip in a standard Si wafer. This allows to post-process the chip with standard equipments. Third, we demonstrate a method to integrate WO_x-based ReRAMs in the BEoL of a CMOS chip. The integration relies on the use of W vias as Bottom Electrode (BE), and on their subsequent oxidation [39]. Next, the electrical characteristics of the CMOS integrated ReRAMs are presented. Finally, the conclusion of the paper is given.

Toward ReRAM integration development

As anticipated on the previous section, the proposed integration method uses W vias as the memory BE. Among the different metal-oxide films reported for ReRAMs with W BE [39], WO_x is extremely attractive due to the CMOS compatibility and its simple and low cost process. As top electrode material (TE), several choices are possible. Pt shows larger resistance window with WO_x ReRAM cell [53] compared to other top electrodes. However, due to its high material cost and high vapor pressure, which makes the Pt etch not CMOS compatible, TiN was preferred. TiN is already largely present in CMOS technology as a diffusion barrier material, and good electrical characteristics can be obtained for TiN TE in WO_x-based memories.

Before proceeding with the CMOS-integration, we fabricated WO_x-based ReRAMs on standard wafer substrates. This allowed us to have a reference for the WO_x switching behavior, that can be compared with the CMOS integrated memories. The fabricated memories have a Pt BE and a TiN TE. The BE material choice is justified by the fact that, for wafer stand alone memories, Pt is easier to process because it is simple to guarantee the absence of contaminants or native oxide layers.

The schematic diagram of the process flow used for preparing WO_x-based ReRAM cells is shown in Figure 4.1. First, Ti/Pt films are deposited on a 100 mm Si wafer by magnetron sputtering with a thickness of 5 nm and 125 nm, respectively. The Pt film, which acts as BE, is

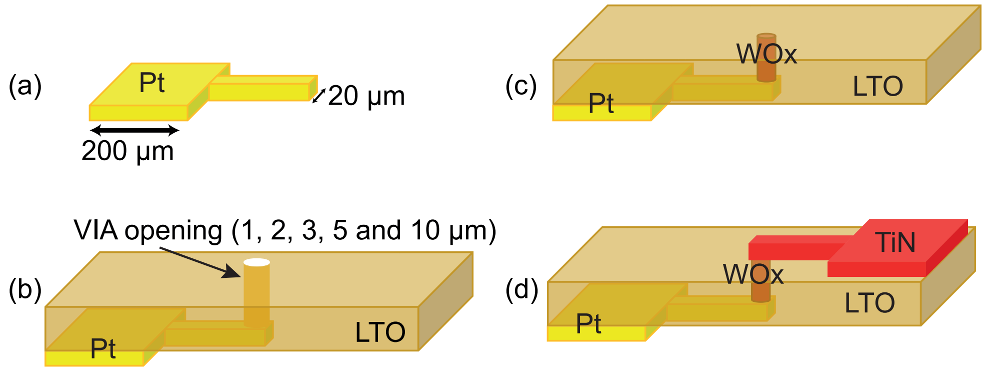

Figure 4.1 – Schematic drawing of the Pt/WO_x/TiN ReRAM 1 μm devices.

patterned via reactive ion etching (RIE) in a Cl_2/BCl_3 ambient. Next, a 100 nm passivation layer of SiO_x low temperature oxide (LTO) is deposited by low pressure chemical vapor deposition (LPCVD) at 400° C. Different via dimensions (1, 2, 3, 5, 10 μ m) are patterned by optical lithography to define the memory unit cells. The LTO layer is opened by means of BHF wet etching. Then, a 60 nm WO_x film is deposited by sputtering. Finally, the top TiN TE is deposited by sputtering and patterned by a shadow mask.

Electrical characterizations are carried out with an agilent B1500A semiconductor device parameter analyzer and a PA200 probe station under dark condition. Current-voltage (I-V) DC sweeps for 1 μm Pt/WO_x/TiN cells are shown in Figure 4.2. The memories are cycled between -2 V to 2 V, with a Set current compliance of 10 mA. The devices show a Set voltage of 1.2 V, and a Reset voltage of -1.8 V. The cell resistance was calculated 30 Ω and 90 kΩ for the LRS and HRS, respectively, with a HRS/LRS ratio of 10^3 (at a read voltage of 0.6 V).

Chip post-processing approach

A post-processing technique based on fully finished CMOS chips is advantaged due to lower costs and rapid prototyping. The major disadvantage of this method is the difficulty to handle a small CMOS die. As the most research fabrication equipments are compatible with 100 mm wafer, we fabricated a carrier wafer to handle stand-alone chips [158]. The chip is hosted into a dedicated notch. Figure 4.3 shows the main fabrication steps. Figure 4.3(e) displays scanning electron microscopy (SEM) micrograph of the carrier wafer. The carrier configuration was designed in a way to easily mount and dismount the chips, be reusable and to compensate the chip dimension variations caused by the dicing tolerances.

For the fabrication of the carrier wafer, we used the 100 mm diameter Si wafers with a thickness of 525 μm (Figure 4.3(a)). 4 μm, thick AZ-ECI 3027 resist film was spun onto the wafer and baked for 90 s at 125° C on a hotplate. The wafers were patterned via photolithography, using MA 150 double side mask aligner, and developed (Figure 4.3(b)). After the development, deep

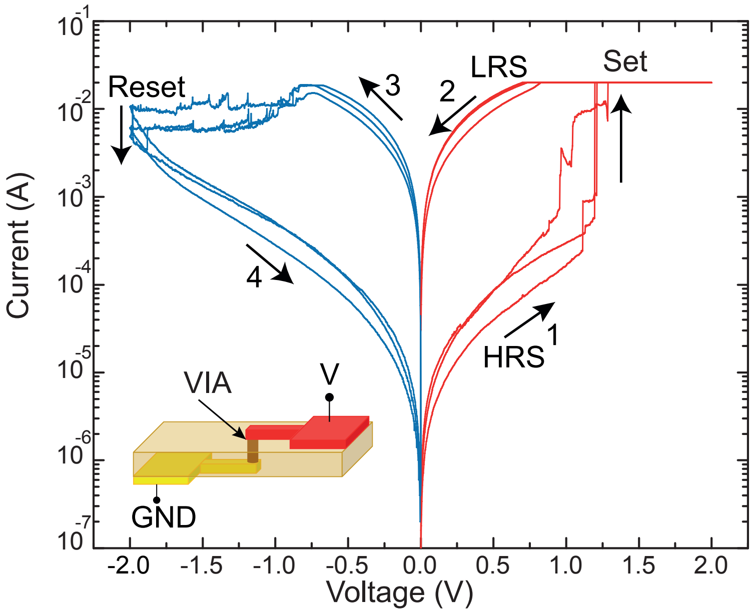

Figure 4.2 – DC I-V resistive switching characteristics for the 1μm Pt/WO$_x$/TiN ReRAM cells.

reactive ion etching (DRIE) was performed to etch the exposed area (Figure 4.3(c)). In order to obtain good lithography resolution for the subsequent fabrication steps, the carrier depth was optimized with respect to the total thickness of chip and quick stick (306 μm). Finally, the chip was fixed into the carrier notch by quick stick with a baking at 120° C (Figure 4.3(d)). Figure 4.3(e) shows the SEM micrograph of embedded chip inside the carrier wafer and the inset shows top view enlargement of memory structure in which the small square at the center hosts the memory device, while the four larger squares are the pads used for electrical characterization.

Chip ReRAM-integration & material study

Prior to ReRAM-chip heterogeneous integration, it is essential to acquire chip layer thicknesses and material composition for the post-processing steps. The microstructure of 180 nm technology CMOS chip, as shown in Figure 4.4, was observed by means of a Transmission Electron Microscope (TEM), using a Philips CM-20 equipment working at 200 kV and a JEOL 2200FS high-contrast TEM for electron energy loss spectroscopy (EELS). Chip lamella preparation is performed using a FEI Nova 200 nanolab DualBeam SEM/FIB system. Figure 4.4(a,b) show bright field TEM micrograph of the CMOS chip and measured thicknesses for each layer. Chemical mapping shown in Figure 4.4(c) explains the chip layer material composition: metal lines are composed by Al and TiN, the passivation layer by SiO$_2$ and via plugs made by W.

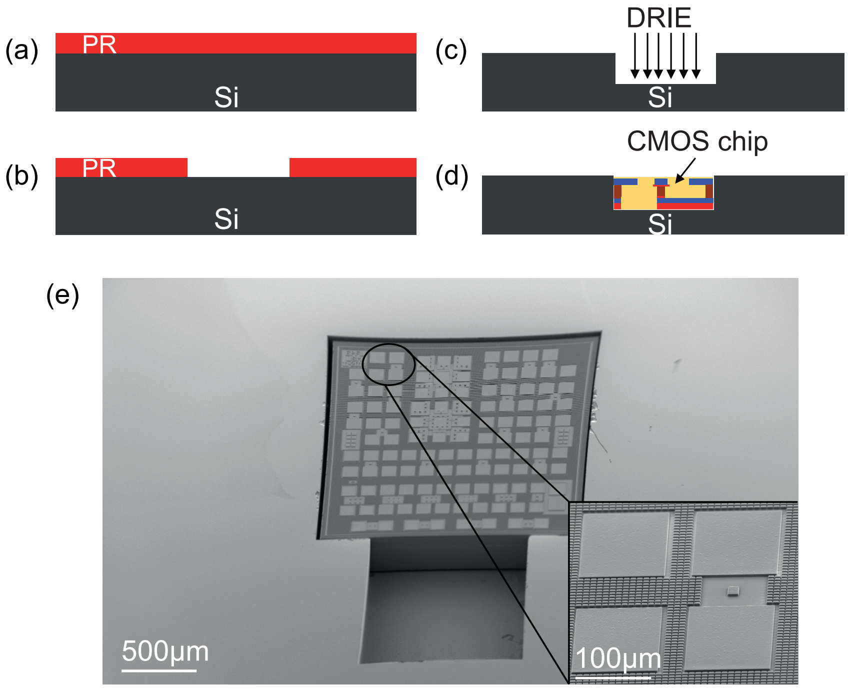

Figure 4.3 – Schematic process flow for chip carrier wafer: (a) Photoresist coating; (b) Wafer photolithography; (c) Si DRIE for carrier creation; (d) Chip embedding in carrier wafer using quick stick; (e) Scanning electron micrograph of 306 μm carrier wafer notch with the embedded CMOS chip. Inset shows the chip area detail, in which the small square at the center hosts the memory devices and the four larger squares are the pads used for the electrical characterization.

Chip ReRAM co-integrated fabrication

The summarized schematic process flow of the self-aligned WO_x ReRAM co-integrated with CMOS chip is shown in Figure 4.5. The flow starts with the photolithography to open the area that will host the memories. Then, the chip passivation is etched by the RIE with CF_4 chemistry to expose metal 6 (M6) (Figure 4.5(b_1)). Afterwards, the M6 is dry etched in an ambient Cl_2/BCl_3 mixture to access the W plugs (Figure 4.5(b,b_2). The W plugs serve as the memory BE which define the effective size of memory cell in to 280 nm (plug diameter). Subsequently, the top surface of the W plugs is oxidized by a JETFIRST200 rapid thermal processing (RTP) tool to create the WO_x memory (Figure 4.5(c)). The used RTP parameters, presented in [39] and summarized in Table 4.1 targets 60 nm WO_x film. The chemical composition of WO_x surfaces were analyzed and will be explained in the following section. Then, TiN TE is deposited by sputtering tool at room temperature and etched in Cl_2/BCl_3 chemistry (Figure 4.5(d)). Thereafter, RIE is performed to open the pads passivation used for the electrical measurements (Figure 4.5(e)) to avoid direct probe pressure damages on TE. One of the pads are electrically connected to M5, is for the BE connection. The last step, consists in the connection of the other pad to the TE with 100 nm TiN sputtered deposition (Figure 4.5(f)).

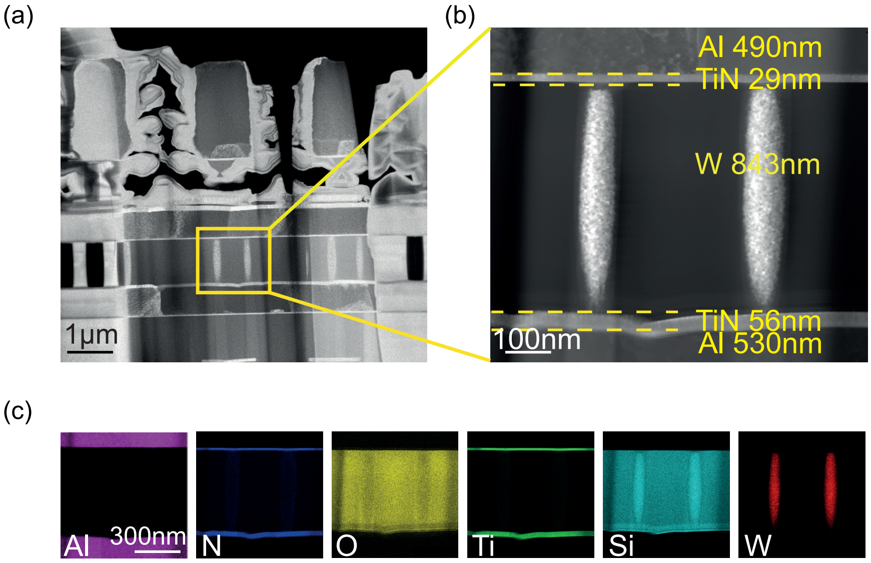

Figure 4.4 – (a) TEM cross section image of chip lamella sample from metal layer M4 to M6. (b) Represents each layer thickness measurement of partial section of chip. (c) EELS mapping respectively for the elements: Al, N, O, Ti, Si and W (scale: 300 nm).

Material study

In this section the RTP method which is used to form WO_x-based memory devices and material analysis of the oxidized W plug surfaces are explained. WO_x growth on W plugs were executed under two conditions of dry oxygen ambient and vacuum load lock with oxygen flow of 100 sccm. The RTP experimental details are summarized in the Table 4.1.

The chemical bonding state in the WO_x film for non-oxidized and oxidized samples were further examined using x-ray photoelectron spectroscopy (XPS). The W4f XPS spectrum for three samples are illustrated in Figure 4.6. The spectrum has been charge corrected with reference to adventitious C1s binding energy peak at 284.5 eV. The W4f spectrum was deconvoluted for three samples into pairs of W4f doublet peaks appropriating to W^{6+} tungsten oxidation states. The $W4f_{7/2}$ and $Wf_{5/2}$ peaks affiliated to W^{6+} are centered at 37.7 eV and 35.5 eV for all three samples indicating that the film is composed of stoichiometric WO_3.

For the reference sample, the W4f spectrum become broader with much lower intensity and one more pair of peaks that are located at binding energy of 31 eV and 33 eV attribute to the presence of W in metallic state (in W^0 state). Atomic concentration calculated from XPS spectrum for sample 3 (10.9%) is more than sample 2 (5.4%) and reference sample (2%). Sample 3 has been used for the heterogeneous ReRAM fabrication, since according to the XPS results and group [39], this condition form highest density of the most stable tungsten oxide form (WO_3) among tested experiments.

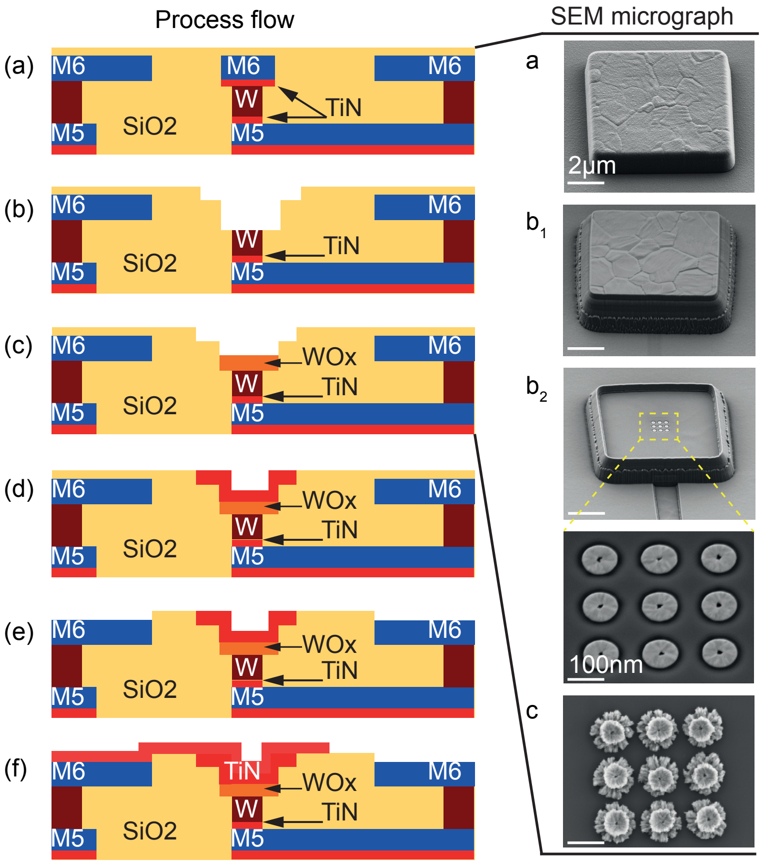

Figure 4.5 – Schematic process flow and SEM micrograph for ReRAM chip-based co-integration. Process flow: (a) Chip cross section; (b) Passivation and M6 RIE; (c) W plug oxidation; (d) TiN TE sputtering; (e) Chip pads passivation opening; (f) TiN pads connection sputtering. SEM micrograph: (a) top view of non-processed chip area which will host memory ; (b_1) top view of M6 (Al) after passivation removal (scale: 2 μm); (b_2) top view (scale: 2 μm) and enlargement (scale: 100 nm) of the W plugs after M6 and TiN RIE; (c) W plugs oxidation image to form the resistance layer for ReRAMs (scale: 100 nm).

Table 4.1 – RTP oxidation parameters on the W plugs compositions

Sample ID	Temperature	Time	O_2 Flow	W4f (Wt.%)
Reference sample	-	-	-	2%
Sample 2	500 °C	60 s	100 sccm	5.4%
Sample 3	500 °C	60 s	ambient	10.9%

Device characterization

Electrical characterization was carried out for the final device W/WO_x/TiN with the same as Set up measurements described in previous section. Double I-V DC sweeps have been used to investigate the resistive switching behavior. The positive/negative potential is applied on TiN top electrode and W plug bottom electrode is grounded (Figure 4.7 inset). Typical I-V

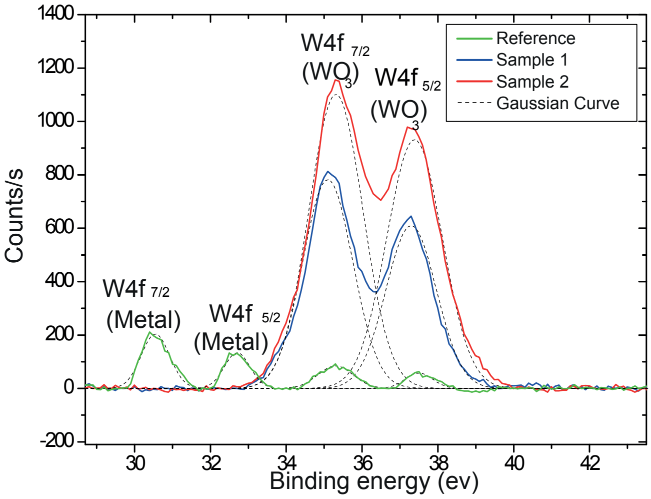

Figure 4.6 – W4f core level XPS analysis taken from the WO_x plug surfaces of three samples. The spectrum is deconvoluted into $W4f_{7/2}$ and $W4f_{5/2}$ doublets associated with W^6 and W^0 oxidation states.

sweep for chip co-integrated W/WO_x/TiN ReRAM is shown in Figure 4.7. A specific forming procedure is required since the integrate memories showed an initial low resistance state (LRS) with a resistance of approximately 50 Ω.

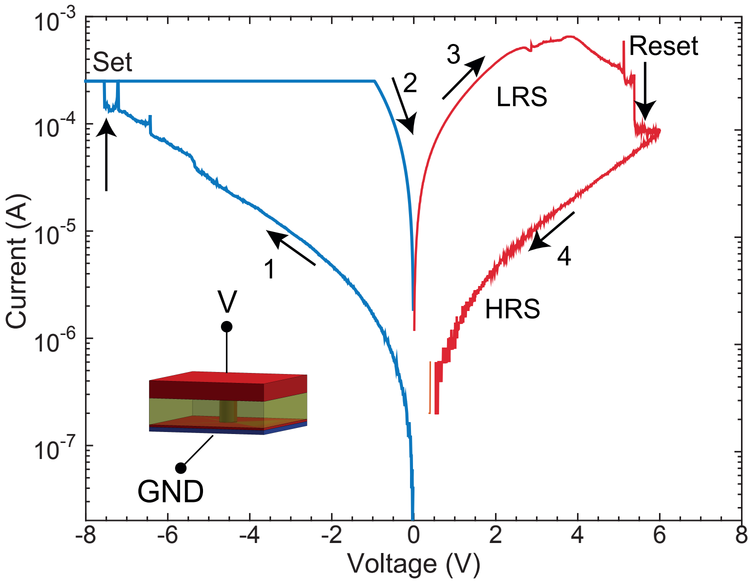

Figure 4.7 – DC I-V resistive switching characteristics for the CMOS-integrated W/ WO_x/ TiN ReRAMS .

The I(V) characteristic curve reveals the bipolar resistive switching character of WO_x ReRAM. The W/WO_x/TiN ReRAM unit switches from HRS to LRS at the Set voltage of -7.24 V as illustrated in step 1 to step 2 of Figure 4.7. The HRS resistance is around 0.6 MΩ read at -1 V. During the SET operation, the LRS current is limited by the compliance current of $I_{cc} = 250\,\mu A$ to prevent the hard dielectric breakdown. This compliance current is applied by an external parameter analyzer. After the Set operation, the sample has the LRS of around 4 kΩ at -1 V. The HRS is recovered by applying another positive sweep between 0 V to 6 V without current limitation. The Reset occurs at 5 V as shown in step 3 to step 4 of Figure 4.7.

The integrated memory device operates with low current (300 μA) and resistance window of HRS/LRS= 156, demonstrating suitability for low power consumption application. The relatively high operating voltage is caused by the low initial resistance state. Due to the low pristine resistance value, the memory cell has high leakage current which require high applied voltage to recover the Reset procedure properly. The low pristine resistance state of WO_x is explained by group Lu et al [39]. WO_x ReRAM that is provided by RTP, has the CMOS BEOL temperature limitation to be co-integrated with chips. Low oxidation temperature can cause the formation of tungsten sub-oxides below the plug surface. Tungsten sub-oxide has lower resistance than WO_3 oxide form, results in leakage path in pristine WO_x ReRAM and consequently lower initial resistance state. In order to overcome this issue, it is necessary to optimize RTP parameters for a better control on composition and intensity of WOx to achieve the maximum intensity of WO_3 oxide state.

Conclusion

Chip-level W/WO_x/TiN ReRAM-CMOS integration have been fabricated and characterized. We demonstrated low-cost and fast prototype for the heterogeneous integration of 280 nm ReRAM devices in the BEoL of fully finished 180 nm CMOS chips. The fabricated ReRAM performed at low current of 300 μA, with a high resistance state of 0.6 MΩ and low resistance state of 4 kΩ. The electrical performances promise the integrated non-volatile memories on the BEoL of standard CMOS chips, enabling low-cost integration of the memory components with the CMOS chip circuitry.

4.2 Performance improvement of chip-level CMOS-integrated ReRAM cells through material optimization

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Article status: Under review

Authors contribution: ES conceived the research, developed the fabrication process, produced the samples, performed the electrical tests, data analysis and simulation, contributed in the material characterization, and wrote the manuscript. TL performed the TEM-EDX material characterization and contributed in the manuscript writing. TD performed the CMOS chip design. YL supervised the research and revised the manuscript.

Performance improvement of chip-level CMOS-integrated ReRAM cells through material optimization

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Abstract

The integration of the resistive random access memory (ReRAM) with CMOS logic circuitry provides a solution to scaling limitations, and offers promising candidates for use in next generation computing applications. It is challenging to realize a reliable, time and cost effective integration technique and at the same time provide device stability with CMOS-compatible materials that are used in the relevant device applications. In this study, we demonstrate a technique for the nm-scale hybrid integration of ReRAM on the foundry-produced CMOS 180 nm technology chip. Tungsten (W), as a material of choice for vertical vias in CMOS circuitry, is employed as the ReRAM electrode. However, W oxidizes readily, having multiple oxidation states, which influences the device reliability. In particular, the generation of semi-stable oxides at the electrode/switching layer (W/HfO_2) interface has a profound influence on device performance. To achieve reliable W-based integrated ReRAM, we modulated and controlled the W electrode oxidation within the different co-integrated ReRAM stacks by increasing HfO_2 switching layer thickness, through the post-metallization annealing under O_2-ambient, and by adding an Al_2O_3 barrier layer between the W and HfO_2 layers. The effect of W interface modifications is further studied through the analysis of switching mechanism and TEM micro-structural characterization. A notable improvement in HRS/LRS resistance ratio and switching stability was observed in optimally fabricated (W/Al_2O_3/HfO_2/TiN) ReRAM on the back end of the line (BEoL) of 180 nm CMOS chip.

Introduction

Due to physical limitations of CMOS scaling, NAND-type flash memory can no longer satisfy the commercial demands for miniaturized and low-cost data storage applications. Resistive random access memory (ReRAM) is a promising replacement due to its excellent scalability, high device density, simple structure and CMOS compatibility [6, 14, 20, 40]. A typical ReRAM cell consists of metal-insulator/semiconductor-metal structure, which switches between at least two resistance states of high resistance state (HRS) and low resistance state (LRS) under suitable voltage stimuli. In bipolar oxide-based ReRAM, the transition from HRS to LRS

(*Set*) and the reverse operation from LRS to HRS (*Reset*) occur at opposite voltage polarities. The switching mechanism is mainly based on the creation and rupture of the conductive filament(s) (CF) made of oxygen vacancies. The hybrid integration of ReRAM with CMOS circuitry can combine the advantage of high yield and a mature circuit functionality of CMOS with the high-density feature of ReRAMs [15–17]. The integration of ReRAM as a passive circuit element within active CMOS circuitry as well as the availability of intermediate resistance levels, meet the requirements for neuromorphic computing circuit [18], reconfigurable logic [7] and analog computation [19] applications. The conventional CMOS-ReRAM co-integration, e.g., 1T1R configuration, needs costly hybrid technology [5], while embedding ReRAM on the foundry-produced CMOS chips offers reduced fabrication costs and increased accessibility, particularly for research-oriented and small industrial units. Various chip-level ReRAM-CMOS co-integration methods have been developed [7–9, 40, 97]. However, it is still challenging to realize a reliable, and economically feasible integration prototype that provides device stability using the industry standard CMOS-compatible materials.

In this study, we propose a method for the heterogeneous integration of ReRAM on the back end of line (BEoL) of standard CMOS technology. Tungsten (W), as a material of choice for vertical vias between metal layers in standard CMOS processing, is used for the ReRAM bottom electrode (BE). This technique enables the creation of nm-scale ReRAM devices with large device density through a simple, rapid and cost effective process. Tungsten, having a low work function, can facilitate the electronic bipolar resistive switching, thereby reducing power consumption [98]. However, W has high affinity for oxygen forming compounds with multiple oxidation states [55], and the generation of semi-stable oxides at the switching layer/electrode (W/HfO_2) interface greatly influences device stability. We have carefully investigated the material property requirements for reliable W electrode-based ReRAM performance. For the integrated ReRAM stack, TiN is employed as an inert top electrode (TE), and HfO_2 is used as an oxide switching material. The effect of W chemical interaction is modulated in different co-integrated ReRAM stacks by increasing HfO_2 switching layer thickness, post-metalization annealing under O_2-ambient and adding an Al_2O_3 barrier layer. The addition of Al_2O_3 barrier layer enhances the HRS/LRS resistance ratio and switching uniformity. Adding Al_2O_3 layer provides a strong barrier against oxygen diffusion and inhibits the W electrode from leaching oxygen from the W/HfO_2 interface, preventing deterioration of its electronic properties. The effectiveness of Al_2O_3 barrier in preventing oxygen leaching of the HfO_x layers was confirmed by TEM micro-structural characterization and chemical analysis, where the measured oxygen content in W bottom electrode remained at the same base level as other elements in samples which underwent multiple switching cycles. The switching mechanism is well explained by trap-controlled space charge limited current (SCLC) conduction mechanism. The Al_2O_3 layer with high barrier potential (8.4 eV) provides asymmetric barrier potential in W/ Al_2O_3 (3 nm)/ HfO_2 (5 nm)/TiN structure that facilitates SCLC electronic conduction mechanism.

Experimental procedure

Device fabrication

Four different ReRAM devices, (W/ HfO_2(5 nm)/TiN)- (W/ HfO_2(5 nm)/TiN-annealed in O_2 environment)- (W/ HfO_2(10 nm)/TiN)- (W/ Al_2O_3 (3 nm)/HfO_2(5 nm)/TiN), were integrated on the back end of the line (BEoL) of the CMOS 180 nm technology chips (Figure 4.8(a)). The ReRAM integration method is based on the chip-scale post-processing. An optical micrograph of the post-processed test chip is shown in Figure 4.8(b). The chip has the dimension of $1.6 \times 1.6\ mm^2$ which contains 28 square-shaped active areas with the width of 3-15 μm for passive memory integration. The active areas are placed between the 100 μm pads that are used for the electrical measurements. Figure 4.8(c) shows the TEM cross-section image of the CMOS 180 nm technology. The chip is made of six Al metal layers that are connected through the vertical W vias. The adjacent metal layers (M) and vias are isolated by the SiO_x/SiN passivation layers. The memory cells are fabricated on the top of W based material vias, between the M5 and M6, using W also as the bottom electrode (BE).

An overview of the process flow and their corresponding SEM micrograph for the chip-level ReRAM-CMOS co-integration are shown in Figure 4.9(a)-(h) (see SI 1 for the detailed process flow). The process starts with photolithography to access the areas that host the memory cells. First, 1.8 μm of SiO_x/SiN passivation layer on the Al (M6) is removed through reactive ion etching (RIE) using CF_4. Then, the Al is selectively etched away by the RIE etching with Cl_2/BCl_3 to access the underlying W via (Figure 4.9(c,d)). The nm-scale W via defines the effective size of the final memory cells (280 nm). The dielectric layer of HfO_2 and Al_2O_3 are deposited using the atomic layer deposition (ALD) at 200°C. For the HfO_2, the deposition are performed from Tetrakisethylmethylamino Hafnium (TEMAH) and H_2O precursors. To deposit the Al_2O_3 layer, Trimethyl Aluminum (TMA) and H_2O precursors are used. Afterwards, 100 nm TiN is reactively sputtered at room temperature as the TE. The process then continues by applying another photolithography and RIE (Cl_2/BCl_3) to pattern the memory cells (Figure 4.9(e,f)). In next processing step, 100 nm TiN is reactively sputtered at room temperature and patterned as the memory TE (Figure 4.9(e,f)). Finally, another 100 nm of TiN film is deposited and patterned by RIE to make an electrical connection between the memory cell and the measurement pads, see Figure 4.8(g,h). The surface morphology of the ReRAM active areas has been analyzed using atomic force microscopy (AFM). The AFM map on W via BE (Figure 4.8(f)) reveals that the peak to peak roughness is about 10 nm, confirming that planarization processing steps are not required [9].

Structural characterization

The device microstructure and chemical mapping were investigated in cross-sectional samples using FEI Titan Themis transmission electron microscopy (TEM) at 60-300 kV equipped with

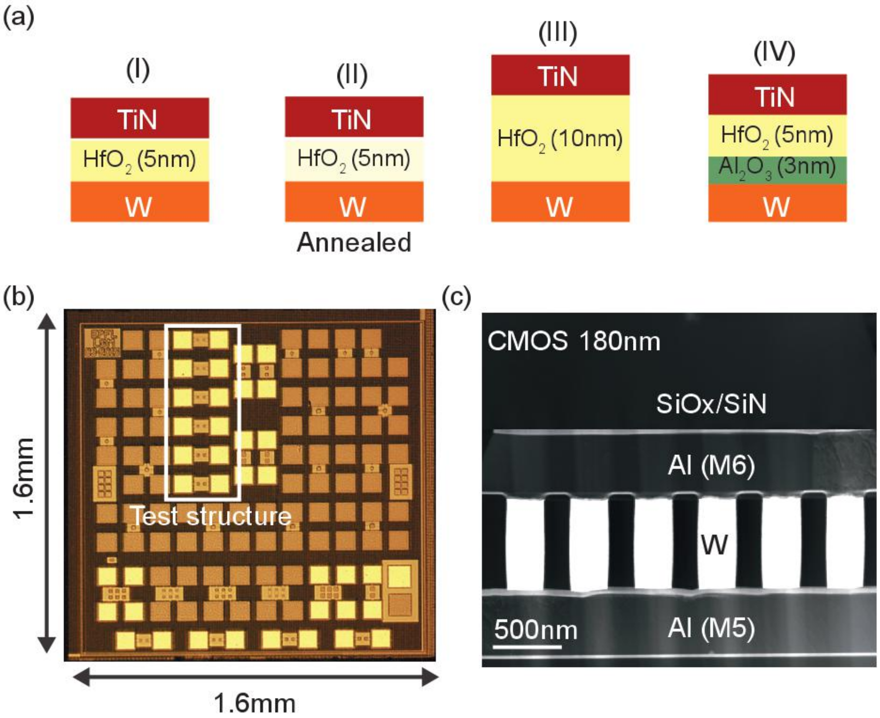


Figure 4.8 – (a) Schematic structure for the CMOS co-integrated (W/ HfO_2(5 nm)/TiN), (W/ HfO_2(5 nm)/TiN-annealed under vacuum), (W/ HfO_2(10 nm)/TiN), and (W/ Al_2O_3 (3 nm)/HfO_2(5 nm)/TiN) ReRAM devices. (b) An optical micrograph of the foundry-processed CMOS 180 nm technology test chip. The marked test structure shows the memory area with the probe pads. (c) Cross-sectional TEM image of the CMOS 180 nm chip from metal 5 (M5) to metal 6 (M6) layer. ReRAM cells are fabricated on the top of W via between Al M5 and M6 layers.

the SuperX^{TM} energy dispersive X-ray spectroscopy (EDX) technology for the (W/ HfO_2(10 nm) /TiN), and (W/ Al_2O_3 (3 nm)/HfO_2(5 nm)/TiN) ReRAM device configurations. TEM sample lamella preparation were performed using a FEI Nova 200 nanolab DualBeam focused ion beam (FIB) system. The device micrographs were obtained using a Zeiss Merlin scanning electron microscope (SEM) operating at 3 kV. An AFM imaging was conducted on a Bruker's Dimension FastScan AFM system and was carried out on the W via after etching the Al metal layer using the tapping-mode acquisition setup.

Electrical characterization

The current-voltage (I-V) properties of the integrated ReRAM cells were measured by using an Agilent B1500A semiconductor device parameter analyzer and PA200 probe station. For all the I-V tests, the bias-voltage was applied on the TE while the BE was grounded and no compliance current (I_{cc}) was employed. All the devices show bipolar switching behavior with

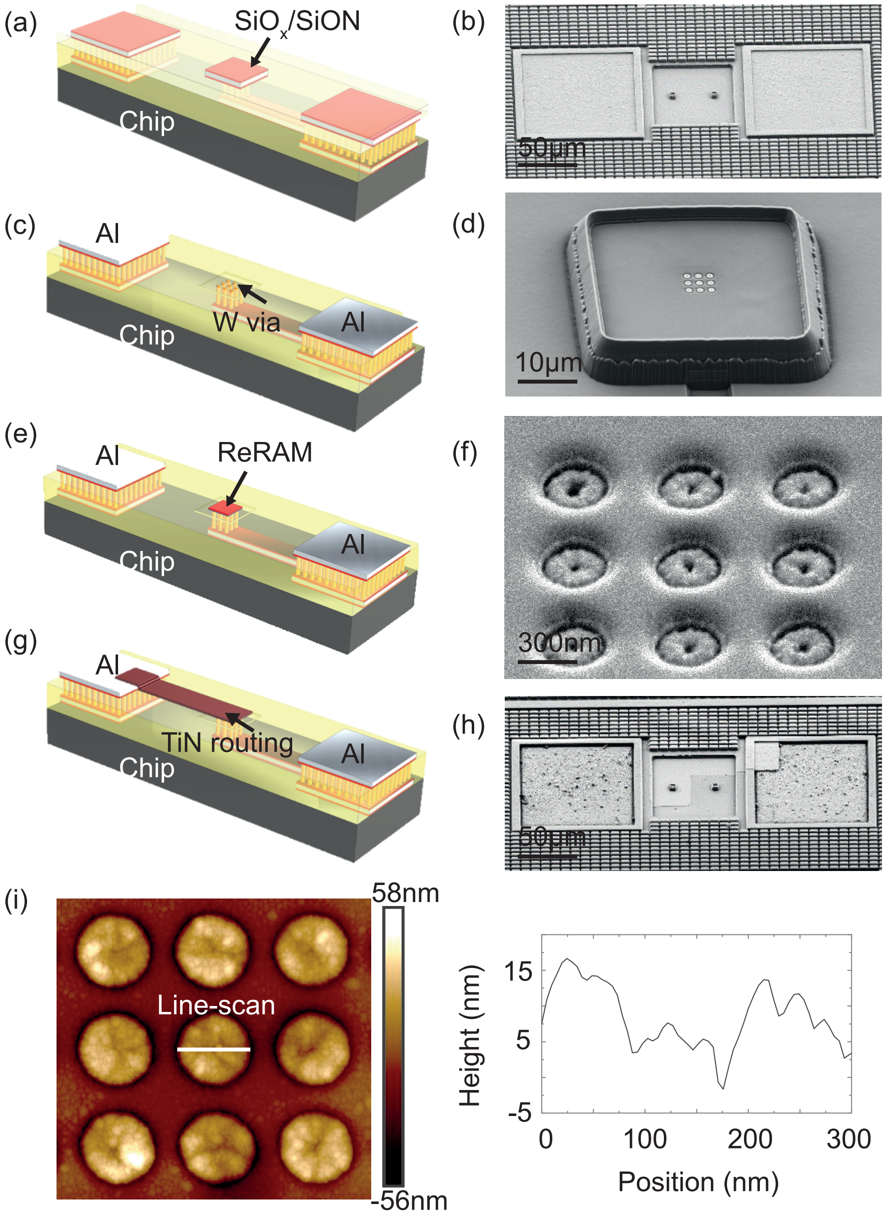

(a)
SiO$_x$/SiON
Chip
(b)
50µm
(c)
Al
W via
Chip
Al
(d)
10µm
(e)
Al
ReRAM
Chip
Al
(f)
300nm
(g)
Al
TiN routing
Chip
Al
(h)
50µm
(i)
Line-scan
58nm
-56nm
Height (nm)
15
5
-5
0
100
200
300
Position (nm)

Figure 4.9 – The schematic process flow and respective SEM micrograph of the W-based ReRAM chip-level co-integration. The flow starts with (a) and (b); chip cross section in which the small square hosts the ReRAM device and the larger squares are the pads for the electrical measurements. (c) and (d) are the W vias after etching the $\mathrm{SiO}_x/\mathrm{SiN}$ passivation and Al (M6) layers. (e) and (f) are the enlarged W vias after dielectric and TiN TE layer deposition. (g) and (h) are ReRAM device routing to the pads for the electrical characterizations. (i) AFM topography imaging over 2x2 μm^2 area and peak to peak roughness measurement on the 300 μm W via.

the negative *Set* and positive *Reset* operation. The reading operation is performed at 0.5 V.

Results and Discussions

The DC switching characteristics of the four different W-based ReRAM integrated cells were studied. Of the ReRAM device configurations, the (W/ HfO_2(5 nm)/TiN) device did not show stable switching properties. The cells require high operating voltage (-6 V to 6 V), while the memory remained at the LRS state being unable to switch resistance states after a few cycles (see SI 2). Moreover, the device tended to show high current fluctuation through the *Set* operation before the abrupt change to *Set* regime occurs. The high operating voltage and the fluctuations in the *Set* operation decrease the device reliability and degrade device performance quickly. The high current fluctuations may arise from the microstructural features of the interface between the W electrode and HfO_2 switching layer. Tungsten readily oxidizes and can form a variety of different oxide compounds, e.g., WO_2, $WO_{2.72}$, $WO_{2.90}$, $WO_{2.96}$ and WO_3 with different Gibbs free energies (ΔG), ranging from -550 $Kjmol^{-1}$ to -750 $Kjmol^{-1}$ [55]. The W electrode undergoes a continuous oxidation from WO_2 to WO_3 to form the most thermodynamically stable oxide. Though W oxidizes readily, compared to other low-work function electrodes like Ti and Hf, it has a higher barrier to oxidation |ΔG|. That is, in the initial states of the ReRAM performance, higher driving forces are required to form the stable WO_3 phase [131]. During *Set* operation and before the formation of a stable conductive filament (CF), there is a stochastic creation of oxygen vacancies ($V_{\ddot{O}}$, following the $Kr\ddot{o}ger - Vink$ notation [118]) due to the sequential and spontaneous W oxidation which require high operating voltage to reach steady state. Therefore, the inefficient oxygen exchange properties of W electrode result in an O_2 deficient HfO_2 layer that fails quickly in the LRS regime.

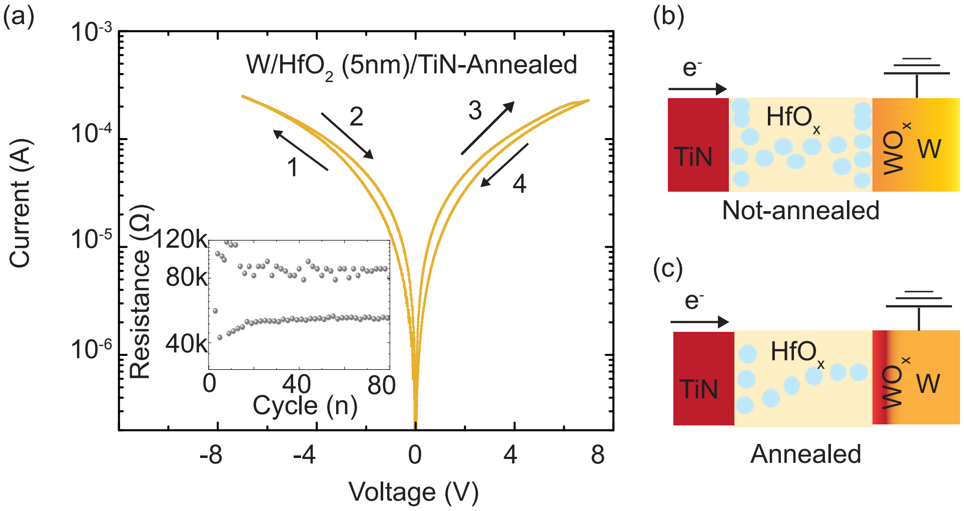


Figure 4.10 – (a) Bipolar resistive switching I-V curve for the co-integrated annealed (W/HfO_2 (5 nm)/TiN) ReRAM, The inset shows endurance characteristics over 90 cycles read at 0.5 V. (b) A schematic of the switching mechanism for the (W/HfO_2 (5 nm)/TiN) before and (c) after O_2 ambient annealing at 300°C for duration of 5 min.

To control the W oxidation at W/HfO_2 interface and produce more reliable devices, different solutions and processing steps were proposed and tested. As a first step, we annealed the devices under an O_2 rich environment to thermodynamically stabilize the WO_x phase formation on the W via interface and reduce oxygen extraction from the HfO_2 layer. Secondly, the thickness of the HfO_2 switching layer was increased to minimize the dielectric leakage. Lastly, we added a thin Al_2O_3 barrier layer to limit the oxygen diffusion to the W electrode. The ALD deposited Al_2O_3 provides a good barrier against oxygen diffusion due to the large Al-O bonding energy and high band-gap [160] and prevents the W electrode from scavenging oxygen, thereby preserving the stoichiometry and the electronic properties of the HfO_2 layer.

W/ HfO_2 (5 nm)/ TiN-annealed

The I-V curve for the (W/ HfO_2 (5 nm)/TiN-annealed) is shown in Figure 4.10(a). The samples are annealed in the O_2 environment using JETFIRST 200 Rapid Thermal Processing (RTP) machine. The process is carried out with the heating ramp of 5 s, at 300°C for 5 min. The voltage is swept from 0 → -7 V → 0 V in which the memory performs a small self-compliance *Set* operation, and for the voltage sweep of 0 → 7 V → 0 V, the memory *Resets* slightly, though no steep current transition is observed. The device switches with stable HRS of 90 kΩ and LRS of 50 kΩ. The endurance measurement over 90 cycles is shown in Figure 4.10(a)-inset, demonstrating higher switching stability and uniformity compared to not-annealed (W/ HfO_2 (5nm)/TiN) devices. The improved stability may relate to a reduced density of defects in the annealed sample. The schematics of the proposed switching mechanism for the (W/ HfO_2 (5 nm)/TiN) memory before and after annealing are depicted in Figure 4.10(b,c). Annealing in the O_2 environment at 300°C, thermodynamically stabilizes the WO_x formation on the W via interface and minimizes the W oxygen leaching from HfO_2. Thus, the HfO_2 layer has fewer oxygen vacancies, generating preferred electronic properties that do not alter with cycling due to the stable diffuse barrier formed by the tungsten-oxide. The HfO_2 layer's low defect density enhances switching uniformity while reduces the HRS/LRS resistance ratio due to the high LRS value.

W/ HfO_2(10 nm)/ TiN

Figure 4.11(a) shows the bipolar resistive switching I-V curve for the co-integrated (W/HfO_2 (10 nm)/TiN) cell. The voltage is swept from 0 → -2 V(step 1) → 0 V (step 2) → 3 V (step 3) → 0 V (step 4). In the negative voltage region, the memory switches to the LRS at -1.5 V and increases current towards -2 V; the current is limited without applying the I_{CC}. In the positive voltage region, the LRS retains up till +2 V, and the memory switches back to the HRS gradually at 3 V. The calculated HRS and LRS are 9 kΩ and 4 kΩ, respectively. The decreased operating voltage suggests that by increasing HfO_2 thickness, the formation of WO_x phases by leaching O from HfO_2 is only partially affects the layer thickness. Though an oxygen gradient within the

HfO_2 layer results, the electronic properties are preserved. The oxygen gradient also assists CF confinement, leading to the partial rupture/formation at lower operating voltage. The cell endurance over 90 cycles is plotted in Figure 4.11(b) in which the LRS degrades in the HRS regime after 50 cycles. For the first few cycles, the formed WO_x layer leaks current but does not influence the resistance states significantly. After applying a higher number of negative *Set* operation cycles, HfO_2 becomes depleted in oxygen and the WO_x layer becomes thicker and transitions to the more stable WO_3 phase which adds resistance to the HfO_2 switching layer and increases the total LRS (Figure 4.11(d)). To quantitatively investigate cycle-to-cycle (CTC) uniformity, the mean (μ) and normal standard deviation (σ) of LRS and HRS are calculated as (3.63 kΩ, 0.43) and (7.98 kΩ, 0.36) where the LRS shows higher variation (Figure 4.11 (c)).

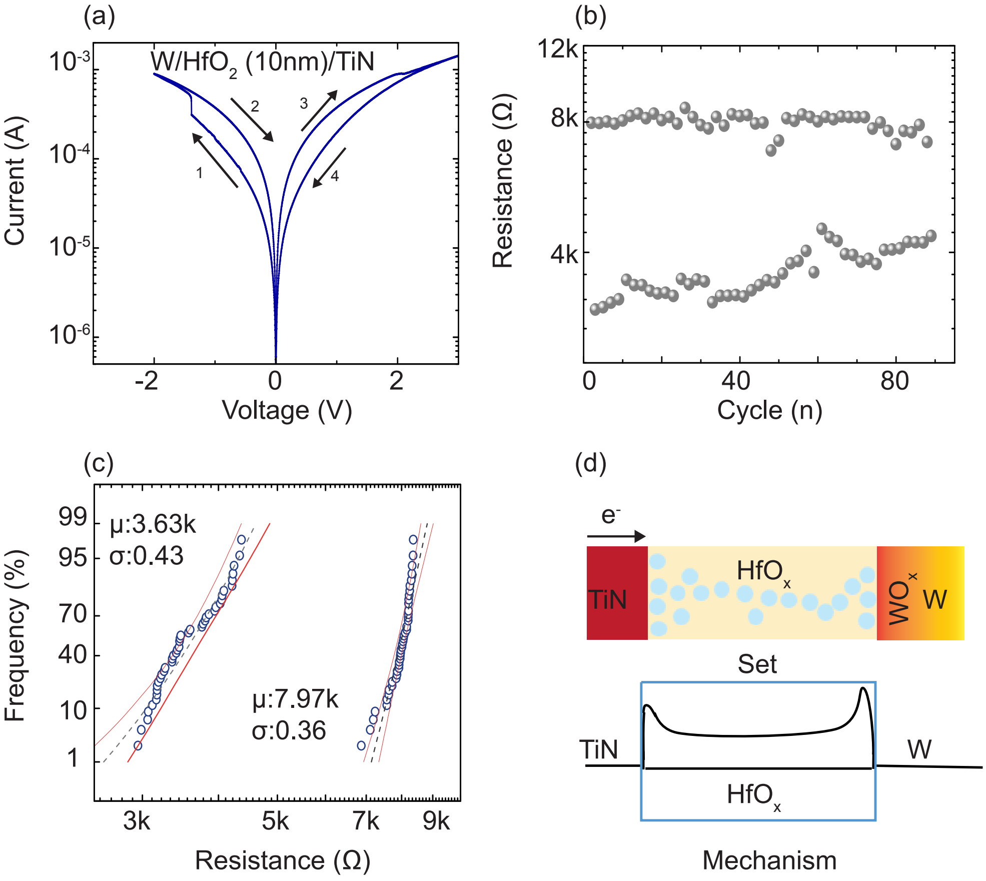


Figure 4.11 – (a) Bipolar resistive switching I-V curve for the co-integrated (W/HfO_2 (10 nm)/TiN) ReRAM, (b) Endurance measurements for 90 cycles read at 0.5 V. (c) Cumulative distribution of HRS and LRS with standard deviation fit in gray dash line. The mean (μ) and normal standard deviation (σ) are reported. (d) A schematic of the switching mechanism for the (W/HfO_2 (10 nm)/TiN) in the negative Set operation.

W/ Al_2O_3 (3 nm)/ HfO_2 (5 nm)/ TiN

Figure 4.12(a) shows the DC bipolar switching performances of the co-integrated (W/Al_2O_3(3 nm)/HfO_2 (5 nm)/TiN) ReRAM devices. For the *Set* operation the voltage is applied from 0 → -3 V(step 1) → 0 V (step 2) with no I_{CC}. The sample switches from HRS to LRS at -1 V while the HRS state is retained to the voltage of -2 V. The device continues to function in the self-rectifying *Set* operation to -2.5 V and reaches a current of 1 mA at -2.5 V. Then, the voltage is swept from 0 → 3 V (step 3) → 0 V (step 4), and the LRS switches back to the HRS gradually at a voltage range of 2 V to 3 V. Figure 4.12(b), presents the cell resistance endurance measurements for 100 cycles. After 40 cycles, both HRS and LRS reach a state of high stability with the value of 20 kΩ and 3 kΩ, respectively. For the C2C variability assessment, the (μ) and (σ) of HRS (17.82 kΩ, 4.11) and LRS (3.5 kΩ, 0.9) are evaluated for switching over a 100 cycles and reported in Figure 4.12(c). It is evident that (W/Al_2O_3(3 nm)/HfO_2 (5 nm)/TiN) shows a greater resistance ratio (HRS/LRS = 6) in comparison to the (W/ HfO_2 (10 nm)/TiN) and (W/HfO_2 (5 nm)/TiN-annealed) with the resistance ratio (HRS/LRS) of 3 and 2.5, respectively (SI 3). The addition of the Al_2O_3 layer having a high barrier potential and low oxygen mobility [140, 141] inhibits W oxidation and provides the necessary asymmetric barrier potential with respect to the electrical field direction, improving overall device performance [98].

Conduction Mechanism

To investigate the conduction mechanism of the co-integrated (W/Al_2O_3(3 nm)/HfO_2 (5 nm) /TiN) ReRAM, the bipolar I-V curves in both *Set* and *Reset* operation have been replotted in the log-log scale to determine the power law relationship ($I \propto V^m$). Double-logarithmic I-V curves are shown in Figure 4.13. The fitted slope trends indicate that conduction is governed by a trap-controlled space charge limited current (SCLC) mechanism. According to the standard SCLC theory [12], there are three main sections: low-field region, which corresponds to the Ohm's law ($I \propto V^1$), the Child's square region ($I \propto V^2$), and steep current jump in the high-field region. The current density J at the high-field region is given by the following equation:

$$J = \frac{9}{8}\theta\varepsilon_r\varepsilon_0\mu(\frac{V^2}{d^3}) \tag{4.1}$$

Where, θ is the ratio of the free electrons to the shallow trapped electrons, ϵ_0 is the permitivity of free space, ϵ_r is the static dielectric constant, μ is the electron mobility, V is the applied voltage and d is the film thickness. The CF characteristics in HfO_2-based ReRAM [161] [162] can be described by a mechanism in which both oxygen ions and charge carriers contribute to control CF profile under an electrical field with respect to the electrodes. In the *Set* regime (Figure 4.13 (a,b)) , with the negative bias voltage on the TE, the electrons start to pass through

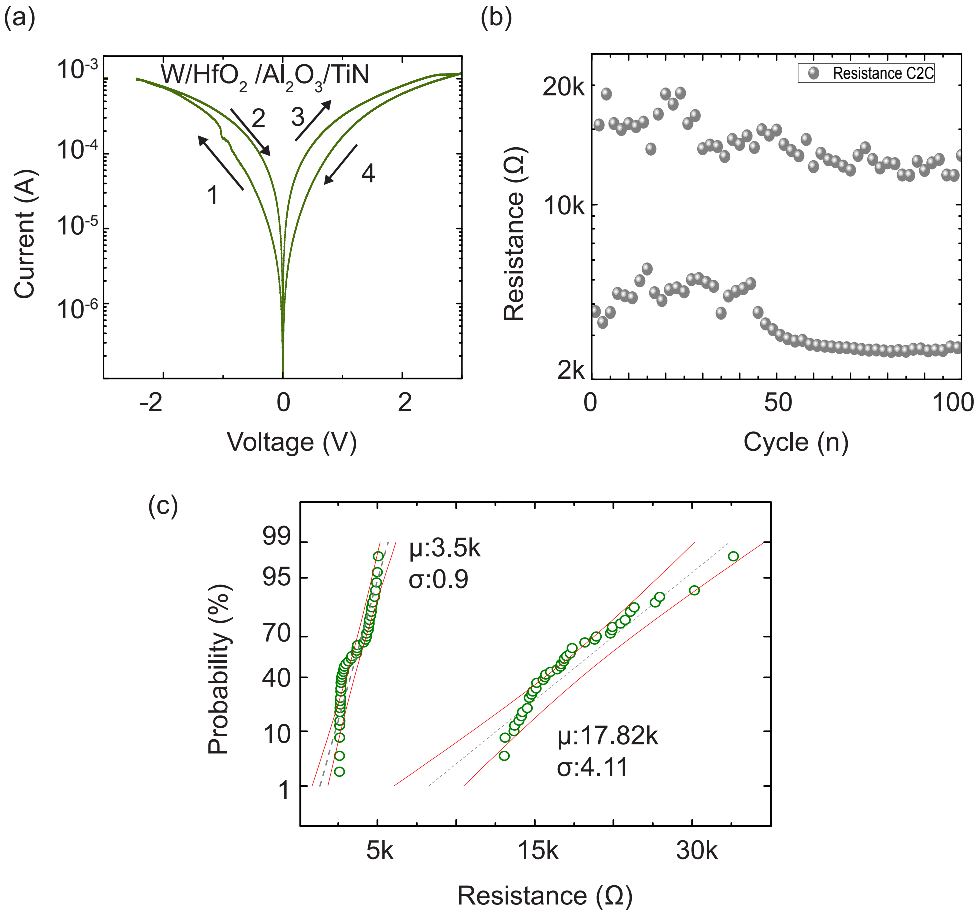


Figure 4.12 – (a) DC bipolar I-V switching obtained from integrated (W/Al_2O_3(3 nm)/HfO_2 (5 nm)/TiN) ReRAM (b) DC resistance endurance measurements for 100 cycles switching. (c) Cumulative distribution of HRS and LRS with standard deviation fit in gray dash line. The mean (μ) and normal standard deviation (σ) are reported.

the TiN/HfO_2 interface. From 0 V up to -0.27 V, the number of injected electrons is lower than the thermally generated free electrons in the oxide film, indicating that the traps are empty. Therefore, the current follows the Ohm's law. Increasing the voltage from V_{ON} (-0.27 V), provides a higher density of injected electrons and the traps become filled which reduces the trap's barrier height for electron transport, resulting in a deviation of the trend in the I-V curves from an Ohmic conduction mechanism to that of an SCLC mechanism (from -0.27 V to -0.91 V). After the trap-filled region (V_{TFL}=-0.91), there is a small jump in the current, and the memory switches from HRS to LRS. When the voltage is swept back to V_{ON}, the traps are still full and the trend in the I-V curve exhibits non-Ohmic conduction behavior. After the V_{ON} is reached the carrier injection rate decreases, and the device I-V curve trend follows an Ohmic-conduction mechanism. In the *Reset* operation regime (Figure 4.13 (c,d)), when the positive bias is applied on the TE, the electrons inject from the W/Al_2O_3 interface that

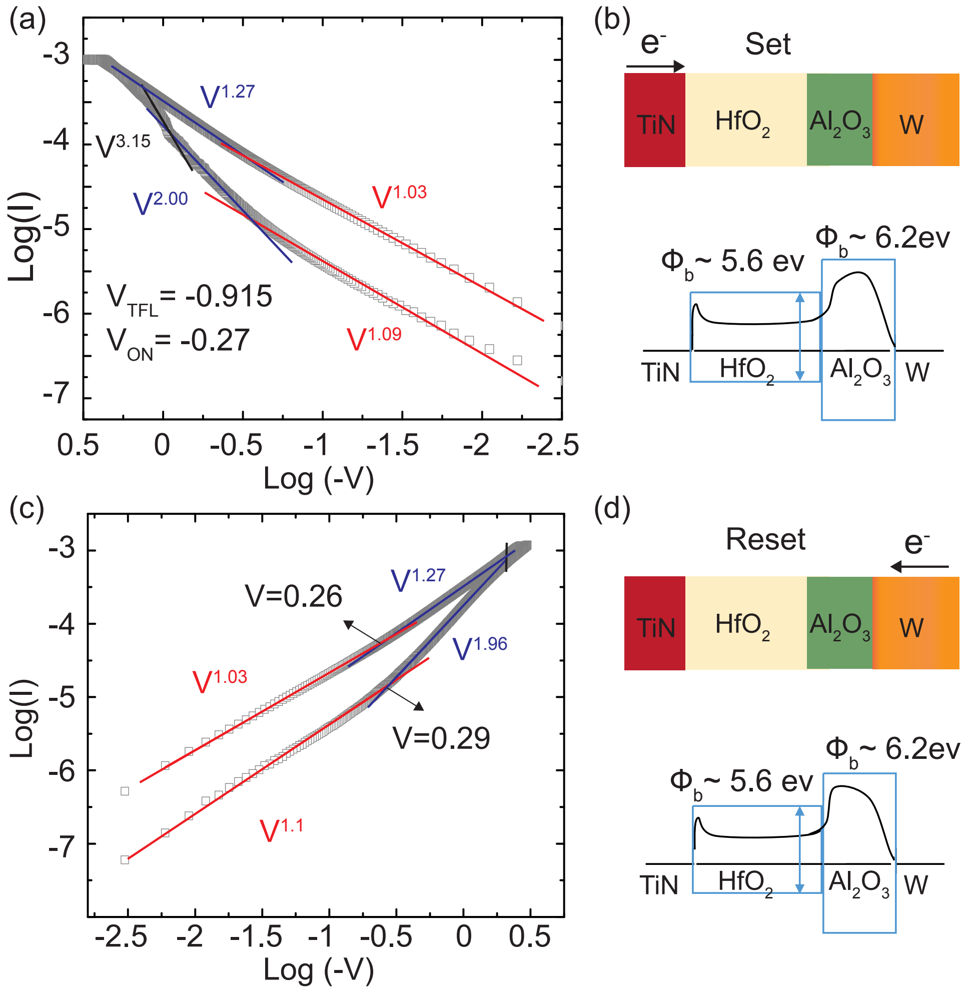


Figure 4.13 – The I-V characteristics from the CMOS co-integrated (W/Al_2O_3(3nm)/HfO_2 (5nm)/TiN) plotted on a double-logarithmic scale. a) Negative voltage region for the *Set* operation and b) positive voltage region for the *Reset* operation. The corresponding slopes for the different regimes determined by a linear fit are presented in the plots. (c) Schematic drawing of the band diagram for the W/Al_2O_3(3nm)/HfO_2 (5nm)/TiN in the negative *Set* operation. (d) Schematic drawing of the band diagram for the W/Al_2O_3(3nm)/HfO_2 (5nm)/TiN in the positive *Reset* operation.

has a higher barrier potential compared to the TiN/HfO_2 interface due to the presence of Al_2O_3 [47, 120]. The traps being full from the previous cycle, and the positive voltage not being strong enough driving force to empty the traps, increasing the applied positive bias provides increased electron injection from the W/Al_2O_3 interface. As a result, the current deviates from the Ohmic conduction mechanism. With decreasing voltage, the I-V curve trend changes, showing a slope of 2 for voltages above 0.29 V, corresponding to the trap-electron discharging (SCLC mechanism) in which the device switches from LRS to HRS. Decreasing of the voltage further from 0.29 V to 0 V induces the Ohmic conduction mechanism in which the traps are empty. The transition voltages are not similar between the positive-bias region (0.27 V) and negative-bias region (0.29 V). The slight difference is due to the different barrier potential height of the TiN/HfO_2 compared to the W/Al_2O_3 as shown in Figure 4.13 (b,d). In the positive-voltage region, the electrons consume a certain amount of voltage to pass through the higher barrier potential (W/Al_2O_3(3 nm)) which results in a higher voltage transition value.

Material Characterization

The device design aim of adding an Al_2O_3 layer stack is to prevent oxygen from diffusing into the W bottom electrode and leaching O from the HfO_2 layer that causes detrimental degradation of its electronic properties. In the memory device architecture without Al_2O_3 diffusion barrier, we observe near the interface of the W electrode and HfO_2 layer a significant drop in O content in the HfO_2 layer with the uncertainty error of absolute EDS values (~ ± 10 at %). The line-scan in Figure 4.14(b,c) shows that the O and Hf contents do not reach the same level (oxygen level is higher), showing elevated O content in the W electrode after 20 nm position from the W/HfO_2 interface. In the contrary case of (W/Al_2O_3(3 nm)/HfO_2 (5 nm)/TiN) sample (EDS results shown in Figure 4.15 (b,c)), Hf, O and Al atomic fraction have the same base level after a distance of 15 nm, confirming there is no gradient in O across the interface and that Al_2O_3 layer is an efficient diffusion barrier. Complimentary to the EDS results, the layer thicknesses measured from the STEM and EDS images match the reported thickness of the ALD deposited HfO_2 (5 nm) and Al_2O_3 (3 nm) on W via in the microfabrication of the devices.

Device Simulation

To define the device characteristics for a circuit design, the results of the integrated (W/Al_2O_3(3 nm)/HfO_2 (5 nm)/TiN) ReRAM are fit using a SPICE (simulation program with integrated circuit emphasis) compact model, developed by Guan et al [163]. The model is translated from Verilog-A into MATLAB code. The fit is performed on the average switching IV curve for a series of 100 cycles (black line), as shown in Figure 4.16(a). The fitting parameters of the obtained simulation results are listed in Figure 4.16(b). This model is compatible for multiple conduction mechanisms that are associated with ReRAM switching, i.e., for trap-assisted tunneling, Poole-Frenkel emission, Fowler-Nordheim tunneling, and direct tunneling in which the current is defined as an exponential function of the voltage and the gap based on the following equation:

$$I = I_0\, exp(\frac{-g}{g_0})\, sinh(\frac{V}{V_0}) \tag{4.2}$$

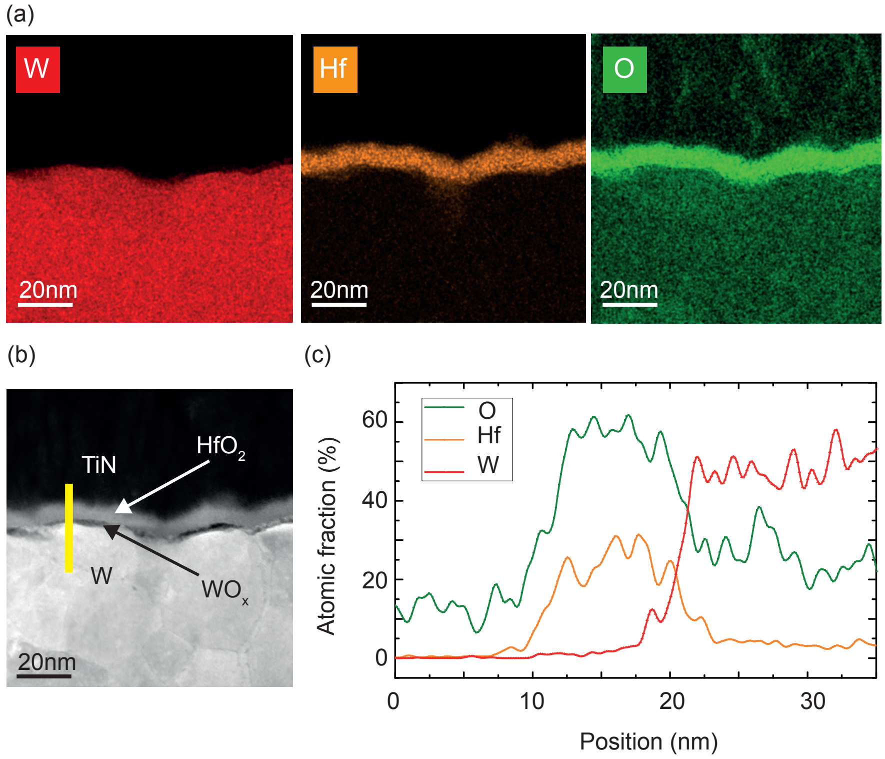


Figure 4.14 – (a) HRTEM-EDX maps for W, Hf and O. (b) HAADF image of the co-integrated (W/ HfO_2 (10 nm)/TiN) ReRAMs. (c) The EDX results for the atomic fraction variation of the W, Hf and O versus the distance from TiN to the TE along the entire yellow line-scan. EDS measurements with low signal over background are prone to large uncertainty errors, especially for low Z elements, which are detected in ranges with an inherently high X-ray background. Also, measurements using a standardless quantification method are less accurate for the absolute values of low Z materials, as can be seen for higher base value (~ 10 at.%) for O in vacuum region of the sample. Thus, O content will have the fictitious elevated value shown in the plots.

$$dg/dt = -v\,exp(\frac{-qE_a}{TK_b})\,sinh(\frac{qVa_0}{t_{ox}k_bT}) \tag{4.3}$$

where g is the gap length between the filament end and the electrode, v is velocity containing the attempt escape frequency, E_a is the activation energy, a_0 is the atomic spacing, t_{ox} is the oxide thickness and γ is an enhancement factor considers the uniform potential distribution in the cell and the polarizability of the material. k is the Boltzmann constant and q is the elementary charges. I_0, g_0 and V_0 are the fitting parameters. The details of the equations and the complete list of the fitting parameters are available in (SI 4).

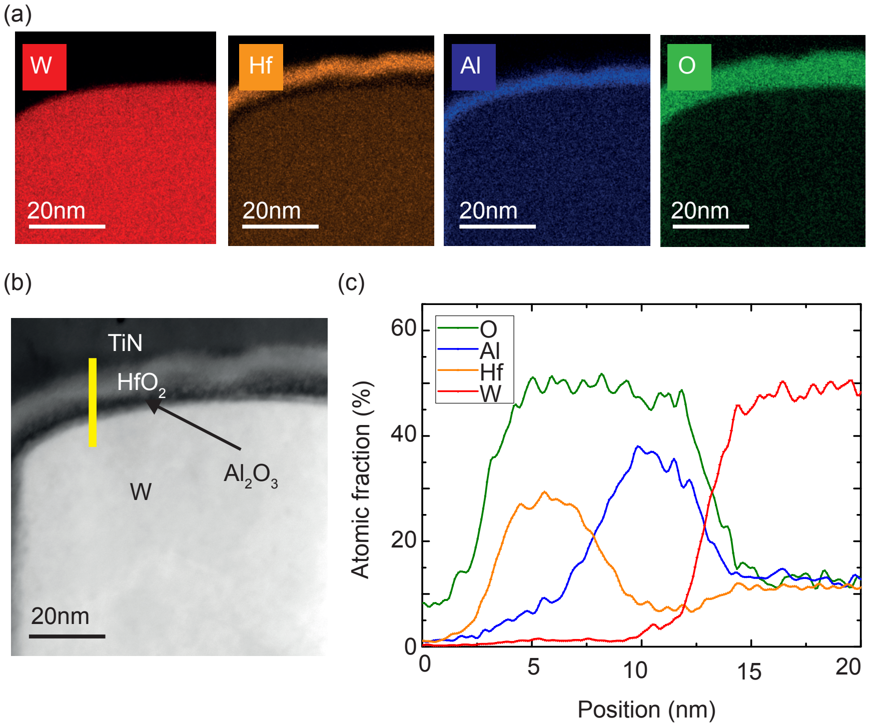
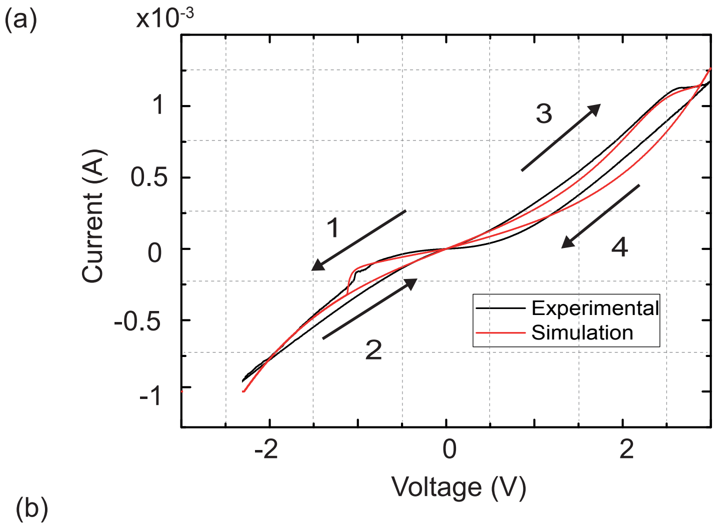


Figure 4.15 – (a) HRTEM-EDX maps for W, Hf, Al and O. (b) HAADF image of the co-integrated (W/Al_2O_3(3nm)/ HfO_2 (5nm)/TiN) ReRAMs. (c) The EDX results for the atomic fraction variation of the W, Hf, Al and O versus the distance from TiN to the TE along the entire yellow line-scan. Please note as in the case EDS measurements shown in Figure 4.14, large uncertainty errors exist for the absolute values of oxygen. However, the precision in comparative trends in the measured elements is high and valid.

Conclusion

In this paper, we have ascertained a technique for the hybrid integration of nm-scale ReRAM on the foundry-produced CMOS 180 nm technology chip. W vias from the CMOS BEoL stack are used as the ReRAM bottom electrode which brings high density, scalability, reliability and compatibility for the CMOS-ReRAM post-processing. We have carefully investigated the material property requirements for the reliable W-based ReRAM performances. The effect of W oxidation is modulated in different co-integrated ReRAM stacks by increasing HfO_2 switching layer thickness, post-metalization annealing under O_2-ambient, and adding Al_2O_3 layers that acts as an O diffusion barrier. The role of Al_2O_3, as an oxygen barrier layer at W interface has been observed using TEM. It has been shown that the incorporation of a thin (3 nm) Al_2O_3 layer at the W interface prevents the W electrode layer from scavenging oxygen, resulting in lower power consumption and more stable switching behavior in comparison to the previously reported results. All the co-integrated stacks show self-rectifying behavior with an operating current less than 1 mA, and the co-integrated $W/Al_2O_3/HfO_2$/TiN exhibits HRS



(b)

Parameter	Name	Value	Unit
Fitting parameter	g_0	1.6e-9	m
Fitting parameter	V_0	1.12	V
Fitting parameter	υ	1.1	nm/ns
Fitting parameter	I_0	300e-6	A
Activation energy	E_a	0.45	ev
Hopping distance	a_0	0.25e-9	m
Oxide thickness	t_{ox}	8e-9	m

Figure 4.16 – (a) Linear DC I-V average curve of the integrated (W/Al_2O_3(3 nm)/HfO_2 (5 nm)/TiN) ReRAM (black line) and the simulated I-V curve (red line). (b) Table of the model's fitting parameters used for the simulations.

of 20 kΩ and the LRS of 3 kΩ with the self-compliance *Set*/*Reset* operation of -2 V/3 V at 1 mA and the switching mechanism is well described by the SCLC mechanism.

Supplementary information

A supplementary PDF file including the complementary DC characterization, TEM material study, test setup and Model fitting parameters is attached.

Acknowledgment

The authors thank Dr.Jury Sandrini for his valuable advices in device fabrications and Tolga Celik for his help on the device modeling. The authors are thankful to the staff of the Center of Micro/Nanotechnology (CMi) of EPFL for the helps and supports. The authors gratefully acknowledge Dr.Lucie Navratilova at CIME-EPFL for the FIB lamella samples preparations. This research has been partially funded by a grant provided by Samsung Electronics.

Supplementary Information

Performance improvement of the chip-level CMOS-integrated ReRAM cells through material optimization

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Process flow

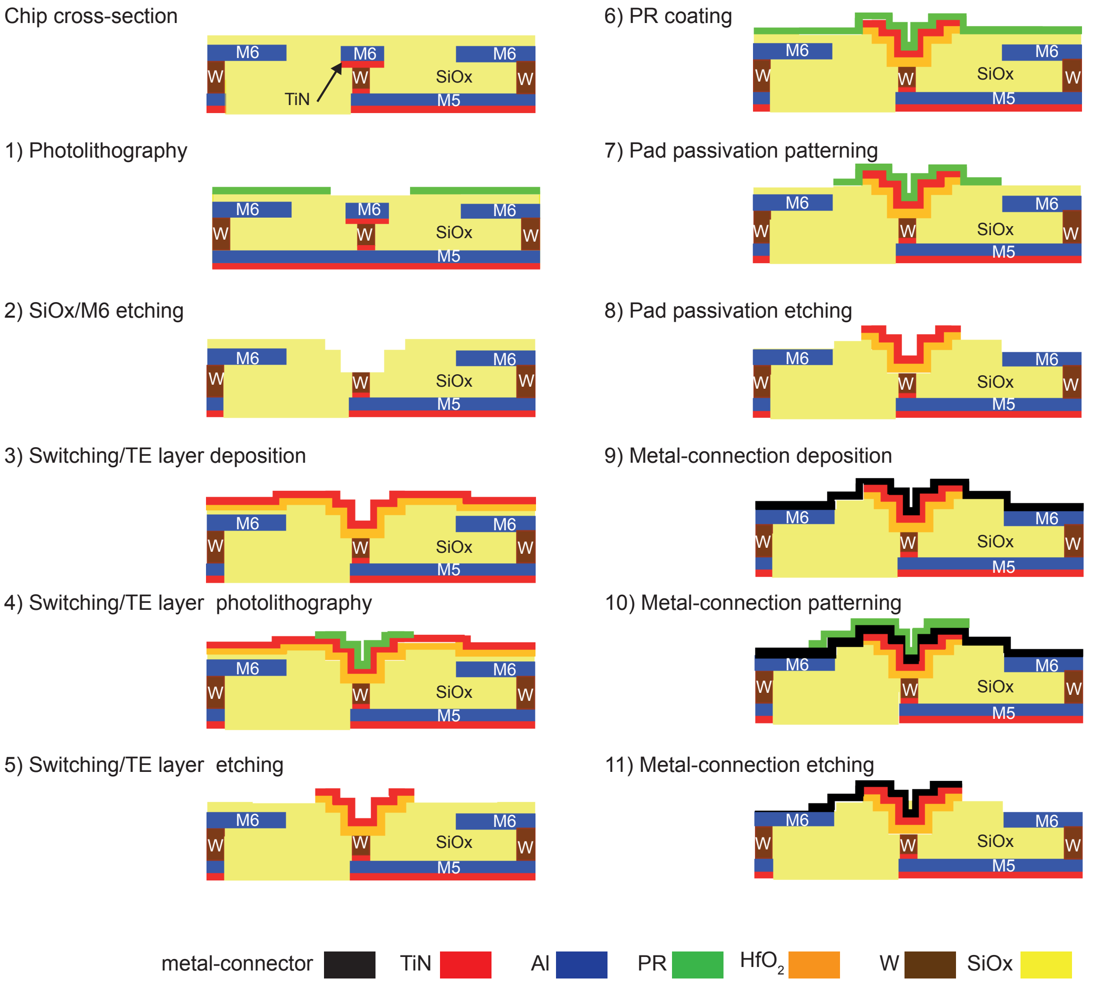
Chip cross-section
M6
M6
M6
W
W
W
SiOx
TiN
M5
1) Photolithography
2) SiOx/M6 etching
3) Switching/TE layer deposition
4) Switching/TE layer photolithography
5) Switching/TE layer etching
6) PR coating
7) Pad passivation patterning
8) Pad passivation etching
9) Metal-connection deposition
10) Metal-connection patterning
11) Metal-connection etching
metal-connector
TiN
Al
PR
HfO2
W
SiOx

Figure 4.17 – The schematic details of process flow for the W-based ReRAM chip-level co-integration

W/ HfO_2 (5 nm)/TiN

Figure 4.18 shows an overview of the DC I-V performance of the co-integrated (W/ HfO_2 (5 nm)/TiN)ReRAM. The device is not able to switch at the operating voltage < (-4 V, 4 V). We have progressively increased the applied voltage and the memory switched at (-6 V, 6 V) while after few cycling, it stucked at the LRS. The memory has not been able to switch back to HRS even through an application of higher reset voltage (10 V).

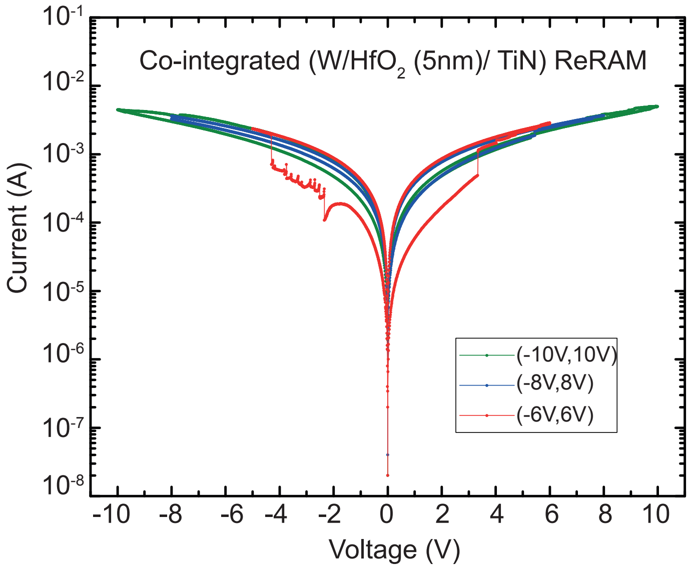

Figure 4.18 – DC I-V characteristics of the co-integrated (W/ HfO_2 (5 nm)/TiN) ReRAMs.

Device comparison

Figure 4.19 demonstrates cycle-to cycle distributions of the HRS and LRS for the integrated devices. The calculations have been carried out on 100 cycles per each stack. (W/ Al_2O_3 (3 nm)/HfO_2 (5 nm)/TiN) ReRAM shows higher resistance window with more variations. One should notice, the main part of resistance fluctuations particularly the LRS is related to the first few cycles before the cell stabilized as shown in the paper.

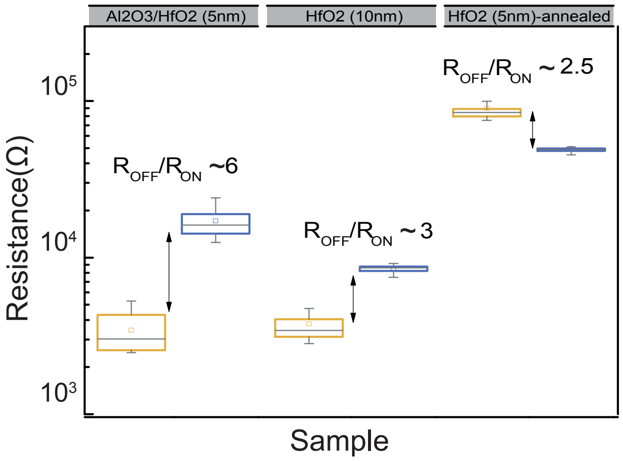

Figure 4.19 – The Cycle-to-cycle distribution of HRS and LRS for the integrated (W/ Al_2O_3 (3 nm)/ HfO_2 (5 nm)/TiN), (W/ HfO_2 (10 nm)/TiN) and (W/ HfO_2 (5 nm)/TiN-annealed) ReRAMs. For the boxplots, the horizontal line within the box presents the median value while the upper and lower lines of the box show the first and third quartile receptively. The data is calculated over 100 cycles per each stack.

SPICE model fitting parameter

Table 4.2 – Parameters Used for the Integration Fits

Parameter	name	value	unit
Average switching fitting parameter	g_0	1.60e-9	m
Average switching fitting parameter	V_0	1.12	V
Average switching fitting parameter	$Velo$	1.1	nm/ns
Average switching fitting parameter	I_0	300e-6	A
Average switching fitting parameter	$beta$	0.35	1
Gamma initial value	γ_0	10	A
Average switching fitting parameter	γ_{neg}	2.5	A
Model type (Static, Dynamic)	model-switch	0	NA
Threshold temperature	T_{crit}	500	K
Variation fitting parameter	$deltaGap$	0.02	m
Variation smoothing parameter	T$_{smth}$	600	K
Activation energy	Ea	0.45	ev
Hopping distance	a_0	0.25e-9	m
Initial device temperature	T_{ini}	298	K
Minimum field requirement	F_{min}	0.51e8	V/m
Initial gap distance	gap_{ini}	10e-10	m
Minimum gap distance	gap_{min}	15e-12	m
Maximum gap distance	gap_{max}	10e-10	m
Thermal resistance	R_{th}	110e3	K/W
Oxide thickness	t_{ox}	8e-9	m
Time step	$time-step$	1e-9	s

This section details the model described in the paper. The Verilog-A model developed by Guan et al. [163] is translated to MATLAB. The program takes as an input the experimental results for the current and the voltage input; then the fitting parameters can be used to fit the I-V curves. A stochastic model of the filament, which includes the effects of temperature, and the current compliance can also be incorporated.

The model uses a local temperature variable T and a variable γ, which is affected by the electric field, to determine the change of gap width. The gap width is defined as the distance of the tip of the filament to the opposite electrode and determines the resistance level. The gap changing rate is defined according to the following equations:

$$\frac{d\langle g\rangle}{dt} = v_0 \exp\left(\frac{-E_a}{kT}\right)\sinh\left(\gamma\frac{qa_0V}{t_{ox}kT}\right), \quad \langle g\rangle \geq g_{min} \tag{4.4}$$

where v_0 is the velocity containing the attempt-to-escape frequency, E_a (E_m) is the activation energy (migration barrier) for vacancy generation (oxygen migration) in a Set (Reset) process, t_{ox} is the thickness of the oxide, a_0 is the atomic spacing, V is the voltage across the memory, g_{min} is the minimum gap size at which the filament is assumed to be in contact with the opposite electrode. γ is the local enhancement factor, which is defined as:

$$\gamma = \gamma_0 - \beta g^3 \tag{4.5}$$

where β and γ_0 are the fitting parameters. The noise term for modeling the stochastic temperature-dependent filament migration and the total gap width are given as:

$$\delta_g(T) = \frac{\delta_g^0}{1 + \exp\left(\frac{T_{crit} - T}{T_{smth}}\right)} \qquad g|_{t+\Delta t} = \int \left(\frac{dg}{dt} + \delta_g \chi(t)\right) \tag{4.6}$$

where T_{crit} (400-450K) is a threshold temperature above which significant random variations occur, $\chi(t)$ is standard Gaussian noise, with δ_g^0 and T_{smth} (smoothing factor) fitting parameters. The local temperature depends on the voltage, current and thermal resistance.

$$T = T_0 + VIR_{th} \tag{4.7}$$

Finally, the current is given with an exponential dependence on the gap width and a hyperbolic dependence on the voltage.

$$I = I_0 \exp\left(-\frac{g}{g_0}\right) \sinh\left(\frac{V}{V_0}\right) \tag{4.8}$$

Where again the g_0 and V_0 are fitting parameters for the gap width and the voltage. The parameters, used for the co-integrated (W/ Al_2O_3(3 nm)/HfO_2 (5 nm)/TiN) ReRAM fits are given in Table4.2.

Material characterization

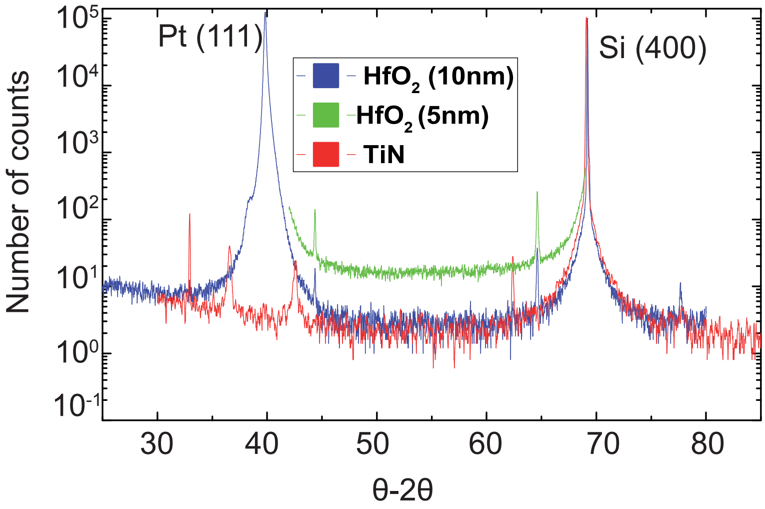

Figure 4.20 – XRD pattern for the as ALD deposited HfO_2 10 nm (blue line), HfO_2 5 nm (green line) and sputtered TiN film (red line)

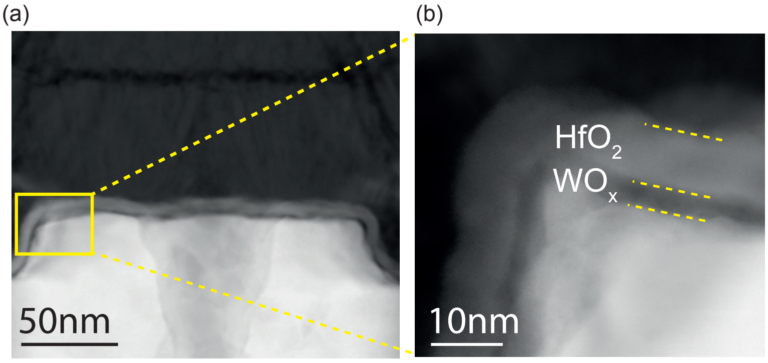

Figure 4.21 – HAADF TEM micrograph of the a) co-integrated (W/ HfO_2 (10 nm)/TiN) ReRAMs b) enlargement of W electrode interface showing the formation of the thin layer WO_x beneath HfO_2 layer.

The texture of the ALD deposited 10 nm and 5 nm HfO_2 switching layer as well as the sputtered TiN TE were determined separately by Bruker D8 advanced X-ray diffractometer using the scan method (θ- 2θ) which is shown in Figure 4.20. Two major peaks in the HfO_2 10 nm corresponds to Pt (111) and Si (400) that are deposited as an inert film on the substrates. The two minor peaks from both 10 nm and 5 nm HfO_2 at 44 ° and 64 ° are correlated to HfO_2 (211) and HfO_2 (123), respectively. The results indicates that the ALD deposited HfO_2 has two crystalline direction components. No significant difference was observed between the 10 nm and 5 nm HfO_2. For the as-deposited TiN, the most significant peaks are found at 36 °, 42 ° and 62 ° that indicate TiN (111), TiN (200) and TiN (220) respectively. The reported work function value [164] for the TiN (111) and TiN (200) is about 4.5 eV.

Figure 4.21a, shows the HAADF TEM micrograph of the co-integrated (W/ HfO_2 (10 nm)/TiN) ReRAMs and Figure S4.21 b is the high magnification of the W/ HfO_2 interface revealing the formation of the thin layer WO_x beneath HfO_2 layer.

5 Fast ion conducting thin films for resistive switching

The high density of mobile oxygen vacancies is believed to have a profound impact on lowering the filament formation energy and device power consumption. Thus, it is substantial to consider the fast ion-conductor film, i.e. CGO and YSZ, as the promising candidates for the switching layer of ReRAM. A systematic evaluation of CGO and YSZ thin film based ReRAM was performed. We have extensively studied the thin film processing conditions impact on the performance of switching layers. The process is optimized in order to achieve the minimum forming energy, stable resistance states as well as operating voltage. Furthermore, the pulse endurance characteristics were carried out to determine the qualified functionality of CGO and YSZ based ReRAMs. The first part of this chapter is dedicated to the feasibility study of efficient switching behavior in CGO and YSZ thin films. Finally, the further scaling process optimization and stack engineering have been performed on the CGO-based ReRAM. For the first time, the outstanding electrical characteristics have been achieved for the (Pt/CGO (14 nm) /Al (3 nm) /TiN), including operating voltage of (-2 to 1 V) at 150 µA, high endurance of 10^5 *with the 100 µs pulse width and the capability of multi-level switching by the careful pulse programming operation. This results is presented in a paper format which is in preparation for the publication.*

5.1 Fast ion conductive materials

Ion conducting materials mostly exhibit fluorite related structures as an open structure that has an exceptional tolerance for a high concentration of atomic disorder introduced by doping and non-stoichiometric phase due to the oxidation or reduction [165]. Doping with di- or trivalent cations substitutes, e.g. gadolinium or yttrium, results in the formation of oxygen vacancies to preserve the charge neutrality. The created oxygen vacancies increase the ion conductivity. Doped CeO_2 and doped ZrO_2 are the most well-known examples of oxide with fluorite structure with high ion conductivity that are also investigated at thin film scale [166]. The crystal structure of Gd doped cerium oxide consists of simple cubic oxygen lattice while cerium or gadolinium ions occupy alternate body centers as shown in Figure 5.1. The substitution of 20% Ce^{4+} with Gd^{3+} produces 5% vacant oxygen sites as a result of the charge neutrality. Meaning, for every two Gd^{3+}, there is a corresponding creation of one oxygen vacancy. The Gd doping concentration strongly influences the mobility of created oxygen vacancies. Schmitt et al. reported the Gd doping concentration of 20% associates with the highest number of "free" oxygen vacancies while the vacancies become immobile at higher concentration of Gd (>20%) decreasing the ion conductivity [4].

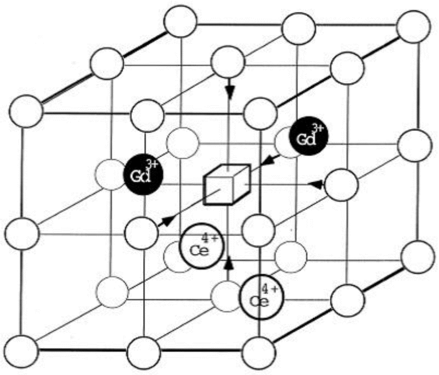

Figure 5.1 – Schematic view of the Gd-doped ceria (CGO) lattice structure [10].

Likewise, zirconium oxide doping by Y^{3+} leads to the creation of oxygen vacancies that contributes to the ion conductivity. The initial purpose of Y doping is in fact to stabilize the zirconia structure over wide temperature ranges in order to avoid the structural phase change. The main difference of Gd-doped ceria (CGO) and yttrium stabilized zirconia (YSZ) is the dual valance feature of cerium (Ce^{3+} and Ce^{4+}) that in non-stoichiometric or reducing conditions can lead to higher number of oxygen vacancies and increased ion conductivity. This makes both and in particular CGO thin films as interesting materials to be used as the switching layer in ReRAMs.

This section presents a systematic evaluation of CGO and YSZ thin film potential to be utilized as the switching layer for ReRAM. In the device structure, Pt and TiN are used as the bottom and top electrode, respectively. We have extensively studied the thin film processing conditions impact on the performance of switching layers. The process is optimized in order to achieve the minimum forming energy, stable resistance states as well as operating voltage. Furthermore, the pulse endurance characteristics with the pulse width of 50 μs were carried out to determine also the qualified functionality of CGO and YSZ based ReRAMs. The results provide a better insight on the dynamic of conductive filament evolution in which the multi-filament and single-filament formation are proposed as the control mechanism of CGO and YSZ switching, respectively.

5.2 Experimental methods

Device fabrication

The process starts with the bottom electrode (BE) deposition, Ti/Pt (5/100nm) sputtered film at room temperature, on 100 mm Si wafer passivated with 500 nm SiO_2. After BE patterning, a passivation layer using 100 nm low temperature SiO_2 (LTO) deposition via LPCVD technique was carried out to avoid the bottom and top electrode contact. To form the memory active area 1-10 µm wide via were etched through the LTO layer using BHF solution. Afterwards, the wafer was diced into 2×2 cm^2 chips. Before switching layer and top electrode (TE) deposition, a chip-sized shadow mask was installed on the chips to fabricate multi ReRAM cells (Figure 5.2(a)). The Si-based shadow masks were prepared using conventional deep reactive ion etching (DIRE) accompanied by wafer grinding to obtain the trenches of 300 µm square side. It is important to have a sufficient large trenches for the correct via alignment. CGO and YSZ depositions were performed using RF magnetron sputtering as the ReRAM switching layer. Finally, a 100 nm TiN TE was sputter deposited at room temperature to complete the device structure. The schematic view of the device fabrication is presented in Figure 5.2(b).

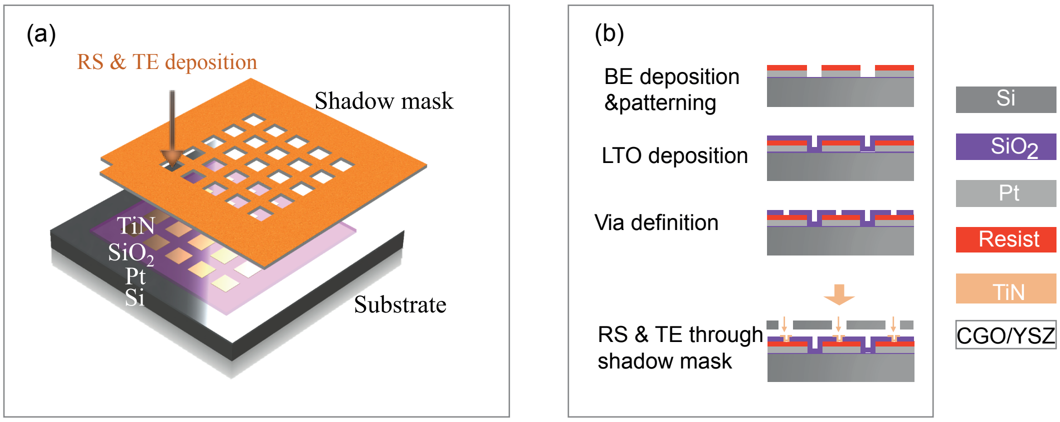

Figure 5.2 – Fabrication of ReRAMs through the shadow mask process (a) Schematic representation of resistive switching layer and top electrode deposition through the shadow mask membrane. (b) Fabrication process flow of ReRAMs. The silicon substrate consists of 500 nm thick SiO_2 covered with the 5 nm/100 nm Ti/Pt sputtered film. After the patterning of Pt bottom electrode, 100 nm of SiO_2 is deposited by LPCVD. The vertical "in-via" patterns are defined by BHF etching ranging from 1µm to 10µm in size. Later, the substrate is protected by the shadow mask membrane. The resistive switching layer and 100 nm TiN top electrode will be sputtered and patterned through the shadow masks.

Thin film processing

The details of the deposition parameters for the electrodes and switching layers are presented in Table 5.1. Ti and Pt are deposited using the magnetron sputtering tool (Pfeiffer SPIDER 600 Cluster) at room temperature. The Ti layer was acting as an adhesion layer for the Pt BE. The TiN layer was deposited as TE with an Alliance-Concept DP650 in which the TiN target is placed 30 mm away from the substrate. CGO and YSZ were deposited in Nordiko magnetron sputtering tool at room temperature from $Ce_{0.8}Gd_{0.2}O_{1.9}$ and $(Y_2O_3)_{0.08}(ZrO_2)_{0.92}$ targets, respectively. The deposition rate for the YSZ has been already evaluated as 4 nm/min while for the CGO, the rate had to be measured. Initially, two depositions for 1h and 2h were made on dummy wafers to evaluate the approximate deposition rate and thin film uniformity along the wafer. Figure 5.3(a) shows the thickness of deposited layer in steps of 0.5 mm along the wafer diameter using the mechanical profilometer. The average deposition rate was about 3 nm/min. The further depositions with the smaller duration of 5 min and 10 min were carried out in which the more precise rate was calculated for the small range of film thickness as 4.4 nm/min. The SEM micrographs of later depositions are shown in Figure 5.3(a-b). The deposition rate was further confirmed using TEM-microstructural characterization (see next section).

Table 5.1 – Electrode and switching layer deposition condition by means of sputtering technique

Type	Thin film	Deposition pressure (mTorr)	Power (W)	Ar flow (sccm)	Temperature (C)
Electrode	Ti	2.7	1000 (DC)	9	RT
	Pt	2.7	1000 (RF)	15	RT
	TiN	3.7	200 (RF)	30	RT
Switching layer	CGO	10	200 (RF)	10	RT
	YSZ	15	200 (RF)	30	RT

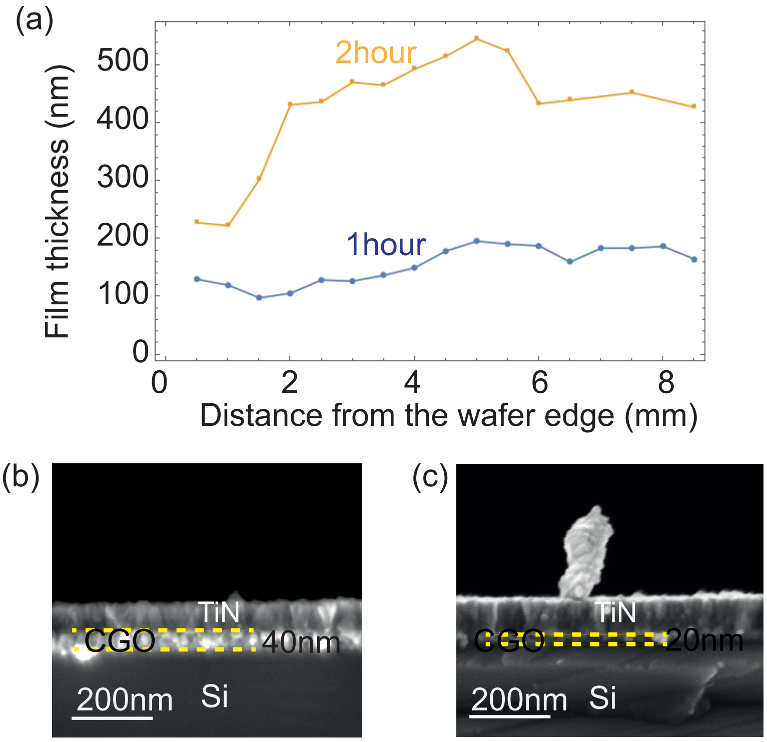

Figure 5.3 – (a) Thickness of deposited film along the wafer diameter for two different disposition times of 1 h and 2 h. The SEM cross-sectional micrographs of the CGO deposited for the durations of (b) 5 min and (c) 10 min.

Electrical characterization

The DC electrical characterization was performed using a Keysight B1500 semiconductor device parameter analyzer in the dark room environment and in the quasi-static conditions. The bias voltage was applied on the ReRAM TE while the BE is grounded. Initially the cells were at the high resistance states and a positive voltage sweep was applied to "form" the devices. After forming, a negative voltage has been applied to "Reset" the device (LRS to HRS). The process was followed by "Set" process (HRS to LRS) within corresponding (-2 to 2 V) voltages. During the forming and Set operations, 500 μA (I_{cc}) was used to limit the maximum current flowing through the test device. In order to evaluate the memories endurance, an AC Pulse measurement has been performed. A nMOSFET (IRLB8721PbF) is connected in series to the ReRAM device with the test fixture. The V_{gate} of 1.969 V corresponds to I_{cc} of 500 μA limits the current through the transistor during the Set pulse operation. For the read operation, a small fixed double ramp value between 200 mV to 250 mV is applied to minimize the resistance state variation during the read operation. The details of the pulse parameters are explained for each device accordingly.

5.3 Results and Discussion

CGO-Based ReRAMs

The impact of CGO thickness on the ReRAM switching performance were investigated. The (Pt/CGO/TiN) stacks with the CGO thickness of 24, 20, 18, 14 and 10 nm were fabricated in which the CGO 24 nm and 10 nm did not show stable switching performances and were excluded from the analysis. Figure 5.4 presents the forming voltage comparison of the CGO-based ReRAM with the thickness of 20 nm to 14 nm. As it was expected, the forming voltage increases by increasing the CGO thickness varying between 2.5 to 5 V. Moreover, by reducing the CGO thickness, the forming voltage variation is reduced due to the defect population effect [167]. The evolution of the LRS and HRS with respect to the CGO thickness are shown in Figure 5.5(a). The graphs include the analysis of several devices with different via dimension per each CGO thickness. It is notable that CGO 14 nm shows the better resistance window with smaller variations compared to the other stacks. Lower forming voltage results in more controllable defects creation and the more stable device performances. Regarding the Set/Reset voltage evaluation, the same consideration is valid. Therefore, in this work, we have mainly focused on the (Pt/ CGO (14 nm) /TiN) stack due to the smaller operating voltage with the better switching uniformity.

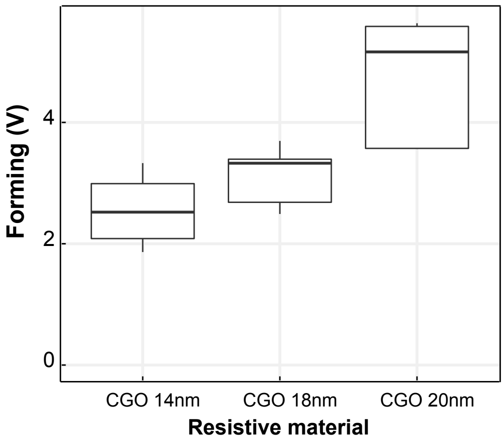

Figure 5.4 – The effect of CGO thickness variation on the forming voltage of (Pt/CGO/TiN) stacks.

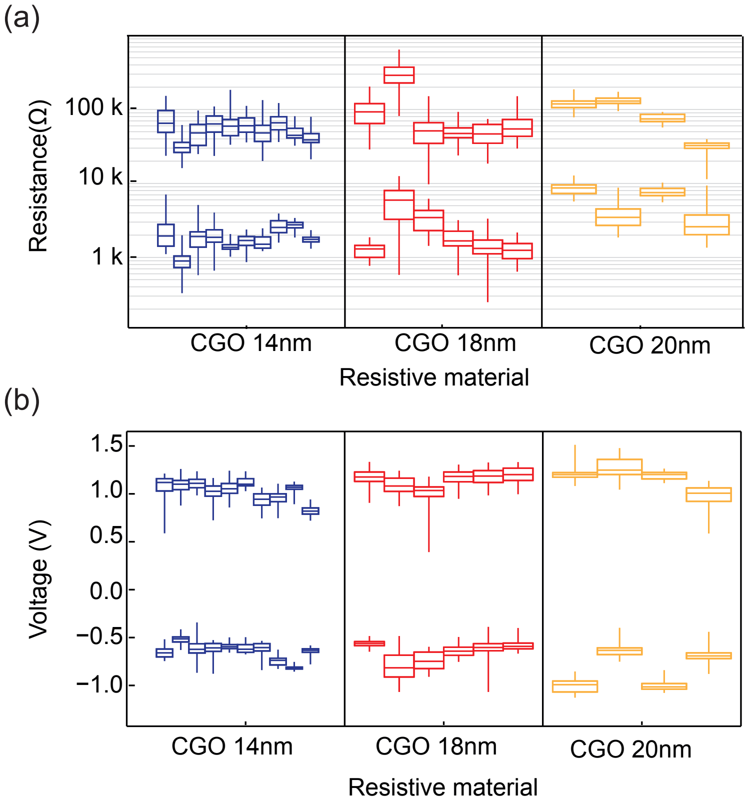

Figure 5.5 – The impact of CGO film thickness on the ReRAM (a) resistance states (LRS/HRS) and (b) operation voltages (Set/Reset)

Figure 5.6 shows the DC switching characteristics of (Pt/CGO (14 nm) /TiN). The forming voltage (2.3 V) is significantly lower compared to undoped CeO_x-based ReRAMs (7.2-10 V) [65, 78] revealing the enhanced number of oxygen vacancies. 20% Gd doping is expected to create 5% oxygen vacancies besides the ones that are generated due to the reduction of Ce^{4+} to Ce^{3+}. Hadad et al. [168] reported that the CGO thin films processing at room temperature that can have 2-4% additional oxygen vacancies due to cerium valance change. A reduction of 5-10% elastic modulus has been observed in room temperature samples that is correlated to 2-4% concentration of oxygen vacancy [169, 170]. The forming energy of our Gd (20%):CeO_x in comparison to the reported results of undoped ceria, Al doped structure (CeO_2/Al/CeO_2) [78] and even Gd (5%):CeO_x [171] has been reduced by factor of 20-110. The (Pt/CGO (14 nm) /TiN) cell shows an abrupt positive Set and gradual negative Reset behavior. The Set and Reset voltage distribution (Figure 5.5) are evaluated as V_{Set} (1 to 1.1 V) and V_{Reset} (-0.574 to -0.616 V). The resistance cycle-to-cycle stability over 100 cycles is presented in Figure 5.6 (b) showing the stable HRS and LRS with the median values of 40 $k\Omega$ and 1 $k\Omega$, respectively (V_{read}=± 0.25 V). There is a current overshoot of 1 mA in the first Reset cycle (marked in red) in Figure 5.6 (a). The overshoot current is mainly caused during the forming operation and correlates with the different parameters such as switching layer properties [172], device geometry and measurement setup [173]. The stochastic creation of thermally-assisted vacancies during the forming operation, results in fast current transition (in range of μs) that can not be recorded and limited by our parameter analyser and it is reflected to the first Reset cycle. In our case, the large TE sizes of ($300\times300\mu m^2$) and the common BE (Figure 5.2(a)) act as a series capacitor which excessing the overshoot current.

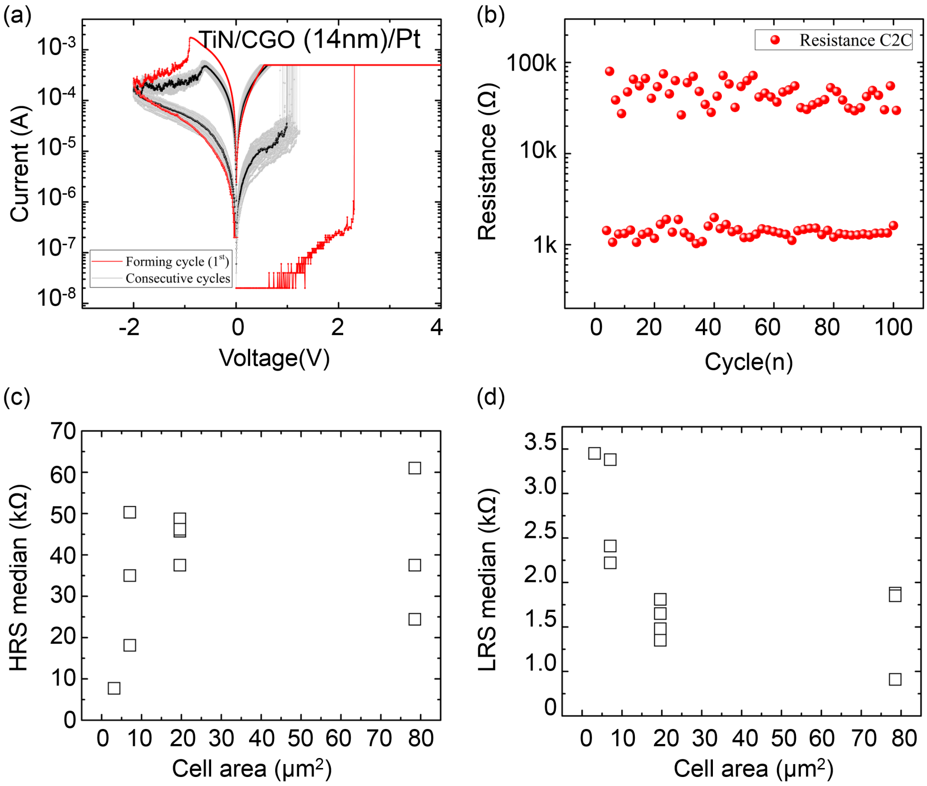

Figure 5.6 – (a) DC I-V switching characteristics for 14 nm CGO in 5μm via size. (b) The DC cycle-to-cycle resistance states uniformity over 100 cycles for 14 nm CGO at V_{read}=± 0.25 V. (c) The HRS trend as a function of device size and (d) the LRS trend as a function of device size.

To further understand the switching mechanism of CGO-based ReRAM, the impact of cell area on both HRS and LRS were investigated (Figure 5.6 (c,d)). The HRS does not exhibit any remarkable trend with respect to the cell area while LRS is prone to decrease by increasing the device area. This can be an indication of the multi-filament switching mechanism which all the filaments are ruptured in the Reset process. Since in the single filamentary-type switching , the LRS and HRS are independent to the cell area due to the nm-scale localized filament and in the interface-type switching, both LRS and HRS should scale with the device active area. The schematic of the proposed switching mechanism for the CGO-based ReRAM is presented in Figure 5.7.

Initially, the existing oxygen vacancies in CGO film are randomly distributed and are not yet

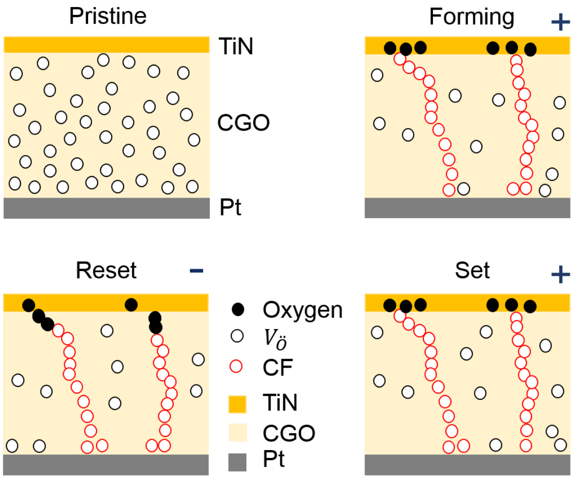

Figure 5.7 – Schematic view of possible mechanism for resistive switching in Gd doped ceria thin films

arranged to form the filaments, thus, the cell is at high resistance states. By applying a positive bias during the forming/Set operation, the oxygen ions push towards the TiN TE and the vacancies drift to create the conductive filament in which the device switches to the LRS. In Reset, when the negative bias is applied on TE, the oxygen ions drift back to CGO film and oxidize the vacancies which break the filaments. Thereby, the cell switches to the HRS. The lowered electrical potential in Set step compared to the forming voltage reveals that the filaments are not completely destroyed at Reset process.

The pulse endurance measurements have been carried out to further confirm the qualified functionality of CGO film as a switching layer for the ReRAM. Figure 5.8 shows the stable resistance switching obtained from 10^4 cycles with the Reset/Set pulse voltage of -2 V/1.5 V at the pulse width of 50 μs and the pulse slope of 20 %. The cell switches with the HRS value of 200 kΩ and LRS value of 3kΩ. The HRS/LRS ratio is almost doubled in AC mode compared to the DC measurements. In the AC mode, the CGO film receives smaller energy due to the small pulse duration. Therefore, there is lower number of conductive filaments leading to the higher LRS and better recovery of HRS in the Reset step.

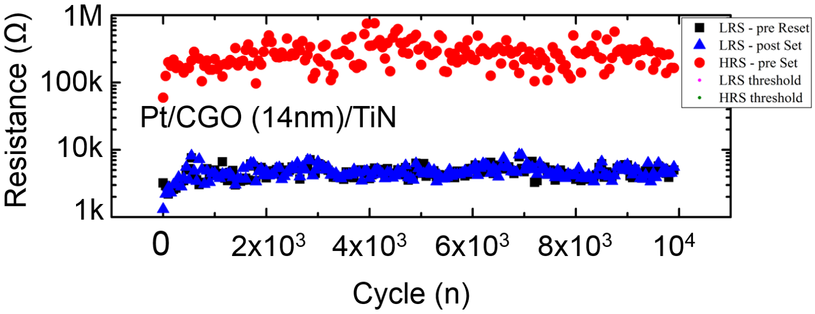

Figure 5.8 – The pulse endurance measurement of the (Pt/CGO (14 nm)/TiN) over 10^4 cycles with I_{cc}= 500μA and pulse width and slope of 50μs and 20% respectively.

YSZ-Based ReRAMs

The switching potential of the YSZ thin film was also studied in the (Pt/YSZ/TiN) ReRAM cells by varying the YSZ thickness in the range of 8 to 20 nm. The different switching parameters such as forming voltage, Set/Reset operating voltages and resistance values are evaluated in the several samples per each YSZ thickness. The statistical analysis exhibits that forming voltage is increasing from 2.5 V to 6.9 V by increasing the YSZ thickness from 8 nm to 20 nm and the device-to-device variation is also higher at the thicker YSZ film (Figure 5.9). The evolution of the LRS/HRS and Set/Reset voltages with respect to the YSZ thickness are shown in Figure 5.10(a-b). unlike the lower operating voltage of YSZ 8 nm, the cells are prone to show high switching variation which could be due to the low sputtered film uniformity or inadequate YSZ film thickness for stable switching properties. Among all, YSZ 12 nm shows the better resistance window with the better uniformity and we mainly focused on the (Pt/ YSZ (12 nm) /TiN) stack for the further analysis.

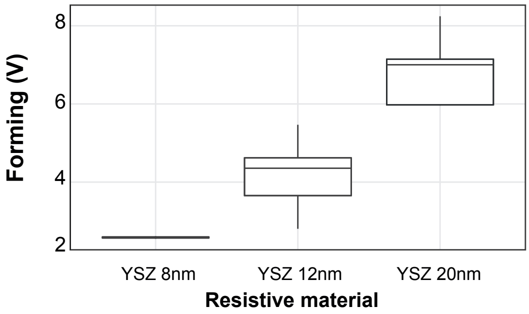

Figure 5.9 – The effect of YSZ thickness variation on the forming voltage of (Pt/YSZ/TiN) stacks.

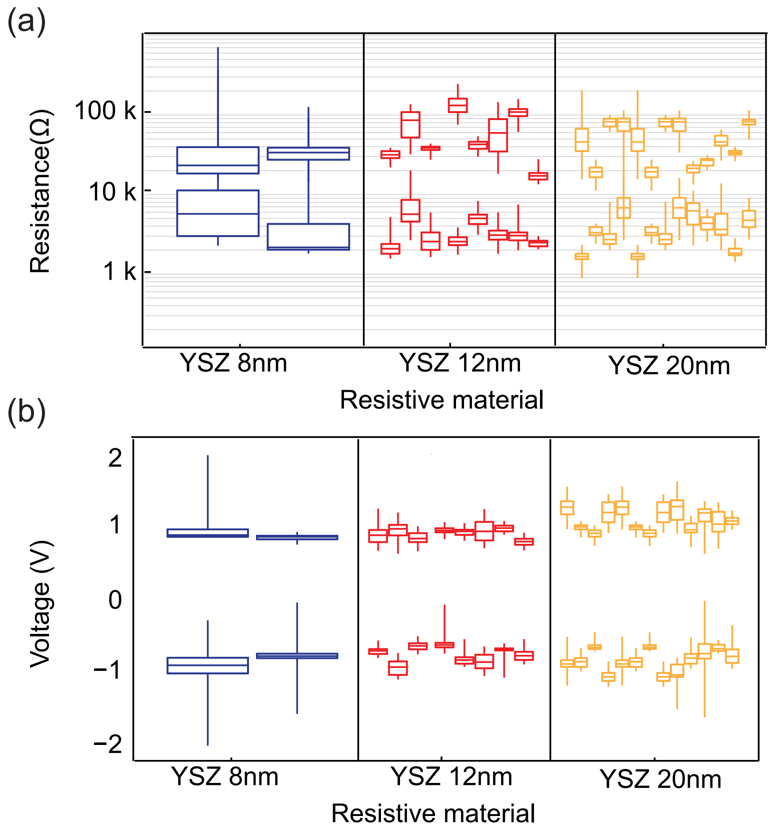

Figure 5.10 – The impact of YSZ film thickness on the ReRAM (a) resistance states (LRS/HRS) and (b) operation voltages (Set/Reset)

Figure 5.11(a-b) shows the DC I-V characteristics of 12 nm thick YSZ-based ReRAM and the cycle-to-cycle resistance variation for 100 cycles. The forming voltage compared to CGO 14 nm thin film is almost 2 times higher, 4.9 V. The difference between the required electric field for the formation of oxygen vacancies in CGO thin film (2.9 MV/cm) and YSZ (1.5 MV/cm) reveals the effect of Gd dopant on reducing the formation energy of vacancy. However, in comparison to the HfO_2 forming voltage at the same I_{CC} ($V_{forming}$=3.3 V for 5 nm thick HfO_2 layer), YSZ still requires the half of the electric field. The (Pt/YSZ (12 nm) /TiN) shows an abrupt Set transition with the Set voltage of 1 V while the Reset occurs gradually starting at the voltage of -0.6 V. The memory switches with the stable resistance states showing the median LRS and HRS of 3 kΩ and 80 kΩ, respectively. Unlike CGO-based devices, HRS and LRS does not pursue any trend by device size scaling (Figure 5.11 (c-d)) in agreement with the localized formation of filament across the YSZ film independent of the cell active area. The AC endurance pulse measurement was carried out using the Reset pulse value of -2 V and the Set pulse value of 1.5 V at the pulse width of 50 μs and the pulse slope of 20 % and no resistance degradation is observed up to >10^4 cycles. The device switches with the HRS median value of 100 kΩ and LRS median value of 3kΩ. The LRS is 6 times higher compared to DC mode while HRS is comparable to DC one showing that smaller number of vacancies are contributing during the Set in the AC mode due to the lower energy provided by the pulses. In addition, it is notable that LRS increments from DC to AC is more significant in YSZ compared to CGO revealing the higher number of mobile vacancies in CGO film suitable for the fast switching operation.

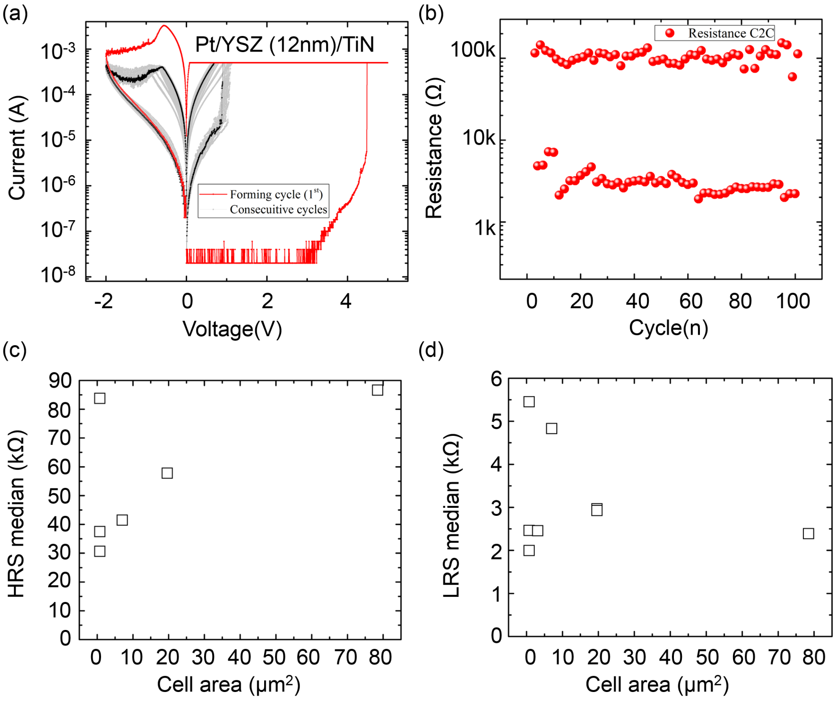

Figure 5.11 – (a) DC I-V switching characteristics for 12 nm YSZ in 5μm via size. (b) The DC cycle-to-cycle resistance variation over 100 cycles for 12 nm YSZ at V_{read}=± 0.25 V. (c) The HRS trend as a function of device size and (d) the LRS trend as a function of device size.

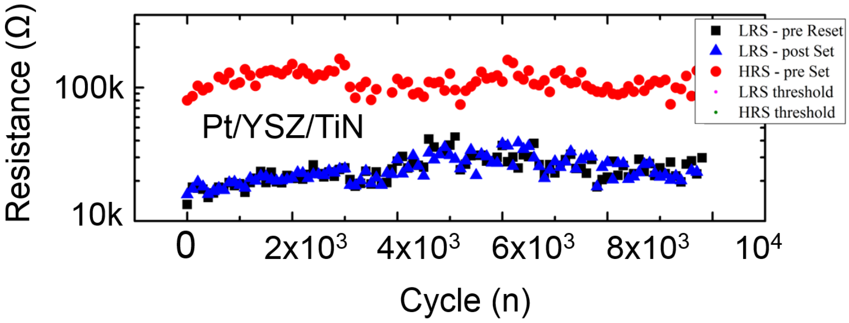

Figure 5.12 – The pulse endurance measurement of (Pt/ YSZ (12 nm)/TiN) devices over 10^4 cycles with the I_{cc}= 500μA and pulse width and slope of 50μs and 20% respectively.

Electrical forming process

One of the main concern for the ReRAM devices is the forming voltage dependency to the device area which can limit the ReRAM scaling feature [174] [175]. Even though that the forming is a one time process for the circuitry, it is important to ascertain the dependency of forming voltage with respect to the required memory size. Figure 5.13 shows the forming voltage versus the device via diameter for the CGO 14 nm, YSZ 12 nm and HfO_2 5 nm ReRAM cells. As it was expected, the forming is reducing with device enlarging owing to the number of defects are increasing by the device area.

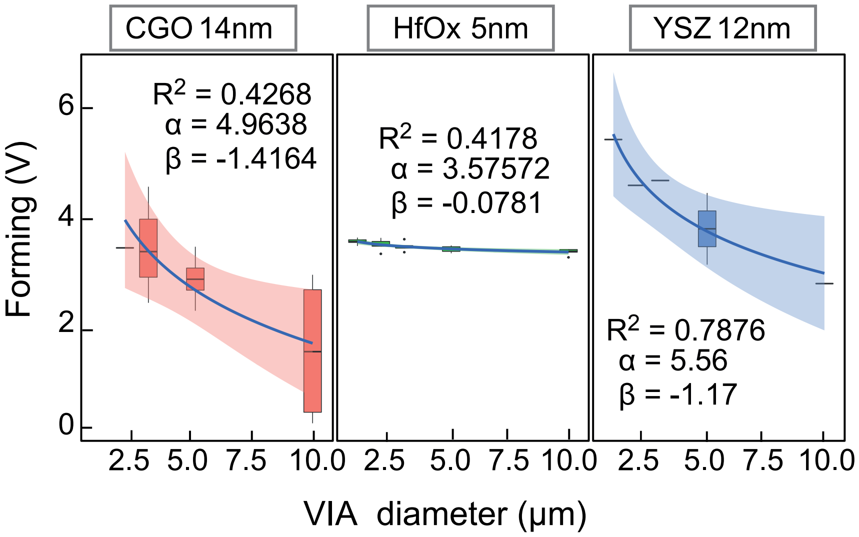

Figure 5.13 – Forming voltage versus device area for the CGO (14 nm), HfO_2 (5 nm) and YSZ (12 nm) ReRAM

The scaling trends of forming voltage are modeled using the first-order analytical model proposed by Chen et al. [167]. The model assumes that oxide contains of certain number of cells in which the forming occurs when a chain of cells (weakest line) with oxygen vacancies is created between BE and TE. The model is applicable for both single and multi-filament formation since the only difference is the number of cells that are contributing in the forming operation. The simplified model express as:

$$V_f = \alpha + \beta ln(\frac{A}{a^2}) \tag{5.1}$$

where

$$\alpha = (\frac{a}{k}) ln(-ln(1-P_f)) + (\frac{t}{k}) ln(\frac{1}{r_0}) \tag{5.2}$$

$$\beta = -\frac{a}{k} \tag{5.3}$$

α and β are reflecting the geometry and physical characteristics of the oxide layer. (A) is the device active area, (a) is the segment (cubic) dimension, (k) is Boltzmann constant, (P_f) is the forming probability, (t) is the oxide thickness, and (r_0) is the transition rate ($r=r_0 e^{\frac{kV_f}{t}}$) constant. The evaluated R^2 in each plot is the determination coefficient of the fitting line (in blue) and the colored zone explains the 95% confidence interval of this model. The forming voltage of CGO and YSZ show stronger dependency to via size compared to the HfO_2. However, the lower forming voltage of CGO compared to well-established oxide material, i.e. HfO_2 switching layer determine the great potential of CGO film for the RERAM switching layer.

Overall, CGO thin films are showing very interesting switching characteristics that can lead to low-power and fast-switching behavior. However, in order to confirm the potential one has to avoid the impact of geometry arise from the top electrode sizes due to shadow mask technique. In addition, the functionality of memory should be analyzed by adjusting the pulse parameters input to achieve a better switching endurance along with the retainable, stable and controllable resistance states. Hence, we have moved towards photolithography methods using lift-off process to address the geometry issue and studied the pulse programing impact. The results are presented in the next section in format of paper manuscript.

5.4 Improved performance and multi-level control of conductive filament in CGO-based ReRAM by the impact of Al interlayer

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Manuscript state: In preparation

Authors contribution: ES and MH conceived the research, developed the fabrication process, participated in the electrical and material characterization, data analysis and wrote the manuscript. MR contributed in the device fabrication and electrical measurements. YL and PM supervised the research and revised the manuscript.

Improved performance and multi-level control of conductive filament in CGO-based ReRAM by the impact of Al interlayer

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Abstract

The further performance improvements of resistive random access memory (ReRAM) relies on the development of design concept, switching mechanism understanding and novel material processing. In this paper, we have systematically studied the resistance switching of $Ce_{0.8}Gd_{0.2}O_{2-x}$ (CGO), classically known as fast ion conductor, containing the maximum number of "mobile" oxygen vacancies. The CGO-based ReRAM exhibited an improved DC performances in comparison to the previous reported results operating with the voltage of -2/1.3 V and the compliance current of 150 μA. Furthermore, the impact of Al interlayer on the pulse performance has been observed. Al modulates the the oxygen vacancies configuration resulting in significant enhancement in the pulse performance reliability and stability. High endurance of 10^5 at the pulse width of 100 μs is achieved. We have tunned precisely the device resistance states through the pule transient operation and variation of Reset voltage amplitude. Our finding leads to the better understanding of the filament dynamic and related switching mechanism of CGO-based ReRAMs suitable for the brain-inspired computing application. To the best of our knowledge, the reported electrical performance is the best achieved switching parameter of CGO-based ReRAMs.

Introduction

Resistive random access memory (ReRAM) has intensively studied as one of the most promising emerging non-volatile memory. High speed, low operating voltage, long retention, ease of fabrication, and scalability aroused ReRAM among the memory technologies [176]. ReRAM is basically a simple capacitor-like structure in which an insulating (semiconductor) thin film is sandwiched between two electrodes. The operation mechanism is based on device resistance switching between at least two distinguishable states (HRS: high resistance state and LRS: Low resistance state). The switching mechanism of metal-oxide material is mainly due to the formation and rupture of conductive nano filament/s (CNF) made of oxygen vacancies categorized as valance change memories (VCM). In bipolar VCM-type ReRAM, the switching from HRS to LRS (Set) and the reverse operation from LRS to HRS (Reset) are happening in the opposite voltage polarity.

Among the long list of materials that has been studied [15], Ta_2O_5, HfO_2, Al_2O_3 and TiO_2 are the most popular ones. TaO_x is showing ultra-high resistance ratio, fast operation speed in range of sub-nano seconds as well as high endurance (>10^{12} cycles) [154, 177]. HfO_x [107] has also fast operation speed and high endurance. One can also add nickel oxide [28], tungsten oxide [54] and copper oxide [178], where the last two ones are the highly compatible with CMOS back end of line (BEoL) process [40]. Surprisingly classically known fast ion conductors, i.e. $Ce_{0.8}Gd_{0.2}O_{2-x}$ (CGO) and $Y_{0.08}Zr_{0.92}O_{2-x}$ (YSZ), used as an electrolyte in Solid Oxide Fuel Cells (SOFCs) [179] have been disregarded compared to the other studied materials. Cerium oxide, CeO_2, is a well-established mixed ionic-electronic conductor that potentially can exhibit fast resistive switching. In fact, the coexistence and reversible valance state transition of Ce^{4+} and Ce^{3+} can lead to rapid creation and annihilation of oxygen vacancies which is very critical for resistive switching [68]. Different concepts have been studied including using an interlayer, i.e. Si [65], Ti [79] and Al [78], UV treatments as well as CeO_2 nano-cubes [68]. Younis et al [68] with using of CeO_2 nano-cubes reported great resistance window (10^4), however at relatively high current compliance (I_{cc}) of 60 mA. With introducing Al interlayer, Ismail and co-workers [78] had improved the cell performance by lowering the I_{cc} to 10 mA, although, the resistance window decreased to 10^2. The high forming power (P=VI) can be due to the limited number of oxygen vacancies that can be enhanced by using doped structures. Recently, Younis et al [171] have studied the filamentary switching in 10% Gd doped ceria, where it has been shown that the switching performance can be manipulated by means of UV radiation. By application of UV light due to the high concentration of oxygen vacancies one can form multi-filament in CGO thin films and consequently obtain multi-step switching. The HRS/LRS ratio was enhanced by factor of 100 under radiation of UV light. The set voltage was reduced from 2.56 V to 2.2 V. In Reset process two resistance steps have been obtained. 10^4 consecutive cycles have been made and three resistance states were clearly separable. This finding confirms the potential of Gd doped ceria thin films to be studied for memory devices however, I_{cc} is still as high as 10 mA. The common feature among different studies of CeO_x-based ReRAMs is the high forming energy i.e. high formation voltage or high operating I_{cc}. The impact of I_{cc} is very likely due to the thermally-assisted switching process that facilitates the ion migration due to the Joule heating.

In the present work, we have systematically studied the resistance switching in CGO thin film at different thickness and with an insertion of Al scavenging layer. We employed 20 % of Gd dopant content which has been found as the optimum Gd dopant concentration in CGO film showing the highest oxygen ionic mobility [4, 180]. Although the CGO-based ReRAMs exhibited the enhanced DC switching performances with the operating voltage of (-2 to 1.3 V) and the I_{cc} of 150 μA, the memory performances were deteriorated in the pulse mode. High switching stability with low energy consumption require sufficient number of vacancies that are free to be set into proper configuration in order to form/break the filament path. The insertion of an Al interlayer which can act as both oxygen reservoir and oxygen barrier layer can modulate the filament configuration as well as vacancies mobility leading to the more efficient exchange of oxygen and pulse switching performance improvement. As expected, significant enhancement in performance and reliability, including operating voltage of (-2 to 1 V) at I_{cc} of 150 μA and high endurance 10^5 with the 100 μs pulse width have been achieved. Additionally, by tunning of the input pulse parameters, distinct resistance levels are obtainable. Moreover, the HRS modulation through the pule transient operation and variation of Reset voltage amplitude provide a better understanding on the filament dynamic and related switching mechanism of CGO-based ReRAMs.

Experimental

Device fabrication

The fabrication process starts with a thermal growth of 500 nm SiO_x on standard 4" Si wafer. Then, a Ti/Pt (5/125 nm) BE was sputter deposited using Pfeiffer Spider 600 cluster systems. The BE is patterned using standard photolithography and deep reactive ion etching (DRIE) process by STS Multiplex ICP. Afterwards, a 100 nm thick low thermal oxide (LTO) was grown by LPCVD at 425°C to be served as a passivation layer. Subsequently, via structure with dimensions of 1, 2, 3, 5 and 10 μm are patterned by photo-lithographic processes and BHF wet etching to define ReRAM active area. The CGO switching layer with approximate thicknesses of 14, 18 and 20 nm is deposited at room temperature, in Nordiko 2000 magnetron sputtering from $Ce_{0.8}Gd_{0.2}O_{1.9}$ target by optimized parameters of 10 sccm Ar plasma at 15 mTorr and RF power of 200 W. For the deposition of Al buffer layer, a 3 nm is sputtered at room temperature with 300 sccm Ar gas at 5×10^{-3} mbar and 400 W plasma with 1% Si impurity. Finally, a 56 nm TiN TE film is sputtered by an Alliance-Concept DP 650 with 300 sccm Ar gas at 5×10^{-3} mbar and the RF power of 200 W. The TE patterning has been done by means of optimized lift-off process with gentle undercut profile. The schematic structure of the CGO-based ReRAM with Pt bottom electrode and TiN top electrode is depicted in Figure 5.14(a). The details of the process flow and lift-off parameters are available in SI 1.

Structural characterization

Chemical composition and device micrograph were obtained using a Zeiss Merlin scanning electron microscope (SEM) operating at 2-3 kV. The CGO film microstructure and chemical mapping were investigated in cross-sectional sample using FEI Tecnai Osiris transmission electron microscopy (TEM) at 200 kV. A chemical mapping by Energy dispersive X-ray spectroscopy (EDX) measurement was carried out. Figure 5.14(b-c) is the cross sectional HRTEM-EDX micrographs of the CGO switching layer at both TiN and Pt interfaces showing 14 m thickness with a uniform distribution of elements through the device structure. CGO shows a polycrystalline structure which in fact can improve the switching performance uniformity [181]. The grain boundaries of crystalline structure act as the seed points to create uniform distribution of conductive paths across the switching layer.

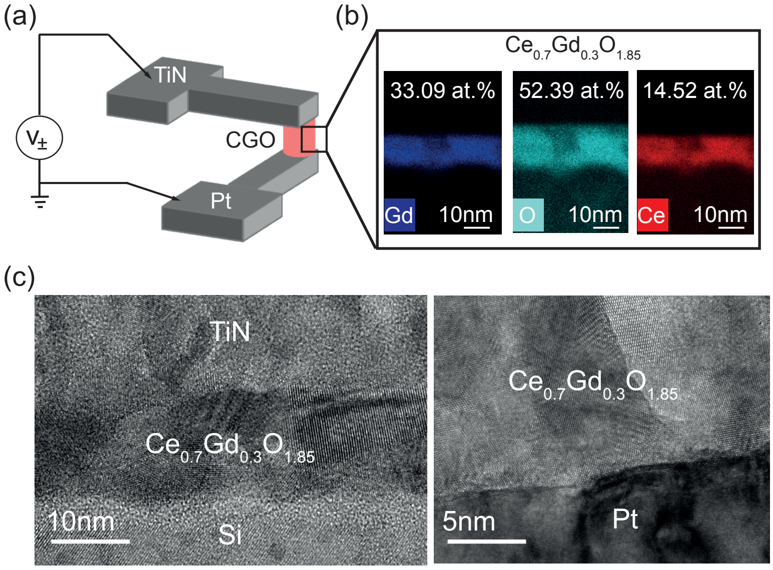

Figure 5.14 – (a) Schematic structure for CGO-based ReRAM cell with Pt bottom electrode and TiN top electrode (b) HRTEM-EDX maps of the CGO switching layer showing 33.09 at.% of Gd, 52.39 at.% of O and 14.52 at.% of Ce which results in $Ce_{0.7}Gd_{0.3}O_{1.85}$. The EDX results for the atomic fraction content of Gd, O and Ce are detected from small area along the film thickness and does not report the total Gd dopant density of the film. (c) Cross-sectional HAADF-TEM micrograph of the 14 nm CGO film used for the ReRAM switching layer.

Electrical Characterization.

The device electrical characterization is performed through a two-point contact using an Agilent B1500 parameter analyzer with grounded BE and biased TE. Two different setups are used for voltage ramp measurements (DC) and pulse measurements. The device forming is conducted using the voltage ramps from 0 to 6 V with the I_{cc} of 150 μA. In DC mode, the voltage is swept from 0 V → -2 V → 0 V → 2 V → 0 V and the Set current (I_{cc}:150 μA) is limited by the parameter analyser. The retention tests were carried out at room temperature, reading the resistance every 2 min. For the pulse measurements, a series external transistor is employed for the current limiting during Set operations. The pulse endurance measurements were carried out using the pulse width of 100 μs and Pulse slope of 20 %. The details of other test's parameters are specified in the corresponding section.

Results and discussion

CGO-based ReRAMs

Figure 5.15(a) demonstrates DC IV characteristics of (Pt/CGO/TiN) ReRAM cells with varying the CGO thickness between 14 to 20 nm. The cells are showing the bipolar resistive switching characteristics with the positive Set and negative Reset operation. All the devices were initially at the high resistance state and a forming operation was applied to trigger the LRS by creation of conductive nano filaments. A reduction of forming voltage ($V_{forming}$) from 4.6 V to 3.6 V is observed by reducing CGO thickness. In the positive Set region, all the stacks switch from HRS to LRS with an abrupt current jump, whereas in the negative voltage region, the cells switch from LRS to HRS with an entire gradual Reset operation and no steep Reset behavior have been observed up to -2 V. Figure 5.15(b) compares the cycle-to-cycle resistance distribution of HRS and LRS for all the stacks over 100 continuous cycling. The resistance states are stable and the obtained resistance ratio (HRS/LRS) of > 50 are sufficient for an efficient memory functionality [182]. It is notable that there is slight reduction in LRS with increasing CGO thicknesses. The increased $V_{forming}$ (V_{Set}) at higher CGO thickness leads to the stochastic creation of $V_{\ddot{O}}$ and consequently lowers the LRS [174] and switching stability. Regarding the operational voltages variability, the relative frequency with the mean value (μ) and normal standard deviation (σ) of V_{Set} and V_{Reset} are evaluated over 100 cycles per each stack (Figure 5.15(c-d)). CGO 14 nm shows the better switching voltage uniformity with the smaller dispersion of V_{Set} (1 to 1.25 V) and V_{Reset} (-0.5 to -0.75 V) compared to CGO 18 nm and 20 nm with the wider variation in V_{Set} (1 to 1.75 V) and V_{Reset} (-0.5 to -1 V). Moreover, the magnitude of V_{Set} is reducing with the thickness scaling as the calculated mean values (μ) are 1.25 V, 1.19 V and 1.09 V for CGO 20 nm, CGO 18 nm and CGO 16 nm, respectively. The dependency of V_{Set} to the active layer thickness implies the field-induced properties of Set phenomenon in CGO which has been previously observed in the CeO_x-based ReRAMs [71], While, the V_{Reset} does not show any remarkable changes with respect to the film thickness meaning that the cells consume the same power for the rupture of CNF.

HRS and LRS data retentions of (Pt/CGO (20 nm)/TiN) device for 10 hours at room temperature is presented in Figure 5.16(a) proving the non-volatility and stability of the memory resistance levels. The pulse endurance characteristics of (Pt/CGO (20 nm)/TiN) over 10^4 is shown in Figure 5.16(b) using V_{Set}/V_{Reset} of -2 V/1.8 V. LRS is increasing with repetitive switching cycles while HRS is more stable. LRS exhibits three regimes during endurance measurements. The increase of LRS from 4.5 kΩ to 20 kΩ indicates the incomplete Set operation in the pulse mode. The similar unstable characteristics have been observed for the pulse endurance measurements of (Pt/CGO (18 nm)/TiN) and (Pt/CGO (20 nm)/TiN) (not shown here). Unlike DC mode operation, by applying the short pulse width, the CGO film does not receive sufficient energy to form thermodynamically stable filaments which results in the increase of LRS. Increasing set voltage/current amplitude or pulse width can result in more stable response,

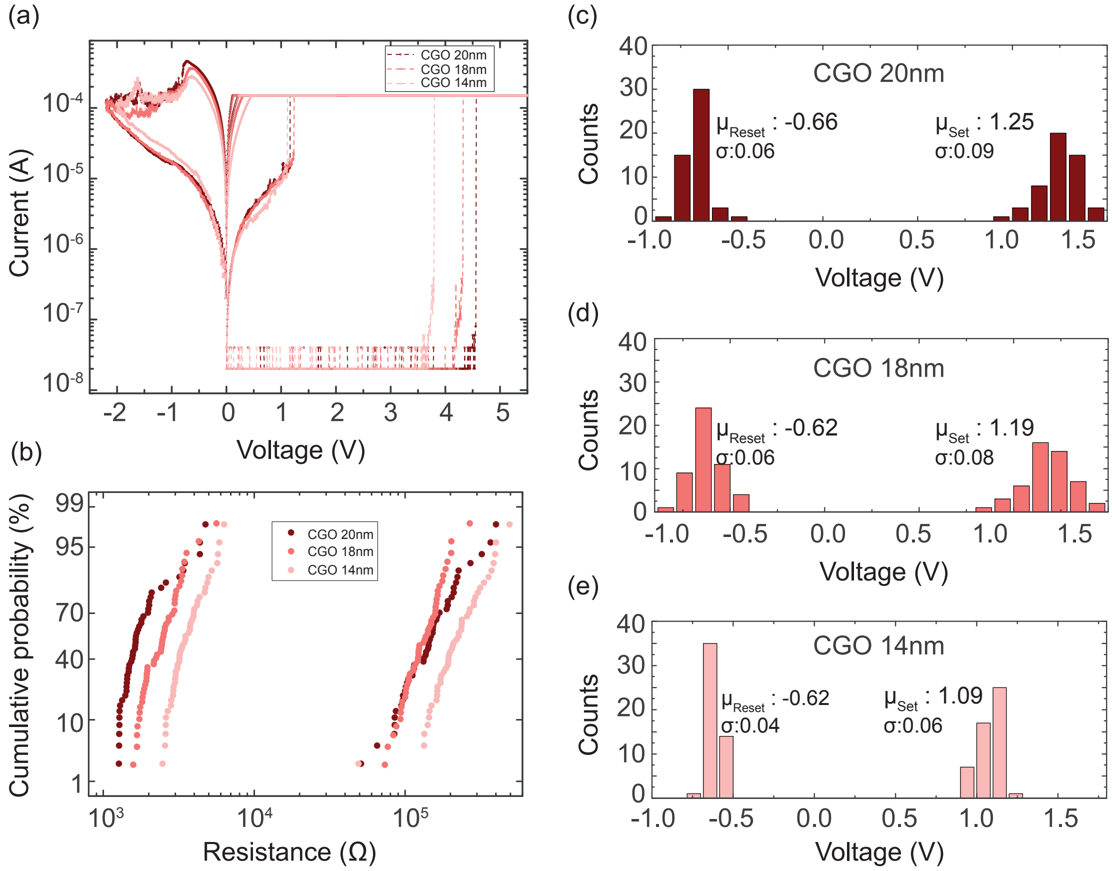

Figure 5.15 – (a) DC bipolar IV switching characteristics obtained from (Pt/CGO (20 nm)/TiN), (Pt/CGO (18 nm)/TiN) and (Pt/CGO (14 nm)/TiN). (b) Cumulative distribution of HRS and LRS over 100 cycle for CGO 20 nm, CGO 18 nm and CGO 14 nm ReRAM cells measured at V_{read} = 0.25 V. The histogram V_{Set}/ V_{Reset} distribution of 100 cycles for (c) CGO 20 nm , (d) CGO 18 nm and (e) CGO 14 nm.

however it is not suitable for the memory application due to the high power consumption. A proper choice of electrode material can modulate the vacancies configuration creating thermodynamically stable CNF which improves device endurance and stability particularly at the pulse operation. Among different active metals that have been previously studied for the CeO_x-based ReRAM [79, 183, 184], Al is one of the best candidates due to its lower work function (4.28 eV) in comparison to ceria (4.69 eV) and Pt BE (5.69 ev) and easy oxidizing properties -quantified by its ΔG value of -1582.3 kJ/mol [47]- that facilitate the charge carrier transfer during switching. Thus, a 3 nm Al is added at CGO/TiN interface; without the vacuum break in the (Pt/CGO (14 nm)/TiN) device. The effect of Al incorporation on both DC and pulse switching characteristics have been studied extensively.

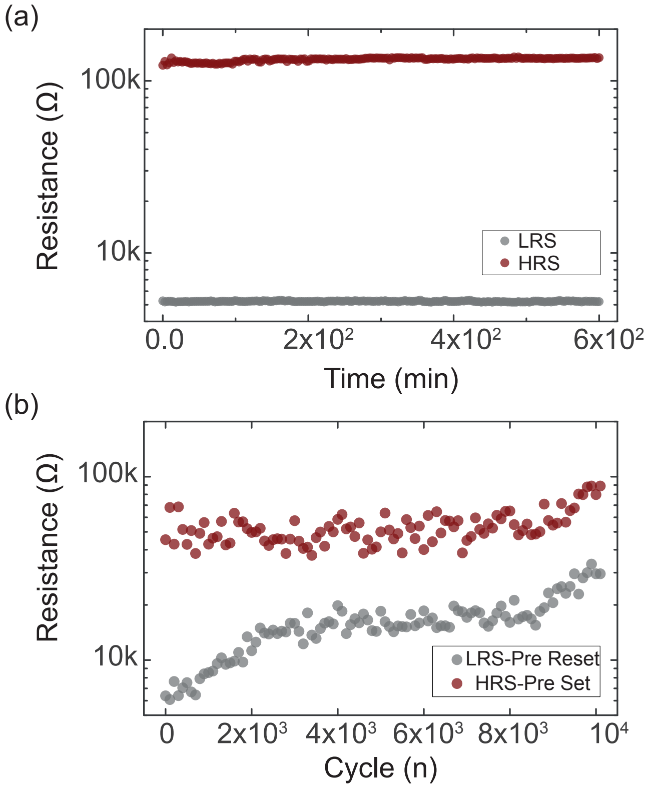

Figure 5.16 – (a) HRS and LRS data retention at room temperature obtained from (Pt/CGO (20 nm)/TiN), reading performed every 2 min and (b) 10^4 pulse endurance of (Pt/CGO (20 nm)/TiN) device (V_{Set}/V_{Reset} = -2 V/ 1.8 V, I_{cc}= 150 μA, Pulse width = 100 μs and Pulse slope = 20 %).

Impact of Al interlayer

Figure 5.17 shows the forming operation of (Pt/CGO (14 nm)/Al (3 nm)/TiN) with the device diameter varying between 1 to 10 μm. All the devices are showing high initial resistance states. It can be observed that with increasing the area, the device are prone to show more gradual current rising before an abrupt forming occurs. In the forming transition regime, the leakage current is increased by a factor of 20 from 1 to 10μm via size. The same trend was not observed in (Pt/CGO (14 nm)/TiN) (Figure 5.15) highlighting the effect of Al inter layer. Figure 5.17(b) represents the statistical analysis of forming voltage dependency with respect to the device dimension obtained from 5 devices per each via diameter. The forming voltage is increasing from 3.2 to 4.8 V by scaling via diameter from 10 to 1μm. Reducing the area lowers the number of potential sites to trigger the filament formation, defect population effect [167]. The positive forming voltage attracts oxygen ions towards Al interlayer, creating a thin AlO_x at CGO/Al interface. AlO_x provides asymmetric Schottky barrier potential at CGO/Al interface as shown schematically in Figure 5.17(d). In order to verify the Schottky emission in the forming current transition regime, the IV behavior of devices with different dimension are plotted in $Ln(I)$-

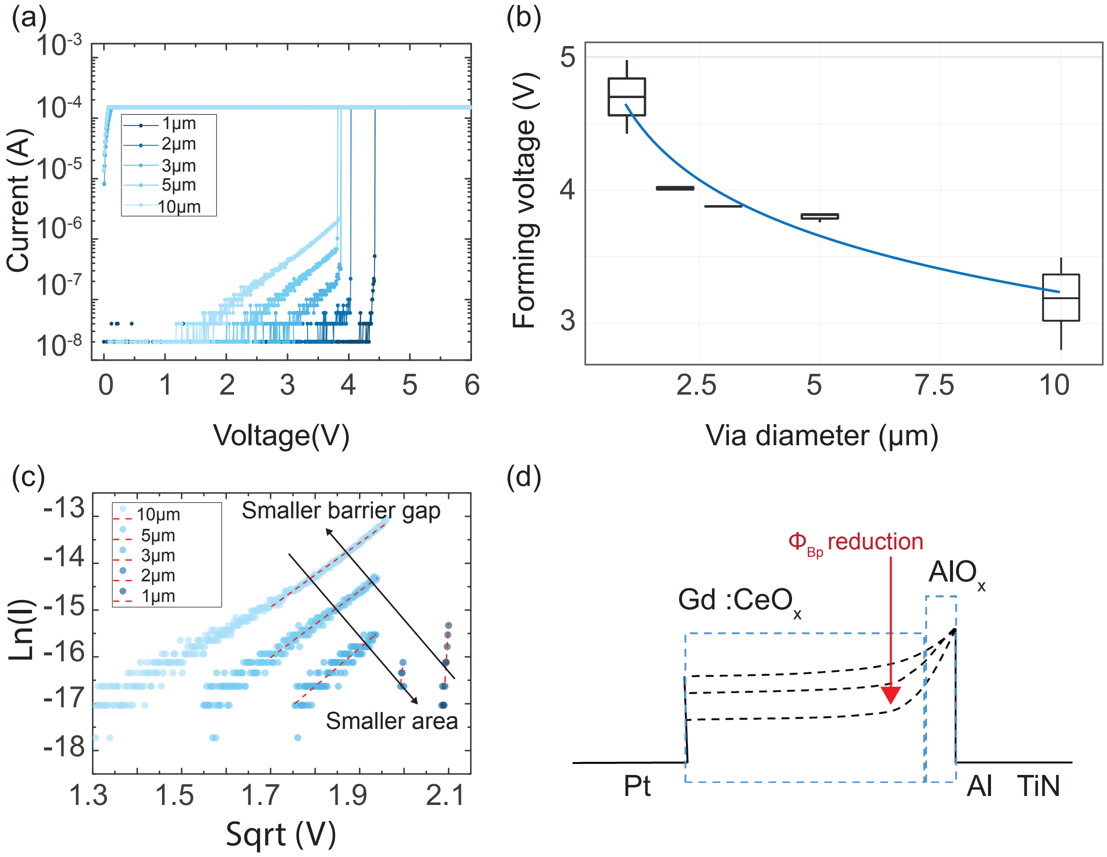

Figure 5.17 – (a) Forming IV characteristics of (Pt/CGO (14 nm)/Al (3 nm)/TiN) devices with different via diameters between 1 μm to 10 μm. (b) Device dimension dependence of forming voltage for (Pt/CGO (14 nm)/Al (3 nm)/TiN). (c) I-V curves fitted by Schottky law ($Ln(I) - \sqrt{V}$) for the forming transition region in different device dimension (1-10 μm). (d) Schematic of energy band diagram for different via diameter of (Pt/CGO (14 nm)/Al (3 nm)/TiN).

$\sqrt{V}$ (Figure 5.17(c)). The linearity in the behavior of $Ln(I)$- $\sqrt{V}$ governs Schottky transport in accordance with Richardson-Schottky law [34]:

$$J_{SD} = A^* T^2 \, exp\left[\frac{-q(\Phi_B - \sqrt{qE \setminus 4\pi\epsilon})}{kT}\right] \tag{5.4}$$

where A^* is the Richardson's constant, k is the Boltzmann constant, T is the device temperature during the operation and ϕ_B is the barrier height. The Schottky ϕ_B is extracted from an intercept of $Ln(J/A^*T^2)$- $\sqrt{V}$ plot as:

$$\phi_B = \frac{-kT}{q} \times intercept \tag{5.5}$$

The devices with the via diameters of 10, 5 and 3μm are showing the AlO$_x$ barrier potential of 1.9 eV, 2 eV and 2.16 eV, respectively. However, in <3μm devices, the forming is not any more governed by the Schottky emission due to the less number of defects at the interface [185].

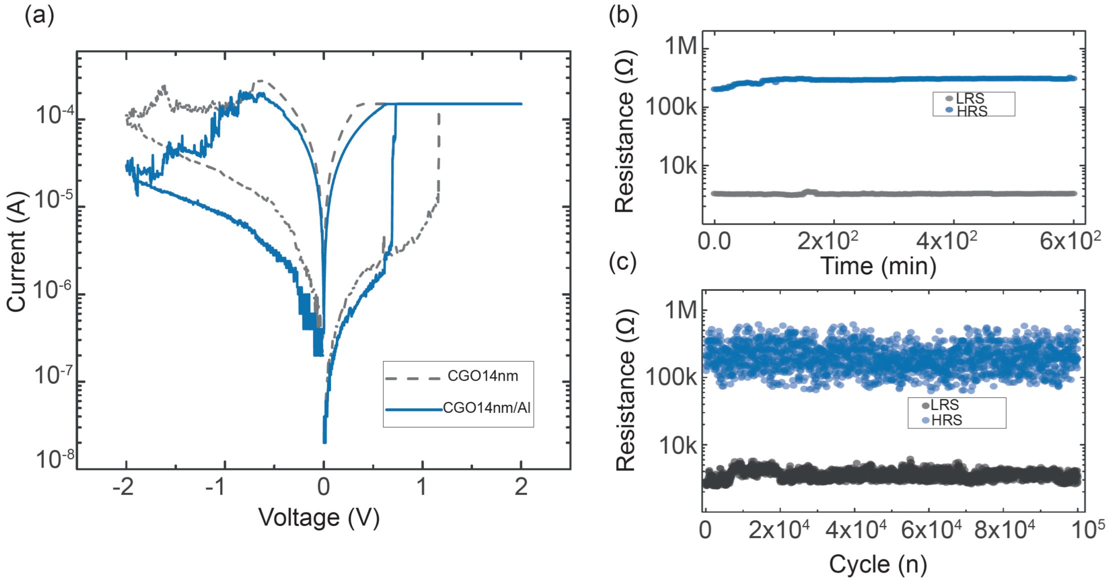

Figure 5.18 – (a) DC bipolar IV switching characteristics obtained from (Pt/CGO (14 nm)/ Al (3 nm)/TiN). (b) HRS and LRS data retention at room temperature obtained from (Pt/CGO (14 nm)/ Al (3 nm)/TiN), reading performed every 2 min and (c) 10^5 pulse endurance of (Pt/CGO (14 nm)/ Al (3 nm)/TiN) ReRAM (V_{Set}/V_{Reset} = -2 V/ 1.8 V, I_{cc}= 150 μA, Pulse width = 100 μs and Pulse slope = 20 %).

Figure 5.18(a) shows the bipolar resistive switching I-V curve for the (Pt/CGO (14 nm)/ Al (3 nm)/TiN) cell. In the positive Set part, the memory switches to the LRS at 0.8 V and in the negative Reset region, the cell switches back to HRS at -0.8 V and the current is decreasing till -2 V. Unlike (Pt/CGO (14 nm) /TiN) (Figure 5.18(a)-gray line), the cell shows multi-level Reset behavior. To further evaluate the stability of resistive switching in (Pt/CGO (14 nm)/ Al (3 nm)/TiN), retention and pulse endurance measurements have been conducted. Figure 5.18(b) displays HRS and LRS data retentions for 10 hours at room temperature in which both LRS and HRS are showing stable levels. Figure 5.18(c) demonstrates pulse endurance characteristics of the device for 10^5 cycling under application of V_{Set}/V_{Reset} of -2 V/1.8 V. The HRS and LRS are varied between 100-500 kΩ and 2-3 kΩ, respectively. Nevertheless, a clear resistance ratio (HRS/LRS) of about 10^3 is still achievable without any resistances degradation. Enhanced pulse switching stability in (Pt/CGO (14 nm)/ Al (3 nm)/TiN) cell is attributed to the role of Al layer which acts as both oxygen diffusion barrier and oxygen reservoir layer.

The CGO-based ReRAM with inert electrodes, i.e. TiN and Pt, is prone to show multi-filaments switching behavior due to the high concentration and random distributions of mobile intrinsic defects [4]. CGO grows with polycrystalline structure (see Figure 5.14(c)) with high density of grain boundaries facilitating multi-filament formation [186]. The evidence of such conduction mechanism is observed in the endurance measurement of (Pt/CGO (20 nm)/TiN) cell (see Figure 5.16(b)). At the beginning, multiple filaments are contributing in the resistive switching, in which only few filaments can sustain over pulse cycling and an increase is observed in the LRS. The insertion of Al with high oxygen affinity determines an increase of the vacancy concentration in CGO close to the Al layer, which initiates the filament formation. At the CGO/Al interface, a thin AlO_x layer is formed. Therefore, it is expected the formation of a conic-shape filament with a vacancy concentration gradient from the CGO/Al interface to the Pt/CGO one. The confined filament geometry leads to uniform switching characteristics and more stable pulse performances (see Figure 5.18(c)).

Switching dynamic modulation through pulse programming

The device switching dynamic is investigated under both pulse transient operation and Reset voltage amplitude variations. The HRS is modulated using both pulse width and amplitude showing the multi-level capability of CGO-based ReRAMs. An overview of the pulse time effect on the resistance states of (Pt/CGO (14 nm)/ Al (3 nm)/TiN) is presented in Figure 5.19. The voltage stimuli with pulse width of 5 to 1000 μs and slopes of 10 % to 40 % are applied in the consecutive endurance measurements. The pulse width was changed every 55 cycles whereas the slope was varied every 330 cycles with the fixed Reset/Set pulse of -2 V/1.8 V.

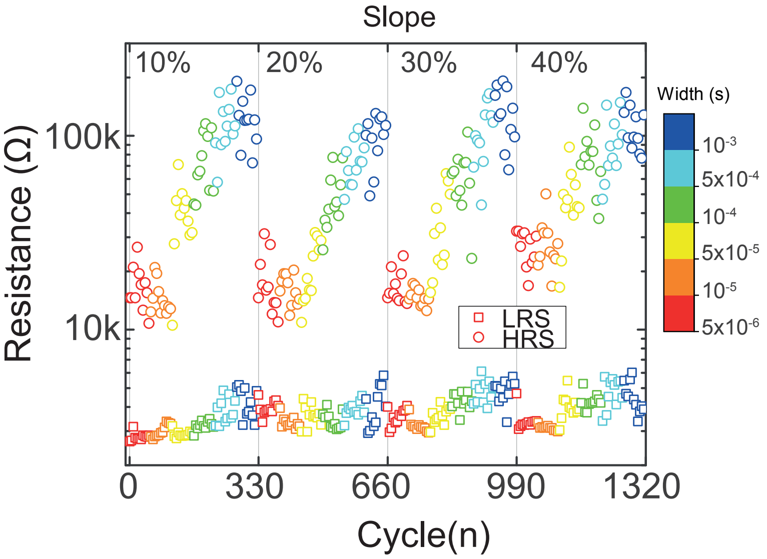

Figure 5.19 – An overview of the slope and pulse width variation influence on the (Pt/CGO (14 nm)/ Al (3 nm)/TiN) memory resistance states with -2 V Reset pulse, 1.8 Set pulse and I_{cc}= 150 μA. The slope value varies every 330 cycles from 10% to 40%, while the pulse width changes every 55 cycles from 5μs to 1 ms. Reading is performed every 5 cycles.

To obtain a better insight on underlying Set and Reset switching kinetics, HRS and LRS are analyzed separately. Figure 5.20 shows the mean value and standard deviation calculation of HRS and LRS as a function of Rise time (t_r). Rise time is introduced as an assessment factor which includes the impact of both pulse width (W_p) and pulse slope (S_p) as $t_r = W_p \times S_p$. HRS is increasing from 10 to 120 kΩ by increasing the rise time showing distinct resistance states. It is notable that HRS reaches a saturation after a rise time threshold (Figure 5.20 (a)). Giving enough energy with increasing the rise time associates with the rupture of higher number of filaments which results in deeper HRS. The same HRS trends with respect to the rise time has been observed in the CGO-base ReRAM without Al layer (SI 2). However, the difference lies in the LRS behavior. The creation of AlO_x barrier layer lowers the effect of Joule heating and consequently prevents the LRS degradation towards higher values (Figure 5.20(b)).

The resistance modulation with the Reset pulse amplitude is studied at the fixed pulse width of 100 μs and 5 μs (SI 3). Figure 5.21 shows the HRS distribution of (Pt/CGO (14 nm)/ Al (3 nm)/TiN) device as a function of applied Reset pulse amplitude. For 100 μs pulse width, the HRS decreases from 1 MΩ to 10 kΩ in the voltage range of -2.2 V to -1.4 V (step:0.05) and for the 5 μs pulse width, the HRS reduces from 1 MΩ to 3 kΩ with the smaller voltage range of -2.2 V to -1.6 V (step:0.1). The resistance exhibits stronger dependency at higher Reset pulse amplitude defining two distinct regimes in log(R)-Reset pulse plot. It is widely accepted that Reset is due to the rupture of conductive filament through the field-driven and Joule-heating ion

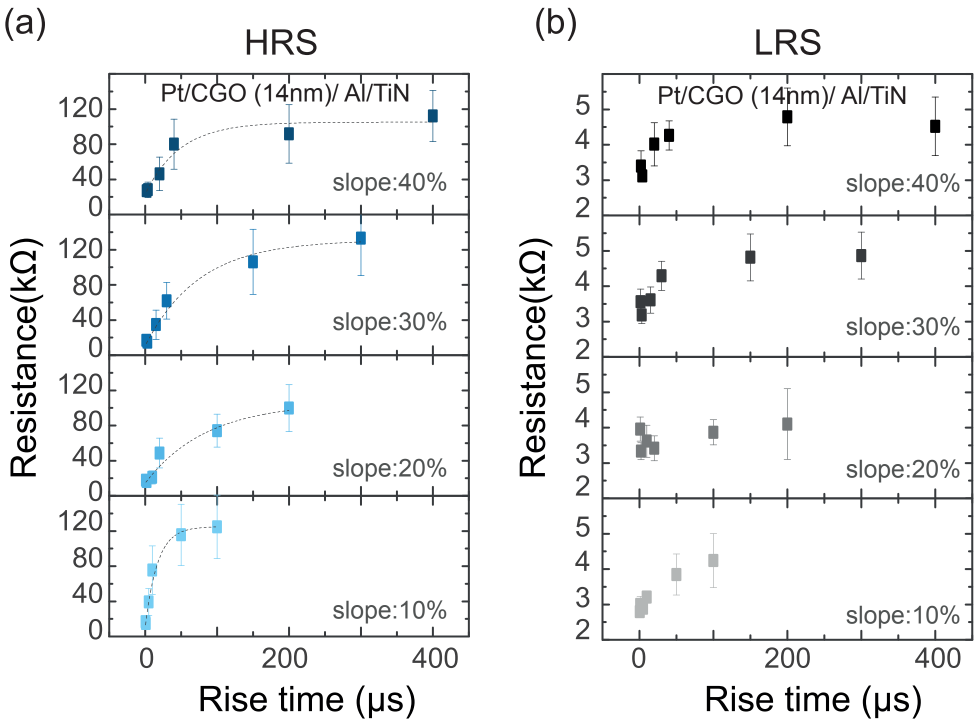

Figure 5.20 – Statistical analysis on the effect of rise time for (a) HRS and (b) LRS obtained from 50 consecutive cycles of each pulse widths and slopes; V_{Set} is fixed at 1.8 V, V_{Reset} at -2 V and I_{cc} at 150 μA.

migration [113, 187] . The effect of Joule heating is lowered by decreasing the voltage amplitude where the ion migration is mainly field driven phenomena and lower HRS is achieved [188]. Moreover, at smaller pulse width, the resistance reduction rate with lowering pulse voltage is higher. The lower HRS values with the shorter pulse duration is in fact consistent with HRS modulation with rise time, presented earlier.

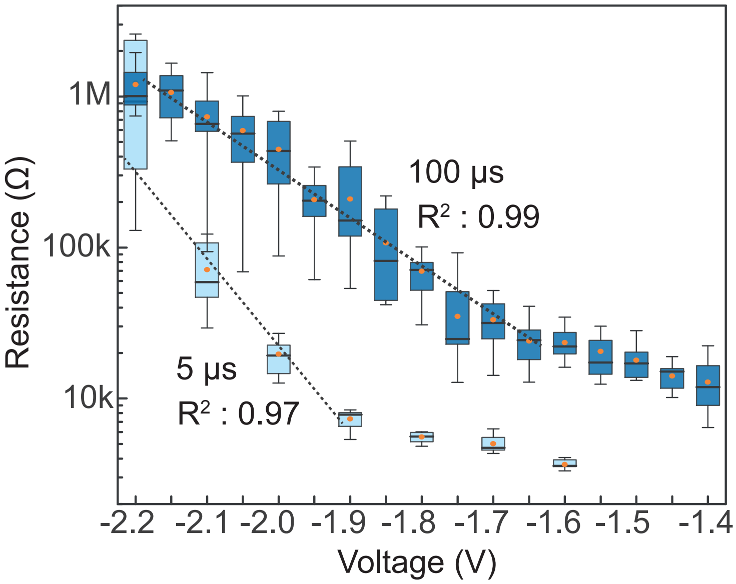

Figure 5.21 – Distribution of (Pt/CGO (14 nm)/ Al (3 nm)/TiN) device high resistance states as a function of Reset pulse amplitude at two pulse durations of 100 μs and 5 μs. V_{Set} is fixed at 1.8 V, V_{Reset} at -2 V and I_{cc} at 150 μA. The results are obtained from 50 cycles for each measurement

Conclusion

We have reported an improved performance and multi-level control of conductive filaments in CGO-based ReRAM by the impact of Al scavenging layer. The CGO-based ReRAMs exhibited the enhanced DC switching performances with the operating voltage sweep of -2 to 1.3 V and the I_{cc} of 150 μA. However, the memory performance was deteriorated in pulse operation mode. We achieved an excellent resistive switching by insertion of an Al inter layer. The Al interlayer can act as both oxygen reservoir and oxygen barrier layer modulating the filament configuration as well as vacancies mobility. This leads into the lower power consumption and more reliable pulse switching performance. (Pt/CGO (14 nm) /Al (3 nm) /TiN) switched with the operating voltage of -2/1 V at I_{cc} of 150 μA, HRS/LRS ratio of 40 and high endurance of 10^5 at the pulse width of 100 μs. Furthermore, the memory resistance states were precisely tunned through pulse transient operation and Reset voltage variation showing distinct resistance states suitable for the brain-inspiring computing application.

Acknowledgment

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Supplementary Information

Improved performance and multi-level control of conductive filament in CGO-based ReRAM by the impact of Al interlayer

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Process flow

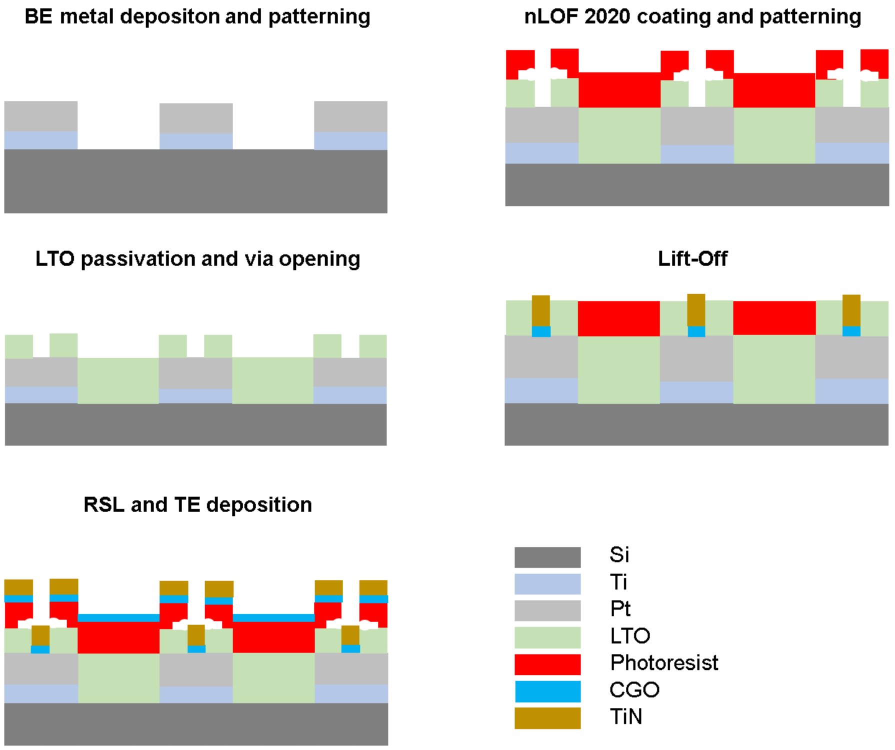
BE metal depositon and patterning
nLOF 2020 coating and patterning
LTO passivation and via opening
Lift-Off
RSL and TE deposition
Si
Ti
Pt
LTO
Photoresist
CGO
TiN

Figure 5.22 – The schematic details of process flow for the CGO-based ReRAM fabrication through a lift-off process

A lift-off process was developed for the CGO and top electrode (TE) patterning, to avoid the ion bombardment damages caused by dry etching. For the successful lift-off process, having a gentle undercut profile, with especial attention to the sputtering deposition technique, different parameters including nLOF 2020 resist thickness, exposure dose, post exposure bake (PEB) temperature/duration and resist development time have been optimized. An example of the resist-development time effect on the resist undercut profile are shown in Figure 5.23. Figure 5.23(a) represents an excessive undercut profile due to long development time which is not entirely stable over the deposition process. The best lift-off results have been achieved using exposure dose of 60 mj/cm^2 with 60 s PEB at 106 °C with the development duration of 105 s.

Pulse transient operation

The effect of pulse time on the resistance states of (Pt/CGO (20 nm)/TiN) and (Pt/CGO (16 nm)/TiN) is shown in Figure 5.24. The voltage stimuli with different pulse width of 5

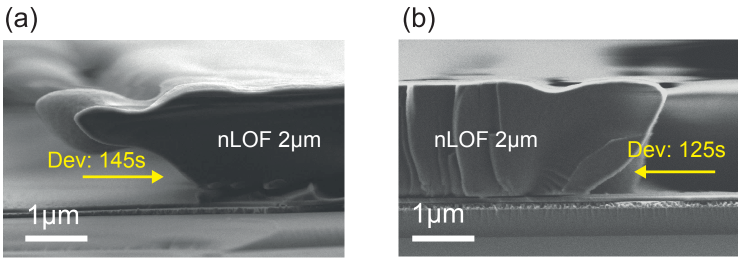

Figure 5.23 – The SEM micrographs of 2 different lift-off process with negative nLOF 2020 resist development time optimization trial. 2 μm resist thickness with 60 s post exposure baking at 106 °C with the exposure dose of 60 mj/cm^2 with different development time of (a) 145 s and (b) 125 s.

to 1000 μs and different pulse slopes of 10 % to 40 % are conducted through consecutive endurance measurements. Width was changed every 55 cycles whereas slope was varied every 330 cycles. LRS and HRS are increasing with respect to the pulse width. As it is expected from the pulse endurance measurement, Pt/CGO/TiN ReRAM does not show stable switching characteristics since LRS is deteriorated towards HRS through the cycling. The LRS degradation is more significant at smaller CGO film thicknesses.

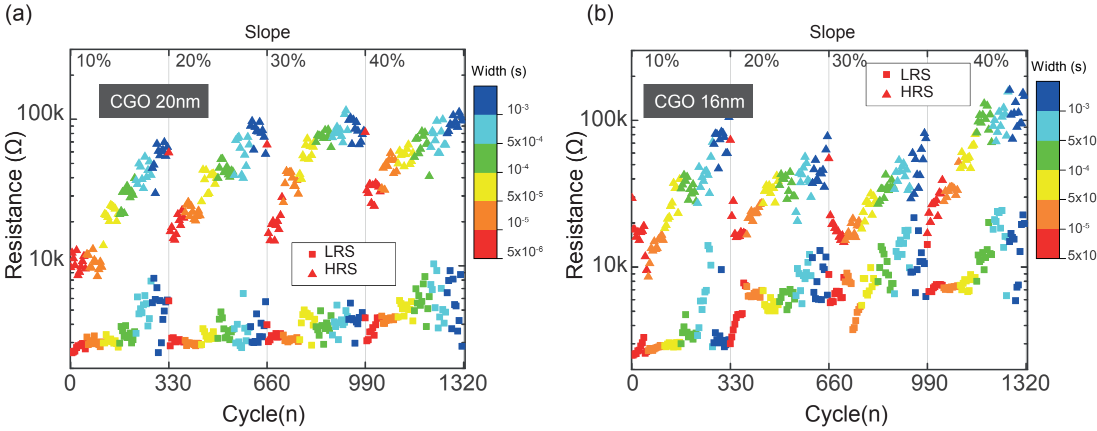

Figure 5.24 – An overview of the slope and pulse width variations influence on the (Pt/CGO (20 nm)/TiN) and (Pt/CGO (16 nm)/TiN) memory resistance states with -2 V Reset pulse, 1.8 Set pulse and I$_{cc}$= 150 μA. The slope value varies every 330 cycles from 10% to 40%, while the pulse width changes every 55 cycles from 5μs to 1 ms. Reading is performed every 5 cycles.

Resistance modulation through Reset pulse programming

The effect of Reset pulse amplitude on the resistance states of the (Pt/CGO (14 nm)/ Al (3 nm)/TiN) at the pulse width of 100 μs and 5 μs are shown in Figure 5.25 showing tunable HRS states while LRS remains stable. The HRS reduction rate with respect to the Reset voltage is faster at pulse width of 5 μs. The effect of Reset pulse voltage has been also evaluated on the (Pt/CGO (20 nm)/TiN) and (Pt/CGO (16 nm)/TiN) in which less stable LRS are observable in both cases.

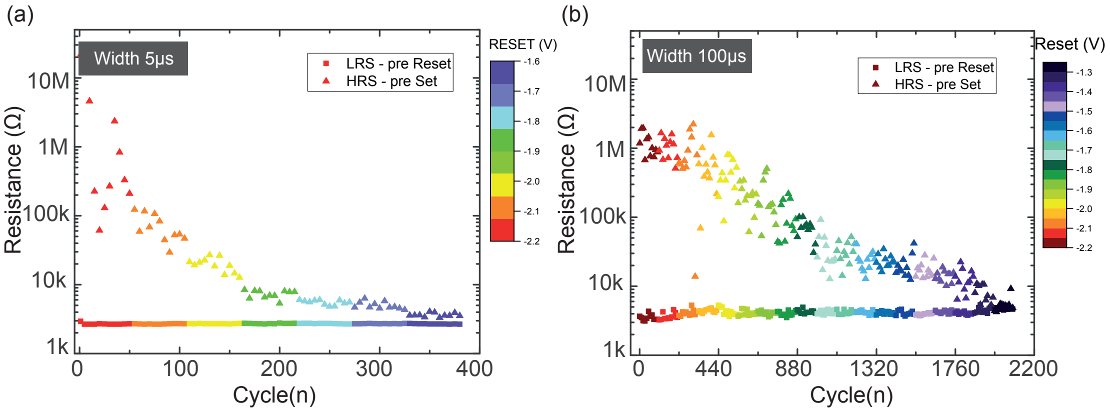

Figure 5.25 – An overview of the resistance variations by RESET pulse amplitude for (Pt/CGO (14 nm)/ Al (3 nm)/ TiN) at the fixed Set pulse of 1.8 V and the pulse width of (a) 5 μs (Reset voltage varies between -2.2 V to -1.6 V (step 0.1)) and (b) 100 μs (Reset voltage varies between -2.2 V to -1.4 V (step 0.0.5)). Consecutive 50 cycles per test parameter and a reading of every 5 cycles.

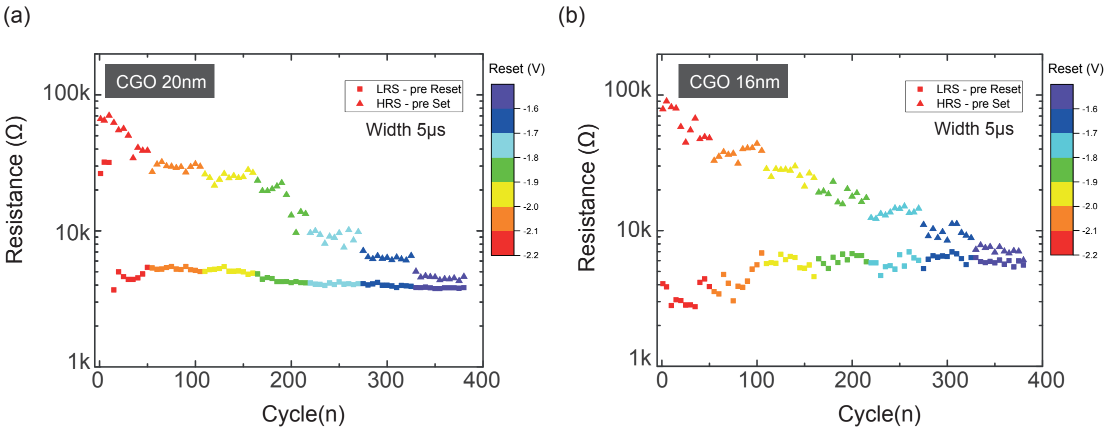

Figure 5.26 – Resistance variations by RESET pulse amplitude for (a) (Pt/CGO (20 nm)/TiN) and (b) (Pt/CGO (16 nm)/TiN). The Reset voltage varies between -2.2 V to -1.6 V (step 0.1) with the fixed Set pulse of 2.0 V. Consecutive 50 cycles per test parameter and a reading of every 5 cycles.

6 Summary and Outlook

6.1 Thesis Summary

The present dissertation provides an examination of the ReRAM, based on transition-metal oxide as a viable alternative for non-volatile multi-level data storage from proper material selection to heterogeneous implementation with conventional CMOS technologies. A scalable, reliable and economically feasible technique for the chip-scale ReRAM-CMOS co-integration were studied from different perspective including the effect of electrode material, understanding of switching mechanism, controlled and persistent resistance variation upon the application of proper electrical stimuli, and optimizing further transition-metal oxides (as a direct replacement for current material in today's ReRAM) to boost the performance of the future memory. Tungsten is a material of choice in numerous BEoL process as a vertical inter-connectors (via) between the adjacent metal layers. Application of W CMOS's via as ReRAM electrode provides the creation of nm-scale memory cells with no need to the intricate and expensive processing techniques such as E-beam lithography and chemical mechanical polishing. Moreover, W is a low-work function metal that with the appropriate material combination facilitates the electronic switching mechanism reducing the power consumption and improve the reliability issue. First, the impact of W electrode on ReRAM performance has been investigated. We have engineered the W electrode interface with an in-depth understanding of W electrochemical properties targeting the better control on ReRAM switching properties. Next, a technique for the hybrid integration of nm-scale W-based ReRAM on the foundry-produced CMOS 180 nm technology chip has been established. Lastly, the yttrium stabilized zirconia (YSZ) and gadolinium doped ceria (CGO) as the classically known fast ion-conductor were optimized to be used as resistive switching layer. The ability of structural defect modification in CGO and YSZ for the better ion conductivity leads to a great control of oxygen vacancies mobility having a profound impact on the control of ReRAM switching performances adding a degree of freedom in the modulation of speed, resistance, retention, and endurance. The highlights of each chapter achievements and further opportunities enabled by this thesis are listed below:

W-based stand-alone ReRAM:

To achieve an insight understanding of W electrode properties and its impact on ReRAM performances, the well-established materials, i.e. HfO_2 and Pt were utilized as the switching layer and inert electrode, respectively. The study has been performed on the stand-alone cross-point memory cells avoiding the complication arise from the material and processing issues. The device fabrication process flow has been thoroughly optimized. W oxidizes readily, having multiple oxidation states, which influences the device reliability. This has been verified in the ($Pt/HfO_2/W$) device performances showing high switching instability and performance degradation in the AC mode. We have modulated the W electrochemical interactions at (HfO_2/W) interface by insertion of Al_2O_3 or Ti interfacial layers. The comprehensive DC/AC comparisons have been performed and remarkable improvements in endurance, power consumption, resistance states stabilization, cycle-to-cycle and device-to-device variability are reported for ($Pt/HfO_2/Al_2O_3/W$) and ($Pt/HfO_2/Ti/W$) devices. The time-dependent switching kinetics is investigated in a transient Set/Reset operation. We have observed that the compact stoichiometric ALD-deposited Al_2O_3 barrier layer completely prevents W oxidation, resulting in a sharp current transient in the Reset operation. While, the use of a sputtered Ti buffer layer allows a partial W oxidation, defining a tunable HRS by pulse rise time control. Moreover, switching kinetics and conductive nano-filament (CNF) evolution are studied in detail to understand the microscopic effect of the interface modifications. The tunability of multi-HRS states by pulse timing control in ($Pt/HfO_2/Ti/W$) is indeed in the interest of network and brain-inspired computing applications, adding a degree of freedom in the modulation of its resistance. Furthermore, the multi-storage capability of ($Pt/HfO_2/Ti/W$) has been also carefully investigated by tunning the resistance states with the Reset pulse voltage. The persistence of the multi-resistance states was verified by a retention test after each Reset pulse programming. The cell Set/Reset switching times were assessed as 100/80 ns.

The results of this chapters confirms that the use of W electrodes has to be accompanied by a intermediate layer Al_2O_3 and Ti. Both are improving the device variability, reducing the power consumption and increasing the resistance window. The use of Ti or Al_2O_3 is indeed depends on the electrodes structure and desired performance. For instance, in case of Pt as an inert electrode with relatively high work function, W/Ti can be used to modulate the state by both time and voltage while W/Al_2O_3 results in sharp resistance switching.

ReRAM-CMOS co-integration:

In this section, detailed nanofabrication process of chip-scale heterogeneous ReRAM-CMOS integration, as well as, a carrier wafer for the delicate chip handling and post-processing were extensively studied. The first approach was based on thermal oxidation of W via proposing a self-align and mask-free formation of WO_x switching layer. Even though the technique allocated self-align, quick and accessible prototype for the formation of switching layer on the existing W via, the surface non-uniformity, imprecise oxide thickness and inconsistent film composition necessitate delicate process optimization to obtain performance reliability and reproducibility. Therefore, in the second phase, we have used highly uniform, stoichiometric, ultra-thin and well-established ALD-deposited HfO_2 as the switching layer. The effect of W chemical interaction is studied in different co-integrated ReRAM stacks by increasing HfO_2 switching layer thickness, post-metalization annealing under O_2-ambient and adding an Al_2O_3 barrier layer. All the co-integrated stacks show self-rectifying behavior with an operating current less than 1 mA. As it was expected, the addition of Al_2O_3 barrier layer improved the HRS/LRS resistance ratio and switching uniformity preventing deterioration of cell electronic properties. The impact of Al_2O_3 barrier in protecting HfO_2 from oxygen leaching was confirmed by TEM micro-structural characterization and chemical analysis. It has been observed that the oxygen content in W bottom electrode remained unchanged after multiple cycling. The switching mechanism is well explained by trap-controlled space charge limited current (SCLC) conduction mechanism. To define the device characteristics that can be applicable for circuit/system level design, the results of the integrated (W/Al_2O_3(3 nm)/HfO_2(5 nm)/TiN) ReRAM were simulated using a SPICE compact model in the MATLAB environment.

Fast ion-conducting thin films for resistive switching:

The high density of mobile oxygen vacancies is believed to have a profound impact on lowering the filament formation energy and device power consumption. Thus, it is substantial to consider the fast ion-conductor film, i.e. CGO and YSZ, as the promising candidates for the switching layer of ReRAM. In this section, first, a systematic evaluation of CGO and YSZ thin film based ReRAM was presented. We have extensively studied the thin film processing conditions impact on the performance of switching layers. The process is optimized in order to achieve the minimum forming energy, stable resistance states as well as operating voltage. Furthermore, the pulse endurance characteristics were carried out to determine the qualified functionality of CGO and YSZ based ReRAMs. Both cells have shown stable response over 10^4 cycles with HRS/LRS ratio of 100 and 5 for CGO and YSZ, respectively. The results provide a better insight into the dynamic of conductive filament evolution in which the multi-filament and single-filament formation are proposed as the control mechanism of CGO and YSZ switching, respectively.

Furthermore, the performance of the CGO film was studied in the confined electrode shape by optimizing a lithography-lift-off process flow to avoid the impact of geometry arises from the large shadow-mask top electrode sizes. The lithography CGO-based ReRAM devices exhibited the enhanced DC switching performances with the operating voltage of (-2 to 1.3 V) at the I_{cc} of 150 μA. However, the memory performance was deteriorated in the pulse mode. The insertion of an Al interlayer modulated the filament configuration as well as vacancies mobility leading to the more efficient exchange of oxygen and consequently to the pulse switching performance improvement. As expected, significant enhancement in performance and reliability, including operating voltage of (-2 to 1 V) at I_{cc} of 150 μA and 10^5 cycles endurance with the 100 μs pulse width have been achieved. Additionally, by tunning of the input pulse parameters, distinct resistance levels are obtainable. The HRS modulation through the pule transient operation and variation of Reset voltage amplitude provide a better understanding of the filament dynamic and related switching mechanism of CGO-based ReRAMs. The summary and comparison performance of the (Pt/CGO (14 nm) /Al (3 nm) /TiN) is listed in Table 6.1.

Table 6.1 – Performance comparison on CGO-based ReRAM. HRS: High Resistance State, LRS: Low Resistance State, "-" : Not Reported

Ref.	Structure	Oxide thickness (nm)	Forming (V)	Set/ Reset(V)	HRS/LRS	I_{set} (A)	Endurance(cycle)	Retention (s)
[171]	Au-$Ce_{(1-x)}Gd_xO_x$-FTO (UV irradiated)	-	-	3/ -3	10^3	10^{-2}	10^4	8×10^4
[81]	Pt-$Ce_{0.9}Gd_{0.1}O_x/Er_2O_3$-Cu	200-600	-	200/ -200	15	10^{-4}	-	-
[4]	Pt-$Ce_{(1-x)}Gd_xO_x$-Pt	500	-	10/ -10	2×10^2	10^{-4}	50	-
Present work	**Pt-$Ce_{1-x}Gd_xO_{1.85}$-Al-TiN**	**14**	**4**	**-2/ 1**	**10^2**	**10^{-4}**	**>10^5**	**>10^3**

6.2 Thesis Outlook

W-based stand-alone ReRAM

Regarding the W-based ReRAM stand-alone optimizations, We have carefully investigated the time-dependent switching in transient Set/Reset operation and different trends have been explained by the W electrode interface properties. However, the HRTEM-EDX material characterization on the cross-sectional of both ($Pt/HfO_2/Al_2O_3/W$) and ($Pt/HfO_2/Ti/W$) devices can better support the expected surface morphology and oxygen profile differences. Moreover, it would be interesting to evaluate the resistances retention resulting from the consecutive pulse-timing modulations. Thermal stability of the resistance states can be also measured by elevated temperature retention tests. Furthermore, the impact of other intermediate layers on the W-based transient operation shall be investigated by including the combination of other oxygen scavenging and oxygen barrier materials using different deposition techniques.

ReRAM-CMOS co-integration

Regarding the ReRAM-CMOS integration on the framework of CMOS post-processing, the first attempt shall be the control of the ReRAM operation through an active CMOS circuitry. Moreover, we showed the process flow for the integration of ReRAM on the extremely small CMOS chips with the dimension of $1.6 \times 1.6\,\mathrm{mm}^2$ adding excessive efforts due to the handling and incompatibility of processing tools. The technique is suitable for different ReRAM applications and can be easily adopted on the larger die and the wafer-scale post-processing to obtain self-rectifying devices with high density. Finally, considering the difficulties associated with the forming operation of ReRAM in the circuit level, the form-less characteristics of the (W/WOx/TiN) should be taken into account for the better optimization of the RTP to acquire reliable and stable performances.

Fast ion-conducting thin films for resistive switching

The potential of CGO as ReRAM switching layer has been shown using both shadow-mask and photolithography processes while for YSZ, further studies are still required on the scaled-down cells process and characterization. Regarding the multi-states performance of CGO-based ReRAM, more pulse programming tests can support the determination of the inherent learning capabilities of the devices. It is also important to estimate the persistence of the multiple states achieved by means of pulse timing and Reset pulse voltage control at both room and elevated temperature. Since, there are few studies on these materials, the effect of other buffer/barrier layers and electrodes on both CGO and YSZ should be studied to have more understanding on the switching mechanism, enhance the device performance reliability and lowering the operating current. The study of resistive switching mechanism has to be enriched by TEM and conductive AFM in order to support the interface oxide formation and multi-filament switching. Finally, as the ultimate goal, the CGO and YSZ in ReRAM should be adopted and optimized with W electrode to be implemented on the BEoL of CMOS.

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