High-performance nanowire-based E-mode Power GaN MOSHEMTs with large work-function gate metal

Luca Nela, Minghua Zhu, *Student Member,* Jun Ma, and Elison Matioli, *Member, IEEE*

Abstract— **In this work, we demonstrate high-performance Enhancement-mode (E-mode) GaN Metal-Oxide-Semiconductor High Electron Mobility Transistors (MOS-HEMTs) on Si substrate based on sidewall depletion achieved by nanostructured gate with large work-function metal. The devices presented threshold voltage (V_{TH}) over 0.6 V at 1 μA/mm, large current density (I_{DS}) up to 590 mA/mm, low specific on resistance ($R_{ON,SP}$) of 1.33 mΩ·cm^2, high ON/OFF ratio over 10^{10} and large breakdown voltage (V_{BR}) of 1080 V at 1 μA/mm with grounded substrate. The excellent high power FOM of 877 MW/cm^2 reveals the potential of our approach to obtain E-mode operation, while maintaining exceptional on-state performance and high V_{BR}.**

***Index Terms*— GaN, HEMT, E-mode, Sidewalls depletion, Pt gate, work-function engineering**

I. Introduction

AlGaN/GaN MOS-HEMTs have emerged as promising candidates for high power applications due to superior properties of GaN such as large critical electric field and high electron saturation velocity [1], [2]. However, the presence of a 2D electron gas (2DEG), induced by spontaneous and piezoelectric fields in AlGaN/GaN heterojunction, results naturally in depletion mode (D-mode) operation, which is undesirable for power applications due to safety concerns, and would require an increased complexity for gate drivers. Several methods have been proposed to achieve E-mode devices, among which the most common are based on p-type GaN cap-layers [3]–[7], fluorine implantation [8], [9] and gate recess [10]–[14]. These methods rely on depleting the 2DEG under the gate by removing, by treating the AlGaN barrier, or by depositing p-GaN over the barrier.

Recently, fin-shaped tri-gate structures, formed by structuring parts of the gate region [10], have been developed to demonstrate high-voltage GaN MOS-HEMTs with superior gate control, leading to large ON-OFF ratios and small sub-threshold slopes (*SS*), along with much reduced leakage current, and significantly increased breakdown voltages [15]–[17]. In addition, an excellent control of the threshold voltage (V_{TH}) in tri-gates, achieved by changing the fin width (w), offers an additional device design tool [17] and has been explored to reach E-mode operation in previous works [18]–[21]. This approach relies only on one lithography step to achieve positive threshold voltage through strain relaxation of the barrier layer and electron depletion from the fin sidewalls, and does not require any critical etching as for gate recess or p-GaN gates. However, devices exploiting sidewalls depletion from the fins alone still show negative V_{TH} (defined at 1 μA/mm) and often suffer from performance degradation due to the small fin widths required for E-mode operation. Novel approaches are required to further increase the threshold voltage to positive values and to resolve the performance degradation in narrow nanowires.

In this work, we present high-performance E-mode AlGaN/GaN MOS-HEMTs based on a large work-function gate metal, deposited over nanowires in the gate region, which led to complete sidewall depletion and positive V_{TH}. In addition, a judicious design of the nanostructured gate geometry mitigated the performance degradation caused by the 2DEG removal, and also improved the device breakdown voltage by converting part of the gate electrode into a gate-connected field plate [15]. This resulted in state-of-the-art E-mode devices with positive V_{TH} > 0.6 V at 1 μA/mm, low $R_{ON,\,SP}$ of 1.33 mΩ·cm^2, large I_{DS} up to 590 mA/mm and high V_{BR} of 1080 V with grounded substrate.

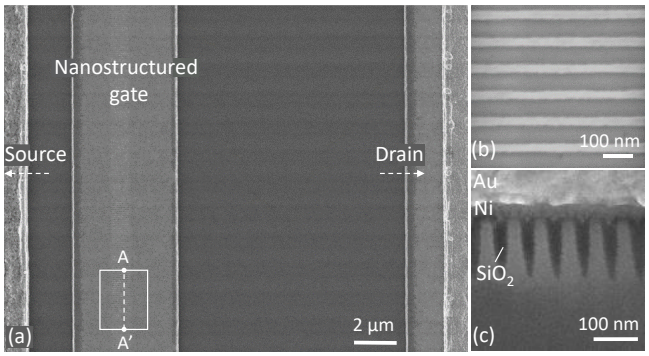

Fig. 1. (a) Top-view SEM image of the device channel region, in which the nanostructured gate region is highlighted. (b) Zoomed SEM image of the nanowire region with 20 nm-wide fins and 50 nm spacing, before gate oxide deposition. (c) Cross-section SEM of the gate nanowires along the AA' line. The fins are conformally covered only by 20 nm ALD SiO_2, on top of which the Ni-Au or Pt-Au gate stacks were deposited.

II. Device structure

The devices were fabricated on a GaN-on-Si heterostructure consisting of 5.4 μm of buffer, 320 nm of unintentionally doped GaN (u-GaN) channel, 24.6 nm of $Al_{0.25}Ga_{0.75}N$ barrier and 3.3 nm of u-GaN cap-layer. The electron concentration and

This work was supported in part by the Swiss National Science Foundation under Assistant Professor (AP) Energy Grant PYAPP2_166901 and in part by the European Research Council under the European Union's H2020 Program/ERC Grant Agreement 679425. The authors are with the Power and Wide-band-gap ElectronicsResearch Laboratory (POWERlab), ÉcolePolytechnique Fédérale de Lausanne, CH-1015 Lausanne, Switzerland (e-mail: luca.nela@ epfl.ch; elison.matioli@epfl.ch).

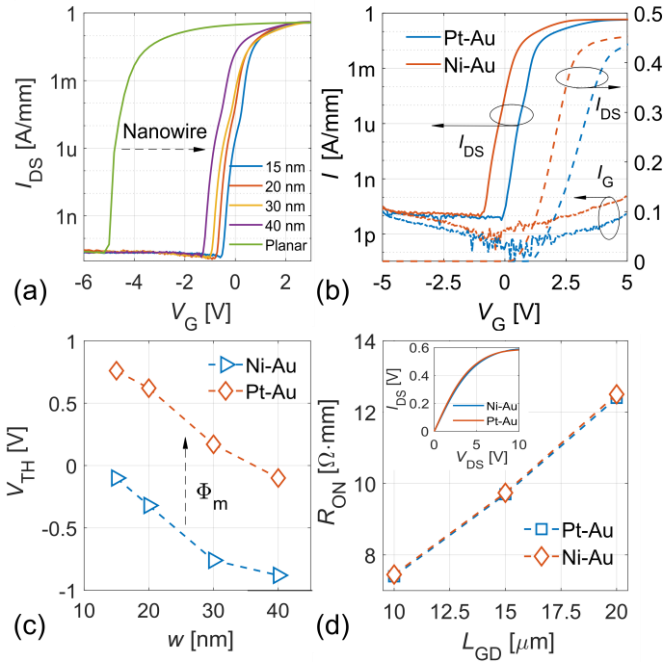

Fig. 2. (a) Transfer curve for different fin width for Ni-Au gate stack at V_{DS}=5 V. As the nanowire width decreases, V_{TH} further approaches 0 V (b) Transfer curve comparison for the same fin width and spacing for Ni-Au and Pt-Au gate stack for V_{DS} = 5 V. The corresponding gate leakage for the two gate metal stacks is also shown. (c) V_{TH} (defined at 1 μA/mm) as a function of the fin width and gate metal. A positive V_{TH} shift of around 0.8 V is consistently observed between the two metal stacks for the different widths. (d) R_{ON} vs L_{GD} for the same fin width and spacing for Ni-Au and Pt-Au gate stack for a saturation gate voltage of 7 V. No difference in R_{ON} is observed between the gate metals. Inset: typical output curves for L_{GD}=10 μm for Ni and Pt gates.

mobility of the 2DEG from Hall measurements at room temperature were 1.3 × 10^{13} cm^{-2} and 1700 $cm^2/V{\cdot}s$, respectively. A scanning electron microscopy (SEM) image of the device channel is shown in Fig. 1(a). The fabrication process started with electron-beam lithography to define the mesa and nanowires in the gate region. The sample was then etched by Cl_2-based inductively coupled plasma etching (ICP) to a depth of 165 nm. The width of the 700 nm-long nanowires in the gate was varied from 15 nm to 40 nm to investigate the effect of sidewall depletion (Fig. 1(b)). The source and drain ohmic contacts were formed by a stack of Ti (20 nm)/Al (120 nm)/Ti (40 nm)/Ni (60 nm)/Au (50 nm) and annealed at 780 °C for 30 s. 20 nm-thick SiO_2 was conformally deposited over the nanowires by atomic layer deposition (ALD) as gate dielectric. Two types of work-function metals deposited over the gate region were investigated: Ni/Au (50 nm/150 nm) and Pt/Au (50 nm/150 nm). No passivation layer was deposited on top of the devices. A Focused Ion Beam (FIB) cross-section of the nanostructured gate region is shown in Fig. 1(c). Unlike in tri-gate structures [15], [17], the gate metal did not penetrated too far in between nanowires due to the small spacing of 50 nm. The transistor dimensions are L_{GS} = 2 μm, L_G = 3 μm and L_{GD} = 10 μm, 15 μm and 20 μm. Device characteristics such as R_{ON}, I_{DS}, I_{OFF} and transconductance (g_m) were normalized by the entire device footprint of 60 μm, rather than by the fin width.

III. Results and Discussion

The I_{DS} versus V_{GS} transfer characteristics for transistors with

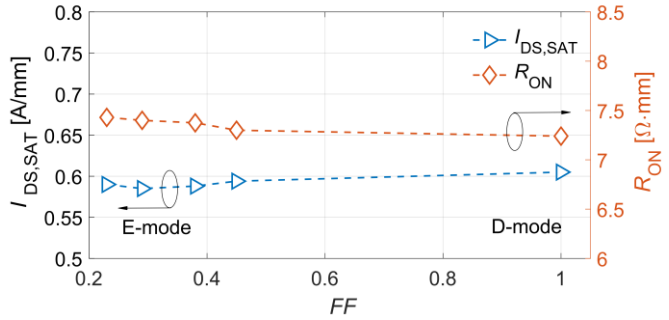

Fig. 3. On-resistance R_{ON} and saturation current $I_{DS,\,SAT}$ versus filling factor (*FF*). The planar gate corresponds to *FF* = 1. A minor degradation, smaller than 3%, is observed for the nanostructured gate devices.

standard Ni-Au gate metal stack are presented in Fig. 2(a). Reference devices with planar gates, co-fabricated on the same chip, presented normally-on behavior with V_{TH} = -4.8 V. A significant shift in V_{TH} of about 4 V was achieved by patterning 700 nm-long nanowires in the gate region with *w* of 40 nm. As the fin width was reduced, V_{TH} further approached 0 V, which is mainly due to strain relaxation of the AlGaN/GaN in addition to sidewalls depletion [20], [22], [23]. However, this is not enough to achieve fully E-mode operation, even for a nanowire width down to 15 nm. This result agrees well with previous works [16], [24] and illustrates the difficulty to achieve normally-off behavior relying solely on sidewall depletion.

To further shift V_{TH} to positive values, an additional mechanism based on the use of a large work-function (ϕ_m) gate metal was deployed. While a similar method has been proposed for p-GaN HEMTs [5], [25], its effect in the presence of a gate oxide requires additional studies. For a MOS-HEMT, the expression of V_{TH} is linearly dependent on the barrier height ϕ_B

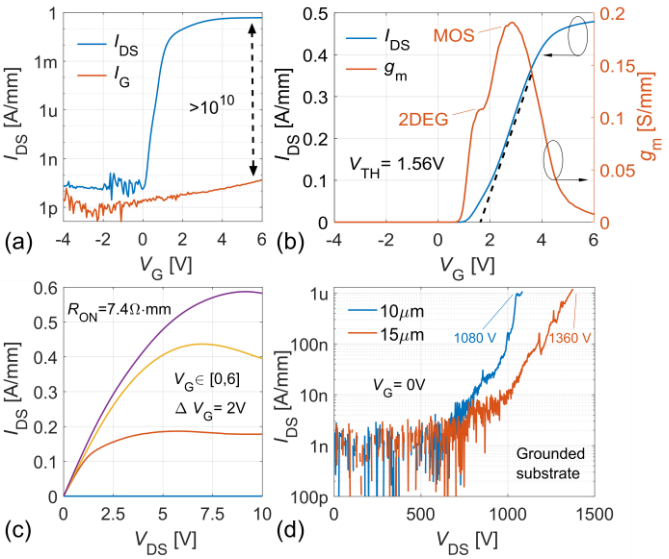

Fig. 4. (a) Device transfer characteristic in logarithmic scale and the corresponding gate leakage for V_{DS} = 5 V. V_{TH} defined at 1 μA/mm is 0.64 V while the Subthreshold Slope (SS) is 110 mV/dec. (b) Linear scale transfer curve and transconductance g_m for V_{DS} = 5 V. V_{TH} from linear extrapolation is 1.56 V. g_m shows two convoluted peaks corresponding to conduction through the fin 2DEG and the MOS channel at the fin sidewalls (c) Output characteristics with V_G ranging from 0V to 6V with ΔV_G=2 V. (d) Breakdown characteristics for L_{GD} of 10 μm and 15 μm. The breakdown voltage is defined at I_{DS} = 1 μA/mm. All the device characteristics have been normalized by the total device footprint (60 μm).

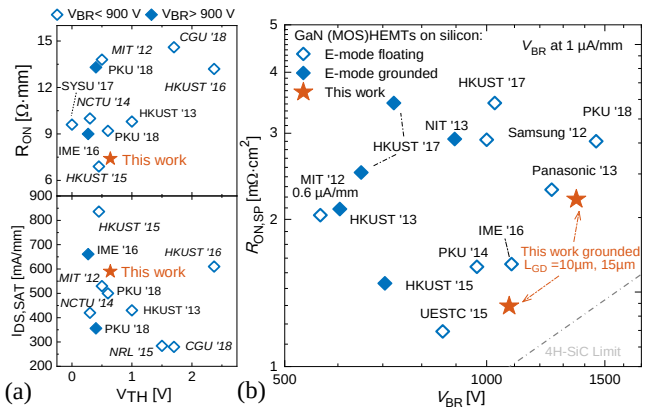

Fig. 5. (a) R_{ON} and $I_{DS,\ SAT}$ versus V_{TH} benchmark for the presented devices compared with E-mode GaN-on-Silicon (MOS)HEMTs. Both V_{TH} and V_{BR} are defined for a current I_{DS} of 1 μA/mm. Devices presenting a large breakdown > 900 V are highlighted in solid blue. (b) $R_{ON,\ SP}$ vs V_{BR} benchmark for the presented devices against state of the art GaN E-mode (MOS)HEMTs on Silicon. V_{BR} results determined with grounded substrate are presented in solid blue. For fair comparison, literature results with unspecified R_{ON}, $I_{DS,\ SAT}$ or I_R were not included.

between the metal and the gate dielectric [9], [26], which can be increased by selecting a gate metal with larger ϕ_m. The larger work-function of Pt (5.64-5.91 eV) [27] compared to that of Ni (5.04-5.35 eV) [28], resulted in a positive V_{TH} shift of about 0.8 V (Fig. 2(b)), which was consistent for all fin widths investigated (Fig. 2(c)), resulting in E-mode operation for devices with fin width below 30 nm. The observed shift agrees well with the work-function difference between the two metals and suggests that SiO_2/AlGaN interface Fermi level is unpinned, which is in agreement with Ref. [29]. In addition, the larger Pt work-function leads to a decrease of the forward gate leakage of about one order of magnitude (Fig. 2(b)). No difference in R_{ON} versus L_{GD} was observed between Ni-Au and Pt-Au gate stacks (Fig. 2(d)).

To determine the influence of w on the device performance, R_{ON} and $I_{DS,\ SAT}$ were extracted from the device output curves and plotted versus their filling factor ($FF = w_{Fin} / w_{Period}$). No clear degradation was observed for FF varying from 0.45 to 0.23, since a decrease in the FF leads to a larger number of nanowires in the gate region which enhances sidewall conduction and compensates the loss of 2DEG due to etching. Even with respect to a planar gate device (FF = 1), the increase in R_{ON} due to the narrow nanowires in the gate is minor (~ 3%) (Fig. 3). This is a remarkable result that offers a large freedom for device design, as the nanowire width mainly affects the V_{TH} without degrading significantly the device output characteristics.

The transfer curve for a typical Pt-Au nanostructured device with w of 20 nm and L_{GD} of 10 μm is shown in Figs. 4 (a,b), presenting V_{TH} of 0.64 V at I_{DS} = 1 μA/mm, while from the linear extrapolation in linear scale, V_{TH} is 1.56 V. Thanks to the small gate dielectric leakage, the ratio of drain to gate current at V_G = 6 V is still >10^{10}. Despite the fact that the gate metal does not fill the trenches between nanowires, as in typical tri-gate structures, the gate control is excellent with ON/OFF ratio > 10^{10}, subthreshold slope (SS) of 110 mV/dec, large transconductance peak of 190 mS/mm and ultra-small leakage currents. The g_m curve exhibits two convoluted peaks at positive V_G corresponding to the conduction contribution from the 2DEG in the fin top layer and the MOS channel at the fin sidewalls (Fig. 4(b)). The transfer curve hysteresis from double sweep measurement was 0.35 V for V_G up to 3 V along with interface trap density D_{it} of about 1.3 × 10^{12} cm^{-2} eV^{-1} extracted for the subthreshold slope [10]. An increase in hysteresis was observed for larger gate voltages which is believed to be due to the poor ALD oxide quality obtained in this batch, since previous nanostructured devices with similar device geometry did not present this issue. No clear difference from gate-lag measurements has been observed between the nanostructured and planar devices. Preliminary dynamic R_{ON} measurement showed an improvement in current collapse for the nanowire devices thanks to the better electric field distribution due to the intrinsic gate-connected field plate [15], [30], however further studies in the presence of a passivation layer will be performed in future experiments. The output characteristics of the device shown in Fig. 4(c), reveals a R_{ON} of 7.4 Ω·mm for L_{GD} of 10 μm, corresponding to a very small $R_{ON,\ SP}$ of 1.33 mΩ·cm^2 (considering a 1.5 μm transfer length for each ohmic contact). The V_{BR} of these devices, defined at 1 μA/mm, was extracted for a V_G of 0 V with grounded substrate (Fig. 4(d)), resulting in 1080 V and 1360 V for L_{GD} of 10 μm and 15 μm, respectively. The V_{BR} for L_{GD} 15 μm was limited by the vertical buffer V_{BR} of 1350 V, determined separately from 2 terminal breakdown measurements. The devices were then benchmarked against state-of-the-art E-mode GaN-on-Si (MOS)HEMTs, comparing $V_{TH,}$ R_{ON} and $I_{DS,SAT}$ (Fig. 5(a)) and V_{BR} and $R_{ON,SP}$ (Fig. 5(b)). It is noteworthy that the R_{ON} of these nanowire-based devices was among the lowest values compared to E-mode GaN devices in the literature. This resulted in an excellent high-power FOM of 877 MW/cm^2 for L_{GD} of 10 μm.

IV. Conclusions

In this work we demonstrated high-performance nanostructured E-mode MOSHEMTs on Si based on the combination of sidewalls depletion with high work-function Pt gate metal with V_{TH} > 0.6 V at 1 μA/mm, low $R_{ON,SP}$ of 1.33 mΩ·cm^2, large I_{DS} of 590 mA/mm, and high V_{BR} over 1050 V. These results demonstrate the outstanding potential of this technology for power applications.

Acknowledgment

The authors would like to acknowledge the staff of CMI and ICMP cleanrooms at EPFL for their technical support. In particular, they would like to thank Zdenek Benes for his help with electron beam lithography.

References

[1] T. P. Chow and R. Tyagi, "Wide Bandgap Compound Semiconductors for Superior High-Voltage Unipolar Power Devices," *IEEE Trans. Electron Devices*, vol. 41, no. 8, pp. 1481–1483, 1994, doi: 10.1109/16.297751.

[2] R. F. Davis, "III-V Nitrides for Electronic and Optoelectronic Applications," *Proc. IEEE*, vol. 79, no. 5, pp. 702–712, 1991, doi:

10.1109/5.90133.

[3] G. Greco, F. Iucolano, and F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate," *Mater. Sci. Semicond. Process.*, no. July, pp. 0–1, 2017, doi: 10.1016/j.mssp.2017.09.027.

[4] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel, and J. Wurfl, "Normally-off AlGaN/GaN HFET with p-type GaN gate and AlGaN buffer," *2010 6th Int. Conf. Integr. Power Electron. Syst.*, pp. 1–4, 2010.

[5] I. Hwang, J. Kim, H. S. Choi, H. Choi, J. Lee, K. Y. Kim, J. B. Park, J. C. Lee, J. Ha, J. Oh, J. Shin, and U. I. Chung, "P-GaN Gate HEMTs with tungsten gate metal for high threshold voltage and low gate current," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 202–204, 2013, doi: 10.1109/LED.2012.2230312.

[6] G. Lukens, H. Hahn, H. Kalisch, and A. Vescan, "Self-Aligned Process for Selectively Etched p-GaN-Gated AlGaN/GaN-on-Si HFETs," *IEEE Trans. Electron Devices*, pp. 1–7, 2018, doi: 10.1109/TED.2018.2860634.

[7] R. Hao, K. Fu, G. Yu, W. Li, J. Yuan, L. Song, Z. Zhang, S. Sun, X. Li, Y. Cai, X. Zhang, and B. Zhang, "Normally-off p -GaN/AlGaN/GaN high electron mobility transistors using hydrogen plasma treatment," *Appl. Phys. Lett.*, vol. 109, no. 15, pp. 1–5, 2016, doi: 10.1063/1.4964518.

[8] Z. H. Feng, R. Zhou, S. Y. Xie, J. Y. Yin, J. X. Fang, B. Liu, W. Zhou, K. J. Chen, and S. J. Cai, "18-GHz 3.65-W/mm enhancement-mode AlGaN/GaN HFET using fluorine plasma ion implantation," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1386–1388, 2010, doi: 10.1109/LED.2010.2072901.

[9] Y. Cai, Y. Zhou, K. M. Lau, and K. J. Chen, "Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based plasma treatment: From depletion mode to enhancement mode," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2207–2214, 2006, doi: 10.1109/TED.2006.881054.

[10] B. Lu, E. Matioli, and T. Palacios, "Tri-gate normally-off GaN power MISFET," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 360–362, 2012, doi: 10.1109/LED.2011.2179971.

[11] T. Oka and T. Nozawa, "AlGaN/GaN recessed MIS-Gate HFET with high-threshold-voltage normally-off operation for power electronics applications," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 668–670, 2008, doi: 10.1109/LED.2008.2000607.

[12] D. H. Son, Y. W. Jo, R. H. Kim, C. Heo, J. H. Seo, J. S. Kim, I. M. Kang, S. Cristoloveanu, and J. H. Lee, "Fabrication of high performance AlGaN/GaN FinFET by utilizing anisotropic wet etching in TMAH solution," in *Eur. Solid-State Device Res. Conf.*, 2015, vol. 2015–Novem, pp. 130–133, doi: 10.1109/ESSDERC.2015.7324730.

[13] S. D. Burnham, K. Boutros, P. Hashimoto, C. Butler, D. W. S. Wong, M. Hu, and M. Micovic, "Gate-recessed normally-off GaN-on- Si HEMT using a new O2-BCl3 digital etching technique," *Phys. Status Solidi*, vol. 7, no. 7–8, pp. 2010–2012, 2010, doi: 10.1002/pssc.200983644.

[14] M. Hua, Z. Zhang, J. Wei, J. Lei, G. Tang, K. Fu, Y. Cai, B. Zhang, and K. J. Chen, "Integration of LPCVD-SiNxgate dielectric with recessed-gate E-mode GaN MIS-FETs: Toward high performance, high stability and long TDDB lifetime," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, p. 10.4.1-10.4.4, 2017, doi: 10.1109/IEDM.2016.7838388.

[15] J. Ma and E. Matioli, "High Performance Tri-Gate GaN Power MOSHEMTs on Silicon Substrate," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 367–370, 2017, doi: 10.1109/LED.2017.2661755.

[16] S. Takashima, Z. Li, and T. P. Chow, "Sidewall dominated characteristics on fin-gate AlGaN/GaN MOS-Channel-HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3025–3031, 2013, doi: 10.1109/TED.2013.2278185.

[17] J. Ma and E. Matioli, "Slanted Tri-Gates for High-Voltage GaN Power Devices," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1305–1308, 2017, doi: 10.1109/LED.2017.2731799.

[18] K. Ohi and T. Hashizume, "Drain current stability and controllability of threshold voltage and subthreshold current in a multi-mesa-channel AlGaN/GaN high electron mobility transistor," *Jpn. J. Appl. Phys.*, vol. 48, no. 8 Part 1, pp. 0810021–0810025, 2009, doi: 10.1143/JJAP.48.081002.

[19] K. S. Im, C. H. Won, Y. W. Jo, J. H. Lee, M. Bawedin, S. Cristoloveanu, and J. H. Lee, "High-performance GaN-based nanochannel FinFETs With/Without AlGaN/GaN heterostructure," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3012–3018, 2013, doi: 10.1109/TED.2013.2274660.

[20] K. Ren, Y. C. Liang, and C. F. Huang, "Physical mechanism of fin-gate AlGaN/GaN MIS-HEMT: Vth model," *WiPDA 2016 - 4th IEEE Work. Wide Bandgap Power Devices Appl.*, pp. 319–323, 2016, doi: 10.1109/WiPDA.2016.7799960.

[21] C. Y. Chien, W. H. Wu, Y. H. You, J. H. Lin, C. Y. Lee, W. C. Hsu, C. H. Kuan, and R. M. Lin, "Breaking Through the Multi-Mesa-Channel Width Limited of Normally Off GaN HEMTs Through Modulation of the Via-Hole-Length," *Nanoscale Res. Lett.*, vol. 12, 2017, doi: 10.1186/s11671-017-2189-3.

[22] M. Azize and T. Palacios, "Top-down fabrication of AlGaN/GaN nanoribbons," *Appl. Phys. Lett.*, vol. 98, no. 4, 2011, doi: 10.1063/1.3544048.

[23] O. Landré, D. Camacho, C. Bougerol, Y. M. Niquet, V. Favre-Nicolin, G. Renaud, H. Renevier, and B. Daudin, "Elastic strain relaxation in GaN/AlN nanowire superlattice," *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 81, no. 15, pp. 1–4, 2010, doi: 10.1103/PhysRevB.81.153306.

[24] S. Liu, Y. Cai, G. Gu, J. Wang, C. Zeng, W. Shi, Z. Feng, H. Qin, Z. Cheng, K. J. Chen, and B. Zhang, "Enhancement-mode operation of nanochannel array (NCA) AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 354–356, 2012, doi: 10.1109/LED.2011.2179003.

[25] G. Greco, F. Iucolano, S. Di Franco, C. Bongiorno, A. Patti, and F. Roccaforte, "Effects of Annealing Treatments on the Properties of Al/Ti/p-GaN Interfaces for Normally off p-GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 63, no. 7, pp. 2735–2741, 2016, doi: 10.1109/TED.2016.2563498.

[26] Y. Zhang, M. Sun, S. J. Joglekar, and T. Palacios, "High threshold voltage in GaN MOS-HEMTs modulated by fluorine plasma and gate oxide," *Device Res. Conf. - Conf. Dig. DRC*, vol. 1280, no. September 2012, pp. 141–142, 2013, doi: 10.1109/DRC.2013.6633833.

[27] T. Tadaaki, "Analysis of Work Functions of Noble Metals in Ambient Atmosphere in Commemoration of Journal Award," *J. Soc. Photogr. Imag. Japan*, vol. 78, no. 1, pp. 16–22, 2015.

[28] B. G. Baker, B. B. Johnson, and G. L. C. Maire, "Photoelectric work function measurements on nickel crystals and films," *Surf. Sci.*, vol. 24, no. 2, pp. 572–586, 1971, doi: 10.1016/0039-6028(71)90282-2.

[29] G. Li, S. Member, T. Zimmermann, Y. Cao, C. Lian, X. Xing, S. Member, R. Wang, P. Fay, S. Member, H. G. Xing, and D. Jena, "Threshold Voltage Control in Al0.72Ga0.28N/AlN/GaN HEMTs by Work-Function Engineering," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 954–956, 2010, doi: 10.1109/LED.2010.2052912.

[30] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200-V normally off GaN-on-Si field-effect transistors with low dynamic on -resistance," *IEEE Electron Device Lett.*, vol. 32, no. 5, pp. 632–634, 2011, doi: 10.1109/LED.2011.2118190.