Resistive Switching Memory Architecture Based on Polarity Controllable Selectors

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***Abstract*—With the continuous scaling of CMOS technology, integrating an embedded high-density non-volatile memory appears to be more and more costly and technologically challenging. Beyond floating-gate memory technologies, bipolar *Resistive Random Access Memories* (RRAM) appear to be one of the most promising technologies. However, when organized in a *1 or 2-Transistor 1-RRAM* (1T1R, 2T1R) architectures, they suffer from large bitcell area, degraded performance and reliability issue during *reset* operation. The association of multiple-independent-gate *Polarity Controllable Transistors* (PCT) with RRAM overcomes these drawbacks, while providing a dense structure. In this paper, we present two innovative PCT-based bitcells and propose an extensive study of their functionality, physical design considerations and performances in read and write operations compared to CMOS-based 1T1R and 2T1R bitcells. The proposed bitcells outperform the performances of 1T1R and 2T1R bitcells in *reset* (5× to 105× speed improvement) are competitive in term of area (1.35× to 2.6× area reduction versus 2T1R) and avoid gate overdrive (1.2V versus more than 2V in 1T1R bitcells) thus reducing selector reliability concerns. We also propose an innovative programming strategy which takes advantage of the PCT polarity control and enabling 500× improvement in *reset* performance. Finally, the proposed bitcells performs 15 to 67% faster than CMOS bitcells in read.**

Keywords—Embedded Memory ; bipolar RRAM; OxRAM; Polarity Controllable Transistors; SiNWFET; 1T1R; 2T1R.

I. INTRODUCTION

With the introduction of advanced CMOS nodes (<2x nm) [1] and the scaling limitation reached by the classical charge storage memory, *Resistive Random Access Memory* (RRAM) appears more and more as a potential candidate to replace conventional *Non-Volatile Memory* (NVM) in microcontrollers *embedded NVM* (eNVM) devices. Among all others *Back-End-of-Line* (BEoL) resistive memory candidates (e.g. *Phase Change* or *Magnetic Memory* – PCM, MRAM), *Oxide-based* and *Conductive bridge-based RRAM* (OxRAM, CBRAM) are the most promising since their *Metal-Insulator-Metal* (MIM) structure is composed of materials already available in foundries, thereby driving down the process costs [2] [3]. However, while bipolar behavior (featured by most of the 2-terminals OxRAM, CBRAM or MRAM technologies) enables better endurance and lower energy consumption [4] than unipolar device, new constraints appear if co-integrated with unipolar selectors such as *Metal Oxide Semiconductor* (MOS) transistors.

When used with bipolar RRAM technologies, unipolar MOS selectors cannot perform equally in each polarity and lead to strongly unbalanced programming operations [5] and strongly overdriven selector during *reset* operation [6] [7] [8] [9], (leading to faster aging of the selector). To overcome this issue, we propose the use of *Polarity Controllable Transistors* (PCT) such as the *multiple independent all-around gate transistors* [10] which are opening a new era in microelectronic circuit design. These transistors enable a dynamic majority carrier selection and so, provide on-demand *n*-type/*p*-type MOS transistor behavior. While PCT have been actively studied for digital circuit design in order to reduce the computation logic area and complexity [11] [12] [13] [14], PCT-based memories, and particularly *Non-Volatile Memories* (NVM) have been poorly studied. To the extent of our knowledge, only [15] proposed a NVM architecture using PCT and *Spin Transfer Torque* (STT-MRAM) memory technology to increase the security of memories. To this end, in [15], the transistor polarity is adjusted depending on the performed programming operation in order to use similar current levels during *set* and *reset*. This leads to a homogeneous thermal and power signature hardening side channel attacks. However, this study does not cover array considerations and there are no reported studies on classical memory architectures.

In this work, we first propose, to highlight the limitations of standard CMOS-based architectures (*1Transistor 1 RRAM* – 1T1R and *2Transistors 1RRAM* – 2T1R [5]). Then, we explore the operation of PCT-based RRAM bitcells and show that these structures can solve the previously identified CMOS bitcells issues without requiring gate overdrive or area increase. Then, we propose two PCT-based array organizations: one standard *1PCT 1RRAM* (1PCT1R) bitcell and an innovative *cross-shaped 1PCT1R* bitcell (1XPCT1R). We demonstrate the operation and functionality of the proposed bitcells by simulating it with an OxRAM compact model [16] calibrated on recent experimental results [17], a 25nm Silicon NanoWire FET (SiNWFET) PCT technology model [18] calibrated on measurement and TCAD data [19], and use as a reference a 28nm low-power CMOS industrial *Product Design Kit* (PDK).

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The main contributions of this work are as follow:

- We propose two innovative PCT-based bitcells featuring $16F^2$ and $25F^2$ density (1.35× and 2.6× area reduction compared to 2T1R).
- We show that for equivalent *reset* conditions, the PCT-based bitcells outperform 1T1R (75× for a 2.2BL-SL voltage at 2V gate overdrive) and 2T1R bitcell (5× at SL-BL=1.8V and 105× at BL-SL=2.2V for a 1.2V gate voltage). On the other hand, the proposed PCT-bitcell do not degrade *set* performances.
- We propose a new programming strategy for PCT-based architectures improving further the *reset* process by performing it with the *n*-type PCT while doing the *set* operation with the *p*-type. We show that *n*-type *reset* enables 500× *reset* time reduction compared to *p*-type *reset*.
- Finally, we benchmark the proposed bitcells in *read* operation and we show: *(i)* from 30 to 67% of *read* time reduction compared to 2T1R, *(ii)* only 8.6% longer *read* time for the 1PCT1R compared to 1T1R and *(iii)* 15% *read* time reduction for 1XPCT1R compared to 1T1R. We take advantage of the lower bitcell density to connect less bitcells to the memory lines, enabling faster *read* operation than CMOS 1T1R (except for extremely wide and thin arrays : more than 300 columns and less than 100 rows).

The remainder of this paper is organized as follows. Section II presents the general background of this work. Section III introduces typical RRAM arrays organizations and identifies its limitations. Section IV presents PCT-based OxRAM bitcell schematic principle and operations mode. Section V proposes a breakthrough PCT-based RRAM bitcell. Section VI evaluates the performance indicators of the proposed approaches. Finally, Section VII discusses and draws the general conclusions of the paper.

II. Background

In this section, we give a brief overview of both technologies, namely Resistive memories (RRAM) technology and *Polarity Controllable Transistor* (PCT) technology. Thereby, we first present the operation of bipolar RRAM with a focus on OxRAM technology, then we introduce PCT technologies with a focus on *Silicon NanoWire FET* (SiNWFET) technology. Finally, the complete simulation set-up together with the compact models used for both technologies is addressed.

A. Bipolar Resistive Switching Memories

Trendy technologies such as *Spin-Transfer Torque Magnetic Memories* (STT-MRAM), *Oxide-based* and *Conductive Bridge-based Resistive Switching Memories* (OxRAM, CBRAM) or *Phase Change Memories* (PCM) are extensively explored by both academic and industrial groups as future replacement candidates for flash technologies [20] [21] [22]. Among these, bipolar OxRAM/CBRAM technologies are seen as the most promising technologies thanks to their fabrication friendly materials, their low cost *Back-End-of-Line* (BEoL) process, their high scalability and their fast switching [17]. Finally, OxRAM technology is currently used in microcontrollers products as data and program memory replacing eFlash [23] [3].

Figure 1 presents the switching operations of a bipolar OxRAM. The *electroforming* step (in green) required by some RRAM technologies [24] [6] in order to create a first oxygen vacancies-based conductive filament is not considered here and assumed to be already performed. Then, the OxRAM can be switched from *Low Resistance State* (LRS) to *High Resistance State* (HRS) by *reset* operation (in red) or from HRS to LRS by a *set* operation (in blue). As a bipolar technology, OxRAM memory is programmed by applying opposed polarity programming pulses across its terminals. *Set* operation is performed by applying a positive voltage difference between the *Top Electrode* (TE) and the *Bottom Electrode* (BE) terminals and limiting the Iprog current to control the achieved LRS value. Oppositely, the *reset* operation is performed by applying a positive voltage difference between the BE and the TE.

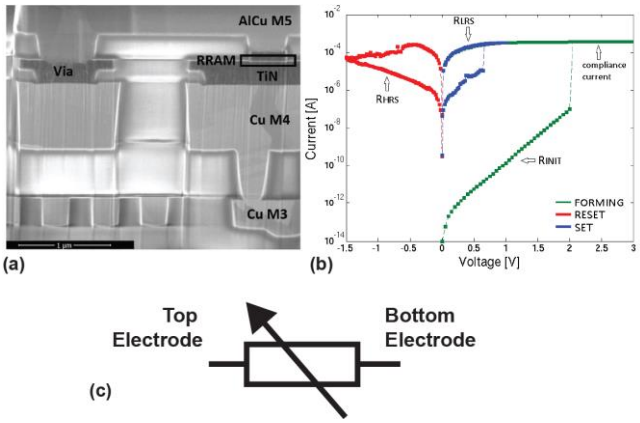

Figure 1: (a) TEM cross-section of an OxRAM memory co-integrated in a 130nm CMOS BEoL process [6]. *(b) I-V curve of the operation of an OxRAM with forming (green), set(blue) and reset (red) operation highlighted* [25]. *(c) Symbol view considered in this paper, the Top Electrode is considered as deposited the latest during the fabrication steps.*

B. Polarity Controllable Transistor

In parallel to the evolution of regular CMOS technologies, the polarity-control behavior has been demonstrated for highly scaled FET devices (below 30nm nodes) based on silicon nanowires [26] [27], carbon nanotubes [28], graphene [29], FinFETs [10] and WSe-based field effect transistors [30]. Among these technologies, the *Silicon NanoWire Fied Effect Transistor* (SiNWFET) using a gate-all-around process appears to be the most natural evolution from FinFET transistors [31]. Figure 2-a and b presents the physical structure of the considered SiNWFET transistors. *Polarity controllable devices* provide huge flexibility, by controlling the voltages on the two *Polarity Gates* (PGs and PGd), on the *Control Gate* (CG), on the *Drain* and the *Source*, several effects can be obtained: polarity control, subthreshold slope control or threshold voltage modulation. These effects have been widely used for logic enhancement [11] [12] but were barely explored in the memory field. In this paper we propose to use the polarity control effect presented Figure 2-c to enhance non-volatile bipolar RRAM memories

performances. By changing the polarity gates bias, it is possible to switch from an *n*-type MOS behavior to a *p*-type MOS behavior. The symbol introduced Figure 2-d represents the PCT where PGs and PGd are connected together under the Polarity Gate (PG) label.

C. Simulation Methodology

The model used to simulate the oxide-based RRAM relies on electric field-induced creation/destruction of oxygen vacancies within the switching layer, as presented in [16] and is calibrated with data from HfO_2 OxRAM technology from [17]. The memory resistance is directly linked to the radius of the *Conductive Filament* (CF), which is calculated thanks to a single master equation continuously accounting for both *forming*/*set* and *reset*. The model takes into account various phenomenon, including the switching time dependency versus the applied voltage for all operations, the relationship between the programming current and the achieved resistance state as well as the temperature effect on all operations. In the following simulations we considered that the OxRAM *forming* step has already been performed.

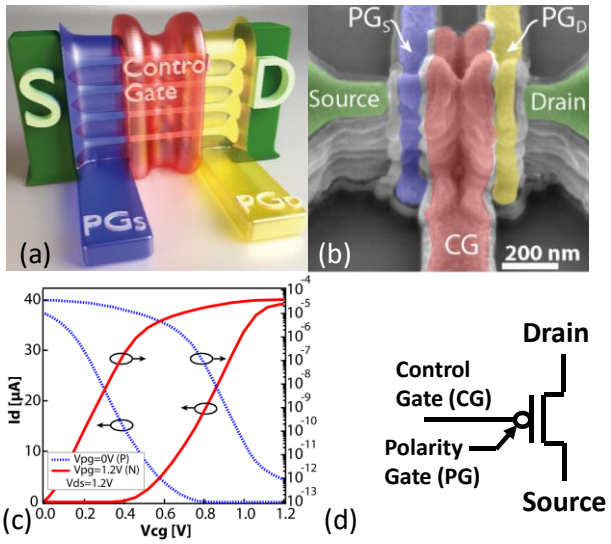

Figure 2: (a) 3D view of a Polarity Controllable SiNWFET structure. (b) Tilted SEM view with detailed polarity gates PGs and PGd (blue and yellow), control gate CG (red), drain D and source S (green) [10]. *(c) Simulated I-V curves of n-type (red) and p-type (blue) operation in a 25nm equivalent node* [19] *with detailed subthreshold current. (d) Symbol view considered in the paper, the polarity gate (PG) node is connected to both PG_S and PG_D.*

In order to simulate the PCT, we use a simple SiNWFET model, as described in [18]. This model is based on a parametric table extracted from TCAD simulations whose basic parameters were fitted on measured device characteristics [31]. Access resistances are estimated according to the device geometry. Each capacitance is extracted from TCAD simulations as an average value under all possible bias conditions. Instead of comparing the performances with advanced CMOS node, the model was calibrated on deeply scaled TCAD considering 25nm channel length SiNWFET [19].

Finally, these two models are used together and simulated using Eldo simulator [32]. As SiNWFET technology is based on a 25nm FinFET technology, we consider FinFET design rules for the layout considerations. On the other hand, as SiNWFET is an ultra-low leakage technology [31], thereby we consider a commercial 28nm FDSOI low power CMOS technology PDK from STMicroelectronics to enable an *apple-to-apple* comparison with CMOS.

III. Standard CMOS-Based RRAM Architecture

In this section, we provide an overview of the CMOS-based bipolar RRAM bitcells and we identify their limitations in terms of area and performances. We also discuss the reliability impact induced by the reset operation on the memory and periphery transistors.

First, it seems mandatory to justify the choice of keeping on logic transistors as selectors for eNVM while most of the community rushes for studies with fully BEoL bitcells or unconventional *Front End of Line* (FEoL) selectors. Extremely high transistor-less bitcell density architectures such as crosspoint/crossbar or Vertical RRAM (VRRAM) have been proposed but, as we demonstrated in [33], due to the high voltages required (3 to 6Volts), peripheral circuitry becomes area hungry and makes it not suitable for embedded memory replacement. On the other hand, extremely aggressive FEoL process, as used in [34], cannot be co-integrated with logic gates, requiring extremely process steps and thus making it not suitable for embedded memories. In this context, standard logic CMOS selectors are considered today by industrials as a viable solution for microcontrollers eNVM [23] [3].

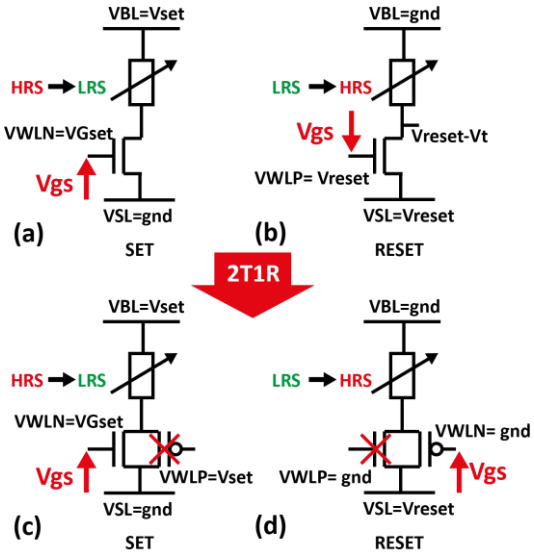

Figure 3 : Operation of a 1T1R (resp. 2T1R) OxRAM bitcell during set (a) (resp. (c)) and reset (b) (resp. (d)) operations. The gate-source voltage V_{gs} is highlighted. In a 1T1R structure, due to the bipolarities programming operations, the V_{gs} is not well controlled during the reset, while in a 2T1R structure, a PMOS transistor is used to overcome this issue.

Standard CMOS-based resistive memory architectures consist of the association of a MOS transistor (usually a *n*-type MOS transistor to maximize the area density w.r.t to a p-type MOS [35] which must be at least two times bigger for the same

drive) and a stacked BEoL RRAM that can fit in one of the first metal-to-metal vias or in a contact [36]. This standard 1T1R structure is presented in Figure 3. As presented in Section II, programming operations in the OxRAM technology are performed in opposite polarity. The *set* operation is carried out by applying a positive pulse to the top electrode. Once the OxRAM starts to switch from the HRS to the LRS, the current has to be limited to control the desired resistance value [17] [34]. The higher the programming current, the lower the obtained resistance value and variability. The *reset* operation is performed by applying a positive pulse to the bottom electrode, the current is controlled with the *reset* voltage (V_{reset}) (a current limitation is not needed during the *reset* operation because the resistance increases progressively, leading to a self-limitation) and the resistance switches to HRS. The obtained resistance depends on the applied *reset* voltage and the programing time [2].

Figure 3 presents the difference between 1T1R and 2T1R bitcells.

With a *n*-type transistor, the current is controlled during the *set* operation by direct control on the *Gate-Source* voltage. During the *reset* operation, to bring a sufficient V_{reset} across the selected OxRAM, the bottom electrode voltage of the ReRAM is slightly lower than $V_{reset} - V_T$ because the gate voltage is equal to V_{reset}. Compensating the V_T loss by increasing the gate polarity (gate overdrive) leads to increased complexity, reliability issues and more complex voltage management. In [6] [7] [8] [9], the *reset* gate voltage is raised between 2.4 up to 6V in order to perform a fast *reset*. The high voltages considered will cause stress in (i) the selected bitcell transistor, (ii) the neighbors bitcells selectors sharing the same BL and WL and in (iii) the near memory array periphery. Figure 3-a presents *set* operation in regards with the Vgs and Figure 3-b the *reset* operation with inverted Vgs.

To overcome this issue, a *p*-type transistor can be added to the 1T1R resulting to a 2T1R bitcell. In this topology, only the *n*-type transistor is used during the *set* operation (Figure 3-c) in order to control the current (the *p*-type transistor *gate-source* voltage is kept zero). During the *reset* operation (Figure 3-d), the *p*-type transistor is used (the *n*-type transistor V_{gs} cannot be controlled properly in reversed polarity). The *p*-type ensures that the *reset* voltage is applied across the OxRAM without V_T loss. To that, two WordLines (WL) are used (WLn and WLp) in order to control independently the *n* and the *p*-type transistors. Exploiting 2T1R architecture allows lower operation voltage during *reset* but increase the bitcell area as we show section VI. As a reference, in [37], a 4-Transistors (2 inverters) driver per bitcell is used to avoid V_T loss.

Several control signals are needed: The *Bit Line* (BL) connected to the RRAM, the *Word Line* (WL) connected to the MOS transistor gate and the *Source Line* (SL) connected to the MOS transistor source.

In order to compare the bitcells footprint, we designed the smallest possible layout in 28nm CMOS technology. Figure 4 shows the layout of 4-bit arrays of 1T1R (Figure 4-a) and 2T1R (Figure 4-b) with highlighted 1-bit footprint. To optimize the bit density, transistors sources are shared. The occupied area for 1-bit blocks that can be directly replicated is 0.031µm² ($12.4F^2$) for 1T1R bitcells. For 2T1R bitcells with minimum *p*-type transistor size enables 0.076um2 (30.3F2) and 0.1008µm² ($40.3F^2$ shown Figure 4-b) for double *p*-type transistor width. It is worth to note that an even denser 1T1R architecture featuring dummy transistors always off, instead of diffusion spacing, can be designed down to $12.1F^2$ per bit in 28nm technology (inspired from [38]). However, it may lead to huge static leakage during both programming and read operations, making it not suitable for eNVM.

In this section, we only focused on area considerations. Section IV describes its performances in *set* while Section VI details the performances of these bitcells in *reset* operation.

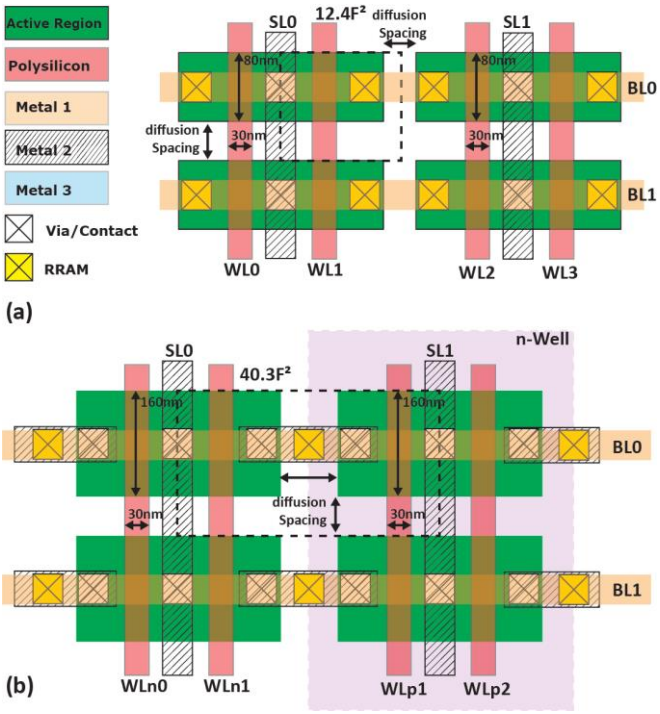

Figure 4: Layout of 2x2 bits (a) 1T1R and (b) 2T1R with double size p-type OxRAM cell array. MOS transistor sources are shared to reduce the bitcell area.

IV. PCT-Based OxRAM Architecture

In this section, we describe precisely the operation of PCT-based RRAM bitcells. Then, we present the physical implementation of a standard PCT-based RRAM bitcell that we name 1PCT1R and validate its functionality through electrical simulations.

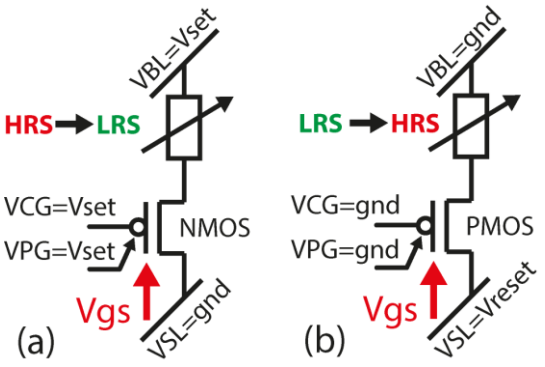

Figure 5 : Schematic of a 1PCT1R bitcell during (a) set and (b) reset operations. The control-gate voltage (CG) defines the polarity of the transistor. For set operation, a n-type MOS is enabled. For reset, a p-type MOS is enabled.

A. PCT-based OxRAM Operation

Beyond standard CMOS-based memory architectures, new bitcells using PCT transistors can be designed. Contrarily to CMOS-based bitcells, as described Figure 3 and Figure 5, these bitcells do not suffer from V_T loss during *reset* operation. Figure 5 presents the operation of a 1PCT1R structure. One additional signal is needed to control the PCT: The *Polarity Gate* (PG).

For *set* operation (as shown Figure 5-a), the PG voltage is put to high voltage to ensure *n*-type operation. Then, the CG voltage is raised to the *set* gate voltage (V_{Gset}) in order to limit the *set* current. During a *reset* operation (as shown Figure 5-b), the PG voltage is set to *Gnd* in order to ensure *p*-type operation. Then, the CG voltage is also set to *Gnd* to drive a *reset* operation with the *p*-type maximum current.

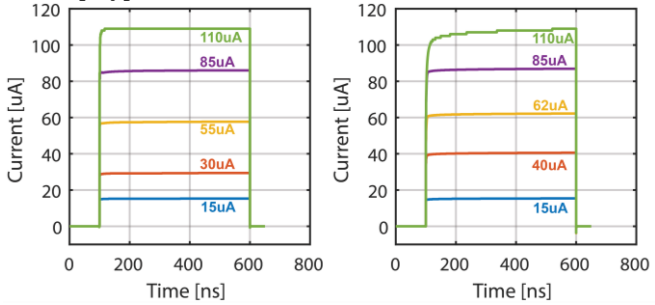

Figure 6 : Waveform of set pulses performed in (a) n-type PCT and in (b) p-type PCT.

Our PCT bitcells was simulated under two configurations: *(i)* with the *set* operation performed with the PCT in *n*-type. *(ii)* with the *set* operation performed with the PCT in *p*-type. We then performed several *set* operations and present the waveforms Figure 6. These waveforms show a uniformity between *n*-type and *p*-type set operation. In Figure 7, we show that the *set* current can be controlled as for standard CMOS-based bitcells. And that for a standard 6 nanowire PCT [15], current from few micro-amperes up to 100µA can be achieved without *gate overdrive*. Regarding the literature, we considered a 60µA programming current which is usually considered as a reliable programming current [6] [36] [34].

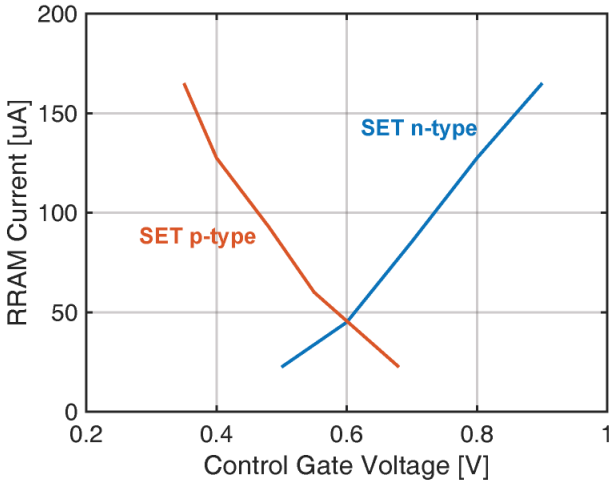

Figure 7 : Iprog-Vgs curve of set operation in PCT-based bitcells for n-type and p-type configurations.

Finally, Figure 8 presents a full *set-reset* programming cycle in 1PCT1R configuration showing a short 100ns set operation and a 22µs reset operation. We deliberately do not give too much details on the *reset* operation in this section, as it will be extensively explored and compared to CMOS bitcells in Section VI.

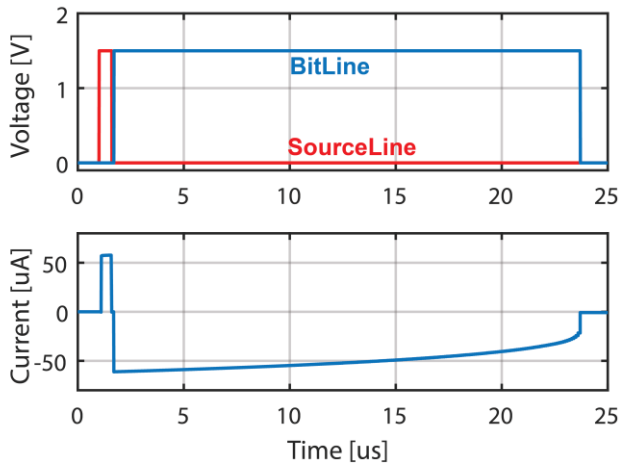

Figure 8: Set Reset cycle of a PCT-based bipolar RRAM bitcell.

B. Physical Implementation Description

Contrarily to [15], we keep a 4-terminal bitcell organization. This way, we provide a good control of the polarity gate voltage, making this architecture compatible with programming and *reading* scheme where some of the BL or SL are kept floating [36] (i.e., we ensure the transistor polarity independently of the array biasing). Finally, this 4-terminal bitcell ease the *reading* process and reduce its energy consumption, by enabling small BL/SL voltage difference (in the common BL/PG configuration from [15], low BL voltages leads to lower read margin or impossible read as then transistor state depends on the BL voltage). Finally, as a reference, 4

terminal bitcells-based memory architectures are common for NOR Flash [39] memories.

Figure 9 presents the layout schematic of the proposed 4-terminal 1PCT1R bitcell and of a 2×2 bit array of 1PCT-1R bitcells implemented in 25nm gate length SiNWFET technology [40]. A *Polarity Line* (PL) is used to bias the additional PGs. To optimize the density in 1PCT1R arrays, PLs are shared along the columns, as well as the PCT terminal connected to the SL. It ends to a 262nm by 245nm bitcell (0.064µm²) for a 25nm node.

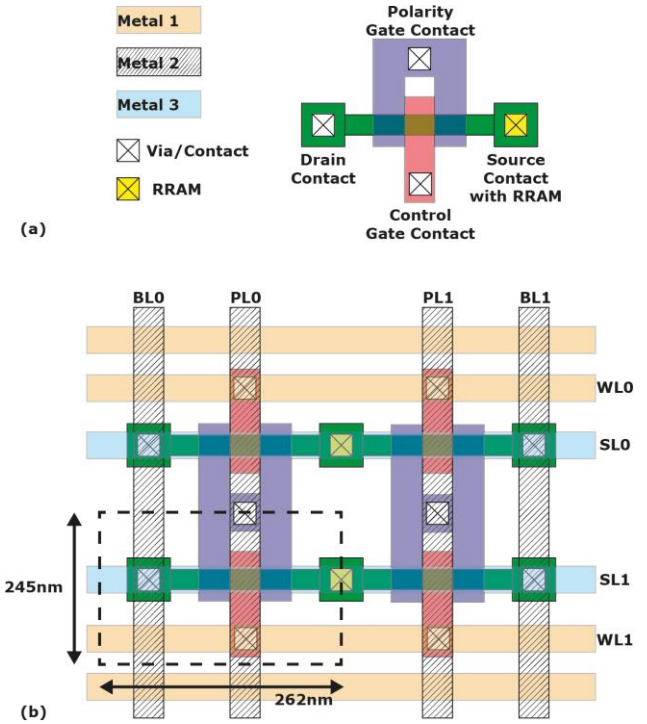

Figure 9 : (a) Layout of a single PCT SiNWFET transistor and detailed layers. (b) Layout of a 2x2 bits 1PCT1R cell array in a 25nm SiNWFET process. Transistors drains are shared to reduce the bitcell area.

C. Programming operations in PCT-based arrays

During the programming operations in 1PCT1R arrays, two main constraints must be considered: *(i)* the accessed bitcell has to be activated, *(ii)* the non-accessed bitcells has to be disabled to avoid parasitic write operations. While the PCT and OxRAM behaviors depend on the relative voltages between PL, SL, BL and WL terminals, the applied voltages can be either positive or negative. In the following, we consider only positive voltages. While the required current to ensure reliability and retention is relatively high (≈60µA), charge and discharge of the array metal lines energy cost was considered as a negligible cost in the programming energy considerations as is it pretty small compared to the memory programming current. In the following, we present the operation of a PCT-based array in *n*-type *set* configuration.

WLs, PLs, SLs and BLs are biased to ensure a *0 volts* V_{gs} or $V_{SL\text{-}BL}$ in the unselected bitcells while enabling the selected bitcell transistor. (1) During the *set* operation, all the PCTs are set in *n*-type (PL voltage at 1.2V), then, all the WLs, SLs and BLs are polarized at the *Gnd*. Then, the selected WL is put at V_{Gset} and the writing pulse (at *set* voltage) is applied on the selected BL. (2) *Read* operation is done using the same procedure. (3) During the *reset* operation, all the PCTs are set in *p*-type (PL voltage at *Gnd*) and the array WLs, BLs and SLs are biased at the *reset* voltage (V_{reset}). The selected WL is pulled down to *Gnd* and the writing pulse (from V_{reset} to *Gnd*) is applied on the selected BL. Table 1 summarizes the bias voltages used for set and reset operations for the selected and non-selected bitcells. In the memory array operations, all the PCT are set in the same polarity (all *n*-type for *set* and *read* operations and all *p*-type for the *reset* operation).

Table 1: Overview of the programming voltages and PCT type for set, reset and read operations.

	Set		**Reset**		**Read**	
Status	selected	Non-selected	selected	Non-selected	Selected	Non-selected
WL	V_{Gset}	0	0	V_{reset}	V_{Gread}	0
SL	0	0	V_{reset}	V_{reset}	0	0
BL	V_{set}	0	0	V_{reset}	V_{read}	0
PL	V_{set}	V_{set}	0	0	Vdd	Vdd
PCT Type	*n*-type	*n*-type	*p*-type	*p*-type	*n*-type	*n*-type

D. PCT-based OxRAM Functionnal Validation

Array simulations are presented in this section. Figure 10 shows a *Set-Read-Reset-Read* sequence in a 1PCT1R 2×2 array (Figure 9). In the presented sequence, each bit is programmed two times: First, a *set* operation is performed, then a *reset* operation is conducted. The bitcells sharing the SL, WL or BL with the accessed one, either see a *0 Volts* V_{gs} either a *0 Volts* BL-SL voltage difference. Thereby, *set* and *reset* operations are achieved without parasitic write in non-accessed bitcells. On the other hand, the *p*-type configuration *set* can be performed as a *reset* operation from Figure 10, as for this configuration, the RRAM is reversed.

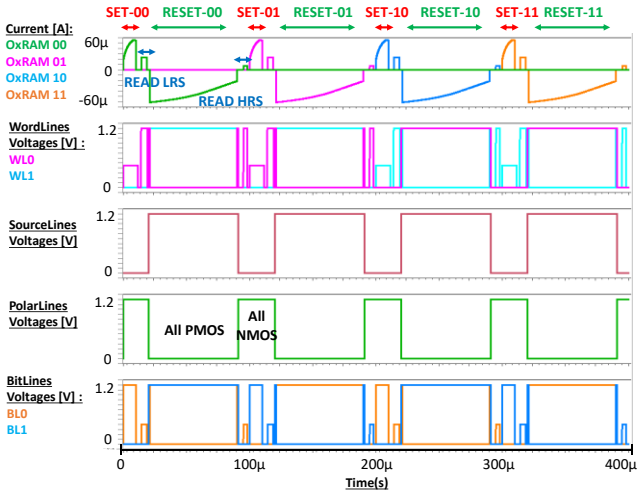

Figure 10: Waveforms of set and reset operations in a 1PCT1R bitcell 2x2 array. WL, PL, BL voltages and OxRAM current are shown. The immunity to programming disturb in non-selected bitcells is ensured.

V. PCT-BASED OXRAM 1XPCT1R ARCHITECTURE

In this section, we present first, an innovative bitcell enabling a better density than the previously presented 1PCT1R bitcell. Then, we validate its functionality and propose an innovative array organization.

A. PCT-based 1XPCT1R Physical Implementation

Thanks to the memories array structure regularity, a higher flexibility is allowed with the design rules compared to standard logic physical design rules. In this section, we take the assumption that gates can be arranged in both vertical and horizontal directions as long as a high level of regularity is ensured (as a reference, the same consideration is taken in SRAM design to increase the contacts and active density). Thereby, we propose an innovating bitcell, using PCT transistors organized in a cross shape. The cross-shaped 1PCT1R bitcell (1XPCT1R) is validated through physical layout feasibility study and electrical simulations.

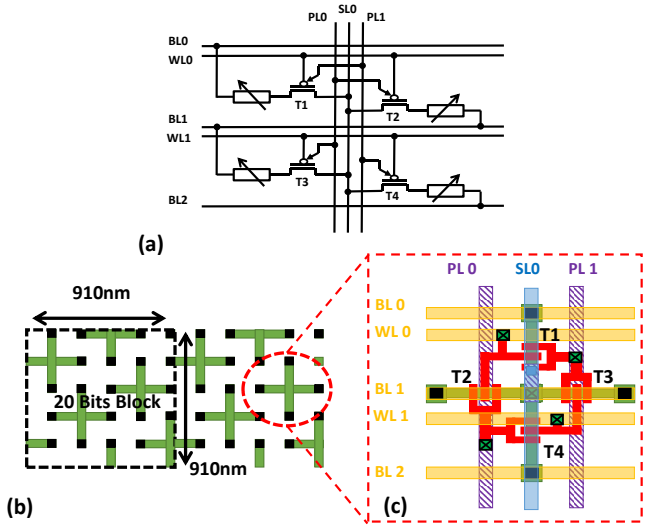

Figure 11: (a) Schematic of a 2×2 bits 1XPCT1R cell array. (b) Physical description of a 20-bits cell array and (c) a detailed layout of a 2×2 bits 1XPCT1R cell array. 1XPCT1R bitcell is constituted of 4 PCTs with common drain. Equivalent bit density is almost 2 times higher than for 1PCT1R bitcell.

Figure 11-a presents the 1XPCT1R schematic diagram. Four 1PCT1R bitcells are organized in cross-shape with common transistor source. The transistors T1 and T2 (resp. T3 and T4) CGs are connected together to the WL0 (resp. WL1). T2 and T4 (resp. T1 and T3) PGs are in common and connected to the PL0 (resp. PL1). T2 and T3 OxRAMs are connected to the BL1 while T1 OxRAM is connected to BL0 and T4 OxRAM to BL2. In Figure 11-b the layout array organization is shown, the 1XPCT1R is a cross-shaped bitcell. Each cross's arm supports a PCT (green) and an OxRAM memory (black squares). The minimum size replicable block is a 20 bits block in a 0.828µm² square. It leads to a 0.041µm² per bit (35% smaller than the standard 1PCT1R area 0.064µm²) for a 25nm physical rules PCT technology node. Figure 11-c presents the detailed physical layout of a 4 bit 1XPCT1R block. The common SL is drawn using a *metal 3* vertical wire. Connection between the SL and the transistors common source is performed through a *metal 1* wire used to shift the contact over T1 transistor. Thereby, BLs (resp. WLs) are drawn using *metal 2* horizontal lines and are connected to the OxRAMs (resp. CGs). Each transistor *drain* supports an OxRAM.

This 1XPCT1R array organization needs specific array border bitcells. Some bits have to be sacrificed in the border. To make all the BLs, WLs, SLs and PLs accessible, the border cross are cut and some bits are not connected as presented Figure 12. The uncompleted cross containing no common SLs are sacrificed. It represents one bit among six for the first and last BLs and SLs. To ease the addressing, first and last BL and SL can be not addressed. Additionally, this array organization features a lower density contact per array lines, requiring more lines, and thus reducing the parasitic capacitance on the WLs, SLs, PLs, and BLs and thus the energy consumption during *read* operation as shown section VI-b.

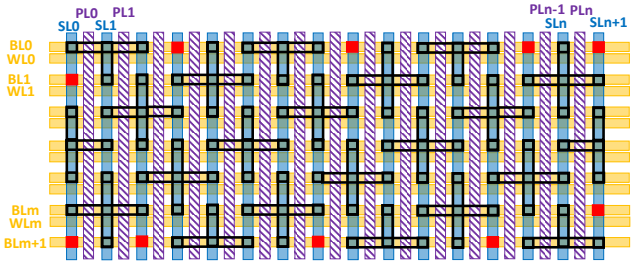

Figure 12: Array of 1XPCT1R bitcells with detailed WL, BL, SL and PL. Border bitcells are detailed: unconnected OxRAMs are highlighted in red and uncompleted cross are cut.

B. 1XPCT1R Bitcell Functionnal Validation

As before, the programming operations are considered as relative voltages differences and can be operated relatively to the *gnd*. *Set* operation is done by considering all the PCT in *n*-type. First all the SL, BL, WL are put at *gnd*. In a second time, the selected WL is biased to V_{Gset} and the writing pulse is applied on the selected BL. During *reset* operation, all the PCT are put in *p*-type (PL voltage at g*nd*) and the array WLs, BLs and SLs are polarized at the *reset* voltage (V_{reset}). Then the selected WL is pulled down to *gnd* and the writing pulse (from V_{reset} to *gnd*) is applied on the selected BL. As for the 1PCT1R, *p*-type configuration *set* operation is simply performed by reversing the bitcell and so the *set*/*reset* configurations.

Due to its non-standard array organization, several scenarios are possible: (a) two bicells with common WL, (b) common PL, common WL and SL, (c) common BL and SL, (d) common PL and SL, (e) and common BL. When a non-selected bitcell is sharing common array lines with a selected bitcell, immunity to write disturb has to be demonstrated. Shared WL, SL and BL are standard non selected bitcells cases (as shown Figure 10). Shared PL is not critical for 1XPCT1R because all the PLs have the same polarization during programing or read operations. Figure 13 presents the disturb immunity for common WL and SL and for common BL and SL. During both *reset* and *set* operations, the write disturb is avoided by the WL, SL, BL and PL voltages.

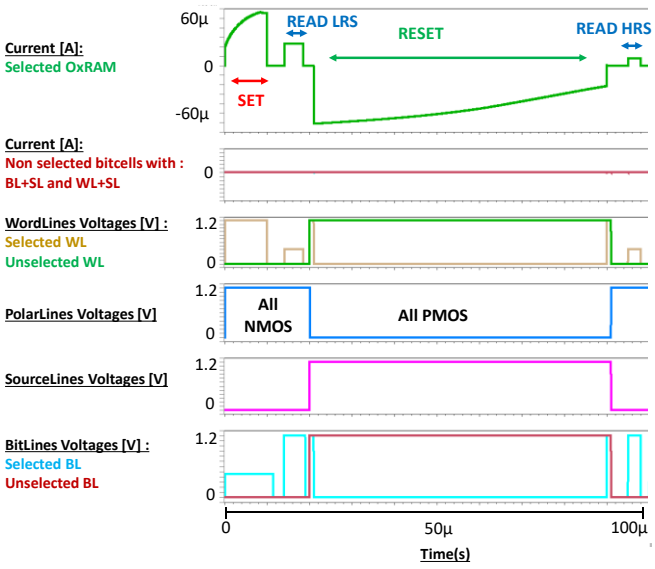

Figure 13: Waveforms of *set* and *reset* operations for 1XPCT1R bitcell array. For each operation on, immunity on unselected bitcells that share WL, SL or BL with selected one is ensured.

VI. Performances Analysis

In this section, we propose to explore the performances offered by PCT-based bitcells in three cases. *(i)* During the *set* operation and show that PCT-based bitcell provide the same performances than MOS-based bitcells. *(ii)* During the *reset* operation and show that PCT-based bitcells solves the gate overdrive issue identified in standard CMOS-based bitcells while adding a limited area overhead. *(iii)* During the *read* operation and show that thanks to its lower density contacts per array lines, the 1XPCT1R array enables faster operations than standard CMOS bitcells.

A. Performances in Set Operation

Figure 14 shows the evolution of the set time of PCT and MOS bitcells versus the BL-SL voltage difference. In that case, as the MOS transistors of the considered PDK have do not have exactly the same electrical behavior than the PCT, we tuned their gate voltage to achieve a 60µA programming voltage (0.6V for a 6 nanowire PCT and 0.9 for a W=80nm n-type transistor MOS bitcell). This way, we demonstrate that the using the proposed PCT-based bitcells do not degrade the performances compared to CMOS-based bitcells.

B. Performances in Reset Operation

We consider CMOS-based 1T1R and 2T1R bitcells and compare it with the PCT-based bitcells proposed in this paper. The 1T1R bitcell is based on a minimum size *n*-type MOS selector (W=80nm). Three different 2T1R bitcells are considered: *(i)* minimum size *p*-type, *(ii)* 120nm width *p*-type and *(iii)* 160nm width *p*-type. For layout regularity, we size the *n*-type selector with the same width. During the *set* operation, we underdrive its gate to keep a 60µA I_{prog}. The layout for configuration *(iii)* and for the 1T1R configuration are shown Figure 4. While configuration *(iii)* occupies a 40.3F^2 area, configuration *(ii)* area is 33.6F^2. Finally, minimum size configuration *(i)* enables at max a 30.3F^2 area (0.0756um^2) for 2T1R bitcells.

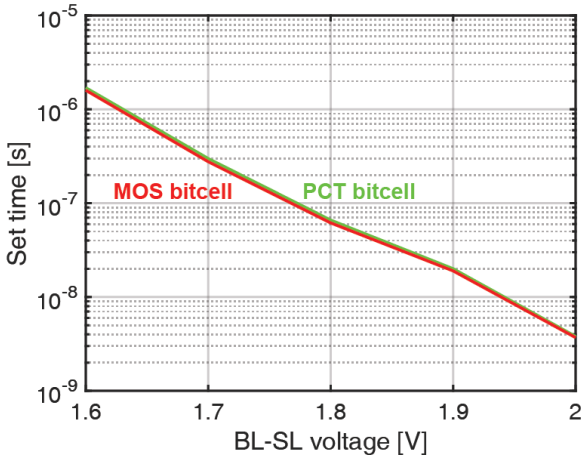

Figure 14: Set time versus BL-SL voltage difference for minimum size 1T1R MOS bitcell (red) and PCT-based bitcell (blue).

For all the 1T1R, 2T1R and 1PCT1R bitcells, we performed *reset* operations with various WL, BL and SL voltages. The reset time is defined as the time required for the RRAM resistance value to achieve a HRS/LRS ratio of 10. We show the *reset* time evolution in Figure 15. As expected, the 1T1R bitcell requires a huge gate overdrive to perform sub-100µsec *reset* time. As a reference, 1T1R bitcells demonstrated in the literature require more from 3 to 5V to enable sub-100ns *reset* operations [6] [7] [8].

Figure 15 presents the evolution of the programming time of the previously mentioned bitcells. In red, the 1T1R bitcell with gate overdrive from 1.7V up to 2V shows poor *reset* performances while causing high voltage stress on the transistor. On the other hand, 2T1R bitcells (in blue) show better *reset* performances and better transistor reliability at the cost of a bigger bitcells (more than 30.3F^2). Finally, the proposed PCT-based bitcells are represented in green. Standard 1PCT bitcell performing the *set* in *n*-type and the *reset* in *p*-type exhibit performances equivalent to 2T1R bitcells while providing area reduction from 1.35× (25F^2 vs 33.6F^2) up to 2.6× (16F^2 vs 40.3F^2) per bitcells depending on the PCT bitcells and 2T1R sizing. Compared to 1T1R with 2V gate overdrive, the proposed bitcell enables 75× *reset* time reduction for a 2.2V SL-BL voltage. Compared to 33.6F^2 2T1R bitcell, it enables from 5× (at SL-BL=1.8V) up to 105× (at SL-BL=2.2V). Finally, the *p*-type *set* operation enables a 500× *reset* time improvement at constant bitcell size compared to standard PCT bitcell. This performance improvement can be enabled by reversing the RRAM stack (which is usually fabricated with top electrode last). It is important to note that equivalent gains could be enabled by 2T1R reversed bitcells. However, it would not bring any gains compared to PCT bitcells, as the minimum 2T1R bitcell area is bigger than the PCT bitcells.

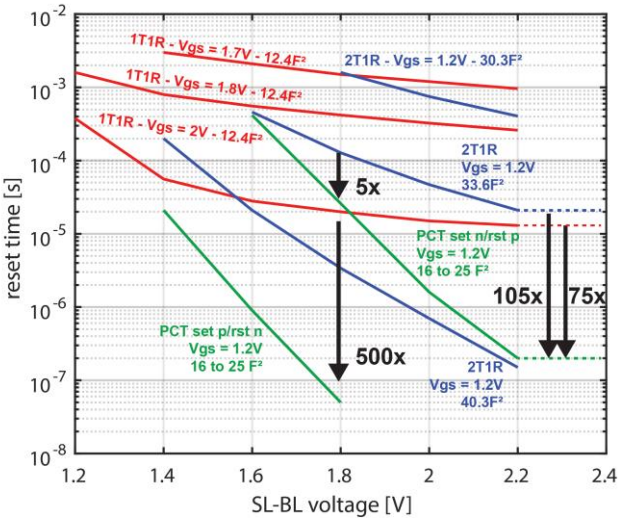

Figure 15: Reset time versus SL-BL voltage difference for CMOS 1T1R bitcell (red) and various gate overdrive voltages (from 1.7 to 2V), CMOS 2T1R bitcells (blue) with various p-type transistor size (from 80nm up to 160nm width) and PCT-based bitcells (green) for n-type and p-type reset.

Figure 17 presents the consumed energy during a 1.8V SL-BL voltage *reset* operation for all the bitcells under study. Extraction of the programming energy shows that, as expected regarding Figure 15, PCT-based bitcells perform with performances equivalent bigger CMOS-based 2T1R bitcells (from 33.6F^2 to 40.3F^2). On the other hand, equivalent *reset* energy (1 to 10nJ) cannot be achieved with 1T1R bitcells without a strong *gate overdrive* higher than 2V (we neglect here the energy consumed by the high voltage generation). However, the use of high voltages induces stress on the selected bitcell gate oxide as well as on the bitcells sharing the WL, and thus strongly reduces the transistor lifetime [41] (i.e., the memory reliability).

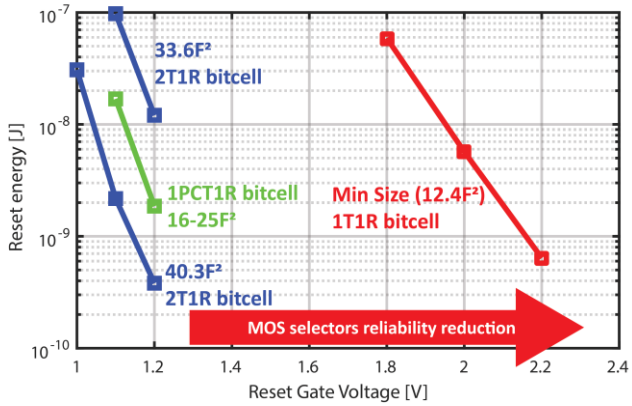

Figure 17: Energy consumed during reset operations for various bitcell architectures versus the required programming voltage. 1T1R bitcell requires an increase of the programming voltage (red) inducing a reduction of the MOS transistor reliability. PCT bitcells (green) enable 2T1R (green) operation voltages without overdrive while using a single PCT transistor per OxRAM bitcell.

C. *Performances in Read Operation*

In this subsection, we explore the performances in *read* operation of the proposed bitcells and we compare it to standard CMOS-based 1T1R and 2T1R bitcells.

Even though the device area is bigger than a CMOS-based 1T1R bitcell, the array organization of 1XPCT1R architecture relies on considering more BLs and thus reducing of a 4/5 ratio the BL contact capacitance as well as the WL gate contact capacitance. While the overall energy consumption of a *read* operation is slightly increased as more SL, BL, WL and PL are accessed as shown Table 2, the BL discharge time is improved of 12% for a 65kb array while the 1XPCT1R bitcell is 32% bigger than a CMOS 1T1R bitcell.

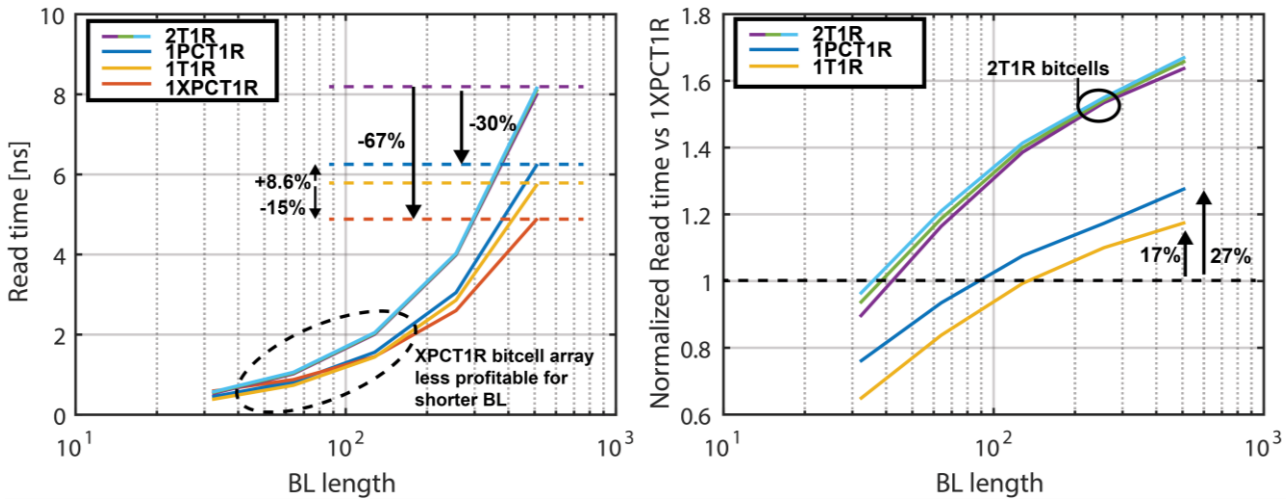

Figure 16: (a) Read time versus BL length for a 512 Bitcells long SL for CMOS and PCT bitcells. (b) Normalized read time versus 1XPCT1R bitcell array.

Table 3 : Summary of the proposed bitcells performances

Bitcell Type	1T1R	2T1R	1PCT1R	1XPCT1R
1-bit area	0.031µm²	0.075-0.1008µm²	0.064µm²	0.041µm²
	12.4F²	30.3-40.3F²	25.67F²	16.4F²
Sub 20µs *Reset* Gate Voltage	>2V	1.2V	1.2V	1.2V
Reset Time 1.8V BL/SL voltage Vg=1.2V (except 1T1R)	2ms@Vg=1.7V 400µs@Vg=1.8V 20us@Vg=2V	1.5ms@30.3F² 100µs@33.6F² 4us@40.3F²	25µs@*n*-type *set*/*p*-type *reset* 50ns@*p*-type *set*/*n*-type *reset*	
Read Time 512×512 array	5.76ns	8.03ns@30.3F² 8.19ns@40.3F²	6.26ns	4.90ns

Table 2 : number of BLs for standard arrays (1T1R, 1PCT1R) and for 1XPCT1R array.

Array size	Array BL and SL	
	1PCT1R	1XPCT1R
256bits	16	18
1kbits	32	36
4kbits	64	72
16kbits	128	144
65kbits	256	287
262kbit	512	574

Thereby, we simulated the CMOS-based and PCT-based arrays during *read* operations in various memory array sizes. The considered architecture features a BL precharge to a *read* voltage and thus, an activation of the WL, leading to a BL discharge through the selected bitcell. As a 60µA programming current gives a 20kΩ R_{LRS} value, we take it as a reference for the *read* operations, and simulate the BL discharge through the selected bitcell while taking into account the WL charging time and the BL discharge time. Figure 16-a shows the evolution of the *read* time versus the BL length for a 512 SL long memory array, for CMOS and PCT-based bitcells, while Figure 16-b shows the ratio between the 1XPCT1R bitcell and the others bitcells. For 512 long BL, 1XPCT1R shows 67% and 15% of gain compared to CMOS 2T1R and 1T1R bitcells respectively. On the other hand, standard 1PCT1R bitcells enables 30% gain versus 2T1R and only 8.6% performance degradation compared to 1T1R. Finally, 1XPCT1R enables 17% and 27% of performances improvements compared to 1T1R and 1PCT1R respectively.

While the PCT gate capacitance is higher than the CMOS gate capacitance, the WL charging time is higher in PCT-based arrays. However, compared to BL discharge through the 20k R_{LRS}, it represents less than 3% (respectively 1%) for a 256×256 PCT (respectively 1T1R) array and 6% (respectively 2%) for a 512×512 array.

For non-square arrays, if the PL or SL is longer than the BL, after a certain point, the PL/SL charging time may be longer than the BL discharge time, limiting the 1XPCT1R array *read* operation speed. As the PL is connected to 2 polarity gates while the SL is connected to 1 single transistor drain, PL parasitic capacitance is higher. In this context, PL charging time will limit the *read* speed when a *read* is performed right after a *reset* operation (cf. Figure 13). As the WL and the BL are in the same direction in 1XPCT1R bitcell, a longer WL charge also correspond to a longer BL discharge, reducing the impact of the WL charge over the *read* performances and keeping its effect low as introduced for squared arrays.

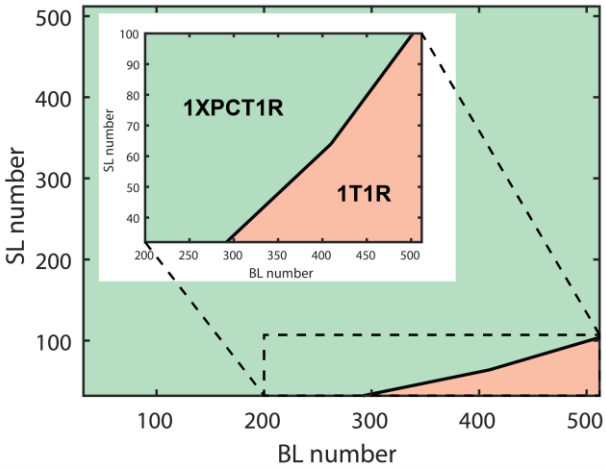

Figure 18: 1XPCT1R over 1T1R read time ratio versus array size (BLs and SLs). Except for extremely wide array, 1PCT1R arrays are more profitable than CMOS-based ones.

Figure 18 shows the evolution of the read time ratio between CMOS 1T1R and 1XPCT1R bitcells array versus the array size (BLs and SLs). The green zone corresponds to 1XPCT1R while the red one to CMOS 1T1R more profitable zone. It appears that the only case where 1T1R is more profitable than 1XPCT1R in terms of performances occurs for extremely wide and thin arrays (more than 300 BLs and less than 100 SLs).

Finally, Table 3 summarizes the area, programming time, read time and programming voltages considered for all the bitcells under study in this work.

VII. Conclusion

In this work we explored the opportunities opened by *Polarity Controllable Transistors* (PCT) in order to enhance the operation of bipolar RRAM memories arrays for eNVM applications. We show that standard CMOS-based memory arrays require a strong gate overdrive (>2V) or a huge bitcell (3×) to perform sub microsecond *reset* operation. In this context

we proposed two innovative 1T1R-like bitcell using PCT and enabling fast *reset* while providing dense organization ($16.4F^2$ to $25.76F^2$ bitcell area). We simulated the proposed bitcells with SiNWFET PCT and OxRAM RRAM technology compact models and compared it with a low power 28nm CMOS FDSOI technology. We demonstrate that PCT-based bitcells enable sub-30µs *reset* without gate overdrive and while keeping a dense bitcell (up to 75× versus 2V overdriven 1T1R and from 5× to 105× versus 2T1R). We also showed that these bitcells can be used with an innovative writing scheme to perform *p*-type *set* operation and *n*-type *reset* operation, and that this scheme enables 500× of *reset* time reduction (50ns) compared to standard *p*-type *reset* operation. Finally, we compared the performances of the proposed bitcells during a *read* operation, and showed that while the 1XPCT1R bitcell is 30% bigger than a 1T1R, its lower contact density enables a smaller parasitic capacitance and thus up to 15% (respectively 67%) faster read operations than 1T1R (respectively 2T1R).

Overall, with this study we show that it exists a tradeoff between density and performances in RRAM memory arrays. Co-integrating PCT technologies (instead of CMOS) with any emerging RRAM technology could enable better performances than CMOS while keeping the density high.

ACKNOWLEDGMENT

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VIII. REFERENCES

[1] C. H. Jan, U. Bhattacharya, R. Brain, S. J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P.Vandervoorn, L. Yang, J. Y. Yeh and P. Bai, "A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications," *IEEE International Electron Devices Meeting Technical Digest. (IEDM Tech. Dig.)*, 2012.

[2] E. Vianello, O. Thomas, M. Harrand, S. Onkaraiah, T. Cabout, B. Traoré, T. Diokh, H. Oucheikh, L. Perniola, G. Molas, P. Blaise, J. F. Nodin, E. Jalaguier and B. D. Salvo, "Back-end 3D integration of HfO2-based RRAMs for low-voltage advanced IC digital design," *IEEE International Conference on IC Design & Technology (ICICDT)*, 2013.

[3] A. Kawahara, K. Kawai, Y. Ikeda, Y. Katoh, R. Azuma, Y. Yoshimoto, K. Tanabe, Z. Wei, T. Ninomiya, K. Katayama, R. Yasuhara, S. Muraoka, A. Himeno, N. Yoshikawa, H. Murase, . K. Shimakawa, . T. Takagi, . T. Mikawa and . K. Aono, "Filament scaling forming technique and level-verify-write scheme with endurance over 107 cycles in ReRAM," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2013.

[4] K. Kawai, A. Kawahara, R. Yasuhara, S. Muraoka, Z. Wei, R. Azuma, K. Tanabe and K. Shimakawa, "Highly-reliable TaOx reram technology using automatic forming circuit," *IEEE International Conference on IC Design & Technology (ICICDT)*, 2014.

[5] J.-M. Portal, M. Bocquet, S. Onkaraiah, M. Moreau, H. Aziza, D. Deleruyelle, K. Torki, E. Vianello, A. Levisse, B. Giraud, O. Thomas and F. Clermidy, "Design and Simulation of a 128 kb Embedded Nonvolatile Memory Based on a Hybrid RRAM (HfO2)/28 nm FDSOI CMOS Technology," *IEEE Transactions on Nanotechnology (TNANO)*, 2017.

[6] A. Grossi, E. Vianello, C. Zambelli, P. Royer, J.-P. Noel, B. Giraud, L. Perniola, P. Olivo and E. Nowak, "Experimental Investigation of 4-kb RRAM Arrays Programming Conditions Suitable for TCAM," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, 2018.

[7] Y. Y. Chen, B. Govoreanu, L. Goux, R. Degraeve, A. Fantini, G. S. Kar, D. J. Wouters, G. Groeseneken, J. A. Kittl, M. Jurczak and L. Altimime, "Balancing SET/RESET Pulse for > 1010 Endurance in HfO2/Hf 1T1R Bipolar RRAM," *IEEE Transactions on Electron Devices (TED)*, 2012.

[8] J. Yi, H. Choi, S. Song, D. Son, S. Lee, J. Park, W. Kim, M. Sung, S. Lee, J. Moon, C. Kim, J. Park, M. Joo, J. Roh, S. Park, S.-W. Chung, J. Jeong, S.-J. Hong and S.-W. Park, "Requirements of bipolar switching ReRAM for 1T1R type high density memory array," *IEEE International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, 2011.

[9] C.-C. Chou, Z.-J. Lin, P.-L. Tseng, C.-F. Li, C.-Y. Chang, W.-C. Chen, Y.-D. Chih and T.-Y. J. Chang, "An N40 256K×44 Embedded RRAM Macro with SL-Precharge SA and Low-Voltage Current Limiter to Improve Read and Write Performance," *IEEE International Solid State Circuits Conference (ISSCC)*, 2018.

[10] J. Zhang, M. D. Marchi, P.-E. Gaillardon and G. D. Micheli, "A Schottky-barrier silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 decades of current," *IEEE International Electron Devices Meeting (IEDM)*, 2014.

[11] L. Arnani, P.-E. Gaillardon and G. D. Micheli, "Efficient arithmetic logic gates using double-gate silicon nanowire FETs," *IEEE International New Circuits and Systems Conference (NEWCAS)*, 2013 .

[12] P.-E. Gaillardon, R. Magni, L. Amarú, M. Hasan, R. Walker, B. S. Rodriguez, J.-F. Christmann and E. Beigné, "Three-Independent-Gate Transistors: Opportunities in digital, analog and RF applications," *IEEE Latin-American Test Symposium (LATS)*, 2016 .

[13] X. Tang, J. Zhang, P. Gaillardon and G. D. Micheli, "TSPC Flip-Flop circuit design with three-independent-gate silicon nanowire FETs," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014.

[14] S. Bobba, P.-E. Gaillardon, J. Zhang, M. D. Marchi, D. Sacchetto, Y. Leblebici and G. D. Micheli, "Process/design co-optimization of regular logic tiles for double-gate silicon nanowire transistors," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2012.

[15] K. Shamsi, Y. Bi, Y. Jin, P.-E. Gaillardon, M. Niemier and X. S. Hu, "Reliable and High Performance STT-MRAM Architectures based on Controllable-Polarity Devices," *IEEE International Conference on Computer Design (ICCD)*, 2015.

[16] M. Bocquet, D. Deleruyelle, H. Aziza, C. Muller, J.-M. Portal, T. Cabout and E. Jalaguier, "Robust compact model for bipolar oxide-based resistive switching memories," *IEEE Transactions on Electron Devices (TED)*, 2014.

[17] E. Vianello, O. Thomas, G. Molas, O. Turkyilmaz, N. Jovanović, D. Garbin, G. Palma, M. Alayan, C. Nguyen, J. Coignus, B. Giraud, T. Benoist, M. Reyboz, A. Toffoli, C. Charpin, F. Clermidy and L. Perniola, "Resistive Memories for Ultra-Low-Power embedded computing design," *IEEE International Electron Devices Meeting (IEDM)*, 2014.

[18] J. Zhang, X. Tang, P.-E. Gaillardon and G. D. Micheli, "Configurable Circuits Featuring Dual-Threshold-Voltage Design With Three-Independent-Gate Silicon Nanowire FETs," *IEEE Transactions on Circuits and Systems (TCAS)*, 2014.

[19] H. G. Mohammadi, P.-E. Gaillardon and G. D. Micheli, "From Defect Analysis to Gate-Level Fault Modeling," *IEEE Transactions on Nanotechnology (TNANO)*, 2015.

[20] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen and a. M.-J. Tsai, "Metal-Oxide RRAM," *Proceedings of the IEEE*, 2012.

[21] D. Apalkov, B. Dieny and J. M. Slaughter, "Magnetoresistive Random Access Memory," *Proceedings of the IEEE*, 2016.

[22] H. -S. P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi and K. E. Goodson, "Phase Change Memory," *Proceedings of the IEEE*, 2010.

[23] "ReRAM embedded Super low-power consumption MCU MN101L," [Online]. Available: https://industrial.panasonic.com/ww/products/semiconductors/microcomputers/mn101l.

[24] S. U. Sharath, T. Bertaud, J. Kurian, E. Hildebrandt, C. Walczyk, P. Calka, P. Zaumseil, M. Sowinska, D. Walczyk, A. Gloskovskii, T. Schroeder and L. Alff, "Towards forming-free resistive switching in oxygen engineered HfO2−x," *Applied Physics Letters*, 2014.

[25] N. Jovanović, O. Thomas, E. Vianello, J.-M. Portal, B. Nikolić and L. Naviner, "OxRAM-based non volatile flip-flop in 28nm FDSOI," *IEEE International New Circuits and Systems Conference (NEWCAS)*, 2012.

[26] M. D. Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici and G. D. Micheli, "Polarity Control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs," *International Electron Devices Meeting*, 2012.

[27] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick and W. M. Weber, "Reconfigurable Silicon Nanowire Transistors," *NanoLetters*, 2012.

[28] Y.-M. Lin, J. Appenzeller, J. Knoch and P. Avouris, "High-performance carbon nanotube field-effect transistor with tunable Polarities," *IEEE Transactions on Nanotechnology (TNANO)*, 2005.

[29] S. Nakaharai, T. Iijima, S. Ogawa, S.-L. Li, K. Tsukagoshi, S. Sato and N. Yokoyama, "Electrostatically Reversible Polarity of Dual-Gated Graphene Transistors," *IEEE Transactions on Nanotechnology (TNANO)*, 2014.

[30] G. V. Resta, S. Sutar, Y. Balaji, D. Lin, P. Raghavan, I. Radu, F. Catthoor, A. Thean, P.-E. Gaillardon and G. d. Micheli, "Polarity control in WSe2 double-gate transistors," *Nature Scientific Report*, 2016.

[31] M. D. Marchi, D. Sacchetto, J. Zhang, S. Frache, P.-E. Gaillardon, Y. Leblebici and G. D. Micheli, "Top–Down Fabrication of Gate-All-Around Vertically Stacked Silicon Nanowire FETs With Controllable Polarity," *IEEE Transactions on Nanotechnology*, 2014.

[32] "Mentor Graphics Website," [Online]. Available: https://www.mentor.com/.

[33] A. Levisse, p. Royer, B. Giraud, J. P. Noel, M. Moreau and J. M. Portal, "Architecture, Design and Technology Guidelines for Crosspoint Memories," *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2017.

[34] J. Zahurak, K. Miyata, M. Fischer, M. Balakrishnan, S. Chhajed, D. Wells, H. Li, A. Torsi, J. Lim, M. Korber, K. Nakazawa, S. Mayuzumi, M. Honda, S. Sills, S. Yasuda, A. Calderoni, B. Cook, . G. Damarla, . H. Tran, B. Wang, C. Cardon, . K. Karda, J. Okuno, . A. Johnson, . T. Kunihiro, J. Sumino, . M. Tsukamoto, . K. Aratani, . N. Ramaswamy, . W. Otsuka and . K. Prall, "Process Integration of a 27nm, 16Gb Cu ReRAM," *IEEE International Electron Devices Meeting (IEDM)*, 2014.

[35] M. Nabavi, F. Ramezankhani and M. Shams, "Optimum pMOS-to-nMOS Width Ratio for Efficient Subthreshold CMOS Circuits," *IEEE Transactions on Electron Devices (TED)*, 2016.

[36] W. C. Shen, C. Y. Mei, Y. -D. Chih, S.-S. Sheu, M.-J. Tsai, Y.-C. King and C. J. Lin, "High-K metal gate contact RRAM (CRRAM) in pure 28nm CMOS logic process," *IEEE International Electron Devices Meeting (IEDM)*, 2012.

[37] X. Tang, E. Giacomin, G. D. Micheli and P.-E. Gaillardon, "Physical Design Considerations of One-level RRAM-based Routing Multiplexers," *ACM International Symposium on Physical Design*, 2017 .

[38] R. Takemura, T. Kawahara, K. Miura, H. Yamamoto, J. Hayakawa, N. Matsuzaki, K. Ono, M. Yamanouchi, K. Ito, H. Takahashi, S. Ikeda, H. Hasegawa, H. Matsuoka and H. Ohno, "A 32-Mb SPRAM With 2T1R Memory Cell, Localized Bi-Directional Write Driver and `1'/`0' Dual-Array Equalized Reference Scheme," *IEEE Journal of Solid-State Circuits (JSSC)*, 2010.

[39] N. Do, "Scaling of split-gate flash memory and its adoption in modern embedded non-volatile applications," *IEEE International Conference on IC Design and Technology (ICICDT)*, 2016.

[40] O. Zografos, P.-E. Gaillardon and G. D. Micheli, "Novel grid-based power routing scheme for regular controllable-polarity FET arrangements," *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014.

[41] X. Federspiel, D. Angot, M. Rafik, F. Cacho, A. Bajolet, N. Planes, D. Roy, M. Haond and F. Arnaud, " 28nm node bulk vs FDSOI reliability comparison," *IEEE International Reliability Physics Symposium (IRPS)*, 2012.

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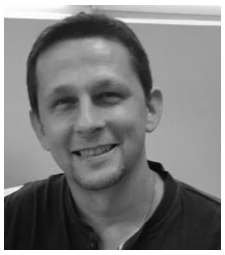

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