Multi-Channel Tri-gate GaN Power Schottky Diodes with Low ON-Resistance

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***Abstract*— In this work we demonstrate high-performance lateral GaN power Schottky barrier diodes (SBDs) based on a novel multi-channel tri-gate architecture. A significant reduction in ON-resistance (R_{ON}) of 50%, down to 7.2 ± 0.4 Ω·mm, along with a much smaller forward voltage (V_F) of 1.57 ± 0.06 V, were achieved with multiple 2DEG channels (multi-channels) formed by periodic AlGaN/GaN heterostructures. We used a tri-anode structure to form Schottky contact to the multi-channels through the fin sidewalls, leading to a small turn-ON voltage (V_{ON}) of 0.67 ± 0.04 V. To simultaneously control the multi-channels and effectively spread the electric field in OFF state, a tri-gate structure was integrated in the anode, resulting in an ultra-low leakage current (I_R) of ~1 nA/mm at -600 V and a high breakdown voltage (V_{BR}) of -900 V at 1 μA/mm with grounded substrate. In addition, the devices presented promising switching performance, due to the small product of R_{ON} and reverse charge (Q), thanks to the optimized tri-gate geometry, and the high effective mobility (μ_e) of 2063 ± 123 cm^2·V^{-1}s^{-1} despite the small fin width (w) of 50 nm. Our approach combines in a unique way the excellent electrostatic control of the tri-gate structure with the high conductivity of multi-channels, offering a promising platform for future advances in GaN power devices.**

***Index Terms*—GaN, SBD, multi-channel, tri-gate, tri-anode, breakdown, leakage current.**

I. INTRODUCTION

GaN-on-Si SBDs are promising as power rectifiers [1]-[10], offering high performance at a competitive cost, and can be integrated with GaN transistors to form advanced integrated power devices [11]-[14] and circuits [15]-[18]. However, a major challenge is to achieve high reverse-blocking capabilities along with low forward-conduction losses, which is an intrinsic trade-off that limits many other types of power devices.

In this work we present novel multi-channel tri-gate SBDs to address this challenge (Fig. 1). We employed periodic AlGaN/GaN heterostructures with multiple 2DEG channels [19]-[22] to reduce the R_{ON} and V_F. 3D tri-anode and tri-gate electrodes were implemented to contact and control the multi-channels, resulting in small V_{ON}, low I_R, and high V_{BR}. This unique design significantly enhanced the device performance, leading to state-of-the-art lateral GaN-on-Si power SBDs, and unveiled a novel platform to drastically improve the efficiency, increase the current rating, and reduce the size of GaN-based power devices.

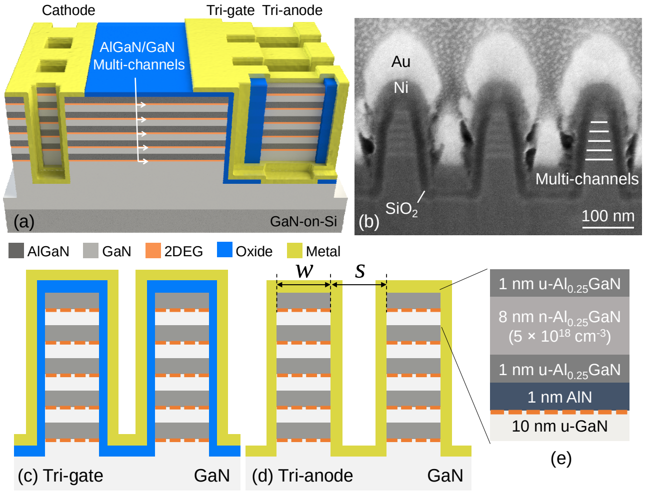

Fig. 1. (a) Schematic of the multi-channel tri-gate SBD. (b) Cross-sectional SEM image of the multi-channel tri-gate region, tilted by 52°. Cross-sectional schematics of the (c) tri-gate and (d) tri-gate regions. (e) Schematic of the heterostructure composing each channel in the multi-channel structure.

II. DEVICE DESIGN AND FABRICATION

The multi-channel AlGaN/GaN heterostructure in this work consisted of 5 parallel 2DEG channels, each composed of 10 nm AlGaN barrier, 1 nm AlN spacer and 10 nm GaN channel layers, in which the barrier was selectively doped with Si at 5 × 10^{18} cm^{-3}. The heterostructure was grown on Si substrate with a 4.3 μm-thick buffer layer, exhibiting a small sheet resistance (R_s) of 230 Ω/sq, along with large carrier concentration (N_s) of 1.5 × 10^{13} cm^{-2} and hall electron mobility of 1820 cm^2·V^{-1}s^{-1}. The anode region was selectively patterned into fins with designed height of 200 nm and width (w) of 50 nm, using Ar/Cl$_2$-based inductively coupled plasma etching, on which the tri-gate (Fig. 1(b)) and tri-anode were formed over the parallel channels. The lengths of the cathode-to-anode (L_{AC}), tri-gate and tri-anode regions were 15 μm, 1.2 μm and 4 μm, respectively. The tri-anode contacts the multi-channels through the fin sidewalls, resulting in a small V_{ON}. The tri-gate/tri-anode regions shield the sidewall Schottky junction from the high electric fields under large reverse biases to reduce I_R [1],[23]. The tri-gate region serves as a field plate, and converts the planar region of the anode into a second field plate, improving the V_{BR} [24]. The ohmic region in the cathode was patterned

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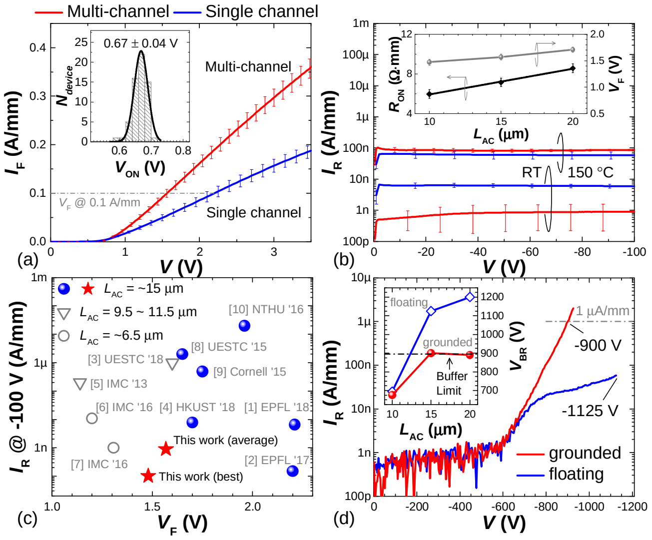

Fig. 2. (a) Forward and (b) reverse characteristics of the multi-channel tri-gate SBDs. (c) Comparison of I_R and V_F of the GaN-on-Si SBDs in this work and literature. (d) Breakdown characteristics of the multi-channel tri-gate SBDs. The inset in (a) shows the distribution of the V_{ON}. The inset in (b) shows the dependence of R_{ON} and V_F upon L_{AC} in multi-channel tri-gate SBDs. The inset in (d) shows the dependence of V_{BR} upon L_{AC} in multi-channel tri-gate SBDs.

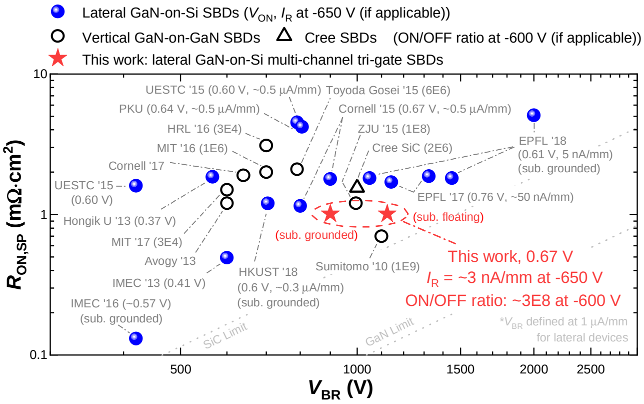

Fig. 3. Specific on-resistance ($R_{ON,SP}$) versus V_{BR} benchmark of the multi-channel tri-gate SBDs against state-of-the-art lateral GaN SBDs. For fair comparison, the V_{BR} for all lateral devices was re-calculated based on the reported data following the definition of V_{BR} at I_R = 1 μA/mm, and devices with unspecified R_{ON} or I_R were not included. Unfortunately the references could not be included here due to the limit in length, however they can be found in Ref. [1] for lateral devices and Refs. [25] for vertical devices.

with *w* and *s* of 500 nm, to contact all parallel channels at the fin sidewalls. In the tri-gate region, 25 nm SiO_2 was deposited by atomic layer deposition as the oxide, and Ni/Au were used as the anode metals. Optimal single-channel SBDs with similar device architecture and dimensions in Ref. [1] were used as reference, which have high mobility of 2000 $cm^2\cdot V^{-1}s^{-1}$ and N_s of 1×10^{13} cm^{-2}. All current values in this work were normalized by the width of the device footprint (60 μm), and the error bars were determined from at least 12 devices of each type.

III. RESULTS AND DISCUSSION

The multi-channel tri-gate SBDs exhibited considerably enhanced performance over counterpart single-channel devices. The R_{ON} was reduced by ~50% to 7.2 ± 0.4 Ω·mm, the forward current (I_F) was increased by ~100% at 3.5 V, and V_F was decreased from 2.21 ± 0.14 V to 1.57 ± 0.06 V (at 0.1 A/mm) in multi-channel tri-gate SBDs, while exhibiting a similar V_{ON} of 0.67 ± 0.04 V at 1 mA/mm (Fig. 2(a)). In these results, the spacing (*s*) between the fins was 100 nm, yielding a filling factor (*FF*) of 33 %. The V_F and R_{ON} in multi-channel tri-gate SBDs changed very slightly with the L_{AC} (the inset in Fig. 2(b)), which is beneficial for high-voltage lateral devices (requiring a large L_{AC}). In addition to the enhanced ON-state conductivity, the multi-channel tri-gate SBDs exhibited a 6x-smaller average I_R of 0.89 nA/mm at -100 V, which increased to only 86 ± 4 nA/mm at 150 °C (Fig. 2(b)), revealing the excellent electrostatic control of the tri-gate over the multi-channels even at high temperature. The small V_F and I_R in this work yields better device performance, in both ON and OFF states, than in other lateral GaN SBDs with similar dimensions (Fig. 2(c)).

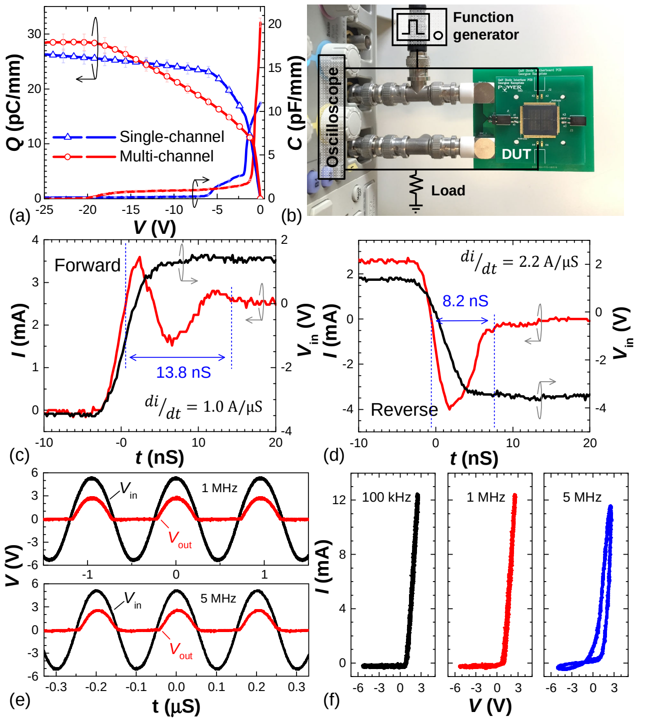

Fig. 4. (a) Capacitance (*C*) and *Q* in multi-channel and single-channel SBDs. (b) Setup for measuring the switching characteristics. The device was bonded onto a printed circuit board (PCB) and connected directly to the oscilloscope to minimize parasitic elements. (c) Forward- and (d) reverse-recovery characteristics of the multi-channel tri-gate SBDs. The devices were switched between 1.5 V to -3.5 V at 1 MHz (limited by the oscilloscope) using the internal oscilloscope function generator and a 50 Ω resistor as the load. (e) Input (V_{in}) and output (V_{out}) waveforms and (f) Lissajous *I-V* plots showing the rectification characteristics of the multi-channel tri-gate SBDs at different frequencies, using an external function generator and a 220 Ω resistor. The small phase shift in (e) between V_{in} and V_{out} was likely caused by parasitic elements in the circuit.

The multi-channel tri-gate SBDs also presented excellent voltage-blocking performance (Fig. 2(d)). The V_{BR} at 1 μA/mm was as high as 900 V with grounded substrate, limited by the 4.3 μm buffer layer (inset in Fig. 2(d)), and the I_R at -650 V was only ~3 nA/mm, which is much smaller than in other reports (Fig. 2(e)). Such high voltage-blocking performance indicate the potential of these devices for 650 V applications, providing an small I_R at the rated voltage and a safety margin of ~50% from the rated voltage to the hard breakdown. The multi-channel tri-gate SBDs presented superb performance and excellent high-power figure-of-merit up to 1.25 GW/cm² (Fig.

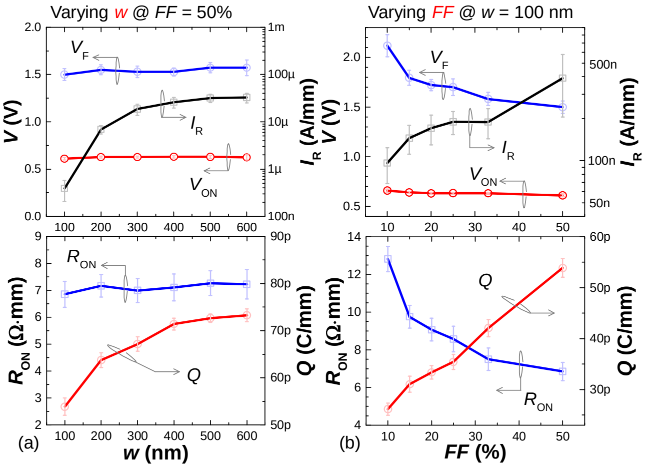

Fig. 5. Dependence of multi-channel tri-gate SBDs' characteristics upon (a) w and (b) FF in tri-gate and tri-anode regions.

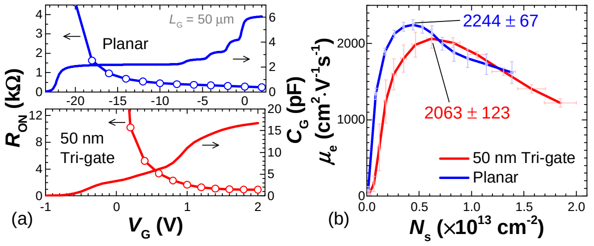

Fig. 6. (a) Average R_{ON} and C_G in multi-channel MOSHEMTs with planar-gates and 50 nm-wide tri-gates. The L_G was 50 µm for both devices, and the gate-to-source and gate-to-drain distances were both 1.5 µm. R_{ON} was measured using drain voltages below 0.1 V, and C_G was measured at 1 MHz. (b) μ_e versus N_s in the two devices. The N_s was normalized by the top surface area of the fins, which did not impact the determination of μ_e.

3), comparable to state-of-the-art GaN-on-GaN vertical SBDs [25],[26] as well as GaN-on-Si power transistors [27].

The switching performance in multi-channel tri-gate SBDs is very promising. Despite the ~50% reduction in R_{ON}, the charge (Q) in multi-channel SBDs increased by only 8.4 % to 28.5 ± 1.5 pC/mm (Fig. 4(a)), which is smaller than in conventional fast-switching GaN-on-Si power SBDs [9],[28], resulting in a much smaller $R_{ON} \cdot Q$ product and thus offering great potential for efficient power rectification at high frequencies. The switching performance of the multi-channel tri-gate SBDs was investigated using a rectification circuit [29] with minimized parasitic elements through an optimized PCB layout and short interconnections (Fig. 4(b)). At a frequency of 1 MHz, the forward-recovery time of the multi-channel tri-gate SBDs was as small as 13.8 ns (Fig. 4(c)), along with a very short reverse-recovery time of 8.2 ns (Fig. 4(d)), which did not change from 10 kHz to 10 MHz. Figures 4(e) and (f) show the V_{in} and V_{out} waveforms as well as Lissajous plots of the I-V characteristics of the multi-channel tri-gate SBDs, respectively, which indicate an effective rectification by these devices up to 5 MHz (at this frequency a phase shift between the V and I was observed).

The high performance of multi-channel tri-gate SBDs depends significantly on the tri-gate/tri-anode geometry to balance the ON-state, OFF-state and switching characteristics. As shown in Fig. 5(a), a smaller w diminishes I_R and Q, but does not significantly degrade R_{ON}, V_{ON} and V_F, thus resulting in a reduced $R_{ON} \cdot Q$ product. The reduction in I_R is due to the smaller pinch-off voltages in tri-gate/tri-anode regions with decreasing w, which lowers the electric field at the Schottky junction and exponentially reduces the I_R [23]. The smaller Q is due to the reduced N_s [30] and smaller threshold voltages in the tri-gate/tri-anode regions as w decreases [1]. Therefore, to have an I_R below 0.1 µA/mm for efficient power devices, w needs to be smaller than 100 nm for the heterostructure used in this work (Fig. 4(a)). FF is another important variable (Fig. 5(b)). A decrease in FF yields a reduction in I_R and Q, but an increase in V_F, V_{ON} and R_{ON}, thus leading to an optimal FF of 33 % for both a small R_{ON} and $R_{ON} \cdot Q$ product.

Another reason for the excellent performance in the multi-channel tri-gate SBDs is the high μ_e in their tri-gate/tri-anode regions. To extract the μ_e, we fabricated multi-channel MOSHEMTs with 50 µm-long planar-gate and tri-gate structures. We measured the R_{ON}, and integrated the measured gate capacitance (C_G) at different gate voltages (V_G) (Fig. 6(a)) to extract the gate charge (Q_G). The μ_e was obtained using $R_{ON} \approx L_G/(W_G \cdot N_s \cdot q \cdot \mu_e) = L_G^2/(Q_G \cdot \mu_e)$, in which L_G and W_G are the gate length and width, respectively, q is the elementary charge, and N_s is the 2DEG concentration in gate region. This method eliminates possible errors in W_G from variation in lithography or normalization. The μ_e in the tri-gate region was as high as 2063 ± 123 $cm^2 \cdot V^{-1}s^{-1}$, which is comparable to that in planar-gate multi-channel devices (2244 ± 67 $cm^2 \cdot V^{-1}s^{-1}$) (Fig. 6(b)), revealing a negligible reduction in μ_e despite the small w of 50 nm, which is much higher than in conventional single-channel AlGaN/GaN fin structures [31]-[33].

The future prospects for the multi-channel tri-gate technology are highly promising. Firstly, it can lead to novel lateral power devices with much smaller R_{ON} and much higher current ratings for a given device area, thanks to its ultra-low R_s, down to 37 Ω/sq [19], combined with the superior voltage-blocking capabilities of tri-gates and slanted tri-gates [1],[27]. Secondly, this approach can be easily extended for high-voltage normally-on/off multi-channel tri-gate GaN transistors [34], nanoscale in-plane-gate transistors, and many other devices and applications, yielding a promising platform for future efficient electronic devices. To unleash the full potential of multi-channel tri-gate technology, an intensive and coupled material research and device engineering are required, which opens tremendous opportunities for future studies in novel epitaxy structures and device designs.

IV. CONCLUSION

In this work we demonstrated novel multi-channel tri-gate GaN-on-Si power SBDs. The devices presented small R_{ON} and V_F, due to the multiple 2DEG channels, and large V_{BR} and ultra-low I_R, thanks to the tri-gate, demonstrating state-of-the-art performance for 600 V/650 V ratings.

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