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Polarity Control of Top Gated Black Phosphorous FETs by Workfunction Engineering of Pre-Patterned Au and Ag Embedded Electrodes

NICOLÒ OLIVA, EMANUELE ANDREA CASU, WOLFGANG A. VITALE (Member, IEEE), IGOR STOLICHNOV, AND ADRIAN MIHAI IONESCU (Fellow, IEEE)

Nanoelectronic Devices Laboratory, Nanolab, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland

CORRESPONDING AUTHOR: N. OLIVA (e-mail: nicolo.oliva@epfl.ch)

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ABSTRACT We propose and experimentally demonstrate top-gated complementary n- and p-type black phosphorous field effect devices (FETs) by engineering the workfunction of pre-patterned electrodes embedded in a SiO_2 bottom layer. Pre-patterned electrodes offer the advantages of reducing the exposure time of exfoliated flakes to oxidant agents with respect to top-contacted devices and maximizing the accessible area for sensing applications. The presented devices are realized by mechanical exfoliation of multilayer black phosphorous flakes on top of pre-patterned embedded source and drain contacts. A capping layer consisting of 15-nm thick Al_2O_3 is deposited to prevent flakes degradation and serves as top gate dielectric. The silicon substrate can be exploited as back gate to program the FETs threshold voltage. We deposited both Au and Ag embedded contacts to investigate the impact of electrodes workfunction on BP FETs polarity. Au contacted devices show p-type conduction with ON/OFF current ratio 140 and holes mobility up to 40 $cm^2V^{-1}s^{-1}$. Devices with Ag contacts exhibit prevalent n-type conduction with ON/OFF ratio 1700 and electron mobility 2 $cm^2V^{-1}s^{-1}$. The reported results represent a substantial improvement with respect to reported alternative implementations of black phosphorous FETs with pre-patterned, non-embedded electrodes. Moreover, we demonstrate that Ag is a promising metal for electron injection in black phosphorous FETs.

INDEX TERMS Black phosphorous, pre-patterned electrodes, 2D materials, field-effect devices, atomic layer deposition.

I. INTRODUCTION

Since the discovery and experimental isolation of graphene, two-dimensional (2D) materials have attracted broad research interest. Graphene exhibits a remarkably high carrier mobility, but its lack of an electronic band gap prevents the realization of field effect devices (FETs) with reasonable I_{ON}/I_{OFF} ratios [1]. Transition metal dichalcogenides (TMDCs) are characterized instead by large band gaps but low carrier mobilities [2]–[4]. Black phosphorous (BP) exhibits a finite direct band gap (0.3 eV in bulk up to 1.5 eV in monolayer) together with high hole mobility, features that make it a promising alternative to TMDCs for the realization of 2D channel FETs and sensors [5]–[8]. However, BP layers are not inert in ambient conditions, and the electrical properties of non-passivated samples are rapidly degraded to such an extent that the functionality of electrical devices is irreversibly compromised [9]. Effective passivation of exfoliated BP flakes against ambient degradation using Al_2O_3 or HfO_2 capping layers has been reported in several works, leading to the demonstration of field effect devices with promising and stable performance [10], [11].

BP FETs are usually realized exfoliating black phosphorous flakes on SiO_2 and depositing by lift-off the electrical contacts, following the same approach used for most of 2D material FETs [5]–[8]. Black phosphorous devices realized with pre-patterned source and drain electrodes have been

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proposed to reduce black phosphorous exposure to air during fabrication [9]. Such electrode configuration moreover allows maximizing the accessible area of black phosphorous flakes for sensing applications, in particular for light detection, while granting a good top gate electrostatic control on the contact area [12]. However, the reported devices showed an I_{ON}/I_{OFF} ratio lower than 10 and reduced carrier mobilities [9]. In a recent work presented at ESSDERC 2017 [13], we reported the implementation of top gated BP FETs with pre-patterned embedded source and drain contacts, realized in Au or Ag. With respect to previously reported pre-patterned contacts, embedding electrodes in a SiO_2 layer allows reducing the amount of mechanical stress on black phosphorous flakes due to topography steps with height comparable or larger than the flakes thickness. Both n and p-type devices have been demonstrated with I_{ON}/I_{OFF} ratios larger than 2 orders of magnitude.

Here, we include the discussion of the impact of back gate bias on the BP FETs transfer characteristic, highlighting in particular its relevance in programming the devices top gate threshold voltage. Moreover, we report the characterization of the FETs hysteresis and subthreshold slope. The measured 1.7 V hysteresis and 1.5 V/dec subthreshold slope values underline how the alumina capping layer, despite being excellent in the prevention of the flakes degradation, provides non-ideal performance both in terms of interface trap density and gate coupling. We also propose fabrication and design solutions meant to close the performance gap between top and bottom contacted BP FETs.

II. DEVICE FABRICATION

The designed process flow is summarized in Fig. 1a, while Fig. 1b shows the atomic force microscopy (AFM) topography image of a complete device. As a first step, a 280 nm SiO2 layer was grown on a Si wafer by wet oxidation. The areas for embedded source and drain contacts were lithographically defined using a direct writing laser tool, VPG200, and a direct resist, ECI 3027. We then etched 45 nm deep boxes in the SiO2 layer exploiting a combination of dry and wet etching, and the electrodes were formed by evaporation and lift-off of either Ti (5 nm) and Au (40 nm), or Ti (5 nm) and Ag (40 nm). The resulting step between the electrodes top surface and the SiO2 layer is reduced to few nanometers. This fabrication approach enables the realization of bottom contacts offering much smaller steps with respect to pre-patterned non-embedded contacts, providing an exfoliation substrate with reduced topography so to facilitate the transfer of BP flakes.

Next, black phosphorous flakes were mechanically exfoliated from a bulk crystal sample (synthetized by *Smart Elements*) following the scotch taping technique. In order to reduce the exposure to ambient oxidizing agents (mainly oxygen and water vapor), the samples were passivated shortly after exfoliation depositing 15 nm of alumina (Al_2O_3) by atomic layer deposition (ALD). The alumina capping layer

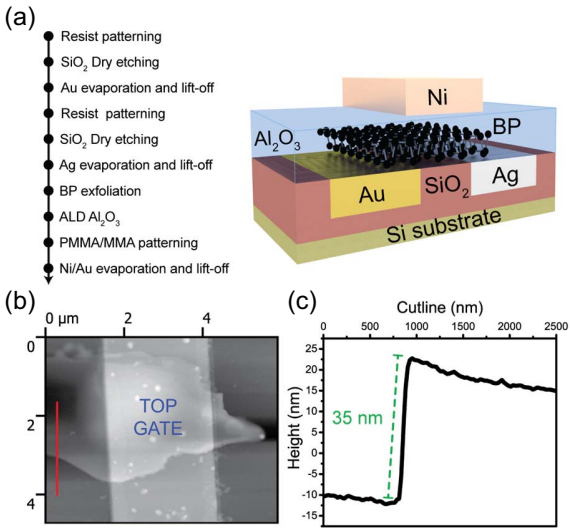

FIGURE 1. (a) Schematic view of the realized devices and summary of the proposed process flow. The embedded pre-patterned electrodes have been realized in Au and/or Ag, while Ni has been selected for the top gate. (b) AFM topography image of the final device measured after the deposition of the top gate. The red line shows the cutline used to extract the flake thickness, as shown in (c). The estimated thickness is 35 nm.

is used also as top gate dielectric. The ALD step was performed in a BENEQ TFS 200 reactor heated at 200°C, using TMA and H_2O as precursors. We then identified flakes favorably connected to the embedded electrodes using optical microscopy. Finally, the top gate electrode was obtained by patterning a PMMA/MMA bilayer using electron beam lithography and evaporating and lifting off Ni (50 nm) and Au (10 nm). In order to limit the gate leakage current, the top gate mask has been designed so to avoid any overlap with the embedded bottom contacts. BP flakes thickness was determined using AFM, as shown in Fig 1c. The results reported in the following have been obtained from BP FETs realized with flakes with thickness in the 30/40 nm range.

III. RESULTS

All the electrical measurements presented have been performed at ambient conditions and room temperature using an HP 4156C semiconductor parameter analyzer.

A. IMPACT OF ELECTRODES WORKFUNCTION ON BP FETS POLARITY

In order to study the impact of the different metals used for the pre-patterned electrodes, we fabricated and characterized Au, Au-Ag and Ag-Ag contacted devices. The transfer characteristics in linear scale for three devices with these metal electrode combinations are shown in Fig. 2a, 2b and 2c. The reported $I_D(V_G)$ curves have been obtained applying a drain to source bias of absolute value equal to 750 or 500 mV. Au contacted devices exhibit p-type conduction, while both Ag and Au-Ag devices, where the Ag contact is used as FET source, show prevalent n-type conduction. The role played by contacts workfunction in the determination of BP FETs

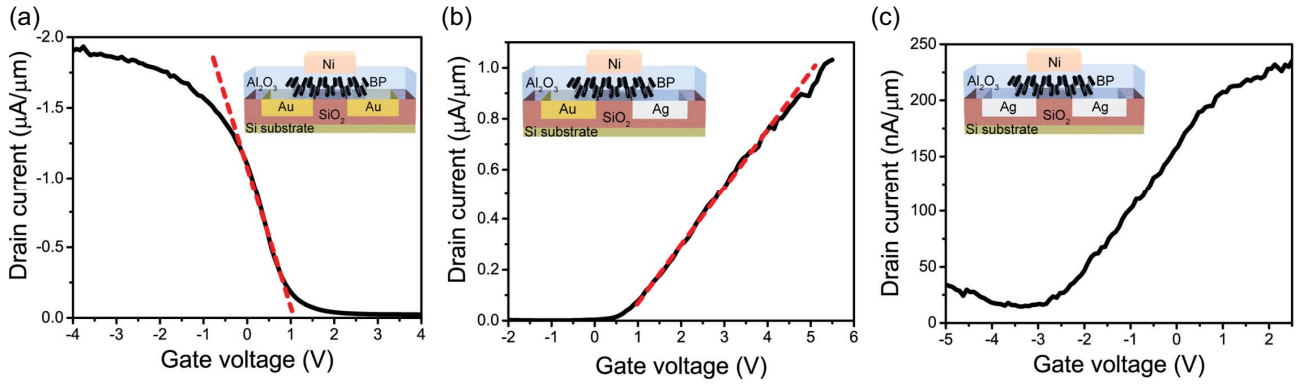

FIGURE 2. **Comparison of the transfer characteristic $I_D(V_C)$ of BP FETs realized with different embedded bottom contacts. The results reported have been obtained applying a drain to source voltage of absolute value equal to 750 mV for the Au-Au contacts device and 500 mV for the Ag contacted devices. (a) Au contacted devices exhibit a clear p-type conduction. (b) and (c) Devices with Ag contacts or Au-Ag electrodes with the Ag used as transistor source show n-type polarity. The red dotted line in (a) and (b) represents the linear fit performed for the mobility extraction. Insets: schematic representation of the BP FETs with the different sets of embedded electrodes.**

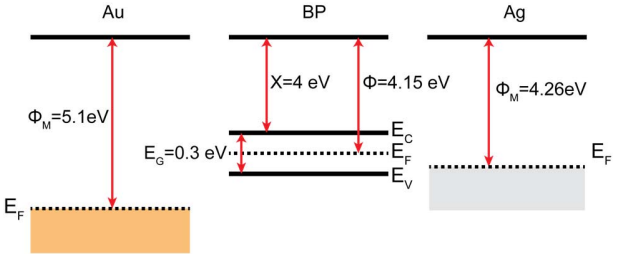

FIGURE 3. **Band diagram in vacuum of Au, multilayer BP flakes and Ag. Multilayer BP flakes show a band diagram similar to bulk samples. Polycrystalline Ag presents a workfunction close to BP one, so it is promising for electron injection in BP conduction band. Au on the contrary has a larger workfunction, favoring hole conduction in BP rather than electron one.**

polarity can be understood referring to the band diagram reported in Fig. 3.

Multilayer BP flakes have a band structure similar to the bulk one, characterized by a 0.3 eV band gap and a 4.15 eV workfunction [14]. Polycrystalline Au and Ag exhibit respectively a 5.1 eV and a 4.26 eV workfunction. As shown in Fig. 3, Ag is expected to offer a small barrier for electron injection to BP conduction band, enabling the n-type conduction observed in Ag contacted BP FETs. Vice versa, Au contacts favor holes injection while providing a high barrier for thermionic injection in BP conduction band. An analogous BP FETs polarity-control based on low workfunction metals (Al and Ti) has been reported for top contacted devices [7], [15].

B. IMPACT OF BACK GATE BIAS ON TRANSFER CHARACTERISTIC

As shown in the schematic structure in Fig. 1, the BP channel can be electrostatically controlled by both the top gate and the silicon substrate. However, because of the thick SiO_2 layer between the flake and the bottom gate, the resulting gate coupling is poor, requiring a relatively large bias to affect the FET conduction. Moreover, the introduction of large embedded metal contacts placed closer to the back gate with respect to the FET channel provides a preferential leakage path from the electrodes that can mask the gate leakage from the BP flakes. Therefore, rather than sweeping the back gate bias, we study the impact of a fixed bias applied to it on the top gate $I_D(V_G)$ curve.

Fig. 4a reports the transfer characteristics of a n-type device measured at different values of substrate bias. The increase of the back gate voltage from negative to positive values determines a clear negative shift of the transfer characteristic. Indeed, the top gate threshold voltage extracted from the intercept of the linear part of the $I_D(V_G)$ curve decreases linearly with the increase of the substrate bias as shown in Fig. 4b. The extracted slope gives a negative shift in the top gate threshold voltage of 56 mV per applied volt at the back gate.

These results show that the back gate can be efficiently exploited to program the threshold voltage of the device, providing a further degree of freedom for the BP FETs biasing.

C. TOP GATE HYSTERESIS AND SUBTHRESHOLD SLOPE

Al_2O_3 has been proven to provide a good passivation against oxidizing agents for BP flakes [10]. However, it is known to be a dielectric characterized by a high density of interfacial charge traps, in particular when deposited on 2D materials [15]. In order to characterize the impact of such traps on the FET conduction, we performed a double sweep measurement on a n-type device with the back gate grounded. The result is shown in Fig. 5a. The measured hysteresis between forward and backward sweeps is 1.7 V, suggesting that the Al_2O_3/BP interface hosts several trap states.

Fig. 5b shows the subthreshold slope plotted vs the output current for the two directions of sweep of the gate voltage. A minimum value of 1.5 V/dec has been obtained. Such results suggest that the quality of the deposited dielectric alumina layer is not excellent, as commonly observed for ALD depositions on 2D materials. However, the measured

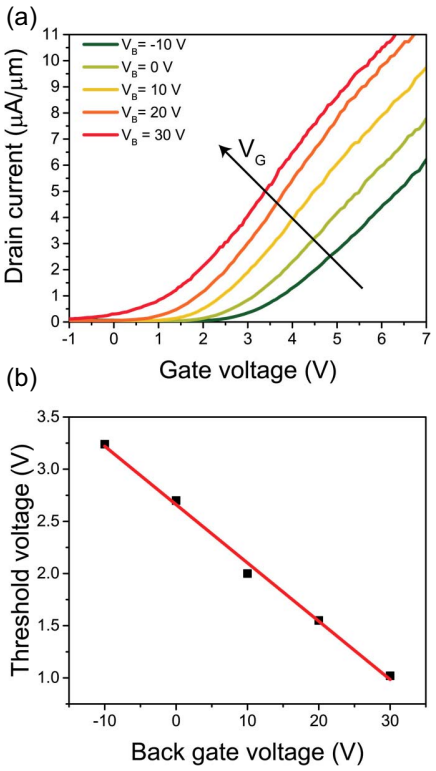

FIGURE 4. **(a) Top gate transfer characteristic of a n-type device measured at different back gate bias values. A clear negative shift of the $I_D(V_G)$ curve is observed under positive substrate bias. (b) Extracted threshold voltage as a function of the back gate bias. The linear fit provides an estimated top gate threshold voltage sensitivity to the substrate bias of −56 mV/V.**

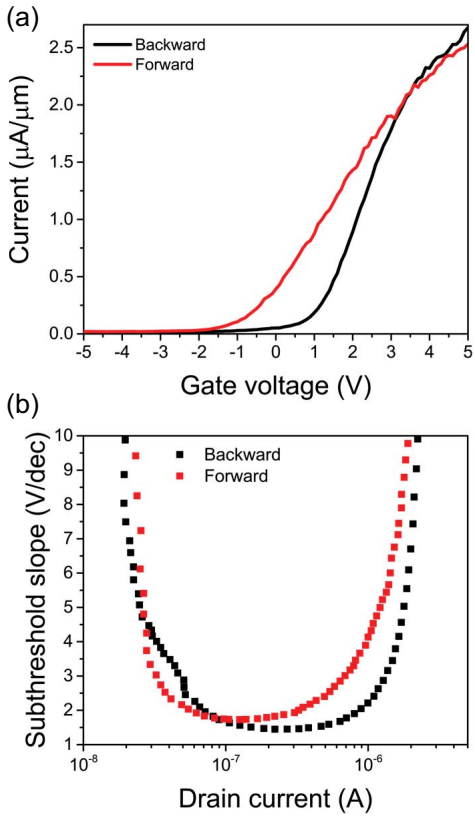

FIGURE 5. **(a) Double sweep transfer characteristic of a n-type device. The measured hysteresis is 1.7V. The minimum subthreshold slope (b) is 1.5 V/dec, maintained over one order of magnitude of the output current.**

top gate leakage current is extremely low, remaining below 5 pA/μm in all the measurements reported in this work.

The reduction of the hysteresis would require the deposition of other high-k dielectrics like HfO_2 that however presents nucleation and film continuity issues on 2D flakes [16]. A substantial improvement of the subthreshold slope could be achieved realizing devices with thinner BP flakes and thinner Al_2O_3 layer, so to increase the capacitive coupling between the top gate and the channel.

D. TRANSFER AND OUTPUT CHARACTERISTIC OF N AND P TYPE BP FET

In the following we present a detailed characterization of the realized FETs, focused on representative p and n-type devices. All the measurements reported have been obtained with the bottom gate grounded. We fabricated both the devices on the same wafer and with the same processing conditions, and we performed the dielectric deposition simultaneously on the two FETs. The p-type device is contacted with Au electrodes and presents gate length L = 2.6 μm and width W = 1.5 μm. The n-type FET has Au drain and Ag source, with L ≈ W = 1.6μm. The output characteristics of these two devices, measured at different gate biases, are reported in Fig. 6. The $I_D(V_D)$ curves of both the Au contacted device (Fig. 6a) and the Ag-Au one (Fig. 6b) show

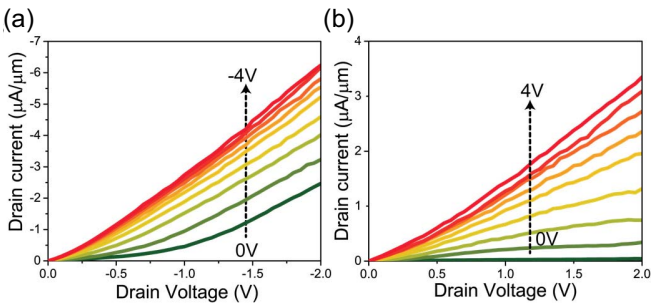

FIGURE 6. **Output characteristic $I_D(V_D)$ in linear scale of Au (a) and Au-Ag (b) contacted BP FETs measured at different gate biases. For both the devices and set of contacts, there is no saturation of the output characteristic and a linear behavior is observed.**

no saturation for the considered gate bias range and a linear behavior.

We report in Fig. 7a and 7b the transfer characteristics of the same devices in semi-logarithmic scale, obtained measuring the $I_D(V_G)$ curves at different drain-to-source biases. The p-type FET (Fig. 7a) shows a I_{ON}/I_{OFF} current ratio larger than two orders of magnitude. The n-type device instead (Fig. 7b) reaches a I_{ON}/I_{OFF} of 1700. These results outperform the ON/OFF current ratios reported for pre-patterned non-embedded contacts [9], and could be further improved in BP FETs realized with thinner flakes and

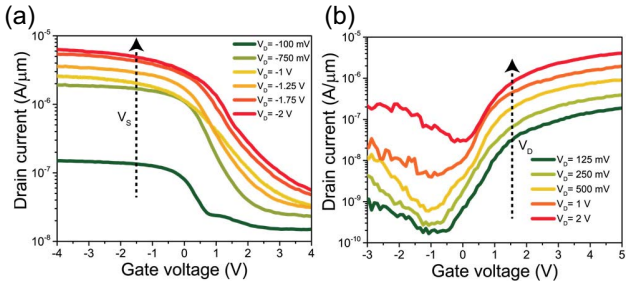

FIGURE 7. Transfer characteristic $I_D(V_G)$ at different drain-to-source biases in semilog scale of the characterized p-type (a) and n-type (b) BP FETs. The p-type device exhibits a I_{ON}/I_{OFF} ratio larger than 10^2, while the n-type FET provides a ON/OFF current ratio larger than 10^3.

bottom gate dielectric, thanks to the larger BP band gap and higher quality of the dielectric layer.

Fig. 8 shows the extracted transconductance (g_m) curves as a function of the gate bias for the two devices, measured under several values of the drain to source bias. The Au contacted device transconductance (Fig. 8a) exhibits a relatively narrow peak in the gate bias range from −1V to 1 V. This suggests that the contact resistance is limiting the transconductance, preventing the saturation of the curve at the peak value [17]. At large negative gate biases, the series resistance provided by the contacts becomes larger than the BP channel resistance determining a decrease of the $I_D(V_G)$ curve slope and the consequent degradation of the transconductance. Conversely, the n-type device transconductance, reported in Fig. 8b, saturates to its peak value over a large window of gate voltages suggesting a lower impact of the contact resistance on the n-type FET conduction.

E. FIELD EFFECT MOBILITY EXTRACTION

We then extracted the two-terminal effective field effect mobility, μ_{FE}, using $\mu_{FE} = g_m L/WC_{ox}V_{DS}$, where g_m is the transconductance extracted from the linear part of the $I_D(V_G)$ curve, W is the channel width and C_{ox} is the gate capacitance per unit area for the deposited 15 nm of Al_2O_3. The relative permittivity of the dielectric layer has been extracted to be equal to 6.9 by characterizing MIM structures included on the same wafer of the devices. The $I_D(V_G)$ curves of the two devices in linear scale are shown in Fig. 1a and Fig. 1b together with the fit of the linear part, whose slope is used for the mobility extraction. The obtained hole mobility for the Au contacted transistor is 10 $cm^2V^{-1}s^{-1}$ at $V_{SD} = 750$ mV, while the Au-Ag FET presents an electron mobility of 1.8 $cm^2V^{-1}s^{-1}$ at $V_{DS} = 500$ mV.

In order to obtain a more accurate estimation of the carriers' mobility by decoupling the impact of the contact resistance, we applied the so-called Ghibaudo Y function method, which provides a robust evaluation of the low-field carrier mobility in 2D channel field effect devices [2]. Assuming that the contact resistance is not dependent on the gate bias, the Y function expression reduces to:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{\mu C_{ox}\,|V_{DS}|\,W}{L}}\,(V_G - V_T) \qquad (1)$$

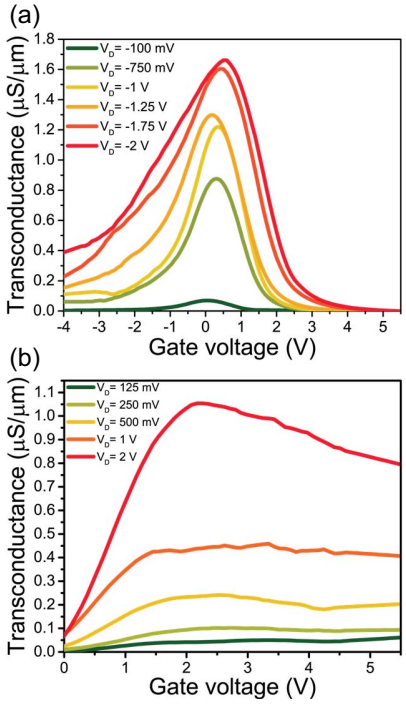

FIGURE 8. Gate transconductance $g_m(V_G)$ at different drain to source biases of the characterized p-type (a) and n-type (b) BP FETs. The Au contacted device shows a peak in the transconductance curve, while the n-type g_m saturates to its maximum value over a wide range of the applied gate bias.

where V_T is the threshold voltage. The carrier mobility is then given by:

$$\mu = \frac{L}{C_{ox}\,|V_{DS}|\,W}\left(\frac{\partial Y}{\partial V_G}\right)^2 \qquad (2)$$

Fig. 9 shows the Y functions extracted for the two reported devices, and the corresponding fit of the linear region from which it is possible to estimate the low field mobility applying (2). The obtained mobilities are 40 $cm^2V^{-1}s^{-1}$ for holes in the Au contacted FET (Fig. 9a) at $V_{SD} = 750$ mV and 2 $cm^2V^{-1}s^{-1}$ for electrons in the Au-Ag device (Fig. 9b) at $V_{DS} = 500$ mV. The large enhancement of the hole mobility for the p-type device estimated with the Y function method together with the gate dependence of the transconductance shown in Fig. 8a, suggests that the contact resistance is playing a relevant role in limiting the Au contacted device performance. Vice versa, the n-type device shows a limited increase of the extracted mobility obtained applying the Y function method, suggesting that Ag constitutes indeed a good contact for electron injection in BP.

The extracted mobility values and I_{ON}/I_{OFF} ratios are larger than the ones reported for pre-patterned non-embedded contacts [9], but are still lower than other results published for top contacted BP FETs [5], [7]. Other sources of mobility reduction not considered here could be the interface roughness scattering, the high density of oxide traps in the SiO_2 and Al_2O_3 dielectric layers and the anisotropic mobility distribution in the 2D plane of black phosphorous [11], [18].

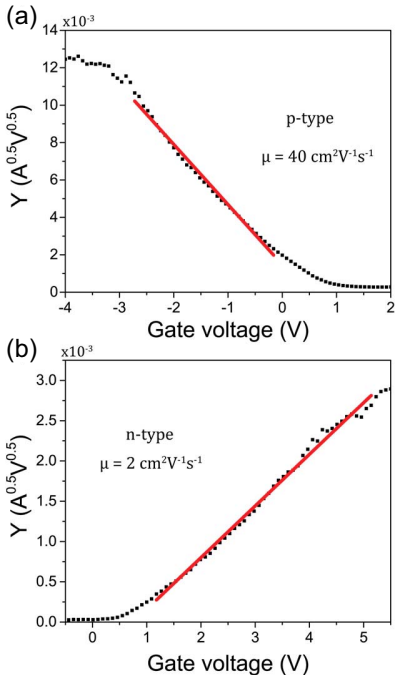

FIGURE 9. Extracted Y function vs gate voltage of (a) the p-type FET at $V_{SD} = 750$ mV and (b) the n-type device at $V_{DS} = 500$ mV. The mobility can be extracted from the slope of the linear part of the curve, shown in red in the figures.

The performance of p-type devices could also be negatively affected by the choice of the top gate dielectric, since Al_2O_3 has been reported to impact considerably the p-type dominant conduction mechanism in black phosphorous FETs [11].

IV. CONCLUSION

In summary, we have demonstrated for the first time the polarity control of top gated black phosphorous FETs obtained by workfunction engineering of embedded pre-patterned contacts, exhibiting enhanced performance with respect to alternative implementations of BP FETs with pre-patterned electrodes. Both n and p-type devices have been characterized, exhibiting electron and hole mobilities respectively 2 $cm^2V^{-1}s^{-1}$ and 40 $cm^2V^{-1}s^{-1}$ extracted applying the Y function method. Moreover, we proved that Ag electrodes can be used as n-type conduction enabler in black phosphorous FETs, whose polarity can be controlled by properly selecting the source and drain contacts workfunction. The silicon substrate can be used as bottom gate to program the threshold voltage of the top gate transfer characteristic, providing a further degree of freedom for the biasing of the devices. Typical devices show a hysteresis of 1.7 V, minimum subthreshold slope of 1.5 V/dec and a top gate leakage current below 5 pA/μm.

The proposed fabrication approach minimizes the exposure of unprotected flakes to ambient oxidants and contaminants. The use of embedded bottom contacts allows a significant reduction of the substrate topography, granting a good transfer and a reduced stress on the BP flakes. The proposed BP FETs structure is particular interesting for sensing application since it maximizes the sensing area and enables the possibility of programming the device threshold voltage using the silicon substrate as bottom gate. Enhancements of the performance would require the reduction of the contact resistance and the improvement of the capacitive coupling between the top gate and the black phosphorous channel, so to increase the gate transconductance and obtain a saturating output characteristic with larger output impedance. The design of the gate mask can be modified to include an overlap of the top gate and the contacts, so to make possible an effective electrostatic doping of the flake areas in direct contact with the bottom electrodes. The deposition of high-k dielectrics with lower interface trap density with respect to Al_2O_3 [11] and the transfer of thinner BP flakes are fundamental to improve the overall performance of the device.

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NICOLÒ OLIVA received the M.Sc. degree in micro and nano technologies for integrated systems from EPFL, Grenoble INP, and Politecnico di Torino in 2015. He is currently pursuing the Ph.D. degree with Laboratory of Micro/Nanoelectronic Devices, EPFL, researching on 2-D materials and heterojunctions for sensing and computing applications. He completed the master's project on piezoelectric resonant transformers for power supplies on chip in Professor Piazza's Group with Carnegie Mellon University, Pittsburgh, in 2016. In 2016, he joined the Laboratory of Micro/Nanoelectronic Devices, EPFL.

EMANUELE ANDREA CASU received the M.Sc. degree in micro and nano technologies for integrated systems from Lausanne (EPFL), Grenoble INP, and Politecnico di Torino in 2012. He is currently pursuing the Ph.D. degree with EPFL. He completed the master's project on oxides growth and characterization on graphene with IBM Thomas J. Watson Research Center. In 2010, he had an undergraduate internship in a startup company, EULEGO srl, Turin, where he researched on C programming for safety-critical embedded system. In 2013, he joined the Laboratory of Micro/Nanoelectronic Devices, EPFL, where he has been researching on MEMS resonators for communication and sensing applications, steep-slope switches based on insulator to metal transition, TMDC/VO_2 junctions, and reconfigurable RF functions based on VO_2.

WOLFGANG A. VITALE received the M.Sc. degree in micro and nanotechnologies for integrated systems from the Swiss Federal Institute of Technology, Lausanne (EPFL), in 2010 and the Ph.D. degree from the Laboratory of Micro/Nanoelectronic Devices, EPFL. His main research interests involve advanced materials and technologies for reconfigurable electronic devices, including vanadium dioxide, RF MEMS, and graphene.

IGOR STOLICHNOV received the master's degree in solid state physics from Saint Petersburg State Polytechnical University in 1994 and the Ph.D. degree from the Laboratory of Ceramics, EPFL, in 2000 for his research on physical mechanisms of losses in ferroelectric nonvolatile memories. From 1995 to 1996, he was with the Wide-Gap Semiconductors Laboratory, A.F. Ioffe Physical Technical Institute, St. Petersburg. Since 2015, he has been a Staff Member of the Laboratory of Micro/Nanoelectronic Devices, EPFL. His scientific interests are focused on functional materials and their applications for information processing and storage, including ferroelectrics, dielectrics and multiferroics, and advanced methods of materials characterization at nanoscale and integration of ferroic nanostructures and films on semiconductors and metals for novel memory devices.

ADRIAN MIHAI IONESCU received the Ph.D. degree from the National Polytechnic Institute of Grenoble, France. He is a Full Professor with the Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland. He has held staff and/or visiting positions with LETI-CEA, Grenoble, LPCS-ENSERG, and Stanford University in 1998 and 1999. He is the Director of the Laboratory of Micro/Nanoelectronic Devices, EPFL. His research interests focus on micro- and nanoelectronic devices aimed at integrated circuit design, particularly process development, modeling, and electrical characterization. He has published over 250 articles in international journals and conference proceedings.