From Wafers to Modules to Mass Production: Solving All Bottlenecks in Silicon Heterojunction Technology

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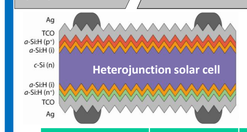
Removing all obstacles to massive market penetration

Silicon heterojunction solar cells have less manufacturing steps and have allowed achieving higher efficiency than PERC cells. However the market has been slow in taking up the technology. Here we show some of the obstacles that have been overcome in the last 10 years which make the technology more ready than ever for a mass market launch.

Chemical baths: c-Si surface preparation → PECVD: a-Si:H thin films deposition, intrinsic and doped: i-n, i-p → PVD: TCO → Metallization: Screen printing + curing at 200° C



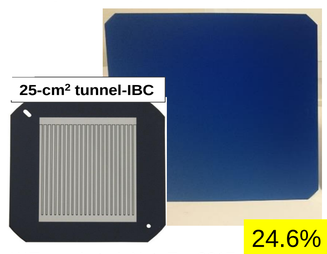
Screen printed laboratory cells
Standard n-type, p-type, 4 cm², da
All results transferrable to CZ, large area

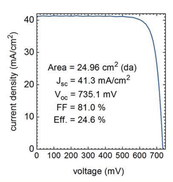
Type	J_{SC} (mA/cm²)	V_{OC} (mV)	FF (%)	EFF. (%)
On n-type Fz wafer	40.8	727	81.1	24.1
On p-type Fz wafer	40.7	722	80.7	23.76

Certified SHJ on p-type ! Record

Some new key recent results

8 steps IBC process (tunnel junction*)**



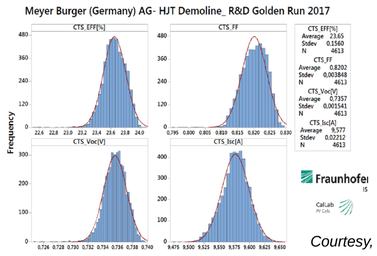


***Tomasi et al. Nat. En. 2017

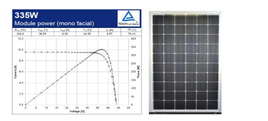
24.6% record for TJ IBC !

Results achieved with Demo-lines at Meyer Burger

Production run, 6 inches, 23.65% busbarless



- 335 Watt 60 cells
- 410 Watt 72 cells
- Up to 92% bificiality



M. König, this conf, ***2DV.3.68 3***

Courtesy, J. Zhao, B. Bonnet-Eymard. M. König,

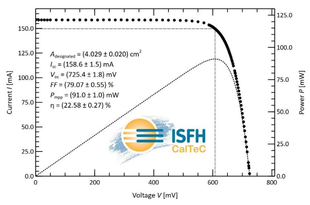
Impossible to get good quality low cost n-type wafer

Wrong

- Strong material improvements over the last 10 years
- Today SOA n-type c-Si does not require gettering or thermal donor killing
- At 180 μm thickness n-type wafer 5% more expensive than p-type (less pulls)
- -1.5cts per 10μm less…
- N-type 140 μm wafers **are cheaper** than 170 μm for standard cells

High Quality n-type wafer at lower cost than p-type wafer by using 30 μm less giving you more Watts

- Suitable for almost all materials
- For QuasiMono and multi, gettering/hydrogenation might be required



22.6% record for cast Quasi-Mono !

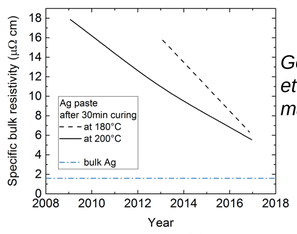
J. Hascke et al. IEEE WCPEC-7
M.M Kiwambe et al. this conf. **2BO.1.2**

No good metallization solutions available, 500 mg of Ag per cell

Wrong

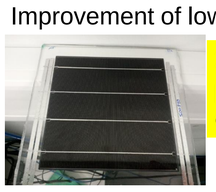
- Strong improvements of low T Ag paste. ρ now down to 5 μΩcm.
- Possibility to plate cells, or to shingle
- Solutions with multi-wire
- Solutions with multi-bus bars

Certified metallization and interconnection with no expensive materials available



Geissbühler et al. PV magazine

Improvement of low-T Ag Paste



24.14% certified plated cell on 225 cm², 4 busbars

Precursors from CHOSHU

A. Lachowicz, this conf. **2CO.12.5**

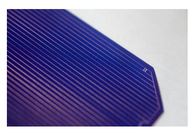
Indium-free smart Wire, with as little as 25 mg Ag per side

Complex manufacturing processes. Solar cell makers do not use // plate PECVD and PVD tools

Wrong

- From thin film solar, flat panel displays and glass coating, low cost per m² from PECVD (e.g. parallel plate reactor) and PVD.
- Fewest number of process steps: 5-7 depending on tools and processes
- Alternative deposition techniques available (hot wire, TCO by PAE)
- Easily controlled homogeneity with good tool design
- > 20 research institutes and (pilot) lines with above 22% efficiency

Fully controlled. Good tools will make in one day >> 20% cells



CSEM/EPFL SILICON HETEROJUNCTION R&D PLATFORM
> 20 tools for advanced and fast R&D

Too expensive industrial productions solutions, reliability issues

Wrong

- Equipements price going down with competition
- Even extra capex 5 M$/100 MW → only 0.8 cts/W extra
- Higher capex, compensated by efficiency/bificiality/energy yield
- When designed properly, ultra-resistant products, no PID.
- Can even improve under light soaking ! *J.Cattin, this conf.* **2DO.1.4.**

Production equipment available allowing competitive costs for manufacturing at GW level

- Now close to 10 lines with > 100 MW capacity
- Several GW announced
- Need of volume as with all c-Si technologies

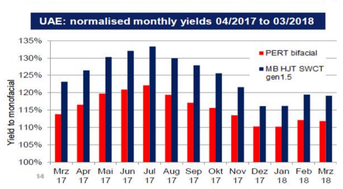
Exemple: Helia Meyer Burger platform for SHJ

Cost of electricity

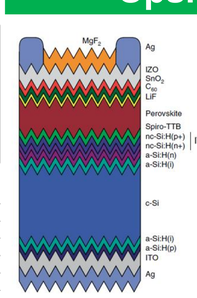
- Low temperature coefficient (-0.2%/°C to -0.27%/°C)
- No PID
- High bifaciliality

→ Higest energy yield and lowest LCOE

A. Richter et al. IEEE WCPEC-7



Upside potential



F. Sahli et al Nat. Mat. 2018, IEEE WCPEC-7

- Transform to IBC with 5-8% rel. Eff. increase
- Move to multijunction III-V/Si (35.9%**)
- Perovskite tandem devices

25.2 % certified record for PK/Si textured

***Essig et al. Nat. En. 2017*

conclusion

Over the last 10 years, improvements in:
- Processes compatible with industrial production,
- Efficiency achieved on production tool,
- Metalization and interconnections, reliability,
- Material quality,
- Tools for cost-effective production.

If/when capital is available, Si heterojunction technology is ready for true mass market launch

Read more: Jan Haschke et al., Solmat 187 (2018), 140

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