

Charge-Based Modeling of Radiation Damage in Symmetric Double-Gate MOSFETs

Farzan Jazaeri, Chun-Min Zhang, Alessandro Pezzotta, and Christian Enz

Abstract—In this paper a comprehensive charge-based predictive model of interface and oxide trapped charges in undoped symmetric long-channel double-gate MOSFETs is developed. The model involves essentially no fitting parameters, but first-principle calculations of both oxide and Si/oxide interface trapping. This charge-based approach represents an essential step toward compact modeling of ionizing dose and aging effects in advanced field effect devices. The soundness of this approach is confirmed by extensive comparisons with numerical TCAD simulations, while the analytical formulation helps understanding the most relevant parameters of the phenomena with respect to a specific technology. The model confirms its validity for all regions of operation, i.e., from deep depletion to strong inversion and from linear to saturation.

Index Terms—oxide traps, interface traps, total ionizing dose, TID, double-gate FET, aging effects, FinFET.

I. INTRODUCTION

THE Large Hadron Collider (LHC) at CERN has been exploring the new high-energy frontier since 2010 and has made the successful observation of the long-sought Higgs Boson possible in 2012. To extend its discovery potential, it will need a major upgrade around 2020 for a ten times higher integrated luminosity. This high-luminosity LHC (HL-LHC) is expected to experience an unprecedented radiation level up to 10 MGy (1 Grad) of Total Ionizing Dose (TID) and 10^{16} neutrons/cm² of hadron fluence over ten years of operation. To select the most appropriate alternative in terms of radiation tolerance, it is of great importance to comprehend the ionizing radiation effects on advanced CMOS from the fundamental physics and basic models points of view [1], [2].

The investigation of radiation effects on MOSFETs has started since the late 1960's by Hughes and Giroux [3], in parallel with the technological innovation in semiconductor manufacturing. So far, the radiation-related characterization and the theoretical model building are proceeding in a mutual-benefiting way for interpreting the radiation response of the MOSFETs. Defects in oxides and at semiconductor/oxide interfaces have been identified as the dominant precursors for MOSFET radiation damages. Whenever the incident radiation creates electron-hole pairs in the oxide, these defects act as traps for those charges, affecting performance [4].

Owing to the CMOS technological scaling, materials and configurations are continuously changing, focusing on power consumption reduction. This has led to the inclusion of

unconventional dielectrics (i.e. high- κ , low- κ materials), or different isolation structures (STI, LOCOS, etc.). All these have to be considered as variables for radiation-induced performance degradation. Double-Gate (DG) MOSFETs demonstrate outstanding electrical characteristics, such as a higher drain current, a more effective mobility [5], [6], a higher transconductance and an enhanced subthreshold slope due to charge coupling [7] and they can be easily modeled using an explicit charge-based expression in compact models [8]–[10].

This work proposes to derive analytical expressions for modeling the effects of total ionizing dose (TID effects) in undoped DG MOSFETs upon technological parameters. Relying on the charge-based approach, this work describes the main mechanism of radiation-induced damages in MOSFETs and the impact of ionizing radiation on the electrostatics of DG MOSFETs. Analytical explicit solutions for the intrinsic gate capacitance and main DC parameters, i.e. subthreshold swing and threshold voltage, are derived.

II. DESCRIPTION OF BASIC PHYSICAL PROCESSES FOR TOTAL IONIZING DOSE EFFECTS

The total amount of collected energy from the incident radiation by a specific material through ionization is named ‘Total Ionizing Dose’. Whilst a MOSFET is exposed to high-energy ionizing radiation, electron-hole pairs are created by the deposited energy in oxides. In the first picoseconds after irradiation, a fraction of them recombines. However, since the electrons are more mobile than the holes [11], [12], most of the electron-hole pairs do not recombine. Remaining electrons are then swept out of the oxide in the next few picoseconds and are collected at the corresponding electrode. The holes surviving the initial recombination and remaining within the oxide volume will move across the oxide through a hopping transport mechanism, leading to a distortion of the local electric field in the oxide. This local distortion tends to trap a fraction of those holes (Q_{ot}) into relatively deep trap states in the oxide bulk or near the Si/oxide interface [4]. It should be remarked that some of the holes are swept out towards the silicon bulk as well, due to tunneling mechanisms. However, holes trapped close to the interface, that can easily capture or emit carriers to the silicon, are called border traps or switching oxide traps [13]. Additionally, reactions between transporting holes and hydrogen-containing defects or dopant complexes can contribute to the formation of those interface traps (Q_{it}) [14]–[16] located exactly at the interface. Therefore, the holes surviving the initial recombination cause ionization damage in the form of oxide charged traps (Q_{ot}) and interface

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Manuscript received in September 14, 2017.

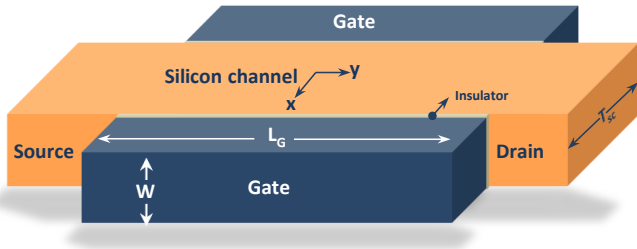


Fig. 1: Schematic view of the undoped channel double-gate MOSFET.

charged traps (Q_{it}). This process is very sensitive to the applied electric field, the temperature and the oxide thickness. The trapped charges modify the electrical characteristics of irradiated MOSFETs as observed in [17], [18]. In particular, they have a strong effect on the weak inversion region of the I - V characteristic. Typically, TID effects give rise to several types of performance degradation, including threshold voltage shift, mobility degradation, and incremental change both in the *off*-state leakage current and in the subthreshold swing [19]–[25]. In this context, a detailed description about how the defects affect the electrical properties of the most common oxide-based devices is delivered.

III. INTERFACE AND OXIDE TRAPPED CHARGES

As mentioned, interface and oxide trapped charges influence the device characteristics, leading to performance degradation and possibly to failure. Therefore, a quantitative description of radiation-induced trap charging requires a knowledge of the physical mechanisms underlying the phenomena, together with numerical simulations of the complete system dynamical evolution, serving as reference for the analytical model.

A. General remarks on interface trapped charges in MOSFET

Close to the interface, a large number of oxygen vacancies occur, due to the out-diffusion of oxygen in the oxide and lattice mismatch at the surface. These oxygen vacancies can act as trapping centers [26], [27]. Due to the fact that interface traps result from dangling silicon bonds at Si/oxide interface [28], these charge states depend on the Fermi level and therefore on the channel surface potential [19], [29]. Thus, interface charged traps can be positive, neutral, or negative. Trap energy levels below the mid-gap exhibit donor-like characteristics, i.e. being positively charged by emitting an electron if above Fermi level and electrically neutral when filled if below. Trap energy levels above the mid-gap exhibit acceptor-like characteristics. These trap levels are electrically neutral when empty if above Fermi level and negatively charged when trapping an electron if below. Therefore, the interface charged traps are amphoteric and whether they behave as donors or acceptors depends on their energy in the band-gap [19], [30]. Fig. 2a illustrates the energy diagram of a lightly doped DG n MOSFET biased in inversion mode, where a positive bias is applied to the gate so that electrons flow towards it and holes move to the silicon substrate. The Fermi level of n MOSFET far from surface

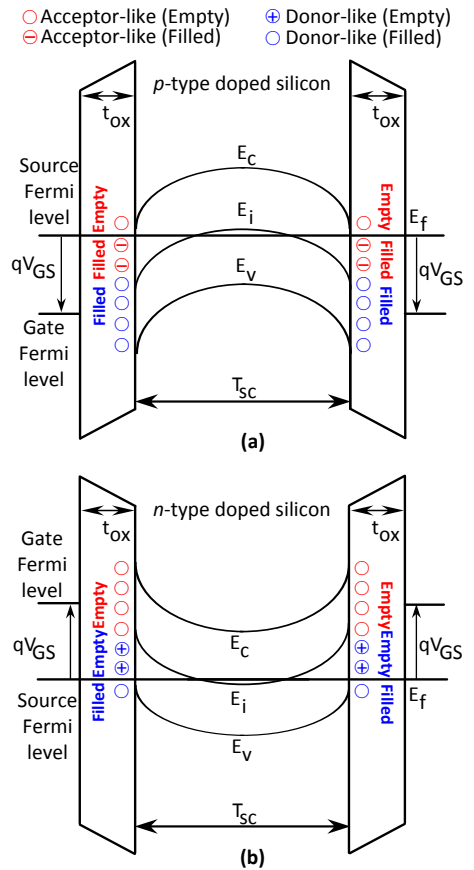


Fig. 2: Energy diagrams for a lightly doped symmetric double-gate (a) n MOSFET where a positive bias is applied to the gate and (b) p MOSFET where a negative bias is applied to the gate terminal.

is located below the mid-gap, while above at the Si/oxide interface. As illustrated, the donor-like interface trap levels are completely filled and acceptor-like trap levels are partially filled. The result is a negative set of interface trapped charges. For sake of completeness, as illustrated in Fig. 2b, in a p MOSFET biased in inversion mode the Fermi level far from the interface is located above the mid-gap energy, vice versa at the surface. Therefore, the acceptor-like trap levels are entirely empty and the donor-like trap levels are partially filled, leading to positive charged traps at Si/oxide interface. The interface charged trap density Q_{it} can be expressed by integrating the product of the interface trap-state density D_{it} , [$Number \times cm^{-2} \times eV^{-1}$] and the trap occupation probability per unit area over energy across most of the band-gap [19], [30]

$$Q_{it} = -q \int_{E_V}^{E_C} D_{it}(E) f(E) dE, \quad (1)$$

where $f(E)$ is the trap occupation probability at energy level E given by $f(E) = 1/\{1 + \exp[(E - E_f)/kT]\}$, $D_{it}(E)$ is the surface-state density per unit area per unit energy. Given the fact that the surface density of state is a continuous function of the trap energy level, (1) has no analytical solution. Therefore, firstly we propose to seek for an approximate solution to (1) for single-level interface traps and later on continuous trap energy distribution. Therefore, given the trap energy E_t and the probability of occupation $f(E_t)$ and $D_{it}(E_t)$ in (1) are moved

outside the integral for sufficiently small changes in energy level (ΔE). The density of interface trapped charges is then given by $Q_{it} = -q N_{it} f(E_t)$, where N_{it} , [$Number \times cm^{-2}$] is the trapped interface state density *per unit area* at E_t , represented by an integration of the interface trap density over ΔE :

$$N_{it} = \int_{E_t - \Delta E/2}^{E_t + \Delta E/2} D_{it}(E) dE = D_{it}(E_t) \Delta E. \quad (2)$$

Introducing the intrinsic Fermi level in (1) (E_{is}) and defining $E_{t-i} = E_t - E_{is}$, the occupation probability for an acceptor-type trap level within the band-gap is obtained by [19], [31]

$$\frac{1}{f(E_t)} = 1 + \exp\left(\frac{E_{t-i}}{kT}\right) \exp\left(-\frac{\Psi_s - V_{ch}}{U_T}\right) \quad (3)$$

where $U_T = kT/q$ is the thermal voltage, Ψ_s is the total sweep of the surface potential given by $-(E_{is} - E_f)/q$ and V_{ch} is the shift in quasi Fermi potential along the channel. Notice that the calculations for this single trap energy level can be extended for all the trap energy levels.

The effect of radiation-induced interface charged traps can be linked to TID through some experimental models, which need accurate approaches for the determination of the Si/oxide interface state density. Several techniques such as CV-measurements [32], [33], deep-level transient-spectroscopy technique (DLTS) [34], charge-pumping technique [35], [36], and weak inversion analysis [37] have been proposed for determining the surface states from the transistor behavior. As a matter of fact, the interface trap density can be experimentally expressed by $N_{it} = a_{it} TID^{b_{it}}$, where a_{it} [$cm^{-2} \cdot rad^{-1}$] and b_{it} [-] are the fitting coefficients. Notice that this relationship can be empirically obtained without taking into account all the technological parameter dependencies.

B. General remarks on oxide trapped charges in MOSFET

The generation of electron-hole pairs in the oxide depends on either the local electric field or the ionizing radiation energy. The TID corresponds to the energy absorbed per unit mass and depends strictly on the material. Therefore, in order to include oxide charged traps effects in the characterization of an irradiated device, a relationship between the density of oxide traps and the TID must be established.

In silicon and oxides, it can be assumed that the absorbed energy is wholly used to generate electron-hole pairs. The radiation-induced generation rate of fixed oxide charged traps can be expressed as $GR = g_0 Y(E) (\partial TID / \partial t)$, where the derivative term stands for the dose rate [$rad \cdot s^{-1}$] and g_0 for the total electron-hole pair generation rate. In the case of SiO_2 , g_0 is equal to $7.6 \times 10^{12} cm^{-3} rad^{-1}$ [38]–[40]. Relying on the work done by Dozier et al. [41], [42], the fraction of holes escaping the initial recombination, $Y(E)$, can be calculated by means of experimental model as $Y(E) = [(|E| + E_0) Y_0] / (|E| + E_0)^m$, where $|E|$ is the electric field magnitude, Y_0 is the zero-field yield factor, E_0 is the critical field value, and m moderates the growth rate of the function ($E_0 Y_0 = 0.1 V/cm$ to ensure convergence; $E_0 = 0.55 MV/cm$ and $m = 0.7$ for γ radiation [42]). However, not all electron-hole pairs become active in the device, due to their recombination in the first picoseconds

after generation. This recombination rate depends on many technological process parameters, i.e. oxide thickness, as well as on the applied electric field. Therefore, once integrating GR , radiation dependent density of trapped charge within the oxide can be obtained by $N_{ot} = g_0 TID \cdot Y(E)$. It is worthy to mention that even though the total trapped charge within the oxide is proportional to TID, the model is not valid anymore for high TID (in the order of several hundreds of Mrad). In case of high doses, as a matter of fact, saturation of oxide and interface trap occurs, which is not accounted for in [2], [17], [18].

IV. ELECTROSTATICS IN DOUBLE-GATE MOSFETS

In this work, an n -type long-channel symmetric double-gate MOSFET (see Fig. 1) is investigated. Here L_G and W are the gate length and width, T_{sc} is the semiconductor thickness, and t_{ox} is the gate oxide thickness. Neglecting the hole density in silicon, the electrostatic potential $\Psi(x)$ profile is given from the 1D-Poisson equation, where x is the orientation across the channel. Similarly to [8], merging the Poisson relationship with the non-degenerate Boltzmann statistics and integrating along x yields to the electric field across the silicon film:

$$E^2(x) = \frac{2q n_i U_T}{\epsilon_{si}} \left[\exp\left(\frac{\Psi(x) - V_{ch}}{U_T}\right) + C \right], \quad (4)$$

where n_i and ϵ_{si} are the intrinsic carrier density and the permittivity of silicon and C is an integration constant explicitly formulated in [8] and expressed in terms of mobile charge density $C = Q_m / (q n_i T_{sc})$. Notice that Q_m , the mobile charge density per unit area, can be linked to the surface potential by $E_s^2 = (Q_m / 2 \epsilon_{si})^2$, where E_s is the electric field at Si/oxide interface. Therefore, we can write:

$$\Psi_s - V_{ch} = U_T \ln \left(\frac{Q_m^2}{8 \epsilon_{si} q U_T n_i} - \frac{Q_m}{q n_i T_{sc}} \right). \quad (5)$$

Due to ionizing radiation, oxide traps (located inside the gate dielectric and in external isolation structures) are positively charged by holes in both n - and p MOSFETs, causing a negative threshold voltage shift and effectively modifying their electrical characteristics. Additionally, they can invert the channel portion close to the Si/oxide interface, causing a leakage current to flow even in the *off*-state condition.

Consequently, oxide-trap and interface-trap charges compensate each other for n -channel and sum up for p -channel transistors (given that the net trapped charge is given by $Q_T = Q_{ot} + Q_{it}$). The charge contribution from radiation-induced charged traps is incorporated through the boundary condition on the normal component of the displacement vector at the Si/oxide interface. It should be remarked that the positively trapped charges in the spacer and STI oxide have a strong effect on the electrical behavior of the transistor. However, it should be emphasized that, to simplify the analysis, Q_{ot} actually corresponds to an equivalent oxide charge density accounting for all the oxide charge traps, located inside the gate dielectric as well as in external isolation structures (including STI). In other words, Q_{ot} is representing an equivalent charge located in the gate oxide that produces the same change in the electrical field with the charges located not only in the

gate oxide but also located in the STI. It is also assumed that this equivalent charge is located at the Si/oxide interface. Additionally, it is worth mentioning that, here we focus on the relation between the electrical behavior of the device and the charge traps (Q_{ot} and Q_{it}) and not on the impact of TID on Q_{ot} and Q_{it} which indeed depends on the physical gate oxide and STI thicknesses.

Therefore, the boundary conditions arising from the continuity of displacement vector at the interface must satisfy $Q_T = D_{si} - D_{ox}$. Moreover, the semiconductor charge density is also related to the potential drop across the gate insulators by

$$-Q_m/2 - C_{ox}(V_{GS} - \Delta\Phi_{ms} - \Psi_s) = Q_{it} + Q_{ot}, \quad (6)$$

where V_{GS} denotes the gate voltage and $\Delta\Phi_{ms}$ is the work function difference between the gate electrode and the intrinsic silicon. Then, the combination of (5) and (6) yields:

$$V = V_{GS} - \Delta\Phi_{ms} - V_{ch} = -\frac{Q_m + 2(Q_{it} + Q_{ot})}{2C_{ox}} + U_T \ln \theta \quad (7)$$

$$\theta = \frac{Q_m^2}{8\epsilon_{si}qU_Tn_i} - \frac{Q_m}{qn_iT_{sc}}. \quad (8)$$

Next, the combination of (3), (5), (7) and (8) gives the general charge-based relationship between potential and charges including both oxide and interface charged traps

$$V = -\frac{2Q_{ot} + Q_m}{2C_{ox}} + U_T \ln(\theta) + \frac{qN_{it}}{(1 + \eta\theta^{-1})C_{ox}} \quad (9)$$

where $\eta = \exp(E_{t-i}/kT)$. Notice that the mobile charge density Q_m is simply twice the gate charge density, $Q_m = -2Q_G$. It should be remarked that imposing $Q_T = 0$ brings back to the general charge-based relationship derived in [8]. To illustrate and appraise the validity of this model, the mobile charge density versus the effective gate voltage in lightly doped double-gate nMOSFET, as obtained from TCAD simulations and from the model, are plotted in Fig. 3 for different values of oxide and interface charged traps. The doping density of silicon body used in TCAD simulations is 10^{15} cm^{-3} . Lines and symbols hold for the analytical model and TCAD simulations, respectively. The validity is demonstrated in the linear and logarithmic representations in full agreement with TCAD simulations.

V. DERIVATION OF THE CURRENT

From now on, it is assumed that the current density can be calculated adopting the classical drift-diffusion transportation which neglects quantum-mechanical effects due to carrier confinement. In this case, the current is given by $I_{DS} = -\mu W/L_G \int_0^{V_{DS}} Q_m dV_{ch}$, where the carrier mobility, μ , is assumed constant along the channel. This work neglects the tunneling current through the gate oxide and the mobility degradation due to interface charged traps. Those effects should obviously be accounted for in the full predictive compact model after the validation of the long channel model. The complex relationship between the charge density and the potential, as

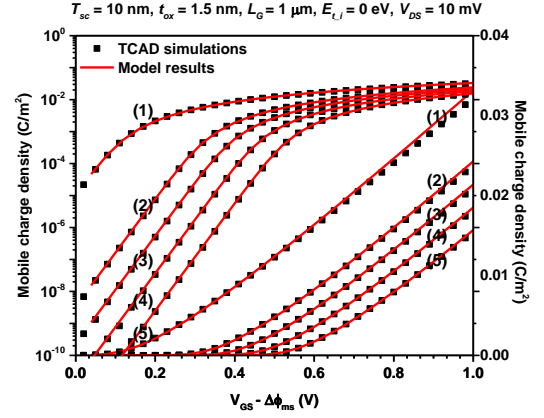


Fig. 3: Mobile charge density (Q_m) versus $V_{GS} - \Delta\Phi_{ms}$ calculated from analytical model and TCAD simulations in linear and log scale for different values of N_{ot} and N_{it} . (1): $N_{it}=10^{10} \text{ cm}^{-2}$, $N_{ot}=5 \times 10^{12} \text{ cm}^{-2}$ (2): $N_{it}=10^{10} \text{ cm}^{-2}$, $N_{ot}=2 \times 10^{12} \text{ cm}^{-2}$ (3): $N_{it}=0 \text{ cm}^{-2}$, $N_{ot}=10^{12} \text{ cm}^{-2}$ (4): $N_{it}=N_{ot} = 0 \text{ cm}^{-2}$ (5): $N_{it}=10^{12} \text{ cm}^{-2}$, $N_{ot}=0 \text{ cm}^{-2}$.

obtained from the general charge-potential dependence, does not lead to a simple analytical expression for the current;

$$I_{DS} = \frac{W\mu}{L_G} \left\{ -\frac{Q_m^2}{4C_{ox}} + U_T [\alpha \ln(Q_m - \alpha) + 2Q_m] + \frac{qN_{it}\eta}{C_{ox}} \left[\frac{2b\sqrt{a}}{\xi} \tanh^{-1}\left(\frac{a-2Q_m b}{\xi\sqrt{a}}\right) - \frac{abQ_m}{bQ_m^2 - aQ_m + ab\eta} \right] \right\} \Bigg|_S^D \quad (10)$$

where $C_{si} = \epsilon_{si}/T_{sc}$ is the silicon layer capacitance, $\xi = \sqrt{a - 4\eta b^2}$, $a = 8\epsilon_{si}qU_Tn_i$, $\alpha = 8C_{si}U_T$, and $b = qn_iT_{sc}$. Concerning the current estimation along the channel, a different set of relationships is expected with respect to [8], since the charge-voltage dependence is modified by appending the trap-related term. However, due to the complexity of such relationship, the proposal is to rely on the same expression for the current proposed in [8] without including the effect of interface trapped charges ($Q_{it} = 0$), only depending on the mobile charge density evaluated at source and drain (see [19]). Therefore, the mobile charge-densities at source and drain are given by (9) and the total drain-source current can be estimated as in [8],

$$I_{DS} = \frac{W\mu}{L_G} \left\{ -\frac{Q_m^2}{4C_{ox}} + U_T [\alpha \ln(Q_m - \alpha) + 2Q_m] \right\} \Bigg|_S^D, \quad (11)$$

The drain current has been calculated by solving (9) numerically for the mobile charge densities at source and drain and introducing it into (11) in the linear and saturation regions ($V_{DS} = 10 \text{ mV}$ and 0.5 V , respectively) and for different values of the trap energy level parameter E_{t-i} . The calculated values are compared to the results, obtained from the 2D TCAD simulations using the same parameters in Figs. 4a and 4b, resulting in an excellent agreement.

VI. CHARGED-TRAPS INDUCED GATE CAPACITANCE

In order to validate the proposed model, it is important to compare the TCAD simulation results with the well-established theoretical model of the intrinsic gate capacitance. In fact, the

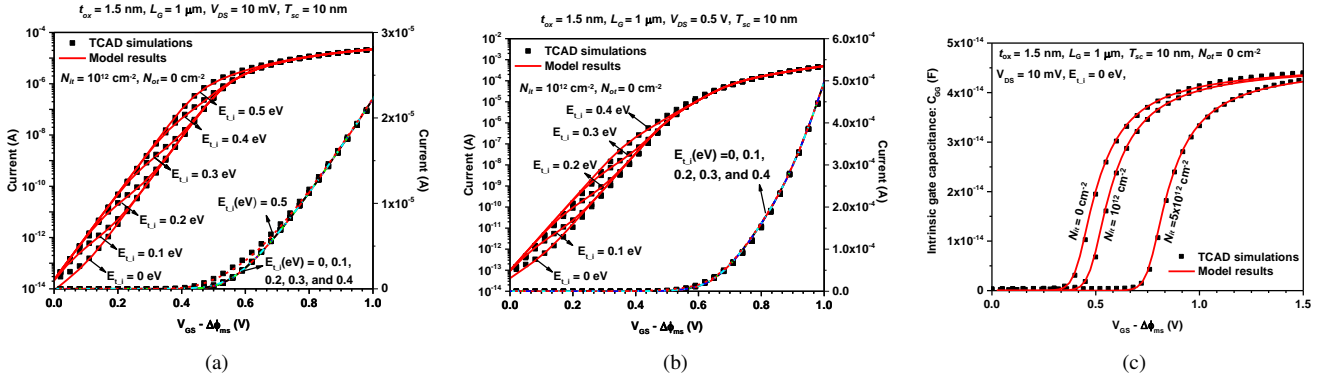


Fig. 4: a) and b) I_{DS} with respect to $V_{GS} - \Delta\Phi_{ms}$ calculated from analytical model (lines) and TCAD simulations (markers) shown in linear and log scale for different trap energy levels in double-gate MOSFET in linear and saturation regions respectively ($\mu = 0.1417$ m 2 /Vs), $N_{it} = 10^{12}$ cm $^{-2}$, and $N_{ot} = 0$ cm $^{-2}$. c) C_{GG} with respect to $V_{GS} - \Delta\Phi_{ms}$ calculated from the analytical model (lines) and TCAD simulations (markers) for different values of charged trap energy level in double-gate MOSFET.

effects of oxide fixed charges and interface trapped charges on the capacitance change as a function of the bias voltage has been well documented from a theoretical point of view [40]. In a MOS structure, the capacitance is completely determined by the variation of the charge with respect to the applied voltage. This charge can be decomposed into two terms, depending on the density of charge placed in the semiconductor and in the surface states. Therefore, the interface charged-trap layer is modulated by the gate potential and contributes to the total intrinsic gate capacitance ($C_{GG}/WL_G = -\partial Q_m/\partial V_{GS}$), the latter proceeding from the bare derivative of the mobile charge density in (9) with respect to generic potentials. This leads to

$$\frac{C_{GG}}{WL_G} = \left[\frac{1}{2C_{ox}} - \frac{U_T \theta'}{\theta} - \frac{\theta'}{\theta^2} \frac{q N_{it} \eta}{C_{ox} (1 + \eta \theta^{-1})^2} \right]^{-1}, \quad (12)$$

$$\theta' = \frac{Q_m}{4 \epsilon_{si} q U_T n_i} - \frac{1}{q n_i T_{sc}}. \quad (13)$$

The intrinsic gate capacitance as a function of effective the gate voltage is then depicted in Fig. 4c for the analytical model and compared to the TCAD simulation results, including interface charged traps. Again, an excellent agreement is obtained in all operation modes and for all values of N_{it} .

VII. TID EFFECTS ON DC CHARACTERISTICS

A. Threshold voltage variation

As discussed, oxide trapped charges (Q_{ot}) effectively modify the electrical characteristics of an irradiated device. This modification mainly manifests as a negative threshold voltage shift (ΔV_{th}^{ot}) which can be simply obtained from $-Q_{ot}/C_{ox}$. This expression establishes the relation between the threshold voltage shift and the equivalent charge density in the oxides that could further link to the corresponding TID.

In contrast, interface charged traps increase the threshold voltage of n - and decrease that of p MOSFETs. An analytical model is derived from (9) to calculate the positive threshold voltage shift induced by interface charged traps (ΔV_{th}^{it}). Keeping the mobile charge density constant and subtracting (9) from itself with $Q_{it} = Q_{ot} = 0$, the difference of the gate

voltages gives insights into the Q_{it} -induced threshold voltage shift:

$$\Delta V_{GS}^{it}(V_{GS}) = \frac{q N_{it}}{(1 + \eta \theta^{-1}) C_{ox}}. \quad (14)$$

where θ is derived from (7) with $Q_{it} = Q_{ot} = 0$:

$$\theta = \exp \left[\frac{V_{GS} - \Delta\Phi_{ms} - V_{ch} + Q_m/(2C_{ox})}{U_T} \right]. \quad (15)$$

To derive an explicit solution for ΔV_{th}^{it} , the subthreshold regime is focused on. Thus the term $Q_m/2C_{ox}$ is neglected and the expression (15) is simplified to

$$\theta \approx \exp \left(\frac{V_{GS} - \Delta\Phi_{ms} - V_{ch}}{U_T} \right). \quad (16)$$

It should be remarked that when the device is in the fully depletion mode, θ tends to zero that pushes (14) to zero, too. Nevertheless, above the threshold, the term $\eta \theta^{-1}$ in (14) is close to zero (θ becomes infinite), leading to a common analytical expression for ΔV_{GS} . Figs. 5a and 5b present both the complete analytical solution and the explicit solution developed in the subthreshold region for the gate voltage shift as a function of the effective gate potential, which corresponds to the same mobile charge density in linear operation ($V_{ch} = 10$ mV) at different values of N_{it} and E_{t-i} . The agreement between the analytical solution and the explicit derivation is excellent in all operation modes from the depletion region to above the threshold.

The analytical expression for ΔV_{GS} above the threshold presents the explicit solution for Q_{it} -induced threshold voltage shift in linear mode as follows $\Delta V_{th}^{it} = q N_{it}/C_{ox}$. It depends only on the interface trap density. The V_{th}^{it} is extracted above the threshold region from 5a and 5b, and plotted in 5c as a function of N_{it} for different values of E_{t-i} . It is observed from 5a, 5b, and 5c that E_{t-i} does not influence the values of V_{th}^{it} but shifting ΔV_{th}^{it} with respect to $V_{GS} - \Delta\Phi_{ms}$. This is due to the term $\eta = \exp[E_{t-i}/(kT)]$ that embodies the trap energy level into the threshold voltage shift. The shifting behavior is only in the transition region from subthreshold to above threshold. It should be mentioned that neglecting $Q_m/2C_{ox}$ for a higher value of E_{t-i} (i.e., 0.4 eV) will slightly overestimate

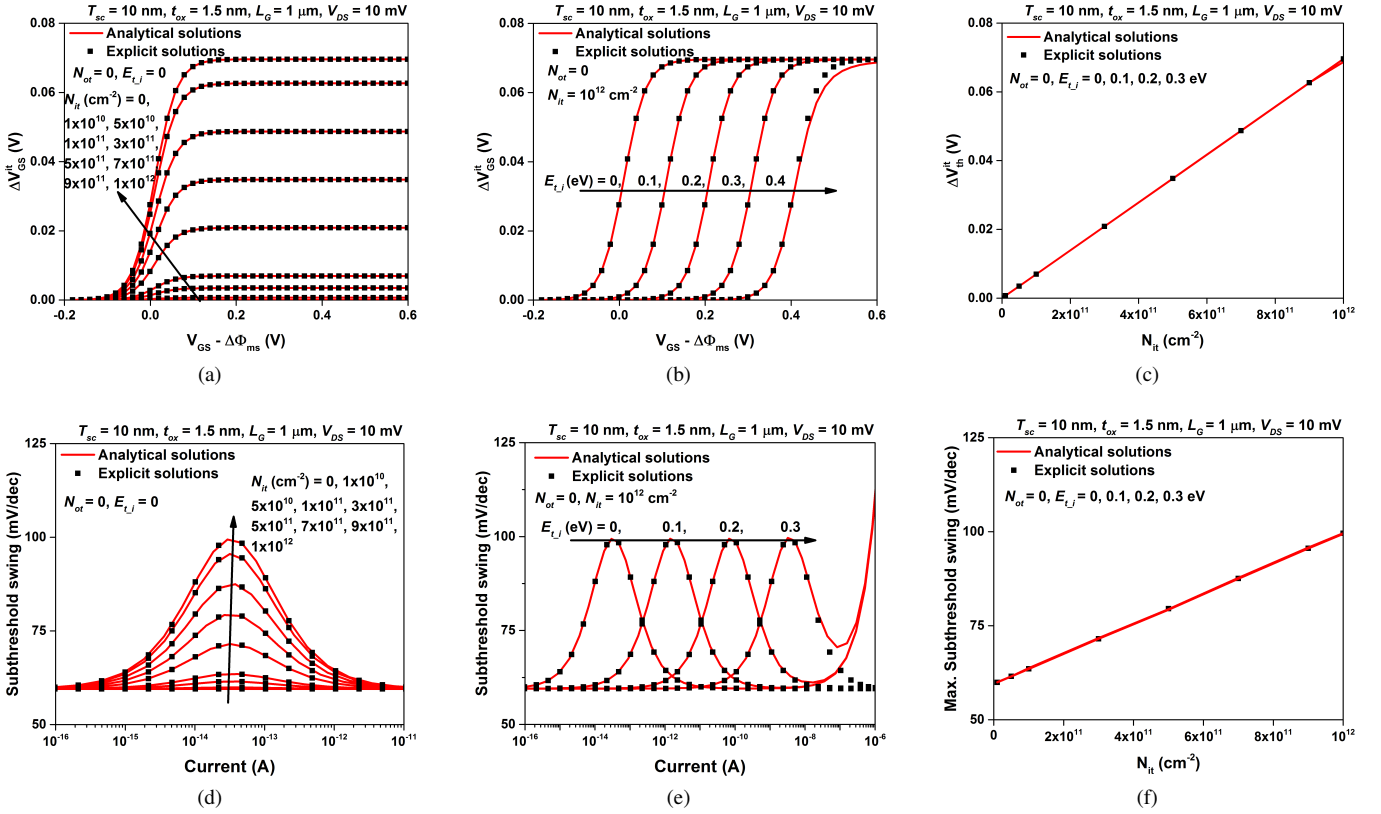


Fig. 5: a) Shift in the V_{GS} due to the interface charged traps with respect to $V_{GS} - \Delta\Phi_{ms}$, while the mobile charge density remains constant. The shift in threshold voltage (ΔV_{th}^{it}) versus N_{it} can be obtained from this figure when the device works above threshold (analytical model: lines and explicit solution: markers). b) The gate voltage shift with respect to $V_{GS} - \Delta\Phi_{ms}$ for different E_{t-i} while the mobile charge density is constant and $N_{it} = 10^{12} \text{ cm}^{-2}$ (analytical model: lines and explicit solution: markers). c) Shift in threshold voltage (ΔV_{th}^{it}) versus N_{it} , in linear mode of operation, for different interface trap energy levels (analytical model: lines and explicit solution: markers). d) The subthreshold swing in linear operation mode with respect to the total drain current for different N_{it} while $E_{t-i} = 0$ (analytical model: lines and explicit solution: markers). e) The subthreshold swing in linear region with respect to the total drain current for different E_{t-i} while $N_{it} = 10^{12} \text{ cm}^{-2}$ (analytical model: lines and explicit solution: markers). f) The maximum subthreshold degradation in linear region of operation versus N_{it} for different values of E_{t-i} (analytical model: lines and explicit solution: markers).

ΔV_{th}^{it} , as seen in 5b. However, this explicit formulation still gives predictive and reliable information about Q_{it} -induced threshold voltage shift.

B. Subthreshold swing degradation

The primary effect of interface charged traps is an increase in the subthreshold swing (SS). Relying on the drift-diffusion transport model for a low V_{DS} ($Q_{ms} \approx Q_{md}$, where Q_{ms} and Q_{md} are the local mobile charge densities at the source and the drain, respectively), the subthreshold swing is expressed as

$$\frac{1}{SS} = \frac{\partial}{\partial V_{GS}} \text{Log} \left(\frac{W}{L_G} \mu Q_m V_{DS} \right) = \frac{1}{Q_m \ln(10)} \frac{\partial Q_m}{\partial V_{GS}}. \quad (17)$$

By neglecting the term $Q_m/2C_{ox}$, $\partial V_{GS}/\partial Q_m$ derived from (9) is given as

$$\frac{\partial V_{GS}}{\partial Q_m} = \frac{U_T \theta'}{\theta} + \frac{q N_{it} \eta \theta'}{C_{ox} (\eta + \theta)^2}. \quad (18)$$

With mathematical manipulations (see Appendix-A), the subthreshold swing is obtained as

$$SS = \ln(10) \left[U_T + \frac{q N_{it}}{C_{ox} (\sqrt{\eta/\theta} + \sqrt{\theta/\eta})^2} \right]. \quad (19)$$

Relying on (19), the maximum subthreshold swing, SS_{max} , is readily reached when η equals to θ :

$$SS_{max} = U_T \ln(10) \left(1 + \frac{q N_{it}}{4U_T C_{ox}} \right) \quad (20)$$

Next, imposing $\eta = \theta = \exp(E_{t-i}/kT)$ in (9) with full-depletion approximation in subthreshold region ($Q_m \approx 0$), a corresponding value of V_{GS} for SS_{max} is obtained by

$$V_{GS}^{max} - \Delta\Phi_{ms} = \frac{E_{t-i}}{q} + V_{ch} + \frac{q N_{it}}{2C_{ox}} - \frac{Q_{ot}}{C_{ox}}. \quad (21)$$

The location of SS_{max} , V_{GS}^{max} , depends on the density of interface traps and the difference between the charged-trap energy level and the intrinsic Fermi level. However, SS_{max} is only relevant to the density of interface traps. This can be seen in Figs. 5d and 5e including both the analytical solution (17) and the explicit solution (19) as a function of the drain current for different values of N_{it} and E_{t-i} . 5d and 5e also evidence the excellent agreement between the analytical solution and the explicit derivation. The maximum SS from 5d and 5e is plotted in Fig. 5f as a function of N_{it} . For different values of E_{t-i} , the curves are placed entirely on the top of each other.

VIII. CONTINUOUS TRAP ENERGY LEVEL DISTRIBUTION

So far, we considered discrete energy levels for interface traps (monovalent states without energy broadening). These are indeed very instructive, but not representative of real devices which indicate a continuous trap energy level distribution.

A. Discretized summation for interface trap level distribution

In Section VII-B, although we restrict the derivation to monovalent trapping states, we could derive TID-induced degradation in SS and also the threshold voltage shift due to TID effects. However, non-uniform and continuous trap energy level distribution can be approximated as a discretized summation for energy broadening of interface trap energy level. Therefore,

$$Q_{it} = \sum_{i=1}^n -qN_{it,i}f(E_{t,i}), \quad (22)$$

where $N_{it,i}$ is the interface trap density at $E = E_{t,i}$. This similarly leads to a general charge-based model including discretized summation of continuous trap energy level distribution:

$$V = -\frac{2Q_{ot} + Q_m}{2C_{ox}} + U_T \ln(\theta) + \sum_{i=1}^n \frac{qN_{it,i}}{(1 + \eta_i \theta^{-1})C_{ox}}. \quad (23)$$

where $\eta_i = \exp(E_{t-i,i}/kT)$ and $E_{t-i,i}$ represents the i^{th} -trap energy level. Now, regarding the influence of the continuous trap level distribution, SS can be similarly expressed as follows

$$SS = \ln(10) \left[U_T + \sum_{i=1}^n \frac{qN_{it,i}}{C_{ox}(\sqrt{\eta_i/\theta} + \sqrt{\theta/\eta_i})^2} \right]. \quad (24)$$

Moreover, since the derivation performed in VII has considered a single trap energy level and has been confirmed by numerical TCAD simulations, the extension of the model for a discretized summation for interface trap level distribution can be considered valid as well, without the need of dedicated TCAD simulations.

B. Uniform distribution of interface trap density

In most of the previous studies, i.e. [10], in order to obtain an analytical solution to (1) for continuous interface trap density, the trap occupation probability is assumed to be unity and the interface-state density is approximated by a continuous and uniform distribution of density of *occupied* interface states per unit area per unit energy (eV), D_{it} , between electron quasi Fermi ($E_f - qV_{ch}$) and intrinsic (E_i) levels. Therefore, due to these assumptions introduced for derivation simplicity, the interface trap density can be expressed as

$$Q_{it} = -qD_{it}(E_f - E_i - qV_{ch}) = -q^2D_{it}(\Psi_s - V_{ch}). \quad (25)$$

Relying on previous works, the estimated value of D_{it} obtained from measurements is in the same order of magnitude as $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Next, combining (6) with (25) yields to a closed-form expression of Q_{it} with respect to Q_m . Inserting Q_{it} into (7) allows obtaining a new charge-based expression useful for compact modeling purposes:

$$V = -\frac{2Q_{ot} + Q_m}{2C_{ox}} + U_T \ln(\theta) \left[1 + \frac{q^2D_{it}}{C_{ox}} \right]. \quad (26)$$

This simplified charge-based relation enables obtaining the mobile charge density along the channel and drain to source current in linear and saturation regions, validated with TCAD simulations and plotted in Fig.6. Similarly, to analyze the reliability degradation due to the total ionizing effects, (11) is used to calculate analytically the total drain current through (26). Subtracting (26) from (26) when $Q_{it}=Q_{ot}=0$, the shift in threshold voltage, where Q_m remains constant, is readily linked to the equivalent oxide and interface trapped charge in linear mode operation through:

$$\Delta V_{th} = \Delta V_{th}^{ot} + \Delta V_{th}^{it} = \frac{1}{C_{ox}} [-Q_{ot} + q^2D_{it}U_T \ln(\theta)]. \quad (27)$$

Assuming that in subthreshold region, $Q_m/(2C_{ox})$ is negligible, (27) is simplified to

$$\Delta V_{th} \approx \frac{1}{C_{ox}} [-Q_{ot} + q^2D_{it}(V_{GS} + V_{ch} - \Delta\phi_{ms})]. \quad (28)$$

Additionally, combining (17) with (26), the subthreshold swing degradation due to Q_{it} is directly linked to the density of states

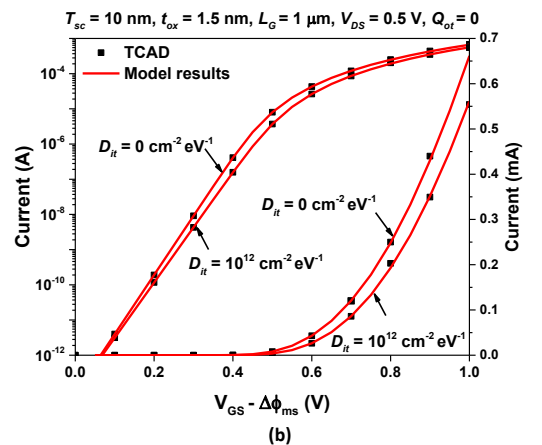
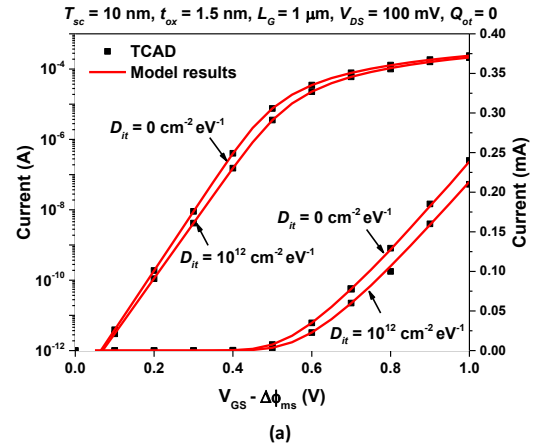


Fig. 6: I_{DS} with respect to $V_{GS} - \Delta\Phi_{ms}$ calculated from analytical model for uniform distribution of interface trap density (lines) and TCAD simulations (markers) shown in linear and log scale in double-gate MOSFET in linear (a) and saturation (b) regions respectively ($\mu = 0.1417 \text{ m}^2/\text{Vs}$), $D_{it} = 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, and $Q_{ot} = 0 \text{ cm}^{-2}$.

uniformly distributed over energy:

$$SS = U_T \ln(10) \left(1 + \frac{q^2 D_{it}}{C_{ox}} \right). \quad (29)$$

It should be remarked that assuming single-level interface traps, SS degradation happens only in a certain region of the gate voltage and this can be shifted by the trap energy level. Although (20) gives the maximum degradation over V_{GS} due to TID, (29) makes the model more representative for real cases to predict the subthreshold swing degradation, assuming a continuous and uniform interface trap density over energy.

Finally, it should be remarked that the developed charge-based model to include TID and aging effects can be easily extended to short channel double-gate FETs by using the proposed model in [43], which is the generalization of charge-based long channel model [8] to short channel undoped double-gate FinFET. On the other hand, the proposed analysis can be easily applied in advanced field effect devices, i.e., nanowire junctionless FETs [44]–[49].

IX. CONCLUSION

A charge-based model for interface and oxide trapped charges in undoped/low-doped symmetric double-gate MOSFET is developed, proposing a physical one-dimensional model. This approach incorporates the impact of radiation damage and TID-induced degradation on DC electrical behavior of double-gate MOSFET. A detailed study of the interface charged traps and oxides trapped charge distributions and their influence on device performance is carried out. Regarding the interface charged traps, monovalent state, single trap energy level without energy broadening, and also uniform/non-uniform continuous trap energy level distributions are considered to model the TID-induced degradation. In particular, the subthreshold swing degradation and the threshold voltage shift have been modeled by means of explicit expressions. To validate the approach in describing the impact of radiation-induced interface trapped charges, the simple analytical model is successfully compared to the results obtained from two dimensional TCAD simulations for different interface charged trap densities. This verification is obtained through the comparison of model calculations and TCAD extractions of mobile charge-density and drain currents as a function of the terminal voltages and the defect densities. This results in good agreement in all regions of operation, from deep depletion to strong inversion and from linear to saturated regimes, as confirmed from a detailed comparison with the TCAD numerical simulations. No empirical parameters have been used, confirming the safe physical roots of the core model.

APPENDIX A

DERIVATION OF THE EXPLICIT SOLUTION FOR SS

Combining (17) and (18), we obtain the full analytical expression for SS :

$$SS = \frac{\ln(10)Q_m\theta'}{\theta} \left[U_T + \frac{q N_{it} \eta \theta}{C_{ox}(\eta + \theta)^2} \right]. \quad (30)$$

The term $Q_m\theta'/\theta$ could be rewritten as below by replacing θ' and θ with their full expressions (8) and (13):

$$\frac{Q_m\theta'}{\theta} = 1 + \frac{1}{1 - 8\epsilon_{si} U_T / (T_{sc} Q_m)}. \quad (31)$$

The term $8\epsilon_{si} U_T / T_{sc}$ for the studied device equals to 0.0021 C/cm^2 . Since SS is a critical parameter in the subthreshold region at which Q_m is much smaller, the second term of (31) is close to 0. Neglecting this term, we get the explicit solution for SS as expressed in (19).

REFERENCES

- [1] Chun-Min Zhang, Farzan Jazaeri, Alessandro Pezzotta, Claudio Bruschini, Giulio Borghello, Federico Faccio, Serena Mattiazzo, Andrea Baschiroto, and Christian Enz, "Characterization of gigarad total ionizing dose and annealing effects on 28 nm bulk mosfets," *IEEE Transactions on Nuclear Science*, vol. PP, no. 99, pp. 1–1, 2017.
- [2] C.-M. Zhang, F. Jazaeri, A. Pezzotta, C. Bruschini, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschiroto, and C. Enz, "Total ionizing dose effects on analog performance of 28 nm bulk mosfets," in *2017 ESSDERC Proceedings*. IEEE, 2017.
- [3] H. Hughes and R. Giroux, "Space radiation affects MOSFETs," *Electronics*, vol. 37, no. , pp. 58–60, Dec 1964.
- [4] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, "Radiation effects in MOS oxides," *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1833–1853, 2008.
- [5] F. Jazaeri, A. Pezzotta, and C. Enz, "Free carrier mobility extraction in fets," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 1–5, 2017.
- [6] F. Jazaeri and J.-M. Sallese, "Carrier mobility extraction methodology in junctionless and inversion-mode fets," *IEEE Transactions on Electron Devices*, vol. 62, no. 10, pp. 3373–3378, Oct 2015.
- [7] J.-T. Park and J. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2222–2229, Dec 2002.
- [8] J.-M. Sallese, F. Krummenacher, F. Prgaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," *Solid-State Electronics*, vol. 49, no. 3, pp. 485–489, 2005.
- [9] C. Enz and E. Vittoz, *Charge-based MOS transistor modeling: the EKV model for low-power and RF IC design*. John Wiley & Sons, 2006.
- [10] I. S. Esqueda, H. J. Barnaby, and M. P. King, "Compact Modeling of Total Ionizing Dose and Aging Effects in MOS Technologies," *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1501–1515, Aug 2015.
- [11] R. Hughes, "Hole mobility and transport in thin SiO₂ films," *Applied Physics Letters*, vol. 26, no. 8, pp. 436–438, 1975.
- [12] Hughes, R.C., "Charge-Carrier Transport Phenomena in Amorphous SiO₂: Direct Measurement of the Drift Mobility and Lifetime," *Physical Review Letters*, vol. 30, no. 26, p. 1333, 1973.
- [13] Fleetwood, D.M., "Border traps in MOS devices," *IEEE transactions on nuclear science*, vol. 39, no. 2, pp. 269–271, 1992.
- [14] H. E. Boesch, F. B. McLean, J. M. Benedetto, J. M. McGarrity, and W. E. Bailey, "Saturation of threshold voltage shift in MOSFET's at high total dose," *IEEE Transactions on Nuclear Science*, vol. 33, pp. 1191–1197, Dec. 1986.
- [15] S. N. Rashkeev, C. R. Cirba, D. M. Fleetwood, R. D. Schrimpf, S. C. Witzczak, A. Michez, and S. T. Pantelides, "Physical model for enhanced interface-trap formation at low dose rates," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 2650–2655, 2002.
- [16] P. Lenahan and J. Conley, "A comprehensive physically based predictive model for radiation damage in MOS systems," *IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2413–2423, Dec 1998.
- [17] A. Pezzotta, C.-M. Zhang, F. Jazaeri, C. Bruschini, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschiroto, and C. Enz, "Impact of gigarad ionizing dose on 28nm bulk mosfets for future hi-lhc," in *2016 ESSDERC Proceedings*. IEEE, 2016.
- [18] C.-M. Zhang, F. Jazaeri, A. Pezzotta, C. Bruschini, G. Borghello, F. Faccio, S. Mattiazzo, A. Baschiroto, and C. Enz, "Gigarad total ionizing dose and post-irradiation effects on 28 nm bulk mosfets," in *2016 Nuclear Science Symposium Proceedings*. IEEE, 2016.

- [19] A. Yesayan, F. Jazaeri, and J.-M. Sallese, "Charge-Based Modeling of Double-Gate and Nanowire Junctionless FETs Including Interface-Trapped Charges," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 1368–1374, 2016.
- [20] J. P. Colinge and A. Terao, "Effects of total-dose irradiation on gate-all-around (gaa) devices," *IEEE Transactions on Nuclear Science*, vol. 40, no. 2, pp. 78–82, Apr 1993.
- [21] J. P. Colinge, *Gate-All-Around Technology for Harsh Environment Applications*. Dordrecht: Springer Netherlands, 2002, pp. 167–188.
- [22] C. R. Cirba, S. Cristoloveanu, R. D. Schrimpf and K. F. Galloway, "Radiation hardness of double-gate ultra-thin soi mosfets," *The Electrochemical Society*, 1989.
- [23] A. Dubey, A. Singh, R. Narang, M. Saxena, and M. Gupta, "Modeling and simulation of junctionless double gate radiation sensitive fet (radfet) dosimeter," *IEEE Transactions on Nanotechnology*, vol. PP, no. 99, pp. 1–1, 2017.
- [24] V. Ferlet-Cavrois, P. Paillet, and O. Faynot, *Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs*. Boston, MA: Springer US, 2008, pp. 257–291.
- [25] B. Jun, H. D. Xiong, A. L. Sternberg, C. R. Cirba, D. Chen, R. D. Schrimpf, D. M. Fleetwood, J. R. Schwank, and S. Cristoloveanu, "Total dose effects on double gate fully depleted soi mosfets," *IEEE Transactions on Nuclear Science*, vol. 51, no. 6, pp. 3767–3772, Dec 2004.
- [26] T. R. Oldham and F. B. McLean, "Total ionizing dose effects in MOS oxides and devices," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 483–499, June 2003.
- [27] A. H. Johnston, R. T. Swimm, G. R. Allen, and T. F. Miyahira, "Total Dose Effects in CMOS Trench Isolation Regions," *IEEE Transactions on Nuclear Science*, vol. 56, no. 4, pp. 1941–1949, Aug 2009.
- [28] G. Chen, K. Y. Chuah, M. F. Li, D. S. H. Chan, C. H. Ang, J. Z. Zheng, Y. Jin, and D. L. Kwong, "Dynamic NBTI of PMOS transistors and its impact on device lifetime," in *Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International*, March 2003, pp. 196–202.
- [29] F. Jazaeri and J.-M. Sallese, *Modeling Nanowire and Double-Gate Junctionless Field-Effect Transistors*. Cambridge University Press, 2018.
- [30] S. M. Sze and K. K. Ng, "Metal-insulator-semiconductor capacitors," *Physics of Semiconductor Devices, 3rd ed. Hoboken, NJ, USA: Wiley*, pp. 214–215, 2007.
- [31] C. L. Wilson and J. L. Blue, "Modeling of Ionizing Radiation Effects in Short-Channel MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 29, no. 6, pp. 1676–1680, Dec 1982.
- [32] C. N. Berglund, "Surface states at steam-grown silicon-silicon dioxide interfaces," *IEEE Transactions on Electron Devices*, vol. ED-13, no. 10, pp. 701–705, Oct 1966.
- [33] J. Koomen, "Interface studies of the MOS-structure by transfer-admittance measurements," *Solid-State Electronics*, vol. 17, no. 4, pp. 321–328, 1974.
- [34] D. V. Lang, "Deep-level transient spectroscopy: A new method to characterize traps in semiconductors," *Journal of Applied Physics*, vol. 45, no. 7, pp. 3023–3032, 1974.
- [35] J. S. Brugler and P. G. A. Jespers, "Charge pumping in MOS devices," *IEEE Transactions on Electron Devices*, vol. 16, no. 3, pp. 297–302, Mar 1969.
- [36] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Transactions on Electron Devices*, vol. 31, no. 1, pp. 42–53, Jan 1984.
- [37] J. Koomen, "Investigation of the MOST channel conductance in weak inversion," *Solid-State Electronics*, vol. 16, no. 7, pp. 801–810, 1973.
- [38] McLean, F.B., Boesch, H.E. Jr., Oldham, T.R., "Electron-hole generation, transport and trapping in sio₂," 1989.
- [39] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, "Radiation effects in mos oxides," *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1833–1853, Aug 2008.
- [40] P. Fernandez-Martinez, I. Corts, S. Hidalgo, D. Flores, and F. R. Palomo, "Simulation of Total Ionising Dose in MOS capacitors," in *Proceedings of the 8th Spanish Conference on Electron Devices, CDE'2011*, Feb 2011, pp. 1–4.
- [41] C. M. Dozier, D. M. Fleetwood, D. B. Brown, and P. S. Winokur, "An evaluation of low-energy X-ray and cobalt-60 irradiations of MOS transistors," *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, pp. 1535–1539, 1987.
- [42] P. Paillet, J. L. Touron, J. L. Leray, C. Cirba, and A. Michez, "Simulation of multi-level radiation-induced charge trapping and thermally activated phenomena in SiO₂," *IEEE Transactions on Nuclear Science*, vol. 45, no. 3Pt3, pp. 1379–1384, 1998.
- [43] A. Yesayan, F. Prgaldiny, N. Chevillon, C. Lallement, and J.-M. Sallese, "Physics-based compact model for ultra-scaled finfets," *Solid-State Electronics*, vol. 62, no. 1, pp. 165 – 173, 2011.
- [44] F. Jazaeri, L. Barbut, and J. M. Sallese, "Generalized charge-based model of double-gate junctionless fets, including inversion," *IEEE Transactions on Electron Devices*, vol. 61, no. 10, pp. 3553–3557, Oct 2014.
- [45] F. Jazaeri and L. Barbut and J. M. Sallese, "Modeling asymmetric operation in double-gate junctionless fets by means of symmetric devices," *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp. 3962–3970, Dec 2014.
- [46] F. Jazaeri, L. Barbut, A. Koukab, and J.-M. Sallese, "Analytical model for ultra-thin body junctionless symmetric double gate mosfets in subthreshold regime," *Solid-State Electronics*, vol. 82, no. Supplement C, pp. 103 – 110, 2013.
- [47] F. Jazaeri, L. Barbut, and J. M. Sallese, "Trans-capacitance modeling in junctionless symmetric double-gate mosfets," *IEEE Transactions on Electron Devices*, vol. 60, no. 12, pp. 4034–4040, Dec 2013.
- [48] F. Jazaeri, L. Barbut, and J.-M. Sallese, "Trans-capacitance modeling in junctionless gate-all-around nanowire fets," *Solid-State Electronics*, vol. 96, no. Supplement C, pp. 34 – 37, 2014.
- [49] F. Jazaeri, L. Barbut, and J. M. Sallese, "Modeling and design space of junctionless symmetric dg mosfets with long channel," *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2120–2127, July 2013.