Advances in the characterization of nanowire photovoltaic devices

THÈSE N^{O} 8884 (2018)

PRÉSENTÉE LE 2 NOVEMBRE 2018

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR

LABORATOIRE DES MATÉRIAUX SEMICONDUCTEURS

PROGRAMME DOCTORAL EN SCIENCE ET GÉNIE DES MATÉRIAUX

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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Suisse
2018

To my lovely wife, Liza,

To my sweet daughter, Emilia,

And to my wonderful parents…

Acknowledgements

Firstly, I would like to thank my advisor, Anna Fontcuberta i Morral, who believed in me 4 years ago and invited to work on the completely new topic for me – nanowire solar cells. You gave me an opportunity to return back to science after several years in the industry, for which I am immensely grateful. I appreciate all you time and ideas, motivation and expertise, you gave to me during these 4 years. The amazing atmosphere in the lab that I found from the beginning of my PhD is totally your merit.

I would like to thank Esther Alarcon Llado for giving me a lot of advice during my first year at EPFL. Your expertise in photovoltaics helped me a lot to start smoothly and give the first results very soon. Moreover, with your great support we made a fantastic collaboration on C-AFM analysis, which otherwise would not be possible.

Thanks to Paul McIntyre, for providing me an opportunity to join your team at Stanford University during 9 months in 2017. This internship was successful not only from the scientific point of view, but also gave me a great experience to work in one of the best universities in the world and to feel the energetic atmosphere of your group.

Thank to Franz-Jozef Haug and Christophe Ballif from PV lab at EPFL for your advices and help with the measurements and fabrication of solar cells. Working on new type of solar cells without support from PV lab would be much harder.

I acknowledge Paul Bowen for finding time and accepting to preside in my committee.

A big thanks to Pablo Romero-Gomez, whose arrival to LMSC certainly helped me to finalize my research and write a thesis. Your motivation and creativity are priceless for me.

This work was full of collaborations and I would like to thank all my collaborators - Andrew Meng and Kechao Tang from Stanford, Maria Ricci from Cambridge, Mikhail Mintairov from Ioffe institute, Josua Stuckelberger from PV lab at EPFL. Your knowledge in different areas of science helped a lot during my research.

Thanks to all former and current member of LMSC, including Jelena, Eleonora, Francesca, Federico, Alberto, Yannik, Gozde, Heidi, Martin, Luca, Mehdi, Wonjong, Lea, Jean-Baptiste, Akshay, Elias, Simon, Anna, Rajrupa, Monika and many others. It was a great time together. I will miss this friendship atmosphere!

A special acknowledge goes to the funding sources, supporting my research at EPFL – NanoTera and Swiss National Science Foundation. Thanks to CMi staff for being kind and supportive every time I made a mess in the cleanroom (especially to Zdenek and Patrick).

Finally, I would like to thank all my friends for helping to achieve perfect work-life balance during PhD.

Thanks to my parents, who convinced me to stay in the science at the beginning of my academic career. This would not have been possible without your great support.

Last but most important, thanks to Liza, my lovely wife, and my sweet Emilia, who accompany me around the world and make life easy and fun. You are my biggest achievement in life.

Dmitry Mikulik

Lausanne, 8th of August 2018

Abstract

III-V nanowires (NWs) have a great potential for solar energy applications due to their diameter-dependent optical properties, which may enhance absorption of light. In addition, core-shell radial p-i-n structures, in which the direction of light absorption is orthogonal to the carrier collection, can provide efficient carrier collection. **The main goal of this thesis is the experimental study of the challenges of NW-based solar cells, related to materials and device fabrication.**

In the first part of the thesis, we present an analysis of where the electrical losses can be originated. By applying an equivalent circuit analysis approach, we classified them into three main groups: (i) the non-uniformity of NWs which may result in a reduction of the parallel resistance, (i) potential barriers originated at the different materials interfaces in the solar cell structure may result in an increase of the series resistance or addition of a second diode and (iii) surface recombination resulting in the reduction of the open-circuit voltage. In this thesis, we propose separate strategies to characterize and tackle these factors.

The electric scheme of a NW-based solar cell consists of an ensemble of p-n junctions connected in parallel. We show how conductive-probe atomic force microscopy, C-AFM, is an essential tool for the characterization and optimization of these parallel-connected NW devices. We demonstrate topography and current mapping of the NW arrays, combined with current-voltage (IV) measurements of the individual NW junctions from the ensemble. Our results provide discussion elements on some of the factors limiting the performance of a NW-based solar cell, such as uniformity and photosensitivity of the individual NW p-n junctions within the array, and thereby a path for their improvement.

Besides parallel losses due to uniformity issues, barriers in the carrier collection through the various heterointerfaces composing the device is discussed. To analyze it, we illuminate GaAs NW-based solar cells at different levels of light intensity and extract IV characteristics. This analysis helps to separately study the NW p-n junction response and the series resistance. The high series resistance of the NW-ensemble device can be attributed to the following interfaces: 1) GaAs-ITO, forming a photoactive Schottky diode, which suppresses the p-n junction at high concentrations of light, and 2) Si-GaAs heterojunction, disturbing the flow of majority carriers.

Finally, the characterization of surface passivation in high-aspect-ratio nano/micro structures is addressed by electrochemical impedance spectroscopy (EIS). The method is applied to Si micropillars, as a proof-of-concept prior to the application to III-V nanowires. We tested structures passivated by a dielectric layer. The effect of different surface treatments on the interface state density were quantified by the analysis of the capacitance-voltage and conductance-voltage characteristics. This method allows the electrical measurements on rough vertical surfaces, which would otherwise suffer from high gate leakage currents if tested using solid-state metal-insulator-semiconductor scheme.

The results and characterization methods, demonstrated in this work, contribute to the overall efforts of the scientific community on how to reveal the main engineering challenges in NW-based solar cells. It thus paves the way to approach the fundamental conversion efficiencies predicted by theory.

Keywords

Nanowire, solar cells, III-V, integration of III-V on silicon, electrical losses, conductive atomic force microscopy, electrochemical impedance spectroscopy, surface recombination, surface passivation

Résumé

Les nanofils (NFs) III-V ont un grand potentiel dans des applications dans le domaine de l'énergie solaire grâce à leurs propriétés optiques qui dépendent de leur diamètre, ce qui peut améliorer leur absorption de la lumière. De plus, des structures p-i-n radiales en géométrie noyau-enveloppe, dans lesquelles la direction de l'absorption de la lumière est orthogonale à celle de la collecte des porteurs de charge, peuvent fournir une collecte de porteurs efficace. **Le but principal de cette thèse est l'étude expérimentale des défis des cellules solaires basées sur des nanofils portants sur les matériaux et la fabrication de dispositifs.**

Dans la première partie de la thèse, nous présentons une analyse des sources de pertes électriques. En utilisant l'approche des circuits équivalents, nous les avons classés dans trois groupes : (i) la non-uniformité des NFs, qui peut causer une réduction de la résistance parallèle, (ii) les barrières de potentiel présentes aux différentes interfaces entre les matériaux dans la structure de la cellule solaire, qui peuvent causer une augmentation de la résistance en série ou l'ajout d'une seconde diode et (iii) les recombinaisons de surface, qui peuvent réduire la tension à circuit ouvert. Dans cette thèse, nous proposons différentes stratégies pour caractériser et traiter ces facteurs.

Le schéma électrique d'une cellule solaire à NFs consiste en un assemblage de jonctions p-n connectées en parallèle. Nous montrons comment la microscopie à force atomique avec sonde conductrice, C-AFM, est un outil essentiel pour la caractérisation et l'optimisation de ces dispositifs à connections parallèles. Nous montrons une cartographie de la topographie et du courant des grilles de NFs combinée avec des caractérisations courant-tension de jonctions de NFs individuels parmi ceux cartographiés. Nos résultats révèlent des éléments de discussion sur certains des facteurs limitants la performance de cellules solaires à NFs, tels que l'uniformité et la photosensibilité de jonctions p-n individuelles de NFs dans la grille et par conséquent une direction pour leur amélioration.

En plus des pertes dues aux problèmes d'uniformité, des obstacles à la collecte de porteurs au travers des différentes hétérointerfaces formant le dispositif sont discutés. Pour les analyser, nous illuminons les cellules solaires à NF de GaAs à différentes intensités et mesurons les propriétés courant-tension. Cette analyse permet d'étudier la jonction p-n du NF et la résistance en série séparément. La grande résistance en série des dispositifs avec grilles de NFs peut être attribuée aux interfaces suivantes : 1) GaAs-ITO, formant une diode Schottky photoactive qui supprime la jonction p-n à hautes concentrations de lumière, et 2) hétérojonction Si-GaAs, perturbant l'écoulement des porteurs majoritaires.

Finalement, la caractérisation de la passivation de surface dans les nano- et microstructures à grand ratio d'aspect est abordée par spectroscopie électrochimique à impédance. La méthode est appliquée à des micropiliers de Si comme preuve de concept avant d'être utilisée sur des NFs III-V. Nous avons testé des structures passivées par une couche diélectrique. Les effets de différents traitements de surface sur la densité des états d'interface ont été quantifiés par l'analyse des caractéristiques de capacité-tension et conductance-tension. Cette méthode permet des mesures électriques sur des surfaces verticales rugueuses qui endureraient dans d'autres cas de forts courants de perte s'il étaient testés dans un schéma métal-isolant-semiconducteur.

Les résultats et méthodes de caractérisations, démontrés dans cet ouvrage, contribuent à l'effort général de la communauté scientifique de déterminer les défis d'ingénierie principaux des cellules solaires à NFs. Cela trace le chemin pour approcher les rendements de conversion fondamentaux prédits théoriquement.

Mots-clés

Nanofil, cellules solaires, III-V, intégration de III-V sur silicium, pertes électriques, microscopie à force atomique conductrice, spectroscopie d'impédance électrochimique, recombinaison de surface, passivation de surface

Contents

List of Abbreviations

PV photovoltaics

SQ Shockley-Queisser

NWs nanowires

ARC anti-reflective coating

MBE molecular beam epitaxy

MOCVD metal-organic chemical vapor deposition

ALD

VLS vapor-liquid-solid

SAG selective area growth

HAR high-aspect ratio

C-AFM conductive atomic force microscopy

EIS electrochemical impedance spectroscopy

IV current-voltage

CV capacitance-voltage

SEM scanning electron microscopy

EBIC electron beam induced current

PDMS polydimethylsiloxane

TCO transparent conductive oxide

MOS metal-oxide-semiconductor

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Chapter 1 Introduction

1.1 Photovoltaics

Clean and renewable energy became increasingly necessary in the last decades, especially due to worldwide agreements such as the Kyoto Protocol (framework convention on climate change) [1]. The benefits of the renewable energy are obvious: less global warming [2], improved public health due to minimization of pollution, inexhaustibility of the energy, stable energy prices, reliability and resilience. Alongside other renewable technologies, conversion of solar light into electricity with photovoltaic (PV) technology is an attractive option for our future.

The photovoltaic effect was first observed by Edmond Becquerel in 1839 [3], while he was working with electrolytic cells, using platinum as both as anode and cathode. Measuring electric current between electrodes, he found its increase under the light compared to dark measurements. The practical use of this effect was only realized many decades later. In 1954, engineers of Bell Labs accidentally discovered photosensitivity of doped Si that led to the fabrication of first c-Si solar cells with efficiency of about 6% [4]. The era of solar cell development began. Modern solar cell systems can be adapted to different situations – from home use with small power needs, to large PV energy plants. Among other elements, the potential of this technology will rely on the availability of raw materials and on the cost for refining them, as the available quantities of raw materials on Earth for global PV capacities are limited [5]. Presently, many research groups in PV focus on optimizing both material consumption and conversion efficiency.

Conventionally, PV technologies have been divided into three generations, G [6]:

- G1 – bulk, wafer based (e.g. c-Si, poly-c-Si)
- G2 – thin film based (e.g. a-Si:H, μ-Si:H, CIGS, CdTe)
- G3 – multi-junction, organic, dye-sensitized and nanostructure based

Today, the term of third generation, G3, has been generalized to next generation solar cells. Next generation photovoltaics aims at the increase of the efficiency at a lower cost or materials consumption. A large manifold of concepts are included in this next generation.

Nowadays, 90% of PV cell market is still accounted by the first generation Si based solar cells. Despite disadvantages of this technology such as the indirect energy band gap, silicon remains the most preferred material for PV. This is due to low cost, close to optimum value of the band gap and well-developed technology processing. Still, high-efficiency Si solar cells require very high quality, defect-free bulk material with large carrier mobilities and long minority carrier lifetimes that drastically increase manufacturing cost. With such requirements, the current record efficiency of 26.7% for a Si solar cell is almost approaching its theoretical limit [7]. However, this value is only relatively close to the Shockley-Queisser (SQ) limit of 33.7% for a single bandgap cell (optimum bandgap of 1.34 eV) [8]. Conversion efficiency in single-junction GaAs solar cells are closer to this limit, with an efficiency approaching 29% from Alta Devices [7]. One inconvenient of the GaAs technology is that the cost is much higher due to the scarcity and extraction costs of Ga.

In recent years, nano- and microstructures have been recurrently proposed in the absorber structure for next generation solar cells. As an example, the nanoscale texture of wafer surfaces decreases the reflectance of the surface allowing a better coupling of the incident light in the device [9–11]. Microstructuring of the surface can also enhance absorption of light by this principle and/or by changing the momentum of the incoming light through a grating coupler effect, thus reducing the effective thickness of the solar cell [12,13]. Furthermore, shortening of the minority carrier collection path reduces bulk recombination losses in nanostructure based p-n junctions [14].

The original way to increase efficiency of conventional single junction solar cells is implementing several p-n junctions composed of two or more semiconductor materials with different energy band gap. For example, epitaxially grown GaInP/GaAs/GaInAs/GaInAs multi-junction solar cells result in an efficiency above 45% under concentrating conditions [7]. Still, the fabrication process is technologically complicated and costly. One of the main challenges is the growth of the multilayer stack which requires multiple steps to reduce stress between layers with different lattice constants [15]. In addition, since the cells are being connected in series, the efficiency is dependent on the nature of the solar spectrum. The variation in the spectrum is relevant when using the same device in different latitudes, but also in different seasons and weather conditions [16]. Therefore, as an alternative to monolithic technology, wafer bonded and mechanically stacked configurations become more and more promising in multi-junction solar cell technology. Another strategy consists of merging different generations to build hybrid solar cells, such as a tandem device formed by a silicon bottom solar cell and a lead-halide perovskite device on top [17].

In summary, the main motivation of the ongoing research in PV is centered on improving the conversion efficiency of PV solar cells using novel approaches while reducing the use of the raw materials. Semiconductor nanowires (NWs) represent an extremely promising option for next generation solar cells. Due to its particular morphology and fabrication methods, NWs should also enable the fabrication of flexible or multiple junction solar cells. Next, main advantages of NWs for PV will be introduced, such as superior light absorption, band gap engineering and radial p-n junction configuration.

1.2 Optical absorption in NW arrays

Several factors can prevent the full absorption of the incident light: parasitic absorption in the transparent and adjacent contacts, partial light reflection and finite thickness of the active material of the solar cell. The decrease thickness of the active material to reduce materials costs or increase carrier collection in the solar cell requires a new way to enhance absorption. In the last decade, the use of photonic principles and nanostructuring of materials has shown to be effective in increasing light collection in the active part of the device [18]. Nanophotonic light trapping can utilize arrays of nanoscale particles, wires or holes that enhance light absorption. Among all mentioned nanostructures, our focus here lies on NWs standing on a substrate.

Historically, the first experimental evidence of the advantages of using NWs in solar cells came from the demonstration of their anti-reflection properties [19]. Compared to the standard anti-reflective coating (ARC) strategy, an array of nanostructures provides an alternative approach. To be a broadband and angularly independent, ARC should consist of a multilayer stack with graded refractive index, which makes its fabrication complex and expensive. Nanostructuration is highly effective in both being thin and easily processed (e.g. black Si). The best Si nanostructures with nanocone shape maintain the absorption above 93% over a broad range of wavelengths and incident angle, compared to 64% for Si thin film [10].

The next step was to use nanostructures for light absorption as an active part of solar cell. For that, scientists utilized numerical simulations to discover new optical properties of nanostructured media.

Different rules than standard reflection, transmission and refraction laws, need to be applied for light propagation in structures of wavelength or subwavelength dimensions. In case of vertically oriented NWs, they can act both as a total reflection or leaky-mode waveguide, only the latter being efficient in coupling the incident light [20,21]. Thus, there is a photon energy dependent absorption due to the corresponding spectral dependence of these modes on the nanowire diameter and refractive index. The introduction of NWs in PV as an active material meant also a new geometrical concept of p-n junction formation. In addition to traditional planar (or axial in NW case) p-n junction, core-shell configuration can be realized. The pioneering idea of using semiconductor NW radial p-n junctions for solar cells was published in 2005 by the Atwater group [14]. In particular, they elucidated for the first time the advantages of radial p-n junctions compared to planar p-n junctions. The radial geometry of the p-n junction in a NW allows the orthogonalization of the light absorption and carrier collection and thus allows for independent optimization of light absorption and carrier collection.

The light absorption efficiency of individual nanostructures can also be characterized by the so-called absorption cross-section. This value represents the ratio between the power absorbed in nanostructure and the nominal power flow per unit area for an incident plane-wave. A value of the absorption efficiency (cross-section area/geometrical area) above 1 indicates the existence of concentration effect. Krogstrup *et al.* showed enhancement of light absorption in single GaAs NW due to an effective light-concentrating property of the standing NW [22]. **Figure 1-1** shows simulations of light absorption and absorption cross-sectional area in a 2.5 µm standing GaAs nanowire that is fully embedded in SU-8 on a silicon substrate. Light absorption in the standing NW is enhanced by a factor of between 10 and 70 with respect to the equivalent thin film. As shown on **Figure 1-1a**, simulations of light absorption exhibit two main absorption enhancement branches. **Figure 1-1b** represents enhancement of absorption cross-section area compared to the geometrical cross-section area. A built-in light concentration up to 12 at photon energies slightly higher than the bandgap was found for a NW diameter of 380 nm.

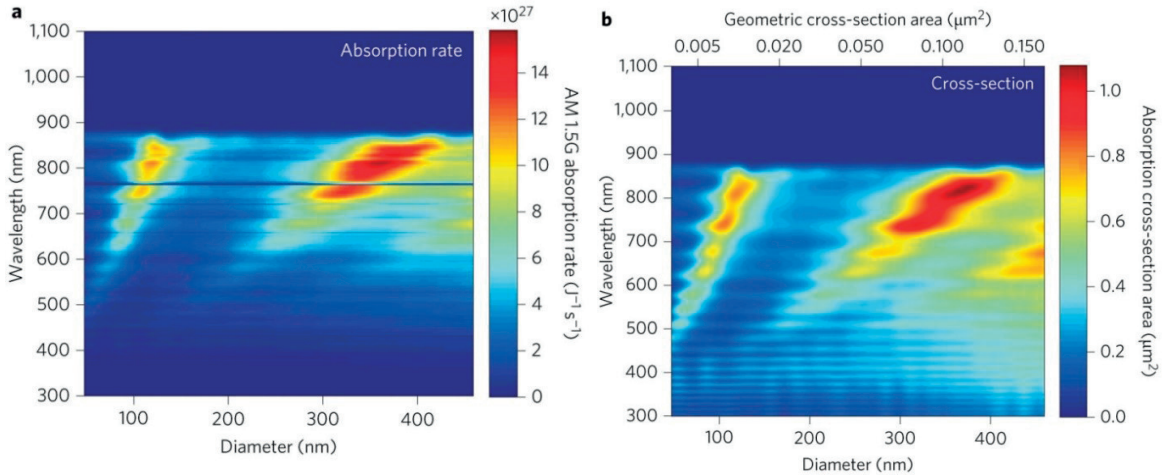

Figure 1-1 Simulations of light absorption (a) and absorption cross-sectional area (b) in a 2.5 µm standing GaAs nanowire that is fully embedded in SU-8 on a silicon substrate. Reprinted by permission from Macmillan Publishers Limited: Nature Photonics [22][COPYRIGHT] (2013)

In case of concentrated solar cells, in which focusing lenses are used to concentrate light. The concentration C has a direct influence on short-circuit current I_{sc} and V_{oc} through linear and logarithmic dependences, accordingly [23]:

$$I_{sc} = I_{sc}^{1} C$$
$$V_{oc} = V_{oc}^{1} + \frac{nkT}{q} \ln C$$

Equation 1 - Short-circuit current and open-circuit voltage dependencies from light concentration.

where I_{sc}^{1} and V_{oc}^{1} – short-circuit current and open-circuit voltage at 1 sun and n the ideality factor. Light concentration increases the carrier generation rate while leaving the equilibrium recombination rate unchanged. One should note here that the light-concentrating effect in NWs for photovoltaics application exhibits a more complicated nature. Recently, Mann *et al.* elucidated the principal difference between macroscopic light concentration and self-concentration in nano-photonics [24]. The absorption cross-section enhancement due to increased coupling of light in the nanowire may increase both generation and recombination rate. In this case, it should not play a role in increasing the V_{oc}. Mann *et al.* propose that V_{oc} may increase because of a reduction in the recombination rate by optimizing the light direction both in absorption and in emission (i.e. by reducing light absorption at oblique angles). By placing single NWs in array with the pitch in the order of the light wavelength, strong directive absorption enhancement at the band edge is observed due to the reduced symmetry of NW geometry (around 150 nm and 380 nm of NW diameter on **Figure 1-1**).

Light emission of the absorber into a solid angle larger than the incident light reduces the overall internal carrier concentration, thus limiting the maximum open-circuit voltage (radiative open-circuit voltage, V_{oc}^{rad}) in the absence of non-radiative recombination. The effect of V_{oc}^{rad} increase due to the photonic effects in NWs was studied recently [25,26]. The explanation is similar to the theory developed by Yablonovitch *et al*. in which an efficient external luminescence is, counterintuitively, a necessity for approaching the SQ efficiency limit [27].

Overall, light absorption enhancement in NWs and its application on photovoltaics should be carefully studied and optimized in order to reach or surpass the SQ limit. Numerical simulations of single NW behavior under the light helps optimizing the nanowire dimensions in devices utilizing NWs as building blocks of nanoscale solar cells. For a realistic device, deterministic arrays of NWs should be fabricated to provide effective absorption of the sunlight over the whole area whilst minimizing materials utilization [28]. When the spacing between nanostructures is on the same scale as optical wavelengths (below 1 μm), photonic crystal effects can play a role, bringing the potential to exceed the conventional ray optics absorption limit [29].

Figure 1-2a represents the results of numerical simulations of light absorption perpendicularly incident on an array of GaAs NWs with a diameter of 150 nm and 2 μm in length. The calculations were performed by Dr. Alarcon-Llado using Finite Difference Time Domain (FDTD) [30]. At the lowest pitch sizes, the NW array performs like a thin film under light illumination. By increasing the pitch, the absorption efficiency increases up to the highest values. Finally, as the spacing between the NWs is further increased, the array absorbs mostly on the low and high energy parts of the spectrum as it is the case single NWs. Based on FDTD simulations, maximum photocurrent vs pitch size can be calculated. **Figure 1-2b** shows surface coverage by NWs (orange line) and maximum photocurrent (green dots and line) vs pitch size on the same graph. At least 60% of maximum photocurrent can be achieved with only several percent of surface covered by NWs (at pitch size 800 nm). This calculation shows the potential in tandem design application with NW based solar cell on top, since a large portion of light will be able to transmit through the NW solar cell for the absorption in the bottom cell.

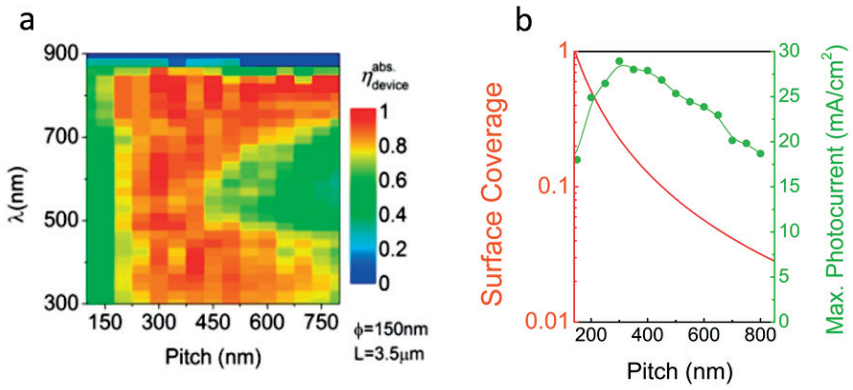

Figure 1-2 a) GaAs nanowire array absorption simulated by FDTD; b) Calculated total photocurrent given by the simulated absorbance and surface coverage as a function of pitch distance. Calculations performed by E. Alarcon-Lladó© 2016 IEEE [30]

1.3 Multi-Junction and III-V on Si approaches

In a semiconductor material photons with energy lower than the bandgap are not absorbed. In addition, the excess energy of high-energy photons above the bandgap is lost in thermalization. Considering the solar spectrum, AM 1.5, the bandgap 1.34 eV gives a maximum solar conversion efficiency of 33.7 % [8]. To increase this efficiency, one can stack together active layers with different band gaps. This minimizes both thermalization and transparency losses. The large band gap material is located on top of the solar cell, and small band gap material is used as a substrate, such as Si or Ge. Intermediate band gap materials can also be added to further increase the light absorption in the form of a triple or multiple-junction solar cell. Combining semiconductor materials with different band gaps into multi-junction solar cells leads to experimental solar conversion efficiencies beyond the theoretical SQ limit for one junction (38.8% for five-junction device under 1 sun [7]). This strategy is widely used in solar concentrating systems and other "niche" application such as solar panels in space, where fabrication cost, extremely high for such technology, is offset by the reduction in weight to efficiency ratio, which greatly reduces fuel related costs. For terrestrial applications, different combinations with low-cost perovskite materials have been intensively studied [31,32]. In case of NW technology, the perspectives of combining NW arrays and c-Si solar cell for tandem configuration were analyzed by Kandala *et al* [33]. Advantages of series connection compared to parallel connection of the sub-cells were depicted using detailed balance calculation. Later on, tandem technology using c-Si substrate with GaAs NWs on top was experimentally introduced by Yao *et al* [34]. In addition, theoretical conversion efficiency of almost 50% was calculated for multi terminal NW solar cell design with three different III-V material NW arrays grown on Si substrate [35]. The potential lower cost of fabrication different material NWs on cheap substrates compared to planar technology opens new avenues for the application of NWs in concentrating photovoltaics. However, the current experimental efficiencies for the tandem-junction design with NWs are still far below single p-n junction NW solar cell.

For a direct band gap semiconductor, such as GaAs, a few micrometers of active layer is enough for effective light absorption and a maximum conversion efficiency of 28.8% has been achieved by Kayes *et al* [36]. However, this achievement requires complexed and expensive technology in order to achieve perfect crystal quality in thin films. Moreover, expensive III-V substrates should be used for the epitaxial growth of device structures. NWs with high crystal quality can easily be obtained on cheaper substrates such as Si by standard epitaxial methods such as Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor

Deposition (MOCVD) [37,38]. The possibility of combining III-V materials with Si thus opens up many new possibilities in multiple-junction solar cells [35].

To date the experimental efficiencies of NW-based solar cells are still far from the theoretical predictions. **Table 1-1** shows current best conversion efficiency values for III-V NW based solar cells. Taking in account results for planar solar cells, implementing multi-junction concept in NW geometry can significantly improve solar conversion efficiency. The tandem configuration for c-Si/GaAs NW solar cell is one of the first attempts in this direction.

Material and Pattern technology	Area (mm^2)	Conversion efficiency	Open-circuit voltage (V)	Short-circuit current (mA/cm^2)	Fill Factor (%)	Reference
InGaAs (EBL)	0.81	7.1%	0.54	18.2	72.1	[39]
InP (NIL)	0.09	17.8%	0.765	29.3	79.4	[40]
GaAs (NIL)	1.08	15.3%	0.91	21.3	79.2	[41]
c-Si/GaAs NW Tandem (PL)	1	11.4%	0.956	20.6	57.8	[34]

Table 1-1 Photovoltaic performance of III-V NW array devices. Pattern technology: EBL – electron beam lithography, NIL – nano imprint lithography, PL – photolithography.

1.4 Radial p-n junction with NWs

Conventional Si solar cells require thick Si layers to maximize light absorption. The charge carriers generated throughout the region must be transported by diffusion over the large distances to be collected efficiently. Different recombination processes might hinder collection. Ordered arrays of vertical NWs with radial junctions (like in **Figure 1-3a**) reduce the path for the photo-generated electrons-hole pairs to the electrodes, thereby improving charge collection. Still, one should note that NW solar cells can also be obtained using axial junctions or substrate junctions (see **Figure 1-3a-b**). In this case, charge carriers diffuse a longer path than in the radial configuration. As a consequence, surface passivation becomes key in order to obtain a good carrier collection [42].

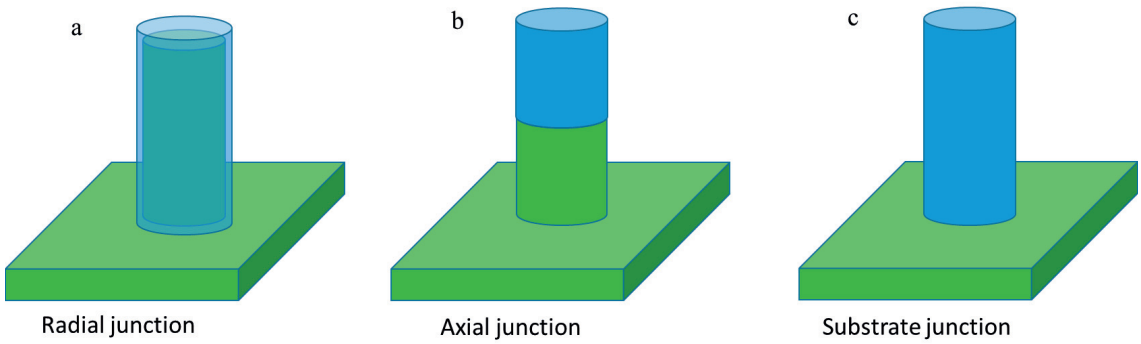

Figure 1-3 Different types of the NW geometry: (a) Radial junctions NW array; (b) Axial junctions NW array; (c) Substrate junctions NW array. Green and blue colors represent different type of doping.

Figure 1-3 represents three different NW p-n junction geometries – substrate junction **(a)**, axial junction **(b)** and radial junction **(c)**. The arrays of NWs with radial junctions maintain all the advantages described above, including reduced reflection, extreme light trapping, radial charge separation, relaxed

interfacial strain, and single-crystalline synthesis on non-native substrates. Axial junctions lose the radial charge separation benefit but keep the remaining ones of radial junctions. Finally, substrate junctions lack the radial charge separation benefit and cannot be removed from the substrate to be tested as single-NW solar cells.

Still, both axial and radial p-n junction NW concepts are highly explored by different scientific groups. The ability to control doping and surface passivation in NWs is one of the key factor for the success of the devices. Simulations showed that NWs with axial junction configuration are more tolerant to doping variation than with radial configuration [43]. Low doping in the core of NW ("base" for radial junction) can lead to inversion of the carrier type caused by the shell doping. However, high doping of the core is not desirable due to reducing mobility and diffusion length. As a result, current records in NW solar cells all belong to axial configuration, which is more robust.

Surface recombination is another major concern for NW-base solar cells due to their high surface-to-volume ratio. Yu *et al* simulated the impact of surface recombination velocity on both axial and radial p-n junction NW arrays [42], and they concluded that the recombination rate at the surface for the same doping level is much higher in the axial configuration than in the radial case.

1.5 The main limiting factors in solar cell operation

The main limiting factors of energy conversion in solar cells were elucidated more than 50 years ago by Wolf *et al* [44]. They are the following: incomplete absorption, quantum loss (band gap), collection losses, voltage drop and dark saturation current, and resistive losses (from contacts). **Figure 1-4** schematically illustrates the main losses in solar cells directly on a schematic p-n junction band diagram. In short, when a photon is absorbed in the active region of solar cell, an electron in the valence band receives this energy and is excited to the conduction band. Afterwards, the electron and the hole created in the valence band after electron excitation are collected at the electrodes due to an internal electric field. However, several additional fundamental processes can occur. Process 1 and 2 correspond to sub-band gap absorption loss and loss of excess energy of high-energy photons to phonons. Junction loss (3) represents the energy loss caused by the voltage drop of the carriers from bandgap voltage to internal voltage of the junction. Non-optimized metal contacts lead to losses of carriers due to series resistance (4). Besides current loss (processes 3 and 4), voltage drop is observed due to recombination effects – surface and bulk recombination (5 and 6). It can be explained by direct dependence on the dark current I_{dark} and open circuit voltage V_{oc} as:

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_{ph}}{I_{dark}} + 1\right)$$

Equation 2 - Open circuit voltage definition.

where k is the Boltzmann constant, T is the cell temperature, q is the electron charge and I_{ph} is the photocurrent. Dark current increases with the increase of recombination rate in solar cells. Finally, solar cell surfaces can reflect part of light, and light can transmit through the absorbing layer without absorption in case of thin film solar cells (7 and 8).

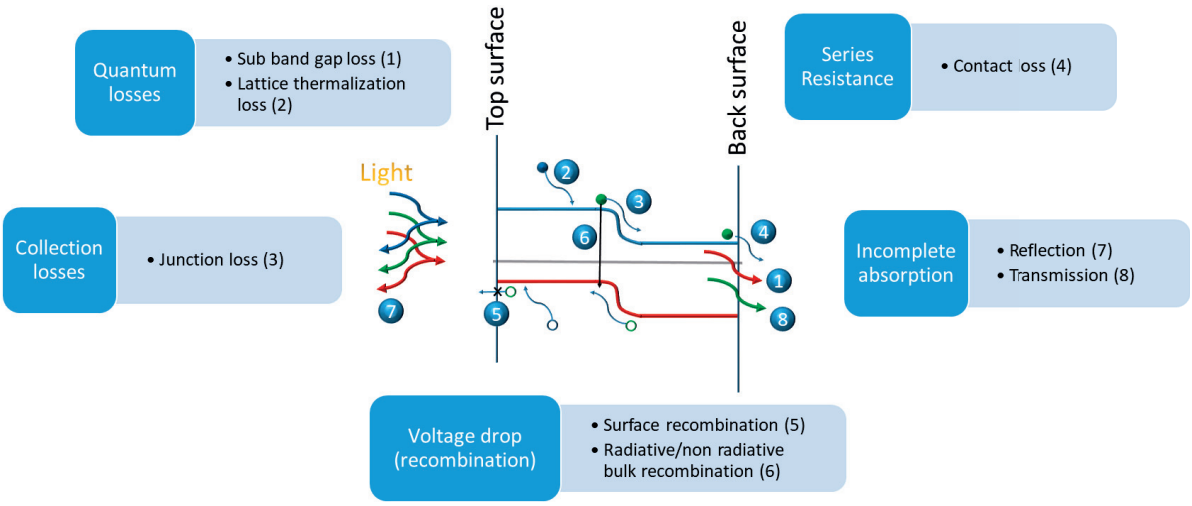

Figure 1-4 The main limiting factors in solar cells.

The introduction of nanostructures in PV devices may allow overcoming some of above-mentioned limitations but may increase other factors that are less relevant in bulk or thin film devices. Nanotexturization can significantly decrease the reflectance of the surface. The ability of nanostructures to enhance absorption of light results in reduced transmission losses due to thin absorbing layer, allowing one to use less material whilst retaining similar levels of absorption. Furthermore, short carrier path for electrons to be collected significantly eliminates bulk recombination losses in nanostructure based p-n junctions. Therefore, light trapping using nanostructures can enhances both the short-circuit current and the open circuit voltage of a solar cell. Worth noting, some of the main losses can be enhanced with the use of nanostructures. Large surface-to-volume ratio in 1D nanostructures makes the surface recombination overall much higher, increasing the importance of the surface passivation. Series resistance due to the not optimized interfaces with transparent front or the back contacts limits the fill factor of the devices.

1.6 Objectives and outline of this Thesis

Device characteristics of radial and axial NW p-n junction solar cells have been reported for various fabrication approaches like the bottom-up vapor-liquid-solid (VLS) and selective area growth (SAG) methods, top-down dry and wet etching methods, electrodeposition and others. **Figure 1-5** illustrates the increase in the best-reported conversion efficiencies based on III-V NW devices in the last few years.

The still comparably low efficiencies for NW-based solar cells indicate many unresolved issues such as obtaining high quality shell formation, reducing surface and interfacial carrier recombination losses, and forming conformal transparent electrodes on the surface of NW with low contact resistance. All these fabrication issues should be carefully analysed to reveal the way to optimize the solar cell structure and increase the solar conversion efficiency up to or beyond planar solar cells, which goes beyond photonic design [45,46]. Another challenge is coming from the scaling NW technology for PV terrestrial applications. Increase in the area of the solar cell leads to the increase of potential losses through the imperfection of the solar cell structure. Garnett *et al*. have shown a scalable technology for Si NW solar cell, achieving areas up to 10 cm^2 [47]. However, III-V NW based solar cells are still much smaller (up to 1 mm^2).

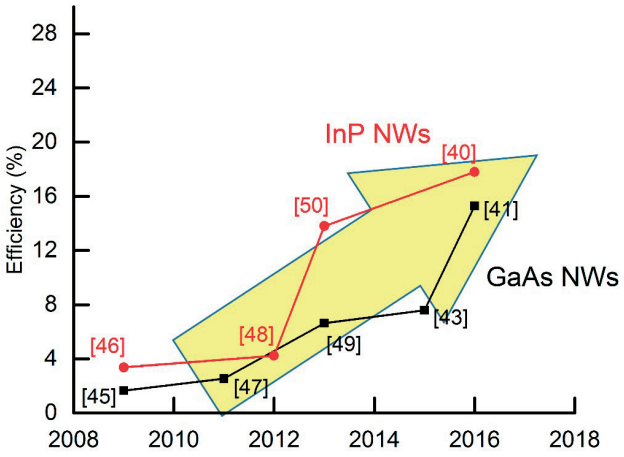

Figure 1-5 Best III-V NW based solar cell efficiencies vs Time [40,41,43,48–53].

Classical electrical characterization of solar cells is not enough to reveal the weak points in NW solar cells due to radically different nature. The focus of this thesis is to provide advanced tools and strategies for the analysis of the losses and solutions in NW-based solar cells.

After this introduction, next **Chapter 2** is dedicated to the fabrication of NW based solar cells and classification of different losses in such devices. Starting from the overview of the growth processes, we investigate and reveal difficulties, coming from it, in post-growth steps and device accomplishment. All losses can be divided in two categories – parallel and series losses. At the end, we show that classic I-V characterization cannot univocally analyse these losses.

Chapter 3 covers the developed characterization methods for the analysis of parallel and series losses in NW based solar cells. First, we introduce important issues with the uniformity in NW array and how conductive AFM (C-AFM) may be useful for its characterization. The second main loss we focus on is different interfaces in NW solar cells, where series resistance can be generated. We separate p-n junction electrical properties from general IV curve using advanced method with applying different intensities of light. The former is widely used in multi-junction solar cells to reveal any losses at the interfaces in solar cell structure.

Finally, in **chapter 4** surface recombination in NW solar cell is recognised as one of the main drawback due to enhanced surface-to-volume ratio. We present an electrochemical impedance spectroscopy (EIS) method that provides a way to obtain quantitative information on the interface states in high-aspect-ratio (HAR) structures.

In **chapter 5**, overview of the thesis and a brief comment on the future perspectives in NW application for PV industry is provided.

Chapter 2 Parallel and series losses in NW-based solar cells

This chapter is dedicated to the fabrication of NW based solar cells and classification of different losses (which can be classified as series or parallel) in such a devices. Starting from the overview of the growth processes, we investigate and reveal difficulties, coming from it, in post-growth steps and device accomplishment.

We start with highlighting several obvious requirements to increase the area of NW based solar cell technology and reduce the cost of fabrication, such as absence of e-beam lithography patterning, need for wafer-scale technology, and cheap or reusable substrates. **Figure 2-1** shows two strategies for NW based solar cell commercialization – rigid solar cell on a cheap Si substrate and a NW-polymer solar cell peeled off from the substrate. For the first scheme, the bottom-up growth of NWs can be performed on p-doped silicon substrate with a dielectric layer acting as a mask. Large scale patterning can be done using, for example, soft imprint lithography [54]. Due to the reduced contact area between highly lattice-mismatched GaAs and Si, the strain is limited and therefore the formation of dislocations and misfits at the interface is suppressed [55]. Thus, NWs represent an opportunity to integrate GaAs on Si for different opto- and microelectronic applications [56]. The latter method requires peel-off step, which constitutes mechanical breakage of the NWs at the bottom, leaving the substrate reusable for the next growth [57]. Using this process, an expensive III-V substrate can be reused for multiple growth of NWs, reducing the total fabrication cost.

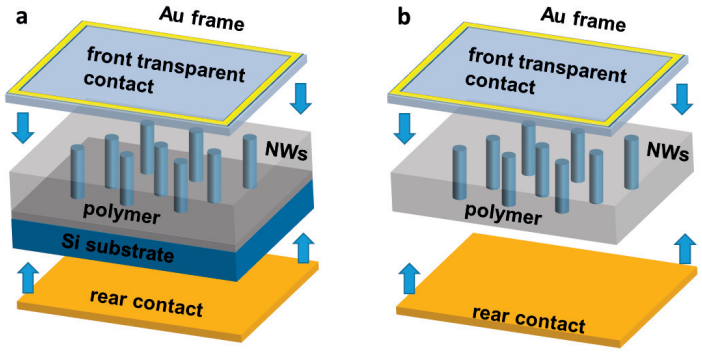

Figure 2-1 Two ways to obtain large area commercial NW solar cells: **(a)** rigid device on Si substrate; **(b)** flexible device utilizing NW-polymer composite.

Scaling fabrication processes for terrestrial applications is one of the main challenges for the introduction of new device schemes in the PV industry. So far, the record efficiency of 17.8 % was obtained for an InP NW based solar cell with the area of only 0.09 mm^2 [40]. Other high performance NW devices have an area around 1 mm^2 or even less. One of the reasons for using reduced sizes is the geometrical and

structural uniformity issues in NW arrays, which introduces electrical losses. Besides scaling, overall efficiency of the best NW devices is much lower than their thin film analogs [7]. Therefore, not only parallel losses due to uniformity issues, but also series losses that are generated through the solar cell structure, limit the potential breakthrough of NWs in the PV industry. Unambiguously, detailed analysis of losses should be done in order to improve NW based solar cell performance. The equivalent electrical scheme can be drawn in order to illustrate parallel and series losses in the NW based solar cell. **Figure 2-2** shows simplified equivalent electrical scheme for NW based solar cell. Parallel connection of n diodes represents different electrical behavior of NWs in array in case of poor uniformity (NW1…NWn). Series losses can be defined by series resistances R1…Rn. Finally, shunt resistance Rsh is nothing else as a leakage path for electrical current past p-n junctions.

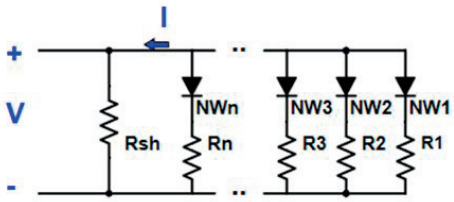

Figure 2-2 Equivalent electrical scheme of the NW based solar cell.

This chapter addresses the potential impact of the fabrication technology on introducing different losses in NW solar cells. We describe the fabrication steps of semiconductor NW based solar cells in details and how it effects on device properties. We start with the growth of NWs and surface passivation, following by post-growth processes, such as polymer embedding and the electrical contacts formation. At the end, applicability of IV electrical characterization method is analyzed in the case of NW based solar cells.

2.1 Growth of semiconductor nanowires

In general, top-down and bottom-up are the two main paradigms in nanostructure fabrication. The first one dominates the modern microelectronics due to the perfect device definition and density, which have typically been the strengths of top-down fabrication. In recent years, advances in bottom-up fabrication processes have opened up the possibility of the integration III-V on Si for different optoelectronic applications. Despite the fact that top-down plasma etching of NWs into a wafer provides the highest uniformity, unresolved reproducibility of mechanical peel-off step (required for substrate re-use) reduces the prospect of this method for commercially available large-area III-V NW based solar cells. Therefore, we focus on the bottom-up growth processes, such as catalyst-free SAG and VLS growth methods by MOVPE and MBE. Below, different technologies to obtain arrays of vertical NWs on substrates are discussed in this context.

Catalyst-free SAG method requires a dielectric mask with openings, formed by a lithographic process and subsequent dry or wet etching. **Figure 2-3a** illustrates SAG method. NWs are epitaxially and locally grown in such holes due to selectivity [58]. Typical features of SAG in MOVPE is high V-III ratio (ratio between V and III group elements) and relatively high growth temperature (700 – 800 °C) [59]. MBE has very low growth rates, therefore, the vapor-solid process, such as SAG, is inexpedient in terms of time and cost of the process. However, the VLS method using Ga or Au droplet as a catalyst is well developed and highly used to grow different types of semiconductor NWs by MBE.

Figure 2-3b shows the VLS method in two steps. The initiation of the growth starts with the droplet formation, where the self-catalyzed method uses Ga droplet formation inside the holes of the pattern [60],

and the Au-catalyzed method needs annealing of the Au film above the liquid phase transition temperature to form Au droplets [61,62] or direct pre-deposition of Au nano particles [63]. Next, precursors in the form of vapor are transported to the substrate and absorbed by the droplets. Finally, due to supersaturation, the material precipitates at the liquid/solid interface. Thus, NW is growing along the direction of the largest surface free energy. MBE VLS method utilizes low V-III ratios (Ga-rich conditions) and relatively low temperatures.

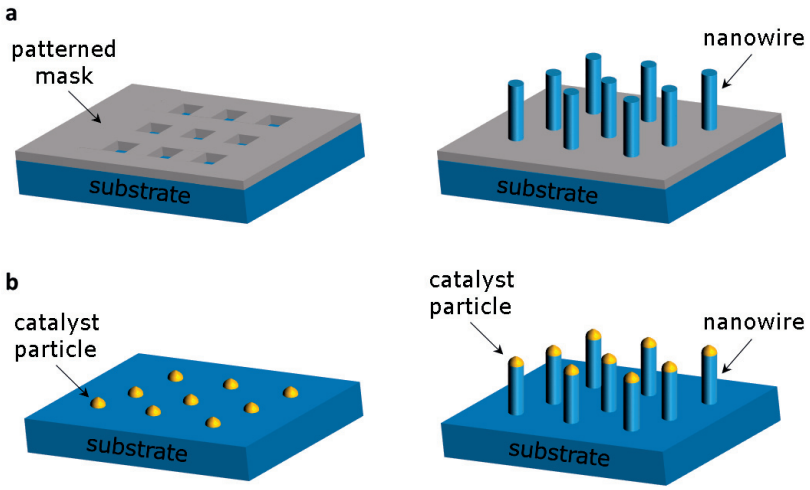

Figure 2-3 Schematic illustration of SAG **(a)** and VLS **(b)** growth methods of semiconductor NWs.

The growth of perfect vertically aligned NW arrays is one of the key factors to develop high-efficiency NW based solar cell. The uniformity of NWs, both geometrical and functional, plays significant role in obtaining high efficiency due to the parallel electrical connection of NWs in the array, as shown on **Figure 2-2**. Each NW p-n junction is a diode, working as a single solar cell. Parallel connection of solar cells is known to be an option to connect solar cells in a solar module [64]. For solar cells connected in parallel, current is additive while voltage is the same. This configuration has high tolerance against complex irradiance conditions (for example, partial shading). However, if among the solar cells connected in parallel there is a cell with open-circuit voltage lower than the others, it will drag down the voltage on all the remaining solar cells. A similar case can be extrapolated on NW based solar cell with NWs connected in parallel in arrays. Therefore, high uniformity in the array is needed to get best performance. Here, we come to the first challenge in large area NW solar cell structures – the need of high uniformity of NWs.

Figure 2-4a shows a scanning electron micrograph (SEM) of a GaAs NW array, grown by SAG MOVPE on a GaAs substrate. Perfect uniformity in NW length and diameter reduces the possible losses due to parallel connection of NWs in device structure. **Figure 2-4b** and **Figure 2-4c** show GaAs NWs obtained on a silicon substrate by Ga-catalyzed VLS growth by MBE, where Ga droplets exist on the top of the NWs. The difference between the last two images comes from the fact that there is no dielectric mask with pre-defined holes on **Figure 2-4b** in contrast to the sample from **Figure 2-3c.** In the absence of the patterned mask, NWs are grown in a self-organizing mode and thus have a wide variation in the diameter and length [65,66]. In addition, parasitic GaAs deposition between NWs is enhanced. These two cases show the importance of the dielectric mask with lithographically defined openings for uniform NW array. It is worth to note additional feature on **Figure 2-4c** such as tapering of NWs in case of small distance between them. Diameter variation in NW should be considered in order to optimize light absorption in arrays with small pitch. Moreover, radial p-n junction in tapered NWs can be non-uniform along the NW length.

The preparation and type of substrate prior to NW growth is key since in rigid NW based solar cells it is used as a back electrical contact (see **Figure 2-1a**). In case of GaAs NWs, native GaAs substrates and foreign Si substrates can be used. The crystalline orientation of the substrate plays a major role in determining the orientation of NWs compared to the substrate. GaAs (111) B and Si (111) wafers allow preferential vertical growth of NWs (perpendicular to the substrate). Besides the growth mechanism on native or foreign substrates and crystalline quality issues related with it, the carrier transport mechanism through the "substrate-NW" interface should be mentioned. In case of using Si as a foreign substrate to grow GaAs NW, a potential barrier between Si and GaAs can occur due to the band alignment characteristics between the two semiconductors. By changing doping levels in the substrate and the NWs, the width of the barrier can be minimized in order to promote carrier tunneling through the potential barrier and therefore reduce series resistance at the interface. We will come back to this question later. Finally, the obvious difference between Si and GaAs is the substrate cost. While Si is cheap and can be a part of the solar cell without increase in the cost, GaAs substrates should be removed and re-used in next growth for reducing the production cost of NW based solar cell.

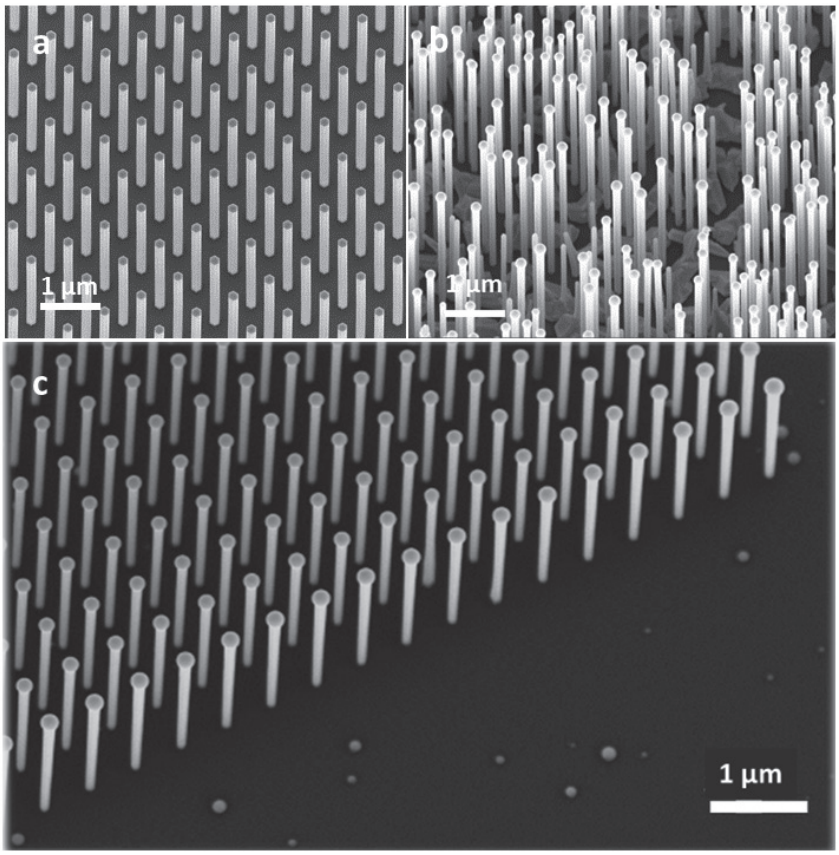

Figure 2-4 SEM images showing the uniformity of GaAs NWs grown by SA-MOVPE on GaAs substrate **(a)**, self-assembled Ga-catalysed VLS MBE on Si substrate **(b)** and Ga-catalysed VLS MBE on Si substrate with hole pattern **(c)** [image by Wonjong Kim] methods.

A conventional solar cell needs p-n junction in order to separate electron-hole pairs. As mentioned in **Chapter 1.4**, axial or radial geometries of junction can be implemented in NW concept. Depending on the growth method, epitaxial technique and geometry of p-n junction, different difficulties with optimal doping of n- and p-type of junction are exist. In VLS growth, the doping is incorporated through the droplet and

therefore less controllable compared to standard doping in vapor-solid growth such as SAG. Not taking in account the technological aspect of this question, the analysis and characterization of the p-n junction in NWs is the fundamental point in order to optimize the carrier transport inside NW p-n junction. The doping level can be measured through the single NW characterization or directly in the array by electron beam induced current (EBIC) method but it requires advanced techniques to prepare the sample for the measurements. In addition to doping concentration evaluation, the p-n junction diode behavior is the important parameter in the solar cell. The diode current is limited by the carrier recombination mechanism in the structure. Therefore, detailed diode analysis provides the main limiting factors in the p-n junction and opens the ways to improve the carrier transport through p-n junction.

2.2 Surface passivation

After the growth of NWs and formation p-n junction, the surface should be passivated. While the one-dimensional nature of NWs provides several advantages, such as enhanced light absorption, this particular morphology and reduced size results also in an increase in the surface-to-volume ratio. Consequently, any defects or energy states at the surface due to oxidation can disturb its functional properties. As shown on **Figure 2-5a**, electronic states at the surface can appear due to an abruptness of the periodical crystal lattice (e.g. dangling bonds) and the existence of a non-stoichiometric surface oxide. These states can act as non-radiative recombination centers and contribute to the trapping of charge carriers. As a consequence, pinning (bending) of the Fermi level at the surface occurs [67]. A pinned Fermi level can push the free carriers from surface to the bulk forming an undesirable depletion layer in NW. Overall, this results in a decrease in the figure of merit of devices such as a reduction of photo-generated power for solar cells.

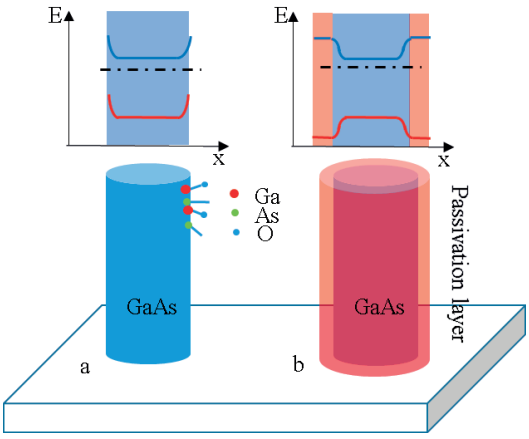

Figure 2-5 Position of the conduction (blue) and valence bands (red) across a NW diameter for: **(a)** un-passivated GaAs NW and **(b)** a GaAs NW passivated with a thin layer of AlGaAs. Below, the 3D drawing of the structures are shown. As-dangling bonds and GaOx are represented at the surface of the un-passivated NW.

One strategy to reduce the effect of surfaces in nanostructures consists of coating with a semiconductor with a lattice-matched material with a larger bandgap, as shown on **Figure 2-5b**. Coating results in the passivation of dangling bonds, while the higher bandgap allows charge carriers to remain in the core of the structure. Note that Fermi level pinning can occur at the surface of passivation layer (not shown on **Figure 2-5**); however, this region is not the part of the electrically relevant area of p-n junction. From the conceptual point of view, coating with a lattice-matched material should result in the suppression of surface states. Therefore, popular way to passivate GaAs NWs is to coat them radially with an AlGaAs layer inside the epitaxial reactor just after the growth. AlGaAs is lattice-matched with GaAs and exhibits a

higher bandgap. The band alignment of GaAs and AlGaAs semiconductors results in type I heterostructure. Capping with a highly doped layer also helps saturating the surface defect states [68,69]. In addition, to prevent further oxidation of Al in AlGaAs, which is highly probable in case of high Al concentration, application of a thin GaAs extra layer can be an option to complete the device structure. The potential losses with such a passivation scheme are related with a non-uniform Al content distribution (also called Al segregation), parasitic absorption in the capping layer and the presence of the potential barrier for majority carriers.

Another strategy focuses on passivation of III-V NWs with an amorphous and high bandgap dielectric, such as aluminum oxide, Al_2O_3, by atomic layer deposition (ALD). This material has shown encouraging results with other III-V NWs such as InAs and InAsSb [70]. In the case of III-V arsenide surfaces, the group III components often oxidize preferentially, producing As dangling bonds and As anti-site defects at the oxide/semiconductor interface [71]. To prevent it, pre-ALD dosing of trimethylaluminium, the standard molecular precursor for Al_2O_3 deposition, can be used before starting deposition to both inhibit subsequent oxidation of the surface and selectively passivate As dangling bonds, as was successfully shown for InGaAs surfaces [72,73].

Efficient passivation of nanostructures by dielectric material by ALD has turned out to be challenging as a few interface states remain, with the consequent impact on the functional properties of the nanostructures. In this sense, there is the need for a deeper understanding of the passivation mechanism of nanostructures as well as defining fabrication procedures for finding optimal passivation layers for different semiconductors. This optimization can only be realized if the surface and interface states can be characterized in a proper manner. In **Chapter 4**, we provide a path for the characterization of surface and interface states in HAR semiconductor structures passivated with dielectric layer.

2.3 Post growth processes

Several post growth processes are realized for the complete fabrication of the solar cell structure. These include planarization and mechanical support via embedding in transparent polymer, opening of the NW tips by polymer etching and electrical front and rear contact formation. All these steps should be optimized to minimize possible losses in solar cell. **Figure 2-6** represents the main post-growth steps in fabrication NW based solar cell.

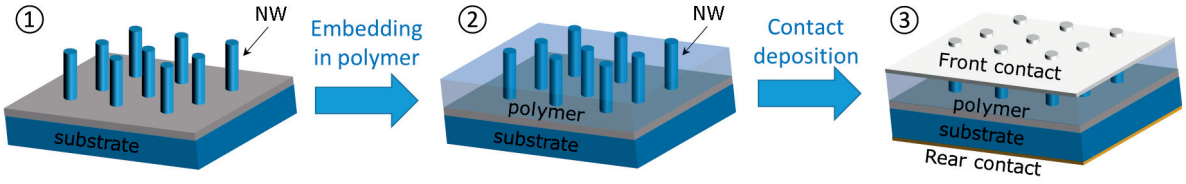

Figure 2-6 Process flow of post-growth fabrication of NW based solar cell.

2.3.1 Polymer embedding

Embedding of NWs into a flexible polymer film was first reported by Plass *et al*. [74]. An array of VLS-grown Si wires was suspended in a Polydimethylsiloxane (PDMS) film. Subsequently, a free standing PDMS film with NWs was created by mechanically peeling the film from the Si substrate. Since the first publication, there were very few reports on the performance of detached NW-polymer composites for solar cell applications due to difficulties in fabrication process. Spurgeon *et al.* [75] demonstrated that this approach could potentially lead to a solar cell without sacrificing solar energy conversion efficiency compared to substrate-supported NW solar cells. Here, we discuss the embedding of NWs in polymer film,

which acts as a supporting layer and reduces the surface roughness of NW array for conformal electrical contacts coating. Additional benefit of the polymer media comes from the ability to cool down the NW based solar cell in more effective way [76]. Embedding the NWs in polymer (such as BCB) increases the spectral emissivity over the whole thermal wavelength range due to better thermal IR absorption in polymer compared to bare NWs case.

To embed NWs in a polymer film, different insulating polymer materials can be used, such as BCB [43,52], PDMS [77,78] and SU-8 [22]. Two of them are discussed in this thesis – PDMS and SU-8. The requirements for integration polymer in NW based solar cells are transparency at visible wavelength range, electrical insulation and chemical compatibility with III-V NWs. The main advantage of PDMS is an opportunity to mechanically peel the NWs from the substrate, while maintaining a low refractive index and transparency. It opens up opportunities to fabricate flexible NW based devices and re-use expensive III-V substrates for NW growth. The standard PDMS embedding process includes several steps, such as PDMS mixture preparation, spin coating and baking. One key aspect that should be considered is the typically high density and aspect ratio of NWs in array. To prevent any mechanical breakage or bending of NWs during spin coating, the PDMS mixture must be diluted by Hexane or another appropriate component for decreasing viscosity. SU-8 resist can be spin coated without dilution at rather low spin rate to obtain thickness down to 1 μm. Comparing both polymers, PDMS is preferred in case of mechanical peeling of the NWs from the substrate, while SU-8 is preferred for rigid NW solar cell design with NWs below several microns.

Here, we highlight another potential issue for large area NW based solar cell, which is the mechanical damaging of NWs during polymer coating. Potentially, it can effect on a carrier transport through the solar cell structure by forming leakage paths. The probability to damage NWs highly depends on two parameters: viscosity of the polymer solution and hardness of the NWs. The first parameter can be tuned by choosing appropriate polymer and/or diluting it with special chemical components. The second parameter comes from geometrical parameters of NWs such as diameter, length and pitch size, as well as NW fabrication method. One can conclude that top-down etched NWs are naturally stronger than ones grown by the bottom-up approach. After spin coating and baking in the oven, the polymer film with NWs on the substrate is cross-linked and ready for the next fabrication steps.

One of the most complicated process steps related to the polymer is dry etching by plasma. To contact NWs with a top electrode, the tips of NWs should be exposed. The etching process requires careful time control and multi-step configuration to get a desirable polymer thickness slightly below the NW height. Imperfection in NW array leads to thickness variation in polymer film after opening the NW tips. This can affect the quality of the top electrical contacts and result in an increase series resistance. In addition, residuals of polymer on NW surface can lead to an additional parasitic contact resistance at the interface between NWs and the top electrical contact.

2.3.2 Electrical contacts to NW based devices

To complete the solar cell, front and rear electrical contacts are needed. Typically, the rear electrical contact is opaque, made from metal alloys. Since the rigid NW solar cell stays on the substrate, the rear contact is provided through the doped substrate and metal film deposited on the back of the wafer. Another option is forming the rear contact on the top of the wafer out of the NW array area. Different metal contacts can be used for the NW device, depending on the substrate material. In the case of III-V substrates, Au alloys form ohmic contacts to GaAs after annealing at certain temperatures, such as

Pd/Ge/Au to n-GaAs and Pd/Ti/Au to p-GaAs. Si substrates as a back contact form ohmic contacts with Al (p-type) or Au and Pt (n-type). This process is well developed for Si technology.

To illustrate the contact formation to GaAs p-n junction structure grown on Si, electronic band diagram in dark at equilibrium is shown on **Figure 2-7**. The software package Nextnano was used to simulate band alignment of the GaAs p-n junction and hetero interfaces [79]. Note that Al rear contact to p-doped Si substrate is considered as ohmic. Regarding additional losses due to rear contacts, we can highlight increased series resistance in the case of low-doped substrate, since carriers have to travel along the whole thickness of the substrate. One should also highlight the barrier at the valence band alignment at the interface between GaAs and Si. This results in a barrier (and added series resistance) for holes that have to diffuse through this interface. Tanabe *et al.* showed that to prevent barrier at the hetero interface, GaAs should be doped up to $5x10^{19}$ cm^{-3} concentration [80].

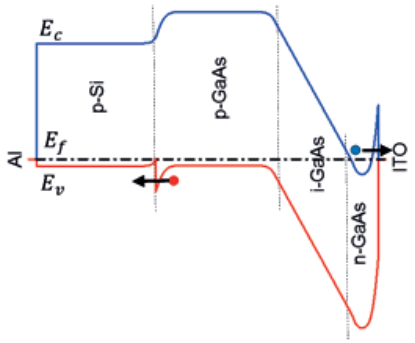

Figure 2-7 One-dimensional energy band diagram of the solar cell structure Al/p-Si/p-GaAs/i-GaAs/n-GaAs/ITO along the NW axis (in dark at equilibrium conditions). Electron (blue circle) and hole (red circle) flow is indicated.

To allow light to couple and be absorbed in the NWs, transparent front contacts are required. Up to now, indium tin oxide (ITO) contacts to n-type III-V materials has been the material that allows quasi-ohmic transparent contacts. This limits the possible configuration of NW to p-n junction with n-type top and p-type bottom contacted through the substrate. A number of reports analyzed different deposition methods including metal interlayers (In, Ti) and annealing steps to improve the contact resistivity at the n-GaAs/ITO interface [52,81]. Even with this configuration, high resistance at the interface decreases the efficiency of the NW based solar cell. The evidence of the resistive top contact can be found by analyzing IV curves of NW based solar cells. In addition, non-optimized ITO contacts to n-GaAs can form reverse Schottky diodes, which diminishes the overall light conversion efficiency. As shown on **Figure 2-7**, difference in work functions between ITO and GaAs can generate a large Schottky barrier with depletion of n-GaAs layer near the interface with ITO. These losses, which appear in equivalent circuits in the form of series resistance and/or reverse diodes, can be analyzed by characterizing the IV curves as a function of the light concentration. This method will be introduced in Chapter 3.2.

2.4 Standard electrical characterization methods of NW based solar cells structures

We can divide and name all losses in NW based solar cells described in previous parts of the Chapter in two main groups: parallel and series losses, depending on their location in the equivalent circuit that describes the device (see **Table 2-1**). It is worth to note that we assume in this analysis a perfect p-n junction inside of NWs. Briefly, parallel losses consist of poor uniformity in NW array and shunting due to forming leakage paths in the structure, such as broken NWs. Series losses can be of different nature, such

as series resistance in substrate or front and rear contacts, potential barriers for majority and minority carriers at different interfaces. The optimization of the conversion efficiency should involve the careful analysis and addressing of all current and potential losses. Before moving to the advanced characterization methods in Chapters 3 and 4, developed specially for NW based devices, the most commonly used electrical characterization approaches are described in detail.

Fabrication step	Parallel losses	Series losses
Growth of NWs	Poor uniformity	Resistance in substrate, potential hetero barrier for carriers (III-V/Si)
Passivation	-	Potential barrier for majority carriers, series resistance
Polymer embedding	Mechanical break of NWs	Parasitic resistance at the interface
Electrical contacts	-	Potential barrier between III-V and TCO, contact resistance

Table 2-1 Electrical losses in NW based solar cell due to fabrication issues

Figure 2-8 shows a cross-sectional SEM image of a NW based solar cell. The GaAs NWs were obtained on a Si substrate by self-assembled Ga-catalyzed VLS growth through MBE [65]. Vertical NWs were embedded in a polymer (PDMS in this case) and top-contacted by ITO layer, resulted in ~1 µm randomly rough surface. In order to analyze potential issues with scaling up NW based solar technology, we developed 13.9 mm^2 area solar cell with self-assembled method, which is one order higher than previously reported III-V NW based solar cells.

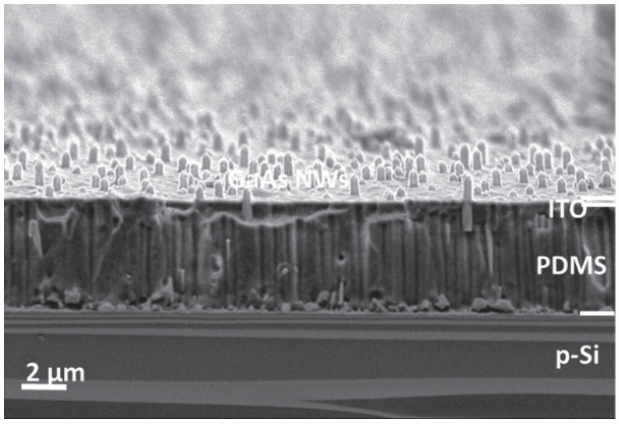

Figure 2-8 Cross-sectional SEM image of GaAs NW based solar cell.

In the following, we move to the description of electrical characterization methods traditionally used in PV, such as IV characterization.

2.4.1 Device current-voltage (I-V) curve characterization

Classic IV curve characterization in the dark and under illumination (at 1 sun) is a common method for analyzing main solar cell properties, such as V_{oc} and I_{sc}. In addition to these parameters, the shape of the IV curve is determined by the fill factor through the resistance effect (series R_s and parallel R_p). Moreover, the ideality factor of the diode, n, and dark saturation current, I_0, give a measure of the main

recombination mechanism in the diode. Overall, solar cell behavior can be described by the following single-exponential equation:

$$I = I_0 e^{q(V-IR_s)/nkT} + \frac{V - IR_s}{R_p} - I_{ph}$$

Equation 3 - Diode equation with series and shunt resistances.

Note that photogenerated current I_{ph} does not always equal I_{sc} due to current losses in the solar cell. **Figure 2-9a** shows an IV curve measurements of GaAs NW solar cell under the light and in the dark that can be obtained using standard electrical probe station and solar simulator.

The shift of light IV curve from dark IV curve indicates the light absorption of the PV device. The one or two diode models can be used to fit experimental curve and extract main solar cell parameters [82,83]. However, several limitations exist in this method. Standard fitting model requires correspondence between the solar cell equivalent schemes to the one diode model (see **Equation 3**). An extended version of this model is the two-diode model, where an additional diode is placed in parallel to the first one, as shown on **Figure 2-9b**. In presence of additional elements in the equivalent scheme of the solar cell due to its imperfection, all parameters extracted by these models can contain significant errors. In some cases, fitting is impossible due to non-linear processes in solar cell, such as the reverse diode connected in series. Another limitation comes from the presence of series resistance in solar cells. Too high series resistance effects the carrier transport mechanism and hides the real performance of the p-n junction diode [84]. In the case of NW based solar cells, applicability of classic IV characterization and one or two diode models to reveal losses in solar cells is difficult due to the parallel connection of NWs in array, high series resistance at the interface between GaAs and ITO, and internal potential barriers in the interfaces.

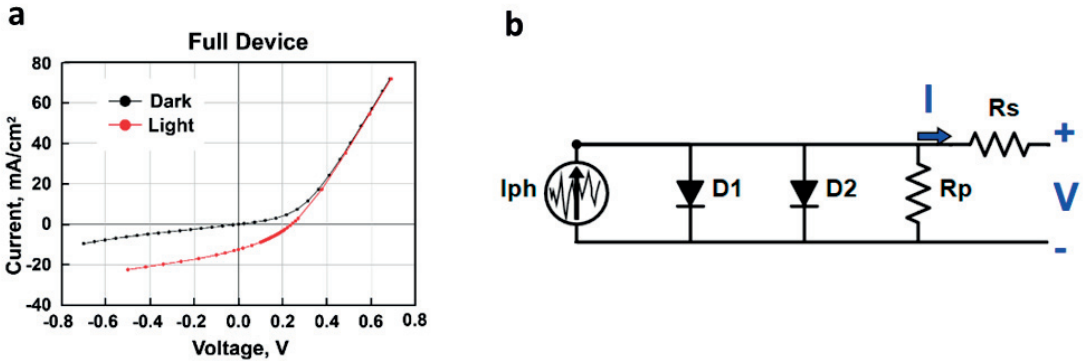

Figure 2-9 (a) IV curve characterization (dark and light) of GaAs NW based solar cell [78]; **(b)** Double diode model equivalent scheme

2.4.2 Single NW I-V curve characterization

Single NW IV characterization is a standard method to analyze the p-n junctions in a NW structure. **Figure 2-10a** shows a SEM image of a single GaAs NW with a radial p-n junction, connected on a handle silicon substrate with 2 metal contacts. To transfer the NW from the growth substrate to the substrate with contact scheme, drop casting is used. The NWs are first diluted in isopropanol (IPA) by submerging a piece of substrate with standing NWs in an ultrasonic bath. During sonication, NWs start to detach forming a NW/IPA solution. Using a pipette, a few drops of NW/IPA solution, containing thousands of NWs, can be transferred on the target substrate. After placing NWs horizontally on the dummy wafer with SiO_2 film,

contacts can be realized using optical or e-beam lithography, depending on required resolution and the size of NWs. In the case of radial p-n junction configuration, the NW shell should be chemically etched at the place of the metal contact to the core. More details on the fabrication method can be found in elsewhere [85]. The active area of horizontally located single NW can be estimated directly from the shape and sizes of NW part between metal contacts in SEM image.

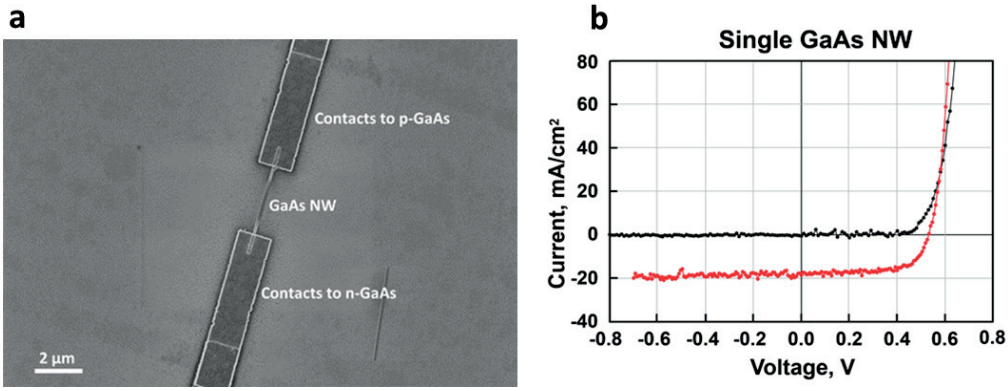

Figure 2-10 (a) SEM image of single GaAs NW with 2 contacts scheme; **(b)** IV curve characterization of single GaAs NW [78].

Finally, classic IV curve characterization is applied to a single NW device and shown on **Figure 2-10b**. This method helps to analyze a single NW detached from the substrate and provides statistics of electrical properties of single NWs in array. Disadvantages of this method is expensive and time consuming sample preparation, as well as impossibility to analyze effect of the substrate in the device performance. In addition, light propagation in horizontally located NW is radically different from vertical NWs, which results in the erroneous estimation of the conversion efficiency [22].

Chapter 3 Electrical characterization of parallel and series losses in NW-based solar cells

3.1 Parallel losses characterization using Conductive-probe Atomic Force Microscopy (C-AFM)

In spite of the high potential suggested by the theoretical analysis, the successful implementation of NW based solar cells faces a manifold of technical challenges [86,87]. One way to tackle these challenges is to investigate and target the potential losses in this kind of devices. NW array-based solar cells consist of multiple vertical NWs that are electrically connected in parallel between the electrodes. One important issue of a parallel-connected NW device is the potential inhomogeneity of the NWs and the possible negative impact of low performing NWs in the array. Non-uniformity in electrical properties of NWs originates from the dispersion of morphology distribution during the bottom-up growth, especially if they are obtained by self-assembly [65]. A priori, achieving perfect geometrical uniformity over the whole surface area is critical in bottom-up NW array solar cells.

The impact of inhomogeneity of NW p-n junctions in the device can be described using a model of parallel-connected solar cells. The inset of **Figure 3-1** shows a virtual device combining two NWs connected in parallel (NW1+NW2) and corresponding IV curves under illumination. The IV curve of the virtual device NW1-2 will consist of the sum of currents and it is plotted in the green-colored curve. The open-circuit voltage of this device, $V_{oc}(1-2)$, will be close to the open-circuit voltage of the less performing NW, $V_{oc}(2)$. This simple calculation indicates that underperforming NWs will certainly influence the NW array device. One of the obvious questions is how many underperforming NW junctions can be tolerated for a minimum impact in the efficiency of the device. The goal of the study in this subchapter is the following: to determine the real influence of such poor performing NWs on the total efficiency of NW based solar cells and evaluate it in a quantitative manner.

Different characterization methods have been used to study NW-based solar cells. Some overview can be found in recent research articles [88–90]. In general, all methods can be divided into two categories – macroscopic and nanoscopic. The first category represents macroscale characterization of NW array solar cell as a full device, where standard methods for characterization of planar solar cells can be used. Two-point electrical measurements such as IV and EQE characterizations are a good example [89,91]. However, the uniformity in the electrical properties of NWs in the array are difficult to address by these methods. Here, nanoscale characterization can be a complementary support for the understanding. As an example, one could address the electrical losses in the array due to the parallel connection of NWs. The main concern for such techniques is the nanoscale resolution in order to examine single NWs in an array. In opposite to well-established macroscale characterization of NW solar cells (e.g. array devices), nanoscale characterization (e.g. single NW in the array) is still an evolving field of research.

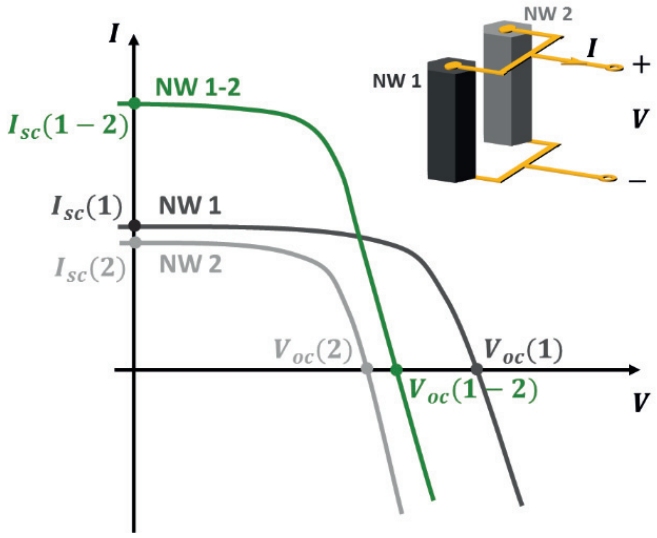

Figure 3-1 Schematic illustration of the electrical device consisted of two NW p-n junctions connected in parallel with corresponding I-V curves under the light. The green-coloured IV curve of the device shows the drop of V_{oc} due to lowest performing NW 2.

The electrical properties of single NWs can be addressed by detaching them from the substrate, combined with nanolithography methods [92,93]. This technique was shown in the previous Chapter. One inconvenient of this method is that it is destructive and difficult to scale-up for investigation of a high number of NWs. As a consequence it cannot be utilized in a large-area characterization of NWs. EBIC measurements represent another developed method to characterize the electrical properties of single NW p-n junction [41,94,95]. In general, an electrical current is recorded during electron beam excitation of NW in SEM. The application of this method was illustrated on axial p-n junction GaAs NWs grown on GaAs substrate by MOCVD method [41]. By profiling the EBIC response across the NW core, the p-n junction formation can be analyzed in details. Also, the NW array device with TCO contact on top enables EBIC mapping of the surface [95,96]. However, the thickness of the front electrical contact should be carefully optimized in order to prevent large beam absorption in this layer. Overall, EBIC (or its analog – laser beam induced current (LBIC)) measurements electrically characterize uniformity of NW p-n junctions in the array only from the electrical current point of view. Thus, there is no possibility to perform complete electrical analysis of NWs in the array, such as obtaining IV curve and photovoltage of single NW.

In this subchapter, we demonstrate that C-AFM is an appropriate and non-destructive method to perform full statistic on the electrical properties of single NWs located in an array. There is a large number of publications on AFM characterization of HAR nanostructures. The significant amount of works focuses on mechanical properties where single NW can be bent by AFM tip. A step forward to characterize the electrical functionality of NWs is the use of conductive AFM. By using a conductive tip it is possible to study the electrical properties by forming local metal-semiconductor contact on the surface of the device [97]. Single NW electrical characterization by C-AFM has been used to analyze doping mechanisms [98], local resistance [99] and single NW IV curves [100]. Scanning mode of C-AFM measurements can provide current/potential maps of the surface. Adding illumination capabilities to the C-AFM method provides an opportunity to study photoconversion properties of the NWs. Here below we summarize all different possibilities that can provide C-AFM and continue by implementing it on the GaAs NW arrays.

We fabricated GaAs radial p-i-n junction NWs based on self-assemble MBE growth on Si substrate [38,65,101]. The fabrication is described in details in the previous Chapter. **Figure 3-2** shows a sketch of the C-AFM analysis of GaAs NW sample. A Pt metal probe is used to electrically contact the NW tips, which are not covered by ITO (opposite to the solar cell devices). The back contact of the device is established between the p-type GaAs NW core and the doped Si substrate. The latter is in contact with a metallic disc working as a back electrode. External light is applied to analyze the response of the device under illumination.

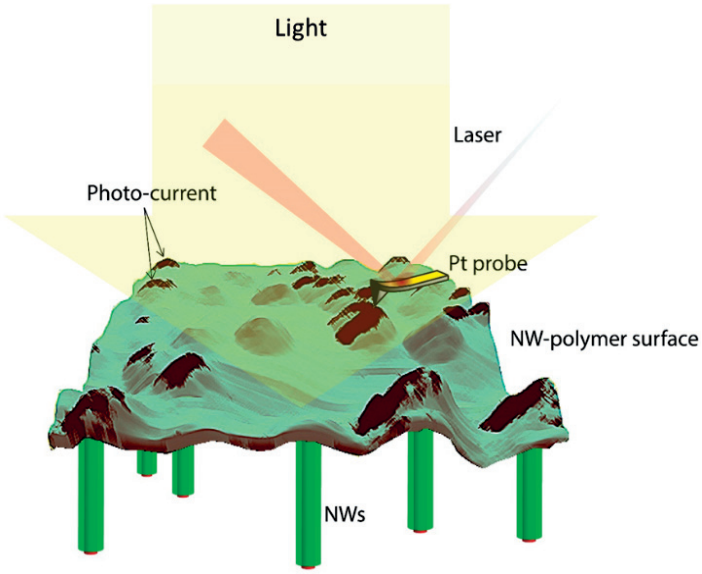

Figure 3-2 Conductive AFM analysis of NW solar structure. The surface is constructed by overlaying of the current map over 3D topography map. Dark spots represent photocurrent obtained under the light at zero bias.

Three different C-AFM modes have been used to characterize NWs in the array.

1. First, we illuminate the sample while applying a zero voltage between the tip and the sample. C-AFM current scan over the examined area can detect photosensitivity of the NW p-n junctions. This mode is shown in **Figure 3-2**, where dark spots, i.e. non-zero photocurrent response, indicate photosensitive NWs.
2. Current mapping can also be performed while applying a bias between the probe and sample. The same area of the sample can be scanned several times in contact mode while applying different DC voltages. By this method, open-circuit voltage values of each NW p-n junction can be roughly estimated.
3. C-AFM technique provides IV measurements of each NW separately. It is useful for routine analysis of NW p-n junctions in a large array in case of the automatization of this method. In our study, we show an example of such a routine analysis by extracting the IV curves from 50 NW p-n junctions in the array.

In addition, we have characterized the NW-based solar cells in two conventional ways: (i) macro-characterization of NW ensemble device by contacting the NW array device and (ii) nano-characterization of single NW device by detaching and contacting separately from the native Si substrate. Results from both methods were further compared with C-AFM analysis.

One comment should be done on piezoelectric properties of GaAs NWs. During scanning process in C-AFM setup, unintentional bending of NWs by Pt tip can induce the mechanical strain and therefore result in piezo-phototronic effect under the illumination [102,103]. It can lead to additional piezo-current and piezo-potential and over-estimate the measured short-circuit current and open-circuit voltage in NW array structure. However, in case of Ga-catalyzed VLS growth, zinc blende (ZB) crystal phase is preferential in GaAs NWs [104], where piezoelectric effect is much weaker than in wurtzite structure due to rather low piezoelectric strain coefficients. In addition, mechanical support from polymer media helps to minimize any bending of NWs during the measurements. Therefore, we assume negligible piezoelectric effect in C-AFM measurements.

Applying all three modes of C-AFM and comparison the results to the standard characterization helped us to answer on the question raised at the beginning of this part of the chapter. Our sample of self-assembled NW p-n junctions has a distribution of open-circuit voltages around 0.5 V that was confirmed by 2nd and 3rd C-AFM modes analysis. This number is similar to the value from single NW electrical characterization, but much higher than one obtained in NW array device by standard IV characterization (0.24 V). The discrepancy can be explained by the existence of electrically active non-photosensitive NWs, which can act as leakages. The 1st C-AFM mode analysis revealed almost half of NWs, which are not photosensitive to light. In addition, detailed analysis of the current maps at different applied bias showed that the non-photo sensitive NWs (absence of current at no applied bias) can still be electrically active at -1 or +1 V. **Figure 3-3** shows how non-photo sensitive NW can effect on total IV curve. Obviously, fill factor and open-circuit voltage can be significantly reduced assuming a high number of non-photosensitive NWs in the array.

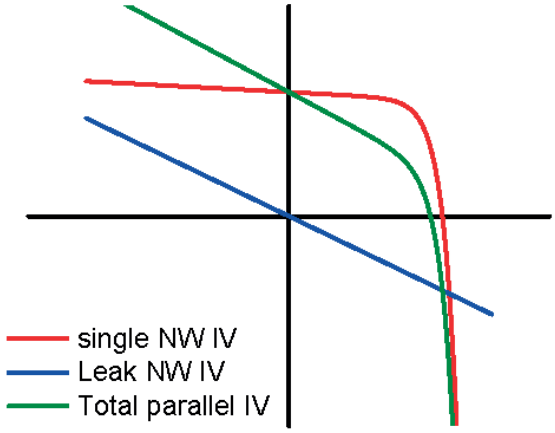

Figure 3-3 Illustrative light I-V curves of two single NWs p-n junctions – leaking and not - and combined device of two NWs connected in parallel.

In summary, we have demonstrated the potentiality of C-AFM to characterize the individual electrical properties of NW p-n junctions in an NW array solar cell structure. We have shown that few less performing NW p-n junctions are detrimental on the characteristics of the full device, but they do not fully determine the V_{oc}. For the optimization of the device, it is key to achieve homogeneity of the properties of the p-n junction as well as their light-response across the whole NW array.

3.1.1 Paper included in this section

This work was published in Nano Energy **41** (2017), 566-572.

doi.org/10.1016/j.nanoen.2017.10.016

This section includes the post-print version of the manuscript. The independent bibliographic references for the manuscript are attached in the end of the corresponding section. The aforementioned bibliographic references differ from the general bibliography of this thesis by means of a different format. For instance, [1] refers to the first reference in the manuscript, while [1] refers to the first reference in the general bibliography presented at the end of this thesis. Supplementary information of the publication is located in Appendix at the end of the Thesis.

TITLE

Conductive-probe atomic force microscopy as a characterization tool for nanowire-based solar cells

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*Equally contributing authors

MY CONTRIBUTION

- I fabricated nanowire samples for C-AFM measurements, excluding epitaxial growth
- I performed C-AFM characterization
- I fabricated and measured the devices including single NW and the NW arrays
- I took active part in interpreting and analyzing the results
- I prepared the figures
- I wrote part of the paper

Conductive-probe atomic force microscopy as a characterization tool for nanowire-based solar cells

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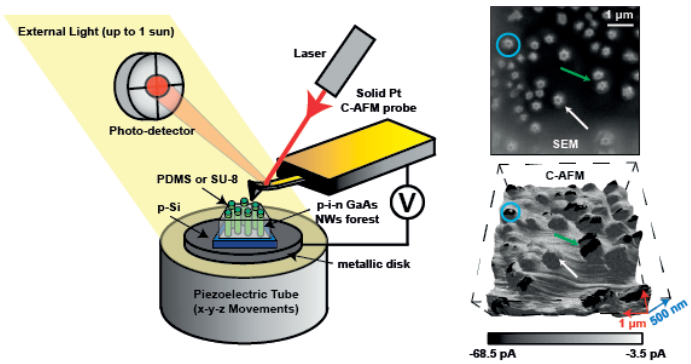
Abstract

The photonic properties of nanowires advocate for their utilization in next generation solar cells. Compared to traditional devices, the electric scheme is transformed from a single into an ensemble of p-n junctions connected in parallel. This new configuration requires new schemes for the characterization. We show how conductive-probe atomic force microscopy, C-AFM, is an essential tool for the characterization and optimization of these parallel-connected nanowire devices. With C-AFM, it is possible to obtain both surface topography and local electrical characterization with nanoscale resolution. We demonstrate topography and current mapping of nanowire forests, combined with current-voltage measurements of the individual nanowire junctions from the ensemble. Our results provide discussion elements on some factors limiting the performance of a nanowire-based solar cell and thereby to provide a path for their improvement.

Graphical Abstract



Research Highlights

- The use of conductive atomic force microscopy (C-AFM) in nanowire-based solar cell devices is used to study the statistical properties of each nanowire p-n junction and compared to the performance of the large-area device.
- The C-AFM measurements reveal the non-uniformity of electrical properties between single NWs in ensemble.

- It is shown that a few poor-performing nanowire devices may not have a dramatic reduction on the nanowire ensemble performance.

Keywords

Next generation photovoltaics, nanowire-based solar cells, conductive-AFM, III-V semiconductors

1. Introduction

Semiconductor nanowires (NWs) are promising for photovoltaic applications due to their superior light absorption with respect to their thin film counterparts [1-7]. The needle-like morphology of NWs is also advantageous for the extraction of the photo-generated carriers via a radial p-n junction design [8, 9]. Today, experimental efficiencies of NW ensemble solar cells are still lower than the record values for planar solar cells [10-12]. Van Dam *et al.* recently achieved a record conversion efficiency close to 18 % for 0.09 mm^2 area of InP NWs-based solar cells [13]. These devices were fabricated using nano-imprint lithography and a top-down approach, etching down nanopillars on an InP substrate with a p-n junction. This approach guarantees the uniformity in size and electrical properties within the ensemble, although it limits the devices to an axial junction configuration. Moreover, it does not provide a path to save expensive and non-abundant elements such as indium. For a more efficient utilization of resources, NWs should be obtained in a bottom-up approach and on foreign substrates [14].

One of the major challenges in bottom-up NW ensemble solar cells is achieving perfect uniformity over the whole surface area as the individual NW p-n junctions are connected in parallel. The main concern is that the electrical properties of the NW ensemble device may be limited by the lowest performing NWs of the ensemble. So far, there is no experimental evidence of how low-performing nanowire p-n junctions affect a solar cell device made of a nanowire ensemble. It is thus necessary to correlate the individual electrical characteristics of single NWs with the overall device. Only in this way, it is possible to progress swiftly in the technology and to determine the factors that significantly affect the performance of the NW ensemble device. So far, to obtain this information, single NWs have been first detached from the substrate and then singularly contacted to perform electrical measurements. This process requires a long nanofabrication process [15]. In addition, the NW is isolated and positioned horizontally on a substrate, thereby strongly changing the light absorption conditions [16]. Finally, the influence of the interface and band-alignment between semiconductor NW and a foreign substrate (e.g. GaAs on Si) cannot be addressed by this technique.

Conductive-probe atomic force microscopy (C-AFM) is a powerful current-sensing technique for the characterization of conductivity variations in resistive samples. C-AFM can simultaneously map surface topography and current distribution of samples by applying a constant voltage between the scanning conductive tip and the sample surface. The main appeal of C-AFM is the possibility to access local conductivity information down to the nanoscale and, at the same time, to explore significantly large areas of the sample surface during the scanning process [17, 18]. This enables, in the specific case of NWs forest, to have single wire resolution but on a statistically significant number of NWs. C-AFM has been widely used to characterize single NWs but without luck in terms of linking morphology and electrical properties [19-23]. The main issue in the case of standing NWs is the big roughness of the sample that makes challenging a proper tracking of the surface and thus a reliable mapping of the sample conductivity.

In this paper, we demonstrate the use of C-AFM for individually characterizing electrical properties of self-assembled GaAs NW p-n junctions standing on a doped Si substrate on which they were grown by Molecular Beam Epitaxy (MBE). In addition, we compare the obtained data from C-AFM with standard

current-voltage (IV) measurements of single NW and ensemble solar cells by probe station. When operated in contact mode, the lateral-spatial resolution of C-AFM is set by the contact area between AFM tip and sample. By choosing sharp probes and appropriate scanning conditions, reliable conductivity measurements are systematically obtained and standing single NWs resolved. To limit the roughness of the sample, the NWs forest was embedded in a polymeric transparent matrix, so that only the top of NWs is reached by the AFM tip. The individual photovoltaic properties are obtained by combining the C-AFM setup with an optical fiber able to introduce external light source with calibrated power. By combining the information from topography and current maps we are able to individually address the NWs. We find that the properties of the MBE-grown NW ensembles are inhomogeneous in terms of electrical properties and that up to half of the NWs can be electrically inactive. The IV characteristics on a statistically significant number of wires are obtained. The individual properties are compared to the statistically averaged properties of the ensemble. This allows us to address the limitations of the NW ensemble device. We prove C-AFM to be a fundamental technique in the analysis of NWs ensemble solar cell structures, particularly in the case of samples obtained by self-assembly growth where more inhomogeneity in the NW properties is expected. We provide a quantitative link between the single wire and the ensemble device performance. This link is fundamental for the optimization of the fabrication process.

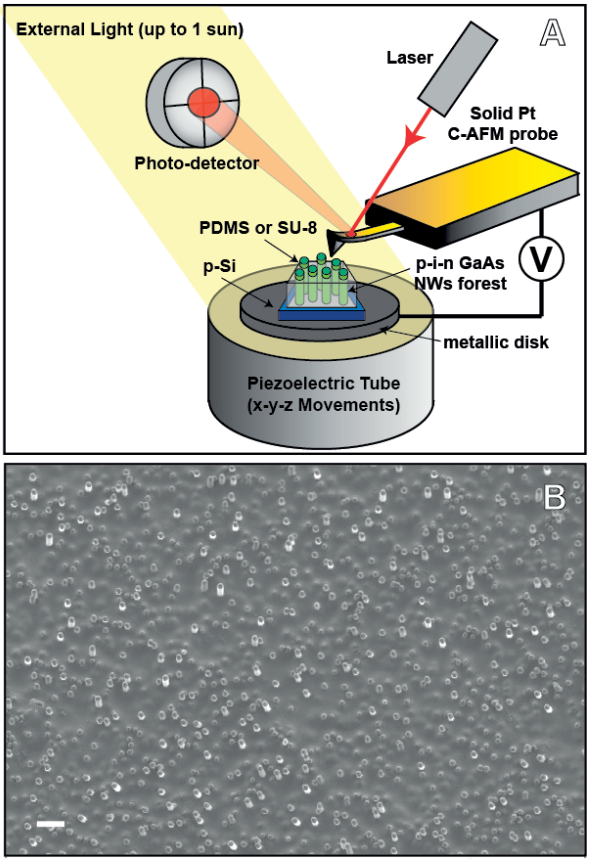


Figure 1. Schematic illustration of C-AFM setup (A) and SEM image of GaAs NWs embedded in polymer matrix (B). The sample for C-AFM measurements is electrically connected to a metallic disk and a bias between the Pt probe and the sample is applied while scanning the surface. The piezoelectric tube enables fine movements in the three x-y-z directions. An external light source is mounted in the AFM enclosure. The light beam with a calibrated power is impinging on the sample. The scale bar is 2 µm.

2. Material and Methods

2.1. GaAs NW growth

In this work, radial p-i-n GaAs NWs were grown on 2-inch p-doped (111) Si substrate by MBE using self-catalyzed vapor-liquid-solid method (VLS). By optimizing growth parameters and thickness of native oxide on Si substrate, self-assembled GaAs NWs were grown vertically with desired geometrical properties [24]. This method allows for the growth of large area ensembles of NWs without using lithographic processes. First, p-GaAs NWs were grown using standard growth conditions, reported in [25], with addition of Si as dopant. The same Si flux used for the doping of the core leads to a nominal doping concentration of 10^{18} cm^{-3} when calibrated with secondary ion mass spectrometry (SIMS) on (100) GaAs substrates. Next, the growth conditions were switched for the shell growth by decreasing the temperature and increasing V/III ratio. This facilitates growth on $\{110\}$ side facets and intrinsic GaAs shell of the thickness of 100 nm was grown. Finally, 30 nm of n-GaAs was grown using Si as dopant [15]. The nominal doping concentration was $5x10^{18}$ cm^{-3} in that case. The morphology of the samples was characterized with scanning electron microscopy (SEM). Images of the samples can be found in Supplementary Information (SI - Figure S1).

2.2. NW ensemble device preparation

After growth, the NWs were embedded in a polymer matrix - polydimethylsiloxane (PDMS) or SU-8, obtaining a flexible transparent thin layer. In the case of PDMS, the as-grown sample was covered with the polymeric solution by spin coating technique. To enhance the adhesion between polymer and the NW ensemble, the curing agent to base ratio was increased from standard 10% up to 20%. Due to the high density of NWs, the PDMS solution was diluted with Hexane (1:6) to decrease the viscosity of the solution. A 3 ml drop of the mixture was placed on the sample and spun at 4000 rpm for 60 sec. The sample was then cured in the oven for 2 hours at 80° C to enable the hardening of the PDMS layer. Finally the PDMS surface was etched in a SF_6 plasma for 5 min to expose the NWs tips and thus enable electrical contact. In the case of SU-8, GM1040 SU-8 photo-epoxy was spun on the as-grown sample at 1000 rpm for 45 s and cured with 1 min UV light and 5 min on a hotplate at 130 °C. After the curing, 1 min oxygen plasma etch was performed to remove SU-8 residuals from the NW tips.

Finally, the front and back contacts were fabricated, so that the radial p-i-n GaAs NW ensemble could also be used as a solar cell. Front contacts were produced by RF sputtering a transparent 200 nm thick Indium tin oxide (ITO) film at room temperature (RT) with a rate of 18 nm min^{-1} and 15 sccm of Ar and 2 sccm of O_2 gases. A 200 nm DC sputtered film of Al was used as a bottom contact to the p-doped Si substrate which was preliminary dipped in buffered HF solution to remove native oxide. To facilitate the electrical probing, a Ti/Au (10/100nm) contact frame was electron-beam evaporated on the sample through a hard stencil mask. It is worth noting, that for C-AFM measurements, the top contact was avoided in order to eliminate any influence of the surrounding NWs on the IV measurements.

2.3. Conductive-probe atomic force microscopy

Figure 1 shows C-AFM setup (A) and the SEM image (B) of the GaAs NW ensemble sample. The NW array has been fabricated with the same process flow as the solar cell, only the top contact is

missing so that the individual IV curves can be recorded. C-AFM measurements were performed using two different AFM equipment: the ORCA module of a Cypher-S AFM and the C-AFM module of a Bruker ICON system. In the first case, we used internal light-emitted diode (LED) lamp to determine the photo-response of NWs in ensemble and analyze behavior of NW p-i-n junctions under different applied voltage. The IV statistics of NW p-i-n junctions were collected with the Bruker ICON system. To illuminate the sample, an external light source from a quartz tungsten halogen lamp was introduced into the AFM set-up through an in-built optical microscope. Due to the internal losses inside optical system, the total light intensity was much lower than 1 sun. The exact spectrum and measured light intensity can be found in SI (fig. S3-1). The aluminium back contact of the sample was attached to a standard metal disk with conductive epoxy glue. The electrical connection between the metallic disk and the voltage supply was obtained using the tools and procedures described by the AFM provider [26, 27]. For the electrical measurements, solid Pt tips were mounted on the cantilever holder. The exact procedure of measurements and details on AFM tips are given in SI (see S3). Standard imaging (not electrical measurements) was performed in Amplitude Modulation using the same machine but with the normal cantilever holder and standard AC240TS tips.

2.4. Standard device and single NW electrical measurements

The IV measurements of the NW ensemble device were performed by contacting the samples with 2-points custom-made needle probe station, equipped with a source meter unit used as a voltage source and current meter. The series of IV measurements were obtained first in the dark and then under light illumination using a one-sun simulator. The intensity was calibrated with the help of a reference solar cell.

In order to validate the C-AFM method, we also provide electrical measurements of the single NW, detached from the substrate and contacted horizontally. For the contacting, we followed the procedure described by Colombo *et al* [15]. Shortly, after detaching the NW p-n junctions from their native Si substrate, we transferred them on a Si wafer covered by an insulating SiO_2 layer and markers for lithography alignment. Next, e-beam lithography is used to form a contact scheme, followed by evaporation of Pd/Ti/Au (40/10/150 nm) contacts for p-type and Pd/Ge/Au (40/170/50 nm) contacts for n-type GaAs. The IV characteristics were measured both in the dark and under 1-sun (AM 1.5) illumination.

3. Results and Discussion

3.1. Standard NW solar cell characterization

Prior to the C-AFM measurements and in order to have a reference of our device properties, we have characterized the NW-based solar cells in two ways: (i) ensemble device characterization by contacting the NW ensemble and (ii) single NW characterization by detaching and contacting separately from the native Si substrate [28-31]. The active surface of the measured device corresponded to 13.9 mm^2. An optical image of the ensemble device as well as an SEM image of the single NW device can be found in SI (see Fig. S2 and S4, respectively). IV measurements were performed both in the dark and under 1-sun illumination. In order to extract the ideality factor (n) and series and shunt resistances (R_s *and* R_{sh}), we fitted I-V curves using the 1-diode model (more information in SI – S5).

Figure 2A depicts the electrical characteristics of the NW ensemble solar cell. The open-circuit voltage (V_{oc}) of the NW ensemble device is 0.24 V, a value much smaller than those found in GaAs solar cells (thin film GaAs – 1.122 V [12], NW array – 0.923 V [32]). The short-circuit current density (J_{sc}) of 12.5 mA/cm^2 is far below the predicted maximum of 28 mA/cm^2 as well. We can calculate the average short-circuit current from each NW (I_{sc}^{nw}), which is the measured $J_{sc}^{ensemble}$ from the NW ensemble device IV divided by the number of NWs in 1 cm^2. Therefore, on average, each NW generates I_{sc}^{nw} of 25 pA, which is an order of magnitude lower than previously reported elsewhere [1]. The ideality factor of the full device is 2.56, which indicates possible tunneling through internal barriers or additional recombination pathways at the interfaces that will be explained further.

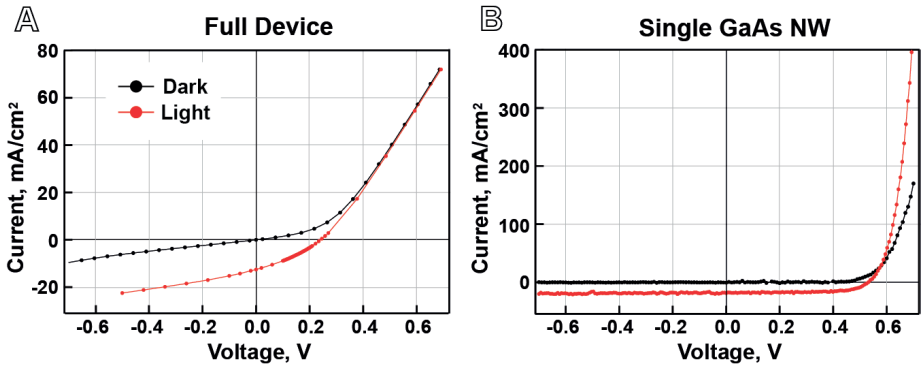


Figure 2: NW ensemble device (A) and single NW (B) IV measurements. In both cases the measurements are performed first in the dark (black curves) and then under 1-sun illumination (red curves). The current density in the case of the ensemble device is 12.5 mA/cm^2, while for a single NW 18 mA/cm^2. Series and shunt resistances (R_s and R_{sh}) are at 4.2 and 46.9 Ohm*cm2 for the ensemble device and 0.04 and 447 Ohm*cm2 for a single NW.

Figure 2B shows IV measurements of a single NW solar cell horizontally lying on an oxidized silicon substrate. The single NW solar cell and the NW ensemble device both come from a sample obtained under the same growth conditions. The active area was calculated by multiplying the NW diameter by the length of the exposed p-i-n junction, as in ref. 15 (see S4). The obtained values for I_{sc} of 50 pA (or 18 mA/cm^2) and V_{oc} of 0.55 V are significantly higher than the estimated average values from the ensemble device measurements (25 pA and 0.24 V, respectively). In addition, the ideality factor of the single NW, n=1.79, is much lower than in the case of the NW ensemble device. Comparing the single and ensemble devices, there is also one and two orders of magnitude difference in R_{sh} and R_s respectively. We attribute this difference in the electrical properties to the lack of GaAs/Si heterojunction in the single NW scheme, as opposed the NW ensemble device obtained on a Si substrate and that can induce a barrier at the interface. Here below we outline in more detail the different causes of the discrepancy between single and ensemble device characteristics:

- Electrical contact configuration: in the single NW configuration ohmic contacts do not need to be transparent. As a consequence, there are less restrictions in the material choice and ohmic contacts are more easily obtained. Since in the NW ensemble configuration the top contact must be as transparent as possible, the device can suffer from increased series resistance as compared to a direct Pd-Au contact. Contacting through the substrate might

also provide some additional series resistance and a hetero-barrier due to the valence band discontinuity between GaAs and Si [33].

- Dielectric environment: in the NW ensemble device we find that the polymeric matrix can eventually be charged. The electrostatic interaction with the matrix affects the electrical properties of the ensemble device, especially when compared to the single NW configuration.
- Difference in the light distribution within the NW core: the single NW is lying on the surface while NWs in the forest are standing and illuminated from above. This results in significantly different absorbance [16, 34].
- Intrinsic high inhomogeneity of the NWs due to the growth process.
- Presence of the non-active NWs in the ensemble device: some of the NWs could be in an open-circuit configuration. For example, during the fabrication process, few NWs can bend and break or are partially covered by the polymer. If this is the case, the corresponding area does not contribute to the overall photocurrent.

It is challenging to understand in more depth the limitations of the system by means of the traditional characterization methods. The issue of the non-uniformity of the NWs grown by VLS method was addressed in case of GaN NW LED structures by F. Limbach *et al.* [35]. The NW-to-NW fluctuations in series resistance lead to broad range in current density between them, resulting in preventing some of the NWs to emit light. Also, in the use of NWs for photoelectrochemistry experiments, it was observed that the photovoltage of the NW array photoelectrode is highly affected by the worst-performing NW [36]. Our original approach here consists of addressing some of these issues in our devices in a more systematic way by C-AFM.

3.2.Conductive AFM: Morphology and Current maps

Current mapping and single NW IV measurements were performed by C-AFM. We performed measurements in the dark and under illumination by using: a) an in-built calibrated LED lamp; b) a light source from a sun simulator. The sample for AFM measurements was obtained with the same growth conditions as NW ensemble device, as described in experimental section.

3.2.1. Surface morphology and light sensitivity

We start by comparing the topographic resolution that SEM and AFM can offer (Fig. 3A and C). We then determine the number of light-responsive NWs in that area by C-AFM. For this, we measure the same area by SEM, topographic AFM and C-AFM.

To find the same area of the NW ensemble in the different set-ups, a gold grid was evaporated onto the surface (see in supplementary information - Figure S3-2). In Fig. 3A and Fig. 3C the exact same 5 x 5 μm^2 area of the surface is presented by respectively SEM and AFM. As a reference, we highlight identical NWs with a circle and colored arrows. From both SEM and topographic AFM it is possible to clearly recognize the wires that protrude from the surface. We count a total of 42 wires for this scanned area. Next, we performed C-AFM on the same area. With the purpose of revealing the percentage of photo-active nanowires, we illuminated the sample with a white LED while applying a zero voltage between the tip and the sample. A more precise characterization with a calibrated lamp is shown in the last part of the paper (part 3.2.3). Figure 3B corresponds to the 3D topography image of a GaAs NW ensemble overlaid with the

current map (at 0 V under light) performed by C-AFM. The area between NWs is not conductive, being an insulating polymer. All NWs, being connected to the back contact, should ideally provide negative current (photocurrent) at zero bias and under illumination. The measurement in Fig. 3B reveals that not each NWs exhibits photocurrent and thus not all of them are working as a p-n junction in the ensemble. Strikingly, almost half of the NWs display an absence of the photo-current (see white arrow). Interestingly, there is a factor 2 difference when comparing the average photocurrent obtained with the characteristics of the NW ensemble and the functioning single NWs (25 pA vs 50 pA).

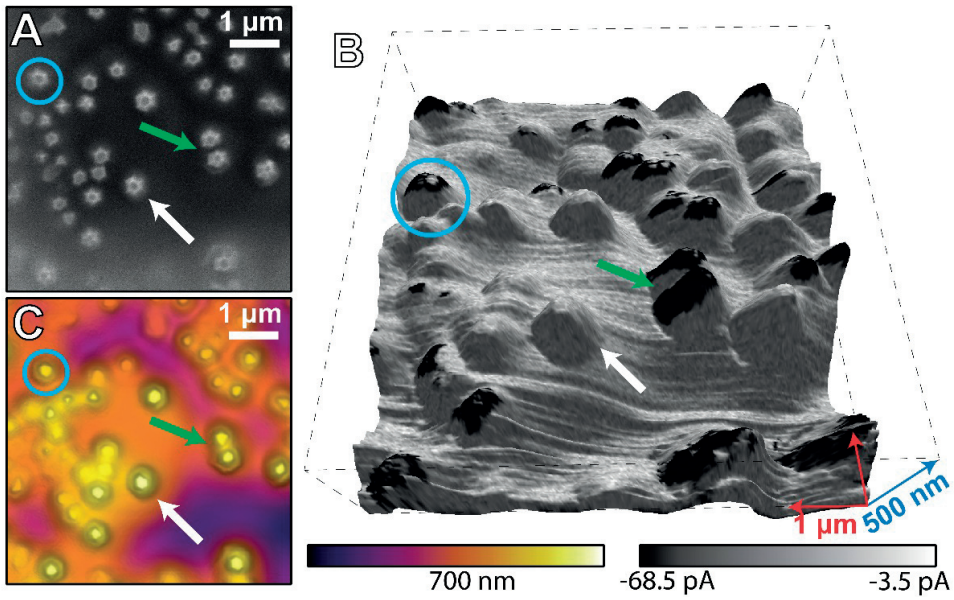


Figure 3. SEM (A), topographic/conducting AFM (B) and topographic AFM (C) images of the same surface area of GaAs NW forest. The same NWs in the three images are highlighted by arrows and circles of the corresponding colours. Image B is obtained by superimposing to the 3D surface reconstruction of the sample the photo-current measured at 0 V between tip and sample. In B, it is clear that not all the NWs are conducting nor photosensitive at the same level. In particular, in this area, only roughly 55% of the wires are light sensitive. C-AFM image is obtained in contact mode with a Pt probe while image C is obtained with standard silicon nitride probe (see experimental section). The height scale (violet-orange-yellow) corresponds to 700 nm. The current colour scale (grey scale) ranges from -68.5pA to -3.5pA. AFM image was a subject to image post-processing.

3.2.2. Scan regime – current map

Current mappings can also be performed while applying a bias between tip and sample. An example of this kind of measurements is presented in Figure 4. Here, the same area of the sample (topographic image Fig. 4A) is scanned several times in contact mode while applying different voltages between the tip and the sample (see Fig. 4B-E). The sample was illuminated with the internal LED lamp of the system to facilitate the experiment. The color scale in C-AFM is set so that for NWs exhibiting different IV characteristics, one observes different grey scale values. Negative values of the current correspond to the generation of a photocurrent, while positive values to the light emission conditions of the diodes [37]. This kind of measurement allows an estimation on the level of homogeneity of dozens of NWs. In addition, by changing the applied voltage a rough estimate of the open-circuit voltage of the NW ensemble device corresponding to the explored area can be obtained. For example in Figure 4D, most of the NWs are not detected in the current map for an applied bias of 0.5 V (the position of a NW is indicated by a red circle). Still, some of

them show either a positive or negative current (see for example the indicated blue and green circles in Fig. 4D).

From this set of measurements it is clear that, not only some of the NW p-n junctions are actually light sensitive, but that there is also a wide diversity in terms of electrical characteristics of the p-n junctions that work as photodiode. In particular there is not a unique value for the open circuit voltage but rather a distribution. The value measured in the ensemble device will thus be related to this distribution. In case of parallel connection of all NWs in one device, the current values of each NW are added to provide total current, but open-circuit voltage value is strongly affected by the lowest values.

In addition, analysis of the current maps at different applied voltage shows that the light passive NWs are still electrically active (at least, part of them). This result points to the existence of additional leakage channels for NW ensemble solar cell, which in turn reduces the device performance.

It is worth to note that the effect of the tip on electrical measurements under the light should be mentioned. One could expect shadowing or improvement in the light coupling due to plasmonic effects, depending on the incident wavelength. This is a much more complete study that we intend to perform in a follow-up study.

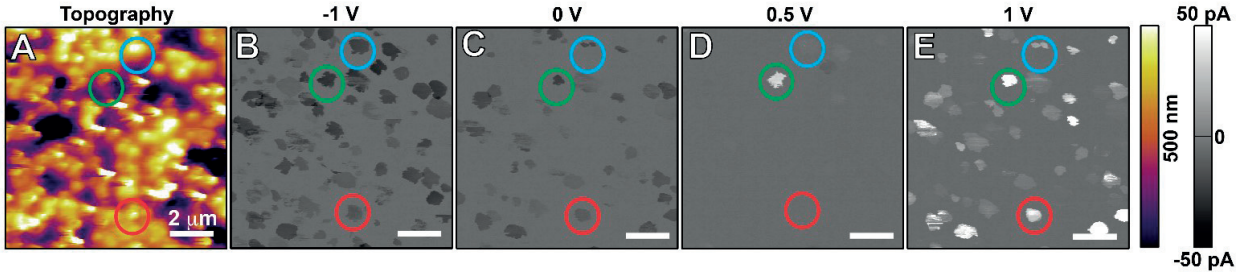


Figure 4. Topography (A) and current maps (B-E) of GaAs NWs ensemble obtained scanning the surface in contact mode while applying different voltage between tip and sample under light illumination. The scan area is the same in all images (images are not drift corrected). The recorded current values in images B-E are presented in grey colour scale and range from -50 pA to +50 pA. Circles of different colour highlight the positions of selected NW in different images. At approximately 0.5 V of bias, most of the NWs do not conduct significantly, although few deviate from the general trend (see for example blue and green circles in D). This reflects the intrinsic inhomogeneity of the electrical properties of the GaAs NWs and the fact that the V_{oc} is unique to each NW. Height data scale range (Violet-orange-yellow colour scale) corresponds to 500nm.

3.2.3. Single NW current-voltage measurements and ensemble properties

Unlike the previous experiments, single NW IV measurements were performed using a Bruker ICON system and introduced an external light source through the built-in optical microscope. The spectrum of the introduced light can be found in SI (see Fig. S3-1). It is worth noting that the light intensity in the C-AFM was checked for being large enough to provide a fully saturated V_{oc}. By probing the top of the single NW with the AFM tip, we can measure the individual IV curve of each p-n junction separately. In order to illustrate the inhomogeneity in the sample, we extracted the IV curves from 50 NW p-i-n junctions over 4 surface areas of 5x5 μm^2 found in the same sample as shown in Fig. 3 and 4. In Fig. 5, the V_{oc} distribution is shown and it ranges from 0.25 to 0.6 V. While most of the p-i-n junctions provide a high V_{oc} around 0.5 V, a very small number of junctions underperforms with V_{oc} values as low as 0.25 V.

While one may think that a NW p-i-n junction with a small V_{oc} may underpin the overall V_{oc} of the device, its contribution may become insignificant. The V_{oc} corresponds to the voltage at which the total current of the device is null, and in a parallel-connection configuration it can be described as:

$$\sum_{i=1}^{n} I_i(V = V_{oc}) = 0$$

where *n* – is the number of NWs, and I_i – current of i-NW at V=V_{oc}. This equation highlights the importance of the ensemble measurements and the impact of an underperforming NW junction.

In the inset of Fig. 5, we show examples of IV characteristics of two individual junctions from our statistical sample along with the calculated output of what would be a device with all the 50 junctions connected in parallel (more details in SI – S6). Strikingly, the overall performance is not as dramatically affected by the underperforming junction as one may initially expect. The reason relies on the shape of the individual IV characteristics. In particular, we observe a large series resistance in the individual cells that improves with illumination intensity (see curves under different illumination conditions in SI – Fig. S3-3). This most probably comes from the p-doped core and the presence of a barrier at the GaAs/Si hetero-interface. This heterobarrier is also reflected by the large ideality factor of 5.96. We plan to further investigate the role of the interface between GaAs NWs and the Si substrate as it can seriously affect the integration of III-V solar cells on Si. Thanks to the large series resistance, the rise in current at forward bias (i.e. V>V_{oc}) is not as sharp as in ideal diodes. As a consequence, the small number of poor performing junctions is being able to easily compensate for the photocurrent of the other individual parallel junctions.

We have calculated the effective open circuit voltage of the combined IV characteristics of the 50 NW devices. We obtain <V_{oc}> = 0.5V for the area investigated with the C-AFM. This value is much higher than one obtained in the NW ensemble device (0.24 V). We believe that this discrepancy is to the due to small number of NWs with low V_{oc} for the investigated areas and the large series resistance coming from the tip contact and the lower illumination intensity. In addition, it is possible that the NW ensemble device also exhibits losses from a non-optimized fabrication process such as leakages around the edges and through the non-photoactive NWs, which could also limit the performance of NW ensemble solar cells. In any case, the C-AFM technique allows us to identify high quality areas that could derive in highly performing devices. Since C-AFM is non-destructive method and can be applied directly before the fabrication of the top transparent contacts.

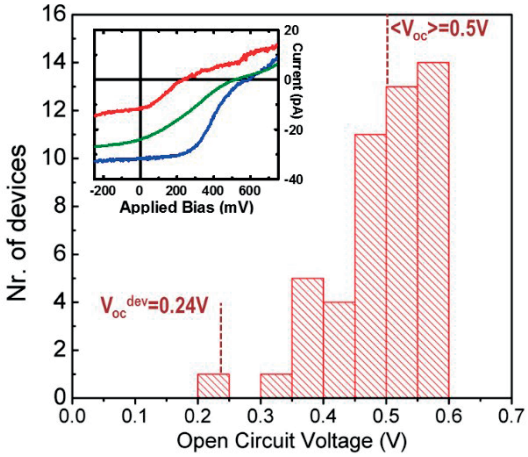


Figure 5. V_{oc} statistics of ensemble of NWs by C-AFM. The calculated combined V_{oc} of the NWs connected in parallel (<V_{oc}>) and the V_{oc} of the NW ensemble device (V_{oc}^{dev}) are marked on the graph by vertical lines. The inset shows 3 IV curves under the light – the worst performing NW junction (red) and the best performing NW junction (blue) from the obtained statistics plus the calculated total IV of the virtual device (green) with the average current (total current divided by 50, the number of NW devices).

4. Conclusions

In conclusion, we have demonstrated the use of C-AFM to characterize the individual electrical properties of nanowire p-i-n junctions in an ensemble solar cell device. We obtained the statistical characteristics and a quantified measure of the inhomogeneity spread in the large ensemble. Our method provides the link between the individual NW and the NW ensemble solar cell performance and the importance of homogeneity in the overall device performance. We also show that few poor-performing single NWs may not have a dramatic effect on the ensemble device characteristics, but rather localized leakage paths. By comparing IV curves of NWs connected to or detached from the substrate, we outlined the influence of the interface barrier between GaAs NWs and the Si substrate, as well as the top transparent contacts. These results indicate some of the drawbacks of using self-assembly growth approaches for solar cells. Optimizing fabrication process and quality of the NWs in the ensemble is the path towards utilizing this technology in terrestrial photovoltaics, and C-AFM a valuable non-destructive tool towards this accomplishment.

Acknowledgements

We would like to thank NanoTera for funding through project Synergia, ERC for the funding of the StG 'UpCon' and H2020 ITN project Indeed. JB Leran and H Potts are also acknowledged for technical support in the MBE machine. M.R. acknowledges the Swiss National Science Foundation for the funding of the Early Postdoc.Mobility fellowship. N.V. acknowledges the Swiss Government Excellence Scholarship. EAL acknowledges the support from the SNF Ambizione Energy program and the research program of FOM, which is financially supported by The Netherlands Organization for Scientific Research (NWO).

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3.2 Characterization of losses linked to series resistances using light concentration

This part of the chapter focuses on the impact of series resistance on the electrical characteristics of NW based solar cells. NW solar cell structure consists of a NW-based radial p-n junction together with the electrodes, passivation and polymer layers. The series resistance and its impact on the electrical characteristics is analyzed with an equivalent circuit model, each element of which should correspond to one or more elements of the device. This is presented and described here below.

Dark IV characteristics of the solar cell can be explained by a standard diode, following the Shockley ideal diode model [105]. Under illumination, an equivalent circuit can represent the solar cell, where the current source is set in parallel with the junction. In real devices, series and shunt resistance losses are added to the circuit. The series resistance depends on the resistivity of the materials (active part, electrodes) and the interfaces between them (heterointerfaces, metal-semiconductor, etc.). The shunt resistance is described by the presence of the leaks and/or short circuits in the device. The correct characterization of these resistances is key for the improvement in the overall device.

In this study, we focus on the contribution of the series resistance to the power losses of the solar cell. For this reason, here we do not discuss losses produced by the non-uniformity of NWs as these contribute to the shunt resistance. To illustrate the role of the series resistance in a solar cell, we draw an equivalent circuit with the corresponding diodes and resistances. **Figure 3-4** shows the sketches of an III-V planar and NW based solar cells together with the two corresponding equivalent circuits. The equivalent circuit ① represents basic configuration with p-n junction diode D_{p-n}, photocurrent source J_g and front R_f and rear R_r contact series resistances. This circuit is valid if the electrical contacts are optimized and the series resistances can be described as ohmic [82]. Traditional planar PV devices are usually studied using this equivalent scheme (plus parallel losses).

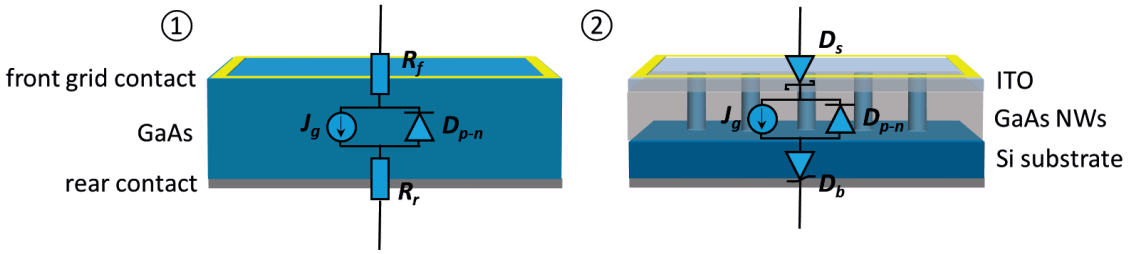

Figure 3-4 A simplified scheme of the planar and NW-based solar cells together with its equivalent circuits: ① - classic; ② - with non-linear series effects.

Equivalent circuit ② differs from the circuit ① by the existence of the two additional diodes at the rear and front parts of the solar cell. The NW-based solar cell exhibits two additional surfaces: the handing substrate (Si in our case) and the front transparent contact that collects the current from all individual NW devices. Existing interfaces in NW based solar cell can act as additional (heterojunction or Schottky) diodes connected in series. The barrier diode D_b corresponds to the interface between NWs and substrate. A similar system was studied by Hoheisel *et al.* [106]. In their case, they studied a GaAs planar solar cell with an AlGaAs back surface field (BSF) and window layer. This layer can introduce a potential barrier in valence and conduction bands for majority carriers. The corresponding diode follows an "S" shape IV curve. The Schottky diode D_s corresponds to the ITO/GaAs interface. This junction is not ohmic as there is a substantial potential barrier between them. The ITO/GaAs interface is known to be a photoactive Schottky diode that even generates a photovoltage [107]. If the Schottky diode direction is opposite to the NW p-n junction, a decrease in V_{oc} will occur. This effect could only be reduced by optimizing the TCO material deposition on

GaAs and by reducing the Fermi level pinning at the GaAs surface [108]. The characteristic surface Fermi level pinning for GaAs occurs near the center of the energy bandgap [109]. This leads to the intermediate barrier height at the interface – not high enough to form a good rectifying contact nor low to form an ohmic contact. It is worth to note, that the series resistance R_s is a part of this additional diode characteristic.

The literature reporting on the accurate description and characterization of the series resistance (linear and non-linear with the voltage) is broad [84,110–112]. IV characterization in the dark along with a one or two diode model fitting is widely used. In such a case, both series resistance and pure p-n junction properties can be extracted. However, it has been shown that this method gives large errors in series resistance estimation [84]. In addition, NW based solar cells can involve more elements than just in the two-diodes, thus the fitting does not work properly [113]. We believe the most robust and reliable method to extract series losses should include the light intensity dependence. Measuring IV curves under varying light intensity results in a number of IV curves shifted by the corresponding photogenerated current density, J_g. In an ideal solar cell, J_g is proportional to the light intensity. The plot $J_g vs\ V_{oc}$ provides the resistance-free dark IV curve. One can then compare this pseudo-IV curve to the experimental in the dark and under 1 sun to extract the lump series resistance of the device in operation. This further analysis of the IV characteristics provides information of the carrier transport limiting mechanisms in the p-n junction.

In this subchapter, the electrical characteristics of GaAs NW based solar cells were analyzed by measuring light intensity dependent IV characteristics. Measurements of IV-curves were carried out on a pulsed solar radiation simulator with intensities up to 1000 suns. **Figure 3-5** shows the optical layout of such a system. Each of four xenon lamps is supplied with a band-pass glass filter, corresponding to a specific part of the spectrum. The simultaneous ignition of lamps forms a light pulse with a quasi-constant part of 1 ms. This mode is used for the characterization of the solar cells with a low lifetime of photogenerated carriers (typical for III-V solar cells). A homogenizer made from the white ceramic material helps to obtain high light homogeneity and to further increase the light intensity.

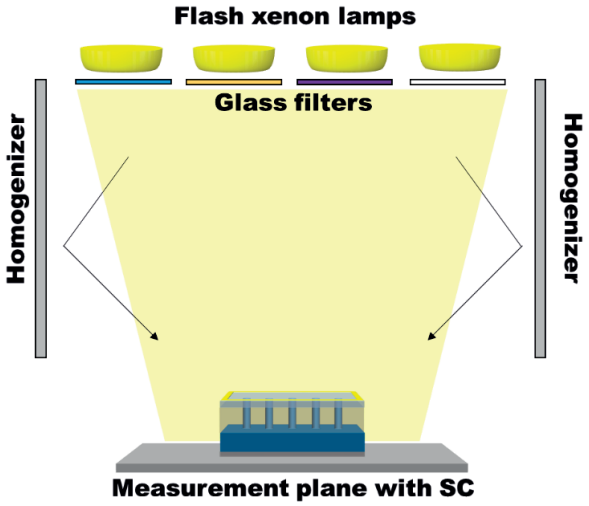

Figure 3-5 Optical layout of flash illumination system.

The analysis of concentration dependences for GaAs NW based solar cells allowed us to determine the photo-generated current at 1 sun and obtain pseudo light IV curve, free from the series resistance. In addition, by fitting resistive-free dark IV curve ($J_g - V_{oc}$ characteristic) with the double-diode fit model,

dark saturation current densities for diffusion and recombination carrier transport mechanisms were calculated. Interestingly, saturation and, then, drop of V_{oc} at high intensities were found by this method. We consider this effect as a proof of reverse Schottky diode at the ITO/n-GaAs interface in our solar cell. Overall, the light concentrating method helps to separate the study and optimization of NW p-n junction from the post-growth fabrication steps that can introduce series losses in the solar cell. To the best of our knowledge this is the first time this method is used in III-V NW based solar cell analysis.

3.2.1 Paper included in this chapter

This work is under preparation (the target journal – Nanotechnology, special issue "Focus on Nanowires").

This chapter presents the pre-print version of the manuscript. The independent bibliographic references for the manuscript are attached in the end of the corresponding section. The aforementioned bibliographic references differ from the general bibliography of this thesis by means of a different format. For instance, [1] refers to the first reference in the manuscript, while [1] refers to the first reference in the general bibliography presented at the end of this thesis.

TITLE

Deep analysis of photovoltaic properties of GaAs nanowire based solar cells using concentrating light

AUTHORS

Dmitry Mikulik*, Mikhail Mintairov*, Ian Nachemson, Valery Evstropov, Pablo Romero-Gomez, Maxim Shvarts and Anna Fontcuberta i Morral

*Equally contributing authors

MY CONTRIBUTION

- I simulated band alignment in studied structures using Nextnano
- I fabricated NW based solar cells
- I took active part in designing the experiment, interpreting and analyzing the results
- I wrote part of the paper

Extraction of p-n junction properties and series resistance in GaAs nanowire based solar cells using light concentration

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Received xxxxxx
Accepted for publication xxxxxx
Published xxxxxx

Abstract

Series resistance in solar cells originates from deficiencies at the contact or absorber level and constitutes an important limitation to the device conversion efficiency. Quantifying it is the first step for the reduction. In this work, we provide a new way to assess the series resistance in nanowire-based solar cells, which significantly underperforms predicted theoretical efficiency. We illuminate the devices at different levels of light intensity (from 1 to 1000 suns), which gives us insight in the carrier transport and series losses mechanism. We demonstrate the method on a device obtained by self-assembled GaAs nanowire p-n junction arrays on silicon. The linear lumped equivalent of series resistance of $14.8\,\Omega \cdot cm^2$ can be attributed to the heterointerfaces in the device. Thus, this analysis helps to distinguish the intrinsic response of the nanowire p-n junction and from the series resistance effects. More generally, this method provides a mean of optimizing the efficiency in next generation solar cells where contacts still have to be developed.

Keywords: GaAs, nanowires, concentrating light, interfaces

1. Introduction

In recent years, semiconductor nanostructures have attracted great interest in photovoltaics (PV) due to many advantages such as ultralow reflectance and excellent light trapping [1]. One of the most interesting nanostructures for solar cells is semiconductor nanowires (NWs) [2]. NWs utilize radial or axial p-n junction configurations along with a submicron critical dimension and have shown to greatly enhance light absorption. Several papers have reported conversion efficiencies up to 18% for III-V NW based solar cells [3–5]. With the possibility to fabricate III-V NWs on Si substrates, recent progress in PV opens new perspectives

in material savings and reducing the cost of III-V single junction and tandem solar cells [6]. However, the conversion efficiencies of these novel structures are still below the values of the planar III-V solar cells [7].

Several challenges in NW based solar cell development should be highlighted, such as parallel connection of NWs in array, optimization of the transparent conductive oxide (TCO) top electrode and the presence of heterointerfaces. Recently, we showed the detrimental effect of non-uniformity in parallel-connected GaAs NW arrays on the total efficiency of the device by means of conductive-probe atomic force microscopy [8]. Besides parallel losses due to non-uniformity, interfaces and contact resistance in NW based solar cell structures introduce series losses which need to be revealed and analyzed. Unlike conventional III-V semiconductor solar cells, two additional interfaces can be highlighted in NW based solar cells. Firstly, in the case of growth on a Si substrate, the III-V/Si heterointerface can play a detrimental role in the electrical properties of the solar cell. Secondly, the need for a TCO layer leads to the additional interface between III-V NW tips and TCO such as indium tin oxide (ITO), indium zinc oxide (IZO) etc. More importantly, analysis of the intrinsic p-n junction properties in NW based devices is difficult in the presence of non-linear series losses on heterointerfaces. Therefore, detailed analysis of the series electrical losses in NW based solar cells should be performed.

Different electrical characterization methods can extract series losses in the PV device [9]. Among them, characterization of solar cell properties by applying concentrated light with up to 1000 suns is widely used in planar single-junction and multi-junction PV, and therefore such measurements should also be used for NW based solar cells [10]. Nowadays, several methods to analyze concentration dependences are present and used to extract important parameters of solar cells. For example, open-circuit voltage (V_{oc}) plotted against the photo-generated current density (J_g) generally represents the resistance-free dark current-voltage characteristics (IV) of the solar cell [11]. The analysis of the dark IV helps to determine the saturation current density (J_0) for different current flow mechanisms through the p-n junction of the solar cell, such as diffusion current and recombination current mechanisms [12]. In addition, resistive losses and effective lifetimes can be found from the concentration dependences [9,13].

Above mentioned methods are in general applied for planar solar cells. However, very few reports describe the behavior of NW based devices under concentrated light (or laser), where the evolution of main solar cell properties (V_{oc}, short-circuit current density J_{sc}, fill factor FF and efficiency η) with the increasing light concentration is analyzed experimentally or theoretically [4,6,14,15].

Here, we provide an analysis of the GaAs NW based solar cell properties using concentration dependences that allows to disentangle the lumped series resistance of the device from the p-n junction properties. In this work, the term “lumped series resistance” is used to describe all elements in solar cell structure excluding p-n junction. We obtain the resistance-free dark ($J_g - V_{oc}$) and light IV curves (also called pseudo IVs) of the device, highlighting the diffusion and recombination IV curve segments, as well as calculate the dark saturation currents. By comparing the pseudo and experimental IV characteristics, series losses can be quantified in terms of linear lumped equivalent of series resistance. Finally, the presence of interace barriers in the NW based solar cell, such as Si/GaAs and GaAs/ITO, is discussed. It is worth noting that this analysis is the first of its kind for NW based solar cells.

2. Experimental

Core-shell p-i-n GaAs NWs were grown on B-doped (111) Si substrates with resistivity < 0.03 Ω·cm by self-assembled Ga-catalyzed vapor-liquid-solid (VLS) method using Molecual Beam Epitaxy (MBE).

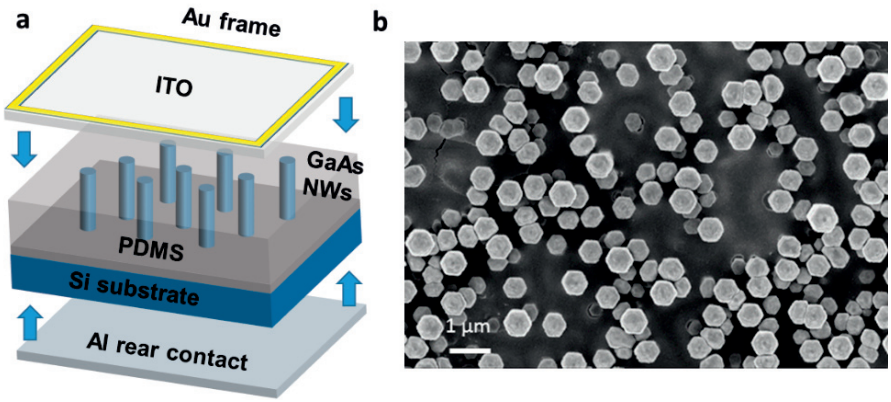

Figure 1. **a)** A scheme of GaAs NW based solar cell on Si substrate; **b)** top view SEM image of the device.

A Si substrate with a native silicon oxide mask was placed into the MBE system for the following growth. The growth method is described in details in reference [16]. Briefly, 5 µm long p-doped GaAs NWs were grown using the growth conditions reported in reference [17], with addition of Si as a dopant. Next, the growth conditions were switched for the shell growth by decreasing the temperature and increasing V/III ratio. This facilitates the growth on {110} side facets and intrinsic GaAs shell of the thickness of 100 nm was grown. Finally, 30 nm of outer-shell n-doped GaAs was grown using Si as a dopant, similar to reference [18]. The same Si fluxes used for the doping of the core and the shell lead to a nominal doping concentration of 10^{18} cm^{-3} and 5×10^{18} cm^{-3} when calibrated with secondary ion mass spectrometry (SIMS) on (100) GaAs substrates.

For the planarization of the top surface, GaAs NWs were embedded in a Polydimetylsiloxane (PDMS) transparent polymer film. After mixing the monomer with the curing agent (5 to 1 in proportion) and degassing, the PDMS solution was diluted by Hexane for decreasing viscosity in order to prevent mechanical damaging of NWs during spin coating at 5000 rpm. An SPTS Advanced Plasma System (APS) module was used for SF_6 plasma etching to reveal the tips of GaAs NWs for further front contact formation. A sputtered ITO layer of 300 nm thickness was used as a full surface covered transparent electrode. For the rear contact, a 200 nm thick layer of Al was sputtered on the back of p-Si substrate. Ti/Au grid contacts were evaporated on top of the sample for area definition and electrical characterization.

The morphology of the samples was analyzed with scanning electron microscopy (SEM) using Zeiss GeminiSEM operating at 3 kV. ***Figure 1*** shows a scheme of the device fabricated on Si substrate (a) and the top view SEM image of the structure (b). Using this growth method, we were able to fabricate NW based solar cell with the surface area of 13.9 mm^2. Nextnano software package was used to simulate band alignment of the GaAs p-n junction and the hetero interfaces [19]. To simulate the band bending in the structure exactly, the 1D Schrödinger-Poisson equation was solved self-consistently. Measurements of IV curves were carried out on a pulsed solar simulator. The illumination level on the device under test and its temperature were monitored at I-V curve recording. The maximum irradiance was about 1000 suns.

3. Results and discussion

Barrier potentials can be identified by simulating band alignment in semiconductor structures. ***Figure 2*** shows the band alignment of Al/p-Si/p-i-n GaAs/ITO structure, where an additional Schottky barrier of 0.5 eV was introduced for visualizing the possibility of a potential barrier at the non-optimized n-GaAs/ITO interface. In ***Figure 2,*** the current in external circuit is equal to photogenerated current, and therefore the single Fermi level is shown. Zhang *et al*. reported an increased contact resistance in case of ITO contacts to

n-GaAs NWs and attributed it to the Schottky barrier [20]. In addition, as can be seen from ***Figure 2***, a barrier potential for majority carriers is formed in the valence band at the interface between Si and GaAs. The height and the shape of the barrier depend on the band offset, permittivity and doping concentration of the semiconductor layers. Assuming doping concentrations of 10^{18} cm^{-3} for Si and GaAs, barrier height equal to 0.3 eV is obtained. Hoheisel *et al.* found that internal majority barriers effect the IV characteristics of the solar cell by disturbing the flow of majority carriers [21]. The barrier may act as an additional diode in the equivalent circuit of the solar cell with a quasi-exponential I-V characteristic. Since the Si/GaAs hetero barrier is located at the rear part of the solar cell, we assume the photosensitivity might be negligible. Opposite to that, the front interface such as the n-GaAs/ITO with Schottky barrier characteristics can generate a photocurrent [22].

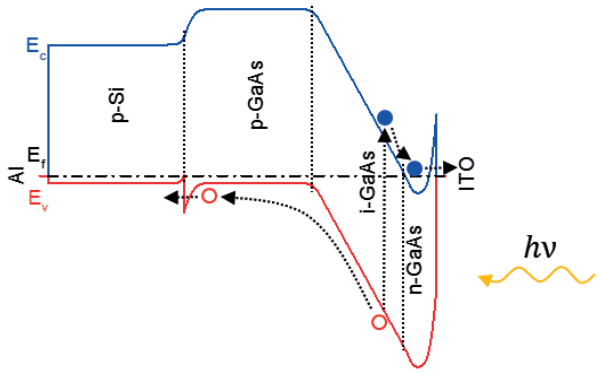

Figure 2. One-dimensional band diagram of the solar cell structure Al/p-Si/p-GaAs/i-GaAs/n-GaAs/ITO along the NW axis. Photogenerated electron (blue filled circle) and hole (red empty circle) flows through the interfaces are indicated.

The addition of the series resistances combined with the interface barriers reduce the total performance of the solar cell. To detect and evaluate losses originating from the barrier potentials, intensity-dependent IV measurements were conducted. A numerical fitting model was used to obtain the photo-generated current density J_g intrinsic to the p-n junction, free from the series resistance.

3.1. A numerical model

The IV response of a solar cell under light may be modeled as a photoactive current source in parallel with a diode, with added series resistance. The shunt resistance is assumed infinite in this model, and can therefore be neglected. When no current is flowing through the device, the voltage is termed open-circuit voltage, V_{oc}. Moreover, the current flowing through the device at zero voltage is the short-circuit current density, J_{sc}. Lastly, the photo-generated current density is termed J_g. Hence, the IV curve under the light is defined by:

$$J = J_g - J_0\left(e^{\frac{V+JR_s}{nkT/q}} - 1\right) \quad (1)$$

where n – diode ideality factor, k – Boltzmann coefficient, T – temperature in Kelvin, q – elemental charge, R_s – linear lumped series resistance and J_0 – dark saturation current density. As well known, J_g increases linearly with the illumination intensity C, while the V_{oc} shows a logarithmic dependence [12]. We may explore the relationship between J_g and J_{sc} by considering the short-circuit regime, i.e. $V = 0$ and $J = J_{sc}$. ***Equation 1*** transforms into:

$$J_{sc} = J_g - J_0(e^{\frac{J_{sc}R_s}{nkT/q}} - 1) \quad (2)$$

Usually, the approximation $J_g \cong J_{sc}$ is used for the photo-generated current density determination. This assumption is valid in case of low R_s and J_0. However, in not optimized solar cells these parameters may be much higher and the diode term cannot be neglected. The effect of series resistance on the relationship between J_{sc} and light intensity (and J_g, respectively) was found to be significant at high intensities, while at low intensities this effect is negligible [23]. Therefore, to obtain photo-generated current density we can use $J_{sc} - J_g$ dependence from ***Equation 2*** in the neighborhood of zero, where the light intensity is low.

To simplify ***Equation 2***, let us consider $J_{sc} \to 0$, where the exponent function of the diode term can be re-written as:

$$\lim_{J_{sc}\to 0} e^{\frac{J_{sc}R_s}{nkT/q}} \to \frac{J_{sc}R_s}{nkT/q} + 1 \quad (3)$$

Therefore, J_{sc} and J_g are equal to each other in the neighborhood of zero with certain error ε:

$$J_{sc}(1+\varepsilon) = J_g \quad (4)$$

where $\varepsilon = \frac{J_0 R_s}{nkT/q}$. The approximation error ε depends on J_0, R_s and n, and therefore can be quantitatively estimated. In studied samples, the maximum percent error does not exceed 1% and thus, J_g is considered approximately equal to J_{sc} in the neighborhood of zero. This approximation forms the basis of the following analysis.

3.2. Proportionality between light intensity and photo-generated current

GaAs NW based solar cells were measured under a flash solar simulator to get the IV curves' dependence on the light intensity. ***Figure 3a*** shows 6 IV curves with the light intensity C from 1 to 180 suns. One can find that the IV curve of the device shifts up with increasing light concentration, signifying an increase of J_{sc}. Up to the light intensity of 20 suns, V_{oc} increases as well.

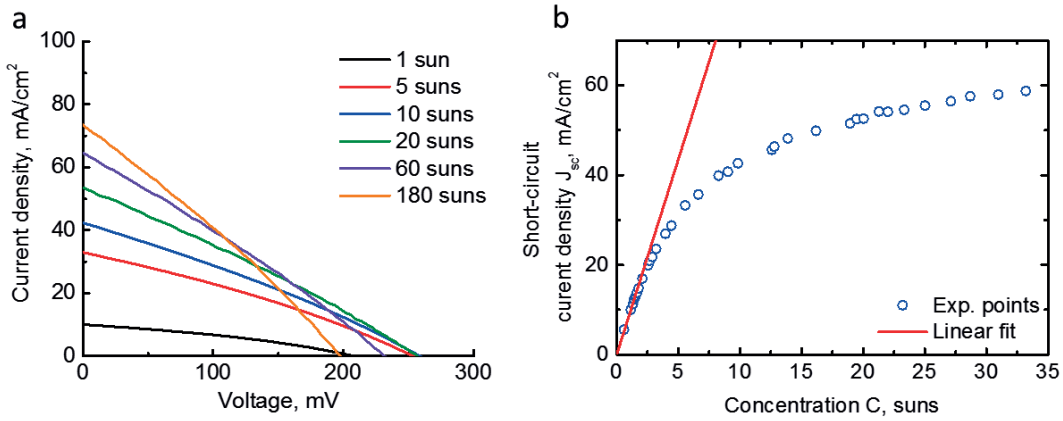

Figure 3. a) IV curves of GaAs NW based solar under 4 lamps flash solar simulator; **b)** $J_{sc} - C$ characteristic with linear $J_g - C$ dependence ($J_g = J_g^{C-1} * C$).

Examination of the IV curves reveals that the experimental J_{sc} of the solar cells is not proportional to the light concentration. From the obtained IV curves, J_{sc} values can be extracted and plotted versus light intensity in suns. ***Figure 3b*** shows $J_{sc} - C$ plot with sublinear dependence starting from ~ 2.5 suns of light

intensity. Using above mentioned linear fitting of the experimental points below 2.5 suns can give us a photogeneration current density at 1 sun as a linear coefficient of proportionality between light intensity and photo-generated current density ($J_{sc} \approx J_g = J_g^{C=1} * C$). High resistance in the solar cell structure suppresses the further linear increase of the photo-generated current density. However, extrapolation of linear fit beyond 2.5 suns helps to obtain J_g at the whole range of intensities (red line in ***Figure 3b***). The coefficient of proportionality $J_g^{C=1}$ is used to convert $V_{oc} - C$ characteristic into $V_{oc} - J_g$ characteristic, which is analyzed onwards.

3.3. $V_{oc} - J_g$ Dependence

In general, describing the solar cell behavior with a single diode model reveals a diode ideality factor n between 1 and 2, a combination of both diffusion and recombination mechanism at the same time. In many cases, due to imperfections in device structure, the ideality factor can be even higher than 2, as shown in many III-V NW based solar cell reports [8,15,24–28].

However, analyzing the same device with the double-diode model would reveal the standard values of $n = 1$ and $n = 2$, which is then interpreted as diffusion for the first diode and recombination for the second [29]. The influence of each mechanism on device operation can be estimated by the dark saturation current densities, J_{01} and J_{02}.

Here, we show the $V_{oc} - J_g$ dependence measured under different illumination intensities. By plotting current density in log scale, we can use the classic double diode fit model to extract main parameters of the solar cell without resistive losses according to:

$$J_g = J_{01}\left(e^{\frac{V_{oc}}{kT/q}} - 1\right) + J_{02}\left(e^{\frac{V_{oc}}{2kT/q}} - 1\right) \quad (5)$$

It is worth to note that ***Equation 5*** represents resisitance-free dark IV curve if replacing $J_g \rightarrow -J$ and $V_{oc} \rightarrow V$.

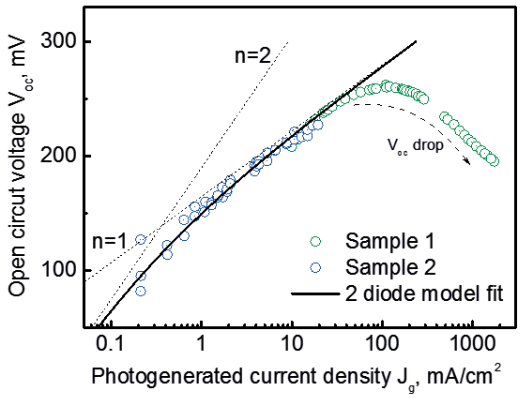

Figure 4. The $V_{oc} - J_g$ data points for GaAs NW based solar cells, shown together with the double-diode model fit.

Figure 4 shows the $V_{oc} - J_g$ experimental points of two GaAs NW based solar cells with GaAs NWs from the same growth batch. Interestingly, both series of experimental points can be fitted with the same double diode model fit. It proves the formation of the same p-n junction in NWs for two solar cells, operating in different current ranges. The saturation current densities for diffusion and recombination mechanisms are

1.3 μA/cm^2 and 23 μA/cm^2 respectively. Such high values for the saturation current densities reveal imperfections in p-n junction itself and the absence of surface passivation. Aberg *et al.* showed 2000-fold decrease in J_{02} after applying AlGaAs passivation on GaAs NWs [3]. The reduction in leakage currents results in the increase of V_{oc}. Except for those two components of the IV curve, an additional diode with $n > 2$ can be observed at low currents (not shown on ***Figure 4***). Such an ideality factor originates from a trap-assisted tunneling carrier transport mechanism. This phenomenon can be explained by considering the NW radial p-n junction as an ultra-thin PV device [30]. Defect-assisted tunneling and shunting under low illumination has been theoretically predicted in devices with thickness smaller than both the depletion width and diffusion length.

IV analysis of optimized planar GaAs solar cell gives a ratio J_{02}/J_{01} of around 10^9 [31]. However, in the NW case this ratio is 8 orders of magnitude lower. This discrepancy may stem from the device geometry, in which the ultra-thin p-n junction renders the diffusion mechanism insignificant. Instead, both current mechanisms are suspected to relate to recombination of the carriers in the space charge region at different energy trap levels – shallow ($n = 1$) and deep ($n = 2$) levels.

The saturation and subsequent drop of V_{oc} is clearly seen at high currents above 100 mA/cm^2 (high illumination intensity), which cannot be fitted with the double-diode model. It is worth to note that the IV curve of a p-n junction diode cannot have segments with the ideality factor lower than the unity, however, in the region above 100 mA/cm^2, $n < 1$ is found. Such a turnaround point in the $J_{sc} - V_{oc}$ characteristic was previously explained in planar Si solar cells with imperfect electrical contacts [32]. The electrical contact can be described by a parallel connection of a Schottky diode and shunt resistance. At 1 sun, a complete shunting of this contact leads to ohmic behavior. However, at high illumination the Schottky diode cannot be shunted completely, resulting in an increased photovoltage, which is opposed to the p-n junction one. In addition, a turn-around point in suns-V_{oc} characteristics can be attributed to internal barriers for carrier transport, as was shown for a-Si/c-Si interface in Si heterojunction solar cells [33].

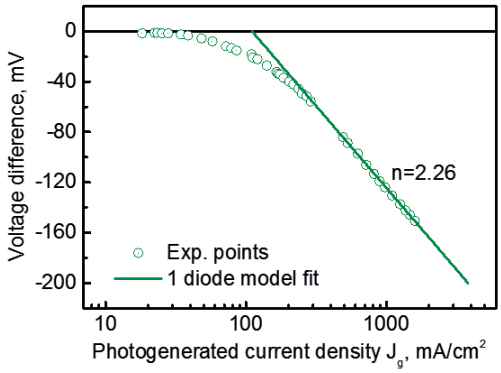

Figure 5. Result of voltage subtraction of experimental $V_{oc} - J_g$ characteristic from fitted one (see **Figure 4**)

The difference between the fit and the experimental data points in the high current regime above a turnaround point is plotted on ***Figure 5***. An ideality factor higher than unity ($n = 2.26$) was found. It can be explained by the voltage sum of the Schottky diode at the GaAs-ITO interface and p-Si/p-GaAs isotype hetero-barrier diode. At high currents, the Schottky barrier formed at the GaAs-ITO interface starts to play significant role and even dominates over the p-n junction diode operation. Furthermore, the detrimental effect of the heterointerface on carrier flow becomes apparent only at high currents, when an increased

rate of photogeneration causes a reduction of the surface potential at the heterobarrier and thus an increase of the effective valence band barrier [33].

3.4. Resistance-free IV curve

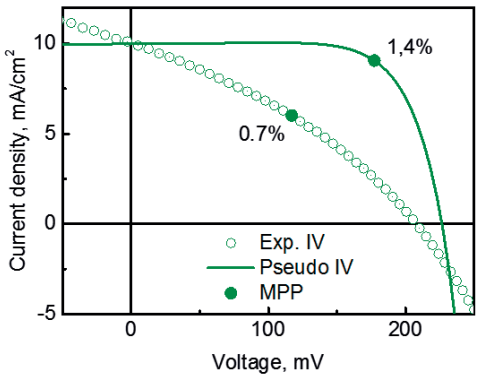

Figure 6. Experimental and pseudo IV curves of GaAs NW based solar cell. MPP is maximum power point.

One of the most important photovoltaic characteristics is the $V_{oc} - J_g$ dependence. In general, this dependence gives the dark pseudo IV curve of the diode, free from series resistance, due to measurements in the open-circuit regime [11]. To get rid of the resistivity effects in the short circuit current measurements under different light intensity, we plot it using linear fitting parameter $J_g^{C=1}$. ***Figure 6*** shows the pseudo IV curve obtained from $V_{oc} - J_g$ measurements and then shifted by J_g (for $C = 1$) and real (experimental) light IV curve at 1 sun of the GaAs NW based solar cell. Maximum power points (MPP) are shown on both IV curves.

The curve, constructed from the intensity dependent IV measurements, indicates a resistive-free efficiency of 1.4%, which is significantly higher than 0.7% of the experimental efficiency at 1 sun. The main impact of the series resistance is to reduce the FF. The lumped series resistance R_s can be estimated by the voltage difference in the maximum power point of the experimental IV curve [23]:

$$R_s = \frac{\Delta V}{J_m} = 14.8\,\Omega \cdot cm^2 \quad (6)$$

In addition, two obvious differences between two IV curves on ***Figure 6*** should be commented. First, one can find a significant drop of V_{oc} from the pseudo IV value to the experimental IV one. We speculate that it is an evidence of the current leakages related to the tunneling through the p-n junction at low currents (low light intensities). Furthermore, this tunneling current mechanism explains the second difference - excess current at negative bias in the experimental IV curve, which is not taken into account in our double-diode fitting model.

4. Conclusions

Overall, the analysis of concentration dependences for GaAs NW based solar cells allows to determine the photo-generated current at 1 sun and obtain the pseudo IV, free from series resistance. In addition, by fitting the resistance-free dark IV curve to the double-diode model, dark saturation currents for diffusion and recombination carrier transport mechanisms were calculated. It was established that the ratio of recombination to diffusion saturation current fo GaAs NW based solar cells was 8 orders lower than for a planar GaAs solar cells. This discrepancy may stem from the device geometry, in which the ultra-thin p-n

junction renders the diffusion mechanism insignificant. A drop of open-circuit voltage at high currents illustrates the presence of the photo-active Schottky barrier at ITO/n-GaAs interface, as well as heterobarrier between Si substrate and GaAs NWs. Finally, the comparison of experimental and calculated resistive-free (pseudo) IV curves allows to obtaine a value of the linear lumped equivalent of series resistance, $R_s = 14.8\ \Omega \cdot cm^2$.

This method helps to separate the study and optimization of the p-n junction from post-growth fabrication steps, that can introduce series losses in the solar cell.

Acknowledgments

This work was supported by the Swiss National Science Foundation under grant 200021_172547 and Nanotera under grant Synergy, as well as by Marie Curie 'R2R-3G' H2020. M.A. Mintairov and M.Z. Shvarts would like to thank the Russian Science Foundation (Grant №17-79-30035).

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Chapter 4 The use of Electrochemical Impedance Spectroscopy for surface states study

Dangling bonds and defects at the semiconductor surface can introduce losses in solar cells. III-V planar devices utilize well-developed lattice-matched semiconductor materials with larger band gap for a sustainable surface passivation [114]. The issue or surface and interface states becomes much more important in the case of nanowires, due to their high surface-to-volume ratio. The performance of unpassivated NW devices is limited due to the existence of charge traps on the NW sidewall facets, which results in the near-surface depletion and recombination of charge carriers at the surface. These issues are especially relevant for the case of NW-based axial junctions. One of the options to circumvent the negative effects of surface and interface recombination is the use of dielectric material passivation [115,116]. The key advantages of dielectric materials are transparency to visible light, maturity (well-studied in microelectronics and Si PV) and availability to deposit using precise and conformal ALD method [117,118]. In addition, long-term stability of the passivation method should be considered. Finally yet importantly, dielectric passivation provides excellent protection from oxidation and environmental corrosion during long time. This renders it applicable also to photo-electrochemistry applications.

Effective dielectric surface passivation schemes in nanoscale III-V devices can be built-up from the historical work on the development of the next generation nanoscale III-V MOS technology [119]. The so-called gate-all-around (GAA) metal-oxide-semiconductor field effect transistors (MOSFET) utilize semiconductor NWs with radial dielectric-gate configuration, where the state of the semiconductor/oxide interface is critical for the functional characteristics of the device [120]. Interface traps located in the band gap of semiconductor play a detrimental role on the carrier transport, modifying the charge carrier density and field-effect mobility. In addition to the density of interface traps, D_{it}, the energy position of traps inside the band gap, E_t also plays an important role in the modification of the device characteristics. The main mechanism for surface recombination corresponds to the recombination at the deep traps, located at the mid-gap energy E_i. The deep traps capture the mobile charges (carriers) and thus modify the transport properties, which leads to the potential and current drop.

Overall, dielectric capping in GAA MOSFET is well established for Si [121] and relatively well-studied for III-V [119,122] nanostructures. This structure can therefore be considered as a good candidate for the passivation of NW device structures. Dhaka *et al.* recently characterized III-V NWs passivated by different dielectric materials, deposited by ALD, with the help of photoluminescence (PL) and time-resolved PL (TRPL) techniques [123]. Analysis of the aging effect revealed the retaining of good optical properties after 6 months storage in the environment. Black *et al.* showed the great improvement of PL intensity by a factor of $\sim$20 in InP NWs applying PO_x/Al_2O_3 passivation scheme [124]. One should note that optical methods characterize indirectly the surface passivation in the form of a radiation recombination measurement. A

technique that would extract D_{it} and E_t values is needed to clarify the trap-assisted recombination mechanisms at the semiconductor/oxide interface. LaPierre theoretically predicted an upper limit of 10^{12} cm^{-2} in surface defect density to achieve high efficiency in a GaAs NW PV device [45]. He claims that in such a case the overall performance is indistinguishable from the perfectly passivated NW device. This substantiates further the need to characterize surface and interface defect density as well as their energetic position within the bandgap. The direct characterization of the dielectric passivation on HAR semiconductor structures is the main topic of this chapter.

We have started by establishing this method on Si HAR microstructures. The testing of new characterization methods on Si microstructures is a necessary first step since the dielectric passivation of HAR Si micro/nanostructures has been widely studied over last years and thus it provides the necessary benchmarking for future studies in III-V HAR nanostructures [125–127]. Here, we propose an ultra-thin ALD Al_2O_3 passivation of Si micropillars (MPs) and introduce Electrochemical Impedance Spectroscopy (EIS) to characterize interface trap densities. **Figure 4-1** shows an illustrative comparison of EIS (left) and solid-state capacitance - voltage (C-V) (right) characterization on Si MPs. A solid-state C-V measurement, well established for quantifying the oxide/semiconductor interface trap density energy distribution in MOS devices, requires conformal coverage of the gate metal over the sample in order to define the device area. This is challenging for topologically complex HAR pillar samples. The fabrication process leaves the pillar sidewalls with ripples due to the nature of the reactive ion etching (RIE) process. As a result, poor-quality deposition of overlying dielectric and metal layers required for solid-state electrical characterization of the interface leads to current leakage and discontinuity of the top electrode layer. On the contrary, when a saturated aqueous solution of KCl is used as a conductive electrolyte in EIS method, a conformal liquid electrode automatically replaces the metal gate in a typical MOS capacitor. The EIS method suppresses charge transfer current through the solid-liquid interface. Due to the absence of a dissolved redox couple, the electrolyte blocks electronic carrier transport. Therefore, this characterization method is beneficial for HAR structures due to conformal electrical contact at the electrolyte-semiconductor interface. EIS measures both the real and imaginary components of impedance with the bias sweep; therefore, we can obtain C-V characteristic using the equivalent circuit of the device.

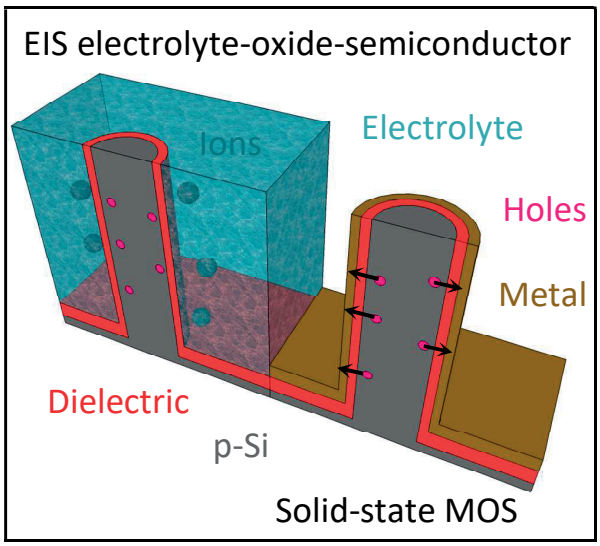

Figure 4-1 EIS and standard solid-state MOS characterization methods shown on HAR structures.

By applying this EIS method [95] and analyzing the data using a full interface state model [96], we obtained D_{it} distribution over the band-gap of Si for different passivation schemes in RIE etched Si MPs. More importantly, we verified the results from EIS with the standard characterization method - Quasi steady state photoconductance measurements (QSSPC). For the first time for Si HAR structures, we experimentally demonstrated the evidence of the same trends in D_{it} and effective lifetime, τ_{eff}, for different passivation methods.

4.1 Paper included in this chapter

This work was published in Advanced Materials Interfaces, 1800865 (2018).

doi.org/10.1002/admi.201800865

This chapter presents the post-print version of the manuscript. The independent bibliographic references for the manuscript are attached in the end of the corresponding section. The aforementioned bibliographic references differ from the general bibliography of this thesis by means of a different format. For instance, [1] refers to the first reference in the manuscript, while [1] refers to the first reference in the general bibliography presented at the end of this thesis. Supplementary information of the publication is located in Appendix at the end of the Thesis.

TITLE

Surface Defect Passivation of Silicon Micro Pillars

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MY CONTRIBUTION

- I simulated band alignment in studied structures using Nextnano
- I performed surface passivation of Si MPs including chemical treatment and ALD
- I performed EIS measurements on Si MPs with different passivation schemes
- I took active part in interpreting and analyzing the results
- I wrote part of the paper

Surface Defect Passivation of Silicon Micropillars

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Keywords: Silicon, passivation, micropillars, electrochemical impedance spectroscopy

Reactive-ion etching (RIE) used to fabricate high-aspect-ratio (HAR) nano/micro structures is known to damage semiconductor surfaces which enhances surface recombination and limits the conversion efficiency of nanostructured solar cells. Here, we report on defect passivation of ultra-thin Al_2O_3–coated Si micropillars (MPs) using different surface pre-treatment steps. Effects on interface state density are quantified by means of electrochemical impedance spectroscopy which is used to extract quantitative capacitance-voltage and conductance-voltage characteristics from HAR dielectric-semiconductor structures which would otherwise suffer from high gate leakage currents if tested using solid-state metal-insulator-semiconductor structures. High temperature thermal oxidation to form a sacrificial oxide on RIE-fabricated Si MPs, followed by atomic layer deposition of 4 nm thick Al_2O_3 after removal of the sacrificial layer produces an interface trap density (D_{it}) as low as 1.5×10^{11} cm^{-2} eV^{-1} at the mid-gap energy of silicon. However, a greatly reduced mid-gap D_{it} (2×10^{11} cm^{-2} eV^{-1}) is possible even with a simple air annealing procedure having a maximum temperature of 400°C.

Introduction

In recent years, nano- and micro-scale structure formation on semiconductor surfaces has become an extremely promising option for next-generation solar cells.[1, 2] For example, nanotexturization decreases the surface reflectance of solar cells and enhances absorption of light.[3] Furthermore, the shortened carrier collection paths for electrons significantly reduces bulk recombination losses in nanostructure based p-n junctions.[4] Previously, we showed 9.7 % efficiency for radial junction Si micro pillar (MP) arrays, with an optimized p-n junction configuration.[5] However, to date, nano/microstructured Si solar cells exhibit lower conversion efficiency compared to conventional cells due to enhanced surface recombination originating from their high surface-to-volume ratio.[6]

Many previous studies focus on surface passivation effects on Si-based nano/microwire solar cells by applying different surface treatment processes and capping layers.[7-10] In addition to the detailed passivation mechanisms for these surface treatments, methods to characterize the detailed nature of passivation effects in high-aspect-ratio (HAR) structures have been examined intensively. Due to the

particular challenges for direct application of standard techniques for surface defect characterization to nanostructured surfaces, estimation of critical parameters such as the surface recombination velocity, minority carrier lifetime and interface trap density from planar samples has been employed widely in such research.[9, 11, 12] In this study, we use a novel electrochemical impedance method that allows direct characterization of interface trap density in high-aspect-ratio structures; the advantage of this approach is that the nanostructure interface, which can differ significantly in morphology from that of planar structures, can be experimentally measured instead of estimated using a planar sample as a proxy.

Aluminum oxide, Al_2O_3, deposited by atomic layer deposition (ALD) has been demonstrated to inhibit minority carrier recombination on lightly doped n- and p-type as well as highly doped p^+-type silicon surfaces.[13-16] In practice, it is virtually impossible to avoid the presence of a layer of SiO_2 interposed between silicon and ALD-grown metal oxides and, indeed, a thin SiO_2 layer acts as an effective template for initiation of film deposition by ALD.[17-20] "Chemical passivation" (e.g. reduction of the density of dangling bonds on or near the Si surface) can be achieved by growth of SiO_2.[21] In addition to chemical passivation by SiO_2, a strong field-effect passivation is found to play a vital role in the performance enhancement achieved by coating silicon solar cells with Al_2O_3, and is consistent with the presence of a large negative fixed charge density near Al_2O_3/SiO_2 interfaces.[9, 16, 22, 23] Industrial application of ALD-grown metal oxides in photovoltaics is is in principle limited due to the relatively low deposition rates.[24, 25] One should still note however, that the implementation of ultra-thin Al2O3 has resulted in excellent surface passivation and thus it can be used in production.[26, 27]

In order to achieve ideal surface passivation of nano/micro pillars, critical challenges such as the existence of pinholes and surface defects must be addressed. It is also difficult to observe directly the passivation effect in wire array devices. For example, solid-state capacitance – voltage (C-V) measurement, well-established for quantifying the oxide/semiconductor interface trap density energy distribution, requires conformal coverage of a highly-conductive gate metal over the sample in order to define the device area.[28, 29] This is challenging for topologically complex HAR pillar samples. Contactless C-V measurements, such as COCOS,[30] are widely used for planar Si samples, but as mentioned recently by T. Pasanen *et al*,[31] interface trap density determination for HAR surfaces (such as black Si) has not yet been demonstrated unambiguously.

Here, we report on ultra-thin atomic layer deposited Al_2O_3 passivation of Si micro pillars (Si MPs) using electrochemical impedance spectroscopy (EIS) to characterize interface trap densities. The application of ultra-thin Al_2O_3 in solar cells requires careful chemical passivation in order to obtain low surface recombination velocities. We evaluate quantitatively the reduction in interface trap density associated with improved chemical passivation. Recently, Meng *et al.* have demonstrated the application of EIS for defect characterization in oxide-semiconductor nanostructures such as Si nano-pyramids obtained by KOH etching of bulk silicon wafers.[32] We find that low interface trap density (D_{it}), indicative of effective chemical passivation, of silicon micropillars (MPs) prepared by reactive Ion Etching (RIE) can be achieved with a simple process combining pre-ALD wet-etching and annealing with a maximum process temperature of 400°C. Such low temperature passivation processes can be beneficial from the viewpoint of reducing thermal budgets in Si solar cell fabrication.

It is well known that the effective lifetime of minority carriers (τ_{eff}), which is often used to assess the quality of interface defect passivation, is determined by D_{it} and fixed charge density (Q_{ss}) values.[33, 34] However, to the best of our knowledge, there is no experimental demonstration of this relationship in nano/microstructured silicon due to the great difficulty of performing D_{it} and Q_{ss} measurements with solid state contacts to HAR devices. This work provides evidence of the trends in D_{it} and τ_{eff} and the specific

contribution of interface trap reduction to chemical passivation for different surface treatments of HAR Si micropillars.

Results and Discussion

The p-type Si MPs were formed on a 500 µm thick Czochralski (CZ) grown Si (100) wafer by photolithographic patterning and deep RIE. The diameter, spacing, and length of the Si MPs were 5 µm, 10 µm, and 36 µm, respectively. **Figure 1a** shows a scanning electron microscopy (SEM) image of a Si MP sample used in this research. We performed all experiments on boron doped p-Si MPs. However, the obtained results should also be relevant to radial/axial p-n junction Si MPs.

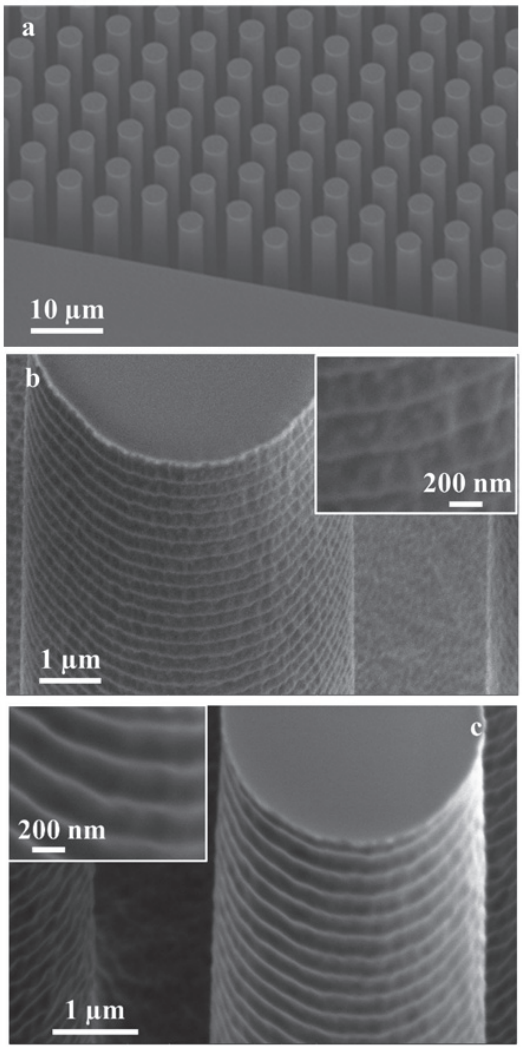

Figure 1. SEM images of the Si MPs array (a) and the single Si MP sidewall surface after RIE process (b) and after sacrificial oxide removal (c). SEM tilting angle is 30°.

It is well known that the RIE Bosch process forms highly-defective etched silicon surfaces. The RIE process leaves the pillar sidewalls with ripples due to the nature of the process sequence which cycles between etch and passivation phases.[35, 36] Figure 1b shows the 30° tilted SEM image of single Si MP

sidewall, where distinctive ripples can be observed. One way to reduce the surface roughness on the sidewalls is formation of a sacrificial oxide layer. Figure 1c shows the MP surface after oxide stripping.

To reduce the density of surface defects, we treated the silicon MPs using several different schemes. The control scheme did not include any surface pre-treatment steps. Scheme A included a surface pre-treatment as follows: 2 min BHF etching of the post-RIE native oxide-coated MPs followed by annealing in air on a hot plate at 400 °C for 30 min. Passivation scheme B had an additional thermal wet (water vapor) oxidation step for the formation of a sacrificial oxide layer in a tube furnace at 900°C for 90 min before the surface pre-treatment, which corresponds to a nominal SiO_2 thickness of 200 nm, as calibrated by oxidation of planar Si (100) wafers. Due to the much higher oxidation rate of the (110) orientation, the thermal wet oxide thickness formed on Si MPs was ~ 500 nm.[37] The final step was identical for all 3 schemes and consisted of deposition of approximately 4 nm of Al_2O_3 at 270 °C using 60 cycles of alternating trimethylaluminium (TMA) and H_2O precursor pulses. The pressure during ALD was approximately 0.68 Torr, as maintained by dry N_2 flow, which is also used to purge the gas lines and chamber between ALD cycles. All passivation procedures are shown in **Figure 2**. After the ALD process, a back-contact to the silicon wafer was formed using an In-Ga eutectic. The active device area for EIS analysis was defined using standard 2-component epoxy (Hysol 9460) and was in the range of $1\text{-}2\times10^{-3}$ cm^2 as measured in an optical microscope.

Interface state density, D_{it}, values were extracted from the measured C-V and conductance-voltage (g-V) data using the full interface state model.[29] This method obtains a continuous distribution of interface traps as a function of their energy. To perform the calculation, the conventional single-energy Y equivalent circuit of a trap capacitance and two conductances (connecting to the conduction and valence bands) must be converted to a Δ equivalent circuit to facilitate integration of circuit elements over all trap energies.

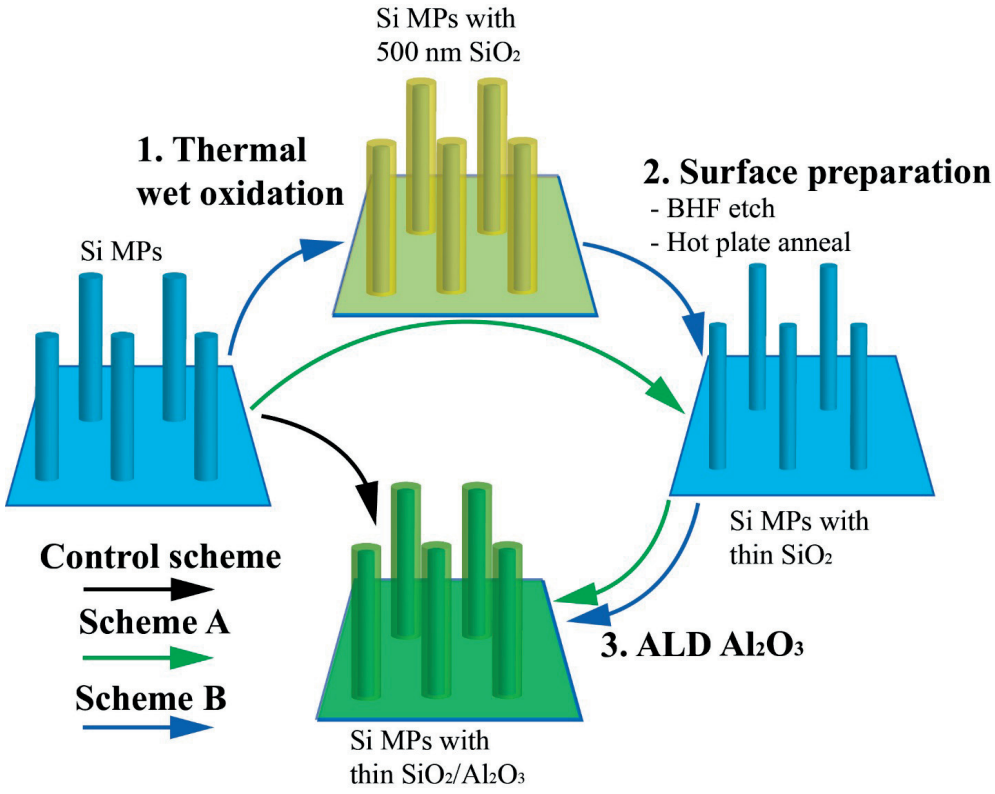

Figure 2. All passivation procedures for p-Si MPs: 1) formation of sacrificial thermal SiO_2 at 900°C for 90 min; 2) BHF etch + hot plate anneal at 400°C for 30 min; 3) 60 cycles ALD Al_2O_3.

First, we performed band alignment and carrier density versus applied bias simulations for the MOS structures. The simulations for the solid-state case can then be compared to the data from the EIS experiments. With a high ionic strength blocking electrolyte contact, the semiconductor undergoes inversion, depletion, and accumulation as its potential is increased versus that of the reference electrode, similar to the solid-state case when substrate bias is increased, due to the very low Debye length of the electrolyte, the large double layer capacitance, and the solution's high conductivity.[32] **Figure 3a-c** shows the band alignment of an Al/Al_2O_3/SiO_2/p-Si MOS structure in accumulation, flat band and inversion regimes, respectively. The charge carrier densities, and therefore the capacitance, can be calculated as a function of gate voltage as it is swept from accumulation, where the surface charge density on the semiconductor is dominated by holes, to inversion, where it is dominated by electrons. The C-V curve of an ideal MOS structure has been calculated by taking the derivative of the total sheet charge density with respect to the bias voltage:

$$C = \frac{dQ}{dV}, \quad (1)$$

where C is the differential capacitance per unit area, Q is the sheet charge density per cm^2 and V is the applied bias. The simulated quasi-static C-V curve of the ideal p-type MOS capacitor structure is shown in Figure 3d. The inversion region (at positive gate bias) shows the predicted rise in capacitance under quasi-static conditions due to the formation of a thin inversion layer at the interface.

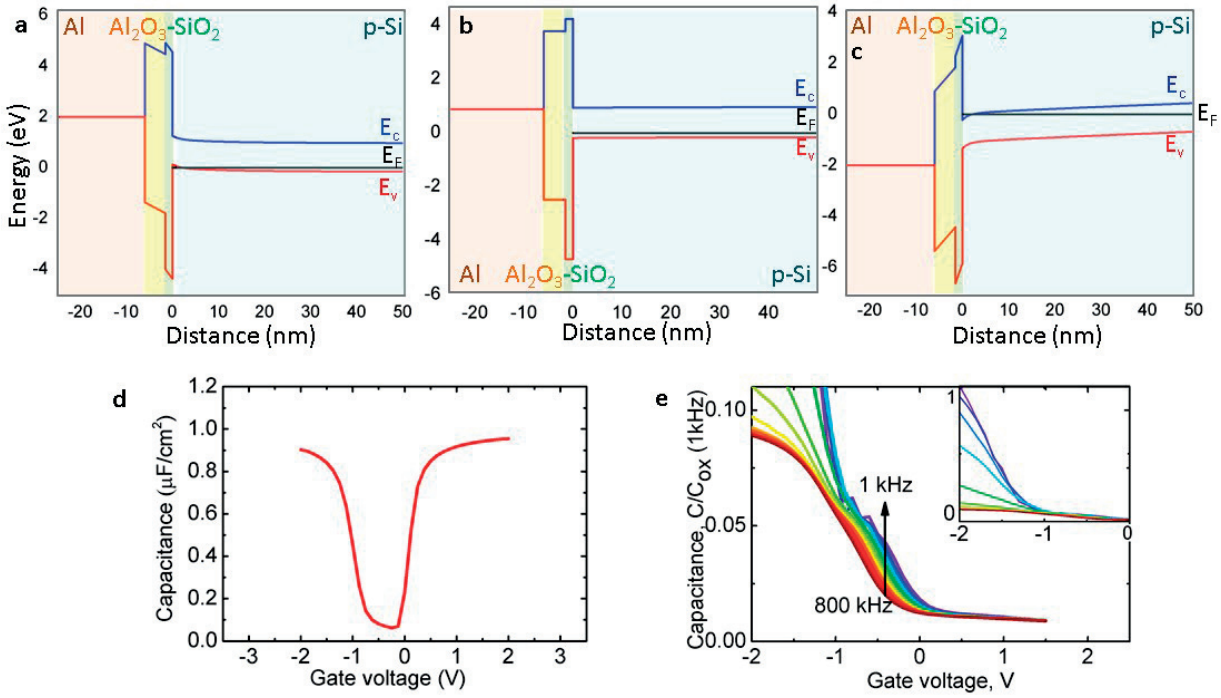

Figure 3. Band alignment of MOS structure Al/Al_2O_3/SiO_2/p-Si in accumulation (a), flat band (b) and inversion (c) modes; (d) The simulated quasi-static C-V curve of the MOS structure; (e) Multi-frequency solid-state C-V data from the Al/Al_2O_3/p-Si MP sample. Inset represents the full capacitance range C-V characteristics.

In order to provide solid-state C-V characterization as a reference, a control MOS structure with Al gate was prepared for MPs which underwent the control passivation scheme. Figure 3e illustrates the C-V characteristics of the MOS structure in the 1 kHz – 800 kHz frequency range normalized to oxide

capacitance (C_{ox}) at 1 kHz. The abnormally large capacitance dispersion in accumulation indicates high leakage current through the oxide. As explained below, this phenomenon can be attributed to a very rough Si surface as a result of the RIE process.

To improve surface passivation of the Si MPs, we applied surface treatment Scheme A, which includes wet etching of the native oxide and formation of a new oxide layer by baking the sample in air on a hot plate. It should be noted that below 600 °C, native oxide growth is approximately self-limited for growth times less than three hours;[38] although, at elevated temperatures (400 °C in our case) the growth rate of native oxide occurs much faster than at room temperature. About 1 nm of native oxide was formed after hot plate baking according to ellipsometry. Chowdhury and co-workers recently investigated native silicon oxide and silicon nitride (SiN_x), deposited by plasma enhanced chemical vapor deposition, for surface defect passivation of c-Si.[39] Approximately 1 nm growth of native oxide was reported to result in a very low dangling bond defect density of $2x10^{10}$ cm^{-2} as calculated from excess carrier density dependent lifetime measurements using the dangling bond interface recombination model.[40] We took a similar approach for our passivation schemes. Scheme B included an additional step of wet oxidation to form a thick sacrificial oxide layer. Oxidation at high temperature is known to form oxide by consuming silicon from the substrate. The application of this step before etching and Al_2O_3 ALD can lead to improvements in the surface of Si MPs by reducing the sidewall roughness of MPs damaged by RIE, as shown on Figure 1b and 1c.

Figure 4 shows C-V characteristics of each passivation scheme in the 1 kHz – 100 kHz frequency range extracted from EIS data. To simplify direct comparison of different passivation schemes, the capacitance was normalized to C_{ox} at 1 kHz, similar to the method of reference [41]. Area-normalized C-V characteristics are shown on Figure S1 in SI. The capacitance is plotted versus substrate potential, which is opposite to the gate voltage in solid state C-V measurements and simulations. The C-V plots show that, starting from inversion (at more negative substrate potentials), the capacitance is at a minimum value and begins to increase as the potential is increased towards depletion. Near depletion, we see a feature in the capacitance in all the measurements at ~ -1 V substrate potential and low frequencies. This feature is attributed to the capacitance associated with charging/discharging of interface traps as will be explained later.[28] Then, as the substrate potential is further increased to more positive substrate potentials, the capacitance reaches its maximum in accumulation.

As clearly seen from the C-V data, the curves have a significant frequency dispersion in accumulation. In solid-state data (see Figure 3e), this phenomenon is related to leakage current through the oxide layer due to pinholes caused by the scalloped surface of the etched MPs (Figure 1b).[35,36] The EIS method suppresses charge transfer current through the solid-liquid interface. Due to the absence of a dissolved redox couple, the electrolyte acts as a blocking layer for electronic carrier transport.[42] The dispersion in accumulation in the EIS method likely comes from the dependence of the double-layer capacitance on measurement frequency.[43] For HAR samples, this effect can be significant due to the large surface area. In accumulation, the effect of the double-layer capacitance being in series with the semiconductor-oxide system is maximized due to comparable values of these capacitances (see Figure S2 in SI). However, in depletion/inversion, the effect is small and the interface trap density can be estimated from measured C-V and g-V data.

To compare the simulations with the EIS data, one should align the voltage scales with the vacuum level. A negative shift of 0.54 V was applied to the simulated C-V curve due to the difference in the work function of Al and the electrochemical potential of the Ag/AgCl (sat. KCl) reference electrode (4.1 eV and 4.64 eV vs. vacuum, respectively).[44,45] The C-V curves are additionally shifted from the ideal C-V characteristic due to the presence of interface and bulk fixed charge. Quantum-mechanical simulations of

the ideal C-V curve provide an estimate of the fixed charge areal density, Q_{ss}. This value, -9×10^{12} cm^{-2}, is larger in magnitude than typically observed in C-V measurements of Si/SiO_2/Al_2O_3, where negative interface fixed charge at the semiconductor-oxide interface is often partially compensated by positive bulk fixed charge in the oxide.[46] Observation of net negative fixed charge in these experiments is consistent with the ALD-grown oxide being very thin.[32,46]

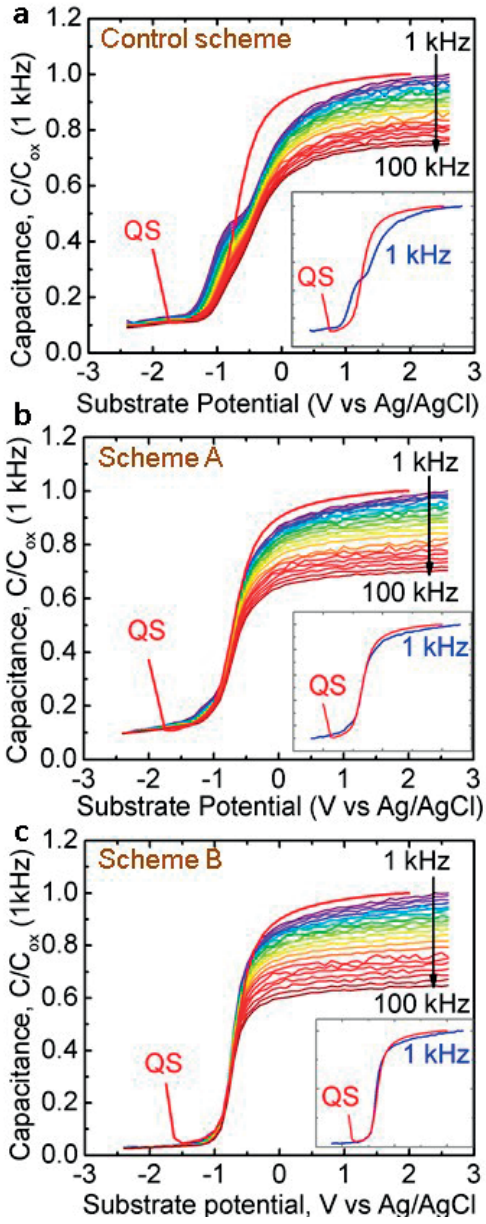

Figure 4. C-V curves extracted from EIS measurements of p-doped Si MPs with different passivation schemes: a) only 4 nm Al_2O_3 cap; b) scheme A with surface pre-treatment and 4 nm Al_2O_3 cap; c) scheme B with etching 500 nm of previously formed sacrificial thermal silicon oxide, surface pre-treatment and 4 nm Al_2O_3 cap. Insets: 1 kHz C-V curve of each passivation scheme vs. simulated quasi-static (QS) C-V curve (plus additional fixed charge).

We observe a frequency-dependent feature in the capacitance at ~ -1 V vs. Ag/AgCl, consistent with the presence of interface traps (see Figure 4a).[32] These traps can be charged/discharged by applying a small AC voltage at different frequencies, leading to changes in the capacitance of the electrolyte-oxide-semiconductor system. Surface pre-treatment can significantly decrease D_{it} (Figure 4b) by improving the Si/SiO_2 interface though formation of a native oxide of better quality compared to the air-exposed etched MPs. With an additional step of growth and removal of a high-temperature sacrificial thermal oxide, the interface trap density can be further suppressed (see Figure 4c). Thermal oxidation of the Si pillars, followed by BHF wet etching and reforming of a high quality native oxide eliminates the majority of surface defects produced by the RIE process. The insets of Figure 4 show simulated QS and 1 kHz measured C-V data for each passivation scheme. An almost perfect match of the curves in the inset of Figure 4c confirms the improved passivation of oxide/silicon interface defects.

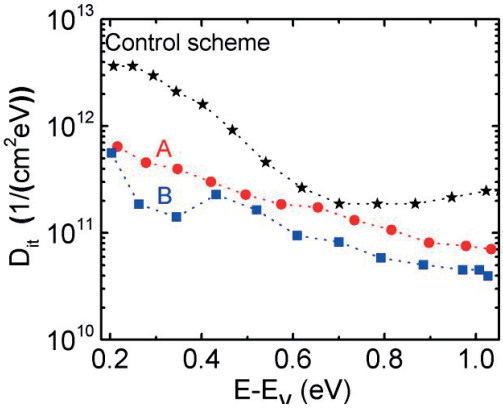

Figure 5. Extracted density of interface states (D_{it}) using the full interface method for three different passivation schemes: a) only 4 nm Al_2O_3 cap (black); b) surface pre-treatment and 4 nm Al_2O_3 cap (red); c) etching 500 nm of previously formed thermal silicon oxide, surface pre-treatment and 4 nm Al_2O_3 cap (blue).

The interface state density can be estimated using the full interface state method.[29] The calculated distribution of interface states in the bandgap is plotted for all three passivation schemes of the p-Si pillars (**Figure 5**). The interface trap density at the mid-gap energy is lowered from 4.2×10^{11} to 2×10^{11} cm^{-2} eV^{-1} as a result of surface pre-treatment and Al_2O_3 passivation and is further lowered to 1.5×10^{11} cm^{-2} eV^{-1} as a result of removal of the outermost 500 nm of the Si MPs by forming and etching the sacrificial thermal oxide prior to the surface pre-treatment and Al_2O_3 passivation. It is well known that the main mechanism for recombination at semiconductor surfaces is electron-hole recombination at deep traps,[47,48] those producing energy levels located in the band gap far ($\gg kT$) from the conduction and valence band edges. The interface state energy profiles in Figure 5 indicate that the passivation effects observed in these experiments are greater than that implied by the mid-gap D_{it} reduction from 4.2×10^{11} to 1.5×10^{11} cm^{-2} eV^{-1}. The reduction in D_{it} is even larger across most of the energy range from 0.3 to 0.8 eV above the valence band edge.

Furthermore, we performed Quasi-steady-state photoconductance measurements (QSSPC) on Si MPs samples with different passivation schemes (see Figure S3 in SI). The effective lifetime of minority carriers, τ_{eff}, are extracted from these measurements and compared with D_{it} values. A number of papers reported much lower τ_{eff} for HAR structures compared to planar samples with the same passivation method (µs vs ms).[11,49] This results from the fact that in high quality bulk material, surface effects, enhanced in high

surface-to-volume structures, dominates the minority carrier transport and, therefore, determines τ_{eff}. Moreover, passivation quality can be poor due to the deep and narrow geometry of HAR structures, which complicates uniform deposition of passivation layers. It is notable that the reduction of minority carrier concentration by the fixed charges of Al_2O_3 is the same for all passivation schemes and, as reported by Terlinden *et al*,[22] in the case of thin oxide layers (only 4 nm in our case) chemical passivation plays a major role. Passivation scheme B resulted in a τ_{eff} of 4 µs, while the absence of a photoconductance signal was observed from the control sample. Finally, τ_{eff} below the detectable level (1 µs) was found for scheme A. Therefore, scheme B provides the best overall passivation, consistent with the D_{it} trend observed by EIS analysis of the interface trap density. It is worth noting that, in the case of radial p-n junction configuration, the diffusion length of minority carriers should be comparable to or larger than the radius of MPs for efficient carrier collection. This condition is achieved with the proposed passivation scheme.

Using passivation scheme B, we achieve a capacitance-voltage behavior consistent with a density of interface traps less than 2×10^{11} cm^{-2} eV^{-1} across almost the entire silicon band gap. Moreover, even simple surface preparation by wet etching and low-temperature oxidation results in a substantial improvement in the chemical defect passivation of Al_2O_3-coated Si MPs. This result is significant as it shows the potential for achieving relatively electrically passive Si MPs surfaces with an inexpensive, low-thermal-budget process.

Conclusions

We studied surface passivation of RIE-formed Si MPs by different process schemes including thermal oxidation and ALD Al_2O_3. The C-V properties were characterized using the EIS method, allowing us to carry-out measurements on high-leakage (scalloped surface) HAR structures. A passivation scheme with a high temperature wet oxidation step for the formation of a sacrificial oxide layer produces the lowest interface trap density of 1.5×10^{11} cm^{-2} eV^{-1} at the mid-gap energy of silicon, resulting in an effective minority carrier lifetime of 4 µs in the silicon MPs. In addition, we found that a simple procedure including air annealing at 400° C prior to ALD Al_2O_3 deposition reduces interface trap density across the silicon band gap to almost as low a value as the sacrificial oxide process. With further optimization, this inexpensive and low-thermal-budget passivation scheme may be useful for fabrication of efficient silicon MP solar cells and photodetectors.

Experimental Section

Electrochemical Impedance Spectroscopy: Electrochemical impedance spectroscopy was performed on different samples to obtain the real and imaginary parts of the impedance from a BioLogic VSP potentiostat. A saturated aqueous solution of KCl is used as a conductive electrolyte, which replaces the metal gate used in a typical metal-oxide-semiconductor capacitor. Three electrode scheme consists of Ag/AgCl/saturated KCl (*aq*) as the reference electrode and a Pt wire counter electrode. EIS was recorded from 1 kHz to 100 kHz at (-2.5; 2.5 V vs. Ag/AgCl) substrate voltage range with an ac oscillation amplitude of 10 mV. To reduce instability during the measurements, waiting time of one full period of the applied ac perturbation before each new frequency and three measurements at each frequency were made. A simple equivalent circuit with parallel capacitance and resistance was used to calculate capacitance versus the applied bias on the sample.[32]

Simulations of the band alignments: Simulations of the band alignments of the structures and of the ideal C-V behavior of a p-type MOS capacitor were performed using the Next Nano software package.[50] We provide numerical simulations of the structure with Al gate as a visualization of the band alignment at the $Si/SiO_2/Al_2O_3$ interface with applied bias. Due to the much larger diameter of MPs compared to the

depletion width in p-Si (300 nm for 10^{16} cm^{-3} doping), simple 1D simulations correctly capture the physics. To simulate the band-bending at the semiconductor–oxide interface exactly, the 1D Schrödinger-Poisson equation was solved self-consistently. The following parameters were used: SiO_2 thickness of 1 nm, Al_2O_3 thickness of 4 nm and doping concentration of p-type Si of $3x10^{16}$ cm^{-3}. A silicon dioxide layer is introduced in the simulations due to oxide formation between the Si surface and the deposited Al_2O_3 dielectric layer either during or prior to the ALD process. The band gaps of amorphous Al_2O_3 and SiO_2 are taken as 6.1 eV and 8.9 eV, respectively.[51] The reported Schottky barrier at the Al/Al_2O_3 interface is 2.9 eV.[52]

MOS device fabrication: MOS structures for reference solid-state C-V measurements were fabricated on the silicon MPs using the control passivation scheme and a nominally 30 nm thick Al gate metal layer was e-beam evaporated through a shadow mask. Circular gates of diameter 250 µm were formed.

Quasi-Steady-State Photo Conductance measurements: QSSPC characterization was performed by means of a WCT-120TS photoconductance setup from Sinton Instruments. It consists of an inductive coil that converts the current produced by the excited carriers into a voltage signal which is coupled to the conductivity of the wafer.[53] The photoconductivity decay with the flash lamp intensity decay is measured. The minimum detectable lifetime is 1 µs.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the Swiss National Science Foundation, mobility fellowship under Grant P1ELP2-172279 and 200021-172547, by Nanotera under grant Synergy and by the U.S. National Science Foundation award DMR-1608927. We would like to thank Dr. Jelena Vukajlovic-Plestina for her support with Si MPs fabrication. P.R-G. acknowledges funding from H2020 through the Marie Curie Action 702629, R2R-3G, MSCA-IF-EF-ST.

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Conflict of Interest

The authors declare no conflict of interest.

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Chapter 5 Conclusions and Outlook

The purpose of this thesis was to provide novel insights in possible origins of underperformance of NW-based solar cells. For this, we have addressed several issues such as surface recombination, inhomogeneity in the electrical properties of the NWs and electrical losses linked to the fabrication methods and materials used as electrodes.

The first chapter of this thesis describes the main physical reasons that has motivated our and other groups to propose NW-based solar cells as candidates for next generation PV devices. From the optical point of view, the filamentary geometry leads to the boosting of the light absorption due to self-concentrating effect for optimal NW diameters. In addition, the reduced size of their diameter favors mostly defect-free hetero-epitaxy on lattice -mismatched substrates, such as III-V on Si. Due to the low contact area, the stress between grown material and the substrate is relaxed in a very effective manner. Misfit dislocations are located solely at the interface with the substrate, with minimal impact on the device properties [130]. Finally, from the functional point of view, these structures can include radial or axial p-n junctions, which renders the design of these devices extremely flexible. Compared to bulk devices, a carrier diffusion length of only several micrometers is enough for efficient carrier collection. The limiting mechanisms in the solar cell may also rely on the NW geometry. These are high surface recombination rates due to the large surface-to-volume ratio, poor conductance of the front electrical contacts originated from the limited contact area with the NW tips, and the existence of possible hetero-barriers at the interfaces blocking the collection of charge carriers. So far and to the best of our knowledge, current technology of NW-based solar cells has not overcome above-mentioned drawbacks. The best-reported efficiencies of the NW-based solar cells are still below the optimized planar devices.

In Chapter 2, we describe in details the fabrication process of GaAs NW-based solar cells and how each step in this process can introduce different types of deficiencies in the device. First, we discuss these issues in terms of an equivalent circuit model. In general, a solar cell can be modeled with a circuit formed by an array of diodes in parallel with added series and parallel resistances. If the device presents a heterointerface (for example the highly doped substrate that acts as electrode), an additional diode in series needs to be added. The different elements of the NW-based solar cell equivalent circuit and their physical meaning are discussed here. At the end, we present standard electrical methods to analyze NW-based solar cells, such as two-point device IV characterization and single NW IV characterization together with the diode fitting models. However, these methods are limited to the classic solar cell behavior, which is not the case in non-optimized NW-based devices. Therefore, additional characterization is needed to better describe the deficiencies in the device.

Experimentally, we measure and identify the series, parallel and surface recombination losses by using advanced characterization methods such as conductive atomic force microscopy (C-AFM). We study a device formed by self-assembled VLS-grown GaAs NWs on silicon with a radial p-i-n junction. Due to the self-assembly process, the distance between the NWs as well as their physical and electrical characteristics can vary. We have characterized both the ensembles and individual NWs using current scanning modes and by measuring the IV characteristics individually. We have revealed that one important deficiency of the

device originates from the high proportion of non-photosensitive NWs. These acts as a leakage path for the carriers. We have compared these results with a regular NW pattern formed by a top-down process. In that case, all NWs were identical and this deficiency was absent. We have thus shown that the homogeneity of NW p-n junctions is extremely important for this kind of device. In addition, we have revealed that C-AFM scanning is an efficient and non-destructive method that helps to target leakage paths and uniformity issues in this kind of device.

Next, in chapter 3, losses linked to high series resistance in GaAs NW-based solar cells are characterized. For this, we use the light intensity dependent IV method. Following this method, as so-called resistance-free $Suns - V_{OC}$ characteristic can be plotted and analyzed by different diode models. This characteristic, plotted as $J_g - V_{OC}$ curve, represents the resistance-free dark IV curve of the p-n junction in the solar cell. It is then possible to obtain the resistance-free dark IV curve with a two-diode model and extract the main fitting parameters, describing the carrier transport mechanism in a p-n junction. In addition, the lumped series resistance of the studied solar cell can be calculated by comparing the $J_g - V_{OC}$ characteristic and the experimental IV curve at 1 sun. This allows us to separate the study of the p-n junction in the NWs and the whole device performance with the non-optimized interfaces and electrodes. Such an analysis, widely used in planar PV, was applied to the NW-based solar cells for the first time. From the perspective point of view, the ability to probe the interface effect on the device properties in NW-based devices can make this method a standard technique in non-optimized new type nanostructured solar cells. The future work will include the characterization of different material NW-based solar cells to reveal and separate the effect of the transparent conductive oxide contacts and hetero-barriers existing in the device.

Finally, in chapter 4, we address the issue of surface recombination in this kind of devices. In particular, we use a novel method to characterize it without damaging the device. The method is electrochemical impedance spectroscopy, EIS. As the surface passivation of III-V NWs has not yet been fully optimized, we applied this method to Si micropillars. We compared the passivation by ALD Al_2O_3 with native and wet oxides. The interface trap density was extracted from the capacitance-voltage and conductance-voltage experimental curves, obtained from the measured impedance of the studied structure. Complimentary measurements of the effective lifetime of minority carriers were in agreement with the data. The highest lifetime coincided with the passivation scheme with the lowest interface trap density.

To summarize, in this thesis we have identified several challenges in the use of NWs for high efficiency solar cells. We have also demonstrated that these can be addressed by specialized characterization techniques. In particular, we have used three characterization techniques: C-AFM, light intensity dependent IV, EIS. We believe this experimental work shows the way to correctly estimate electrical losses in nanostructured solar cells, which is needed to overcome the current efficiency limit of the state-of-the-art NW based solar cells.

5.1 Future Outlook

Even though the number of publications on nanowire-based solar cells has been and is on the rise, conversion efficiencies are still below 20% which is lower the planar counterparts. The optical properties (i.e. light absorption) and the NW fabrication methods (i.e. crystal quality) were optimized and reported intensively during last years. Still, power losses due to poor carrier collection have not yet been resolved in a full manner. This Thesis contributes to the understanding of important aspects leading to conversion losses in the NW-based solar cells. We believe, there is much to be done in a near future both in fundamental and practical aspects.

First of all, the perfect uniformity of the p-n junctions in this kind of devices is extremely important, as was shown by C-AFM analysis. Future work in this area should focus on the finding and optimization of the patterning techniques needed for large-area arrays of NWs. The commercial success of NW-based PV is impossible without cheap and large-scale fabrication process. The highest efficiencies of NW-based solar cells are shown for the area up to 1 mm^2, which is not enough to enter any commercial fabrication attempt. Besides that, an interesting and counter-intuitive solution to reduce parallel losses in NW array solar cells is based on introducing additional resistive buffer layer, which prevents electrical inhomogeneity, i.e. leakages, by enhanced local series resistance. This strategy was implemented in ZnO/CdS/CIGS solar cells, where intrinsic ZnO plays such a role [131].

The optimization of the carrier transport and collection in the NW p-n junction can help to close the gap between the practical NW-based solar cell technology and theoretical limits. In this direction, the heterointerfaces in NW-based solar cells are worth to be investigated in more detail. This includes the compatibility of different TCO layers with III-V semiconductors, where careful engineering of the band alignment is necessary. The proposed intensity dependent IV characterization will help to probe and expose the transport mechanism through the interface. Specifically for the III-V NWs on Si, the evaluation of the heterobarrier between substrate and NW could elucidate if this is one of the reasons for the underperformance compared to the NW devices fabricated on III-V substrates.

Surface passivation of NWs by dielectrics shows an alternative to the standard passivation with higher bandgap ternary alloys, such as AlGaAs on GaAs. With the EIS characterization, this passivation can be characterized and provide a path for improvement of the NW-based solar cells. Next step should be the application of the EIS technique to III-V nano/microstructures. One challenge for this arises from the need for the non-aqueous electrolyte to prevent accidental oxidation of the III-V surface through the pinholes in the oxide.

A few words should be said about the commercial future of NW-based PV devices. Even achieving the photoconversion efficiencies higher than planar III-V solar cells does not guarantee commercial success in the terrestrial use of NW-based solar cells. Si wafer based technology accounted for about 95% of the total production in 2017; the rest is based on all types of thin film technologies and the trend is not favoring to them [©Fraunhofer ISE: Photovoltaics Report, 19 June 2018]. Therefore, one should consider niche applications of NW-based solar cells where the advantages of these nanostructures can be used.

Two visible opportunities for commercialization are barely touched in this thesis. First one based on the idea of concentrating PV (CPV), where the area of the device can be rather small and the technology can be expensive. The self-concentrating optical effect of NWs can enhance the light concentrating by lenses, used in traditional CPV. In addition, due to the large surface-to-volume ratio, the detrimental heating effect in CPV devices at large light concentrations can be minimized. Dorodnyy *et al.* already reported the design concept for multi-junction NW-based solar cells, needed for CPV application [35]. The practical realization of the multi-junction NW-based solar cell will open the new perspective in this niche area.

Another interesting and promising idea is to develop flexible solar cells based on NWs. Transferring NWs from the rigid substrate to flexible polymer media was developed several years ago, and the devices based on this concept were reported. Flexible III-N NW-based optoelectronics devices have already shown impressive progress in efficiency and flexibility [132]. This success can give a new pulse to the development of the technology of flexible solar cells based on III-V NWs.

Appendix

In this appendix the Supplementary Information of the publications is reported.

1. Publication 1 - Conductive AFM as a characterization technique for nanowire solar cells
2. Publication 2 - Surface Defect Passivation of Silicon Micropillars

Electronic Supplementary information

Conductive AFM as a characterization technique for nanowire solar cells

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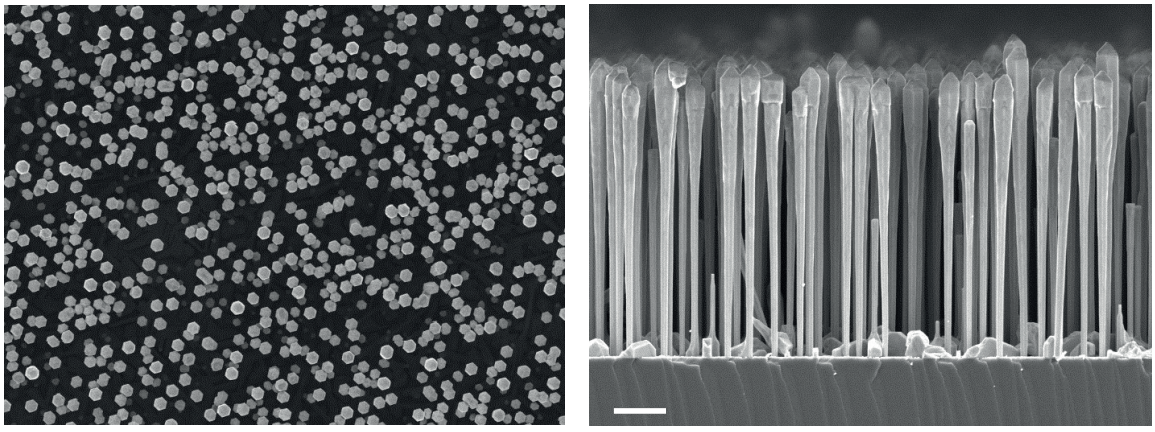
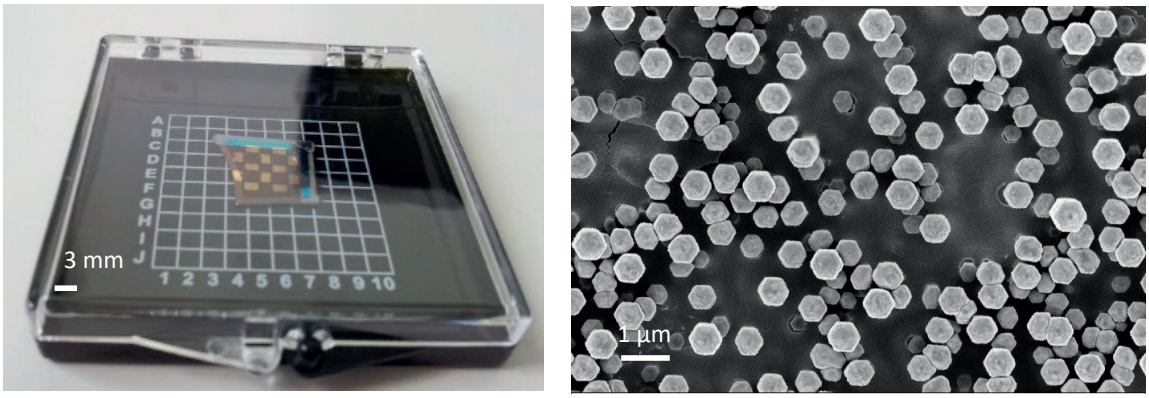
S1. SEM images of the as-grown sample



(a) (b)

Figure S1. Top (a) and cross-section (b) SEM view of the as-grown GaAs NW array sample

S2. Photography and SEM images of the full device



(a) (b)

Figure S2. The photography (a) and top SEM view (b) of the solar cell based on GaAs NW array

S3. Conductive-probe atomic force microscopy:

Measurement sequence and external light.

Cypher-S AFM.

C-AFM was performed using the ORCA module of a Cypher-S AFM. The voltage offset was corrected by measuring the tip-sample bias at 0 applied voltage with a multi-meter. To ensure the tip was conductive and not contaminated, prior the actual measurement we repeatedly scan the tip over a graphite sample. To align the laser spot on the back of the cantilever the procedure provided by the probe manufacturer was followed. The sample was thus engaged in contact mode and the surface scanned with a velocity of either 1Hz or 0.5Hz, depending on the scan size. According to the density of the wires, the scan size was adjusted but generally, the maximum one was of 10µm. Generally the set-point had to be kept relatively low (between 100 and 300 mV with a 0 ± 10 mV starting value of deflection) and the integral gain quite high (around 100) to compensate the high roughness. This is the reason why, occasionally, a feedback-induced ringing can appear in the images. Nevertheless, with these scanning parameters a reliable and consistent tracking of the surface was possible. As a light source for current measurements under the light, we use standard internal LED lamp at maximum power. The exact technical parameters of the LED can be found in the manual.

Bruker ICON AFM.

C-AFM was performed using the standard C-AFM module of a Bruker ICON AFM. The general procedure was similar to one used on a Cypher C-AFM. In addition, the external quartz tungsten halogen lamp was implemented in AFM setup through an in-built optical microscope. The power of the light source was calibrated with a standard reference silicon cell and light intensity spectrum, measured using the spectrometer CCS100. The total power at the sample was 3.55 mW.

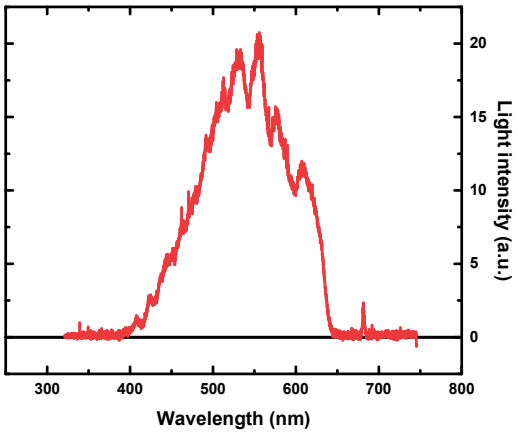
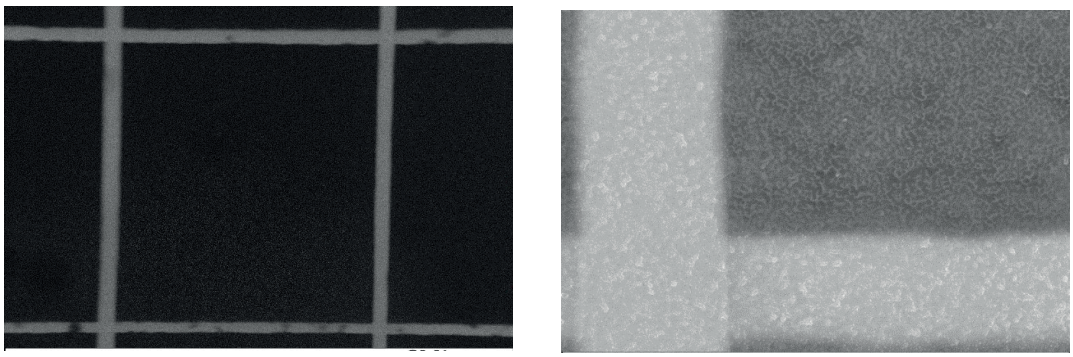


Figure S3-1. The spectrum of the introduced in AFM external light from quartz tungsten halogen lamp. The spectrum is measured at the sample position.

The Au grid implementation for orientation on the sample surface.

Additionally, we implemented Au grid on top of the sample surface. By this, we were able to find the same surface area by AFM and SEM. During C-AFM scan on metal surface, high current was detected via 1 V of applied bias. We chose the area near the square corner of Au grid.



(a) (b)

Figure S3-2. The GaAs NW array surface with Au grid for the orientation on the surface (a) and the square corner where the area was chosen for the measurements (b).

The comparison of NW response to different light sources.

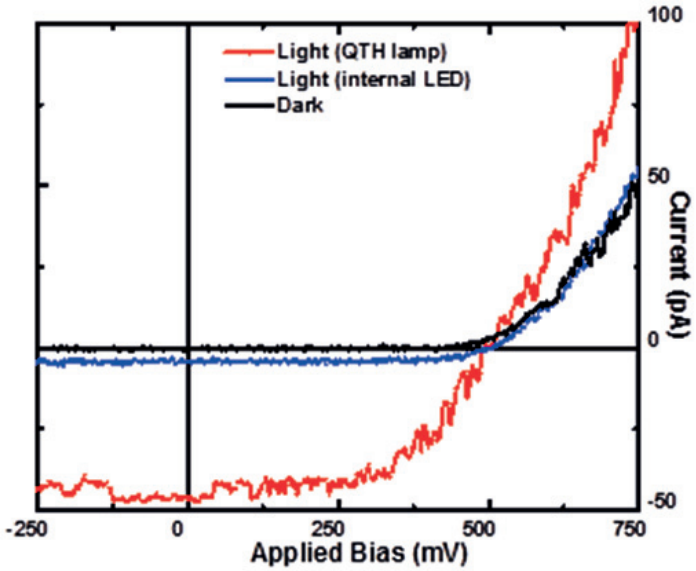


Figure S3-3. The black curve corresponds to a single NW IV in the dark, the blue and red curves correspond respectively to the response under LED and HGT lamp illumination. The V_{oc} does not vary under different illumination intensity.

S4. Standard single nanowire electrical measurements

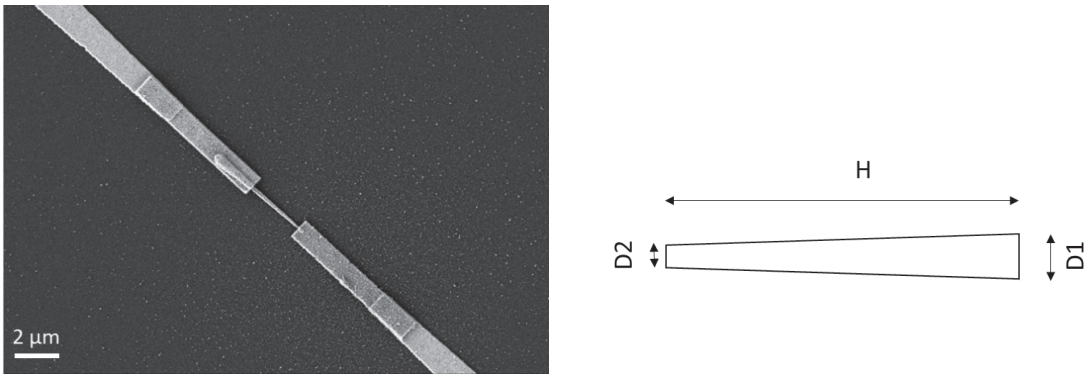


Figure S4. SEM image of the single horizontal GaAs NW solar cell

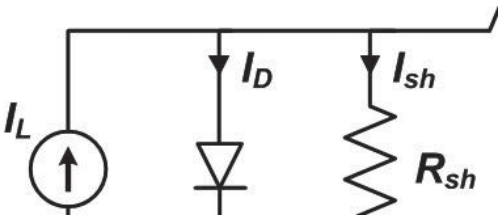
Calculation of the area:

To simplify area calculation, we assume that an isosceles trapezoid with the height L, and bases D1 and D2 represent the p-n junction area. Then, the active area of p-n junction is:

$$S = L * AVG(D1; D2) = 3.92 * 10^{-9}\ cm^2,$$

where length $L = 2.8\ \mu m$, diameter $D1 = 180\ nm$, diameter $D2 = 100\ nm$.

S5. 1-diode equivalent scheme and fitting of IV curves



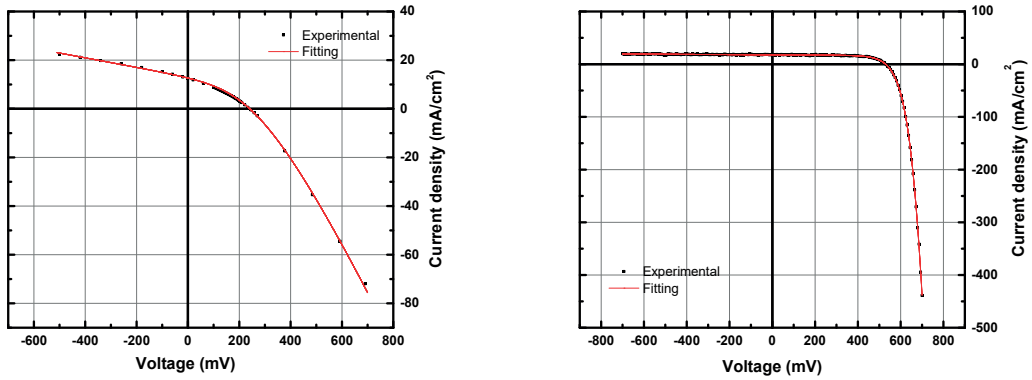
$$I = I_{ph} - I_s * \left(\frac{q*(V+IR_s)}{n*k*T}\right) - \frac{V+I*R_s}{R_{sh}}$$

Figure S5-1. 1-diode equivalent scheme for solar cell performance evaluation and the Shockley equation

The fitting of IV curves was performed using standard 1-diode equivalent scheme and software program "2/3-Diode Fit" by Stephan Suckow [R1]. The main fitting parameters are shown in Table S5. Instead of current in original formula, we use current density to be able to compare data from array of NWs and single NW. The C-AFM IV curve was fitted only to get ideality factor value. Due to not calibrated to 1 sun light in C-AFM, we do not provide additional data of fitting.

	J_{ph}, mA/cm²	J_s, mA/cm²	n	R_s, Ohm*cm²	R_{sh}, Ohm*cm²
Full device	*14.05*	*$2.3*10^{-4}$*	*2.56*	*4.2*	*46.9*
Single horizontal NW	*17.73*	*$1.6*10^{-7}$*	*1.79*	*0.04*	*447*

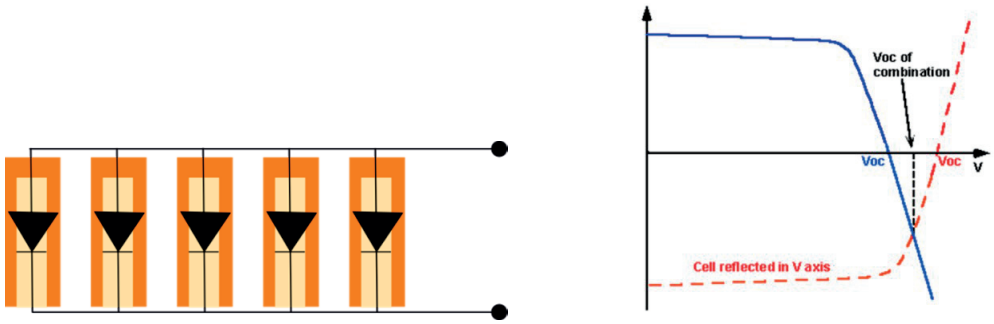
Table S5. Fitting parameters for the IV curves of the samples



(a) (b)

Figure S5-2. Measurements and fits (solid lines) of IV curves of GaAs NW based solar cell illuminated by global AM1.5 light (a – NW array device; b – single NW)

S6. Parallel connected diode scheme and total IV calculations



(a) (b)

Figure S6. Equivalent parallel connected diodes scheme and example of 2 parallel connected diode IV curves [R2].

To represent ensemble of vertical NWs as a solar cell, we can use equivalent parallel connected diode scheme, as shown on Fig S6a. The cores of NWs are all connected to the doped Si substrate and therefore to back contact. In opposite, ITO layer, representing top contact, covers the shells of NWs (the top parts). As shown on Fig. S6b, when we have two parallel connected cells, the V_{oc} of combination is located in the point where sum of the currents is equal 0. Extrapolating it to numerous number of NWs, we have the following condition:

$$\sum_{i=1}^{n} I_i(V = V_{oc}) = 0,$$

where n – number of NWs, I_i – current of i-NW at $V = V_{oc}$.

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[R2] PVEDUCATION.ORG

Electronic Supplementary Information
Surface Defect Passivation of Silicon Micropillars

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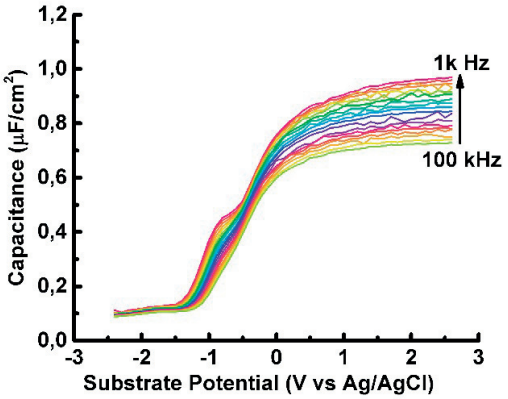
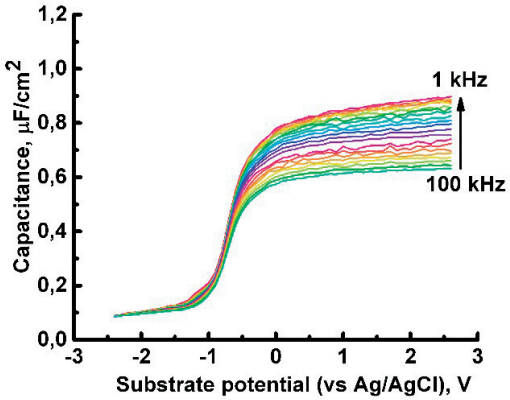
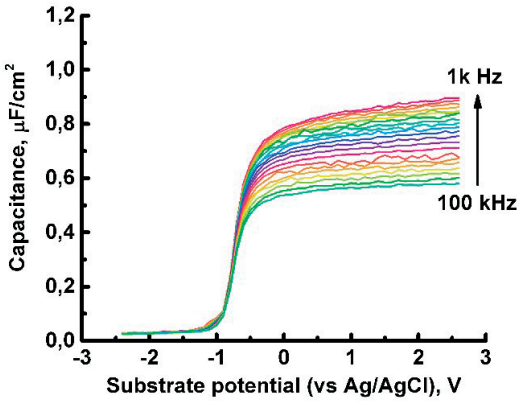
S1. C-V characteristics of Si MPs samples with different passivation schemes, normalized with the area



(a)



(b)



(c)

Fig. S1. Area normalized C-V curves extracted from EIS measurement for p-doped Si MPs with different passivation schemes: a) only 4 nm Al_2O_3 cap; b) surface pre-treatment and 4 nm Al_2O_3 cap; c) etching 500 nm of previously formed sacrificial thermal silicon oxide, surface pre-treatment and 4 nm Al_2O_3 cap.

All three samples were measured in SEM and optical microscope to find the total areas of these oxide-semiconductor structures. On **Fig. S1**, we provide area-normalized C-V characteristics for all passivation schemes. As shown here, the area-normalized oxide capacitance in accumulation is roughly the same for all cases, confirming the improvement in passivation from the reference scheme to schemes A and B without increases the equivalent oxide thickness (EOT).

S2. Double layer capacitance measurements using Pd electrode

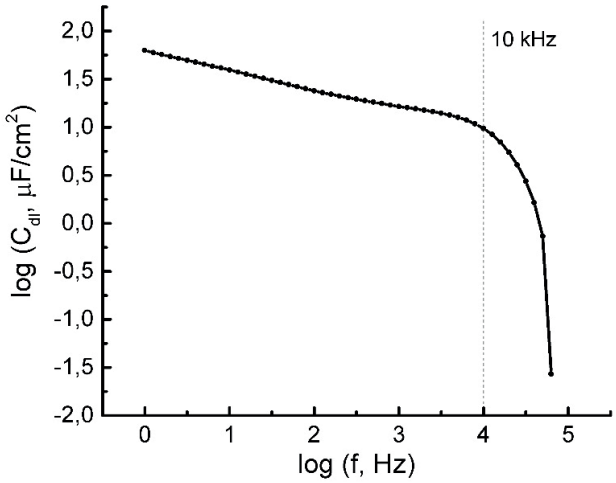


Fig. S2. Log-log graph of C-f data extracted from EIS measurement for Pd electrode.

In order to estimate the effect of double-layer capacitance on impedance measurements of oxide-semiconductor structure by EIS, we provide C-f data for a Pd electrode at 0 V. A metal electrode does not

exhibit capacitance; therefore, a capacitance measured by EIS represents the double-layer capacitance in sat. KCl electrolyte. As shown on **Fig. S2**, at ~ 10 kHz there is the onset of a significant drop of the capacitance from 10 µF/cm^2 down to 0.1 µF/cm^2. Because the double-layer capacitance is in series with the measured impedance, in accumulation there is a strong effect of the double-layer on the total impedance of the system. This phenomenon is consistent with observed large dispersion in accumulation for the EIS-tested samples studied in the paper.

S3. QSSPC measurements

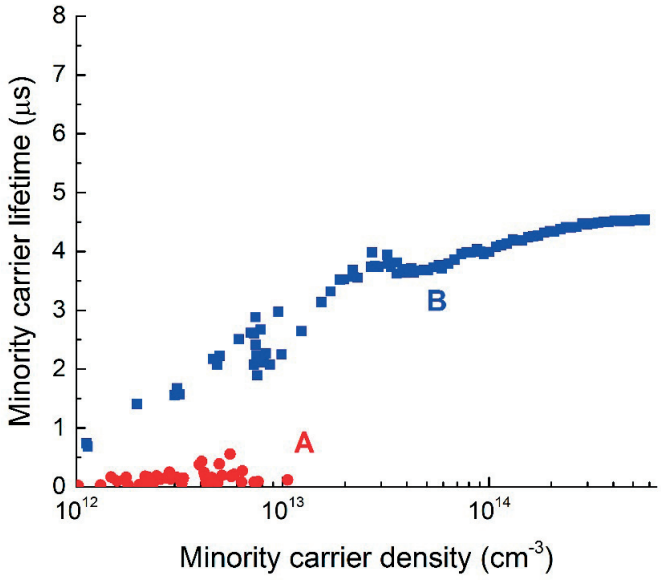


Fig. S3. Quasi steady state photoconductance measurement.

To quantitatively crosscheck the passivation effect, we also perform injection level dependent QSSPC lifetime measurements on the same samples. The mean effective lifetime determined by this method is $\tau_{eff} = 4\,\mu s$ at the typical injection level of $\Delta n = 10^{15} cm^{-3}$ for Scheme B (see **Fig. S3**). The τ_{eff} for Scheme A is impossible to determine due to the below minimum detectable level value. QSSPC measurements of Control scheme sample did not give any photoconductance response at all.

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[1] **Dmitry Mikulik**, Andrew C. Meng, Riad Berrazouane, Josua Stuckelberger, Pablo Romero-Gomez, Kechao Tang, Franz-Josef Haug, Anna Fontcuberta i Morral and Paul C. McIntyre, Surface Defect Passivation of Silicon Micropillars, *Advanced Materials Interfaces* (2018), 1800865.

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[3] Moonsang Lee, **Dmitry Mikulik** and Sungsoo Park, The investigation of *in situ* removal of Si substrates for freestanding GaN crystals by HVPE, *RSC Advances* **8** (2018), 12310-12314.

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[11] Yury Zhilyaev, **Dmitry Mikulik**, Alexander Nasonov, Tatiana Orlova, Valery Panteleev, Nikolay Poletaev, Leonid Fedorov, Mikhail Shcheglov, GaAs *p-i-n* structures for X-ray detectors grown on Ge and GaAs substrates, *Technical Physics Letters* **38** (2012), 399-401.

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Patents

[1] Wanit Manorotkul, Shin Joong-Han, Bongjin Kuh, Hanmei Choi, **Dmitry Mikulik**, US Patent US 9576969 B2, “Integrated circuit device including polycrystalline semiconductor film and method of manufacturing the same”, 2017.

Journal articles *under preparation*

[1] **Dmitry Mikulik**, Mikhail Mintairov, Ian Nachemson, Valery Evstropov, Pablo Romero-Gomez, Maxim Shvarts and Anna Fontcuberta i Morral, Extraction of series resistance in GaAs nanowire based solar cells using light concentration, *Nanotechnology*, under preparation.

Resume

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SUMMARY

- PhD degree in Materials Science from EPFL (Switzerland)
- 3 years of industrial experience in Samsung Electronics including R&D activities on 3D memory developing
- 9-month internship with Stanford University on III-V and Si MOS fabrication and characterization

EDUCATION

1. PhD in Materials Science, September 2018
EPFL (École polytechnique fédérale de Lausanne), Lausanne, Switzerland
Thesis "III-V Semiconductor nanowire-based solar cells: fabrication and characterization"
Courses included:
Advanced experimental methods in condensed matter and nanophysics
Methods of Modelling and Simulation of Materials Science
Modern photovoltaic technologies
Semiconductor photonics and quantum structures
Modelling micro-/nano- field effect electron devices

2. Bachelor and Master of Science in Micro and Nano electronics, June 2005 and June 2007
Saint Petersburg State Electro Technical University, St Petersburg, Russia
Thesis "III-N layers on sapphire and silicon substrates: growth and study of its properties"

EXPERIENCE

Abroad Internship during PhD, February 2017-October 2017
Stanford University, Stanford, California, USA

- Surface passivation of Si and III-V semiconductor micro/nano structures by ALD grown high-k dielectrics
- Characterization of the semiconductor-oxide interface by electrochemical impedance spectroscopy
- Automatization of the data analysis using Python

Doctoral Assistant, October 2014 to January 2017, November 2017 to September 2018

Materials Science Dept., EPFL, Lausanne, Switzerland

- Work on PhD thesis: clean room activities, device design, characterization
- Supervising Bachelor and Master students during semester projects
- Lab equipment development: EQE setup, Optical (reflectance, transmittance) setup

Senior Engineer, November 2013-September 2014
Samsung Electronics, Suwon, South Korea

- Ge-on-SOI LMG growth method for logic applications - AMAT Epi Centura CVD system
- Laser Annealing System for Si passive devices in Optical Interconnect - process development (*1 patent*)
- Si SEG process development for 3D VNAND Flash memory - mini-batch LPCVD tool.

Research Staff Member, January 2012-October 2013
Samsung Advanced Institute of Technology (SAIT), Suwon, South Korea

- Free-standing GaN on Si substrate, CVD growth method (*1st in the world*)
- Non-polar and semi-polar GaN on sapphire by CVD
- Vertical CVD reactor design

Researcher, June 2007-August 2011
Ioffe institute, St Petersburg, Russia

- GaN-on-Si technology - growth of GaN bulk layers on silicon substrate.
- X-ray detector for medical applications – developing of GaAs detector structure (p-i-n diode)

ACTIVITIES

- Co-author of >10 scientific papers
- Co-author of 1 patent
- Grant holder: Bortnik fund (Russia), SNSF (Switzerland), NanoTera (Switzerland)
- 4 oral presentations on international conferences
- Simulation experience: Nextnano
- Process experience:
  - ✓ Wet and dry etching (acid, base, RIE, IBE)
  - ✓ E-beam lithography
  - ✓ Thin film deposition (PECVD, Sputtering, e-beam evaporation)
  - ✓ Polymer processing (SU-8, PDMS, photoresists)
  - ✓ RTA, CVD, ALD, wafer cleavage
- Characterization experience:
  - ✓ SEM, AFM, optical microscopy
  - ✓ Electrical characterization: IV, CV
  - ✓ Optical characterization: EQE, reflectance/transmittance, PL
- Growth experience:
  - ✓ HVPE (GaN, GaAs)
  - ✓ CVD (Si, Ge)