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***Abstract*—With the implementation of energy efficiency regulations for all ships, DC shipboard power systems (SPS) have attracted much attention from the shipbuilding industry due to their advantages in fuel savings with variable speed engines and the closed bus-tie operation for dynamic positioning vessels. However, DC protection coordination is one of the main obstacles to employ DC power systems into ship power networks. Because, in the DC SPSs, fast fault clearing, e.g., several milliseconds, is necessary to avoid the failure of power converters which have much lower short-circuit withstand capabilities than conventional AC electrical equipment, e.g., generators, transformers and cables. This paper presents a comprehensive analysis of voltage drops and fault clearing time to achieve protection selectivity for centralized and distributed DC SPSs. Furthermore, impacts of additional bus capacitance, which is combined with the existing DC SPSs, are analysed in terms of the protection selectivity. The results show that employing the additional bus capacitance has great advantages in a bus protection by mitigating the voltage drop at the unfaulted bus and a feeder protection by providing the selectivity between the faulty and the adjacent feeders.**

***Index Terms*—Protection Coordination, Shipboard Power Systems, DC Micro Grids, Selectivity, Bus-Tie Breaker, Fuse**

I. Introduction

One of the main issues in the shipbuilding industry is to comply with energy efficiency regulations by the International Maritime Organization like the Energy Efficiency Design Index and the Ship Energy Efficiency Management Plan [1]. A promising solution to achieve high efficient ships is the DC SPSs, as shown in Fig. 1, with its main benefits in the marine domain. The DC SPSs can reduce the fuel consumption up to $20\,\%$ by employing variable speed engines compared to fixed speed engines which are applied to keep constant power frequency (50 or $60\,\mathrm{Hz}$) [2]. In addition, the closed bus-tie operation for dynamic positioning vessels is available with the DC distribution systems and it can improve the energy efficiency by reducing the number of engines in service [3].

This new concept of power systems comes with technical challenges in the protection coordination due to very low thermal withstand capability of semiconductors and different fault characteristics compared to AC power systems [4]. The DC SPSs proposed in [2], [3] have three level protections in common: first level - bus protection with solid-state circuit breakers ($10-40\,\mu\mathrm{s}$), second level - feeder protection with high speed fuses ($0.2-1\,\mathrm{ms}$) and third level - generator and rectifier fault control ($0.003-10\,\mathrm{s}$), e.g., excitation removal for a diode rectifier [3] and fold-back fault control for a thyristor rectifier [5]. While the bus and feeder protections are investigated in [6], there are still huge technology gaps which need to be examined in many aspects of the system protection.

This paper presents a comprehensive analysis of voltage drops for the bus protection and fault clearing time for the feeder protection depending on the system topology. The influence of the bus capacitance, which is combined with the existing DC SPSs (the centralised and distributed systems) as depicted in Fig. 1, is investigated in terms of the protection selectivity. In section II, the modelling of the DC SPS in Fig. 1 and analysis conditions are described. The analytical expression and the sensitivity analysis of a DC fault are presented in section III. In the same section, the required minimum values of the system inductance are discussed for the bus protection in four different SPSs considered in this study. The section IV deals with the feeder protection in terms of the capacitance value and the selectivity. The last section summaries the findings and the main results.

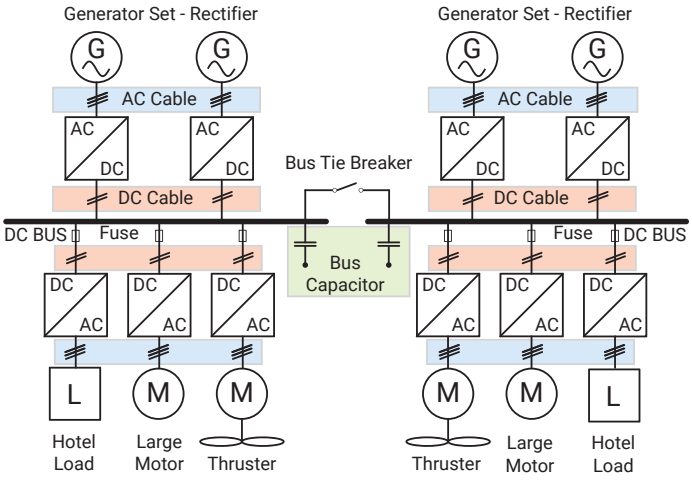

Fig. 1: Schematic of general DC SPS. In the centralised DC SPS, AC cables are used to connect generator-rectifier and inverter-motor. The distributed DC SPS integrates the converters into the DC bus through DC cables. This paper focuses on the impact of the bus capacitors integrated into the DC buses for both DC SPSs.

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II. DC SPS Modelling

There are two design philosophies to employ the DC distribution systems into the DC SPSs: centralised and distributed approaches. The main difference comes from ways to connect different equipment, e.g., generator-rectifier, rectifier-DC bus, DC bus-inverter and inverter-load. The centralised system uses AC cables to connect generator-rectifier and inverter-load. All DC parts, e.g., rectifiers, inverters, isolators and bus-tie breakers, are connected to the DC bus through metallic busbars in the cabinet. On the other hand, DC cables are mainly used to integrate the converters into the DC bus in the distributed system. The distributed system allows for installing the power converters next to the machines and can achieve higher energy efficiency by using the DC cables which have lower power losses than those of the AC cables.

Due to fast discharging characteristics of capacitors, an initial transient current during a DC fault (DC pole-to-pole fault) is mainly contributed by the DC link capacitors which are applied to the power converters. By neglecting the fault current contribution from the AC generator, the centralised DC SPS (T1) during the fault can be modelled as series R-L-C circuits in parallel connected via busbar inductance, as shown in Fig. 2a. In case of the distributed system (T3), series resistance and inductance of the DC cable plays an important role in terms of initial fault current amplitude and its rate of change. Therefore, an equivalent circuit in Fig. 2c is used to conduct a study for the distributed system. Capacitance of the DC cable is neglected because the value of the capacitance is much smaller than that of the DC link capacitor. The equivalent circuits for both two systems (T1 and T3) with the bus capacitors are depicted in Fig. 2b (T2) and 2d (T4), respectively. T2 and T4 are the main elements of the study presented in the paper. ESR and ESL in Fig. 2 are equivalent series resistance and inductance of the capacitor.

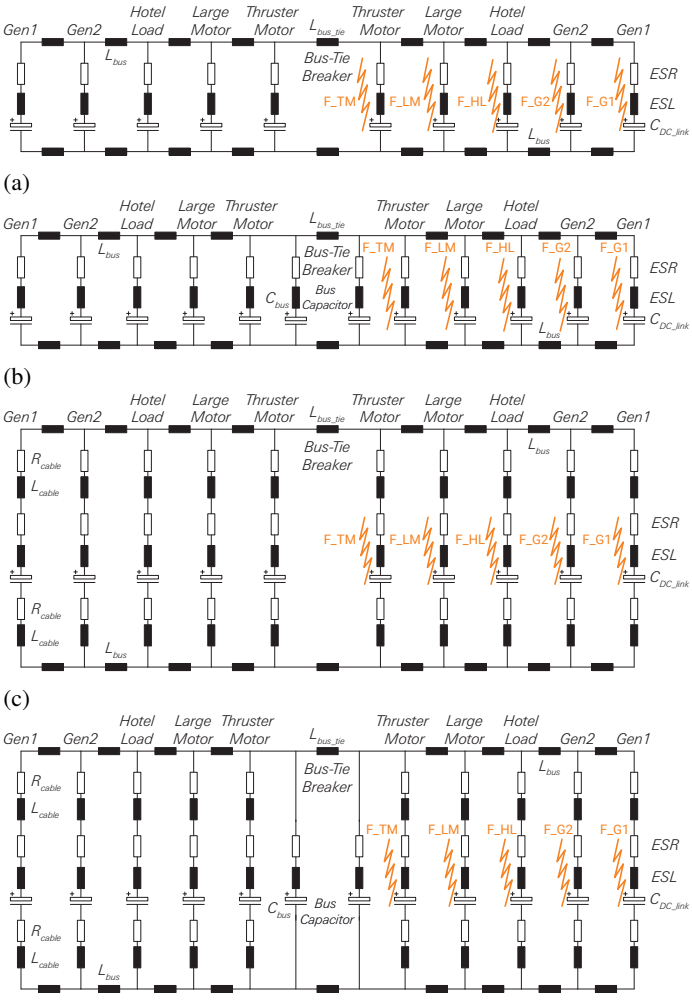


Fig. 2: Equivalent circuits for the DC SPSs: (a) centralised system (T1), (b) centralised system with bus capacitor (T2), (c) distributed system (T3) and (d) distributed system with bus capacitor (T4). Note that the considered DC SPSs are classified into the four categories: T1, T2, T3 and T4.

The system parameters used for the study are provided in Table I, where R_F is the fault resistance. Three considered ship operation modes are presented in Table II with their electric load matrix: OM1 - dynamic positioning (the maximum load condition), OM2 - port in/out (the medium load condition) and OM3 - sailing (the minimum load condition).

TABLE I
System Parameters Used for the Study

V_{DC}	$1kV$	C_{G1}, C_{G2}	$80mF$
L_{bus}	$1\mu H$	C_{HL}	$20mF$
L_{bus_tie}	$1\mu H$	C_{LM}, C_{TM}	$60mF$
R_{cable} [a]	$0.067\Omega/km$	C_{bus}	$100mF$
L_{cable} [a]	$0.284mH/km$	ESR [b]	$58m\Omega$
l_{cable}	$25m$	ESL [b]	$20nH$
R_F	$1m\Omega$		

[a] Single cable parameters. Several cables in parallel are used depending on current ratings.

[b] Data for a capacitor with $1kV$ and $5mF$. Several capacitors in parallel are used depending on capacitor ratings.

TABLE II
Electric Load Matrix for Ship Operating Mode

Electric Load		Operation Mode		
		OM1	*OM2*	*OM3*
Bus1	Gen1 (G1)	✓ [a]		
	Gen2 (G2)	✓	✓	✓
	Hotel Load (HL)	✓	✓	✓
	Large Motor (LM)	✓		✓
	Thruster Motor (TM)	✓	✓	
Bus2	Thruster Motor (TM)	✓	✓	
	Large Motor (LM)	✓		✓
	Hotel Load (HL)	✓	✓	✓
	Gen2 (G2)	✓	✓	
	Gen1 (G1)	✓		

[a] In service.

III. Bus Protection

When the fault current reaches the threshold value, the bus-tie breaker, which is based on solid-state technology to achieve ultra-fast interrupting time, rapidly interrupts the fault current, and then a voltage at the healthy bus is ramped up to be back to normal. It means that the minimum remaining voltage at the healthy bus has to be higher than any undervoltage trip conditions of the load converters during the period of fault clearing time.

A. Influence of DC Inductance

The inductance between the faulty and healthy parts plays an important role to mitigate the voltage drop at the healthy bus with its opposing characteristics in an abrupt current change. Without this inductance, all DC buses might suffer a huge voltage drop from the DC fault and it might disconnect all electric sources and loads from the buses.

An initial current of the DC fault is mainly contributed by the capacitors installed at the DC pole-to-pole because the capacitors have much faster response than the AC generators. Therefore, an equivalent circuit of the DC fault in the initial phase of the fault can be simplified as a series R-L-C circuit, as illustrated in Fig. 3. The analytical expression for the DC fault circuit (Fig. 3) with underdamped condition is:

$$i_f(t) = \frac{V_{DC0}}{\omega_d L_{eq}} e^{-\alpha t} \sin \omega_d t + \frac{\omega_0}{\omega_d} i_{DC0} e^{-\alpha t} \sin(\omega_d t + \beta) \quad (1)$$

where $\alpha = R_{eq}/L_{eq}$, $\omega_0 = 1/\sqrt{L_{eq}C_{eq}}$, $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$ and $\beta = \arctan \omega_d/\alpha$.

With the assumption of $i_{DC0} = 0$, the remaining voltage of the capacitor in pu can be calculated as:

$$\Delta V = R_{eq} i_f(t) + L_{eq} \frac{di_f(t)}{dt} = V_{DC0} e^{-\alpha t} \cos \omega_d t$$
$$\frac{\Delta V}{V_{DC0}} = e^{-\alpha t} \cos \omega_d t \quad (2)$$

Fig. 4 shows the sensitivity analysis in the remaining voltage of the DC capacitor depending on the values of the capacitor and the inductor by using Eq. (2). Note that $R_{eq} = 1m\Omega$

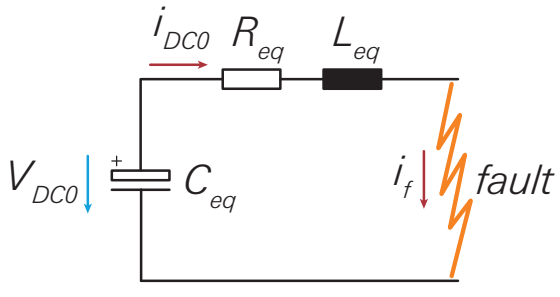


Fig. 3: Equivalent circuit for initial DC fault. The voltage of the DC capacitor V_{DC0} and the current i_{DC0} are the initial values for the DC fault current i_f. $V_{DC0} = 1pu$ and $i_{DC0} = 0$ are used for the analysis.

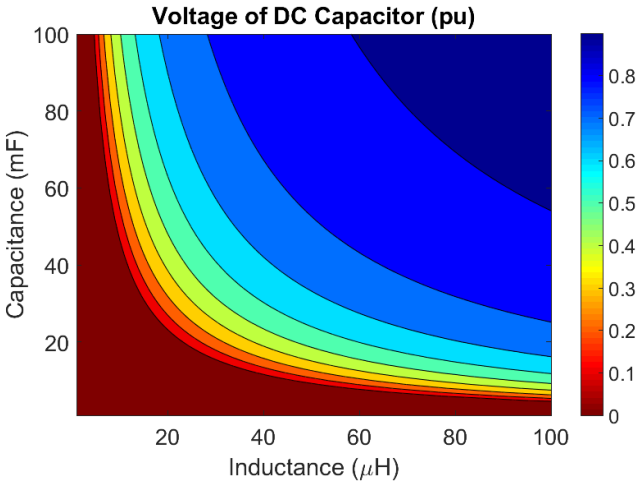


Fig. 4: Sensitivity analysis in remaining voltage of DC capacitor. $R_{eq} = 1m\Omega$ and $t = 1ms$ are used for the analysis. High remaining voltages of the DC capacitor imply its low voltage drops.

and $t = 1ms$ are used for the voltage drop analysis in this section. It is seen that high values of the capacitance mitigate the voltage drops of the DC capacitor by decreasing the dynamic coupling between the two buses. In addition, the DC inductance has more impacts on the voltage drop than the DC capacitance. The DC inductance with "several tens of microhenries" has similar effects on the remaining voltages from the DC capacitance with "several tens of millifarads" under the study condition.

B. Comparison of DC SPSs

As aforementioned, the certain value of the system inductance is necessary to maintain the bus voltage of the healthy part. The required inductance values are different for each system topology. The distributed system (T3) has much higher inductance than the centralised system (T1) due to the DC cable. The circuit conditions, e.g., operation modes and fault locations, also give a huge impact on the voltage drop.

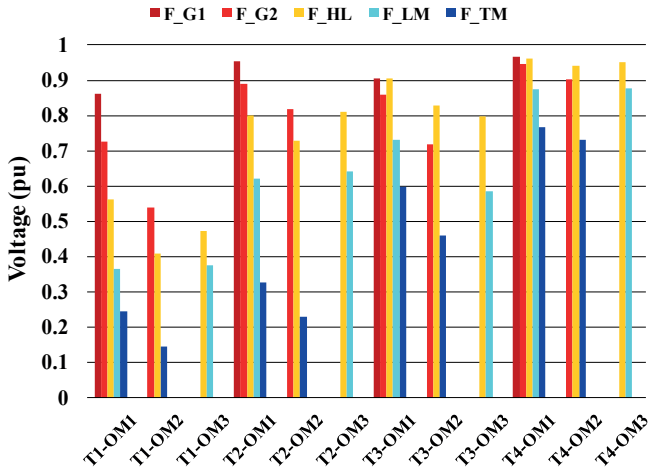


Fig. 5: Remaining voltage of healthy bus at 1 ms after fault by SPS types, operation modes and fault locations.

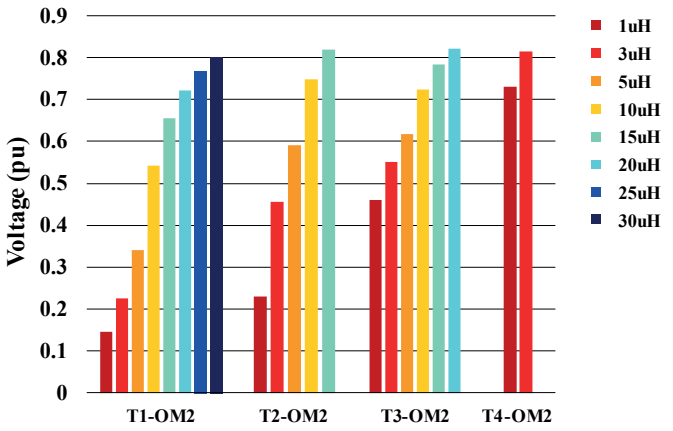


Fig. 6: Required inductance values to keep remaining healthy bus voltage with $0.8\,\mathrm{pu}$ for the four DC SPSs.

With the equivalent circuits in Fig. 2, the system parameters in Table I and the operation modes in Table II, the voltage drop analyses are carried out and the results are shown in Fig. 5. It is observed that the centralised system (T1) has higher voltage drops than the distributed system (T3) for the all operation modes. Among the operation modes, the fault at the thruster motor feeder (F_TM) develops the maximum voltage drop for the four systems considered in the study. When the additional bus capacitors with $100\,\mathrm{mF}$, as indicated in Table I, are installed at the buses, the voltage drops of both systems (T2 and T4) are improved and mitigated, compared to those of the centralised and the distributed systems without the bus capacitors (T1 and T3).

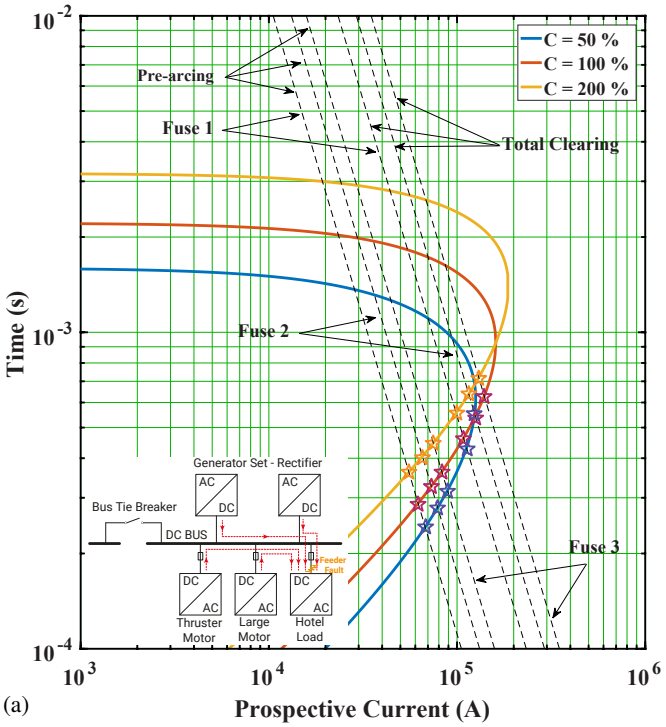
In order to ensure the reliable system design, the DC SPS has to be continuously operated under the worst scenario. In Fig. 5, the port in/out mode (OM2) with the fault at the thruster motor feeder (F_TM) is the worst case. Therefore, with this condition, the required minimum inductance for each system is analysed and presented in Fig. 6. To keep the voltage of $0.8\,\mathrm{pu}$ (chosen for the under voltage condition) at $1\,\mathrm{ms}$ after the fault, the system inductance of $3-30\,\mu\mathrm{H}$ is needed depending on the system topology. Due to lack of the system inductance in the centralised system, higher values of the inductance should be installed at the center of the bus-tie breaker (L_{bus_tie} in Fig. 2). Alternatively, by installing the bus capacitors, the required values of the inductance can be minimised. Furthermore, it can increase the system stability because high system capacitance supports the system stability, while high system inductance might cause the instability issues depending on the system condition and converter type [7].

IV. Feeder Protection

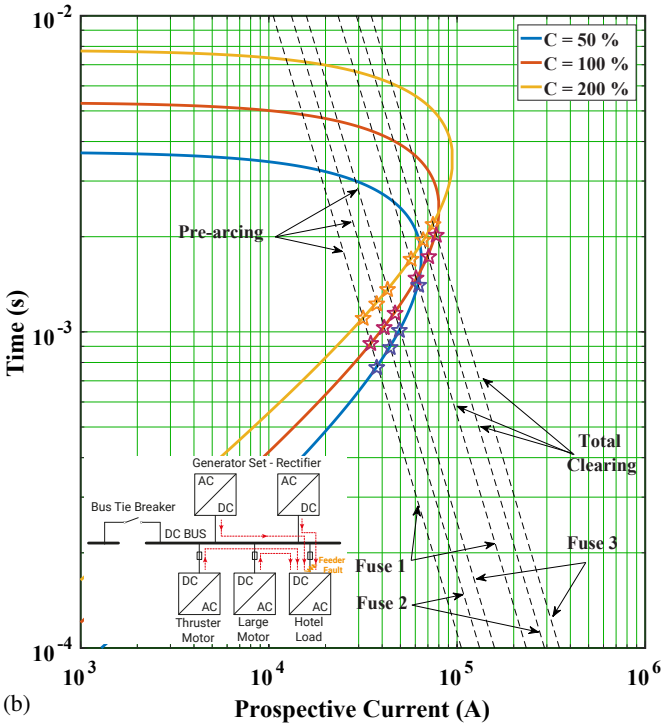
After the bus protection, the high speed fuse (or semiconductor fuse) isolates the faulty feeder by melting its elements within several hundreds of microseconds. In the DC SPSs, the system capacitance is the main energy source to blow up the fuse and its value is related to the total clearing time of the fuse, which is the total time taken by a fuse to clear a fault. Therefore, the influence of the DC capacitance and the issues on the feeder selectivity are investigated.

A. Influence of DC Capacitance

The centralised system (T1) shows faster fault clearing time than the distributed system (T3) for the same fault in Fig 7. In case of "C = $100\,\%$", the total clearing times are about $0.45-0.65\,\mathrm{ms}$ for T1 and about $1.5-2.0\,\mathrm{ms}$ for T3 under the



(a)



(b)

Fig. 7: Time-current curves depending on different capacitor values for the DC SPSs: (a) centralised system (T1) and (b) distributed system (T3). "C = $50\,\%$" is the half of the capacitance values in Table I and "C = $200\,\%$" means the twice of those in Table I.

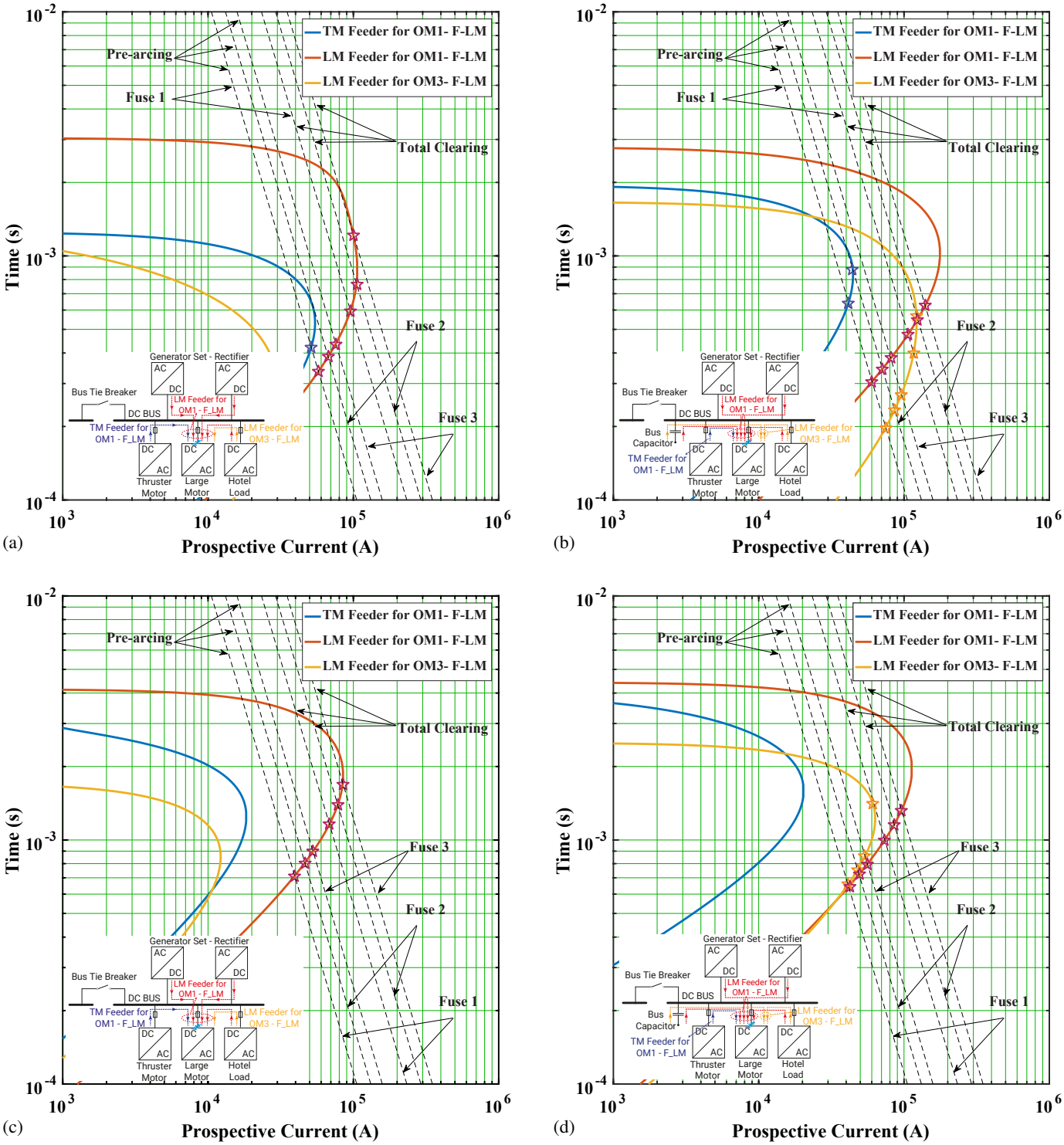


Fig. 8: Selectivity and sensitivity analysis for the DC SPSs: (a) centralised system (T1), (b) centralised system with bus capacitor (T2), (c) distributed system with bus capacitor (T3) and (d) distributed system with bus capacitor (T4).

selected fuses (Fuse 1, 2 and 3). For T3, the time coordination between the feeder protection (the second protection) and the generator-rectifier fault control (the third protection) is hard to implement with these total clearing times. Because the time margin between the two protections needed to increase the protection reliability is not enough, when the operation time of the third protection and the short-circuit capability of semiconductors are considered. Furthermore, it is seen for both systems (T1 and T3) that the higher value of the capacitance ("C = 200 %") increases the current amplitude as well as the fault energy. However, the DC SPSs with high capacitance ("C = 200 %") have slow rising response of the prospective

current and provide the delayed fault clearing time compared to the lower capacitance case ("C = $50\,\%$"). Note that the total clearing ratings (total clearing I^2t) of the fuses considered are assumed as specific values and the total clearing characteristics are drawn by these specific total clearing ratings (I^2t) to simplify the analysis in this section.

B. Feeder Selectivity and Sensitivity

There are two important technical aspects in the system protection: selectivity and sensitivity. The selectivity means that the fuse connected on the faulted feeder has to clear the fault without the pre-arcing of the fuses connected on other feeders. On the other hand, the sensitivity implies that the fuse on the faulted feeder has to clear the faults for the maximum fault condition as well as the minimum fault condition. The system protection by use of the fuse must be designed with the consideration of these aspects. Therefore, the analysis of the selectivity and the sensitivity of the feeder protection are conducted for the four systems and the time-current curves for these analyses are shown in Fig. 8.

For the centralised system (T1) in Fig. 8a, while the Fuse 2 and 3 provide the selectivity between the fuse on the LM feeder (faulty feeder) and the fuse on the TM feeder (healthy feeder and having the same fuse/current rating with the LM feeder), the sensitivity cannot be achieved for OM1 and OM3 due to the low current amplitude and the fault energy under OM3. This sensitivity issue is also observed for the distributed system (T3) in Fig. 8c. The sensitivity issue comes from the fact that the fault energy passing through the fuse on the TM feeder is only provided by the capacitor of the hotel load (C_{HL}) for OM3. The fault energy from C_{HL} is not sufficient to blow up the fuse on the large motor because the value of C_{HL} chosen in this study is one-third of the capacitor for the large motor (C_{LM}) shown in Table I.

In the two systems (T2 and T4), the bus capacitor of $100\,\mathrm{mF}$ directly contributes the additional fault energy passing through the fuse on the faulty feeder under any fault conditions, as shown in Fig. 8b and 8d. In addition, from the comparison of the cases with (T2 and T4) and without (T1 and T3) the bus capacitor, it is observed that the bus capacitor reduces the rate of rise and the maximum value of the current passing through the fuse on the healthy feeder (TM feeder). With these capacitors, the sensitivity issue can be resolved.

In Fig. 8b, the selectivity between the LM feeder and the TM feeder is achievable with the Fuse 1 and 2 for T2. In case of the Fuse 3, there is no time margin between the total clearing time of the LM feeder for OM1 and the pre-arcing time of the TM feeder for OM1.

The benefit of the additional bus capacitance is more significant for the distributed system with the bus capacitors (T4). As shown in Fig. 8d, the current amplitude of the TM feeder is clearly smaller than that of the LM feeder for OM1 and OM3. It means that faster fault clearing for T4 is available if higher value of the bus capacitor than the value of C_{bus} considered in this study is applied to T4.

V. Conclusion

This paper has presented the selectivity for the bus and feeder protections in the DC SPSs. It has been demonstrated that the installation of the additional bus capacitors gives a big benefit for the protection selectivity, although it slightly increases the electrical installation cost. With the modelling for the four DC SPSs, the roles of the system inductance and capacitance have also been investigated.

High values of the DC capacitance and the DC inductance are effective to mitigate the voltage drop of the healthy bus. Especially, the inductance value plays a more important role than the capacitance value in the bus protection. Due to lack of the system inductance, the centralised system shows the higher voltage drops compared to the distributed system. The proposed system topology, by combining the existing DC SPSs (the centralised and distributed systems) with the bus capacitors, improves the selectivity for the bus protection by mitigating the voltage drop.

For the feeder protection based on the fuse technology, the centralised system provides much faster fault clearing time compared to the distributed system. While higher value of the capacitance supplies the high fault energy, it takes more time to clear the fault. The fuse coordination is not available in terms of the selectivity and the sensitivity for the existing centralised and distributed systems. The additional bus capacitance provides excellent performances in the protection selectivity by directly contributing the additional energy to the fuse on the faulted feeder under any conditions.

Acknowledgment

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