This article may be downloaded for personal use only. Any other use requires prior permission of the author and AIP Publishing.

This article appeared in A. Marette et al, “Yttrium zinc tin oxide high voltage thin film transistors”. Appl. Phys. Lett. 113, 132101 (2018) and may be found at http://doi.org/10.1063/1.5048992

APPLIED PHYSICS LETTERS **113**, 132101 (2018)

Yttrium zinc tin oxide high voltage thin film transistors

Alexis Marette,[a] Herbert R. Shea, and Danick Briand

Ecole Polytechnique Fédérale de Lausanne (EPFL), Institute of Microengineering (IMT), Soft Transducers Laboratory (LMTS), Neuchâtel 2000, Switzerland

(Received 19 July 2018; accepted 12 September 2018; published online 25 September 2018)

We demonstrate that doping the semiconductor zinc tin oxide (ZTO) with yttrium leads to a high-voltage thin film transistor (HVTFT) with enhanced switching performance. Adding 5% yttrium leads to an increase in the on-off ratio from 40 to 1000 at an operating voltage of 500 V and to a drop of the subthreshold swing from 65 to 35 V/dec. The performance is improved because of the reduction of the saturation voltage and because of a decrease in the off-current from several μA for undoped ZTO HVTFTs to 100 nA for $Y_{5\%}$ZTO. The decrease in saturation voltage and off-current can be attributed to a lower trap concentration leading to enhanced space-charge limited current and to a decrease in the background charge carrier concentration. At a 500 V bias voltage, an inverter circuit with a yttrium-doped ZTO HVTFT can control the output voltage between 50 V and 500 V, while the undoped ZTO HVTFT can only control the output voltage between 150 V and 450 V. The improvement in high voltage performance of yttrium-doped ZTO HVTFTs is important for future work related to high voltage thin film transistors made of amorphous oxide semiconductors as it demonstrates that this technology enables HVTFTs with simultaneously high operation voltage, high on-current, and high on-off ratio. *Published by AIP Publishing.*
https://doi.org/10.1063/1.5048992

Applications of high-voltage (>100 V) electronics are growing in numbers in the fields of MEMS,[1] X-ray detectors,[2] solar cells,[3] and soft actuators such as dielectric elastomer actuators (DEAs).[4] Designing high-voltage components that can be integrated with these transducers, such as high-voltage diodes[5] or high-voltage thin film transistors (HVTFTs),[1–4,6–10] is critical to achieve more complex devices such as arrays,[1,4] displays,[3,4,6] or soft robots.[11,12] Integrated high-voltage electronics can replace the more traditional bulky optocouplers and power MOSFETs, which limit the compactness of arrays made of high voltage transducers. In particular, HVTFTs are interesting components as they enable compact integration of high voltage transistors on flexible insulating substrates.[4,9]

HVTFTs require a different architecture compared to their lower voltage counterparts, which are designed for optimal operation below 10 V. The HVTFTs can operate at high voltage with a gate electrode offset from the drain, also called offset gate,[1,3,4,6–10] a thicker gate dielectric with high breakdown strength[4,13] and field plates.[7,9,10] These modifications to the transistor gate increase the device breakdown voltage by 1 to 2 orders of magnitude.[1,4,9] However, those modifications strongly decrease the HVTFT transistor performance: the on-off ratio of a HVTFTs is usually lower than 10^4 and the subthreshold swing value can be higher than 10 V/dec. The performance of HVTFTs also depends on the semiconductor used for the channel. Amorphous oxide semiconductors (AOSs) offer advantages over other semiconductors for use in HVTFTs, such as amorphous silicon (a-Si),[1,7] polycrystalline silicon (poly-Si),[6,14] and organic materials:[9,10] AOSs exhibit a high mobility of up to 100 $cm^2/V\,s$[15] and are resistant to short channel effects and therefore to high electric field effects.[16,17] AOSs generally exhibit n-type behaviour, and their electronic properties can be tuned by varying the stoichiometry of the metallic cations.[18,19] Zinc tin oxide (ZTO), in particular, is an interesting AOS as it is an indium free and ternary alloy, which is printable and can exhibit a mobility of up to 30 $cm^2/V\,s$.[23] We reported in Ref. 4 a ZTO HVTFT with a high on current of $I_{on} = 100\,\mu$A operating at 1 kV. However, the on-off ratio of such a ZTO HVTFT is low, 20 at 100 V gate voltage, because of its high off-current higher than 1 μA.

In this letter, we report the design and characterization of the first ZTO HVTFT doped with yttrium. By comparing doped and undoped HVTFTs, we demonstrate that doping ZTO with yttrium leads to better transistor performance at high voltage: the YZTO HVTFTs have a high on-current of 100 μA, an improved on-off ratio of 10^3, and reduced high electric field effects at 500 V. The device had an offset gate of 50 μm and a dielectric stack made of Al_2O_3 and Parylene-C to achieve 500 V operation. It was fabricated on a flexible substrate, polyimide. In an n-type inverter circuit architecture under a 500 V bias voltage, the YZTO HVTFT could switch the output voltage from 50 to 500 V, while an undoped ZTO HVTFT could only drive it from 150 V to 450 V.

Yttrium zinc tin oxide is a quaternary AOS with three metallic cations, yttrium, zinc, and tin. In the ZTO thin film, Yttrium acts as a strong oxygen binder. For low-voltage technologies (<100 V operation voltage), yttrium doping has been reported to cause improvements of the on-off ratio and the decrease in the subthreshold swing at low concentration doping (<5%).[19,21,22] At a higher concentration, adding yttrium leads to the formation of insulating regions of yttrium oxide in the thin film and, consequently, to lower performance.[22]

[a]Author to whom correspondence should be addressed: alexis.marette@epfl.ch

To operate a 500 V YZTO HVTFT, a dielectric stack consisting of a 1 μm Parylene-C and a 100 nm Al_2O_3 layer was used, as well as an offset gate shifted by 50 μm, similar to the architecture shown in Ref. 4. The channel length was 500 μm in order to avoid short-channel effects under a high electric field. The HVTFT channel width was 5 mm resulting in a W/L of 10. The semiconductor synthesis used the same sol-gel process requiring an annealing step at 450 °C as described in Ref. 4. As a consequence, a top gate coplanar electrode architecture was implemented to ensure compatibility with the Parylene-C used as part of the gate dielectric. Figure 1 is a cross-section and a top-view of the HVTFTs.

The HVTFTs were fabricated on a polyimide substrate (UBE, Upilex 50S) coated with a 20 nm-thick aluminium oxide layer deposited by atomic layer deposition (ALD). ZTO and YZTO were synthesized based on a sol-gel process with chloride precursors.[20,23] The precursor solution was made from 0.2 M commercial zinc chloride (99.9% purity, Sigma-Aldrich) and tin chloride (>99.9% purity, Sigma-Aldrich) with Z:T = 2:1 mixed in acetonitrile (>99.9% purity, Sigma-Aldrich) and ethylene glycol (anhydrous 99.8% purity, Sigma-Aldrich). Yttrium chloride (>99.9% purity, Sigma-Aldrich) was then added to produce solutions with 0%, 3%, and 5% of yttrium concentration. The solutions were stirred for 24 h. The semiconductor was deposited by spin-coating (500 rpm) on the polyimide substrate. To solidify the thin film, it was first cured at 120 °C in air for 1 h. The sol-gel process was triggered by annealing the film at 450 °C in air for 1 h. The thin-film thickness was evaluated by ellipsometry to be 40 nm. A comparison between the HVTFTs made with ZTO, $Y_{3\%}$ZTO, and $Y_{5\%}$ZTO is summarized in Table I. The oxygen spectra of the synthesized ZTO and YZTO thin films are shown in Fig. 2. The deconvoluted spectra (530 eV for Metal-Oxygen-Metal bonds in red and 531.4 eV for oxygen vacancies in green) are represented in the plot. The concentration of oxygen vacancies increased with the increasing yttrium concentration: 12%, 19%, and 22% vacancies for ZTO, $Y_{3\%}$ZTO, and $Y_{5\%}$ZTO doped ZTO films, respectively. The dielectric was made of a stack of 100 nm ALD aluminium oxide and 1 μm Parylene-C layers. The source, drain, and gate electrodes have been patterned by the e-beam evaporation of 200 nm-thick aluminium films through shadow masks.

The HVTFT current versus voltage behaviour was characterised with a high-voltage measurement setup consisting of two high-voltage regulated DC-DC converters (EMCO CA20P for the drain and CA02P and CA02N for the gate) and a shielded current-voltage amplifier.[24] Ten HVTFTs were tested for each doping level. The output characteristics (I_d-V_d) are plotted in Fig. 3(a) for ZTO, Fig. 3(b) for $Y_{3\%}$ZTO, and Fig. 3(c) for $Y_{5\%}$ZTO. The transfer characteristics (I_d-V_g) at

TABLE I. Comparison of properties of ZTO, $Y_{3\%}$ZTO, and $Y_{5\%}$ZTO HVTFTs.

	ZTO	$Y_{3\%}$ZTO	$Y_{5\%}$ZTO
Oxygen vacancies[a]	12%	19%	22%
Metal-oxide bonds[a]	88%	81%	78%
Saturation mobility	0.1 cm^2/V s	0.3 cm^2/V s	0.8 cm^2/V s
Off-current	2 μA	2 μA	100 nA
On-off ratio	30	30	10^3
Subthreshold swing	65 V/dec	49 V/dec	35 V/dec
Inverter[b] gain	13	19	19
Inverter[b] gate voltage swing	40 V	25 V	35 V
Inverter[b] output voltage variation	310 V	380 V	450 V

[a]Proportion taken from the entire XPS oxygen spectrum.
[b]With a 500 V bias voltage and a 100 MΩ pull-up resistor.

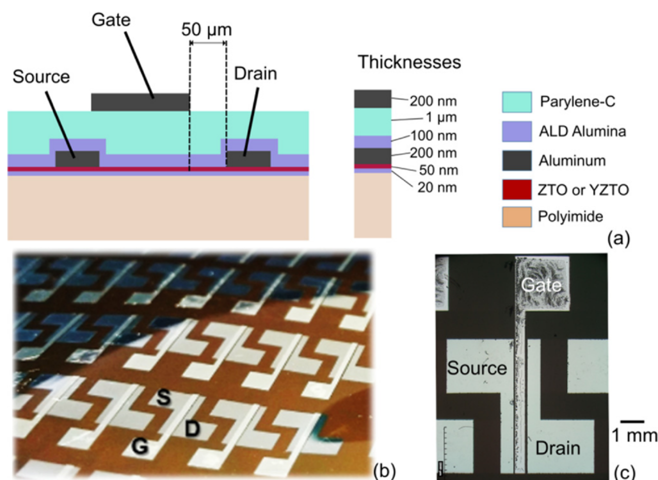

FIG. 1. (a) Cross-section of the high-voltage thin film transistor, using a top gate coplanar electrode configuration. (b) Picture of an array of high-voltage thin film transistors. (c) Optical microscope picture of one HVTFT. The channel width is 5 mm and the channel length is 500 μm. The offset gate is 50 μm.

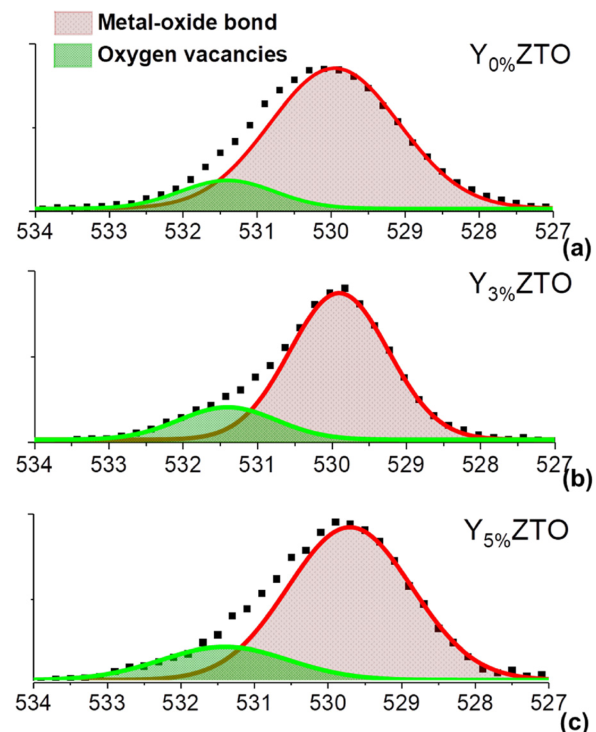

FIG. 2. X-ray photoelectron spectroscopy (XPS) peaks for the oxygen (O1s) spectrum 10 nm below the surface of the thin-film of (a) ZTO, (b) Y3%ZTO, and (c) Y5%ZTO. It was deconvoluted into two peaks centered at 530 eV for the metal oxide bonds and at 531.5 eV for the oxygen vacancies, respectively. The relative concentrations of oxygen vacancies for ZTO, $Y_{3\%}$ZTO, and $Y_{5\%}$ZTO are 12%, 19%, and 22%, respectively. The relative concentration of metal oxide bonds for ZTO, $Y_{3\%}$ZTO, and $Y_{5\%}$ZTO is 88%, 81%, and 78%, respectively, demonstrating the formation of the metal oxide thin film.

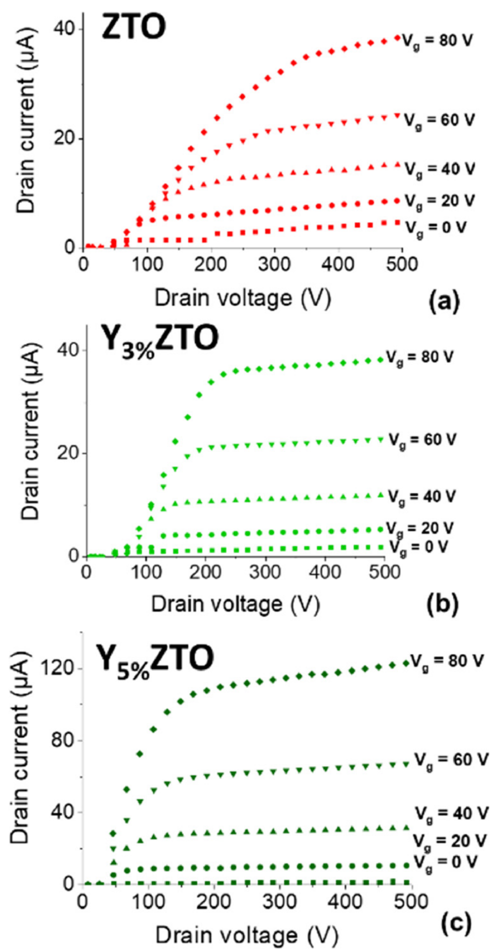

FIG. 3. Output characteristics of HVTFTs with channels made of (a) ZTO, (b) $Y_{3\%}$ZTO, and (c) $Y_{5\%}$ZTO.

500 V are plotted in Fig. 4. We extracted a saturation mobility of $0.10 \pm 0.08\,cm^2/V$ s for ZTO, $0.3 \pm 0.2\,cm^2/V$ s for $Y_{3\%}$ZTO, and $0.8 \pm 0.3\,cm^2/V$ s for $Y_{5\%}$ZTO. The subthreshold swing for these high-voltage TFTs decreased with the increasing yttrium concentration with 65 ± 15 V/dec, 49 ± 10 V/dec, and 35 ± 15 V/dec for undoped, 3% doped, and 5% doped ZTO. Adding 5% of yttrium led to a reduction by an order of magnitude of the off-current, from 2 μA for undoped and 3% yttrium doped ZTO down to 100 nA for 5% yttrium doped ZTO. An on-off current ratio of 10^3 was achieved for 5% yttrium doping in comparison to 30 for undoped ZTO and 3% yttrium doped ZTO. The saturation voltage shifted to lower values with the increasing yttrium concentration, suggesting that high voltage effects due to the offset gate, such as space-charge limited current, affected less the HVTFT with a higher yttrium concentration.

We then evaluated the behaviour of the undoped and yttrium doped ZTO HVTFT when incorporated in a resistive-load inverter. The circuit consists of a 100 MΩ pull-up bias resistor and a pull-down HVTFT. Figure 5(a) shows the output voltage response of the resistive load inverter. Under a constant 500 V bias voltage, the ZTO HVTFT switched the output voltage from 450 V down to 140 V with a gate voltage swing of 40 V. As summarized in Table I, the $Y_{3\%}$ZTO and the $Y_{5\%}$ZTO HVTFT switched the output voltage from 420 V down to 40 V within 25 V gate voltage swing and from 500 V down to 50 V within 35 V

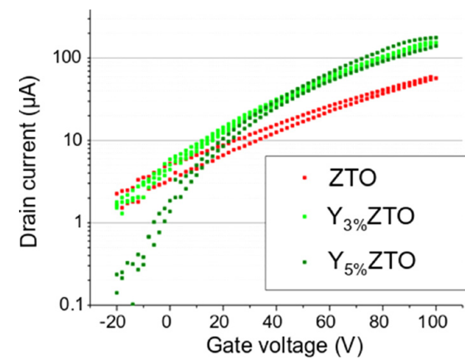

FIG. 4. Transfer characteristics of ZTO, $Y_{3\%}$ZTO, and $Y_{5\%}$ZTO HVTFTs.

gate voltage swing, respectively. The output voltage amplitude increased with the yttrium doping concentration. The lower output voltage at higher gate voltage values can be explained by the drop of the saturation voltage with the increasing yttrium concentration and the steeper output curves in the pre-saturation regime. The higher output voltage at a lower gate voltage value for $Y_{5\%}$ZTO HVTFTs can be explained by the lower off-current obtained for this device, which suppresses a voltage divider effect between the bias resistor and the HVTFT. Figure 5(b) shows the gain of the inverter, obtained by differentiating the output voltage with the gate voltage. The gain of the YZTO inverters is higher with peak values of 19 V/V versus 13 V/V for the ZTO inverters. The input voltage bands are broad, in the

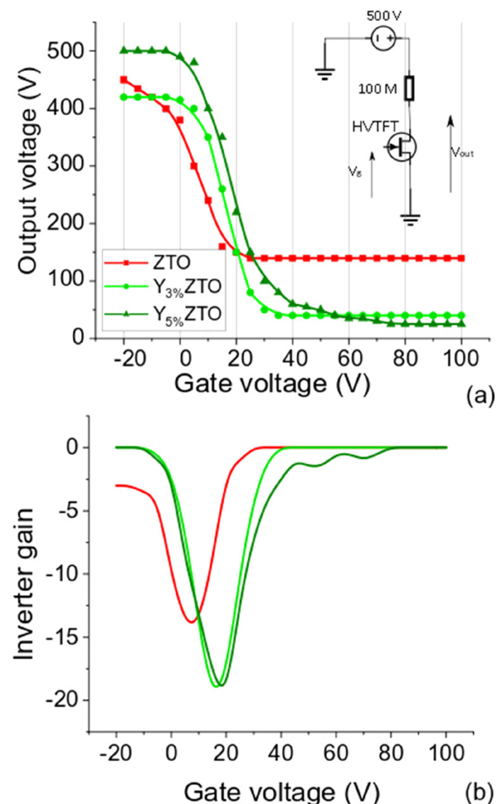

FIG. 5. (a) High-voltage resistive inverter response of the ZTO, $Y_{3\%}$ZTO, and $Y_{5\%}$ZTO HVTFT under a high voltage circuit bias. Due to its low off-current and decreased high electric field effects, the $Y_{5\%}$ZTO TFT is able to control over 450 V of the circuit output voltage. (b) Inverter gain vs applied gate voltage. The YZTO HVTFTs are able of higher inverter gain than the ZTO HVTFTs.

order of 40 V in all cases, demonstrating that the three inverters can operate as high-voltage analog amplifiers.

To explain the better electrical characteristics of yttrium doped ZTO HVTFTs, we first discuss the drop in off-current and then in saturation voltage. The decrease in off-current is in agreement with recent published research on low-voltage yttrium doped metal oxide TFTs.[21,25,26] The increase in oxygen vacancies seen in Fig. 2 has been attributed to the size of the yttrium atom, which leads to disorder in the structure of the metal oxide thin film.[21] This has been reported to lead to the formation of deep donors, which have a minor impact on the semiconducting properties of YZTO.[22] The decrease in the off-current of YZTO could therefore be due to a substitution of shallow donors in the undoped ZTO thin film with deep donors in the YZTO thin film. The drop of saturation voltage correlates with the evolution of the shape of the pre-saturation region of the HVTFT with the increasing yttrium concentration. Several groups have shown that the current in the offset region of the HVTFT is space-charge limited.[4,7,9] As a consequence, the pre-saturation region does not have a linear shape but a quadratic shape. The current density flowing through a space-charge region with traps follows a modified Mott-Gurney's law[27]

$$j = \frac{9}{8}\frac{\mu\varepsilon\varepsilon_0}{L^3}\theta_0 V^2, \quad (1)$$

where μ is the semiconductor mobility, $\varepsilon\varepsilon_0$ the permittivity of the semiconductor, L its length, V the voltage applied across it, and θ_0 the proportion of total free charges, which can be expressed as[27]

$$\theta_0 = \frac{\rho_f}{\rho_f + \rho_t} = \frac{N_c}{N_t}\exp\left(-\frac{A}{k_B T}\right), \quad (2)$$

where ρ_f and ρ_t are the density of free charges and trapped charges in the semiconductor, respectively, N_c is the density of states in the conduction band, N_t is the density of traps, A is the energy distance of the trap energy level from the conduction band, k_B is Boltzmann's constant, and T is the temperature. We can distinguish two cases: case (i) the concentration of trapped charges is negligible in the offset region compared to the number of free charges ($\theta_0 = 1$) as shown in Fig. 6(a); and case (ii) the concentration of trapped charges is important in the offset region ($\theta_0 < 1$), as shown in Fig. 6(b). Figure 6(c) shows the experimental output characteristic data for a gate voltage of 80 V for ZTO, $Y_{3\%}$ZTO, and $Y_{5\%}$ZTO normalized by their respective saturation current. Using the analytical expression in Eqs. (1) and (2), we plotted the output curves for an offset region with a negligible number of traps (in dashed) and with the increasing trap concentration (continuous lines). The decrease in the trapped charge density leads to a current increasing slower in the pre-saturation region in the output characteristics, thus implying an increase in saturation voltage. The comparison between the simulated output characteristics and the experimental data suggests that the addition of yttrium leads to a decrease in the density of trapped charges in the offset region. The $Y_{5\%}$ZTO output characteristics approach then a trap-free behaviour. According to Eq. (2), the concentration of trap states could be several orders of magnitude smaller than the density of states in the conduction band. Electron traps, in particular, might be far less abundant in YZTO thin films than in ZTO thin films. The increase in the subthreshold swing with the increased yttrium concentration can also be interpreted as a decrease in the trap concentration in the semiconductor, corroborating this analysis. In addition to space-charge limited current, self-heating effects could also affect the HVTFTs and have an impact on the electrical characteristics as demonstrated for AOS in Ref. 28.

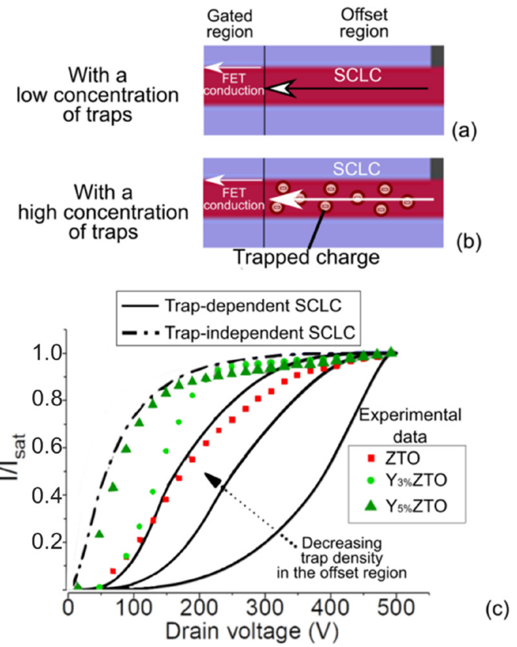

FIG. 6. Cross-sections of the HVTFT channel in the offset-region with (a) trap-free space-charge limited current and (b) trapped charge space-charge limited current. Normalized output characteristics of the HVTFTs at a gate voltage of 80 V. The current has been normalized by the saturation current. We compare space charge limited current output curves modeled based on Mott Gurney's relation with (continuous black line) and without (dashed line) trapped charges in the offset.[27]

In summary, we experimentally demonstrated that yttrium-doped YZTO HVTFTs have superior performance compared to undoped ZTO HVTFTs, exhibiting a higher on-off ratio and high on-current and operation at 500 V. In an inverter biased with a 500 V power supply, the $Y_{5\%}$ZTO HVTFTs could control the output voltage between 50 and 500 V with only 35 V gate voltage swing. This work demonstrates that cation concentration tuning, an advantage specific to metal oxide semiconductors, is not only critical to optimize HVTFT performance but also can lead to the reduction of undesirable effects of high voltage operation. Future work includes optimization of the yttrium doping concentration, reliability studies of the HVTFTs, and their system implementation with high voltage actuators.

This work was supported by the Swiss National Science Foundation (Grants Nos. 200020-153122 and 200020-165993). The authors thank Pierre Mettraux (EPFL-MHMC) for the XPS characterizations, the EPFL-CMi staff for the TFT microfabrication, Christine de Saint-Aubin and Peter Van der Wal for their help with the chemical synthesis, Sam Schlatter for proof-reading, and the LMTS Team for helpful comments and discussions.

[1]E. M. Chow, J. P. Lu, J. Ho, C. Shih, D. De Bruyker, M. Rosa, and E. Peeters, Sens. Actuators, A **130–131**, 297 (2006).
[2]W. Zhao, J. Law, D. Waechter, Z. Huang, and J. A. Rowlands, Med. Phys. **25**, 539 (1998).
[3]W.-C. Hong, C.-J. Ku, R. Li, S. Abbaslou, P. Reyes, S.-Y. Wang, G. Li, M. Lu, K. Sheng, and Y. Lu, Sci. Rep. **6**, 34169 (2016).
[4]A. Marette, A. Poulin, N. Besse, S. Rosset, D. Briand, and H. Shea, Adv. Mater. **29**, 1700880 (2017).
[5]Y. Zhang, Z. Mei, T. Wang, W. Huo, S. Cui, H. Liang, and X. Du, Nano Energy **40**, 289 (2017).
[6]T. Unagami and O. Kogure, IEEE Trans. Electron Devices **35**, 314 (1988).
[7]R. A. Martin, V. M. Da Costa, M. Hack, and J. G. Shaw, IEEE Trans. Electron Devices **40**, 634 (1993).
[8]K. S. Karim, P. Servati, and A. Nathan, Microelectron. J. **35**, 311 (2004).
[9]M. A. Smith, R. P. Gowers, A. Shih, and A. I. Akinwande, IEEE Trans. Electron Devices **62**, 4213 (2015).
[10]A. Shih, E. Schell, and A. I. Akinwande, J. Mater. Res. **33**, 149 (2018).
[11]M. Duduta, D. R. Clarke, and R. J. Wood, in *2017 IEEE International Conference on Robotics and Automation (ICRA)* (2017), pp. 4346–4351.
[12]C. T. Nguyen, H. Phung, H. Jung, U. Kim, T. D. Nguyen, J. Park, H. Moon, J. C. Koo, and H. R. Choi, in *2015 IEEE International Conference on Robotics and Automation (ICRA)* (2015), pp. 4484–4489.
[13]F. C. Luo, J. Vac. Sci. Technol. **16**, 1045 (1979).
[14]T. Unagami, IEEE Trans. Electron Devices **35**, 2363 (1988).
[15]C. Avis, H. R. Hwang, and J. Jang, ACS Appl. Mater. Interfaces **6**, 10941 (2014).
[16]H. Kumomi, T. Kamiya, and H. Hosono, ECS Trans. **67**, 3 (2015).
[17]M. Smith, "Integration of pentacene-based thin film transistors via photolithography for low and high voltage applications," PhD thesis, Department of Material Science and Engineering, MIT, 2012.
[18]K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature **432**, 488 (2004).
[19]E. Fortunato, P. Barquinha, and R. Martins, Adv. Mater. **24**, 2945 (2012).
[20]C. Avis and J. Jang, J. Mater. Chem. **21**, 10649 (2011).
[21]J. W. Hennek, J. Smith, A. Yan, M.-G. Kim, W. Zhao, V. P. Dravid, A. Facchetti, and T. J. Marks, J. Am. Chem. Soc. **135**, 10729 (2013).
[22]W. Hu and R. L. Peterson, J. Appl. Phys. **122**, 105301 (2017).
[23]Y. J. Kim, S. Oh, B. S. Yang, S. J. Han, H. W. Lee, H. J. Kim, J. K. Jeong, C. S. Hwang, and H. J. Kim, ACS Appl. Mater. Interfaces **6**, 14026 (2014).
[24]A. Marette, "High-voltage metal oxide thin film transistors to drive arrays of dielectric elastomer actuators," PhD thesis, Ecole Polytechnique Fédérale de Lausanne (EPFL), 2018.
[25]J. H. Choi, C. M. Lee, S. M. Lee, G. C. Park, B.-H. Jun, J. Joo, and J. H. Lim, Ceram. Int. **43**, 5574 (2017).
[26]M. P. Hung, J. Genoe, P. Heremans, and S. Steudel, Appl. Phys. Lett. **112**, 263502 (2018).
[27]P. N. Murgatroyd, J. Phys. D: Appl. Phys. **3**, 151 (1970).
[28]T. Hsieh, T. Chang, T. Chen, Y. Chen, M. Tsai, A. Chu, Y. Chung, H. Ting, and C. Chen, IEEE Electron Device Lett. **34**, 63 (2013).