

# **Transparent Passivating Contacts for Front Side Application in Crystalline Silicon Solar Cells**

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# Abstract

In this thesis, we present the development and characterization of novel approaches to carrier-selective passivating contacts for crystalline silicon (*c*-Si) solar cells. In our first approach, we benefit from a wide-bandgap material, namely mixed-phase silicon oxide ( $\text{SiO}_x$ ). High hydrogen dilution during the plasma-enhanced chemical vapor deposition of a  $\text{SiO}_x$  layer leads to the growth of vertically oriented silicon filaments embedded in a silicon oxide matrix. The resulting mixed-phase material combines transparency and vertical conduction through the layer. We propose a layered contact structure starting with an ultra-thin chemically grown  $\text{SiO}_x$  ( $\sim 1.2$  nm) at the *c*-Si wafer surface, followed by a phosphorus-doped bilayer of the mixed-phase  $\text{SiO}_x$ , finishing with a nanocrystalline silicon layer that ensures contact with the metallization. With such a stack, an electron-selective passivating contact with a saturation current density  $J_0$  of  $5.3 \text{ fA/cm}^2$  is achieved on n-type wafers with hydrogenation, whereas on p-type wafers the contact reached  $5.8 \text{ fA/cm}^2$  even without hydrogenation.

The contact is analyzed in detail with respect to its structure and its change upon thermal treatment. Two different growth regions are detected: one with the vertically oriented silicon inclusions and a second one in which the silicon phases have more lateral growth. Crystallization and atomic redistribution are analyzed during in-situ annealing in an electron microscope, leading to a better understanding of the change in distribution of phosphorus and oxygen as well as the nucleation sites. The influence of the annealing temperatures and dwell times as well as the initial doping concentration on the resulting in-diffused region and the passivation quality is reported. We use simulations to relate the influence of these parameters on passivation to the different recombination mechanisms.

From the analyzed phosphorus doping profiles, an interesting observation is reported. The chemical oxide varies in thickness and density depending on the wafer polarity as well as the base resistivity.

Proof-of-concept cells including this novel structure demonstrate the suitability for electron-selective passivating contacts at the device level with conversion efficiencies of 19.0% on planar wafers and 20.1% on textured wafers. Promisingly high short-circuit current densities ( $J_{\text{SC}}$ ) of  $35 \text{ mA/cm}^2$  ( $40 \text{ mA/cm}^2$ ) on planar (textured) with low parasitic absorption indicate its potential as a front contact in next-generation solar cells. Additionally, the beneficial feature of the smooth refractive index change within the layers that leads to a low reflectance over a broad wavelength range, similar to a built-in anti-reflection coating, is presented.

A second approach to reach highly transparent electron-selective passivating contacts is

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demonstrated by the use of a plasma process based on the precursor gases phosphine ( $\text{PH}_3$ ), silicon tetrafluoride ( $\text{SiF}_4$ ), hydrogen ( $\text{H}_2$ ), and argon (Ar). The beneficial effect of fluorine in terms of passivation without the need for additional hydrogenation processes is shown, reaching implied open-circuit voltages of 730 mV on planar surfaces and 707 mV on textured surfaces. These layers are implemented in first proof-of-concept working devices with efficiencies of 19.5% on single-side-textured wafers and  $J_{\text{SC}}$  values of up to 40  $\text{mA}/\text{cm}^2$ .

**Key words:**

Solar energy, photovoltaics, crystalline, silicon, solar cell, passivation, passivating, electron, selective, contact, oxide,  $\text{SiO}_2$ ,  $\text{SiO}_x$ , poly-Si, POLO, TOPCon, mixed-phase, efficiency, open-circuit voltage, PECVD, TEM, plasma, hydrogen, silane, fluorine, tetrafluorine,  $\text{SiF}_4$ .

# Résumé

L'objectif principal de cette thèse est de présenter le développement et la caractérisation de nouveaux types de contacts passivants pour cellules solaires. Ceux-ci sont sélectifs aux porteurs de charge de type électrons et permettent de nouvelles approches pour la fabrication de ces cellules. La première famille de contacts développée se base sur un matériau à bande interdite élevée, à savoir l'oxyde de silicium en phase mixte ( $\text{SiO}_x$ ). Une forte dilution d'hydrogène, pendant le dépôt chimique en phase vapeur assisté par plasma, favorise la croissance de filaments de silicium (Si) inclus dans une matrice composée elle-même d'oxyde de silicium. Cette structure en filaments associe une grande transparence optique à une excellente conductivité de charge au travers de la couche. Pour réaliser ce contact, une première couche d'oxyde de silicium ( $\text{SiO}_x$ ) ultra fin ( $\sim 1.2\text{ nm}$ ) est produite par oxydation chimique directement sur le wafer de silicium (*c*-Si). Ensuite, une couche à phase mixte dopée au phosphore, comprenant les filaments de silicium inclus dans une matrice de  $\text{SiO}_x$ , est déposée directement sur cet oxyde fin. Enfin, une dernière couche de silicium nanocristallin, également dopée au phosphore, termine le contact. Avec ce contact passivant sélectif aux électrons, pour une jonction de type  $n^+/n$ , nous avons obtenu une densité de courant de saturation de l'émetteur ( $J_0$ ) de  $5.3\text{ fA/cm}^2$  avec hydrogénation et de  $5.8\text{ fA/cm}^2$  sans hydrogénation.

Une analyse détaillée de la structure du contact et des changements induits par le traitement thermique est effectuée. Il est possible de distinguer deux zones différentes de croissance, une première contenant les filaments de silicium verticaux et une deuxième dans laquelle la croissance de la phase de silicium est plutôt latérale. La cristallisation et la redistribution atomique sont étudiées pendant le recuit in-situ à l'aide d'un microscope électronique. Ceci nous a permis de mieux comprendre le changement de distribution du phosphore et de l'oxygène dans la structure, de même que les sites de nucléation. Nous reportons l'influence de diverses températures et durées de recuit, ainsi que de la concentration initiale de dopage dans la région diffusée sur la qualité de passivation de surface. A l'aide de simulations, nous expliquons le lien entre l'influence de ces paramètres sur la passivation et les différents mécanismes de recombinaison.

Sur la base d'analyses de profils de dopage de phosphore, nous observons que l'épaisseur et la densité de la couche d'oxyde chimique dépendent de la polarité et de la résistivité de base du wafer.

Des cellules solaires utilisant ce nouveau contact passivant sélectif aux électrons démontrent des efficacités de conversion de 19.0% sur wafer poli et 20.1% sur wafer texturé. Des densités

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de courant de court-circuit prometteurs, 35 mA/cm<sup>2</sup> sur wafer poli et 40 mA/cm<sup>2</sup> sur wafer texturé, démontrant ainsi une faible absorption parasite confirment le potentiel de cette structure comme contact avant pour la réalisation de cellules solaires nouvelles générations. De plus, le changement graduel de l'indice de réfraction dans la couche est présenté. Cette particularité induit une faible réflectance sur une large gamme de longueur d'onde, comparable à une couche antireflet incorporée.

Une deuxième approche pour atteindre des contacts passivants sélectifs aux électrons et transparents est démontrée en utilisant un plasma de dépôt composé uniquement des gaz phosphine (PH<sub>3</sub>), tétrafluorure de silicium (SiF<sub>4</sub>), hydrogène (H<sub>2</sub>) et argon (Ar). L'effet positif du fluor est démontré, permettant une excellente passivation sans avoir besoin d'une étape supplémentaire d'hydrogénation. Avec cette approche nous avons atteint des tensions implicites de circuit ouvert de 730 mV (wafer poli) et 707 mV (wafer texturé). Pour démontrer l'efficacité de ce contact, nous avons fabriqué des cellules solaires à partir de wafers texturés à l'avant et poli à l'arrière, les couches décrites ci-dessus ayant été déposées sur le côté texturé. Nous avons obtenu une efficacité de 19.5% et des densités de courant de court-circuit de 40 mA/cm<sup>2</sup>.

**Mots clefs :**

Energie solaire, photovoltaïque, cristallin, silicium, cellule solaire, passivation, passivating, électron, sélectif, contact, oxyde, SiO<sub>2</sub>, SiOX, poly-Si, POLO, TOPCon, phase mixte, efficacité, tension à circuit ouvert, PECVD, TEM, plasma, hydrogène, silane, fluor, tétrafluorure, SiF<sub>4</sub>.

# Zusammenfassung

In dieser Arbeit präsentieren wir die Entwicklung und Charakterisierung neuartiger Ansätze für ladungsträgerselektive, passivierende Kontakte für kristalline Silizium Solarzellen. In unserem ersten Ansatz profitieren wir von einem Material mit einer grossen Bandlücke, genauer gesagt einer Mischphase aus Siliziumoxid ( $\text{SiO}_x$ ) und Silizium. Hohe Wasserstoff Verdünnung während der Plasmaunterstützten chemischen Gasphasenabscheidung des  $\text{SiO}_x$  layers führt zum Wachstum von vertikal orientierten Silizium Filamenten, eingebettet in der Siliziumoxidmatrix. Das resultierende Mischphasenmaterial verbindet Transparenz und vertikale elektrische Leitung durch die Schicht. Wir schlagen eine mehrschichtige Kontaktstruktur vor, die mit einer ultradünnen, chemisch gewachsenen  $\text{SiO}_x$  Schicht ( $\sim 1.2\text{ nm}$ ) an der *c*-Si-Waferoberfläche beginnt, gefolgt von einer phosphordotierten Doppelschicht aus dem  $\text{SiO}_x$ -Mischphasenmaterial und einer nanokristallinen Siliziumschicht, welche den Kontakt mit der Metallisierung gewährleistet. Mit einem solchen Schichtstapel wird auf einem n-Typ Wafer nach einer Hydrierung ein elektronenselektiver, passivierender Kontakt mit einer Sättigungsstromdichte  $J_0$  von  $5.3\text{ fA/cm}^2$  erreicht, während auf einem p-Typ Wafer auch ohne Hydrierung  $5.8\text{ fA/cm}^2$  erreicht werden.

Der Kontakt wird hinsichtlich seiner Struktur und seiner Veränderung bei der Wärmebehandlung detailliert analysiert. Wir haben zwei verschiedene Wachstumsregionen ausgemacht: Eine mit den vertikal ausgerichteten Siliziumeinschlüssen und eine zweite, in der die Siliziumphasen in lateraler Richtung stärker ausgeprägt sind. Kristallisation und elementare Veränderungen werden während des in-situ Glühens im Elektronenmikroskop analysiert. Dies führt zu einem besseren Verständnis der Umverteilung von Phosphor und Sauerstoff sowie der Nukleationsstellen. Wir berichten den Einfluss der Glühtemperaturen und Verweilzeiten sowie der anfänglichen Dotierkonzentration auf den resultierenden eindiffundierten Bereich sowie auf die Passivierungsqualität. Wir verwenden Simulationen, um den Einfluss dieser Parameter auf die Passivierung mit den verschiedenen Rekombinationsmechanismen in Beziehung zu setzen.

Aus den analysierten Phosphor-Dotierprofilen berichten wir eine interessante Beobachtung. Das chemische Oxid variiert in Dicke und Dichte in Abhängigkeit von der Waferpolarität sowie dem Basiswiderstand.

Prototyp-Zellen mit dieser neuartigen Struktur zeigen die Eignung für elektronenselektive passivierende Kontakte auf Deviceebene mit Umwandlungswirkungsgraden von 19.0% auf planaren Wafern und 20.1% auf strukturierten Wafern. Vielversprechend hohe Kurzschlussstromdichten ( $J_{SC}$ ) von  $35\text{ mA/cm}^2$  ( $40\text{ mA/cm}^2$ ) auf planaren (texturierten)

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Oberflächen zeigen durch geringe parasitäre Absorption ihr Potenzial als Frontkontakt in Solarzellen der nächsten Generation. Zusätzlich wird die vorteilhafte Eigenschaft eines glatten Übergangs der Brechungsindices innerhalb der Schichten vorgestellt, die zu einer geringen Reflexion über einen weiten Wellenlängenbereich führt, ähnlich einer eingebauten Antireflexionsschicht.

Ein zweiter Ansatz zur Erzielung hochtransparenter, elektronenselektiver, passivierender Kontakte wird gezeigt durch den Einsatz eines Plasmaprozesses auf Basis der Vorläufgase Phosphin ( $\text{PH}_3$ ), Siliziumtetrafluorid ( $\text{SiF}_4$ ), Wasserstoff ( $\text{H}_2$ ) und Argon (Ar). Wir zeigen die positive Wirkung von Fluor in Bezug auf die Passivierung ohne zusätzliche Hydrierungsprozesse und erreichen implizite Leerlaufspannungen von 730 mV auf planaren Oberflächen und 707 mV auf strukturierten Oberflächen. Diese Schichten werden in ersten Prototyp-Zellen realisiert mit Wirkungsgraden von 19.5% auf einseitig texturierten Wafern und  $J_{\text{SC}}$ -Werten von bis zu  $40 \text{ mA/cm}^2$ .

**Schlüsselwörter:**

Solarenergie, Photovoltaik, Kristallin, Silizium, Solarzelle, Passivierung, passivierend, Elektron, selektiv, Kontakt, Oxid,  $\text{SiO}_2$ ,  $\text{SiOX}$ , Poly-Si, POLO, TOPCon, Mischphase, Wirkungsgrad, Leerlaufspannung, PECVD, TEM, Plasma, Wasserstoff, Silan, Fluor, Tetrafluor,  $\text{SiF}_4$ .

# Sommario

In questa tesi, presentiamo lo sviluppo e la caratterizzazione di nuovi materiali per contatti passivanti e selettivi per celle solari in silicio cristallino (*c*-Si). Come primo approccio proponiamo un materiale con una larga banda ottica ossia l'ossido di silicio a fase mista ( $\text{SiO}_x$ ). Infatti, questo materiale ci consente di integrare nello stesso strato le proprietà di passivazione, trasporto di portatori e alta trasparenza. A tale scopo abbiamo usato un'elevata diluizione del gas di idrogeno usato per la deposizione mediante plasma enhanced chemical vapour deposition (PECVD) che ci ha concesso di realizzare dei filamenti conduttivi di silicio, per una elevata conduzione di portatori verticalmente alla layer, incorporati in una matrice di ossido di silicio altamente trasparente.

Questo lavoro ha previsto lo sviluppo di una struttura di contatto a strati che inizia con un  $\text{SiO}_x$  ultrasottile a crescita chimica (1.2 nm) sulla superficie del wafer *c*-Si, seguito da un doppio strato di  $\text{SiO}_x$  in fase mista drogato al fosforo, che termina con uno strato di silicio nanocristallino che assicura il contatto con la metallizzazione. Con tale stack, si ottiene un contatto passivante selettivo per gli elettroni con una densità di corrente di saturazione  $J_0$  di  $5.3 \text{ fA/cm}^2$  su wafers di tipo n a seguito di un processo di idrogenazione, mentre sui wafers di tipo p il contatto raggiunge  $5.8 \text{ fA/cm}^2$  anche senza idrogenazione.

Un'analisi dettagliata del contatto viene in seguito condotta in relazione alla sua struttura e alla sua variazione durante il trattamento termico. Vengono rilevate due regioni di crescita: una con le inclusioni di silicio orientate verticalmente e una seconda in cui le fasi di silicio crescono prevalentemente in direzione laterale. La cristallizzazione e la ridistribuzione atomica sono analizzate durante l'annealing in-situ in un microscopio elettronico, che fornisce un quadro più dettagliato sull'evoluzione della distribuzione di fosforo e ossigeno così come dei siti di nucleazione. L'applicazione dei trattamenti termici eseguiti (delle temperature e dei tempi di annealing), e la concentrazione iniziale di doping nello strato depositato, costituisce una parte importante dello studio perché influenzano direttamente la regione drogata diffusa e la qualità della passivazione. Per aiutare a spiegare la relazione tra questi parametri e per identificare il contributo dei diversi meccanismi di ricombinazione sulla passivazione abbiamo utilizzato delle simulazioni.

Dai profili di drogaggio analizzati, viene riportata un'osservazione interessante. L'ossido chimico varia in spessore e densità a seconda della polarità e della resistività di base del wafer di silicio.

Il materiale ottenuto a valle del processo di ottimizzazione è stato applicato come contatto passivante e selettivo per gli elettroni in un prototipo di cella solare. A livello di dispositivo

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efficienze di conversione rispettivamente del 19.0% su wafer planari e del 20.1% su wafer testurizzati sono state raggiunte dimostrando la validità del nostro approccio. Densità di corrente di cortocircuito ( $J_{SC}$ ) relativamente elevate, 35 mA/cm<sup>2</sup> ottenute con wafers con superfici planari e di 40 mA/cm<sup>2</sup> per wafers con superfici strutturate indicano basse perdite ottiche e quindi evidenziano il potenziale del nostro strato come contatto passivante da applicare nella regione frontale di celle solari di nuova generazione. Inoltre, viene presentata la caratteristica benefica della variazione graduale dell'indice di rifrazione all'interno dello strato, che porta a una bassa riflettanza su un'ampia scala di lunghezze d'onda, simile a un doppio.

Un secondo approccio per raggiungere contatti passivanti e selettivi per gli elettroni che sia anche altamente trasparente è dimostrato dall'uso di un processo al plasma basato sui gas precursori come: PH<sub>3</sub>, SiF<sub>4</sub>, H<sub>2</sub> e Ar. L'effetto benefico del fluoro sulla passivazione senza bisogno di ulteriore idrogenazione è dimostrato, raggiungendo tensioni di circuito aperte implicite di 730 mV su superfici planari e 707 mV su superfici strutturate. L'implementazione di questi strati in primi prototipi e' risultata in promettenti efficienze del 19,5% su wafer testurizzati su un solo lato con valori di  $J_{SC}$  fino a 40 mA/cm<sup>2</sup>.

**Parole chiave:**

Energia solare, fotovoltaico, cristallino, silicio, cella solare, passivazione, elettrone, selettivo, contatto, ossido, SiO<sub>2</sub>, SiOX poly-Si, POLO, TOPCon, fase mista, efficienza, tensione a circuito aperto, PECVD, TEM, plasma, idrogeno, silano, fluoro, tetrafluoro, SiF<sub>4</sub>

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# List of abbreviations and symbols

AFM	atomic force microscopy
Al-BSF	aluminum back surface field (Al-BSF) cells
ARC	anti-reflection coating
<i>a</i> -Si	amorphous silicon
<i>a</i> -SiC(n)	phosphorus-doped amorphous SiC <sub>x</sub>
chem-SiO <sub>x</sub>	chemically grown SiO <sub>x</sub>
DSP	(mechanically) double-side-polished (wafers)
EDX	X-ray spectroscopy
EELS	electron energy loss spectroscopy
EQE	external quantum efficiency
ERFC	complementary error function
<i>FF</i>	fill factor
FGA	forming gas annealing
FZ	float-zone (wafers)
HAADF	high-angle annular dark field
HF	hydrofluoric acid
HNO <sub>3</sub>	nitric acid
HRTEM	high-resolution transmission electron microscopy
IBC	interdigitated back contacted
<i>iFF</i>	implied fill factor
IQE	internal quantum efficiency
<i>iV</i> <sub>OC</sub>	implied open-circuit voltage
<i>J</i> <sub>0</sub>	saturation current density
<i>J</i> - <i>V</i>	current-voltage measurement
LPCVD	low-pressure chemical vapor deposition
<i>μc</i> -Si	microcrystalline silicon
<i>μc</i> -Si:F	fluorinated microcrystalline silicon
mp-SiO <sub>x</sub> (n)	phosphorus-doped mixed-phase SiO <sub>x</sub>
<i>N</i> <sub>A</sub>	acceptor concentration
nc-Si(n)	phosphorus-doped nanocrystalline Si
<i>N</i> <sub>D</sub>	donor concentration
<i>N</i> <sub>dop</sub>	surface concentration
<i>N</i> <sub>eq</sub>	equilibrium concentration

## Contents

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$N_{\text{sat}}$	saturation concentration
PCD	photoconductance decay measurement
PECVD	plasma-enhanced chemical vapor deposition
PERC	passivated emitter and rear cells
PERL	passivated emitter, rear and locally-doped cells
PERT	passivated emitter, rear totally diffused cells
PESC	passivated emitter solar cells
$pFF$	pseudo fill factor
PSG	phosphosilicate glass
$\rho_c$	specific contact resistivity
$R_s$	series resistance
$R_{\text{SH}}$	sheet resistance
SE	spectroscopic ellipsometry
SHJ	silicon heterojunction solar cells
SIMS	secondary ion mass spectroscopy
SRH	Shockley-Read-Hall recombination
SRV	surface recombination velocity
STEM	scanning transmission electron microscopy
TCO	transparent conductive oxide
TEM	transmission electron microscopy
TF-Si	thin-film silicon solar cells
TLM	transfer length method
TOPCon	tunnel oxide passivated contacts
$V_{\text{OC}}$	open-circuit voltage

# 1 Introduction

In this PhD thesis, the development of a so-called passivating electron contact for wafer-based crystalline silicon solar cells is described. Such passivating contacts are formed to suppress charge-carrier recombination losses at the interface between the silicon absorber and the electrodes to increase the open-circuit voltage ( $V_{OC}$ ) and therefore the efficiency ( $\eta$ ) of the solar cell. To this end, the passivating contact is required to provide well-passivated interfaces with a high carrier selectivity while still maintaining efficient charge-carrier extraction. Additionally the contact is designed to sustain the high-temperature process steps used in industrial fabrication to be easily integrated into the manufacturing process.

More specifically, this work targeted front-side application where, in addition to passivation and current extraction, the optical transparency is important. For this reason, a novel mixed-phase silicon oxide layer was developed, optimized and characterized in detail.

## 1.1 Solar energy in context

The population of the world is increasing and the consumed energy per person is increasing as well due to improving welfare, particularly in the populous rapidly modernizing countries like India and China. Consequently, the global consumption of energy and the demand for electricity—met mainly by the use of fossil fuels and nuclear power—are growing. Both energy sources are problematic due to limited resources on planet earth and environmental drawbacks (carbon dioxide ( $CO_2$ ) emissions, radioactive waste, etc.). In the last decades, the reduction of  $CO_2$  emissions gained increasing political interest worldwide in an effort to stop the global warming that all of us are facing. The main human activity that emits  $CO_2$  is the combustion of fossil fuels like coal, natural gas or oil for the production of electricity, transportation or industrial processes [EPA 2018]. To reduce  $CO_2$  emissions, a change towards renewable energy sources is inevitable. By far the largest source of renewable energy is the sun with its 86 PW of solar radiation reaching the earth's surface; this is around 10'000 times the global power consumption [Hermann 2006, IEA 2014]. This radiation can be converted into heat, electricity (photovoltaic effect), biomass (photosynthesis), and potential energy

(storage of rain in dams). The photovoltaic effect has the advantage of generating electricity directly, which is the highest grade of energy since its conversion into other forms of energy is easy with comparatively few losses. Whereas in the 80's, photovoltaic (PV) devices were not cost competitive compared to classical carbon-based energy sources, in the last 36 years the module price (inflation adjusted) went down by 24% each time the cumulative production doubled (Figure 1.1), which led to a module price below 0.45 € per Watt peak (Wp) in 2016 [Philippis 2017]. A simple calculation for a module with a yield of 1300 kWh/kWp/year and a realistic 20-year lifetime results in a price for solar electricity of 1.7 €-cents per kWh; this calculation includes only the module price. For complete systems we have to take additional costs into account (mounting, inverter, ...). For a typical 10 kWp to 100 kWp rooftop system in Germany in 2016, a price of 1.27 €/Wp is reported leading to ~ 5 €-cents per kWh [Philippis 2017]. Thus, retail grid parity is reached (here with the example of Germany, but in many other countries as well) meaning that for end users the production of their own solar energy is cheaper than buying from an external company.

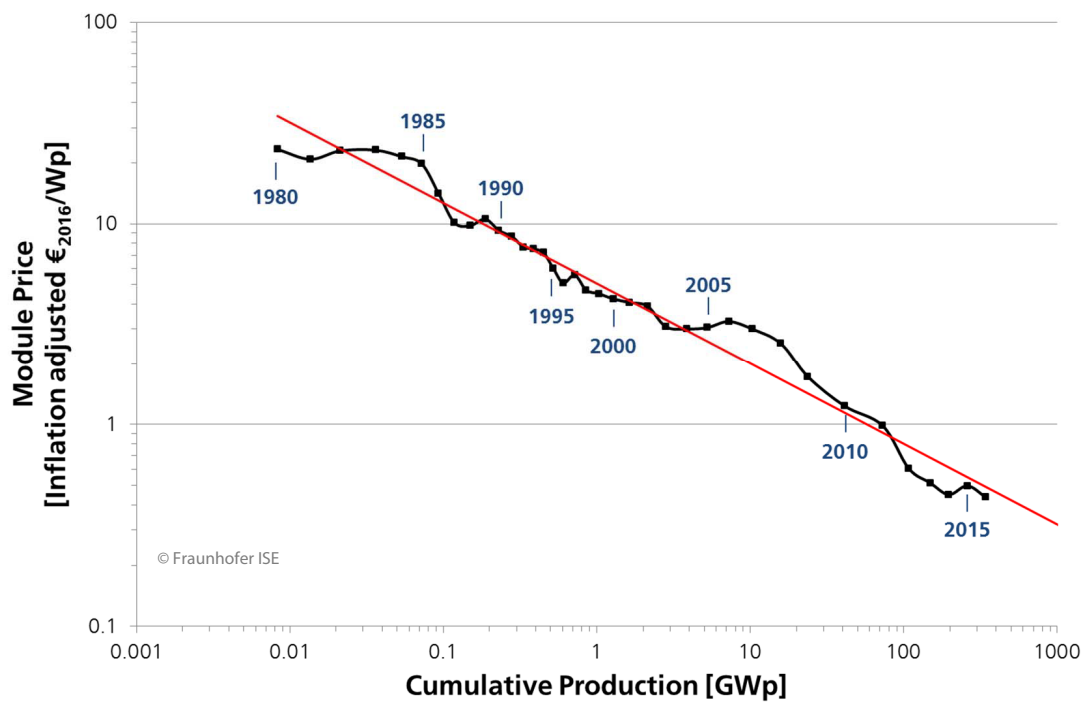


Figure 1.1 – The learning curve for the photovoltaic module price including all commercially available PV technologies as a function of the cumulative production [Philippis 2017].

## 1.2 Theoretical background

To understand the historical evolution and the working principle of solar cells, we review in this section the underlying semiconductor physics. In a photovoltaic device, light (photons)

is directly converted into an electric potential via the photovoltaic effect. In most cases, absorption takes place in a semiconductor with a bandgap  $E_g$ .

### 1.2.1 Generation in semiconductors

An incoming photon with an energy  $hc/\lambda = h\nu \geq E_g$  generates an electron-hole pair by exciting an electron from the valence band to the conduction band (see Figure 1.2). We differentiate between direct bandgap semiconductors—direct transition from the valence band to the conduction band (e.g. GaAs, CdTe, CIGS, ...)—and indirect bandgap semiconductors such as silicon where an indirect transition requires not only a photon, but also a phonon. The interaction with electromagnetic fields is generally described by the dielectric permittivity  $\epsilon(\lambda) = \epsilon_1(\lambda) + i\epsilon_2(\lambda)$  where  $\lambda$  is the wavelength of the incoming light. Alternatively, the refractive index is defined via the following formula:

$$n + ik = \sqrt{\epsilon} \quad (i) \quad \alpha = 4\pi k/\lambda \quad (ii) \quad (1.1)$$

The refractive index  $n$  is an important quantity to describe the reflection at interfaces, and the extinction coefficient  $k$  is directly related to the optical absorption coefficient  $\alpha$  [1/cm] by Equation 1.1.ii. In the law of Lambert and Beer, the absorption coefficient is used to describe the exponential decay of the light intensity along its path through an absorbing medium. In the case of absorption in a weakly-doped semiconductor, the exponential decay yields a relation for the generation  $G(x)$  of electron-hole pairs as a function of the spatial coordinate  $x$ :

$$G(x) = \alpha N_0 e^{-\alpha x} \quad [\text{cm}^{-3} \text{s}^{-1}] \quad (1.2)$$

Here,  $N_0$  is the incoming photon flux. Using the standardized global solar irradiation spectrum (AM1.5g) the generation rate in a silicon wafer exponentially decreases with depth from  $\sim 5 \cdot 10^{21} \text{cm}^{-3} \text{s}^{-1}$  to  $6 \cdot 10^{17} \text{cm}^{-3} \text{s}^{-1}$ . At temperatures above 0 K, carriers (electrons or holes) are also excited thermally. If the semiconductor is kept in the dark, they will eventually recombine. In the resulting thermal equilibrium, the generation rate  $G_{th}$  and the recombination rate  $R_{th}$  cancel each other out:

$$G_{th} = R_{th} \quad (i) \quad n_i^2 = n_0 p_0 \quad (ii) \quad (1.3)$$

Here,  $n_i$  is the intrinsic carrier density of the semiconductor, and  $n_0$  and  $p_0$  are the densities of electrons and holes, respectively. They can be expressed by:

$$n_0 = N_C e^{\frac{E_F - E_C}{kT}} \quad (i) \quad p_0 = N_V e^{\frac{E_V - E_F}{kT}} \quad (ii) \quad (1.4)$$

Here,  $E_F$  is the Fermi energy,  $k$  is the Boltzmann constant,  $T$  is the temperature,  $E_V$  and  $E_C$  are the energies of the valence band and of the conduction band, respectively, and  $N_V$  and  $N_C$  are the effective density of states in the valence band and in the conduction band, respectively.

## Chapter 1. Introduction

Under illumination, the generation of electron-hole pairs leads to an increase in the carrier densities:

$$\begin{aligned} n &\rightarrow n_0 + \Delta n & (i) \\ p &\rightarrow p_0 + \Delta p & (ii) \\ np &> n_i^2 & (iii) \end{aligned} \quad (1.5)$$

Therefore Equation 1.4 can be rewritten as:

$$\begin{aligned} n &= n_0 + \Delta n = N_C e^{\frac{E_{Fn} - E_C}{kT}} = n_0 e^{\frac{q\phi_n}{kT}} & (i) \\ p &= p_0 + \Delta p = N_V e^{\frac{E_V - E_{Fp}}{kT}} = p_0 e^{\frac{q\phi_p}{kT}} & (ii) \end{aligned} \quad (1.6)$$

where  $E_{Fn}$  and  $E_{Fp}$  are the *quasi-Fermi levels* and  $\phi_{n,p}$  represents their deviation from  $E_F$ . The splitting of these quasi-Fermi levels can be directly linked to an implied potential and thus the maximum possible voltage that the device is able to deliver:

$$iV = \phi_p - \phi_n = \frac{kT}{q} \ln \left( \frac{(n_0 + \Delta n)(p_0 + \Delta p)}{n_i^2} \right) \quad (1.7)$$

### 1.2.2 Recombination in the bulk of semiconductors

The inverse process of generation is called recombination which can be separated into three different processes: **radiative** (rad.), **Auger** and **Shockley-Read-Hall** (SRH) recombination as sketched in Figure 1.2:

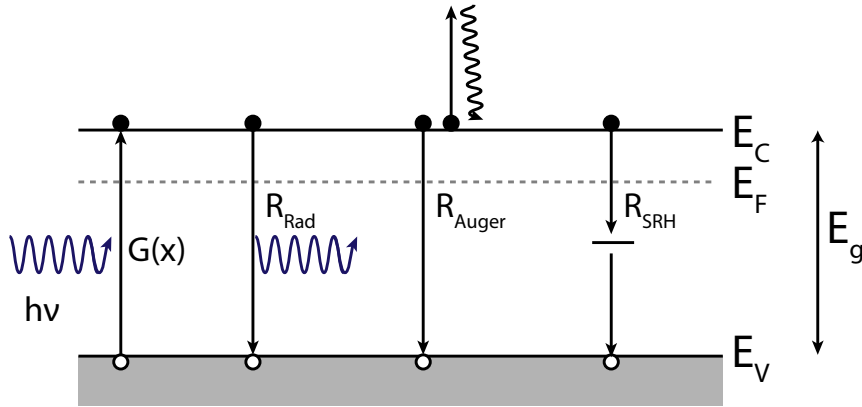


Figure 1.2 – Generation and recombination processes in a semiconductor. Adapted from [Geissbühler 2015].

- **Radiative** recombination is the exact inverse of generation: an electron falls from the conduction band to the valence band, generating a photon with the energy of the

bandgap. This recombination process is more probable for direct bandgap materials than indirect bandgap materials, as in the latter the transition has to be mediated by a phonon. The radiative recombination rate can be given by:

$$U_{\text{rad}} = B(np - n_i^2) \quad (1.8)$$

where B is a constant depending on the material [Green 1982].

- **Auger** recombination involves three particles. An electron recombines with a hole and the generated energy is transferred to another electron (or hole) near the conduction band (valence band) edge, which is subsequently excited into a higher (lower) energy level in the conduction (valence) band from which it thermalizes as shown in Figure 1.2. The recombination rate can be expressed by [De Wolf 2005]:

$$U_{\text{Auger}} = C_n(n^2p - n_0^2p_0) + C_p(np^2 - n_0p_0^2) \quad (1.9)$$

- **SRH** recombination refers to the recombination via defect states which lie deep within the energy bandgap. Recombination takes place when an electron and a hole get captured into the defect state. The recombination rate is given by [Sze 2001]:

$$U_{\text{SRH}} = \frac{v_{th}N_t(np - n_i^2)}{\frac{1}{\sigma_p}(n + n_1) + \frac{1}{\sigma_n}(p + p_1)} \quad \text{with } n_1 = n_i e^{\frac{E_T - E_F^i}{kT}} \text{ \& } p_1 = n_i e^{\frac{E_F^i - E_T}{kT}} \quad (1.10)$$

where  $\sigma_{n,p}$  are the capture cross sections of the defect,  $N_t$  is the defect density at the defect energy level  $E_t$ ,  $E_F^i$  is the intrinsic Fermi energy level and  $v_{th}$  is the thermal velocity.

The difference between the total recombination rate ( $R$ ) and the recombination rate in darkness and thermal equilibrium ( $R_{th}$ ) is called the *net recombination rate*  $U = R - R_{th}$ . We can define the *bulk lifetime*  $\tau_{\text{bulk}}$  for each carrier type reflecting the average times before they recombine:

$$\begin{aligned} \tau_n &\equiv \Delta n / U & (i) \\ \tau_p &\equiv \Delta p / U & (ii) \end{aligned} \quad (1.11)$$

Recombination rates are additive and the effective bulk lifetime can therefore be written as [Nelson 2003]:

$$\frac{1}{\tau_{\text{bulk}}} = \frac{1}{\tau_{\text{rad}}} + \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{SRH}}} \quad (1.12)$$

From this equation it is evident that the shortest lifetime dominates over the others and thus limits  $\tau_{\text{bulk}}$ .

### 1.2.3 Surface recombination

In addition to the recombinations in the bulk, we have to consider recombination processes taking place at the surface of the semiconductor. In the case of a direct Schottky contact to a metal (i.e. contact with a continuous density of states), both carrier types recombine directly. In the case of an insulator (including air), a broken symmetry of the semiconductor lattice leads to dangling bonds and therefore to recombination centers. The surface recombination rate is then given by:

$$U_S \equiv S \Delta n_{Surf} \quad (1.13)$$

Here,  $S$  is the surface recombination velocity and  $\Delta n_{Surf}$  is the excess carrier density at (near) the surface. Analogous to the SRH bulk recombination (Equation 1.10), the surface recombination rate can be expressed by:

$$U_{S,SRH} = \frac{v_{th} D_{it} (n_S p_S - n_i^2)}{\frac{1}{\sigma_p} (n_S + n_1) + \frac{1}{\sigma_n} (p_S + p_1)} \quad \text{with } n_1 = n_i e^{\frac{E_T - E_F^i}{kT}} \text{ \& } p_1 = n_i e^{\frac{E_F^i - E_T}{kT}} \quad (1.14)$$

Here,  $n_S$  and  $p_S$  are the carrier densities near the surface and  $D_{it}$  is the density of surface defects.

In covalent semiconductors such as  $c$ -Si, the surfaces are particularly recombination active. Therefore there are mainly two ways to avoid surface recombination [Cuevas 1996, Olibet 2007]:

- **Chemical passivation** of surface states means a reduction of the number of recombination sites (reduction of  $D_{it}$ ). This can be achieved e.g. by hydrogen atoms or by a thermal oxide that terminates silicon dangling bonds [Olibet 2007, Kerr 2002].
- **Reduction of the minority-carrier concentration** close to the surface (reduction of  $n_S$  or  $p_S$ , sometimes referred to as field-effect passivation). Here the number of recombination sites remains the same, but by reducing the concentration of minority carriers, the probability of a recombination at a certain defect is reduced. This can be achieved e.g. by introducing fixed charges or by a high-low junction (diffusion barrier) resulting in band bending in the surface vicinity [Cuevas 1996, Green 1982].

In the case of a strong band bending, an effective surface recombination velocity  $S_{eff}$  can be defined from Equation 1.13 at a distance  $d$  from the surface where the bands are still flat:

$$S_{eff} \equiv \frac{U_{x=d}}{\Delta n_{x=d}} \quad (1.15)$$

The position of  $d$  is the edge of the  $c$ -Si surface space charge region where the photogenerated excess-carrier densities are equal i.e.  $\Delta n_{x=d} = \Delta p_{x=d}$ .  $S_{eff}$  is typically between  $1 \cdot 10^5$  and

## 1.2. Theoretical background

$1 \cdot 10^7$  cm/s for a direct contact between silicon and a metal where  $S_{eff}$  is limited by the thermal velocity, down to  $< 10$  cm/s for a well-passivated silicon surface. For the case of identical very well-passivated front and rear surfaces (small  $S_{eff} < 100$  cm/s), the surface recombination can be taken into account by defining an effective carrier lifetime  $\tau_{eff}$ :

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surf}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{w} \quad (1.16)$$

Here,  $w$  is the wafer thickness.

### 1.2.4 Main solar cell parameters

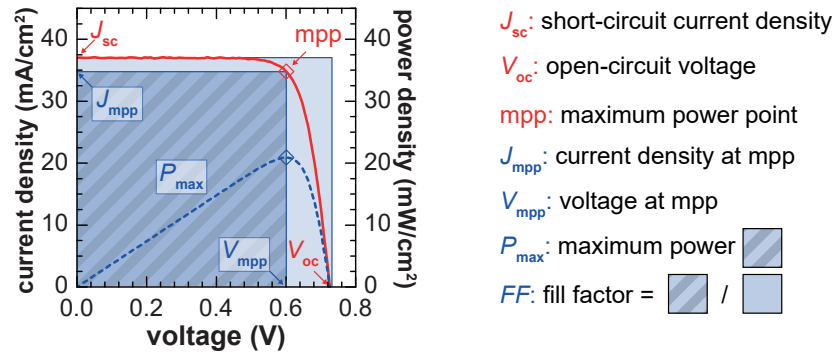


Figure 1.3 – Typical  $J$ - $V$  characteristic of a solar cell under illumination including the relevant parameters (Adapted from [Seif 2015a]).

For a working solar cell, the generation of electron-hole pairs alone is not sufficient; the resulting carriers have to be extracted as well before they recombine. A simple and ideal model describes a solar cell as a diode using the equation for the current density as a function of the voltage:

$$J(V) = J_L - J_0 \left( e^{\frac{eV}{kT}} - 1 \right) \quad (1.17)$$

where  $J_L$  is the photogenerated current that is produced by illumination. The quantity  $J_0$  is called the saturation current density,  $e$  is the elementary charge,  $V$  is the applied voltage,  $k$  is the Boltzmann constant, and  $T$  is the absolute temperature.

Out of this the four main parameters describing the performance of a solar cell can be extracted as sketched in Figure 1.3:

- **Short-circuit current density** ( $J_{sc}$ ) is equal to  $J_L$  in short-circuit conditions ( $V = 0$ ). It is a measure of the maximal current generated in the solar cell and is therefore mainly limited by the number of incoming photons reaching the absorber. This can be reduced

by reflectance or by parasitic absorption in the different layers, mainly at the front of the solar cell.

- **Open-circuit voltage**  $V_{OC}$  is the maximal voltage available from a solar cell when no current is extracted ( $J = 0$ ). At this condition, the voltage is limited only by recombination processes. Therefore, lowering the recombination leads directly to an increase in  $V_{OC}$  which is thus often used as a measure for the passivation quality.
- **Fill factor** ( $FF$ ) defines the squareness of a  $J$ - $V$  curve and is defined as:

$$FF = \frac{V_{mpp} J_{mpp}}{V_{OC} J_{SC}} \quad (1.18)$$

where mpp stands for the maximal-power-point condition, thus the voltage and current at which the extracted power ( $P = V \cdot J$ ) is maximal. The  $FF$  is influenced mainly by recombinations and by the series and shunt resistance. A simple approximation of the influence of the series resistance  $R_s$  on the  $FF$  is given by [Green 1982] via the normalized series resistance  $r_s$ :

$$FF_s = FF_0(1 - 1.1r_s) + \frac{r_s^2}{5.4} \quad \text{with} \quad r_s = R_s \frac{J_{SC}}{V_{OC}} \quad (1.19)$$

where  $FF_0$  is the ideal  $FF$  in absence of series resistance.

- **Energy conversion efficiency** ( $\eta$ ) is defined as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{OC} J_{SC} FF}{P_{in}} \quad (1.20)$$

where  $P_{out}$  is the extracted power density at mpp and  $P_{in}$  is the incident power of the light calibrated to 1000 W/m<sup>2</sup> (AM1.5g).

### 1.3 Photovoltaic technologies

Figure 1.4 shows the record conversion efficiencies of photovoltaic devices over the past 40 years. Efficiencies as high as 46% were obtained with a four-junction solar cell based on III-V materials under a concentration of 508 suns [Green 2017]. Without concentration, the highest efficiency of 38.8% is reached with a similar structure. However, due to their complex and expensive processing, such technologies are mainly used for space applications or in combination with a concentrator.

For terrestrial application, silicon-wafer-based single-junction solar cells are still the major technology with a market share of over 90% [IEA 2016]. For silicon, the highest non-concentrated efficiency was obtained with a 200- $\mu$ m-thick rear-contacted heterojunction solar cell with an impressive 26.7% [Yoshikawa 2017, Green 2017] which is less than 3%<sub>abs</sub> below the theoretical limit of 29.4% for a 110- $\mu$ m-thick cell [Richter 2013]. Recently a

### 1.3. Photovoltaic technologies

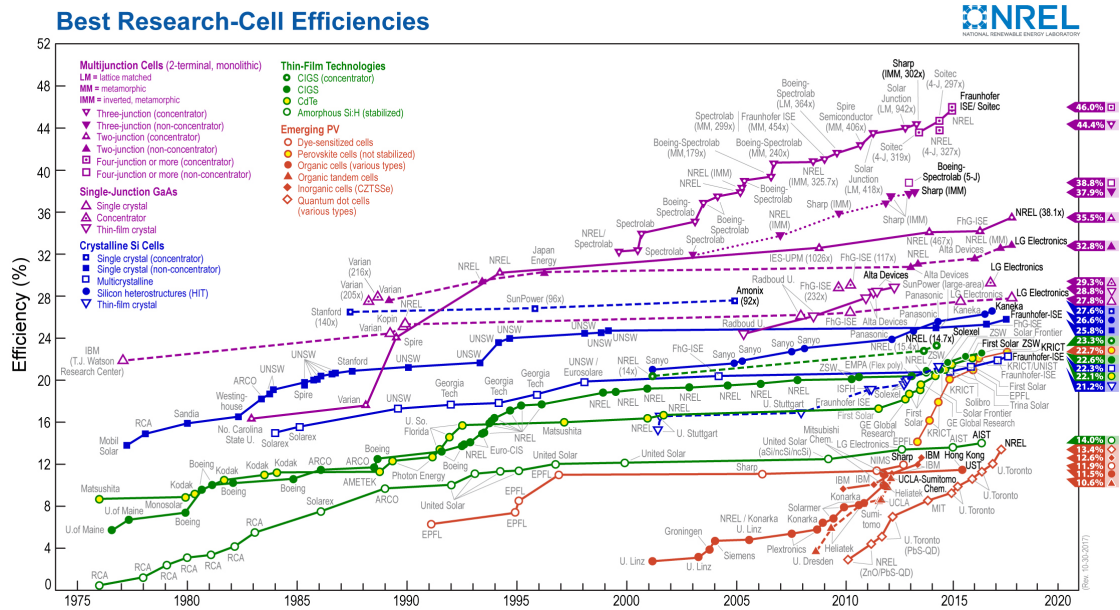


Figure 1.4 – Record efficiencies for different photovoltaic technologies over the last 50 years. This plot is courtesy of the National Renewable Energy Laboratory, Golden, CO, USA [NREL 2018].

rear-contacted cell with oxide-based passivating contacts reached 26.1% [ISFH 2018]. The best both-side-contacted device—one side an oxide-based passivating contact and the other a traditional diffused contact—reached 25.8% efficiency [Richter 2017].

Before the recent boost with oxide-based passivating contacts [Feldmann 2014c], most solar cells were contacted directly with metals in geometries of varying sophistication. A relatively simple design was the Passivated Emitter Solar Cell (PESC) of the early 80's whose front surface was partially passivated. In the late 80's the same concept was refined by localizing the area of the metal contacts at the rear to small areas in Passivated Emitter and Rear Cells (PERC). A further refinement was introduced by restricting the highly-doped regions to the areas underneath the contacts in the Passivated Emitter, Rear Locally-diffused (PERL) and the Passivated Emitter, Rear Totally-diffused (PERT) solar cells. In industry, the most common cell type is essentially a PESC cell, slightly modified by the introduction of a back surface field (BSF). At the time of writing, it represents about 65% of industrial production: ca. 30% are produced with PERC technology. The remaining 5% are silicon heterojunction cells (SHJ).

Another group are thin-film solar cells which have the advantage that they use less material. The most industrially common are CIGS and CdTe; cells on the basis of these materials reach efficiencies of 22.6% and 22.1%, respectively. Recently, perovskites have gained a lot of interest with a record efficiency of 22.7% (not stabilized) even though their high sensitivity to humidity and oxygen make the commercialization of this material challenging [De Wolf 2014, Löper 2014].

Additionally, thin-film silicon (TF-Si) solar cells based on amorphous silicon (*a*-Si) or microcrystalline silicon ( $\mu$ c-Si) mostly in a multi-junction configuration reached efficiencies of 14% [Green 2017, Sai 2015]. Despite the low cell and module production cost for this technology, they continuously lost market share because of their low efficiencies which require more surface area and a higher balance of system (BOS) cost. Nevertheless, some of the ideas for new deposition regimes used for passivating contacts are based on work done by our colleagues and ourselves on TF-Si solar cells and are explained more in detail in appendix A.

### 1.3.1 Aluminum back surface field (Al-BSF) cells

The photovoltaic industry was dominated for years by the Al-BSF technology due to its simplicity of fabrication [Glunz 2012]. The structure is sketched in Figure 1.5a using either a mono-or multicrystalline silicon p-type wafer with a resistivity of ca.  $1 \Omega \text{cm}$  (Acceptor density  $N_A \approx 1 \cdot 10^{16} \text{cm}^{-3}$ ). To scatter the incoming light and increase the path way of photons inside the absorber, the front side of the solar cell is textured to a depth of a few micrometers either by an alkaline wet etching in the case of mono-crystalline wafers or by acidic etching in the case of multi-crystalline wafers. Next, the wafers are annealed at  $800^\circ\text{C}$  to  $900^\circ\text{C}$  in a tube furnace in an atmosphere of phosphorus oxychloride ( $\text{POCl}_3$ ) and oxygen  $\text{O}_2$ . For this, nitrogen as the carrier gas is flowing through a bubbler with liquid  $\text{POCl}_3$  before it is mixed with oxygen ( $\text{O}_2$ ) and conducted directly to the quartz tube [Neuhaus 2007]. Phosphorous oxide  $\text{P}_2\text{O}_5$  is deposited on the wafers and forms a two-layer stack of a phosphosilicate glass (PSG) and a silicon oxide ( $\text{SiO}_2$ ) as well as a diffused region within the wafer forming the selective electron collector [Werner 2017]. The released  $\text{Cl}_2$  removes metal impurities while the diffused phosphorus reduces the concentration of impurities by gettering, both of which improve the quality of the bulk material [Neuhaus 2007]. The diffused region typically has a donor concentration  $N_D$  above  $1 \cdot 10^{20} \text{cm}^{-3}$  at the wafer surface which falls steeply below  $N_A$  within  $1 \mu\text{m}$ . Typically, the diffused region has a sheet resistance of around  $75 \Omega/\square$  [Glunz 2012]. The surface concentration and the depth of the diffusion profile can be optimized by a two-step annealing in which the  $\text{POCl}_3$  supply is switched off during the second phase for a drive-in diffusion [Dastgheib-Shirazi 2013]. After removing the PSG/ $\text{SiO}_2$  layer stack by hydrofluoric acid (HF), a silicon-rich silicon nitride  $\text{SiN}_x$  layer with a refractive index of  $\approx 2.1$  [Bustarret 1988] and thickness of  $\approx 75 \text{nm}$  is deposited by plasma-enhanced chemical vapor deposition (PECVD) to form an anti-reflection coating (ARC). At the rear an aluminum-based metallic paste is screen-printed on the full area and dried prior to the screen-printing of the silver front grid. Finally, both contacts are co-fired (a thermal treatment at around  $800^\circ\text{C}$  for a few seconds with fast heating and cooling). During firing, the aluminum back surface field is formed at the rear, while at the front, the silver paste locally penetrates the silicon nitride to contact the front n-type diffusion [Ballif 2003]. At the same time, hydrogen is released from the  $\text{SiN}_x$  layer to passivate defects at the wafer surface and in the bulk.

The enormous success of this structure relies on several main drivers: the simplicity of the production, a high tolerance against variations in wafer quality and perhaps most

important—the main structure elements or process sequences are not severely protected by patents. On the other side, the main drawbacks are the direct metal-semiconductor interfaces at the front and the rear that lead to recombination losses. The diffused region at the front as well as the Al-BSF at the rear reduces the recombination by the reduced concentration of minority charge carriers, but the devices are still limited by recombination losses. There is little margin to further increase the doping levels since this would introduce more Auger recombination. The saturation current density  $J_0$  at the front and the rear is in the range of 100–1000 fA/cm<sup>2</sup> limiting the  $V_{OC}$  to around 660 mV [Cuevas 2013].

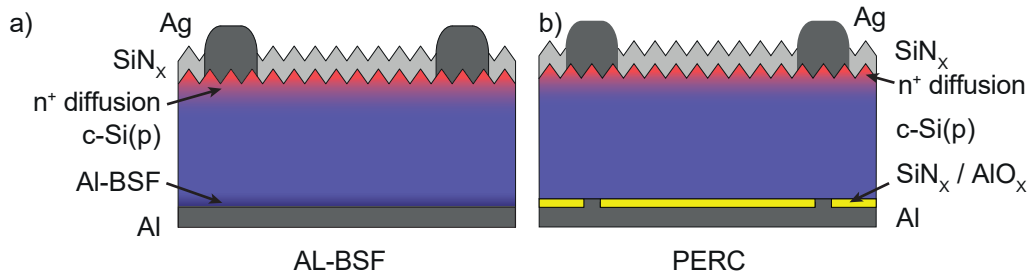


Figure 1.5 – Sketch of a cross section of an (a) aluminum back surface field solar cell in comparison with (b) a PERC cell. Adapted from [Seif 2015a].

### 1.3.2 Passivated emitter and rear cell (PERC)

To overcome the discussed recombination losses, the structure was modified as illustrated in Figure 1.5b. At the rear side of the cell (hole contact) a passivation layer is introduced and opened only locally for the highly recombinative metal contact. This adds several steps to the fabrication process. Thermally grown silicon oxide is a common passivation layer, but  $\text{SiN}_x$  is used very successfully at the front whereas  $\text{Al}_2\text{O}_3$  is increasingly used at the rear since its negative resident charge provides a field effect passivation for the p-type bulk. The local openings at the rear still have a direct metal/wafer interface that is recombination active (can be improved by a locally formed BSF) but due to the reduced surface the emitter saturation current density at the rear can be reduced to 35–100 fA/cm<sup>2</sup> [Deng 2015] which makes the front the limiting factor to a maximum  $V_{OC}$  of 680 mV [Cuevas 2013].

### 1.3.3 Oxide-based poly-silicon contacts

In 2014, a full-area passivating electron-selective contact was demonstrated by [Feldmann 2014a] reaching high efficiency with the structure sketched in Figure 1.6. The contact is based on an ultra-thin chemically grown silicon oxide layer (1.4 nm) covered by an n-doped polysilicon layer before the stack is annealed at temperatures above 600 °C. Together with a boron-diffused emitter at the front side, an impressive conversion efficiency of 23.0% was demonstrated with a  $V_{OC}$  of 698 mV and a fill factor of 81.1% [Feldmann 2014a]. This confirmed that excellent passivation together with a low series resistance was possible with

this contact. Since no contacts have to be opened, the fabrication of this contact design is simple and, due to the full-area coverage of the interface by the silicon oxide, passivation is also improved. The transport was explained first by tunneling giving this contact the name tunnel oxide passivated contacts (TOPCon). In recent years the exact transport mechanism has been discussed widely in several publications, and therefore contact structures based on the same design can be found under POLO (polycrystalline on oxide) or just poly-silicon (poly-Si) contacts. Since the work we present in this thesis is based on this contact structure, a more detailed description and the current state of the art can be found in section 1.3.5.

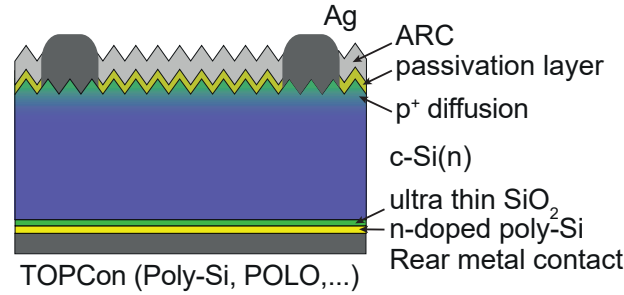


Figure 1.6 – Sketch of a cross section of a cell with a silicon-oxide-based rear contact, here as an example together with a boron-diffused front. Adapted from [Seif 2015a].

### 1.3.4 Silicon heterojunction solar cell

In contrast to the solar cells presented so far, silicon heterojunction (SHJ) solar cells do not rely on the diffusion of dopants to the wafer to form a  $p$ - $n$ -junction. SHJ solar cells are based on intrinsic and doped  $a$ -Si layers as sketched in Figure 1.7. But similar to the TOPCon device, the passivation with  $a$ -Si is on the full area without local openings and the current flow is dominated by the transport through the thin  $a$ -Si layer. The fabrication has no need of high-temperature processes and is extremely efficient and straight forward. The metallization is done by a transparent conductive oxide (TCO) layer since the lateral conductivity within the doped  $a$ -Si is too low to transport the carriers to the fingers. Thanks to good passivation of  $a$ -Si, maximal voltages of 769 mV were predicted [Tiedje 1984] for a 100- $\mu$ m-thick wafer. However, the gain in surface passivation is achieved at the expense of the current output causing a lower  $J_{SC}$  [Holman 2012]. Comparing the SHJ in Figure 1.7 to the PERC in Figure 1.5b, it is evident that, for PERC cells, the metallic fingers at the front that directly contact the absorber through local openings enable excellent transport while the highly transparent dielectric layers between the contacts give good light incoupling, but they suffer in passivation. SHJ cells, in contrast, rely on transport through the  $a$ -Si layers and TCO. These layers lead to parasitic absorption and challenges in carrier transport. Nevertheless, the current world record for silicon solar cells is hold by a SHJ device with the interdigitated back-contacted (IBC) design reaching 26.7% [Green 2017, Yoshikawa 2017].

A more detailed introduction to SHJ solar cells can be found in [De Wolf 2012].

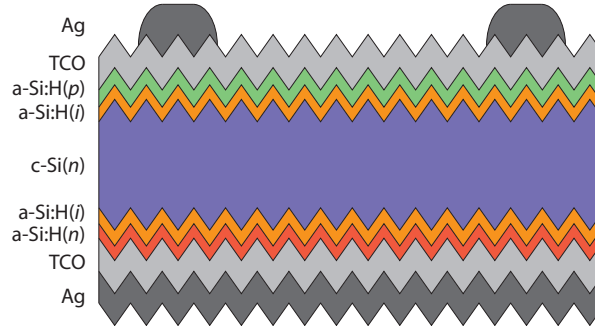


Figure 1.7 – Sketch of a cross section of a SHJ cell. Adapted from [De Wolf 2012].

### 1.3.5 State of the art

Approaches to passivate silicon wafers with a thin silicon oxide layer capped with doped poly-Si were pioneered in the 1980s [Gan 1990, Kwark 1984, Yablonovitch 1985]. Instead of using pure poly-Si layers, semi-insulating poly-Si (SIPOS) alloyed with oxygen was used, obtaining impressive passivation, but the films were too resistive for efficient extraction of current from solar cells [Kwark 1984, Yablonovitch 1985, Matsushita 1981]. In 2014 this approach was brought back first by [Feldmann 2014a] reaching high conversion efficiencies using an ultra-thin chemically grown oxide (chem-SiO<sub>x</sub>) and in-situ-doped *a*-Si deposited by PECVD. Since then, impressive solar cell results have been demonstrated using a similar approach, mainly on the rear side for both-sided-contacted solar cells and interdigitated back contacted (IBC) devices without alloying with oxygen [Feldmann 2016, Römer 2014, Tao 2015, Young 2014, Nogay 2017, Richter 2017, Krügener 2017]. All these structures have in common that a highly-doped surface region is formed within the wafer by the in-diffusion of dopants from the deposited layer during a thermal annealing step. This highly-doped surface region supports the charge-carrier selectivity of the contact [Brendel 2016]. Additionally, most structures benefit from a hydrogenation step, which reduces the electronic defect density at the wafer/chem-SiO<sub>x</sub> interface or in the layer stack [Stesmans 2000]. In 2015, a world-record efficiency for both-side-contacted solar cells (25.1%, [Glunz 2015]) was achieved using a boron-diffused front with an n-type TOPCon contact at the rear, which has been since then further improved to 25.8% [Richter 2017, Green 2018]. Recently an even higher efficiency was reported in IBC design reaching 26.1% ([ISFH 2018]), which is the current world record for p-type wafer-based silicon solar cells.

Though all of these contacts are based on a thin silicon oxide layer covered by a poly-Si layer, a broad variation of process parameters is reported. The influence of the interface oxide was investigated in detail for several different thicknesses and growth techniques. Chemically

grown oxides that self-saturate at a certain thickness dependent on temperature and chemical solution are most commonly used [Yan 2015, Upadhyaya 2016, Moldovan 2014, Moldovan 2015, Nemeth 2014]. The use of ozone for the growth of oxides has been tested and characterized [Moldovan 2014, Moldovan 2015, Zacharias 1999, Richter 2017, Kern 1990]. Thermally grown oxides have also been investigated [Römer 2015, Römer 2014, Rienäcker 2017]. For the latter, control of the desired remaining thickness is more difficult. Due to the variation of interfacial oxides used, the optimal annealing temperatures were also different, from 800 °C up to temperatures above 1000 °C. (The higher temperatures apply mainly to the thermally grown oxides.) The annealing temperatures and the type of oxides define the transport mechanism through the oxide. There are mainly two mechanisms that are discussed:

- **The tunneling model** describes transport through the thin layer by tunneling [Steinkemper 2015, Feldmann 2018, de Graaff 1979, Eltoukhy 1982], assuming that the oxide remains intact over the full area.
- **The pinhole model** postulates transport by perturbations in the thin oxide leading to pinholes and direct contact between the wafer and the poly-Si layer above [Peibst 2014, Peibst 2016, Wietler 2017, Gan 1990, Hamel 1992].

The pinhole model was proposed mainly for thicker oxides (>2 nm) and higher annealing temperatures (>900 °C) and supported by transmission electron micrographs showing the pinhole formation. The tunneling model better explains the characteristics of thinner oxides and lower annealing temperatures. Recently [Feldmann 2018] distinguished the transport mechanisms by temperature-dependent  $J$ - $V$  measurements. Whereas intact oxide barriers lead to an exponential increase in contact resistance (tunneling model) with decreasing temperature, oxide barriers that are slightly ruptured show a linear ohmic decrease (pinhole model).

So far, this contact has been introduced as a planar rear contact to update the PERC cell. Note, however, that this requires a p-type poly-Si contact, which is harder to achieve than the n-type poly-Si that is used with a boron-diffused front. The application on the front side has only recently become a focus of research. Whereas the structure of a passivating oxide-based contact on both sides was already proposed by [Yablonovitch 1985], working devices were demonstrated just in the last years on the lab scale on planar surfaces [Feldmann 2017, Römer 2014]. Recently single-side-textured devices were presented by [Peibst 2017, Ingenito 2018b] with passivating contacts on both sides. The lower passivation quality on textured surfaces, mainly for p-type contacts, seems to be related to a lower passivation quality of SiO<sub>x</sub> on silicon <111> surfaces [Larionova 2017].

In summary, in the last years, selective passivating contacts based on silicon oxide have shown their potential on the planar rear side of solar cells with impressive efficiencies. The next step with selective passivating contacts on both sides presents opportunities for additional research.

## 1.4 Objectives and structure of this thesis

The personal motivation for this thesis is to contribute to a change to greener electricity generation in the future whereas the scientific motivation is to gain a better understanding of the material properties of thin films based on silicon and silicon oxide and the parameters defining their growth, as well as the underlying principles of passivation or current transport through such layers.

### 1.4.1 Approach of a mixed-phase silicon – silicon oxide material

In section 1.3.3 the approach of passivating contacts based on an ultra-thin silicon oxide was introduced. This contact structure showed the potential to reach very low emitter saturation current densities below  $10 \text{ fA/cm}^2$  and therefore the front becomes the efficiency-limiting element [Glunz 2015]. Consequently, in order to further increase the solar cell efficiency, carrier-selective passivating contacts are also needed at the front side. While requirements for a passivating front contact are similar to these for the back contact in terms of passivation behavior, carrier selectivity and electrical transport, the front layer system also has to be **optically highly transparent in the visible to avoid any parasitic absorption losses**. This can be achieved with thin and highly crystalline silicon layers since the absorption coefficient of crystalline silicon in the visible is much lower than that of amorphous silicon. Full crystallization of thin silicon layers can be reached by prolonged thermal annealing [Zacharias 2000]. This might, however, lead to deteriorated surface passivation as the interfacial oxide (called chem-SiO<sub>x</sub> hereafter) layer ruptures [Feldmann 2014b, Wolstenholme 1987, Moldovan 2014]. Alternatively, thicker SiO<sub>x</sub> buffer layers can be used [Gan 1990, Römer 2014], but this approach requires a “SiO<sub>x</sub> break up” step at 1050 °C which might degrade surface passivation or alter the doping profile in an unwanted way.

To overcome this limitation we propose to use the strength of parallel-plate PECVD, which is an industrial technique, not used for such a purpose. **The versatility of this tool enables us to nucleate silicon crystallites at the initial stage of the PECVD deposition** and grow the silicon layer in a nanocrystalline state, such that moderate temperatures (700–900 °C) are sufficient to achieve high crystallization. To further decrease optical absorption we introduce a wide-bandgap material, namely silicon oxide, as a matrix around the silicon crystallites, replacing the amorphous silicon phase. This mixed-phase of nanocrystalline silicon embedded in silicon oxide (mp-SiO<sub>x</sub>) gives the opportunity to tune the refractive index while the silicon crystallites ensure a good vertical conductivity [Cuony 2010]. Furthermore, the additional deposited silicon oxide phase can enhance surface passivation by supporting the thin chemical oxide and preventing it from breaking up. To ensure a good electron-selective contact to the metallization, additionally a highly-doped nanocrystalline silicon layer (nc-Si(n)) covers the oxide-rich layer. The resulting bilayer (or trilayer, including the interfacial oxide) after the thermal treatment leading to the in-diffused region within the wafer is

sketched in Figure 1.8 together with the resulting band diagram simulated by AFORS HET [Varache 2015].

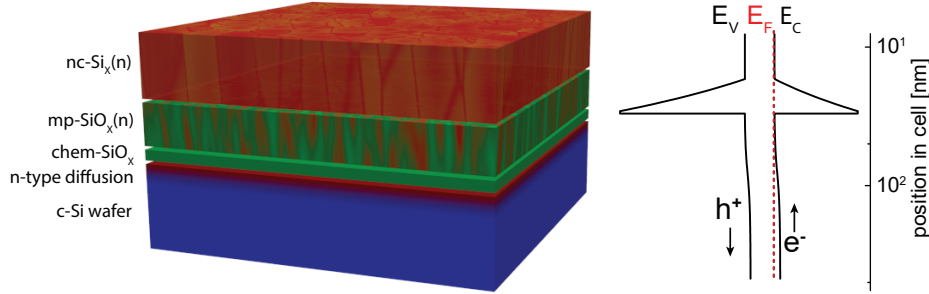


Figure 1.8 – Sketch of the targeted bilayer structure after the thermal treatment including the phosphorus-diffused region together with the resulting band diagram with logarithmic depth scale simulated by AFORS HET [Varache 2015].

### 1.4.2 Structure of this thesis

The thesis contains the following chapters:

- **Chapter 2:** Experimental details on the fabrication processes as well as the characterization techniques are given. For each chapter to stand alone, the basic experimental information is given in each chapter as well.
- **Chapter 3:** The structure and the mixed-phase nature of the proposed chem-SiO<sub>x</sub>mp-SiO<sub>x</sub>(n)/nc-Si(n) stack are analyzed in detail by Raman spectroscopy as well as by transmission electron micrographs in the as-deposited state and during the thermal treatment.
- **Chapter 4:** The passivation quality and the influence of the annealing temperature are reported on n-type and on p-type wafers. Additionally, the electrical properties are reported analyzing the current flow through the layer stack.
- **Chapter 5:** The influence of the phosphorus concentration in the deposited layer stack on passivation and electrical contact is described together with the influence of sputtered indium tin oxide on the passivation quality. Finally, a first proof-of-concept device is presented.
- **Chapter 6:** The optical properties, measured by spectroscopic ellipsometry, are reported. Simulations using these reproduce measured currents and reflectances at the cell level, and the optical losses within the single layers are quantified by a series of layer thicknesses. A way to control the doping profile within the wafer is introduced, and losses appearing during the cell fabrication are analyzed. Finally the contact is transferred to textured surfaces and integrated into textured devices.

- **Chapter 7:** A second approach to reach highly transparent electron-selective passivating contacts is demonstrated by the use of a plasma regime based on the precursor gases  $\text{PH}_3$ ,  $\text{SiF}_4$ ,  $\text{H}_2$ , and Ar. Impressive passivation without a hydrogenation process is reported on planar as well as on textured surfaces together with first proof-of-concept solar cell.
- **Chapter 8:** Each chapter is summarized together with an outlook.

### 1.4.3 Contribution of this thesis to the research field

One of the main contributions of this work is the development of a novel approach to form a mixed-phase silicon oxide layer that is used to advance the field of carrier-selective passivating contacts. The deposition of a  $\text{SiO}_x$  layer with high hydrogen dilution leads to vertically oriented silicon filaments in an oxide matrix, rendering the films transparent and conductive in the vertical direction. How this structure changes under different thermal budgets in terms of crystallization and atomic distribution was not previously investigated.

The passivation quality of this structure and the beneficial effect of additional oxygen during PECVD, which suppresses the formation of pinholes in the interfacial oxide layer at higher temperature, are analyzed. The influence of the phosphorus doping concentration on passivation is analyzed and simulations are used to separate the recombination behavior into the contributions from different mechanisms.

First proof-of-concept cells including this novel layer demonstrate the concept as an electron-selective passivating contact at the device level. Promisingly high currents on planar as well as on textured surfaces with low parasitic absorption indicate the potential as a front contact in next-generation solar cells. Additionally the beneficial feature of the smooth index change at the mp- $\text{SiO}_x(\text{n})$ / nc-Si(n) interface is presented leading to a low reflectance over a broad wavelength range, similar to a built-in anti-reflection coating.

A second approach to reaching highly transparent electron-selective passivating contacts is demonstrated by the use of a plasma regime based on the precursor gases  $\text{PH}_3$ ,  $\text{SiF}_4$ ,  $\text{H}_2$ , and Ar. The beneficial effect of fluorine in terms of passivation on planar as well as on textured surfaces without the need of additional hydrogenation processes is reported and the resulting layers are implemented in first proof-of-concept working devices.

The work presented in this thesis led to several publications as a first author [Stuckelberger 2015, Stuckelberger 2016a, Stuckelberger 2016b, Stuckelberger 2018], as co-first author [Mack 2018]<sup>1</sup>, and as co-author [Nogay 2016b, Nogay 2017, Ingenito 2018b, Wyss 2018, Mikulik 2018].

Additionally a patent evolved based on the work on the mixed-phase silicon oxide layer [Stuckelberger 2017].

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<sup>1</sup>I. Mack and J. Stuckelberger contributed equally to this work



## 2 Experimental processes, equipment and characterization techniques

In this chapter, the fabrication tools and characterization techniques used for this study are explained in detail. Many processes and systems were described earlier in great detail and we refer to the literature for them. Several process steps are performed in close collaboration and in the laboratory of the Swiss Center for Electronics and Microtechnology (CSEM).

### 2.1 Processes and systems

For the approach described in this study temperatures up to 950 °C were used. At such temperatures, elements are very mobile and likely to diffuse into silicon. Therefore avoiding any contamination during the processes was an essential point. For this reason, different cleanliness states were introduced and every system, tweezer, box etc. was dedicated to a certain position in the overall process sequence.

#### 2.1.1 Wafer preparation and growth of chem-SiO<sub>x</sub>

To start in a very clean state, the used wafers are undergoing an RCA cleaning that consists of several steps in chemical baths to remove organic or metallic residues and particles [Kern 1990, Itano 1993, Kern 1993]. The solutions oxidize and etch the wafer surface to remove particles without changing the surface smoothness. Between each every chemical step the wafers were thoroughly rinsed in deionized water. At the end of the cleaning process, a chemical oxide (henceforth referred to as "chem-SiO<sub>x</sub>") is grown by immersion into 80 °C hot HNO<sub>3</sub> solution (69 wt.-%) for 10 min [Asuha 2003, Grant 2009], leading to a thickness of ~ 1.2 nm depending on the wafer doping and resistivity (more information in section 6.4). Since the wafer is further oxidizing in ambient air, the time between the growth of the chem-SiO<sub>x</sub> and the following plasma-enhanced chemical vapor deposition (PECVD) should be kept short.

### 2.1.2 Deposition of silicon-based contact layers by PECVD

The silicon-based layers on top of the chem-SiO<sub>x</sub> are grown by PECVD with a substrate temperature of 200 °C. A dual-Plasma Box chamber Kai-M reactor described in detail in [Bugnon 2013] is used to create a plasma between two electrodes using a frequency of 40.68 MHz. The plasma decomposes the precursor gases into radicals for the layer growth. The main precursor gases are silane (SiH<sub>4</sub>) and hydrogen (H<sub>2</sub>). Phosphine (PH<sub>3</sub>, 2 vol.-% diluted in H<sub>2</sub>) is added for phosphorous-doped n-type layers. Carbon dioxide (CO<sub>2</sub>) is used to incorporate oxygen in order to grow SiO<sub>x</sub>. Alternatively to SiH<sub>4</sub>, silicon tetrafluoride (SiF<sub>4</sub>) is used as precursor gas for the results presented in chapter 7 and appendix A. Due to the stronger Si-F bonding in the SiF<sub>4</sub> molecule compared to Si-H in SiH<sub>4</sub>, argon (Ar) is added to decompose the SiF<sub>4</sub> molecule and to support ignition and stabilization of the plasma. Using such a plasma, containing SiF<sub>4</sub> and H<sub>2</sub>, it was reported that HF forms which foster crystalline growth [Dornstetter 2014a, Hänni 2014], but meanwhile it is also quite aggressive and a pre-coating of the chamber walls is recommended.

### 2.1.3 High temperature annealing

After PECVD, an annealing at temperatures between 800–950 °C is performed in nitrogen atmosphere. Whereas first tests were done wafer by wafer in a rapid thermal processing (RTP) system from Jetfirst (results not shown), a tube furnace (Tempress) became available at CSEM at a later stage. It uses slower heating ramps (10 °C/min) and slower cooling ramps of 2–4 °C/min.

For the fluorinated contacts, a tube furnace named PEO is used with similar ramps as in the Tempress tube but using an argon atmosphere.

### 2.1.4 Hydrogenation

Hydrogen is used after the high temperature step to passivate defects at the wafer/chem-SiO<sub>x</sub> interface as well as within the layer [Pearton 1992]. Two approaches are used:

- **Forming gas anneal (FGA):** The RTP system is used for annealing at 500 °C for 30 min in forming gas (4% H<sub>2</sub> in N<sub>2</sub>) atmosphere. This process provides molecular hydrogen which diffuses into the layer and to the interface to passivate dangling bonds.
- **Hydrogenation by SiN<sub>x</sub> :** Around 80 nm PECVD deposited SiN<sub>x</sub> is grown on both sides of the wafer at 250 °C using 81 MHz with SiH<sub>4</sub>, NH<sub>3</sub> as precursor gases in an in-house built system. The deposition is followed by a hotplate-annealing for 30 min at 450 °C in air to release atomic hydrogen from the SiN<sub>x</sub> to the layers below. Since SiN<sub>x</sub> is an insulator, the layer needs to be stripped afterwards. Usually, a 12 min etch in hydrofluoric acid (5 vol.-%) is used, alternatively an etch in boiling H<sub>3</sub>PO<sub>4</sub> (180 °C) is less aggressive against silicon and especially silicon oxide [Liu 2007]. For the latter one,

an etching time of 30 min was sufficient to fully remove the  $\text{SiN}_x$  layer. An over-etch at parts of the wafer surface cannot be avoided by this process since the  $\text{SiN}_x$  deposition is inhomogeneous and the  $\text{SiN}_x$  needs to be fully removed everywhere.

### 2.1.5 Single-side etch

For the integration in solar cells, the two sides of the wafer are often processed differently and need therefore a separate conditioning. In our case, the instability of the  $\text{SiO}_x(\text{n})$  layer against HF forced us to etch only on one side. Mostly this was used to remove a  $\text{SiO}_x$  layer grown on the opposite side of the wafer without etching the  $\text{SiO}_x(\text{n})$  layer stack. This oxide on the rear side is either grown unintentionally during the annealing when the wafer surface is unprotected, or intentionally when a protection layer was applied (s.f. section 6.6.1). Here, we would like draw the attention of the reader to the fact that HF can cause serious damage to health and should be handled with greatest caution and appropriate protective gear. First we used the *Single-droplet method*<sup>1</sup>. To this end, the wafer is placed horizontally and a drop of HF is applied to the wafer surface with a pipette. Normally, the silicon wafer surface is hydrophilic due to silicon oxide, but as soon as the oxide is removed partially by the HF, the etched area becomes hydrophobic. This hydrophobic behavior means wetting of the HF-droplet (mainly water) and the wafer surface decreases and the surface tension of the HF-droplet gets more dominant. Therefore, the droplet gets more spherical as sketched in Figure 2.1 and the droplet is propelled to areas still covered with silicon oxide, driven by better wetting of such areas. At the border of the wafer, the surface tension of the droplet is high enough to prevent it from falling off. The movement of the HF-droplet continues until all the oxide is removed. Finally, the HF-droplet is removed from the surface by a pipette or by carefully dipping the wafer into deionized (DI) water. For unprotected surfaces with only a thin silicon oxide layer, this method worked well, whereas for a thicker oxide some traces of the droplets were visible. Therefore we propose the *Double-droplet method*<sup>1</sup> for which after the oxide is removed by the Single-droplet method and the droplet is removed, a second drop is placed on the wafer surface covering almost the entire wafer surface (~5mm at the border) and remains there for 10 min before it is removed again by the pipette or by a dip in the DI water.

<sup>1</sup>These methods were developed together with Philippe Wyss.

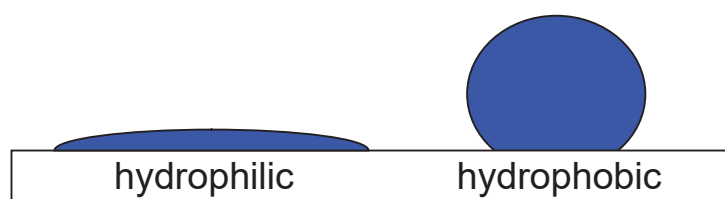


Figure 2.1 – Hydrophilic versus hydrophobic behavior.

### 2.1.6 Metallization

If not otherwise mentioned, we used the standard metallization the was developed for silicon heterojunction (SHJ) solar cells [Geissbühler 2015, Seif 2015a]. To this end, indium tin oxide (ITO) was used as transparent conductive oxide (TCO) and silver (Ag) as rear reflector. Both are deposited by magnetron sputtering using argon as sputter gas mixed with additional oxygen in the case of ITO. Prior to the sputtering, an HF (1 vol.-%) etch is applied to the samples until the n-side was hydrophobic in order to remove residual native or thermal oxide layers at the wafer surface. The ITO sputtering on the front and rear was done through  $2.2 \times 2.2 \text{ cm}^2$  shadow masks that were aligned to cover the same area. Thicknesses of 80 nm and 130 nm were used for the front and the rear-side of the solar cells, respectively. The solar cells were then finished by sputtering a silver reflector on the rear side and screen-printing an Ag grid on the front side, followed by curing for 30 min at  $210^\circ\text{C}$  in a belt furnace.

Figure 2.2 shows two wafers with different layouts of solar cells. The “old design” applies to pseudo-square wafers and accommodates only three cells on a pseudo-square 4-inch wafer. Additionally, one busbar is placed within the illuminated area, leading to shading losses of 5% together with the fingers. A “new design” containing 5 solar cells per 4-inch wafer was applied. By placing two busbars outside of the illuminated area and by using thinner fingers only, effective shading losses are reduced to 3%. Additionally, pads with ITO deposition but without silver are present in both cell designs for optical measurements. The transfer length method (TLM) pads are for ITO characterization. The analysis of the contact resistivity measurements in the underlying silicon structure requires dedicated samples as explained in section 2.3.8.

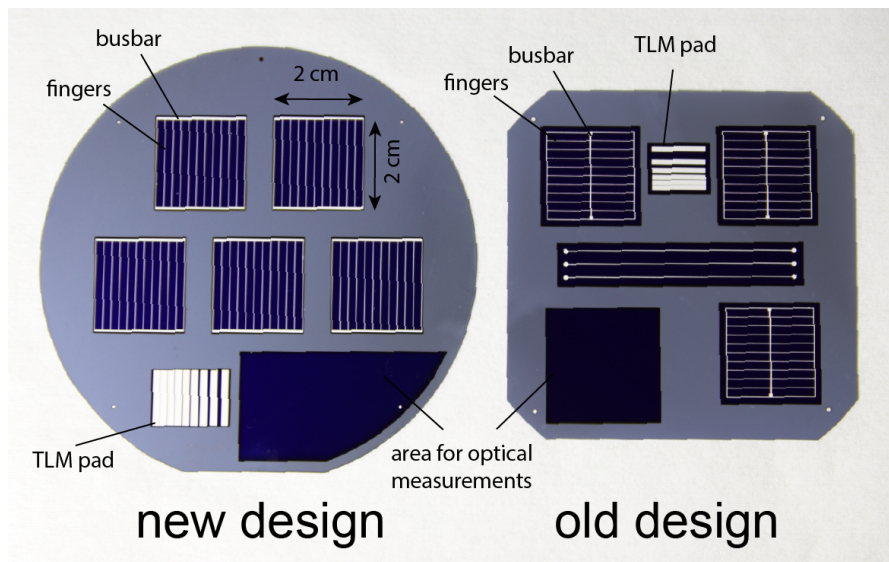


Figure 2.2 – Foto with finished solar cells on a using the old (right) an new (left) cell design.

## 2.2 Fabrication of solar cells

Since in our Laboratory no boron-diffused emitter was available to test the electron-selective emitter in a complete solar cell, two other strategies were followed for the implementation into working devices. First, a so called hybrid cell was used where an  $a$ -Si(i)/ $a$ -Si(p) rear heterojunction was added at low temperature after the front side high temperature processes are finished. Second, the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack was combined with a boron-doped passivating contact deposited subsequently to the n-type contact as well by PECVD; this approach will be called "co-annealed" hereafter since both in-diffused regions are formed in one single annealing step. We start with a description of the hybrid cell since this device design was available earlier in the thesis.

### 2.2.1 Process flow for hybrid solar cells

The process flow for hybrid cells using a SHJ rear contact is sketched in Figure 2.3.

- (a) Starting with a bare silicon wafer, the wafer is cleaned and the chem-SiO<sub>x</sub> is grown on both sides of the wafer by a 80 °C hot HNO<sub>3</sub> solution for 10 min.
- (b) The electron-selective contact layer (either the mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer stack as sketched or a  $\mu$ c-Si:F(n) layer used in chapter 7) is deposited on one side of the wafer by PECVD using the Kai-M system. On the opposite side an intrinsic amorphous silicon oxide layer (prot.oxide, details in section 6.6.1) is deposited used as protection against the in-diffusion of impurities.
- (c) Annealing at 800–950 °C in the Tempress tube in nitrogen atmosphere (if the PEO system is used, this is mentioned). During this step phosphorus diffuses through the chem-SiO<sub>x</sub> into the wafer forming a highly-doped region close to the interface. An FGA is performed for hydrogenation of the interfaces. But to avoid contamination of the PECVD system used later on for the SHJ rear, no atomic hydrogenation by SiN<sub>x</sub> is used for the hybrid cell approach.
- (d) But first, the protection oxide at the rear is removed by a one-side HF-etch using either the Single-or Double droplet method.
- (e) HF-etch (1 vol.%) of the full wafer for 75 s (planar) or 60 s (textured), respectively. In the same PECVD system (Kai-M) as before, an intrinsic  $a$ -Si(i) (~ 4 nm) followed by a boron-doped  $a$ -Si(p) (~ 12 nm) layer is deposited on the rear side.
- (f) ITO is sputtered on front and rear through 2.2 x 2.2 cm<sup>2</sup> shadow masks that were aligned to cover the same area. Thicknesses of 80 and 130 nm were used for front and rear side of the solar cells, respectively. The solar cells were then finished by sputtering silver on the rear side, for both contact and reflector functionalities, and screen printing an Ag grid on the front side, followed by curing for 30 min at 210 °C in a belt furnace.

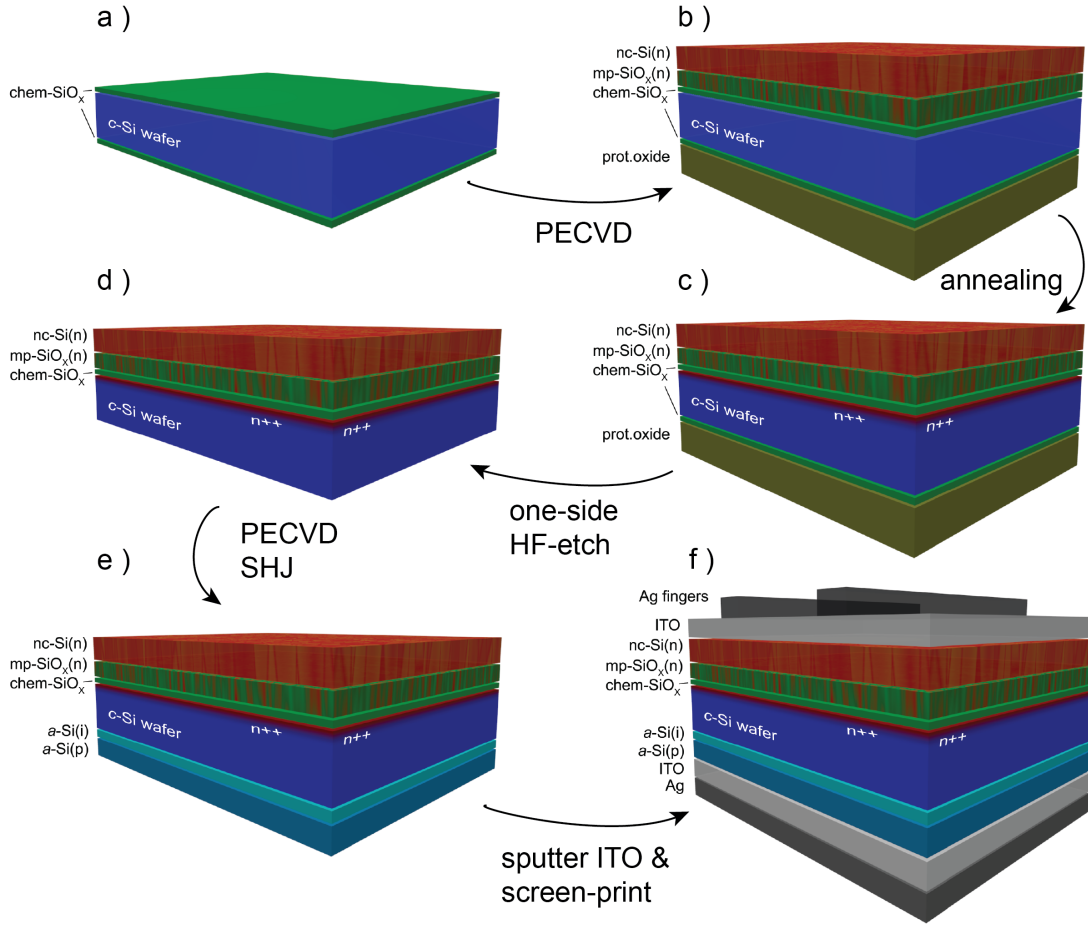


Figure 2.3 – Process flow for the fabrication of a hybrid solar cell, starting with (a) a clean bare wafer and growing the chem-SiO<sub>x</sub> in hot HNO<sub>3</sub>, (b) deposit the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack at the front and a protection oxide at the rear by PECVD, (c) annealing at 800–950 °C, (d) remove the protection oxide by a one-sided HF-etch, (e) deposit a SHJ *a*-Si(i)/*a*-Si(p) rear by PECVD, (f) sputter the ITO front and rear ITO/Ag layers and finish the cells by screen-printing silver fingers on the front and cure for 30 min at 210 °C.

### 2.2.2 Process flow for co-annealed solar cells

For the co-annealed cells, the process flow is sketched in Figure 2.4.

- (a) Starting as the hybrid cell with a bare silicon wafer, the wafer is cleaned and the chem-SiO<sub>x</sub> is grown on both sides of the wafer by a 80 °C hot HNO<sub>3</sub> solution for 10 min.
- (b) The electron-selective contact layer (either the mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer stack as sketched or a  $\mu$ c-Si:F(n) layer used in chapter 7) is deposited on one side of the wafer by PECVD using the Kai-M system. On the opposite side, for the hole-selective contact either a SiO<sub>x</sub>(i/p) [Wyss 2018] or an *a*-SiC<sub>x</sub>(p) [Nogay 2017] was used.

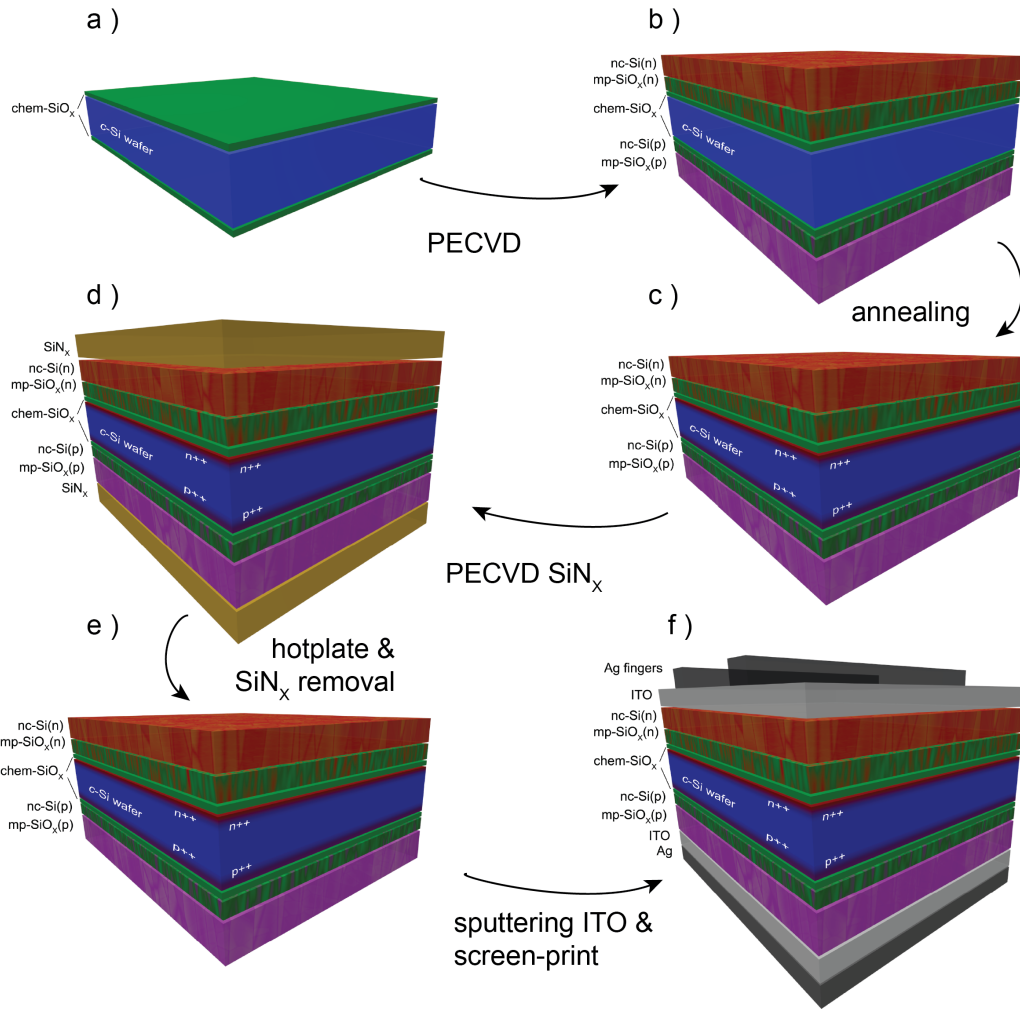


Figure 2.4 – Process flow for the fabrication of a co-annealed solar cell, starting with (a) a clean bare wafer and growing the  $\text{chem-SiO}_x$  in hot  $\text{HNO}_3$ , (b) deposit the  $\text{mp-SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  layer stack at the front and a hole-selective contact (in this case a  $\text{SiO}_x(\text{i/p})$  bilayer) at the rear by PECVD, (c) annealing at  $850\text{--}900\text{ }^\circ\text{C}$ , (d) deposit a  $\text{SiN}_x$  layer by PECVD on both sides, (e) after a hotplate-annealing, remove the  $\text{SiN}_x$  by HF or boiling  $\text{H}_3\text{PO}_4$ , (f) sputter the ITO front and rear ITO/Ag layers, and (f) finish the cells by screen-printing silver fingers on the front and cure for 30 min at  $210\text{ }^\circ\text{C}$ .

- (c) Both contacts are then annealed at the same time during which the dopants diffuse into the wafer and form a highly phosphorus- and boron-doped region below the  $\text{chem-SiO}_x$  on each side of the wafer respectively. This is done at  $900\text{ }^\circ\text{C}$  for 15 min in the Tempress tube in nitrogen atmosphere when the  $\text{SiO}_x(\text{i/p})$  contact is used to fit its thermal budget. For co-annealed cells with the  $\text{a-SiC}_x(\text{p})$  hole contact, the PEO system is with a dwell time of 0 min at  $850\text{ }^\circ\text{C}$ . This means that the heating with  $10\text{ }^\circ\text{C}/\text{min}$  is directly followed by a cooling ramp of  $2\text{ }^\circ\text{C}/\text{min}$ , i.e. without annealing dwell time.

- (d) An FGA is performed for molecular hydrogenation and additional an atomic hydrogenation using  $\sim 80$  nm PECVD deposited  $\text{SiN}_x$  on both sides of the wafer, which releases hydrogen to the interfaces during a hotplate-annealing at  $450^\circ\text{C}$  for 30 min.
- (e) The insulating nitride needs to be etched off which is done either in a solution of HF (5 vol.-%) for 12 min or in a solution of boiling ( $180^\circ\text{C}$ )  $\text{H}_3\text{PO}_4$  for 30 min (f). When  $\text{H}_3\text{PO}_4$  is used, an HF-etch (1 vol.%) of the full wafer for 75 s (planar) or 60 s (textured) is done whereas when the nitride is stripped by HF the ITO sputtering followed directly.
- (f) ITO is sputtered on front and rear through  $2.2 \times 2.2 \text{ cm}^2$  shadow masks that were aligned to cover the same area. Thicknesses of 80 and 130 nm were used for front and rear side of the solar cells, respectively. The solar cells were then finished by sputtering silver on the rear side, for both contact and reflector functionalities, and screen printing an Ag grid on the front side, followed by curing for 30 min at  $210^\circ\text{C}$  in a belt furnace.

## 2.3 Characterization

### 2.3.1 Raman measurement

Crystallization of the Si phases and stress in the layer were characterized by Raman spectroscopy. The polarization of the laser was chosen such that the underlying  $\langle 100 \rangle$ -oriented wafer does not contribute to the measured signal [Yoo 2015]. As illustration, a bare  $c$ -Si  $\langle 100 \rangle$  wafer is measured using a polarized green Ar laser (514 nm) placed on a rotation stage<sup>2</sup>. In Figure 2.5a the  $c$ -Si peak ( $520 \text{ cm}^{-1}$ ) intensity is shown as a function of the wafer orientation. The signal from the  $\langle 110 \rangle$ -direction is decreased compared to the signal

<sup>2</sup>This measurement was performed by Yanfei Zhao during a semester project.

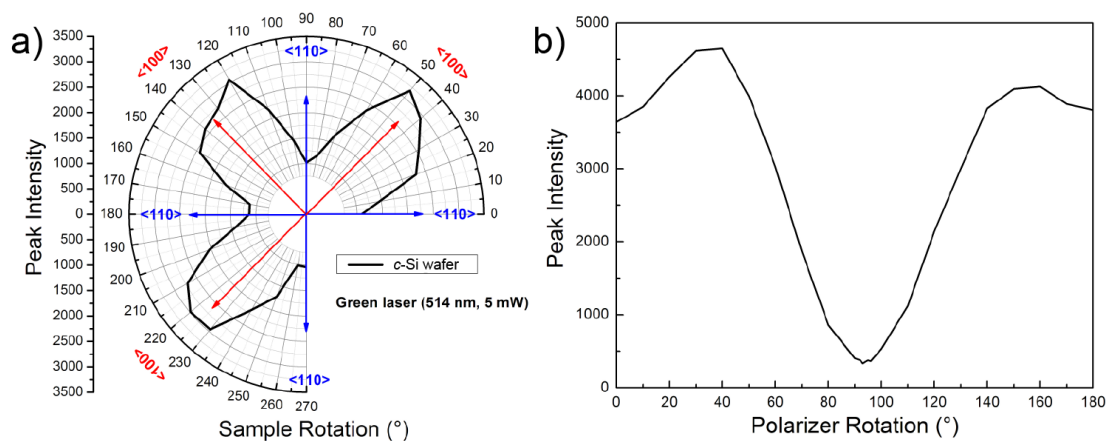


Figure 2.5 – Raman  $c$ -Si peak ( $520 \text{ cm}^{-1}$ ) intensity of a bare  $c$ -Si wafer as (a) a function its orientation and (b) of the rotation of a polarizer placed in the collection path of the Raman system.

in  $\langle 100 \rangle$ -direction by a factor of  $\sim 3$ . To further suppress the signal from the wafer, a linear polarizer is placed in the optical path of the collecting system and the  $\langle 110 \rangle$ -direction of the wafer is measured and the  $c$ -Si peak ( $520 \text{ cm}^{-1}$ ) intensity is plotted as a function of the analyzer rotation (Figure 2.5b). The measurement result shows that the peak intensity can be decreased by another ten times at proper polarizer rotation angle. Since the  $a$ -Si and  $\mu c$ -Si layers that we analyze are randomly oriented, choosing the correct angle and polarizer position leads to a suppression of the  $c$ -Si signal while the signal of the layers are only minimally affected.

The Raman measurements in chapter 3 were performed by Dr. Ledinsky from the Laboratory of Nanostructures and Nanomaterials at the Academy of Sciences of the Czech Republic in Prag and are acknowledged by the author. Care was taken to suppress the signal of the silicon wafer in order to get a clear signal only from the deposited layers. This was done using a 442 nm laser, which has a Raman collection depth of only around 150 nm in  $c$ -Si [Ledinský 2008].

Measurements presented in chapter 7 were performed on a MonoVista CRS+ (Spectroscopy & Imaging GmbH) using a 325 nm laser, which has a Raman collection depth of only around 13 nm in  $c$ -Si [Carpenter 2017]. The Raman measurements were performed by Luca Antognini and are acknowledged by the author.

All the measured spectra are normalized with respect to their  $c$ -Si peak and background signal between 550–650 nm.

### 2.3.2 Spectrophotometer

Transmittance ( $T$ ) and reflectance ( $R$ ) are measured by a Perkin-Elmer Lambda 950 spectrometer equipped with a 150 mm InGaAs detector attached to an integrating sphere. A wavelength range of 320–2000 nm is typically used and the absorbance ( $A$ ) is obtained using  $1 = T(\lambda) + R(\lambda) + A(\lambda)$ .

### 2.3.3 Ellipsometry

Variable angle spectroscopic ellipsometry (VASE, uvisel Horiba) was used to extract the optical properties of the layers after the application of an appropriate model using the software DeltaPsi2 (Horiba). The samples were measured using angles of  $60^\circ/70^\circ/80^\circ$  with respect to the plane. The angular range was chosen since the measurement is most sensitive around the Brewster angle which is  $74^\circ$  for the interface between air and  $c$ -Si [Stuckelberger 2014]. A more detailed description of the used model can be found in section 6.3.

### 2.3.4 Scanning electron microscopy

The scanning electron microscopy (SEM) images were acquired using a Zeiss Gemini 300 microscope, equipped with a beam booster to maintain high brightness of the electron

probe at low landing energies. The microscope is also equipped with two secondary electron detectors (Everhart-Thornley and In lens), two backscattered electrons detectors (standard one and the energy-selective backscattered detector) and one energy-dispersive X-ray (EDX) detector. The SEM measurements were performed by Federica Landucci at the Interdisciplinary centre for electron microscopy (CIME) at EPFL and are acknowledged by the author.

### 2.3.5 Transmission electron microscopy

The structural changes were further characterized by transmission electron microscopy (TEM) in a FEI Titan Themis if not otherwise mentioned. The microscope was operated at 300 kV for experiments involving high-resolution (HR) TEM and scanning TEM (STEM) high-angle annular dark field (HAADF) imaging combined with EDX spectroscopy. An acceleration voltage of 200 kV was used for STEM electron energy-loss spectroscopy (EELS) measurements which were performed with a convergence of 28 mrad and a similar collection angle using a Gatan GIF Quantum ERS high energy resolution EELS spectrometer and energy filter (dispersion of 0.1 eV per channel). Other TEM images were taken using a FEI Tecnai Osiris microscope operated at 200 kV and equipped with Chemistem detectors for the EDX analysis. To this end, TEM lamellae were prepared from samples that were either as-deposited or annealed at 850 °C or 900 °C using the conventional focused ion beam (FIB) lift-out technique in a Zeiss Nvision 40.

Advanced characterization in the TEM was performed by in-situ annealing of the sample such that the same spot was analyzed during its structural changes. To this end, the sample was

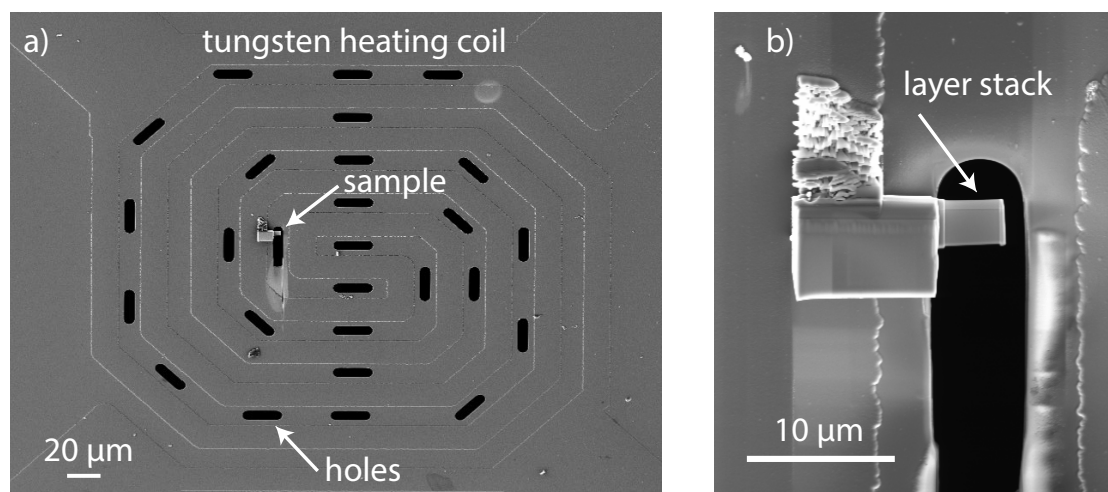


Figure 2.6 – (a) Center of the MEMS Nano-chip used for in-situ annealing during TEM measurements with the tungsten heating coil and (b) a magnification where the sample lamella is placed.

placed on a MEMS (Microelectromechanical system) Nano-chip (wildfire, [DEN 2018]) based on silicon covered by a thin amorphous silicon nitride film ( $\text{Si}_3\text{N}_4$ ). The silicon is etched from the rear below the nitride film at the point of interest and a tungsten heating coil is used to control the temperature by a four-point probe resistive feedback (left side in Figure 2.6). Thus, only a small volume is heated and cooled down, giving the possibility to measure with high accuracy without a strong drift. The sample lamella is placed above one of the holes (right side of Figure 2.6) within the heating coil.

The TEM measurements were performed by Dr. Jeangros at the Interdisciplinary centre for electron microscopy (CIME) at EPFL and are acknowledged by the author.

### 2.3.6 Photo-conductance decay

The passivation quality was analyzed by photo-conductance decay (PCD) measurements using a WCT-120 lifetime measurement tool from Sinton Instruments. The contactless method can be used to measure the effective charge carrier lifetime  $\tau_{eff}$  for a wide range of excess charge carrier densities  $\Delta n$ . The sample is placed on a coil that measures the conductance of the sample via its reflectivity in the microwave range. By a flash of a given duration, excess carriers are generated and increase the conductance. After the flash, the conductance decreases due to recombination of the excess carriers. The lifetime  $\tau_{eff}$  of the sample is then given by:

$$\tau_{eff}(\Delta n) = \frac{\Delta n(t)}{G - \frac{\partial \Delta n(t)}{\partial t}} \quad (2.1)$$

where  $G$  is the photogeneration as explained in 1.2.1. In this report the measurements were performed in *transient* mode which uses a flash with a decay time of  $\sim 30\mu\text{s}$ , which is much smaller than the lifetime of the sample and therefore the generation can be neglected leading to:

$$\tau_{eff}(\Delta n) = \frac{\Delta n(t)}{\frac{\partial \Delta n(t)}{\partial t}} \quad (2.2)$$

Knowing the wafer thickness and the doping concentration together with formula 1.7, the implied open-circuit voltage ( $iV_{OC}$ ) can be calculated:

$$iV_{OC} = \frac{kT}{q} \ln \left( \frac{\Delta n(N_A + \Delta n)}{n_i^2} + 1 \right) \quad (2.3)$$

For the extraction of the emitter saturation current density  $J_0$ , the method of Kimmerle [Kimmerle 2015] was applied which modifies the method proposed by [Kane 1985] by taking into account the finite carrier diffusion coefficient. If not otherwise stated,  $J_0$  was extracted at a excess carrier density corresponding to ten times the base doping.

### 2.3.7 Electrochemical capacitance-voltage measurements

The electrically active phosphorus doping profile diffused into the *c*-Si was measured by electrochemical capacitance-voltage (ECV) measurements using 0.1 molar ammonium hydrogen difluoride (NH<sub>4</sub>HF<sub>2</sub>) solution for the etch process in a wafer profiler CVP21 (WEP).

If not otherwise stated, the measurement was performed after stripping the stack of deposited layers and the interfacial oxide by prolonged etching in a 20 vol.-% HF solution.

### 2.3.8 Transfer length method

The transfer length method (TLM) was originally proposed by Shockley and is still a common method to determine the contact resistivity between a semiconductor and planar ohmic contacts [Schroder 1984]. The method works by placing a series of metallic pads separated by various inter-pad distances  $d$  as illustrated in Figure 2.7b. The total resistance  $R_T$  is deduced between two pads and plotted as a function of the inter-pad distance as sketched in Figure 2.7a. Ideally, the resistances follow a linear behavior whose slope is related  $R_{SH}$ . The intersection with the ordinate is directly related to the contact resistivity  $\rho_c$ . The total resistance  $R_T$  is the sum of two times the resistance directly under the contact and the resistance outside the contact region:

$$R_T = \frac{R_{SK} \cdot L_T}{W_{TLM}} + \frac{R_{SH} \cdot d}{W_{TLM}} \quad (2.4)$$

where  $R_{SK}$  is the sheet resistance directly under the contact,  $R_{SH}$  the sheet resistance between the pads,  $W_{TLM}$  the width of the TLM pads as sketched in Figure 2.7b,  $L_T$  the transfer length and  $d$  the inter-pad distance. From the slope of  $R$ - $T$  the sheet resistance  $R_{SH}$  can be directly

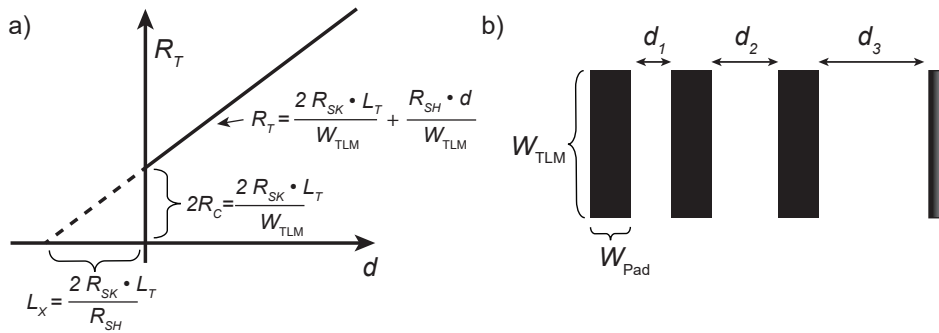


Figure 2.7 – (a) Total resistance measured by TLM as a function of the inter-pad distance  $d$ , adapted from [Reeves 1982]. (b) A sketch of the topview of the TLM structure with increasing distances  $d_i$  between the metallic pads

calculated.

$$\frac{\partial R_T}{\partial d} = \frac{R_{SH}}{W_{TLM}} \quad (2.5)$$

A first approximation in TLM is done by assuming that  $R_{SK}$  is equal to  $R_{SH}$  leading to  $L_X = 2L_T$ . Moreover, the transfer length must be much smaller than the pad length ( $W_{Pad}$ ), at least  $W_{Pad} > 2L_T$  [Schroder 1984]. This leads to an effective contact area of  $L_T \cdot W_{TLM}$  instead of  $W_{Pad} \cdot W_{TLM}$  and therefore the contact resistance can be calculated:

$$R_C = \sqrt{\frac{\rho_c}{W_{TLM} \cdot L_T}} \quad (2.6)$$

This method assumes a homogeneous semiconductor which is not the case here due to the in-diffused regions. Even though we have not seen a current spreading within the deposited layers itself, we have observed an influence of the higher-doped region at the interface as is explained more in detail in section 4.3.3.

### 2.3.9 $J$ - $V$ measurements

Current voltage ( $J$ - $V$ ) characteristics of the cells were measured at 25 °C with a source meter (Keithley, 2601A), using an AAA solar simulator (Wacom) calibrated to 100 mW/cm<sup>2</sup> with a  $c$ -Si reference cell measured at CalLab PV Cells—Fraunhofer ISE. A shadow mask on the front is used to define the illuminated area to 2 x 2 cm<sup>2</sup>. Out of this measurement, the most important parameter for the solar cell, open-circuit voltage  $V_{OC}$ , short-circuit current density  $J_{SC}$ , and the fill factor  $FF$  can be deduced and the conversion efficiency  $\eta$  is calculated. An example of an  $J$ - $V$  curve together with explanations to the single parameters can be found in section 1.2.4.

### Temperature-dependent $J$ - $V$ measurements

Temperature-dependent  $J$ - $V(T)$  measurements were performed using an in-house built hybrid light-emitting diode (LED)-halogen solar simulator in the temperature range of –100 °C to 75 °C. Detailed information about this set-up can be found in [Riesen 2016]. The illumination intensities and the spectrum of this setup are not perfectly calibrated, as the distance between light source and chuck was increased and an additional glass pane was introduced to enable temperature measurement down to –100 °C. Therefore, it is possible to compare between samples measured on this system, but absolute values will slightly differ from calibrated  $J$ - $V$ -measurements performed with the sun simulator (Wacom).

### 2.3.10 External quantum efficiency

The external quantum efficiency (EQE) is the ratio of extracted charge carriers to the number of photons incident on the solar cell at a given wavelength  $\lambda$  and can be calculated from the measured spectral response  $SR(\lambda)$  (in  $AW^{-1}$ ), which is a measure for the collected charge carrier current to the incident photon power:

$$SR(\lambda) = \frac{q}{hc} \cdot EQE(\lambda) \cdot \lambda \quad (2.7)$$

Here,  $q$  is the elemental charge,  $h$  the Planck constant, and  $c$  the velocity of light in vacuum. Convoluting the  $SR(\lambda)$  with the solar spectrum  $\Phi_{AM1.5g}$  (in  $W m^{-2} nm^{-1}$ ) and integrating over the spectral range, the  $J_{SC}$  can be calculated [Stuckelberger 2014]:

$$J_{SC,EQE} = \int_0^{\infty} SR(\lambda) \cdot \Phi_{AM1.5g}(\lambda) d\lambda \quad (2.8)$$

This gives the possibility to identify loss mechanism inside solar cells. Light with short wavelength (blue, high-energetic photons) is absorbed within the first 10–100 nm of a cell, whereas light with longer wavelength (red light, low-energetic photons) can pass the full wafer and even bounce back and forth until it is either absorbed or reflected out of the solar cell. Therefore losses in the blue part of the spectrum are more related to front side effects whereas losses in the red are more related to the bulk and rear side.

For the measurements two different systems were used, either an IQE-SCAN (pv-tools) or an in-house built system (more details in [Dominé 2009]). The IQE-SCAN system measures the EQE including the metallization (3–5% shading losses depending on the used cell design) on the full  $2 \times 2 \text{ cm}^2$  cell. The system also measures the reflectance ( $R$ ). The in-house built system has a small spot size that measures between the fingers without shading losses. The reflectance is measured separately by the photospectrometer explained in section 2.3.2. Note that the photospectrometer measures with a different spot size on the optics pad of the wafer shown in Figure 2.2. Out of the EQE and  $R$  the internal quantum efficiency (IQE) is calculated:

$$IQE = \frac{EQE}{1 - R} \quad (2.9)$$

We don't expect to have down conversion of a high energy photon transferring its energy to two lower energy photons in the investigated samples and therefore the IQE has only a physical meaning between 0 and 1. Measurement artifacts, mainly due the different spot size between EQE and  $R$ , lead to a variation of  $\pm 1\%$  in the calculated IQE. For the cases when the IQE exceeded 1, the minimal reflectance was recalculated to an IQE of 1 and  $R(\lambda)$  changed accordingly.

For comparison of  $R$  and IQE with simulations using OPAL [PVLighthouse 2018b], the reflectance (measured including shading losses) are corrected by subtracting 3% shading losses to achieve spectra without shading losses. Subsequently the EQE is corrected by a factor

of 1.03 for calculating the IQE.

### 2.3.11 Suns- $V_{OC}$ measurement

Suns- $V_{OC}$  measurements were carried out at 25 °C using the Suns- $V_{OC}$  unit of a WCT-100 photoconductance tool by Sinton Consulting Inc. A Suns- $V_{OC}$  measurement detects the photogenerated voltage of a finished solar cell as a function of the illumination. The measurement is free of any transport related losses since no current is extracted during the measurement. Therefore a so called pseudo- $J-V$  curve is obtained and can be used in comparison with the standard  $J-V$  curve to calculate the series resistance  $R_S$  [Wolf 1963, Pysch 2007a]. Additionally, the comparison of  $iV_{OC}$  with pseudo $V_{OC}$  ( $pV_{OC}$ ) can be used to determine selectivity of a contact structure [Würfel 2015].



## 3 Mixed-phase silicon oxide — Structure

In this chapter, the structure of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack is investigated. The crystallinity of the nc-Si(n) layer is measured by Raman measurements for different thermal budgets and the related stress release within the layer is shown.

Two growth regimes are identified within the mixed-phase silicon oxide layer: A region with columnar silicon-rich phases and a second region in which the silicon inclusions develop more in lateral direction. In both regions, the silicon and oxide phases remain separated during the thermal treatment.

Within the mp-SiO<sub>x</sub>(n) layer, an oxygen content of 50–60% is quantified at the chem-SiO<sub>x</sub>/wafer interface, decreasing to around 25% near the border with the nc-Si(n) layer. We find more phosphorus in the as-deposited state with a higher content in the nc-Si(n) layer compared to the mp-SiO<sub>x</sub>(n) layer while, after annealing, a higher concentration is observed in the mp-SiO<sub>x</sub>(n) layer.

Finally we present silicon oxide channels through the layer stack which are formed during the thermal treatment and which we relate to be one of the main reasons for the high sensitivity to chemical treatments of this structure.

Some of the results of this chapter were published in 2016 in *Solar Energy Materials and Solar Cells* [[Stuckelberger 2016a](#)].

### 3.1 Introduction

For the development of an electron-selective contact, we target a layer stack that is optically transparent while maintaining good surface passivation and electrical transport of the majority carriers. To reach higher transparency, on one side highly crystalline layers were targeted to reduce parasitic absorption in the amorphous phase; on the other side part of the silicon was replaced by a wide-bandgap material. We propose a structure as sketched in [Figure 3.1](#) having an ultra-thin chemical SiO<sub>x</sub> (chem-SiO<sub>x</sub>) layer covered by a mixed-phase silicon

oxide ( $\text{mp-SiO}_x(\text{n})$ ) layer and a nanocrystalline silicon ( $\text{nc-Si}(\text{n})$ ) layer, both highly-doped with phosphorus. After the thermal treatment an in-diffused region within the wafer is formed directly below the  $\text{chem-SiO}_x$ .

In the 1980s, first approaches to passivate silicon wafers with a thin silicon oxide layer capped with doped poly-Si were pioneered [Gan 1990, Kwark 1984, Yablonovitch 1985]. Semi-insulating poly-Si (SIPOS) alloyed with oxygen was used, obtaining impressive passivation, but the high contact resistivity limited efficient extraction of current from solar cells [Kwark 1984, Yablonovitch 1985, Matsushita 1981]. The SIPOS structure was understood as randomly oriented silicon crystals embedded in a matrix of silicon oxide. A similar model is used to describe photoluminescent silicon nanoparticles which are obtained after the annealing of silicon-rich  $\text{SiO}_x$  layers that are placed between near-stoichiometric  $\text{SiO}_{2-x}$  layers [Hartel 2013, Zacharias 2002, Ledoux 2000, Hiller 2017, Löper 2013, Gnaser 2014, König 2015]. Inspired by the work of [Cuony 2011], we propose the use of in-situ grown nanocrystalline  $\text{SiO}_x$  which has a higher oxygen content than the SIPOS structure. Rather than containing randomly oriented nanocrystals, it consists of silicon filaments in the direction of growth that supports transverse conductivity.

## 3.2 Experimental details

The investigation of the passivating electron contact was done using symmetrical structures based on 280- $\mu\text{m}$ -thick double-side-polished 4-inch wafers. They are 100-oriented and boron-doped to a conductivity of 2.8  $\Omega\text{cm}$ . After cleaning, using standard wet chemistry, a thin ( $\sim 1.2\text{ nm}$ )  $\text{SiO}_x$  layer was formed by wet chemical oxidation [Asuha 2003, Grant 2009] also referred to as  $\text{chem-SiO}_x$ . Subsequently, a phosphorus-doped  $\text{mp-SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  bilayer structure of a mixed-phase silicon oxide ( $\text{mp-SiO}_x(\text{n})$ ) layer and a nanocrystalline silicon ( $\text{nc-Si}(\text{n})$ ) layer was deposited by PECVD on both sides. The individual layers are also referred to as  $\text{mp-SiO}_x(\text{n})$  and  $\text{nc-Si}(\text{n})$  in order to distinguish from the  $\text{chem-SiO}_x$ . The samples were

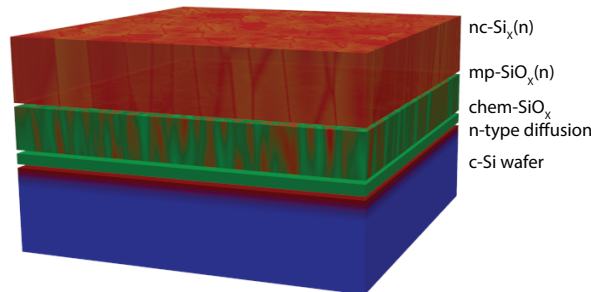


Figure 3.1 – Sketch of the targeted bilayer structure after the thermal treatment including the phosphorus-diffused region.

### 3.3. Crystallinity measured by Raman spectroscopy

then annealed for 15 min in nitrogen ( $N_2$ ) atmosphere at temperatures from 750 °C to 950 °C. This was followed by 30 min of forming gas (4%  $H_2$  in  $N_2$ ) annealing at 500 °C to passivate electronic defects at the wafer-chem-SiO<sub>x</sub> interface.

Crystallization of the silicon phases and stress in the layer were characterized by Raman spectroscopy. Care was taken to suppress the signal of the silicon wafer in order to get a clear signal from the deposited layers only. This was done by using a 442 nm laser, which has a Raman collection depth of only around 150 nm in *c*-Si [Ledinský 2008], and by polarizing the laser in such a way that the signal from the underlying wafer was minimized [Yoo 2015]. More details on this technique can be found in section 2.3.1. The Raman measurements were performed by Dr. Ledinsky from the Laboratory of Nanostructures and Nanomaterials at the Academy of Sciences of the Czech Republic in Prague.

The surface roughness was analyzed by atomic force microscopy (AFM) using the height sensor in an AFM Dimension Edge (Bruker Inc.) in the forward and reverse direction in Scanasyt mode as well as in tapping mode.

### 3.3 Crystallinity measured by Raman spectroscopy

The crystallinity of the contact layer was analyzed by Raman spectroscopy, as illustrated in Figure 3.2. Already in the as-deposited state, the Raman spectrum is dominated by the transverse optical (TO) *c*-Si phonon with a peak around 520.5  $cm^{-1}$ . However, the signal still shows a pronounced shoulder at wavenumbers between 400  $cm^{-1}$  and 510  $cm^{-1}$ , which can be attributed to an *a*-Si phase [Iqbal 1982]. After 15 min of annealing at 750 °C, measured at

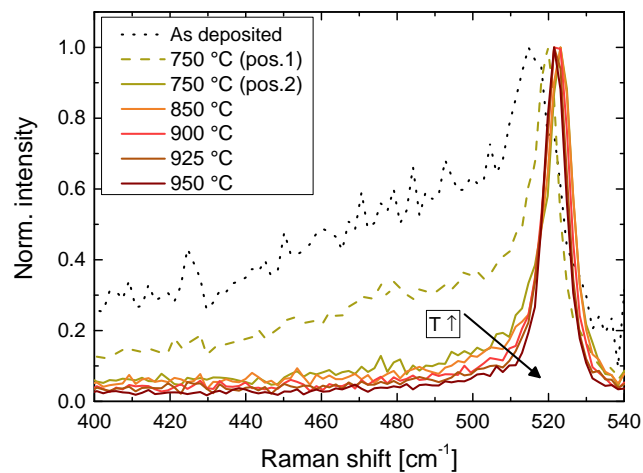


Figure 3.2 – Raman spectra showing a clear tendency towards a lower amorphous fraction with increasing temperature. [Stuckelberger 2016a].

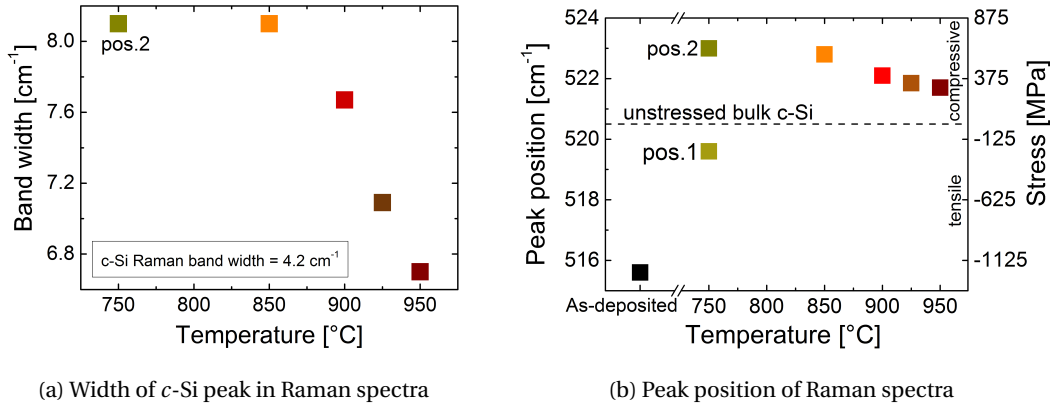


Figure 3.3 – (a) The width of the crystalline peak as a measure for the crystallinity plotted as function of the annealing dwell temperature. (b) The peak position (left axis) which is directly related to stress in the layer system (right axis) plotted versus the annealing dwell temperature. The dashed line represents the unstressed bulk position of the *c*-Si peak at  $520.5 \text{ cm}^{-1}$  [Stuckelberger 2016a].

position 1, the amorphous fraction is still present. Measuring at a slightly different position only some micrometers apart (position 2), the amorphous fraction is hardly detectable. This means that annealing at  $750 \text{ }^{\circ}\text{C}$  for 15 min is not sufficient to fully crystallize the layers homogeneously. For higher annealing temperatures, the amorphous fraction decreases further and lateral inhomogeneities vanish (not shown here). The amorphous contribution almost disappears for a dwell temperature of  $950 \text{ }^{\circ}\text{C}$ , meaning that the layer is almost fully crystalline. This is more visible when the Raman peak is fitted by a Gaussian. The width of the crystalline peak is plotted in Figure 3.3a as a function of the annealing dwell temperature. With higher temperatures the peak becomes narrower, indicating a higher crystallinity and a reduced contribution of the amorphous matrix. For comparison, by measuring a planar *c*-Si wafer, the peak width for crystalline material was  $4.2 \text{ cm}^{-1}$  in this setup.

A deviation of the Raman shift from its equilibrium position is a measure for internal stress in the layer system [Wolf 1996]. To extract the internal stress, the fit of the Raman peak by a Gaussian is used and the position  $x_0$  of the crystalline peak is plotted as a function of the annealing dwell temperature in Figure 3.3b. The Raman peak shift from the equilibrium position of the *c*-Si TO phonon band at  $520.5/\text{cm}$  is directly proportional to internal stress in the silicon layer ( $\Delta x = 1/\text{cm} \approx 250 \text{ MPa}$  [Wolf 1996]). A deviation towards higher wavenumbers is attributed to compressive stress whereas a deviation towards lower wavenumbers means tensile stress. In the as-deposited state the layer system is under tensile stress of  $1125 \text{ MPa}$ . After annealing at  $750 \text{ }^{\circ}\text{C}$ , the stress at position 1 that had more amorphous material relaxed to  $225 \text{ MPa}$  whereas the stress at position 2 became compressive ( $625 \text{ MPa}$ ). By increasing the temperature to  $950 \text{ }^{\circ}\text{C}$ , the compressive stress relaxes to  $300 \text{ MPa}$ . This might be due to a reorganization of the mp-SiO<sub>x</sub>(n) layer, also accompanied by a phase separation towards a

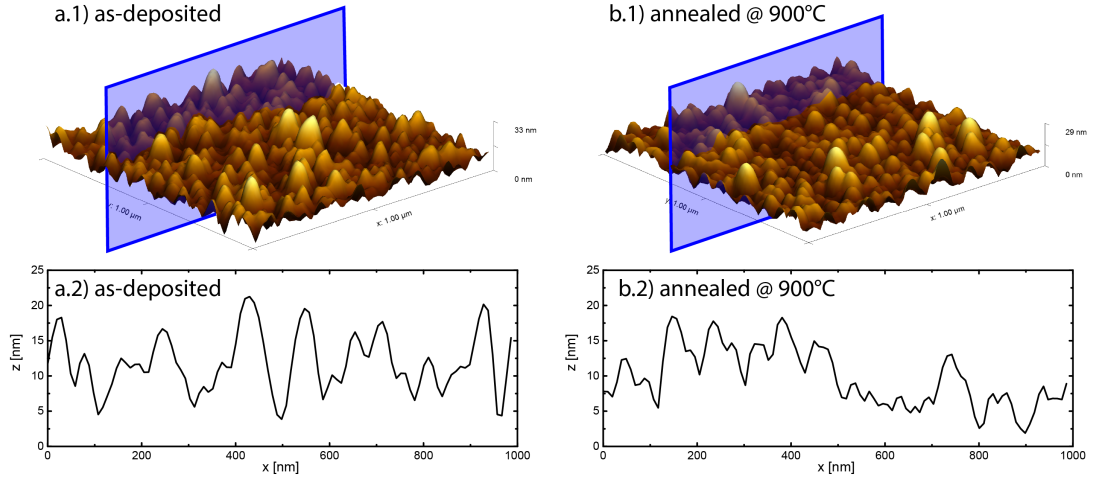


Figure 3.4 – AFM height maps representing the surface of (a.1) the as-deposited sample and (b.1) after an annealing at 900 °C. In (a.2) and (b.2) the corresponding profile at  $y = 300$  nm along the indicated plane in the AFM image is shown.

more stoichiometric  $\text{SiO}_2$ . Additionally a restructuring of the mixed phase takes place, which leads to a lower structural defect density as the stress in the film is lowered [Zacharias 1999].

### 3.4 Surface roughness analysis by AFM

Figure 3.4 shows the AFM height map of the structure after PECVD deposition before any thermal treatment—the so-called as-deposited state—and the corresponding height map after annealing at 900 °C. The surface roughness is quantified by the root-mean-square roughness  $R_{rms}$ , giving  $R_{rms} \sim 4.8$  nm in the as-deposited state and of  $R_{rms} \sim 4.2$  nm after annealing, respectively. Whereas this value is already around one sixth of the stack thickness, some parts have a thickness difference of more than 15 nm, in extreme cases of up to 25 nm which is almost the full layer thickness. This gets even more visible using a line scan (taken at position  $y = 300$  nm). Whereas the overall roughness is diminishing with annealing, this is not observed for the maxima and minima.

### 3.5 Mixed-phase nature analyzed with TEM

The nanostructure of the layer stack and its transformation upon thermal annealing were both investigated by TEM. An STEM HAADF image of the mp- $\text{SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  bilayer structure in the as-deposited state is shown in Figure 3.5. Contrast variations in STEM HAADF images are related to differences in thickness (here approximately constant as a result of the focused-ion beam (FIB) preparation process) and atomic mass, with darker regions highlighting positions

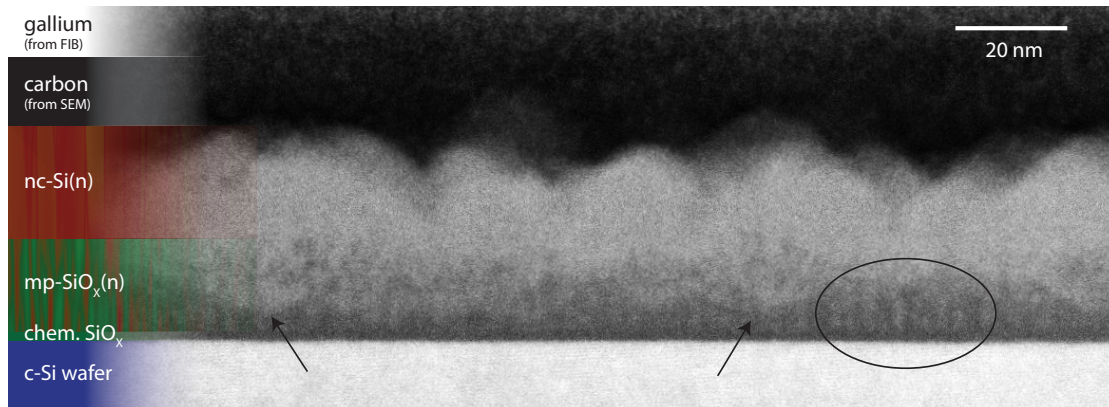


Figure 3.5 – STEM HAADF image of the bilayer structure after the PECVD deposition before any thermal treatment. Region A with vertically oriented silicon filaments is circled, region B with silicon clusters forming a cone is indicated by arrows.

richer in O and P when compared to Si-rich regions. The lower part of the Figure shows a perfect interface between the wafer and the chem-SiO<sub>x</sub> whereas the interface between the mp-SiO<sub>x</sub>(n) and the nc-Si(n) is clearly undulating. Finally, the surface of the nc-Si(n) exhibits a severe roughness. The shading of the nc-Si(n) is brighter than that of the mp-SiO<sub>x</sub>(n) layer, indicating that it is richer in silicon. The darker layers in the upper part of the Figure are part of the sample preparation method. They consist of carbon (dark) deposited from a gas phase by the electron beam of the SEM and a carbon layer including gallium (bright) due to its deposition by focused-ion beam.

The surface roughness detected in Figure 3.4 is visible at higher magnification in Figure 3.5. Protrusions of ca. 20 nm height are formed every 10–40 nm. The main driver for this surface roughness can be associated with the incubation of the silicon phases within the oxide matrix. In the first 2–3 nm on top of the chem-SiO<sub>x</sub>, silicon phases are vertically oriented within the oxide matrix, well distributed and separated from each other by only a few nm. The further growth can be roughly divided into two regimes. In region A (circle), growth of vertically oriented silicon filaments prevails, whereas in region B (arrows) the silicon phases develop more laterally, forming a cone. These two growth regimes proceed with their different deposition rates, leading to locally enhanced layer thicknesses that form spherically shaped hillocks directly above each nucleation center.

In order to investigate in detail the presence of silicon phases within the deposited SiO<sub>x</sub> layer, low-loss electron energy loss (EEL) spectra were recorded in STEM. Using the methodology presented in [Schamm 2008, Cuony 2012], first, three 4-eV-wide images centered at 10 eV, 17.5 eV and 23 eV were extracted from the EELS data. From the first and last images, a linear background was extrapolated and subtracted from the second image taken at the position of the silicon plasmon peak at 17.5 eV as illustrated in Figure 3.6a. The contrast in the resulting image is related to differences in the plasmon signal between silicon (bright) and SiO<sub>x</sub> (dark)

### 3.5. Mixed-phase nature analyzed with TEM

and hence reveals fluctuations in composition within the mp-SiO<sub>x</sub>(n) layer. Please note that the resolution of the STEM EEL spectrum images is limited by the delocalization of the plasmon signal (on the order of 2 nm [Egerton 2009]) which is inherent to the technique. At the wafer surface, a 2–3 nm continuous SiO<sub>x</sub> layer is distinguishable (Figure 3.6b–c). Directly above, the mixed-phase nature of the deposited mp-SiO<sub>x</sub>(n) layer is visible in both regions. In region A, the mp-SiO<sub>x</sub>(n) layer consists of vertically oriented silicon-rich phases that are a few nanometers in diameter and separated from each other by only a few nm. They are well distributed and extend throughout the oxide matrix up to the nc-Si(n) layer deposited on top (arrows in Figure 3.6b1–b2). In region B (Figure 3.6c1–c2, note the different scale), silicon phases develop more in lateral direction than in region A, forming cones surrounded by an oxygen-rich matrix. The apex angle of the cone is  $\sim 75^\circ$  with increasing silicon content towards the silicon layer deposited on top. These cones are clearly wider than those observed for  $\mu$ c-Si grain growth in *a*-Si in which the apex angle is 20–50° [Fejfar 2004, Kočka 2004].

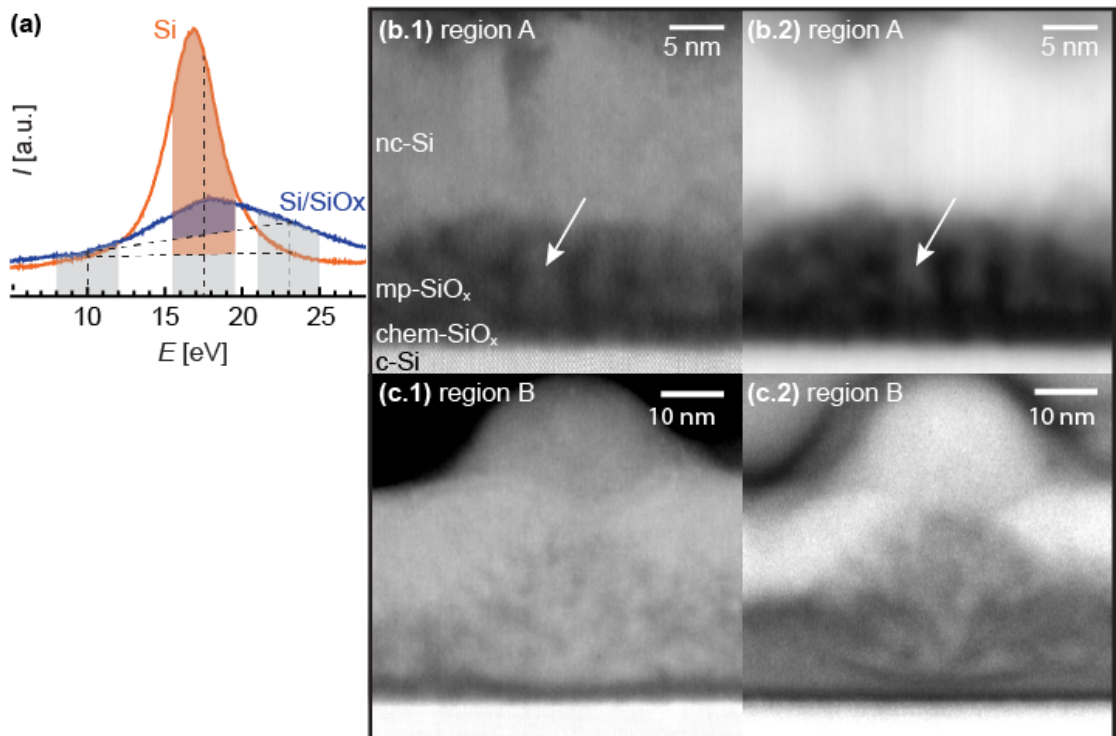


Figure 3.6 – (a) EEL spectra of *c*-Si and mixed Si/SiO<sub>x</sub> regions; (b1–2) STEM HAADF and corresponding EELS spectrum image of plasmons after background subtraction (colored region of the spectrum shown in (a) of region A in the as-deposited state; (c1–2) STEM HAADF and plasmons EELS spectrum image of the region B in the as-deposited state. Note the scale changes between (b) and (c) (adapted from [Stuckelberger 2016a]).

### 3.5.1 Growth model for the mixed-phase silicon oxide

The growth and nucleation of silicon on a silicon dioxide substrate is well described in [Claassen 1980] in which the formation of hemispherical clusters are observed as well.

From the cluster density at several temperatures the authors were able to draw conclusions on the incubation mechanism. In nucleation theory, a thin film starts growing with the formation of small clusters if the cohesive forces between the atoms within the cluster are stronger than the adhesive forces between adsorbed atoms (adatoms) and the substrate. With the arrival of atoms or molecules from the vapor, a small cluster begins to form which diffuses across the surface and grows or decays by the addition or loss of single atoms or molecules. If the cluster exceeds a critical size, it becomes energetically favorable to grow further.

From studies on nanocrystals obtained from homogeneously grown  $\text{SiO}_x$  films by a phase separation during a post-deposition annealing at  $> 900^\circ\text{C}$  [Schamm 2008, Iacona 2000, Boninelli 2005] the conclusion was drawn that phase separation in  $\text{SiO}_x$  layers into Si and  $\text{SiO}_2$  regions is energetically favorable but limited by the atom diffusion [Cuony 2011]. While high temperatures provide the additional energy for the phase separation in the literature cited above, a different energy source is needed for our films, which are deposited at a substrate temperature of  $200^\circ\text{C}$ . From the studies on plasma-deposited  $a\text{-Si}/\mu\text{c-Si}$  mixed-phase materials, it is known that hydrogen increases the structural order of the growing film via an increase of adatom diffusion length through surface heating and passivation of surface dangling bonds [Matsuda 1999, Fujiwara 2002, Sriraman 2002]. Furthermore, atomic hydrogen can relax strained bonds and etch off weakly bound atoms. All of these reactions increase the chance that silicon atoms find other coordinated silicon atoms, resulting in the formation of phase separated silicon clusters in the  $\text{SiO}_x$  matrix, a structure which was shown to be energetically favorable [Cuony 2011].

The  $\text{SiO}_x$  matrix is a complex structure and even the stoichiometric form of  $\text{SiO}_2$  is not completely understood yet. An interesting review on this material system can be found in [Salh 2011] from the point of view of defect creation in amorphous silicon dioxide  $a\text{-SiO}_2$ . The  $\text{SiO}_2$  structure is based on two tetrahedra, each having four oxygen atoms located at the four tips and a single silicon atom at the center as sketched in Figure 3.7. Each silicon atom has a valence charge of 4 in  $sp^3$  orbitals trying to acquire four electrons through sharing to complete its outermost energy shell. Each oxygen atom has two electrons to share with the silicon atoms so if four oxygen atoms surround one silicon atom, the silicon atom is complete and stable, whereas the oxygen atoms have one remaining electron, allowing them to connect to another silicon atom to form another tetrahedron. The Si–O bond energy is very high (4.5 eV) compared to the Si–Si bond (2.3 eV) and is approximately 50:50 ionic:covalent and lone-pair oxygen orbitals are present [Edwards 2000, Fanderlik 1991, Salh 2011]. The covalency favors the tetrahedral coordination of Si by O and maintains the O–Si–O bond angle ( $\phi$ ) very close to the ideal tetrahedral angle of  $109.5^\circ$ . The  $\text{SiO}_4$  tetrahedra can be treated in most cases as rigid units and can be linked together to form pairs, rings, chains, sheets, or frameworks. The

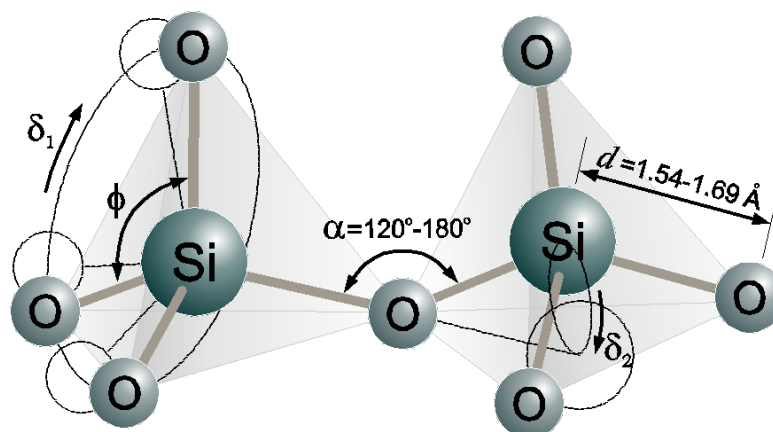


Figure 3.7 – Schematic of the regular silica structure. Several parameters define the structure: the Si–O bond length ( $d$ ), the tetrahedral angle ( $\phi$ ), the inter-tetrahedral bond angle ( $\alpha$ ), and the bond torsion angles ( $\delta_1, \delta_2$ ). (adapted from [Salh 2011])

inter-tetrahedral angle ( $\alpha$ ) is most probable at  $144^\circ$  but can vary between  $120^\circ$ – $180^\circ$  depending on the surrounding matrix with only a slight energy penalty [Fanderlik 1991, Salh 2011, van Santen 1991, Schutte 2011, Yuan 2003].

The role of hydrogen in silicon oxygen hydrides  $\text{SiOH}_n$  ( $n=0$ – $4$ ) is explained in a theoretical study presented by [Lucas 1993] investigating the ionization energies and enthalpies. They state that in silicon-oxygen systems a bonding of hydrogen to oxygen (O–H) is stronger and therefore preferential compared to bonding to silicon (Si–H).

As previously mentioned, the growth in our structure is strongly related to hydrogen. During the growth, hydrogen passivates dangling bonds, but it also breaks up existing Si–Si and Si–O bonds [Salh 2011]. We assume that for the growth in our structure most of the surface states are passivated by hydrogen. The lower bonding energy of Si–H over O–H results in an easier breakup of this bonding, resulting in the growth of silicon-rich phases. We observed a clearly enhanced deposition rate in region B compared to the surrounding region A. Since in hydrogen-supported growth regimes, an interplay between etching of bonds and forming of new ones takes place, we can't differentiate from the observations so far whether the varying deposition rate is due to enhanced growth in region B or due to enhanced etching in region A or due to a combination of the two. We can state that in region A the adatom diffusion length is in good balance with the rate of incoming atoms and the distance between the filaments, leading to a "homogeneous" mixed-phase layer. In region B, the clusters reach a critical size in the nucleation state; since they are energetically more favorable, they attract surrounding silicon atoms and deplete the surrounding oxide matrix. Therefore, the hydrogen content in region B would need to decrease locally to counteract this cluster formation.

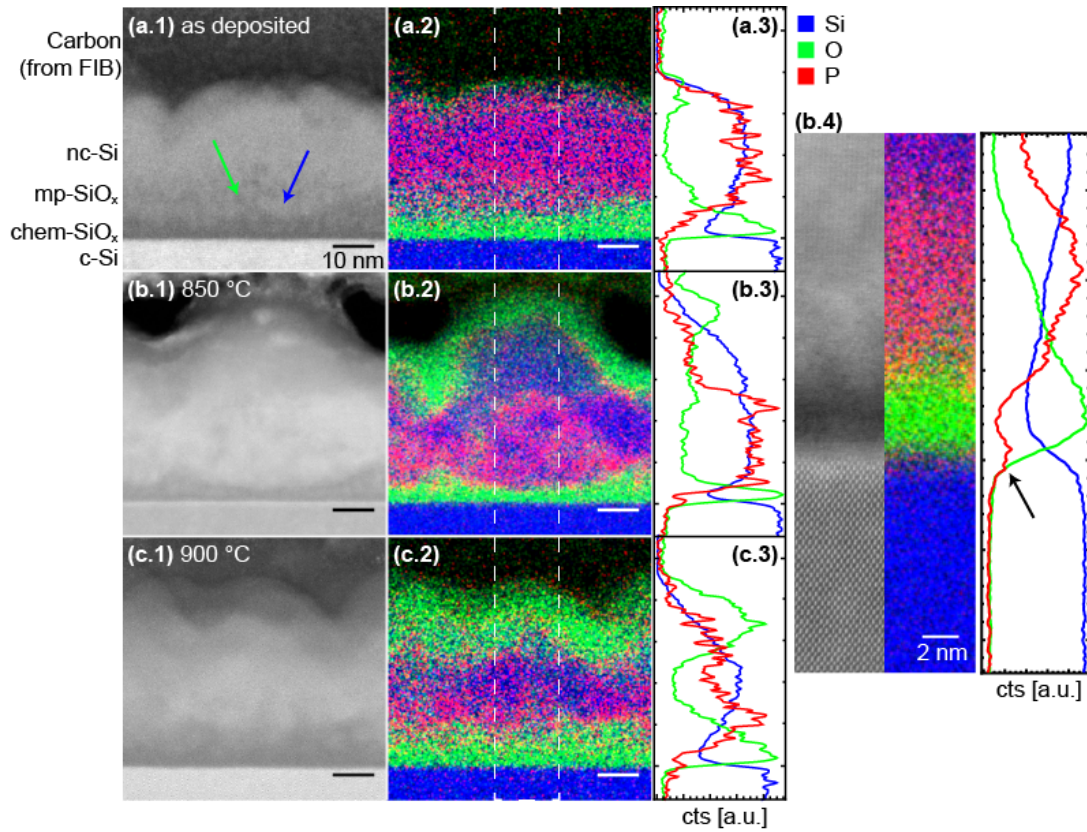


Figure 3.8 – (1) STEM HAADF images of the bilayer structure (a) as-deposited, (b) annealed at 850 °C and (c) at 900 °C along with (2) corresponding EDX maps and (3) line scans (EDX integrated signal of each element normalized to unity – in arbitrary units, extracted from the dashed region shown in 2). (b.4) The inset shows a high-resolution STEM HAADF image, EDX map and line scan of the wafer/contact interface at 850 °C [Stuckelberger 2016a].

### 3.5.2 Influence of thermal treatment

The structure and composition of this mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack is studied by STEM HAADF images and corresponding EDX maps and line scans of samples as-deposited and samples annealed at 850 °C or 900 °C, shown in Figure 3.8. In this investigation, the samples were deposited, annealed and characterized (see chapter 4 and [Stuckelberger 2016a]) before the TEM analysis was performed.

In Figure 3.8, a thin (~2 nm) continuous dark layer is distinguishable at the Si wafer interface in the HAADF image, which according to the EDX map corresponds to SiO<sub>x</sub>. As the chemically grown oxide layer is only ~1.2 nm thick, the remaining ~0.8 nm is explained by a contribution from the deposited mp-SiO<sub>x</sub>(n) layer. The EDX O signal is then observed to decrease over a range of ~15 nm as the layer evolves into phase separated layer of SiO<sub>x</sub> (dark regions – green arrow) and Si (brighter regions – blue arrow) with increasing Si content towards the top surface. In the upper 10–15 nm, a rather homogeneous silicon layer is visible, corresponding

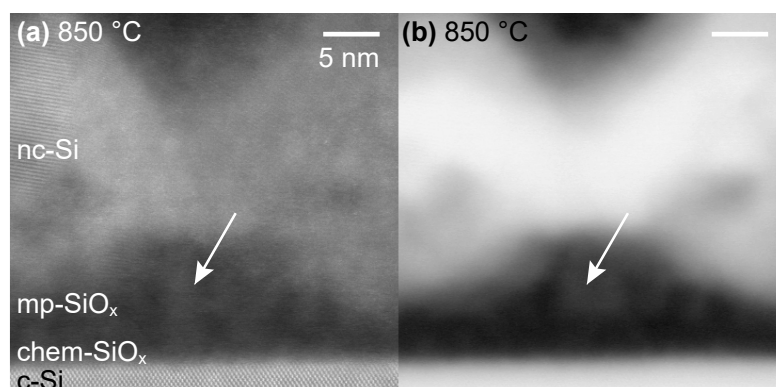


Figure 3.9 – (a) STEM HAADF and (b) corresponding EELS spectrum image of plasmons after background subtraction of region A in the sample annealed at 850 °C [Stuckelberger 2016a].

to the deposited nc-Si(n) layer. The P dopant appears to be homogeneously distributed in the nc-Si(n) phase after deposition of the layers. With annealing, the top surface is slightly oxidized, visible in Figure 3.8b–c. Whereas the wafer/chem-SiO<sub>x</sub> interface remains intact at 850 °C and 900 °C, the surface oxide layer is observed to thicken with increasing annealing temperature, probably due to residual oxygen present in the furnace, leading to detrimental effects as is explained in chapter 6. In addition, the P dopant distribution within the contact becomes inhomogeneously distributed during annealing. As observed for the structure annealed at 850 °C at larger magnification in Figure 3.8b.4, P has accumulated at the interface between the chemical SiO<sub>x</sub> and the wafer (black arrow), while the interfacial SiO<sub>x</sub> itself remains P depleted.

In order to investigate in detail the silicon phases within region A after annealing, low-loss EEL spectra were recorded in STEM. At the wafer surface, a 2–3 nm-thick continuous SiO<sub>x</sub> layer is distinguishable and still present after annealing at 850 °C (Figure 3.9a–b). The vertically oriented silicon-rich phases observed in Figure 3.6 remain present after annealing (arrow). On both sides of the image, part of region B is observed with a higher silicon content but still with oxygen phases included, whereas the bright top layer is well distinguishable with its high silicon content. Please remember that the resolution of the STEM EEL spectrum images is limited by the delocalization of the plasmon signal (on the order of 2 nm [Egerton 2009]) which is inherent to the technique.

The crystallinity of the layers was assessed by high-resolution TEM imaging. Figure 3.10 shows HRTEM micrographs of the contact in the as-deposited state and after annealing at 850 °C and 900 °C along with their Fourier transforms and colored inverse Fourier transforms of selected reflections. The results demonstrate a clear increase in crystallinity of the contact layer when annealed at 850 °C with grain sizes of up to ~10 nm, whereas annealing at 900 °C leads to larger grains of up to ~30 nm. This finding corroborates the high crystallinity observed by Raman spectroscopy shown in Figure 3.2. Moreover, the crystalline Si phases extend locally to about 3 nm of the wafer interface, building a percolating crystalline network through most of the contact structure. From a comparison with Figure 3.6 we conclude that the Si filaments in the

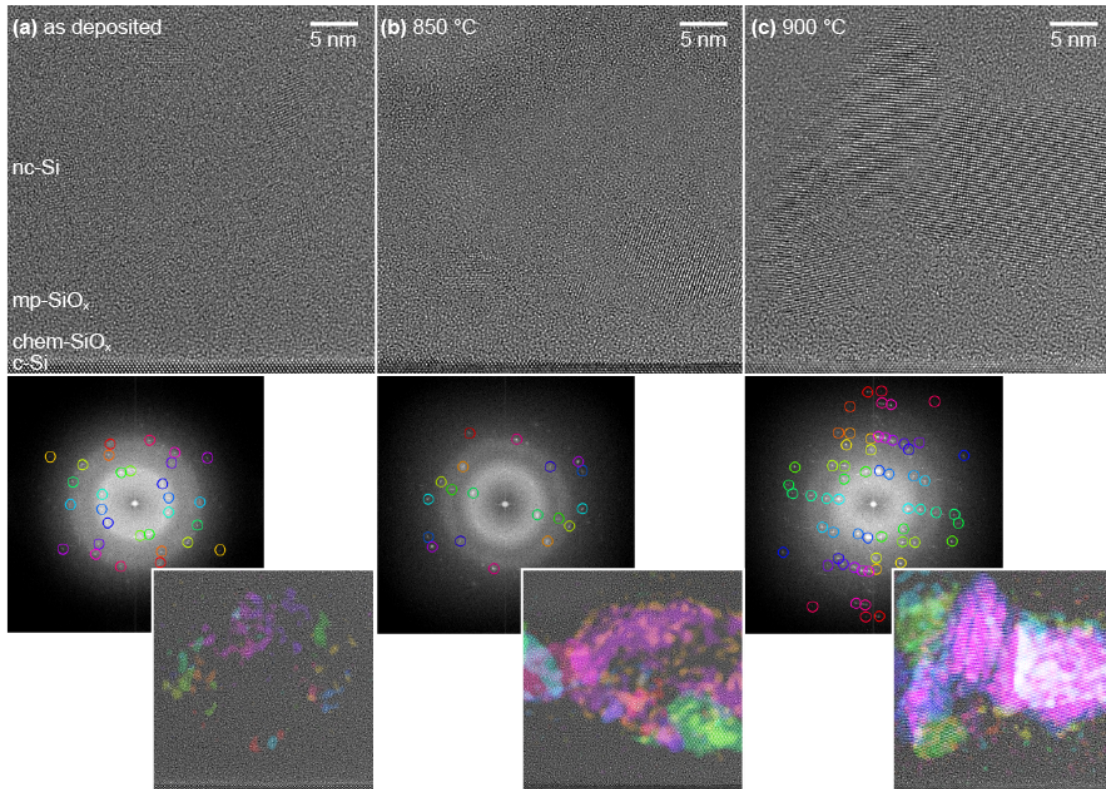


Figure 3.10 – (top) HRTEM micrographs, (middle) Fourier transforms and (bottom) inverse Fourier transforms of selected reflections colored and superimposed to the HRTEM image of the contact structure (a) as-deposited, (b) annealed at 850 °C and (c) annealed at 900 °C [Stuckelberger 2016a].

lower part of the deposited mp-SiO<sub>x</sub>(n) layer remain amorphous even after annealing, but silicon crystallites are observed further away from the interface and in the nc-Si(n) layer. At the interface with the wafer, the SiO<sub>x</sub> appears to remain amorphous.

### 3.6 Structural change observed in-situ during annealing

The structure and its change during annealing was investigated by TEM in HAADF mode and using EDX to detect movements of the species. To this end, the sample was mounted on the MEMS chip as shown in Figure 2.6 and heated to 900 °C, reproducing the temperature profile with a ramp of 10 °C/min. Two images were taken during the ramp up (at temperatures of 700 °C and 800 °C) and four images at isochronal intervals of 5 min during the dwell temperature of 900 °C as sketched in Figure 3.11. The measurements were performed at room temperature, but due to the specially designed sample holder, cooling down and heating up were achieved within one second.

In Figure 3.11 region B within the mp-SiO<sub>x</sub>(n) layer is shown in the as-deposited state (top

### 3.6. Structural change observed in-situ during annealing

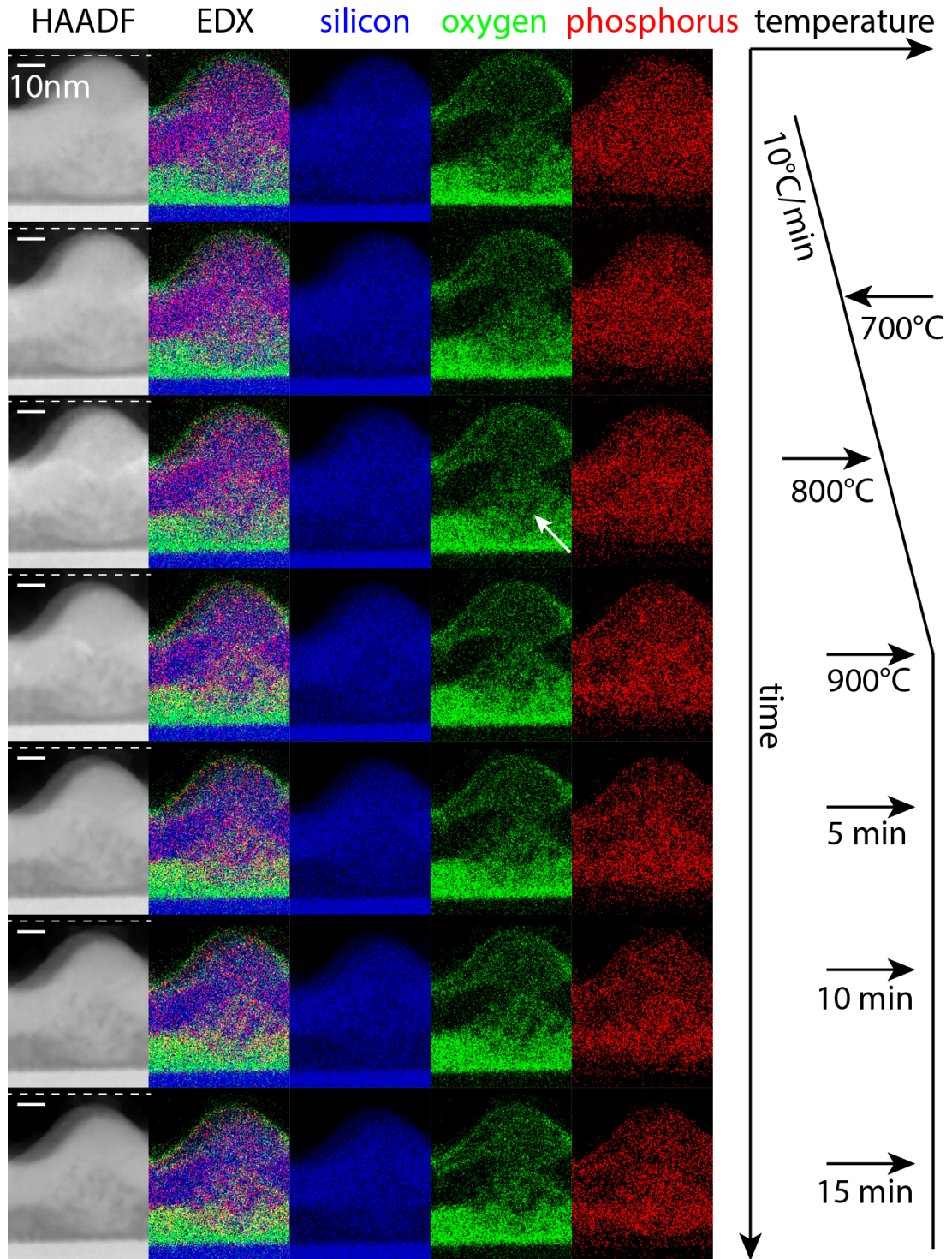


Figure 3.11 – STEM HAADF images and the corresponding EDX maps for the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack at variable states during the annealing process, indicated on the right.

row) in a STEM HAADF image (left column) and the corresponding EDX maps. Interestingly, first we detect a volume shrinkage of the layer stack of up to 10% with increasing temperature, indicated by the dashed line giving the thickness in the as-deposited state. This could be a measurement artifact induced by a bending of the sample or an effect of the electron beam. On the other hand, this could also be due to effusion of H or P or due to a rearrangement of the structure together with a crystallization.

The STEM HAADF images show that the silicon phases within the cone get more pronounced and separated from the oxide phases. This starts by 800 °C and continues until the end, and is also visible in the EDX maps. Within this cone, the maps of oxygen and silicon show that regions with less oxygen appear (arrow) and that they get more pronounced with time. We also observe a depletion of silicon with time in the region outside the cone within the mp-SiO<sub>x</sub>(n) layer, whereas the signal in the nc-Si(n) layer is increasing. This effect is driven mainly by a diffusion of the phosphorus atoms towards the wafer, depleting the top nc-Si(n) layer, as also observed in Figure 3.8 for ex-situ annealing.

Using a line scan (Figure 3.12), the silicon, oxygen and phosphorus concentration and distribution within the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack gets more visible and can be quantified

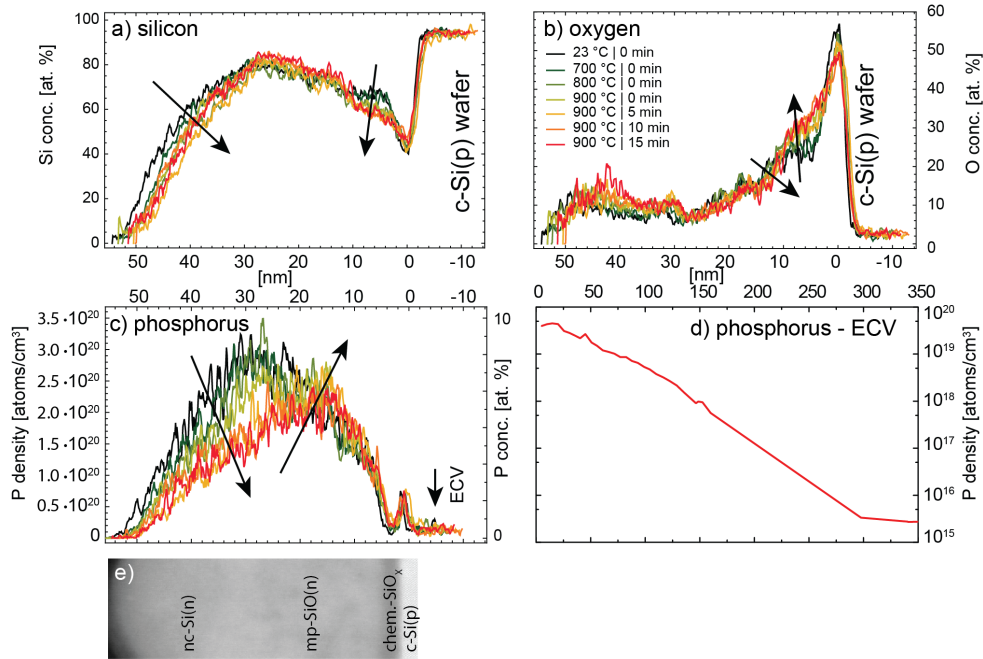


Figure 3.12 – The atomic concentration as a function of depth within the mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer structure measured by EDX in [at.-%] for (a) silicon and (b) oxygen, and quantified as density [atoms/cm<sup>3</sup>] for (c) phosphorus. The color code represents the evolution during in-situ annealing. In (d) the P profile within the wafer after ex-situ annealing is measured by ECV. (e) Micrograph showing the analyzed structure as guidance for the eye.

### 3.6. Structural change observed in-situ during annealing

(in at.%). The silicon line scan shows the shrinkage of the whole stack at the surface. Additionally a reduction of the silicon concentration within the mp-SiO<sub>x</sub>(n) stack is observed, especially when the temperature increases from 700 °C to 800 °C.

The inverse trend can be seen in the oxygen concentration. Within the mp-SiO<sub>x</sub>(n) layer, oxygen is quantified starting with 50–60 at.% at the chem-SiO<sub>x</sub>/wafer interface, decreasing gradually to around 25 at.% at the border with the nc-Si(n) layer in the as-deposited state. The slightly lower value at the interface than the expected 66 at.% for SiO<sub>2</sub> can be explained by a contribution from the wafer due to the sharp transition from Si to SiO<sub>2</sub>. With increased temperature, the concentration is slightly increased in the mp-SiO<sub>x</sub>(n) layer going along with a slightly decreased thickness leading to a more pronounced interface to the nc-Si(n) layer.

Interestingly, phosphorus is piling up at the *c*-Si surface below the chem-SiO<sub>x</sub> already in the as-deposited state; this does not change with annealing. We relate this to the presence of highly energetic P atoms in the plasma that penetrate the chem-SiO<sub>x</sub> during the early stages of deposition. In the as-deposited state, P is more highly concentrated in the nc-Si(n) layer than in the mp-SiO<sub>x</sub>(n) layer, but with increasing temperature and annealing dwell time, the P concentration close to the top surface is reduced. The P concentration in the mp-SiO<sub>x</sub>(n) layer increases with temperature due to a P diffusion towards the *c*-Si wafer. However, the interfacial chem-SiO<sub>x</sub> itself remains depleted of phosphorus as was seen also in the ex-situ measurements.

The amount of P losses in the layer stack is compared with the amount of P diffused to the *c*-Si wafer. Figure 3.12 shows the P concentration profile in the wafer beneath the interface as determined by electrochemical capacitance-voltage (ECV) measurements on a different part of the sample. Integration of the P content in the annealed films and of the diffusion profile suggests that approximately 10 times more P atoms effuse from the film than diffuse into the wafer. One possible reason for this discrepancy could be the measurement method of ECV which measures only active dopants, but not inactive clusters. However, this amount of inactive dopants would lead to a high density of recombination centers, which should influence the passivation quality of the sample, which we did not find in lifetime measurements. Another reason could be desorption into vacuum under the influence of the electron beam, accentuated by the high surface-to-volume ratio of the TEM lamella.

The nucleation and crystallinity of the layers were assessed by fast Fourier transforms (FFT) of the STEM HAADF images recorded during the in-situ annealing. In Figure 3.13, the STEM HAADF images are shown with the corresponding Fourier transforms and colored inverse Fourier transforms of selected Si- $\langle 111 \rangle$  reflections appearing at 3.2 nm<sup>-1</sup>, overlapped with the STEM image. Whereas in Figure 3.10 reflections representing crystal phases were detected already in the as-deposited state, this is not the case here using the STEM HAADF image, due to its lower sensitivity. At 700 °C, first reflections (and their mirror) appear in the nc-Si(n) layer. This means that at this temperature a phase change from amorphous silicon to more crystalline material has already taken place. This continues at 800 °C. More reflections appear

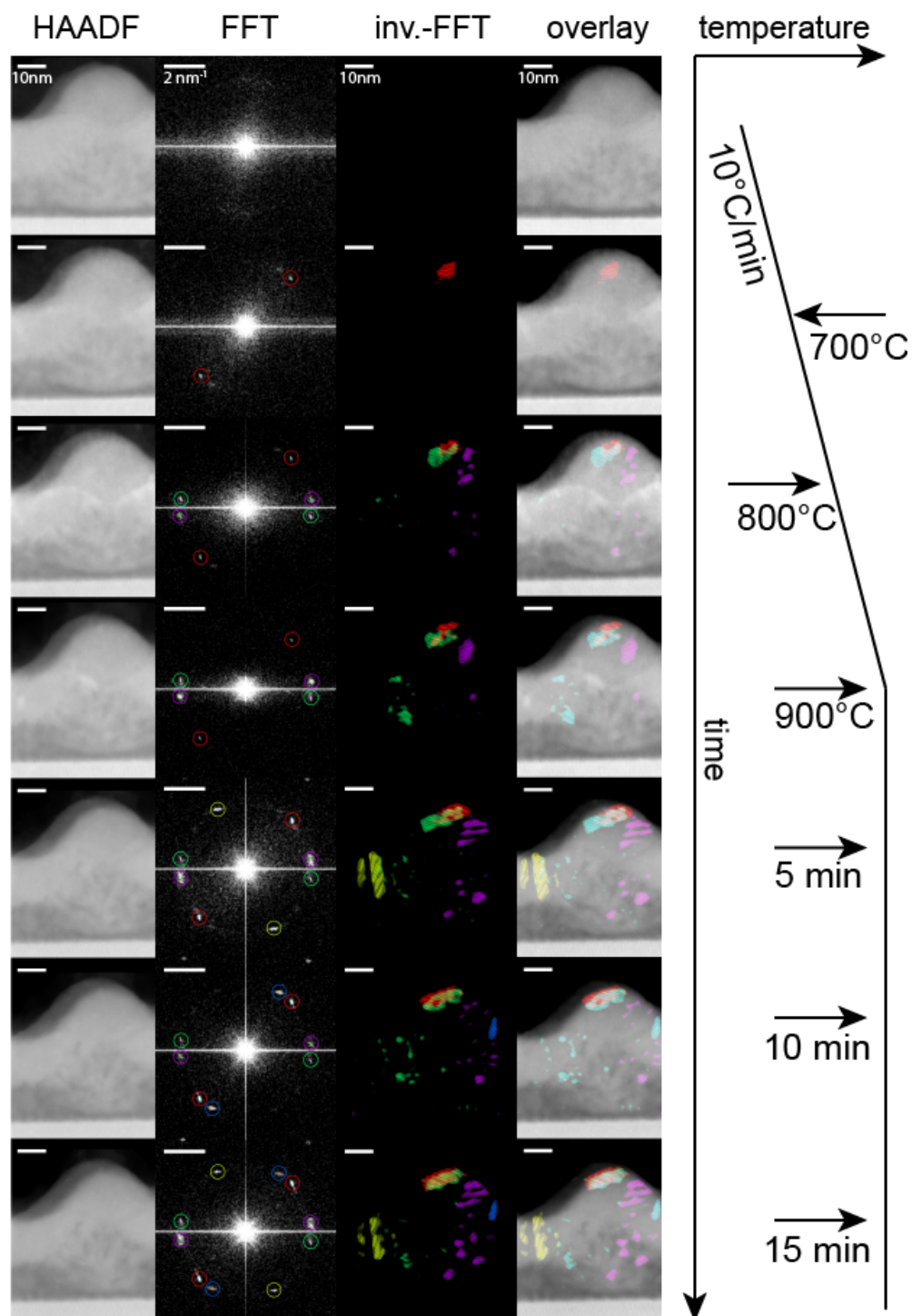


Figure 3.13 – STEM HAADF images, the corresponding fast Fourier transforms and colored inverse Fourier transforms of selected reflections overlapped with the STEM image at variable states during the annealing process, indicated on the right.

and the first crystalline phases of  $\sim 5$  nm are detected in the mp-SiO<sub>x</sub>(n) layer. By increasing the temperature further, more reflections appear in both layers. Some of the reflections disappear again with evolving temperature. We relate this to a measurement artifact due to a minimal tilt of the sample.

## 3.7 Surface roughness and oxide channel leading to chemical instability

Whereas the additional oxide in the mp-SiO<sub>x</sub>(n) layer and improved crystallinity of the nc-Si(n) layer targeted enhanced transparency, chemical stability is an issue during the integration of this layer stack into working devices as will be described in chapter 6. The reason for the chemical instability is directly related to the surface roughness and the additional oxide as can be seen in Figure 3.14a. In Figure 3.8b, the EDX O signal is plotted for a broader range of the sample. The above mentioned oxide layer growing at the surface during the annealing step is well visible. Together with the surface roughness resulting in regions that are noticeably thinner, this can lead to detrimental oxide channels (arrow) through the whole mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack, connecting the thermally grown surface oxide with the oxide phases at the wafer interface. When such a contact structure is further processed, especially during chemical etching in hydrofluoric acid (HF), there is a risk that the entire oxide channel may be etched, including the interfacial oxide.

This could result in complete loss of passivation, as was seen for a sample with a much thinner mp-SiO<sub>x</sub>(n) layer (15 s of deposition time) and a thicker nc-Si(n) layer (288 s) than the ones shown so far in this chapter. Figure 3.14b shows the TEM bright-field (BF) image together with corresponding Au, Si and O EDX maps of this sample after etching for 150 s in HF (1 vol.-%) (note the different scale bar). The sample got an Au coating before the TEM lamella preparation by FIB. Contrast variations in TEM BF images are related to differences in thickness (here approximately constant as a result of the FIB-preparation process) and atomic mass, with brighter regions highlighting positions of atoms with a larger mass, here mainly regions richer in Au when compared to Si- or O-rich regions. In the BF image, the wafer is covered with a thin bright layer and a porous, little connected structure on top. We assume that the HF etching removed most of the silicon oxide, leaving behind this porous silicon structure. Likely, a native oxide of 1–2 nm grew homogeneously on all silicon surfaces in the time between etching and coating with gold, which is part of the preparation of the TEM lamella. Taking the EDX maps as guidance, the thin layer on the wafer surface is indeed identified as silicon oxide and the bright porous structure as silicon.

Since the gold coating easily percolates through the porous structure all the way to the wafer surface, we can imagine that sputtering of the transparent conductive oxide (TCO) after an HF dipping would fill the porous structure very similarly, leading to a loss of passivation. In Figure 3.14c, a TEM BF image shows the porous silicon structure in higher magnification. It includes darker regions of only 1–2 nm diameter and shows smooth borders, which support

the explanation being related to etching.

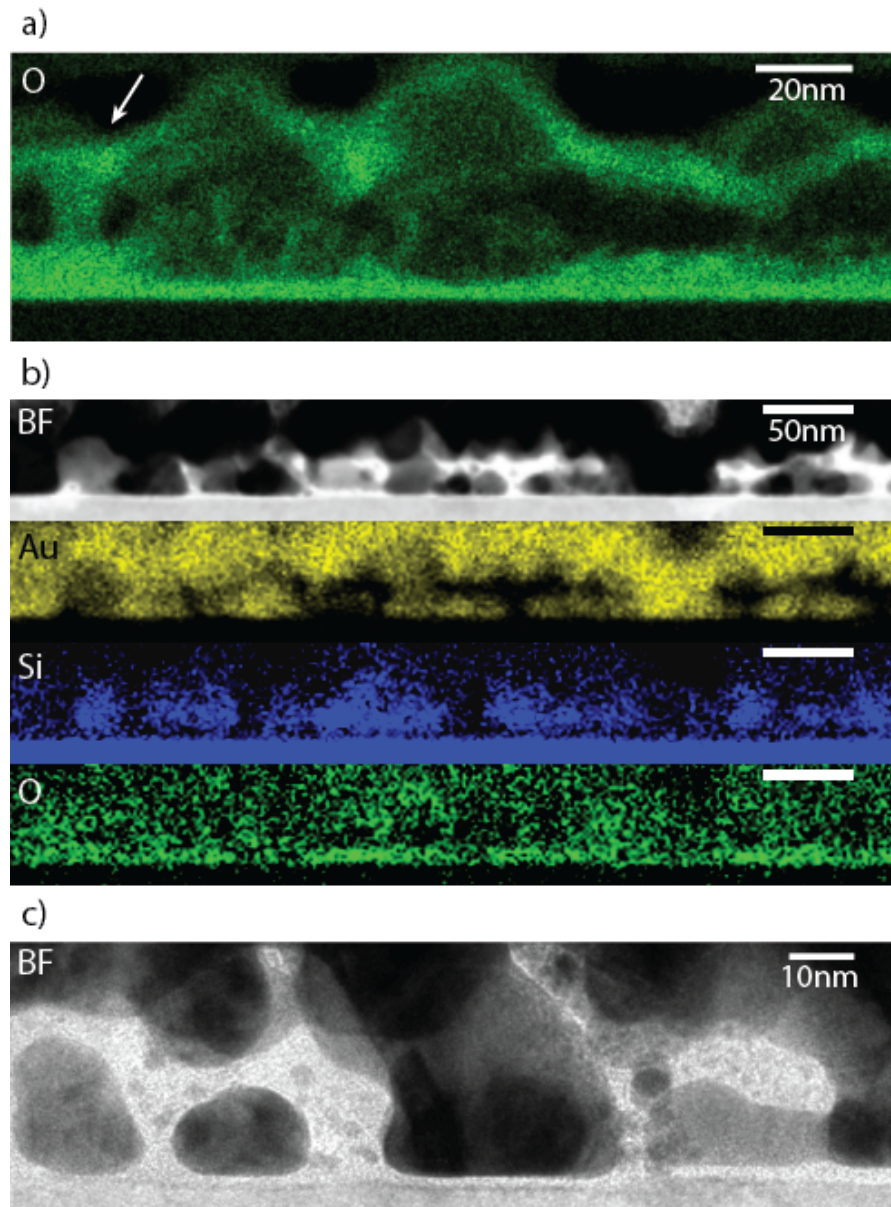


Figure 3.14 – (a) EDX oxygen map after annealing at 900 °C for 15 min shows an oxide channel (arrow) connecting the surface thermally grown oxide with the oxide of the mp-SiO<sub>x</sub>(n) layer and therefore the chem-SiO<sub>x</sub>. (b) TEM bright-field (BF) image with the corresponding Au, Si and O EDX map after 150 s of etching in HF (1 vol.-%). (c) TEM BF image with higher magnification.

### 3.8 Application to textured surfaces

Up to now, the structural characterization was done on polished surfaces since TEM on textured surfaces is a difficult task. However, since this passivating contact targets front-side application, the films should ultimately be applied to textured surfaces in final devices. In this case, the chemical stability may be even a bigger issue. A possible solution would be to replace the nc-Si(n) layer with an amorphous silicon layer (*a*-Si) to cover the mp-SiO<sub>x</sub>(n) layer more homogeneously. Another approach would be to implement an *a*-Si seed layer directly on top of the chem-SiO<sub>x</sub> to initiate incubation and growth of more homogeneously distributed silicon filaments. In SEM micrographs of a tilted top view after the annealing at 900 °C for 15 min, the surface is analyzed with focus on surface roughness and the formation of silicon clusters.

In the first column of Figure 3.15 (a.1–e.1), sketches of the analyzed layer stacks applied to textured surfaces are shown. The given thicknesses of *a*-Si(n) are calculated from deposition rates extracted from thicker layers on flat substrates using a scaling factor of 0.6 for use on textured surfaces. In Figure 3.15a.2, the bare mp-SiO<sub>x</sub>(n) layer extends over the full textured surface covering the tips and the valleys well despite a thickness of only 12 nm. Magnification (3.15a.3) reveals the formation of widely spread spherical clusters with diameters of up to ~30 nm for the bare mp-SiO<sub>x</sub>(n) layer. We relate these to the growth characteristic as seen in Figure 3.5 in region B.

Covering with a nc-Si(n) layer (~17 nm, Figure 3.15b.1–3, please note the different scale of image b.2) results in a higher density of spherical clusters with increased diameters of up to ~60 nm. Additionally in between the clusters, smaller spheres are formed that cover the whole surface.

Replacing the nc-Si(n) with an *a*-Si layer (~10 nm, Figure 3.15c.1–3) leads to a surface covered only partly by spherical clusters. The largest ones have a size of ~60 nm, i.e. similar to the coverage with a nc-Si(n) layer, but very few clusters are formed between the large ones, keeping some areas uncovered with spheres. A thicker *a*-Si layer (~20 nm, Figure 3.15d.1–3) changes the outcome very little; the larger clusters increase slightly to ~70 nm, but a large part of the surface stays uncovered. We explain the different growth of the nc-Si(n) and the *a*-Si(n) with the difference in the plasma regimes, having more hydrogen present for the growth of  $\mu$ c-Si. As explained earlier, the additional hydrogen helps to break up surface bonds and therefore also to create new nucleation sites.

Since the mp-SiO<sub>x</sub>(n) layer itself shows already a strong surface roughness with formed silicon clusters when deposited on an oxidized substrate, a seed layer of *a*-Si(n) (~4 nm) is introduced between the chem-SiO<sub>x</sub> and the mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer (Figure 3.15e.1–3). The surface roughness is decreased drastically and almost no clusters are formed. This example shows the strong dependence of layer growth on the substrate surface and the available nucleation sites.

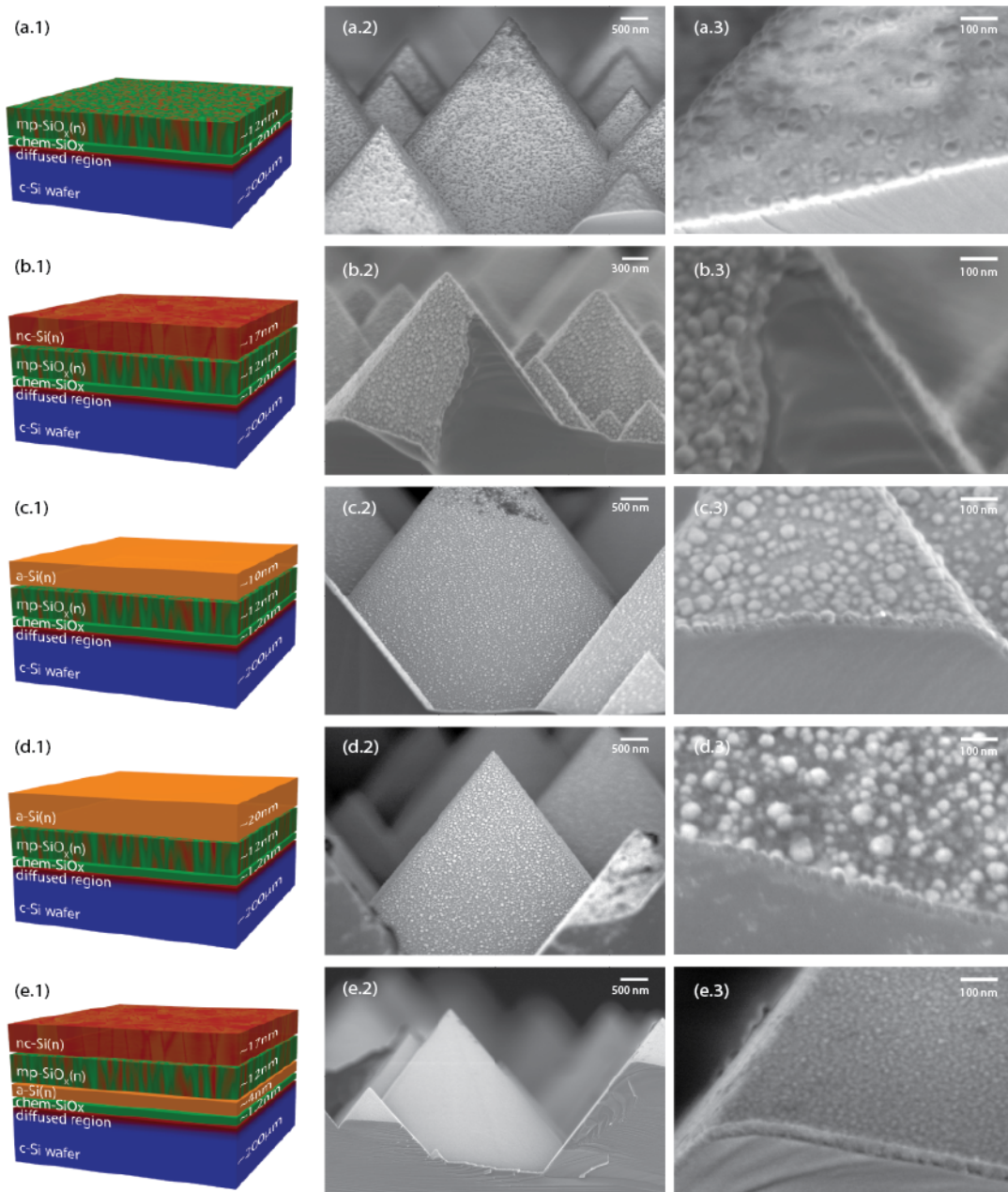


Figure 3.15 – (a.1)–(e.1) Sketches of varying layer stacks on top of the chem-SiO<sub>x</sub> with (a) only mp-SiO<sub>x</sub>(n), (b) mp-SiO<sub>x</sub>(n)/nc-Si(n), (c) replacing the nc-Si(n) layer with an *a*-Si layer (~10 nm), (d) increasing the thickness of the *a*-Si to ~20 nm, and (e) using an *a*-Si seed layer (~4 nm) below the mp-SiO<sub>x</sub>(n)/nc-Si(n). (a.2)–(e.2) SEM micrographs of the different layer stacks applied on textured surfaces and (a.3)–(e.3) magnifications thereof. Please note the different scale in (b.2).

### 3.9 Conclusion

In this chapter, the structure of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack in the as-deposited state and the structural changes that occur during thermal annealing were investigated in detail. Raman measurements revealed the high crystallinity of the nc-Si(n) layer for different thermal budgets as well as the related stress release within the layer.

In a detailed analysis by TEM, the mixed-phase nature of the mp-SiO<sub>x</sub>(n) layer was investigated and two different growth regimes were identified: Region A with columnar silicon-rich phases and region B forming cones with an apex angle of  $\sim 75^\circ$  which is responsible for the high surface roughness. Using in-situ annealing inside the TEM in EDX mode revealed the redistribution of elements undergoing the structural change with temperature. The silicon-rich phases within the oxide matrix remain mainly amorphous whereas the nc-Si(n) top layer starts to crystallize at 750 °C. The oxygen content in the mp-SiO<sub>x</sub>(n) layer was found to be 50–60% at the chem-SiO<sub>x</sub>/wafer interface and to decrease gradually to around 25% towards the border with the nc-Si(n) layer. With increased temperature a slight increase within the mp-SiO<sub>x</sub>(n) layer was observed going along with a slight decrease in its thickness. The phosphorus content in the nc-Si(n) layer was higher compared to the mp-SiO<sub>x</sub>(n) layer in the as-deposited state and is shifting towards the wafer with annealing, leading to a higher content in the mp-SiO<sub>x</sub>(n) layer after annealing. The intrinsic chem-SiO<sub>x</sub> remains depleted of P before and after thermal treatment.

Silicon oxide channels through the entire layer stack were found to be one of the main reasons for the high sensitivity to chemical treatments. On textured surfaces, replacing the nc-Si(n) layer with *a*-Si led to less homogeneous coverage due to increased surface roughness, whereas introducing a seed layer of *a*-Si between chem-SiO<sub>x</sub> and mp-SiO<sub>x</sub>(n) layer demonstrated a clear decrease in surface roughness.

Therefore, we propose three strategies to reduce the formation of oxide channels and to improve chemical stability. (i) A reduction of the hydrogen content in the deposition regime might suppress the nucleation. It would be necessary to take care that the vertical silicon phases of region A are grown so that the nc-Si(n) layer can cover well the smoother surface. (ii) An increase of nucleation sites should reduce the distances between cones, such that they merge before the desired film thickness is reached as was demonstrated with the *a*-Si seed layer. However, this would lead to an increased silicon content which is detrimental for the transparency. (iii) A reduction of the residual oxygen in the tube furnace would decrease the oxidation at the surface and would probably suppress the formation of channels.



## 4 Mixed-phase silicon oxide — Influence of thickness and annealing dwell temperature

This chapter compares the influence of the PECVD deposition time and annealing dwell temperature of the contact structure presented in chapter 3 on passivation and electrical transport. In section 4.2, the influence of the mixed-phase silicon oxide (mp-SiO<sub>x</sub>(n)) layer thickness on passivation is shown. Section 4.3 analyzes the impact of the annealing dwell temperature on passivation and on the electrical transport, which is investigated by repetitively etching the transfer length method (TLM) structures to confine the current pathway.

Some of the results of this chapter were published in 2016 in *Solar Energy Materials and Solar Cells* [Stuckelberger 2016a].

### 4.1 Experimental details

The passivating electron contact was investigated using symmetrical structures based on 280- $\mu\text{m}$ -thick double-side-polished 4-inch (100) 2.8  $\Omega\text{cm}$  silicon wafers doped with phosphorus or boron. After cleaning using standard wet chemistry a thin ( $\sim 1.2\text{ nm}$ ) SiO<sub>x</sub> layer was formed by wet chemical oxidation [Asuha 2003, Grant 2009] also referred to as chem-SiO<sub>x</sub>. Subsequently, a phosphorus-doped mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer structure of a mixed-phase silicon oxide (mp-SiO<sub>x</sub>(n)) layer and a nanocrystalline silicon (nc-Si(n)) layer was deposited by PECVD on both sides. The samples were then annealed for 15 min in a nitrogen (N<sub>2</sub>) atmosphere at temperatures from 750 °C to 950 °C. This was followed by 30 min of forming gas (FGA, 4% H<sub>2</sub> in N<sub>2</sub>) annealing at 500 °C to passivate electronic defects at the wafer–chem-SiO<sub>x</sub> interface [Aberle 1992].

The effective minority-carrier lifetime was measured by photoconductance decay and the method of Kimmerle [Kimmerle 2015] was applied to extract the emitter saturation current density ( $J_0$ ) at an excess charge-carrier density of  $1 \cdot 10^{16}\text{ cm}^{-3}$ . This leads to small variations for the values reported in this thesis compared to the publication [Stuckelberger 2016a] in which the method of Kane and Swanson [Kane 1985] was applied. The latter does not include effects of bandgap narrowing. The doping profile was analyzed by secondary-ion

mass spectroscopy (SIMS) with a Cameca ims 4f-E6. For electrical characterization, coplanar aluminum (Al) contacts were thermally evaporated, and the specific contact resistivity was measured using the transfer length method (TLM) as explained in section 2.3.8.

## 4.2 Influence of mp-SiO<sub>x</sub>(n) thickness on surface passivation

Here we present the effect of the additional silicon oxide phase in our passivating layer stack. The deposition time of the mp-SiO<sub>x</sub>(n) layer was varied while the total deposition time of the mp-SiO<sub>x</sub>(n)/nc-Si(n) stack was kept constant. The implied open-circuit voltage  $iV_{OC}$  and the emitter saturation current density  $J_0$  after annealing at 900 °C and an FGA are plotted in Figure 4.1 for both wafer polarities. Results of n+/n- and n+/p-junctions are shown in Figures 4.1a and 4.1b, respectively. The surface passivation is clearly enhanced with increasing mp-SiO<sub>x</sub>(n) thickness, especially for the n+/n-junctions. We explain the increased passivation by the additional oxide provided by the deposited mp-SiO<sub>x</sub>(n) layer supporting the stability of the chem-SiO<sub>x</sub> layer. Additionally, a thicker mp-SiO<sub>x</sub>(n) layer leads to a deeper in-diffused region within the wafer, measured by electrochemical capacitance voltage measurements (ECV), which could be the reason for the slightly increasing  $J_0$  for n+/p-junctions. More about using the mp-SiO<sub>x</sub>(n) layer as a doping source can be found in chapter 6.

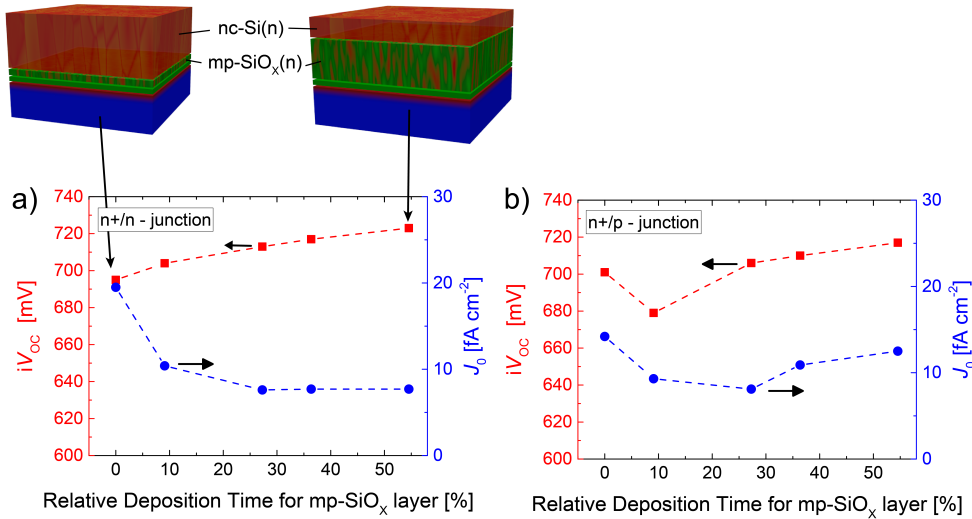


Figure 4.1 – Measured implied open-circuit voltage (red, left axis) and emitter saturation current density (blue, right axis) of the contact structure after an annealing at 900 °C and an FGA on (a) an n-type wafer and (b) a p-type wafer as a function of the relative deposition time of the mp-SiO<sub>x</sub>(n) layer compared to the deposition time of the whole bilayer stack, as sketched on top for the two extreme cases. (adapted from [Stuckelberger 2016a])

### 4.3 Effect of annealing temperature

#### 4.3.1 Surface passivation

We tested the tolerance of our contact structure to variations of dwell temperature for a stack with 36% mp-SiO<sub>x</sub>(n) relative deposition time. The dependence of  $iV_{OC}$  and  $J_0$  on annealing dwell temperature is shown in Figure 4.2 for n+/n-junctions (a) and n+/p-junctions (b). Excellent surface passivation is achieved for temperatures above 850 °C up to 950 °C for both n- and p-type wafers. In other studies, in which the doped Si layer was deposited directly on the chem-SiO<sub>x</sub> layer, the surface passivation was reported to degrade for annealing temperatures above 875 °C [Tao 2015] or 900 °C [Feldmann 2014b]. The authors attribute the degradation to a breakup of the chem-SiO<sub>x</sub> layer [Wolstenholme 1987].

This break-up can be explained with the phase separation  $\text{SiO}_x \longrightarrow (2-x)/2 \text{Si} + (x/2) \text{SiO}_2$  [Zacharias 2000] occurring in thin SiO<sub>x</sub> layers sandwiched between two Si phases, in conjunction with interstitial oxygen generation upon annealing of SiO<sub>2</sub> films on Si wafers in N<sub>2</sub> atmosphere ( $\text{SiO}_2 + \text{Si} \longrightarrow 2\text{SiO}$ ) [Devine 1996].

We explain the beneficial effect of the mp-SiO<sub>x</sub>(n) layer (Figure 4.1), as well as the excellent temperature stability of the passivation shown in Figure 4.2 with an enhanced structural stability of the interfacial chem-SiO<sub>x</sub> layer due to the larger amount of oxygen available from the deposited mp-SiO<sub>x</sub>(n) layer. With temperatures as high as 950 °C, an  $iV_{OC}$  of 723 mV and  $J_0$  of 9.0 fA/cm<sup>2</sup> is reached for the n+/p-junction and an  $iV_{OC}$  of 722 mV and a  $J_0$  of 5.3 fA/cm<sup>2</sup> for n+/n-junction. Please note that even without forming gas annealing (open symbols) these samples reach  $J_0$  values of 5.8 fA/cm<sup>2</sup> (n+/p-junction) and 9.5 fA/cm<sup>2</sup> (n+/n junction).

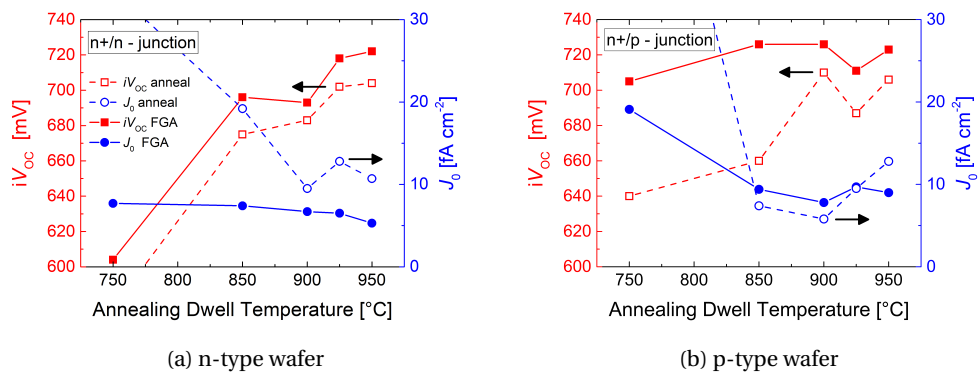


Figure 4.2 – Measured implied open-circuit voltage (red, left axis) and emitter saturation current density (blue, right axis) of the contact structure after annealing (open symbols) and after FGA (filled symbols) on (a) an n-type wafer and (b) a p-type wafer as a function of the annealing dwell temperature (adapted from [Stuckelberger 2016a]).

### 4.3.2 Doping profiles

Figure 4.3a shows the doping profiles measured by SIMS on the same p-type wafers. They reveal a similar behavior for all studied temperatures in the wafer to a depth about 20 nm from the wafer/chem-SiO<sub>x</sub> interface. Beyond that region, they show the expected behavior of deeper in-diffusion at higher temperatures, reaching a depth of 290 nm for annealing at 950 °C. To understand the electrical properties of highly P-doped regions, the surface concentration  $N_{\text{dop}}$  for the different temperatures can be related to the equilibrium concentration  $N_{\text{eq}}$  and the saturation concentration  $N_{\text{sat}}$  as reported by [Solmi 1996]. For 750 °C,  $N_{\text{dop},750} = 3.00 \cdot 10^{20}$  atoms/cm<sup>3</sup>, which is higher than  $N_{\text{sat},750} = 2.16 \cdot 10^{20}$  atoms/cm<sup>3</sup>, meaning that a considerable amount of P is incorporated in the form of SiP precipitates. These do not act as dopants, but they are recombination active. For 850 °C,  $N_{\text{dop},850} = 3.51 \cdot 10^{20}$  atoms/cm<sup>3</sup>, which lies in between  $N_{\text{sat},850} = 4.05 \cdot 10^{20}$  atoms/cm<sup>3</sup> and  $N_{\text{eq},850} = 2.84 \cdot 10^{20}$  atoms/cm<sup>3</sup>, denoting that some phosphorus is inactive but not recombination active. After annealing at 900 °C and higher,  $N_{\text{dop},950} = 3.92 \cdot 10^{20}$  atoms/cm<sup>3</sup> is  $\lesssim N_{\text{eq},950} = 3.89 \cdot 10^{20}$  atoms/cm<sup>3</sup>, indicating that the phosphorus is electrically active. Integrating the doping profiles and calculating the sheet resistance  $R_{\text{SH}}$  according to the mobility model of Klaassen et al. as demonstrated by [Klaassen 1992] gives values from 300 Ω/□ for 750 °C down to 160 Ω/□ for 950 °C.

Comparing SIMS profiles with ECV profiles (Figure 5.3) which measure only electrically active phosphorus, a clear difference is visible especially within the first 20 nm. Due to the  $N_{\text{sat}}$  values for this temperature, we don't expect the reason for this difference to be SiP precipitates but rather a measurement artifact of phosphorus atoms driven in during sputtering with

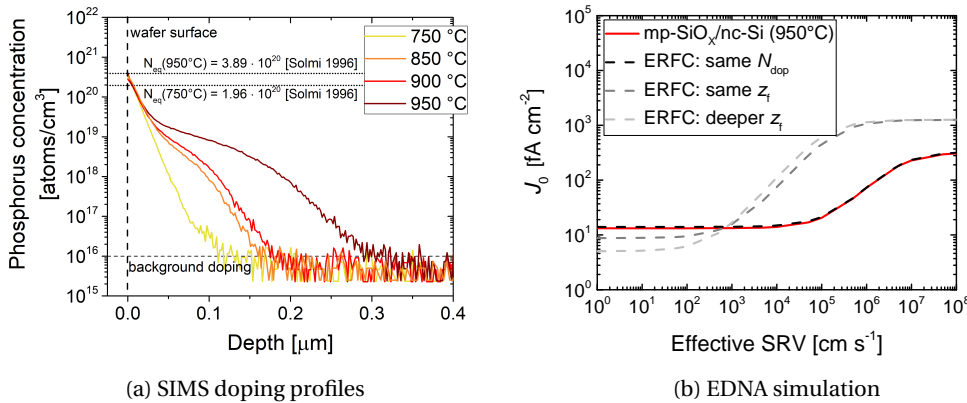


Figure 4.3 – (a) Doping profile measured by SIMS for different annealing dwell temperatures. (b) Simulation of charge-carrier recombination with EDNA [PVLighthouse 2018a] out of SIMS doping profiles of (a). The emitter saturation current density is plotted as a function of the surface recombination velocity for the 950 °C annealed sample in comparison with generated ERFC doping profiles for same  $N_{\text{dop}}$ , same  $z_f$  and a deeper  $z_f$  [Stuckelberger 2016a].

primary ions during the SIMS measurement. Additionally, the wafer resistivity, polarity and temperature of the nitric acid growing the chem-SiO<sub>x</sub> were different for these two sample series. Since we have observed that all these parameters influence the growth of the chem-SiO<sub>x</sub> in terms of thickness and density and therefore the diffusion through, we will not go more in detail here to investigate this difference. But more information can be found in section 6.4.

To separate the influence of intrinsic (Auger and radiative) recombination from recombination at the surface and to explore further the potential for optimization, we perform simulations of the highly-doped region using EDNA2 [PVLighthouse 2018a]. We assume zero Shockley-Read-Hall recombination in the bulk of the emitter (simulations of the effect of the SRH in the emitter can be found in section 5.5). For simplicity we model our structure as a highly-doped region in the wafer at a surface with an effective surface recombination velocity (SRV). This effective SRV thus lumps all recombination phenomena, independent of their exact mechanism and whether they occur at the interface between the wafer and the deposited layer stack, or within the layer stack.

The simulation shows that the effective SRV at the wafer/chem-SiO<sub>x</sub> interface is below 10000 cm/s for all annealing temperatures  $\geq 850^\circ\text{C}$ . Figure 4.3b shows  $J_0$  as function of the effective SRV for the doping profile of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack annealed at  $950^\circ\text{C}$ . For this case, the simulation shows the saturation current density is largely independent of surface recombination for SRV values of up to  $1 \cdot 10^4$  cm/s. The simulated value of  $J_0 = 13 \text{ fA/cm}^2$  matches our experimental result within the experimental error, which is estimated to be  $\pm 2 \text{ fA/cm}^2$ . Consequently, this contact is dominated by a reduction of the minority carriers by the in-diffused profile, suggesting that it cannot be improved further by optimizing the recombination properties of the interface or the layer stack.

To explore possibilities for further  $J_0$  reduction we compare with simulations for complementary error function (ERFC) doping profiles with the same sheet resistance. For the case of an ERFC doping profile with the same phosphorus surface concentration  $N_{\text{dop},950}$  and same sheet resistance as the sample annealed at  $950^\circ\text{C}$ , the junction depth  $z_f$  must be equal to  $0.03 \mu\text{m}$ . This value is similar to the measured profile, and the behavior in Figure 4.3b is barely distinguishable. Lowering the surface concentration but keeping the sheet resistance constant requires deeper junctions. For comparison, simulated ERFC doping profiles with a deeper junction ( $N_{\text{dop}} = 9.95 \cdot 10^{18} \text{ atoms/cm}^3$ ,  $z_f = 0.5 \mu\text{m}$ ) and the junction depth of our  $950^\circ\text{C}$  sample ( $N_{\text{dop}} = 2.08 \cdot 10^{19} \text{ atoms/cm}^3$ ,  $z_f = 0.29 \mu\text{m}$ ) are added to Figure 4.3b. The modeled results suggest that lower  $J_0$  values can be attained by combining a lower surface concentration and an increased junction depth. This might be accomplished by decreasing the phosphorus concentration in the deposited layer and increasing the annealing dwell time. However, Figure 4.3b shows that this strategy would come at the cost of the  $J_0$  being more sensitive to the surface recombination properties. Our experimental profile has the advantage that it provides good passivation even in the case of comparatively strong surface recombination.

### 4.3.3 Electrical characterization

We extracted the specific contact resistivity  $\rho_{c,TLM}$  and sheet resistance  $R_{SH,TLM}$  for structures on p-type wafers and n-type wafers annealed at 900 °C with the transfer length method (TLM) using the Berger structure [Berger 1972]. According to the SIMS measurements shown in Figure 4.3a these samples feature a highly P-doped region in the wafer which extends about 200 nm underneath the deposited layer stack, which is also highly P-doped. Generally, current could flow from one contact to the other through the deposited layer stack, specifically through the topmost nc-Si(n) layer, and also through the in-diffused region in the wafer. In the case of an n-type wafer, the lowly-doped wafer itself can additionally contribute to conductance. To investigate the current pathway, the region between the TLM pads was repetitively etched for 2 s in a  $SF_6/O_2/Ar$  plasma using the aluminum pads as an etching mask, and the samples were measured after each etch process by TLM and atomic force microscopy (AFM) to determine the etched depth. In Figure 4.4a and 4.4b a representative behavior of  $\rho_{c,TLM}$  and  $R_{SH,TLM}$  as a function of etching depth is shown for n+/n and n+/p-junctions, respectively. The specific contact resistivity and the sheet resistance both increase upon etching for etch depths exceeding 30 nm for n+/p-junction and 50 nm for n+/n-junction, respectively. Please note that the data points are unequally spaced despite of the constant etch time, which is caused by the lower etch rate of  $SiO_x$  compared to Si. Consequently, the region with closely spaced data points corresponds approximately to the  $SiO_x$  layer (low etch rate).

Both for the n+/n and n+/p-junction,  $\rho_{c,TLM}$  and  $R_{SH,TLM}$  do not change upon etching of the deposited layer (the first 30 nm). This indicates that the deposited layer does not contribute to lateral current transport, but that current rather flows through the wafer including the in-diffused region.

The sheet resistance on the n+/n-junction is increasing from 45  $\Omega/\square$  before etching to a

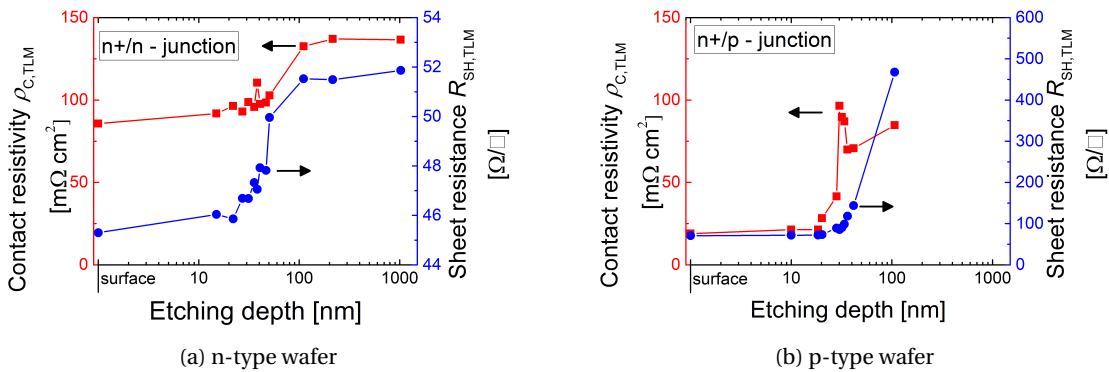


Figure 4.4 – Specific contact resistivity  $\rho_{c,TLM}$  and sheet resistance  $R_{SH,TLM}$  for the passivating contact annealed at 900 °C, as a function of the etching depth for (a) n+/n-junction and (b) n+/p-junction [Stuckelberger 2016a].

### 4.3. Effect of annealing temperature

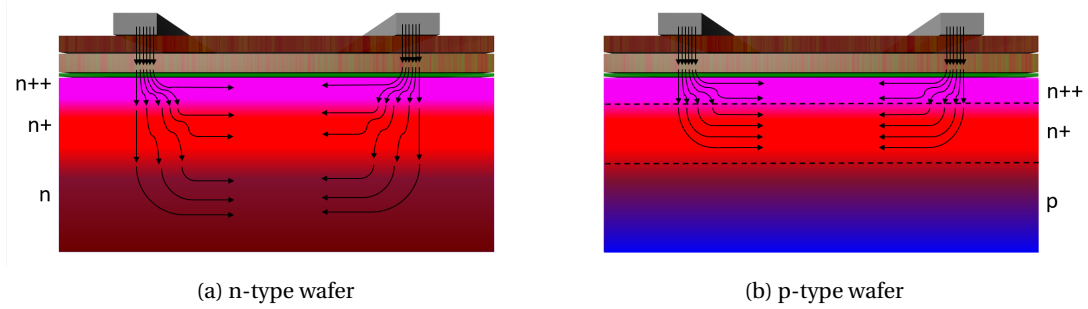


Figure 4.5 – Qualitative illustration of the current pathway during TLM measurements for (a) an n+/n-junction and (b) an n+/p-junction, indicating the current spreading and the electrically effective area [Stuckelberger 2016a].

constant value of  $52 \Omega/\square$  after etching over 200 nm which matches fairly the total calculated sheet resistance of the wafer together with the diffused region at the opposite side of the contacts of  $68 \Omega/\square$  (calculated from the wafer thickness  $280 \mu\text{m}$ , background doping  $1.66 \cdot 10^{15} \text{ atoms/cm}^3$  and ERFC profile  $N_{\text{dop},900} = 2.82 \cdot 10^{20} \text{ atoms/cm}^3$ ,  $z_f = 0.027 \mu\text{m}$ ). This small increase indicates the loss of the current pathway within the surface-near region of the wafer below the chemical oxide. For the n+/p-junction the sheet resistance is  $70 \Omega/\square$  before etching and is increasing sharply as soon as the diffused region starts to be etched. For etch depths exceeding 100 nm the current pathway is too resistive to be measured. Consequently, for the n+/p-structure, the lateral conductive channel is the in-diffused n+ region only, and additional current flow through the wafer is effectively blocked by the n+/p-junction.

The specific contact resistivity of the n+/n-junction remains largely unchanged while etching the layer stack, but slightly increases from  $86 \text{ m}\Omega \text{ cm}^2$  to  $137 \text{ m}\Omega \text{ cm}^2$  once the layer stack

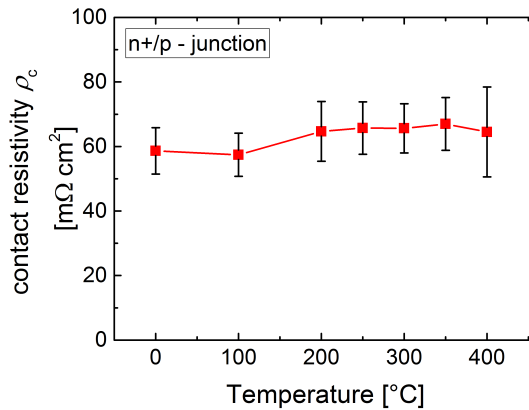


Figure 4.6 –  $\rho_{c,\text{TLM}}$  is plotted as a function of post-metallization sintering temperature for an n+/p-junction [Stuckelberger 2016a].

is etched and also the diffused region within the wafer is removed. For the n+/p-junction, a similar but more pronounced behavior is observed with an increase from  $19 \text{ m}\Omega\text{cm}^2$  to  $85 \text{ m}\Omega\text{cm}^2$ . Please note that while the structures on n+/p-junctions fulfill the assumptions made in the TLM theory, the latter is not strictly valid for the n+/n-junction because the conductive "channel" includes the wafer and is thus comparatively thick.

Interestingly, in case of the n+/p-junction, the increase of the specific contact resistivity is more pronounced than for the n+/n-junction and occurs at lower etch depth than the increase of the sheet resistance. The n+/n-junction shows opposite behavior, the sheet resistance starts to increase at an etch depth of 30 nm, but  $\rho_{c,\text{TLM}}$  starts to increase only for etch depths of  $> 60 \text{ nm}$ . This hints at current spreading in the first 20 to 40 nm in the wafer which are doped to  $> 2 \cdot 10^{19} \text{ atoms/cm}^3$  (cf. Figure 4.4a), before the current is laterally transported over the entire depth of the conductive channel. The current flow is qualitatively sketched in Figure 4.5. Current spreading increases the electrically effective area of the contact. Once the spreading is reduced (here by etching away the conductive channel) the contact resistivity increases. We explain the sharper increase of  $\rho_{c,\text{TLM}}$  in case of the n+/p-structures with current spreading being more pronounced than for n+/n-junctions because the current is confined to a thin conductive channel and can spread only on the topmost first nm, see Figure 4.5b. In the n-type wafer, on the other hand, current is transported over the entire wafer thickness and the spreading can thus take place over the entire n+ region, as depicted in Figure 4.5a.

We also performed sintering experiments to investigate the conditions required for establishing a good contact. Samples with the same structure as discussed above (Figure 4.4b) were repeatedly sintered for 15 min on a hot plate in air at temperatures up to  $400^\circ\text{C}$  and measured after each sintering step. We find a value of  $59 \text{ m}\Omega\text{cm}^2$  before the first sintering step. However, the specific contact resistivity could not be lowered by sintering for this contact structure.

Using Equation 1.19 the influence of the contact resistivity on cell level can be estimated. Planar cells fabricated with this contact structure perform with a short-circuit current of  $35.0 \text{ fA/cm}^2$  and an open-circuit voltage of 690 mV. A contact resistivity of  $19 \text{ m}\Omega\text{cm}^2$  (n+/p-junction) or  $86 \text{ m}\Omega\text{cm}^2$  (n+/n-junction) result in a fill factor loss of  $\sim 0.10\%$  or  $\sim 0.49\%$ , respectively. By using a textured cell the current is increased ( $J_{\text{SC}} = 40 \text{ mA/cm}^2$ ) which enhanced the effect on the fill factor to  $\sim 0.12\%$  (n+/p-junction) and  $\sim 0.54\%$  (n+/n-junction), respectively.

Nevertheless, the TLM measurements presented within this section show that this mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack provides not only an excellent surface passivation but also a promising contact resistivity for a sufficient transport of the majority carriers for full-area contacts.

## 4.4 Conclusion

In summary, this chapter showed the beneficial effect of the addition of the mp-SiO<sub>x</sub>(n) layer between the chemical oxide and the nc-Si(n) layer to enhance thermal stability of surface passivation. In-diffusion of phosphorus creates a doping profile with surface concentration of  $3.92 \cdot 10^{20}$  atoms/cm<sup>3</sup>. Without any hydrogenation for defect passivation, emitter saturation current densities of 12.8 fA/cm<sup>2</sup> (n+/p-junction) and 10.7 fA/cm<sup>2</sup> (n+/n-junction) are reached. With forming gas annealing, an excellent surface passivation is achieved with emitter saturation current densities of 9.0 fA/cm<sup>2</sup> for n+/p-junction and 5.3 fA/cm<sup>2</sup> for n+/n junctions, respectively, yielding specific contact resistivities between 19 mΩ cm<sup>2</sup> and 86 mΩ cm<sup>2</sup>.

Additional insight into the current pathway of this passivating contact is gained by monitoring  $\rho_{c,TLM}$  and  $R_{SH,TLM}$  as the contact layers and the surface of the underlying wafer are gradually etched off. We find that the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack does not significantly contribute to the measured resistivity.



## 5 Mixed-phase silicon oxide — Influence of initial doping concentration and anneal dwell time

In this chapter, we investigate the relation between the doping profile and screening of minority carriers, Auger recombination, and interface recombination, all of which increase monotonically with dopant concentration at the surface [del Alamo 1985, King 1990, Cuevas 1996]. The properties of the junction are analyzed for varying the annealing time and initial doping concentrations of the deposited stacks and different annealing times. The underlying effects are separated by investigations before and after hydrogen passivation in a forming gas anneal (FGA) and supported by simulations performed with EDNA2 [PVLighthouse 2018a].

Additionally, we apply an electrode of sputtered indium-tin-oxide (ITO) in order to finalize a solar cell structure and to study possible effects on passivation quality for samples dominated by different recombination mechanisms.

Some of the results of this chapter were published in 2018 in *IEEE Journal of Photovoltaics* [Stuckelberger 2018].

### 5.1 Experimental details

The investigations of passivating electron-selective contacts shown in this chapter are based on 200- $\mu\text{m}$ -thick 4-inch  $\langle 100 \rangle$ -oriented 10  $\Omega\text{cm}$  phosphorus-doped n-type FZ silicon wafers. After cleaning using standard wet chemistry a  $\sim 1.2\text{ nm}$  thin  $\text{SiO}_x$  layer was formed on both sides by wet chemical oxidation [Asuha 2003, Grant 2009] also referred to as chem- $\text{SiO}_x$ . Subsequently, a phosphorus-doped mp- $\text{SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  bilayer structure of a mixed-phase silicon oxide (mp- $\text{SiO}_x(\text{n})$ ) layer and a nanocrystalline silicon (nc-Si(n)) layer was deposited by PECVD on both sides. The phosphorus concentration during deposition was varied and given as relative phosphine ( $\text{PH}_3$ ) flux compared to the maximal flux used in the previous chapter. The symmetric structures were annealed at 900  $^\circ\text{C}$  for four different dwell times, namely 15, 30, 60, and 90 min, resulting in different doping profiles with different surface concentrations. The annealing was followed by a forming gas anneal (FGA, 4%  $\text{H}_2$  in  $\text{N}_2$ ) for

30 min at 500 °C to passivate electronic defects at the *c*-Si/chem-SiO<sub>x</sub> interface. In order to remove native oxide that grew unintentionally during the annealing steps, the samples were dipped in diluted hydrofluoric acid (HF, 1 vol.-%) until the surfaces became hydrophobic. Finally, ITO was sputtered on both sides, and the samples were cured at 210 °C for 30 min in air.

The effective minority carrier lifetime was measured by photo-conductance decay (PCD) applying the method of Kimmerle [Kimmerle 2015] to extract the emitter saturation current density  $J_0$  at an excess carrier density corresponding to ten times the base doping. The error in this  $J_0$  measurement including inhomogeneity over the wafer area is smaller than 10%.

For the proof-of-concept solar cells we prepared first the passivating electron contact on the front side of a planar <100>-oriented 1 Ωcm phosphorus-doped 200-μm-thick n-type FZ silicon wafer. In this case, the rear side of the cell was only protected by the chem-SiO<sub>x</sub> during the annealing step, which was removed by a one sided HF etch using the Single-droplet-method (see section 2.1.5). Then we applied a silicon heterojunction (SHJ) hole-selective contact to the rear side by applying a thin passivation layer of intrinsic amorphous silicon (*a*-Si(i)) and contact layer of boron-doped *a*-Si(p) layer. An HF (1 vol.-%) dip until the n-side was hydrophobic was followed by ITO sputtering on front and rear through 2.2 x 2.2 cm<sup>2</sup> shadow masks that were aligned to cover the same area. Different from lifetime samples, thicknesses of 80 nm and 130 nm were used for the front and the rear-side of the solar cells, respectively. The solar cells were then finished by sputtering a silver reflector on the rear side and screen printing an Ag grid on the front side, followed by curing for 30 min at 210 °C in a belt furnace. A sketch of the final layer stack of our device is illustrated in Figure 5.8 and more detailed information about the fabrication process for the hybrid cells can be found in section 2.2.1.

The external quantum efficiency (EQE) was measured between the metal fingers by a system that was built in-house, using a calibration with a certified SHJ cell. Together with the reflectance (R) measured in a Perkin-Elmer Lambda 950 spectrometer, the internal quantum efficiency (IQE) was calculated.

## 5.2 Surface passivation

Figure 5.1 shows the measured emitter saturation current density ( $J_0$ ) as a function of relative phosphine (PH<sub>3</sub>) flow during deposition (maximal used PH<sub>3</sub> flow is set to 1) after applying four different anneal dwell times at 900 °C. The  $J_0$  is measured directly after the annealing process and then again after the FGA. The error in this  $J_0$  measurement including inhomogeneity over the wafer area is smaller than 10%. The open symbols show that even without the FGA, remarkably good passivation with  $J_0$  values below 20 fA/cm<sup>2</sup> can be attained for the higher PH<sub>3</sub> flows. For short dwell times of 15 and 30 min, a relative flow of 0.77 during deposition leads to best passivation. For longer dwell times, on the other hand, a relative flow of 0.56 shows the best behavior, leading to a value of  $J_0 = 12.4$  fA/cm<sup>2</sup>.

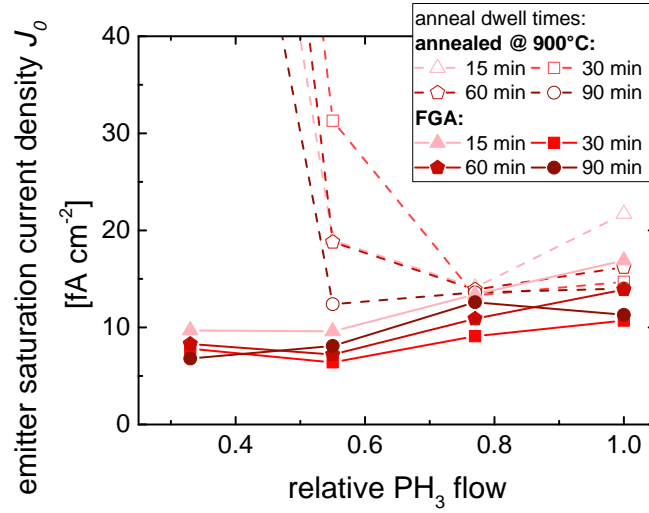


Figure 5.1 – Emitter saturation current density  $J_0$  as a function of the relative  $\text{PH}_3$  flow used during PECVD for four different anneal dwell times directly after the annealing (dashed lines, open symbols) and after a hydrogenation by FGA (lines, filled symbols) [Stuckelberger 2018].

Full symbols show that the FGA is especially effective to improve  $J_0$  of samples with low phosphine flow, suggesting that their behavior is dominated by defects at the chem- $\text{SiO}_x$ /wafer interface. With FGA, the optimum is reached for a relative  $\text{PH}_3$  flow of 0.56 and a dwell time of 30 min, resulting in  $J_0 = 6.4 \text{ fA/cm}^2$ .

Samples with high phosphine flows are insensitive to FGA, suggesting that the overall recombination rate is dominated by the in-diffused region which is little affected by hydrogenation. The increase of  $J_0$  for relative flows higher than 0.56 (after FGA) can be explained with an increasing contribution from Auger recombination.

These results show different pathways to improve surface passivation, either by low initial doping concentrations combined with long annealing and hydrogenation or high initial doping concentrations, for which a short annealing dwell time is sufficient and an FGA is not necessary.

### 5.3 Electrical characterization

The specific contact resistivity  $\rho_c$  for this sample series is shown in Figure 5.2 as a function of relative  $\text{PH}_3$  flow and for the four different anneal dwell times at 900 °C before metallization. Error bars denote the deviation over three TLM samples prepared for each condition. For both contact types, high doping is needed for low contact resistivity, but evaporated aluminum (blue open symbols) yields lower values than sputtered ITO with silver paste (ITO/Ag, red filled symbols).

For low doping of 0.33 relative  $\text{PH}_3$  flow, the samples were hardly measurable giving  $\rho_c$  values of above  $5 \Omega \text{cm}^2$ . For a relative  $\text{PH}_3$  flow of 0.56,  $\rho_c$  is decreasing with longer anneal dwell time and only for 90 min annealing and contacting with aluminum  $\rho_c$  gets below  $500 \text{ m}\Omega \text{cm}^2$ . For a relative  $\text{PH}_3$  flow of 0.77,  $\rho_c$  is not following a trend with anneal dwell time, only a clear beneficial behavior of aluminum over ITO/Ag is observed leading to  $\rho_c$  of  $\sim 200 \text{ m}\Omega \text{cm}^2$ . For comparison, the contact resistivity of  $a\text{-Si(i)}/a\text{-Si(n)}$  SHJ contacts (see the dashed line in Figure 5.2) is reported to be ca.  $300 \text{ m}\Omega \text{cm}^2$  [Nogay 2016a]. For a higher relative  $\text{PH}_3$  flow of 1.00,  $\rho_c$  with ITO is also below  $500 \text{ m}\Omega \text{cm}^2$  for some conditions. Using aluminum,  $\rho_c$  is lower for shorter anneal dwell time with an optimum at 15 min, leading to an average  $\rho_c$  of  $26 \text{ m}\Omega \text{cm}^2$ . An explanation for the lower  $\rho_c$  for Al compared with ITO could be a difference in their work function. For ITO, the work function varies with stoichiometry, organic contamination, and oxidation type [Centurioni 2003, Harvey 2006]. A higher effective barrier for ITO would broaden the depletion region and lead to a decrease in tunnel probability [Schroder 1984]. However, the surfaces of ITO as well as of silicon are prone to Fermi level pinning [Klein 2010, Allen 1962], making it difficult to predict the extend of the effective barrier. There is also the possibility that presence of oxygen during the ITO sputtering oxidizes the surface of the nc-Si(n) resulting in an additional barrier.

As can be seen from the error bars, the samples with ITO should be treated with caution and are reported here to give a more complete picture and to show that a charge carrier transport with low  $\rho_c$  is possible through this mixed-phase  $\text{SiO}_x$  layer stack, but only by using higher

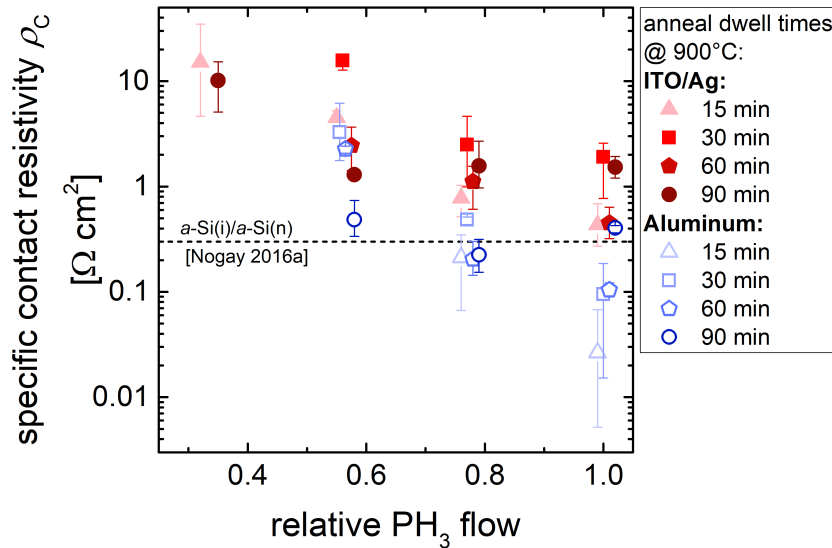


Figure 5.2 – Specific contact resistivity  $\rho_c$  as a function of the relative  $\text{PH}_3$  flow used during PECVD for four different anneal dwell times extracted from TLM measurements using ITO/Ag (red filled symbols) or aluminum (blue open symbols) as metallization. The data points are moved slightly in the horizontal direction for better readability [Stuckelberger 2018].

doping concentrations. Since a  $J_0$  value  $< 10 \text{ fA/cm}^2$  should be sufficient for most applications in high-efficiency solar cells, these higher  $\text{PH}_3$  flows needed for a good electrical transport can be applied.

## 5.4 Doping profiles

The doping profiles of our sample set after FGA are shown in Figure 5.3. There are roughly three groups which are distinguished primarily by low, medium, and high  $\text{PH}_3$  flow. The dwell times give rise to only minor differences within the groups. A relative flow of 0.33 results in a comparatively shallow profile for all anneal dwell times, whereas a relative flow of 0.56 already increases the surface concentration by more than one order of magnitude. For 0.77 and 1.00 relative  $\text{PH}_3$  flow, the doping profiles are on a similar level, but it should be noted that the profiles were measured by electrochemical capacitance voltage (ECV) measurements which only detects electrically active dopant atoms.

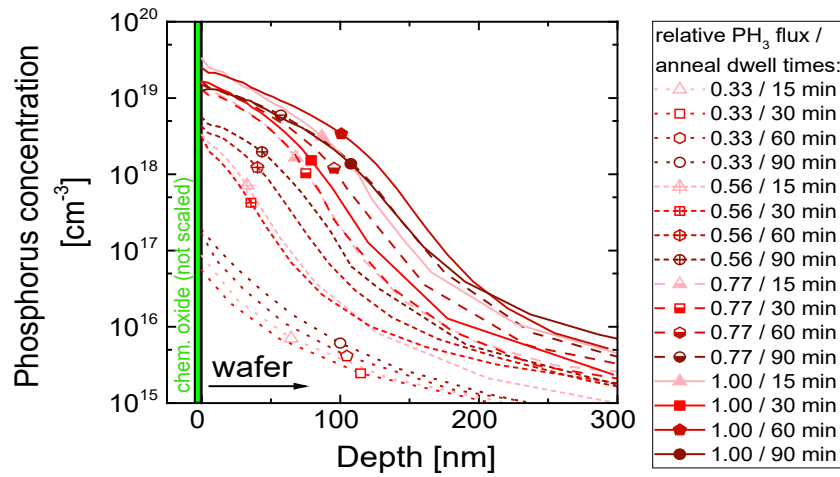


Figure 5.3 – Phosphorus doping profiles measured by ECV in the *c*-Si wafer after etching off the deposited layer stacks [Stuckelberger 2018]. The position of the symbols is only for a better readability.

## 5.5 EDNA2 simulations

The doping profiles shown in Figure 5.3 were used to simulate  $J_0$  as a function of SRV at the wafer/layer stack interface using EDNA 2 [PVLighthouse 2018a]. This SRV thus lumps all recombination processes occurring at the interface between the wafer and the deposited layer stack and within the layer stack, independently of their exact mechanism. Figure 5.4 resolves

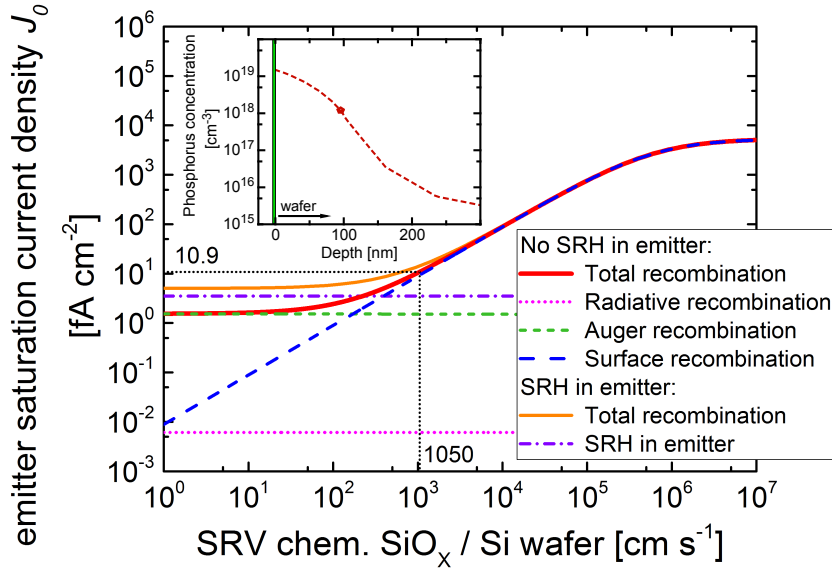


Figure 5.4 – Total  $J_0$  as a function of SRV at the chem-SiO<sub>x</sub>/wafer interface for the example of a relative PH<sub>3</sub> flow of 0.77 and an anneal dwell time of 60 min (doping profile shown as inset). The contribution of radiative (purple), Auger (green), and surface (blue) recombination to the total  $J_0$  (red) are indicated. The effect of SRH in the emitter (violet) leads to a different total  $J_0$  (orange). In dotted black lines the measured  $J_0$  after FGA and the corresponding SRV is marked [Stuckelberger 2018].

the individual contributions illustrated for the doping profile (inset) of the sample with 0.77 relative PH<sub>3</sub> flow and an annealing of 60 min at 900 °C. Radiative recombination (purple) is taken into account according to the model of Trupke [Trupke 2003], Auger recombination (green) is treated with the model described by Richter in ([Richter 2012], table II), giving a lower threshold for  $J_0$  at low SRV, and surface recombination (blue) is determined by  $U_{\text{surf}} = \text{SRV} \cdot \Delta n$ , with the recombination rate  $U_{\text{surf}}$  and the excess carrier concentration  $\Delta n$ . Based on the experimentally determined  $J_0$  of 10.9 fA/cm<sup>2</sup> after FGA, an SRV of 1050 cm/s is read off the characteristic.

For simplicity, we assume zero surface charge and no Shockley–Read–Hall (SRH) recombination in the bulk of the emitter because the material used was of high quality and the measured P concentrations are more than one order of magnitude lower than the solubility limit given by Solmi [Solmi 1996]. Note that this assumption leads to an upper limit for the SRV derived on the basis of the measured  $J_0$ . To further support our assumption, we projected a worst-case scenario in Figure 5.4 using the assumption  $\tau_{n0} = 5000\mu\text{s}$ , a low minority carrier lifetime  $\tau_{p0} = 1\mu\text{s}$  and a trap energy of  $E_t - E_i = 0.3\text{eV}$  to illustrate the effect of SRH recombination in the emitter (violet), leading to a different total  $J_0$  (orange). This would result in an SRV of 657 cm/s (intersection with orange curve) instead of SRV 1050 cm/s (intersection with red curve).

The simulations for the ECV doping profiles of all 16 samples are summarized in Figure 5.5. The symbols overlaid on the curves refer to the experimentally determined values of  $J_0$  after FGA. For low phosphorus concentrations (relative  $\text{PH}_3$  flow of 0.33) the dependence of  $J_0$  on SRV (straight line in the log–log plot) is approximately described by a power-law over almost the whole SRV range. This trend indicates that on one hand it is possible to reach very low  $J_0$  values for very low SRV, but on the other hand, the contact is very sensitive to the amount of interface recombination.

By increasing the doping to a relative  $\text{PH}_3$  flow of 0.56, the lowest obtainable  $J_0$  values extend into a similar range, but they are less sensitive to SRV values between 1 and 50  $\text{cm/s}$ . Figure 5.3 showed that this condition yields a deeper in-diffused region, resulting in reduction of the minority hole concentration close to the interface between chem- $\text{SiO}_x$  and wafer and thus a lower recombination rate at this interface.

For even higher relative  $\text{PH}_3$  flows of 0.77 and 1.00, the minimal attainable  $J_0$  for low SRV is clearly increased up to values between 1 and 4  $\text{fA/cm}^2$  due to Auger recombination, but at the same time, it is more robust against variation of the SRV. As Figure 5.5 depicts,  $J_0$  stays almost constant until around 1000  $\text{cm/s}$  before the monomial behavior arises.

For SRV in the range between  $1 \cdot 10^3$  and  $1 \cdot 10^5$   $\text{cm/s}$ , in which all curves show monomial behavior, higher doping concentrations result in slightly lower  $J_0$  values. All lie in the range of 100–1000  $\text{cm/s}$ , giving the possibility to use higher doping concentrations without being limited by Auger recombination.

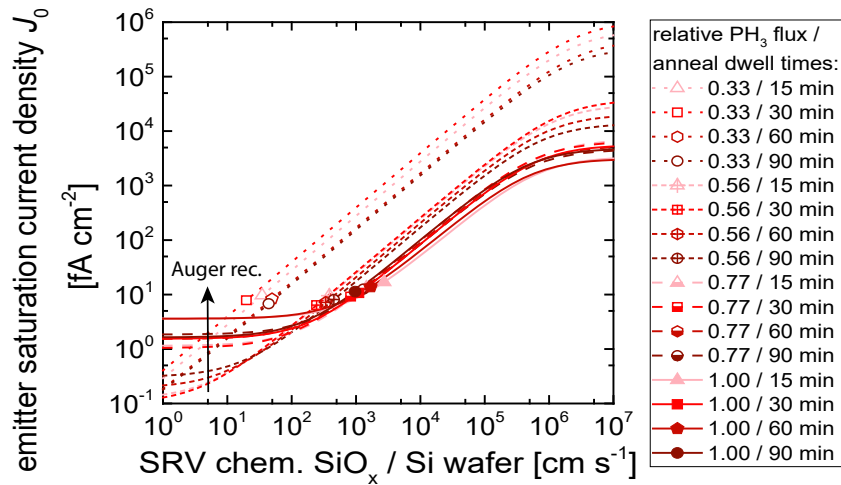


Figure 5.5 – Simulations by EDNA 2 [PVLighthouse 2018a] for  $J_0$  as a function of SRV at the chem- $\text{SiO}_x$ /wafer interface out of doping profiles shown in Figure 5.3 [Stuckelberger 2018].

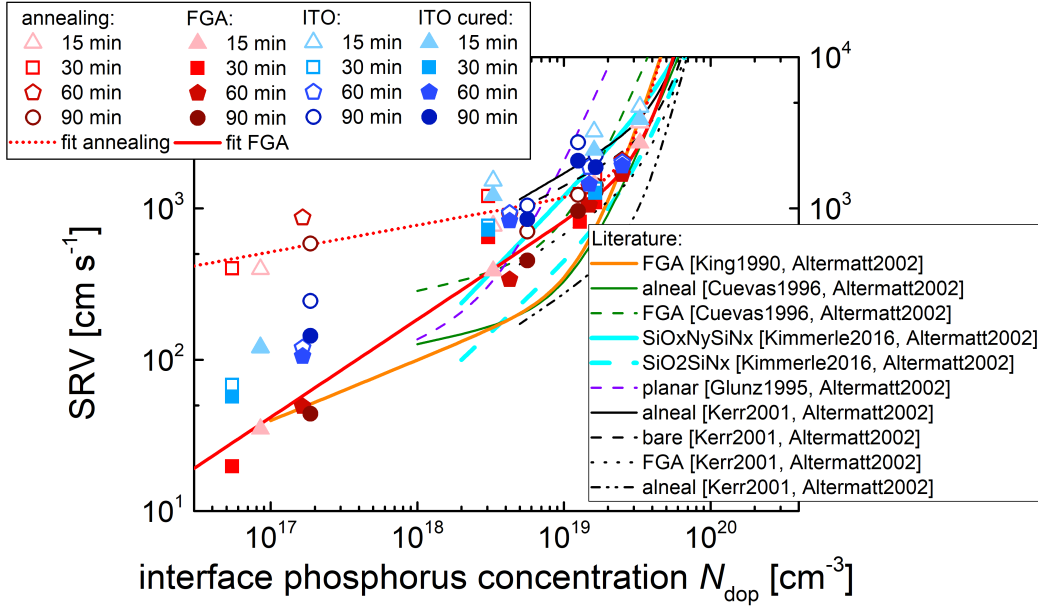


Figure 5.6 – Extracted SRV values from the combination of measured  $J_0$  and the simulations out of doping profiles plotted versus the phosphorus concentration at the chem-SiO<sub>x</sub>/wafer interface. The values are compared with literature data for dielectric passivation layers [Stuckelberger 2018].

### 5.5.1 Surface recombination

We determined the SRV of all of our structures from the simulated  $J_0$  (SRV) dependence and the experimentally determined  $J_0$  values. Additionally, we measured  $J_0$  after sputtering of ITO electrodes and once more after curing. Figure 5.6 depicts the extracted SRV values as a function of the phosphorus concentration at the wafer surface ( $N_{\text{dop}}$ ). Note that even with a relative error of 10% in  $J_0$ , almost all error bars for the resulting SRV are smaller than the symbol size, so they are not plotted. Before FGA (red open symbols) the SRV for low  $N_{\text{dop}}$ ,  $5 \cdot 10^{16} - 2 \cdot 10^{17} \text{ cm}^{-3}$ , and high  $N_{\text{dop}}$ ,  $1 - 4 \cdot 10^{19} \text{ cm}^{-3}$ , lie between 400 (low  $N_{\text{dop}}$ ) and 3700  $\text{cm/s}$  (high  $N_{\text{dop}}$ ). After FGA (red filled symbols), the SRV of those with low  $N_{\text{dop}}$  improve by a factor of up to 20 to values as low as 20  $\text{cm/s}$ , whereas for high  $N_{\text{dop}}$  the SRV improve only by a factor of 1–1.5.

In Figure 5.6, we have also replotted literature data for SiO<sub>2</sub> and SiO<sub>x</sub>/SiN<sub>y</sub> passivation layers [King 1990, Cuevas 1996, Kimmerle 2016, Glunz 1995, Kerr 2001, Altermatt 2002]. Note that these layers were dielectric layers, and did not work as charge carrier extraction layers. Figure 5.6 shows that the SRV of our passivating electron contact follows a very similar dependence on  $N_{\text{dop}}$ . Following [Altermatt 2002] we describe the dependence of SRV on the interface

phosphorus concentration by the following equation [Altermatt 2002]:

$$\text{SRV} = S_{p1} \left( \frac{N_{\text{dop}}}{10^{19} \text{cm}^{-3}} \right)^{\gamma_1} + S_{p2} \left( \frac{N_{\text{dop}}}{10^{19} \text{cm}^{-3}} \right)^{\gamma_2} \quad (5.1)$$

using the fit parameters  $S_{p1}$ ,  $S_{p2}$ ,  $\gamma_1$ , and  $\gamma_2$ . Due to the lack of data at high  $N_{\text{dop}}$  the second term is rather uncertain and  $\gamma_2$  is therefore set to 4 as used by [Altermatt 2002] to parametrize the data of [Kerr 2001]. The found parametrizations for the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack after annealing and after FGA are summarized in Table 5.1 and compared with the parametrizations reported for a dielectric thermal silicon oxide before and after an FGA [Kerr 2001, Altermatt 2002]. Whereas the exponent  $\gamma_1$  is clearly lower for the chem-SiO<sub>x</sub>mp-SiO<sub>x</sub>(n)/nc-Si(n) samples without FGA compared with the reported samples with bare oxide, this fit parameter  $\gamma_1$  is very similar when comparing after the FGA.

Table 5.1 –  
Parameters in Equation 5.1 to approximate SRV values shown in Figure 5.6

	$S_{p1}$ [cm/s]	$\gamma_1$	$S_{p2}$ [cm/s]	$\gamma_2$
mp-SiO <sub>x</sub> (n)/nc-Si(n)(after annealing)	1165	0.18	19.0	4
mp-SiO <sub>x</sub> (n)/nc-Si(n)(FGA)	816	0.65	7.7	4
thermal SiO <sub>2</sub>	1400	0.5	4	4
thermal SiO <sub>2</sub> (FGA)	670	0.65	4	4

The dielectric passivation layers [King 1990, Cuevas 1996, Kimmerle 2016, Glunz 1995, Kerr 2001, Altermatt 2002] are electrically insulating and thus do not allow the establishment of an electrical contact for charge carrier extraction. The passivating contact layer stack presented here shows a very similar dependence of SRV over the studied surface phosphorus concentration range and in addition, this layer stack also acts as electrical contact to the silicon wafer, thanks to the silicon inclusions as was shown in chapter 3.

Figure 5.7 shows  $J_0$  (left axis) at the different steps of contact formation, grouped by the relative PH<sub>3</sub> flow. The crosshatched area at the top of the bars represents the contribution of Auger recombination, extracted from the EDNA 2 simulations as described in Section 5.5. Low PH<sub>3</sub> flows and short anneal dwell times result in shallow doping profiles and therefore low Auger recombination. These conditions yield the lowest  $J_0$  values after FGA. For longer dwell times and increasing doping levels,  $J_0$  generally increases due to increasing Auger recombination. Additionally, the diffusion of a larger amount of dopants through the chemical oxide can also create defects and hence additional recombination centers at the interface.

Sputtering of ITO increases  $J_0$  in all cases, but it is particularly detrimental for the  $J_0$  of samples with low relative PH<sub>3</sub> flows of 0.33 and 0.56. These conditions coincide with low surface phosphorus concentrations in the range of  $10^{16}$ – $1 \cdot 10^{17} \text{cm}^{-3}$ . In Figure 5.6, the corresponding

## Chapter 5. Mixed-phase silicon oxide — Influence of initial doping concentration and anneal dwell time

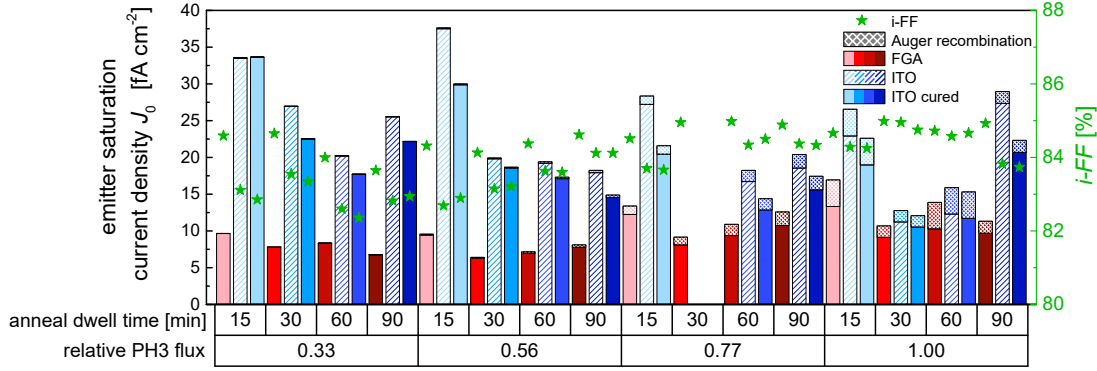


Figure 5.7 – Emitter saturation current density  $J_0$  and its evolution after FGA (red), after ITO sputtering (blue striped) and its curing (blue filled) as a function of the relative  $\text{PH}_3$  flow and the anneal dwell time. The contribution of Auger recombination to each  $J_0$  is marked crosshatched. The  $i\text{-FF}$  (green stars, right axis) shows the influence of the ITO deposition at maximum-power-point (mpp) conditions [Stuckelberger 2018].

samples showed the largest improvements by FGA (reduction of their SRVs by a factor of up to 20), but also larger sensitivity to loss of interface passivation (increase of SRV after ITO sputtering by a factor of  $\sim 3$ – $5$ ). Samples with higher relative phosphorus flow of 0.77 and 1.00 are more resilient against ITO sputtering damage. Consequently, they are more promising for device fabrication despite their higher contribution of Auger recombination.

For heterojunction solar cells, it was reported that the detrimental losses of ITO sputtering can be regained by curing [Morales-Masis 2015, Wolf 2012]. This effect is also visible for our passivating electron contact, but the SRV shown in Figure 5.6 is reduced only by a factor of 1–1.5, and rather independently of the phosphorus surface concentration as shown by the filled blue symbols in Figure 5.6, indicating that sputtering induced damage cannot be fully recovered. This leads to SRV values after curing between 50 and  $150 \text{ cm/s}$  for  $N_{\text{dop}}$  of  $10^{16}$ – $1 \cdot 10^{17} \text{ cm}^{-3}$ . For  $N_{\text{dop}}$  in the range of  $1 \cdot 10^{18} \text{ cm}^{-3}$  SRV ranges between 700 and  $1200 \text{ cm/s}$ . For still higher  $N_{\text{dop}}$ , an SRV in the range of 1500–4000  $\text{cm/s}$  is extracted. The influence of the curing (after ITO deposition) is also shown in Figure 5.7, and for most samples it is on a similar level.

Conditions with higher relative  $\text{PH}_3$  flows and longer anneal dwell times lead to several conditions with a  $J_0$  below  $15 \text{ fA/cm}^2$ . The optimum in our dataset is found at a relative  $\text{PH}_3$  flow of 1.00 and a dwell time of 30 min, resulting in a  $J_0$  of  $12.1 \text{ fA/cm}^2$ . Therein, Auger recombination contributes  $1.5 \text{ fA/cm}^2$ .

A closer look at the impact of ITO (including the curing) on the passivation clearly shows a stronger impact on samples with low interface concentrations for which chemical passivation plays a dominant role to reach high surface passivation. It is remarkable that even though

some of the conditions used have rather high interface concentrations of  $2.5 \cdot 10^{19} \text{ cm}^{-3}$ , the resulting contribution of Auger recombination to  $J_0$  was found to be  $< 3.6 \text{ fA/cm}^2$  and has therefore a lower impact on the final performance than the ITO sputtering.

We also report the implied fill factor ( $iFF$ ) in Figure 5.7 (green stars, right axis) in order to show the influence of the ITO deposition at maximal-power-point conditions. The same trend as for  $J_0$  is observed: The degradation is stronger (losses of up to 1.75% absolute) for low doping, and the  $iFF$  does not recover by curing, whereas for the best condition with a relative  $\text{PH}_3$  flow of 1.00 annealed for 30 min, the  $iFF$  drops only by 0.25% from 85.0% to 84.75%.

We assume that the doping profile and therefore the Auger recombination is not affected by the ITO sputtering. Therefore, this higher impact on samples with low interface concentrations could be related to a degradation of the chemical passivation due to sputtering and/or to the detrimental effect of band bending induced by the work function of the ITO, effectively reducing the electron concentration at the Si surface, an effect already reported for heterojunction solar cells [Tomasi 2016, Rößler 2013].

## 5.6 Proof-of-concept solar cells

As a proof-of-concept and to further investigate this mixed-phase  $\text{SiO}_x$  layer stack, a hybrid solar cell (SHJ rear side) was fabricated on a planar  $1 \Omega \text{ cm}$  phosphorus-doped n-type FZ wafer

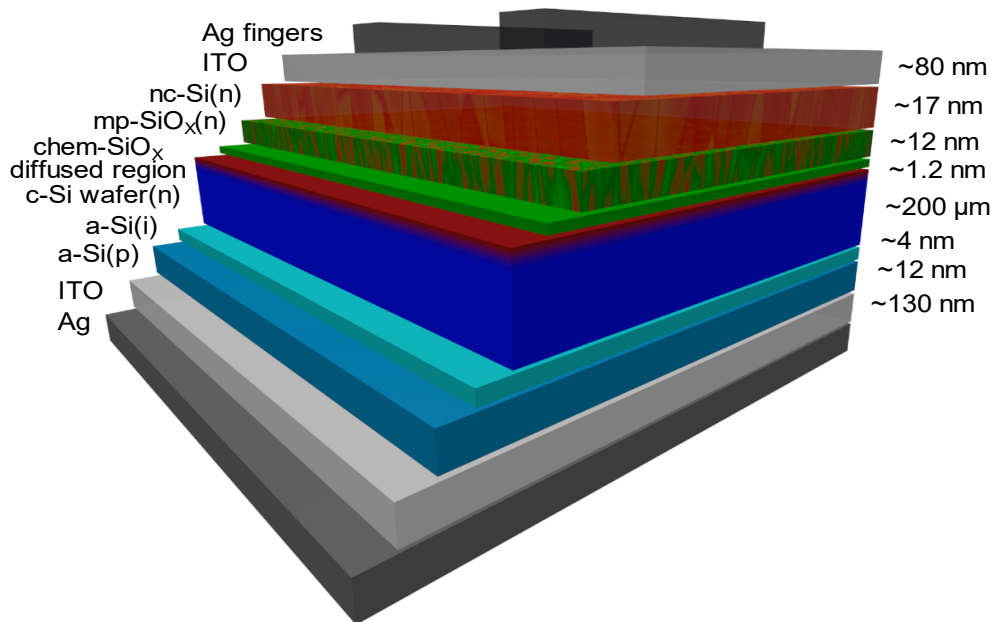


Figure 5.8 – Sketch of the layer stack employed in the proof-of-concept solar cell [Stuckelberger 2018].

having ITO/Ag as metallization. The final structure is sketched in Figure 5.8 and in section 2.2.1 more details can be found on the fabrication. To this end, the condition giving the lowest  $\rho_c$  with a relative  $\text{PH}_3$  flow of 1.00 and anneal dwell time of 15 min was chosen, no FGA was applied.

Figure 5.9a depicts the measured  $J$ - $V$  curve under illumination (blue) together with the Suns- $V_{OC}$  measurement (dashed red). A fill factor ( $FF$ ) of 79.4% demonstrates efficient carrier transport through the mixed-phase layer. Nevertheless, the value falls short of the  $iFF$  of 84%. The difference is (partially) explained by the contact resistivity of  $0.5 \Omega \text{ cm}^2$  which reduces the idealized value of the  $iFF$  from 84% to 81.7% [Green 1982]. The remaining losses can be partly attributed to the SHJ rear. The short-circuit current density ( $J_{SC}$ ) of  $33.9 \text{ mA/cm}^2$  is promising for a planar solar cell compared with an upper limit of  $35.7 \text{ mA/cm}^2$  simulated with Wafer ray tracer [PVLighthouse 2018c] for a planar ideal device using nitride/wafer/nitride/Ag on a  $200 \mu\text{m}$  wafer including the same shading losses of 5%. The high  $J_{SC}$  shows the potential of this contact as a front layer even though the open-circuit voltage ( $V_{OC}$ ) of 691 mV is lower than expected from its  $iV_{OC}$  value of 706 mV. We relate the low  $V_{OC}$  to several not optimized cell fabrication steps, especially to the wafer surface conditioning before the SHJ rear side deposition, since the lifetime after the rear side deposition is only improving slightly. We also assume this to be the reason for the low pseudo- $FF$  ( $pFF$ ) of only 83.0%, since on symmetrical samples with  $a\text{-Si(i)}/a\text{-Si(p)}$ , using the same fabrication method as for the proof-of-concept cell, an  $iFF$  of only 78.4% was observed before the ITO deposition. Nevertheless, the planar proof-of-concept device shown in Figure 5.9a has a conversion efficiency  $\eta$  of 18.6%.

In Figure 5.9b, the  $EQE$  of the planar proof-of-concept solar cell is plotted together with the

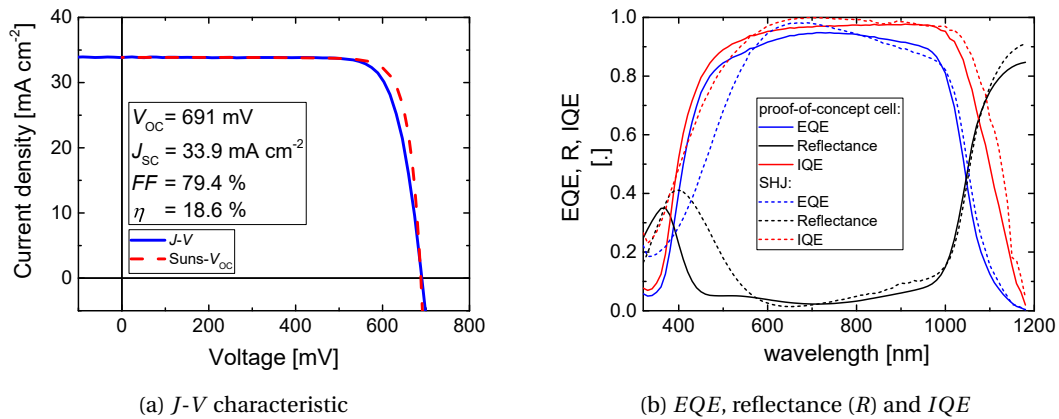


Figure 5.9 – (a)  $J$ - $V$  characteristics of a planar hybrid cell (blue solid line) with the mixed-phase  $\text{SiO}_x$  layer n-type stack at the front and an amorphous heterojunction p-type hole collector at the rear. The Suns- $V_{OC}$  curve is plotted in a red dashed line. (b) The EQE (blue), reflectance (black), and IQE (red) of the hybrid cell (solid lines) is set in comparison with a planar SHJ cell (dashed lines) [Stuckelberger 2016a].

reflectance ( $R$ ) and the calculated  $IQE$  in comparison with a planar SHJ cell (dashed lines) in rear emitter configuration (all  $EQE$ s are measured between the contact fingers). Both cells have an  $a\text{-Si(i)}/a\text{-Si(p)}$  rear contact, but the contacts were not co-deposited, and the flat SHJ cell was fabricated on a 270- $\mu\text{m}$ -thick n-type wafer, thus explaining the differences at long wavelengths. At short wavelengths, the differences visible in  $EQE$  and  $R$  are mainly determined by the front layer, allowing a direct comparison of our mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack ( $\sim 12/\sim 17$  nm) with the SHJ  $a\text{-Si(i)}/a\text{-Si(n)}$  front ( $\sim 4/\sim 6$  nm). Below 400 nm, the  $EQE$  response of the proof-of-concept cell is lower than the SHJ. This could be related to parasitic absorption which is lower for  $a\text{-Si}$  than for nc-Si(n) in this range. Between 400 and 550 nm, the proof-of-concept cell shows a strong increase in  $EQE$  as well as  $IQE$  which is associated to the low parasitic absorption in the front mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack as well as low reflectance. Above 550 nm, the  $IQE$  of the proof-of-concept cells remains below 97%, indicating recombination losses at the front side.

An interesting additional feature of the proof-of-concept cell is visible in  $R$ . For a broad wavelength ( $\lambda$ ) range of  $450\text{ nm} < \lambda < 950\text{ nm}$ ,  $R$  is below 10% showing an anti-reflection behavior of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack at the front, even though the ITO thickness is not optimized yet. We therefore conclude that the effective refractive index of the mp-SiO<sub>x</sub>(n)/nc-Si(n) stack lies between the one of ITO and crystalline silicon, thus giving a smoother index transition than a direct ITO/ $a\text{-Si}/c\text{-Si}$  interface.

## 5.7 Conclusion

We investigated the influence of the initial doping concentration and the anneal dwell time at 900 °C on electron-selective passivating contacts based on a highly phosphorus-doped mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack, and we related our findings to the properties of the junction. The results indicate a trade-off between reduced recombination due to a reduced density of minority carriers in the in-diffused region and the interface, and increased recombination by the Auger effect and at the defects created in the interfacial oxide.

Based on EDNA 2 simulations we discussed the impact of the doping profile on the relation between the emitter saturation current density  $J_0$  and the surface recombination velocity SRV. The contact presented here exhibits a very similar dependence of SRV on phosphorus surface concentration as for passivation with dielectric layers reported in the literature. A deeper profile with a higher phosphorus concentration is less sensitive to the SRV and relies therefore less on chemical passivation of the interface. When using hydrogenation to optimize surface passivation it should be kept in mind that the negative influence of the ITO sputtering (causing surface passivation damage) may be stronger in case of a predominant chemical passivation. For our sputtering conditions, we find a  $J_0$  value of 12.1 fA/cm<sup>2</sup> for higher doping levels and we note that such P doping levels are also needed in our mixed-phase SiO<sub>x</sub> contacts to ensure a sufficient carrier transport through the layer.

Finally, we presented a planar proof-of-concept solar cell with a  $FF$  of 79.4%, a  $J_{SC}$  of

## **Chapter 5. Mixed-phase silicon oxide — Influence of initial doping concentration and anneal dwell time**

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33.9 mA/cm<sup>2</sup> and a  $V_{OC}$  of 691 mV leading to a conversion efficiency of 18.6%.

This result points out that the use of high doping levels in the deposited layers enables an efficient current extraction whereas the nano-structure of the mixed-phase SiO<sub>x</sub> layer ensures a low level of parasitic absorption in the layers of our front-contact, enabling comparatively high short-circuit current density for our flat cells.

Additionally, we found that this layer stack is capable of strengthening the anti-reflection behavior of our ITO front contact.

## 6 Mixed-phase silicon oxide — Optical analysis and cell integration

In this chapter we investigate the optical properties of mp-SiO<sub>x</sub>(n) and nc-Si(n). First the refractive index  $n$  and the extinction coefficient  $k$  of the individual layers are extracted by spectroscopic ellipsometry. For the mp-SiO<sub>x</sub>(n) layer, values between those of SiO<sub>2</sub> and SiO<sub>1</sub> are extracted, which confirms the high oxygen content reported in chapter 3. The measured values are used to simulate the spectral response in finished solar cells.

We present the influence of several parameters on the in-diffusion of phosphorus into the wafer during thermal treatment at 900 °C. The roles of the wafer doping and polarity are addressed as well as the role of doping in the mp-SiO<sub>x</sub>(n) layer.

The challenges to implement the mp-SiO<sub>x</sub>(n)/nc-Si(n) into working solar cells are reported together with results of finished solar cells as hybrid devices or as co-annealed cells. The losses during the fabrication process are analyzed on planar surfaces and on textured surfaces. In planar co-annealed cells, short-circuit current densities ( $J_{SC}$ ) of 35.0 mA/cm<sup>2</sup> show the potential of this layer stack for use at the front. Together with a fill factor ( $FF$ ) of 80% and an open-circuit voltage ( $V_{OC}$ ) of 686 mV, an efficiency of 19% is reached. Out of the thickness-dependent losses in the measured internal quantum efficiencies, the absorption losses are quantified for the individual layers as 0.4 mA/cm<sup>2</sup> per 10 nm within the nc-Si(n) layer and only 0.07 mA/cm<sup>2</sup> per 10 nm within the mp-SiO<sub>x</sub>(n) layer. Transferring the mp-SiO<sub>x</sub>(n)/nc-Si(n) to textured surfaces, the  $J_{SC}$  remains promising with 40 mA/cm<sup>2</sup> whereas the  $V_{OC}$  suffers during the fabrication processes and a loss in  $FF$  is observed on textured surfaces. To overcome the losses in  $V_{OC}$  the nc-Si(n) is replaced with an  $a$ -SiC(n) layer resulting in conversion efficiencies of up to 20.1%.

### 6.1 Introduction

With a contact stack of mp-SiO<sub>x</sub>(n)/nc-Si(n) we target application on the front side of a solar cell and therefore its optical properties are of high interest. In the previous two chapters, the passivation quality and current extraction were analyzed, whereas here the focus will be

on the optical parameters extracted by spectroscopic ellipsometry (SE) as well as the overall performance at the cell level. Parasitic absorption in this contact structure is simulated at the cell level by using the software tool OPAL [PVLighthouse 2018b].

The short-circuit current density ( $J_{SC}$ ) is a measure of the maximal current that can be drawn from a solar cell. It is strongly dependent on how much of the incoming photon flux is absorbed and lost in the front layers before reaching the silicon wafer to generate carriers. So far, the highest reported  $J_{SC}$  for single-junction *c*-Si solar cells is 43.3 mA/cm<sup>2</sup> [Richter 2017] with a 400-μm-thick solar cell. The more commonly used 200-μm-thick absorber can reach a  $J_{SC}$  of 42.5 fA/cm<sup>2</sup> [Richter 2017]. This is also the current world-record efficiency for both-side-contacted solar cells. This  $J_{SC}$  is impressive considering that the maximal current density for a 200-μm-thick silicon absorber is 44.1 fA/cm<sup>2</sup> [PVLighthouse 2018b]. These cell concepts come with a boron-diffused front junction passivated by an Al<sub>2</sub>O<sub>3</sub> passivation layer and a double anti-reflection coating (DARC) of SiN<sub>x</sub> and MgF<sub>2</sub> that is locally opened for the contacts. Such openings are feasible to fabricate for high-efficient lab cells, but are probably too complex for integration into industrially applicable solar cells.

Such high currents have been reached only for both-side-contacted cells using a diffused emitter that is passivated by non-conductive layers with local openings, or by firing through these layers, which damages the passivation. The literature on cells with a full-area passivating carrier-selective contact at the front is still sparse except for heterojunction solar (SHJ) cells. Recently, a  $J_{SC}$  of 38.8 mA/cm<sup>2</sup> was reported [Ingenito 2017] for a SiC<sub>x</sub>(n) electron-selective emitter co-annealed with a rear SiC<sub>x</sub>(p) contact, and a  $J_{SC}$  of 39.9 mA/cm<sup>2</sup> was demonstrated for a POLO contact with an additional *α*-SiO<sub>x</sub> anti-reflection coating on top of the silver grid [Morales Vilches 2018]. Both-side-contacted SHJ solar cells have reached  $J_{SC}$  values of 40.8 mA/cm<sup>2</sup> in record devices [Green 2016, Adachi 2015].

Therefore, transparent passivating carrier-selective contacts are of high interest for the next generation of solar cells.

## 6.2 Experimental details

The investigation of the optical properties of the passivating electron contact at the layer level was done on 200-μm-thick double-side-polished 4-inch (100) 2 Ω cm silicon wafers doped with phosphorus or boron. The same contact structure was used in previous chapters. After cleaning using standard wet chemistry a thin (~ 1.2 nm) SiO<sub>x</sub> layer was formed by wet chemical oxidation [Asuha 2003, Grant 2009] also referred to as chem-SiO<sub>x</sub>. Subsequently, a phosphorus-doped mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer structure of a mixed-phase silicon oxide (mp-SiO<sub>x</sub>(n)) layer and a nanocrystalline silicon (nc-Si(n)) layer was deposited by PECVD. The individual layers are also referred to as mp-SiO<sub>x</sub>(n) and nc-Si(n) in order to distinguish them from the chem-SiO<sub>x</sub> whereas the whole mp-SiO<sub>x</sub>(n)/nc-Si(n) is also referred to as SiO<sub>x</sub>(n). The deposition time for the individual layers is given by the form 120 s / 210 s standing for 120 s of mp-SiO<sub>x</sub>(n) and 210 s of nc-Si(n) deposition time, respectively. The samples were then

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### 6.3. Spectroscopic ellipsometry measurements

annealed for 15 min in a nitrogen ( $N_2$ ) atmosphere at  $900^\circ\text{C}$ . This was followed by 30 min of forming gas (FGA, 4%  $H_2$  in  $N_2$ ) annealing at  $500^\circ\text{C}$  to passivate electronic defects at the wafer–chem- $SiO_x$  interface.

For the solar cells we differentiate between two types: hybrid solar cells having a SHJ rear side or co-annealed solar cells using a passivating hole-selective contact at the rear that is annealed together with the front. For the hybrid cells, the passivating electron contact is deposited on the front side of the silicon wafer. A sketch of the final layer stack of our device is illustrated in Figure 5.8. More detailed information about the fabrication process for the hybrid cells can be found in section 2.2.1.

For the co-annealed solar cells, a  $SiO_x(i/p)$  hole-selective emitter is applied, using a similar thermal budget. The  $SiO_x$  part of this layer is kept intrinsic due to a better performance which is the reason why it is called  $SiO_x(i/p)$ . More information on the development of this layer can be found in [Wyss 2018]. This gave us the opportunity to simplify the fabrication process as explained in section 2.2.2 and deposit the mp- $SiO_x(n)/nc-Si(n)$  bilayer on one side and subsequently the  $SiO_x(i/p)$  layer on the other side. Annealing them together at  $900^\circ\text{C}$  for 15 min in a  $N_2$  atmosphere, led to the formation of boron- and phosphorus-doped regions on opposite sides of the wafer. After annealing, an FGA was applied at  $500^\circ\text{C}$  for 30 min. A second hydrogenation was carried out by using PECVD to deposit  $SiN_x$  on both sides of the wafer followed by an annealing on a hotplate at  $450^\circ\text{C}$  for 30 min in air. The  $SiN_x$  is afterwards removed in a  $H_3PO_4$  solution at  $180^\circ\text{C}$  for 30 min [Liu 2007] and an HF etch (1 vol.-%) is applied until a hydrophobic n-side is reached. Next, 80 nm of ITO was sputtered onto the front and 130 nm onto the rear. The solar cells were then finished by sputtering a silver reflector on the rear side and screen printing a Ag grid on the front, followed by curing for 30 min at  $210^\circ\text{C}$  in a belt furnace. A sketch of the finished cell can be found in Figure 6.18.

The effective minority-carrier lifetime was measured by photo-conductance decay (PCD) applying Kimmerle's method [Kimmerle 2015] to extract the emitter saturation current density  $J_0$  at an excess-carrier density of  $1 \cdot 10^{16} \text{ cm}^{-3}$ .

The external quantum efficiency (EQE) and the reflectance (R) were measured with an IQE-Scan from PV-tools and include the shading losses. From those measurements, the wavelength-dependent internal quantum efficiency (IQE) was calculated.

### 6.3 Spectroscopic ellipsometry measurements

Spectroscopic ellipsometry (SE) uses a polarized illumination source and measures wavelength-dependent changes in the polarization of the reflected beam. For the extraction of characteristic material properties like refractive index  $n$ , extinction coefficient  $k$  or absorption coefficient  $\alpha$ , an adequate modeling of the structure is needed. As chapter 3 revealed, the layer stack used here consists of a mixed-phase  $SiO_x(n)$  layer leading to a rough interface with the nc- $Si(n)$  layer and consequently to an even higher surface roughness of the bilayer stack.

layer thickness [nm]		model 1: mp-SiO <sub>x</sub> (n) only			
4	<input checked="" type="checkbox"/> 18.00 <input type="checkbox"/> %	<input checked="" type="checkbox"/> SiO <sub>x</sub> _nam.dsp	50.00 % <input checked="" type="checkbox"/>	<input type="checkbox"/> void.dsp	50.00 % <input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
3	<input checked="" type="checkbox"/> 6.00	<input checked="" type="checkbox"/> SiO <sub>x</sub> _nam.dsp			<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
2	<input type="checkbox"/> 1.20	<input type="checkbox"/> SiO <sub>2</sub> .dsp			<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
1	<input type="checkbox"/> 200000.00	<input type="checkbox"/> c-Si_KA.dsp			<input checked="" type="checkbox"/> <input checked="" type="checkbox"/>
5		Void.ref			<input checked="" type="checkbox"/> <input type="checkbox"/>

Figure 6.1 – Model used to fit the spectroscopic ellipsometry measurement of the mp-SiO<sub>x</sub>(n) layer only. The thickness of each layer is indicated on the left.

This roughness together with the mixed-phase nature with a low absorbing oxide makes the modeling of this layer stack challenging. The extracted values should therefore be regarded with caution.

First we modeled the mp-SiO<sub>x</sub>(n) layer without a cover layer to decrease the complexity, depicted in Figure 6.1. The wafer is represented by the model "c-Si KA", a dispersion model for silicon proposed by Kato and Adachi [Kato 1994, Horiba 1994]. Reflections at the rear are taken into account by the "void" layer, whereas no difference was observed when the same layer stack was implemented at the rear in reverse order, or with a direct c-Si/void interface. The chem-SiO<sub>x</sub> layer is assumed to be 1.2 nm of SiO<sub>2</sub> (SiO<sub>2</sub>.dsp) covered by the SiO<sub>x</sub> layer, modeled by the "new amorphous" (nam) dispersion formula [Horiba 2006] based on the formulation of [Forouhi 1986, Forouhi 1988]. The five fitting parameters for the "new amorphous" dispersion formula are:

- $n_{\infty}$ : value of the refractive index when  $\omega \rightarrow \infty$
- $f_j$ : strength (amplitude) of the extinction coefficient peak
- $\Gamma_j$ : broadening of the absorption peak
- $\omega_j$ : approximately the energy at which the extinction coefficient is maximum. As the value of  $\omega_j$  increases, the peak is shifted towards the UV region.
- $\omega_g$ : energy bandgap. This is the energy from which the absorption starts to be non-zero.

The surface roughness is modeled using a 50% "void" within the surface layer. The thicknesses of the two upper layers as well as the material SiO<sub>x</sub> are fitted as can be seen by the "F"'s in Figure 6.1. This results in thicknesses of  $5.8 \pm 0.8$  nm and  $18.5 \pm 0.7$  nm for the SiO<sub>x</sub> layer and for the surface layer, respectively. The material for the mp-SiO<sub>x</sub>(n) layer is best fitted using the parameters  $n_{\infty} = 1.97 \pm 0.04$ ,  $f_j = 0.005 \pm 0.002$  eV,  $\Gamma_j = 0.41 \pm 0.10$  eV,  $\omega_j = 5.02 \pm 0.06$  eV and  $\omega_g = 2.15 \pm 0.40$  eV leading to an error  $\chi^2 = 0.73$ . These errors include only the fitting to the measured data. The uncertainties due to simplification and assumptions in the model are certainly higher. The resulting refractive index  $n$  and extinction coefficient  $k$  of the mp-SiO<sub>x</sub>(n) layer are plotted in Figure 6.2 in blue. The diagram also contains the characteristics of SiO<sub>2</sub> (solid grey line) [Palik 1998], and the starting material for fitting "SiO<sub>x</sub> nam" representing SiO

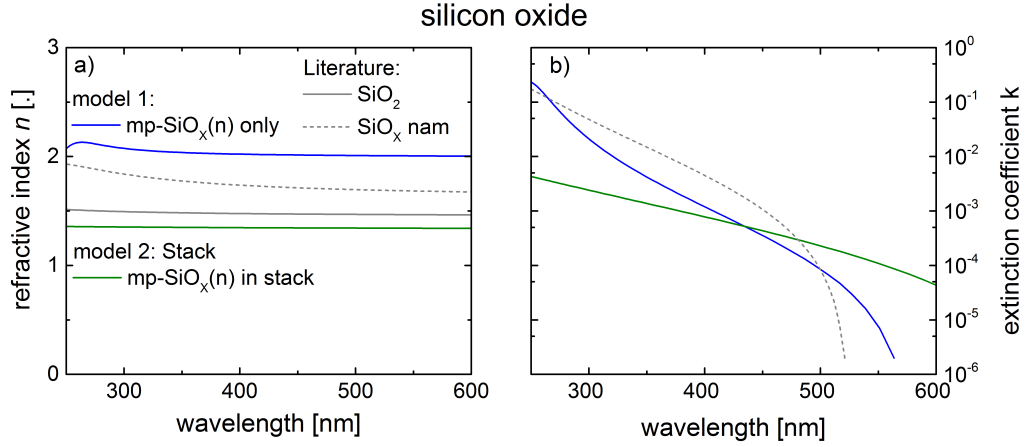


Figure 6.2 – (a) The refractive index  $n$  and (b) the extinction coefficient  $k$  obtained for the mp-SiO<sub>x</sub>(n) layer from the ellipsometry measurements for the mp-SiO<sub>x</sub>(n) layer only (model 1, blue) and for the mp-SiO<sub>x</sub>(n) layer in the mp-SiO<sub>x</sub>(n)/nc-Si(n) stack (model 2, green). For comparison,  $n$  and  $k$  values from the literature are added: SiO<sub>2</sub> (solid grey line, [Palik 1998]) and SiO<sub>x</sub> nam (dashed grey line, [Horiba 2006]).

(dashed grey line). The refractive index  $n$  is slightly increased over the full wavelength range with a value of 2.00 at 635 nm compared to 1.67 for SiO and 1.46 for SiO<sub>2</sub>, respectively.

The extinction coefficient  $k$  for SiO<sub>2</sub> is too small to be shown on this scale and in the models is assumed to be zero [Palik 1998]. A higher silicon content as in "SiO<sub>x</sub> nam" leads to an increase in  $k$  for wavelengths below 525 nm with a maximum of 0.25 whereas above 525 nm  $k$  is still assumed to be zero. The  $k$  of the modeled mp-SiO<sub>x</sub>(n) layer is slightly lower than "SiO<sub>x</sub> nam" below 500 nm whereas the point at which  $k$  is assumed to be zero is with 575 nm slightly shifted to higher a wavelength.

Unfortunately the model found for single layers of mp-SiO<sub>x</sub>(n) could not be implemented into the mp-SiO<sub>x</sub>(n)/nc-Si(n) stacks. Therefore a new model (model 2, stack) was set up using the observations of the TEM images presented in chapter 3 for the thicknesses of the individual layers. Figure 6.3 shows that the model starts with a "void" layer at the rear, followed by the wafer represented by the material "c-Si KA". The chem-SiO<sub>x</sub> is again assumed to be 1.2 nm of SiO<sub>2</sub> (SiO2.dsp) covered by the SiO<sub>x</sub> layer modeled by the "new amorphous" (nam) dispersion formula [Horiba 2006]. For this fitting, we kept the amplitude of the extinction coefficient peak constant at  $f_j = 0.0841$  eV as proposed by [Horiba 2006] for SiO. Additionally, limiting values of  $1.6 \text{ eV} < \omega_g < 3.0 \text{ eV}$  are set for the energy bandgap.

The nc-Si(n) layer is modeled by a material called "p-Si large grain KA" based on the dispersion formula of Kato and Adachi [Kato 1994, Horiba 1994] and was used and developed for the analysis of thin-film silicon solar cells with microcrystalline silicon having different grain sizes. To satisfy the high surface roughness, 20% "void" is implemented into the upper part

layer thickness [nm]		model 2: Stack	
6	<input type="checkbox"/> 4.00	<input type="checkbox"/> SiO <sub>2</sub> .dsp	x x
5	<input type="checkbox"/> 10.00 <input type="checkbox"/> %	<input type="checkbox"/> void.dsp 20.00 % x <input type="checkbox"/> p-Si_large grain_KA.dsp 80.00 %	x x
4	<input type="checkbox"/> 7.00	<input checked="" type="checkbox"/> p-Si_large grain_KA.dsp	x x
3	<input type="checkbox"/> 12.00	<input checked="" type="checkbox"/> SiO <sub>x</sub> _nam.dsp	x x
2	<input type="checkbox"/> 1.20	<input type="checkbox"/> SiO <sub>2</sub> .dsp	x x
1	<input type="checkbox"/> 200000.00	<input type="checkbox"/> c-Si_KA.dsp	x x
0		Void.ref	x

Figure 6.3 – Model used to fit the spectroscopic ellipsometry measurement of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack. The thickness of each layer is indicated on the left.

of the nc-Si(n) layer. The layer stack is finished with a 4-nm-thick SiO<sub>2</sub> layer representing the thermal oxide grown during annealing at 900 °C.

The mp-SiO<sub>x</sub>(n) is best fitted using the parameters  $n_{\infty} = 1.33 \pm 0.01$ ,  $\Gamma_j = 14.01 \pm 3.71$  eV,  $\omega_j = 2.72 \pm 0.62$  eV and  $\omega_g = 1.75 \pm 0.55$  eV leading to an error  $\chi^2 = 0.73$ . These errors include only the fitting to the measured data. The uncertainties due to simplification and assumptions in the model are certainly higher. Compared to the material found by modeling single mp-SiO<sub>x</sub>(n) layers, all parameters are decreased except for  $\Gamma_j$ , which represents the broadening of the absorption peak.

The resulting refractive index  $n$  and extinction coefficient  $k$  for the mp-SiO<sub>x</sub>(n) layer is added to Figure 6.2 in green. The refractive index  $n$  of mp-SiO<sub>x</sub>(n) modeled within the stack behaves like SiO<sub>2</sub> with a value of 1.34 at 635 nm compared to the 1.67 for SiO and 1.46 for SiO<sub>2</sub>. We assume that the slightly lower  $n$  for mp-SiO<sub>x</sub>(n) than for SiO<sub>2</sub> is due to a simplification of the model and not due to the real physical properties of this material. The extinction coefficient  $k$  is below 0.005 for the full wavelength range, but it decays towards long wavelengths with a lower slope due to the larger  $\Gamma_j$ . As mentioned before, these values should be taken with care since the nc-Si(n) layer on top dominates the absorption and the overall behavior of this layer stack.

In Figure 6.4  $n$  and  $k$  of the modeled nc-Si(n) layer are plotted in comparison to  $c$ -Si (solid black line), the starting material "p-Si large grain KA" (dashed black line) and  $a$ -Si (dotted black line). For longer wavelengths, the refractive index behaves like crystalline silicon whereas below 400 nm the amorphous fraction plays a more crucial role by decreasing  $n$ . Nevertheless, it is close to the characteristic of  $c$ -Si, suggesting a crystalline material with smaller grain sizes. Below 300 nm,  $n$  closely follows the behavior of  $a$ -Si. The extinction coefficient  $k$  is clearly increased in the wavelength range above 370 nm compared to  $c$ -Si. Between 370–300 nm a slightly lower  $k$  than all three forms of Si is found whereas below 300 nm  $k$  lies again between  $a$ -Si and  $c$ -Si.

Even though this models should be taken with care, we conclude that the mp-SiO<sub>x</sub>(n) layer behaves similarly to SiO<sub>x</sub> with  $1 \leq x \leq 2$ , leading to a very low absorption within this layer.

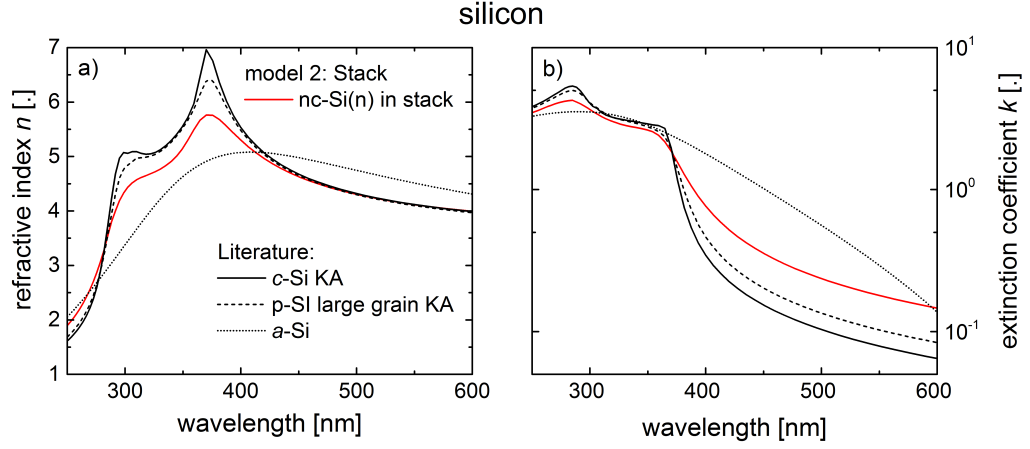


Figure 6.4 – (a) The refractive index  $n$  and (b) the extinction coefficient  $k$  obtained from the ellipsometry measurements modeling the nc-Si(n) layer within the stack (model 2, red). For comparison,  $n$  and  $k$  values from the literature are added in black:  $c$ -Si (solid line [Horiba 1994]), "p-Si large grain KA" (dashed line [Horiba 1994]), and  $a$ -Si (dotted line [Jellison 1996]).

Even though the  $\Gamma_j$  in the nc-Si(n) layer above is similar to other poly-silicon layers in passivating contacts, the mp-SiO<sub>x</sub>(n) layer gives the possibility to increase the thickness of the stack without increasing its parasitic absorption. This can be used for example to decrease the influence of the metallization on the  $c$ -Si/chem-SiO<sub>x</sub> interface, to shift the interference condition for better anti-reflection, or to tune the doping profile inside the wafer, as will be explained in the next section.

## 6.4 Controlling the doping profile by the mp-SiO<sub>x</sub>(n) layer thickness

The diffusion of impurities (non-silicon atoms) in crystalline silicon is driven by the gradients of the concentration profile until equilibrium is reached.

Impurities used as active dopants such as boron (B) or phosphorus (P) mainly replace a silicon atom at its lattice position (substitutional), so that the dopant atom can contribute free electrons or holes to the silicon lattice. The diffusion may follow three mechanisms: i) vacancy – a substitutional atom exchanges lattice position with a vacancy, ii) interstitial – an interstitial atom jumps to another interstitial position, or iii) interstitialcy – a combination of the two mechanisms, such that a silicon self-interstitial displaces a substitutional impurity to an interstitial position; the impurity then may knock a silicon lattice atom into a self-interstitial position again. The diffusion of dopant impurities is closely linked to the presence of vacancies and interstitial point defects, and the probability of jumping from one position to another

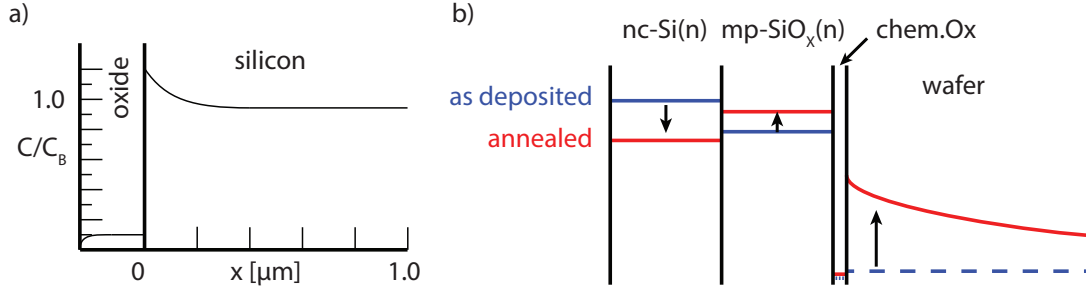


Figure 6.5 – (a) Illustration of phosphorus segregation between oxide and silicon (adapted from [Jones 2008]). (b) Illustration of the phosphorus concentration in the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack in the as-deposited state (blue) and after annealing (red).

increases exponentially with increasing temperature [Jones 2008, Mostafa 2017].

In polycrystalline silicon, diffusion within the grains follows the same characteristics as in a bulk single-crystal material. But at the grain boundaries, diffusion can proceed at 100 times faster and thus dominate the diffusion process. When silicon dioxide is added on the surface in the model, the impurities will redistribute again until equilibrium is reached, whereas the ratio of the impurity concentrations—segregation coefficient  $m$ —in Si and SiO<sub>2</sub> stays constant as defined by the formula [Jones 2008]:

$$m = \frac{\text{Equilibrium concentration of impurity in silicon}}{\text{Equilibrium concentration of impurity in silicon dioxide}} \quad (6.1)$$

Another factor that effects the redistribution of impurities is the diffusivity within silicon dioxide: a low diffusivity means the impurity is rejected by the oxide. In the case of phosphorus, the segregation coefficient is 10, meaning that the equilibrium concentration in silicon is 10 times higher than in SiO<sub>2</sub> with a low diffusivity [Grove 1964, Jones 2008]. This is one of the reasons why the diffusion of P out of POCl<sub>3</sub> gas works well since the P atoms are pushed out of the phosphor-silica-glass (PSG, mixture of P<sub>2</sub>O<sub>5</sub> and SiO<sub>2</sub>) which is grown at the surface. In Figure 6.5a the redistribution of P at silicon–SiO<sub>2</sub> interface is illustrated.

In the case of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack, the situation is a bit more complex. The silicon is present mainly in amorphous form and can therefore contain a considerably higher amount of P compared to *c*-Si, in which the solubility is limited [Solmi 1996, Nobili 1982, Olesinski 1985]. The exact limit is still under discussion, as is well reviewed by [Mostafa 2017]. In Figure 6.5b, the P concentrations within the layer stack in the as-deposited state as well as after annealing are sketched.

In the as-deposited state, only the background doping (either B or P) is present within the wafer. The chem-SiO<sub>x</sub> is intrinsic and only a small amount of P is introduced during the PECVD deposition. From the EDX measurements presented in chapter 3, we can estimate the

#### 6.4. Controlling the doping profile by the mp-SiO<sub>x</sub>(n) layer thickness

concentrations for mp-SiO<sub>x</sub>(n) and nc-Si(n).

The deposited silicon oxide in the mp-SiO<sub>x</sub>(n) layer is highly-doped with a concentration of  $\sim 2 \cdot 10^{20} \text{ cm}^{-3}$  increasing to  $\sim 3 \cdot 10^{20} \text{ cm}^{-3}$  in the nc-Si(n) layer. After annealing, the concentration of the nc-Si(n) decreased to  $\sim 1.5 \cdot 10^{20} \text{ cm}^{-3}$  and the concentration in the mp-SiO<sub>x</sub>(n) layer increased slightly with a maximum at  $\sim 2.5 \cdot 10^{20} \text{ cm}^{-3}$ . We relate the decrease in the nc-Si(n) layer towards the mp-SiO<sub>x</sub>(n) layer to a high diffusivity of the P due to the limited solubility within the crystalline grains [Sadovnikov 1991]. The intrinsic chem-SiO<sub>x</sub> remains P depleted whereas within the wafer a P profile is built up with a concentration decreasing away from the wafer surface.

In section 5.4 we discussed the influence of the PH<sub>3</sub> flux during the PECVD deposition of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack and the annealing dwell time on the resulting phosphorus profile within the wafer. However, the doping profile is influenced by more parameters than just the doping and the annealing temperature and time. We have observed that the wafer polarity and resistivity have a strong impact on the doping profile as well. Figure 6.6 shows the phosphorus doping profiles diffused from mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer with 12 nm mp-SiO<sub>x</sub>(n) (120 s) and 17 nm nc-Si(n) (210 s). The different characteristics represent p-type wafers as well

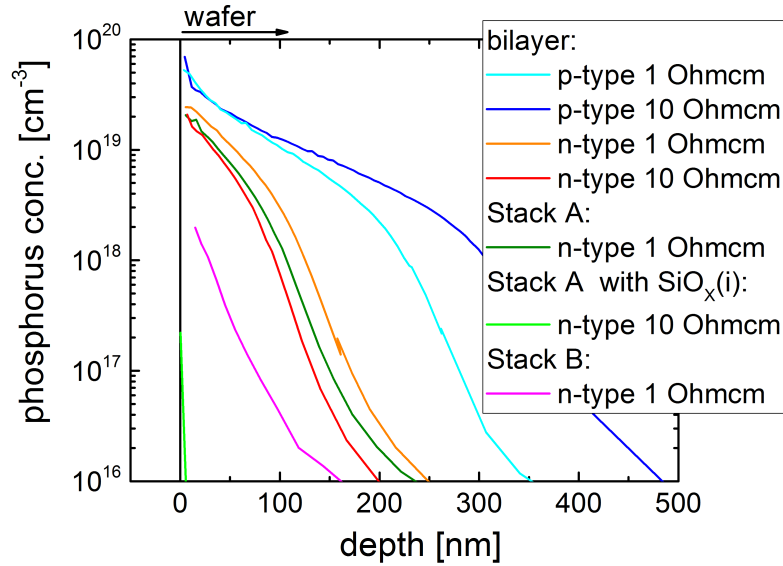


Figure 6.6 – The phosphorus profile for the mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer stack on p-type wafer as well as on n-type wafer using for both polarities two different base resistivities of 1 Ω cm and 10 Ω cm, respectively. The doping profiles are set in comparison to the two stacks with alternating mp-SiO<sub>x</sub>(n) and nc-Si(n) layers as sketched in Figure 6.7. Additionally the doping profile is shown using stack A without doping in the mp-SiO<sub>x</sub>(i) layers.

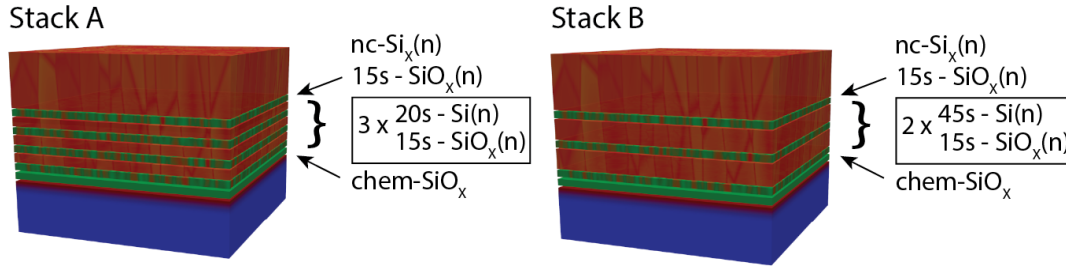


Figure 6.7 – Two different layer stacks are sketched with alternating mp-SiO<sub>x</sub>(n) and nc-Si(n) layers covered by the same nc-Si(n) layer as for the bilayer stack.

as n-type wafers, additionally using base resistivities of 1  $\Omega$  cm and 10  $\Omega$  cm for both polarities. These samples were co-processed, meaning that the chem-SiO<sub>x</sub> layers were grown in the same bath, the layer stacks were grown in the same PECVD run, and all of them were annealed in the same batch. Using a 10  $\Omega$  cm p-type wafer (dark blue) results in a deeper profile than using a 1  $\Omega$  cm p-type wafer (light blue) even though the interface concentrations are similar.

For the n-type wafer the behavior is different, the 1  $\Omega$  cm wafer (orange) yields a deeper profile than for the 10  $\Omega$  cm wafer (red). Comparing n- and p-type wafers a much stronger in-diffusion is observed for the p-type wafer in terms of depth as well as surface concentration. Similar results were observed for boron diffusion. Wafer resistivity and polarity do not influence diffusion when the chem-SiO<sub>x</sub> is removed by an HF dip before the PECVD deposition. However, we found that wafer polarity and resistivity influence the thickness of the interfacial oxide. Therefore, we assume that the differences shown in Figure 6.6 are mainly related to the properties of diffusion through the interfacial oxide.

When a slight change in the chem-SiO<sub>x</sub> influences the doping profile strongly, what then is the influence of the SiO<sub>x</sub> on the mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer stack? Another interesting observation came to our mind when stacks with alternating thin mp-SiO<sub>x</sub>(n) and nc-Si(n) layers were analyzed as sketched in Figure 6.7. In stack A, on top of the chem-SiO<sub>x</sub> three times 15 s mp-SiO<sub>x</sub>(n) and 20 s nc-Si(n) layer are altered, followed by another 15 s mp-SiO<sub>x</sub>(n) underneath the covering thick nc-Si(n) layer on top. In stack B the alternating part varies to two times 15 s mp-SiO<sub>x</sub>(n) and 45 s nc-Si(n) layer instead. So the silicon content is increased in B compared to A. It is important to mention that both, the mp-SiO<sub>x</sub>(n) as well as the nc-Si(n) layer, are highly-doped with phosphorus. From the EDX measurements presented in chapter 3 we expect a higher phosphorus concentration implemented into the nc-Si(n) layer than into the mp-SiO<sub>x</sub>(n). The doping profiles of stack A (dark green) and stack B (magenta) are added to Figure 6.6 in comparison to the bilayer stacks.

Interestingly, stack B with its higher silicon content clearly diffused a lower amount of phosphorus into the wafer than stack A. Comparing them to the bilayer structure, on the same wafer polarity and resistivity, which has the lowest silicon content in the bottom layer, an

#### 6.4. Controlling the doping profile by the mp-SiO<sub>x</sub>(n) layer thickness

even deeper profile is observed. Therefore, the doping profile is not primarily determined by the amount of P in the layer, but by the mobility and diffusivity of P within the layer stack and towards the wafer. An explanation could be that in the stack B, the nc-Si(n) layers sandwiched between the oxide layers are thick enough so that the P can pile up to high concentrations due to the segregation coefficient, leaving "emptied" silicon oxide layers in between and thus blocking the diffusion towards the wafer.

In stack A on the other hand, the silicon layers are too thin and not separated enough for such a high concentration difference to seriously pile up, similar to the self-purification effect observed in Si nanocrystals where a decreasing P-concentration is observed with decreasing NC size [Dalpian 2006, Hiller 2017, Gutsch 2012]. This would implicate that the silicon oxide layers within Stack A do not get depleted and the P within the whole alternating stack is pushed towards the wafer, acting—in terms of diffusivity—as one doped silicon oxide layer. The cover nc-Si(n) layer acts as a reservoir with an expulsion characteristic due to the crystallization, refilling the empty sites left behind by the P atom diffused to the wafer leading to kind of channels for the P to diffuse through the mixed phase silicon oxide matrix.

The role of P already existing in the deposited mp-SiO<sub>x</sub>(n) is analyzed by replacing for example the mp-SiO<sub>x</sub>(n) layers in stack A by intrinsic mp-SiO<sub>x</sub>(i) layers (Figure 6.6, light green). This resulted in a drastically decreased P diffusion to the wafer. Similar tests (not shown here) show that an intrinsic layer of 15 s mp-SiO<sub>x</sub>(i) is enough to block almost completely the P diffusion to the wafer, similar to the case of the chem-SiO<sub>x</sub> where slight changes in thickness or density have a strong influence on the doping profile. Therefore, the fact that P is already present in the deposited silicon oxide helps for the diffusion during the annealing. This gives the possibility to tune the doping profile accordingly by introducing an adequate mp-SiO<sub>x</sub> layer either intrinsic or doped.

The influence of the mp-SiO<sub>x</sub>(n) and the nc-Si(n) on the doping profile are further investigated by performing a series in which the mp-SiO<sub>x</sub>(n) thickness (in terms of deposition time) is varied (15 s, 40 s, 65 s, 90 s, 120 s), keeping the nc-Si(n) deposition time constant (210 s) and vice versa keeping the mp-SiO<sub>x</sub>(n) thickness constant (15 s) varying the nc-Si(n) deposition time (210 s, 249 s, 288 s, 328 s, 375 s). Again, both the mp-SiO<sub>x</sub>(n) as well as the nc-Si(n) layers are highly-doped with phosphorus. For this series 250-μm-thick 2 Ω cm p-type wafers were used, and all the samples were annealed together at 900 °C for 15 min.

In Figure 6.8 the resulting doping profiles are shown with increasing nc-Si(n) thickness from light blue to dark blue and increasing mp-SiO<sub>x</sub>(n) thickness from light red to dark red. Interestingly, the increase of the P reservoir by increase of the nc-Si(n) thickness influences the doping profile only very slightly in terms of surface concentration, resulting in a variation from  $2.6 \cdot 10^{17} \text{ cm}^{-3}$  to  $9.8 \cdot 10^{17} \text{ cm}^{-3}$ . At a depth of ~ 70 nm all concentrations decayed below  $1 \cdot 10^{16} \text{ cm}^{-3}$ . However, increasing the mp-SiO<sub>x</sub>(n) thickness, a different behavior is observed. Whereas deposition times of 15 s, 40 s and 65 s mp-SiO<sub>x</sub>(n) lead to very similar results, a higher surface concentration and a deep profile is observed for the sample with 90 s and an even

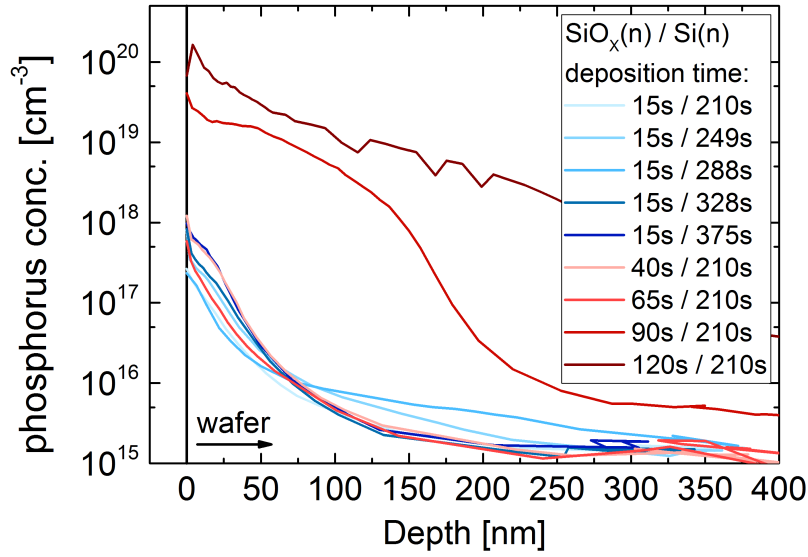


Figure 6.8 – Phosphorus doping profiles for mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer stacks with varying thicknesses of mp-SiO<sub>x</sub>(n) (red) and nc-Si(n) (blue) keeping one of the two layer thicknesses constant.

deeper one for 120 s. Thus, we conclude that the mp-SiO<sub>x</sub>(n) is a more efficient reservoir for P-diffusion than nc-Si(n). This could be related to the more amorphous matrix in the case of mp-SiO<sub>x</sub>(n) compared to nc-Si(n) or due to the low diffusivity within silicon oxide which rejects P with increasing temperature. Additionally, the more pronounced in-diffusion could also be related to an increase in defects close to the interface which play a major role in the diffusion mechanism [Uematsu 1997]. Further investigations and dedicated experiments would be needed to understand the diffusion mechanism within this mixed-phase material which are beyond the scope of this thesis.

## 6.5 Transmittance, reflectance and absorptance in the as-deposited state.

We investigated the optical properties of our mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stacks in the as deposited state by adding a transparent glass substrate during the PECVD deposition. Figure 6.9 shows the transmittance (T) and reflectance (R) of this series together with the calculated absorptance (A) using the formula  $1 = T + R + A$ . By increasing the deposition time of the nc-Si(n) layer from 210 s (light blue) to 375 s (dark blue) the absorptance below 500 nm is clearly increased as expected due to parasitic absorption in silicon. By increasing the deposition time for the mp-SiO<sub>x</sub>(n) from the same starting point with 15 s (light blue) over 40 s (light red) to 120 s (dark red), the absorptance is not changing. This illustrates that in the

### 6.5. Transmittance, reflectance and absorptance in the as-deposited state.

as-deposited state the oxygen content is high enough in the mp-SiO<sub>x</sub>(n) layer to make it highly transparent.

To further investigate the effect of the O content, the ratio of SiH<sub>4</sub>/CO<sub>2</sub> was varied for the mp-SiO<sub>x</sub>(n) layer, keeping its deposition time of 120 s. The covering layer of nc-Si(n) was also kept the same, using a deposition time of 210 s. Panel d) in Figure 6.9 shows a variation of the CO<sub>2</sub> flux varied from 5 sccm (light green) to 20 sccm (dark green), keeping a constant silane flux of 15 sccm. A clear reduction is observed from 5 sccm to 10 sccm whereas additional CO<sub>2</sub> beyond 10 sccm has no influence on absorption anymore.

Increasing the silane flux to 20 sccm and additionally varying the CO<sub>2</sub> flux from 10 sccm (light brown) to 20 sccm (dark brown), results in less transparent layers. Comparing the two samples with a silane/CO<sub>2</sub> ratio of 1, the one with lower fluxes (15/15) is more transparent which could be due to a thinner resulting layer. Probably the available silicon during the deposition is determining the silicon content whereas additional available CO<sub>2</sub> is not built into the layer and is pumped away. This assumption is supported by the fact that no change was observed for 15 sccm silane when the CO<sub>2</sub> flux increased from 10 to 20 sccm. Although the influence of the mp-SiO<sub>x</sub>(n) thickness was previously observed to be negligible, our assumption for the higher absorption using (20/20) is the higher silicon content, meaning that the silicon

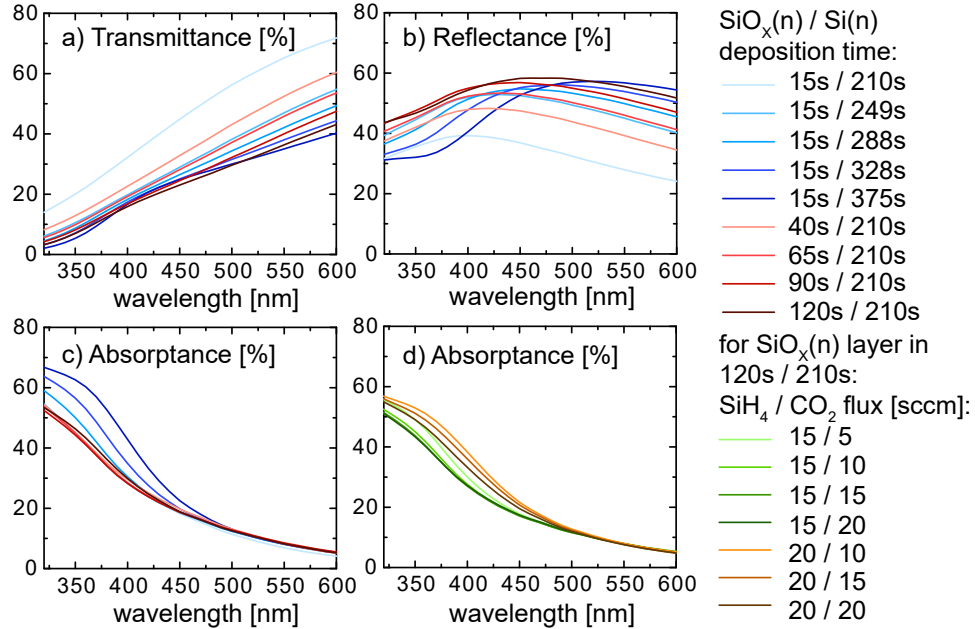


Figure 6.9 – (a) Transmittance, (b) reflectance and (c) absorptance in the as-deposited state using varying deposition times of the mp-SiO<sub>x</sub>(n) (red) and nc-Si(n) (blue) layer, respectively. (d) The absorptance in the as deposited state varying the SiH<sub>4</sub>/CO<sub>2</sub> flux for a deposition time of 120 s / 210 s.

available during the deposition determines the silicon content, whereas additional available  $\text{CO}_2$  is not built into the layer and is pumped away. This assumption is supported by the observation that no change was observed for 15 sccm silane between 10 to 20 sccm  $\text{CO}_2$  flux.

## 6.6 From layers to cells — a sensitive matter

Since in our laboratory no boron-diffused emitter was available to test this mp- $\text{SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  layer stack in a complete solar cell, two other strategies were followed for the implementation into working devices. First, a so called hybrid cell was used where an  $a\text{-Si}(\text{i})/a\text{-Si}(\text{p})$  rear heterojunction was added at low temperature after the front side high temperature processes are finished. Second, the mp- $\text{SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  layer stack was combined with a boron-doped passivating contact; this approach will be called "co-annealed" hereafter. We start with a description of the hybrid cell since this device design was available earlier in the thesis.

### 6.6.1 Silicon oxide protection layer for the rear

Most of the investigations presented so far were done using symmetrical samples having the mp- $\text{SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  on both sides of the wafer. For the integration in cells only one side is processed, the other is covered only by the chem- $\text{SiO}_x$ . However, we noticed that the process depends on the history of the tube furnace, i.e. whether it was used for oxidation of  $\text{POCl}_3$  diffusion before the annealing of our mp- $\text{SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  stack. Therefore, a layer was developed to protect the rear side from impurities such as the in-diffusion of residual

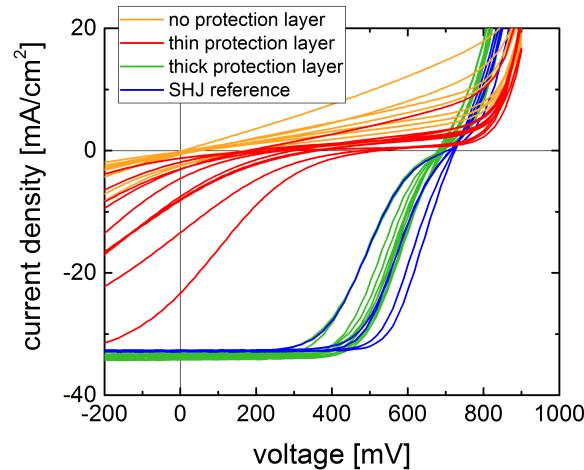


Figure 6.10 –  $J$ - $V$  characteristics for planar hybrid cells protecting the rear during annealing only by the chem- $\text{SiO}_x$  (orange), a thin protection layer (red) or by a thick protection layer (green). For comparison a co-processed SHJ reference cell (blue) is added.

phosphorus. As we have seen in section 6.4, an intrinsic amorphous silicon oxide layer can block diffusion of P efficiently and when optimized accordingly, it is easy to remove it afterwards by hydrofluoric acid (HF). Thus, after finishing the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack dedicated to the front, the wafer were flipped and a protection layer was deposited to the rear. Two different thicknesses — ~4 nm and ~50 nm — were tested together with wafers having no protection layer. After annealing at 900 °C for 15 min, a one-sided HF-etch was applied to the rear and a heterojunction was deposited. For comparison, a reference with a low-temperature front-heterojunction was added to the deposition. The cells are finished as described in the experimental section with sputtered ITO and screen-printed fingers at the front and sputtered ITO/Ag at the rear followed by curing for 30 min at 210 °C.

In Figure 6.10 the *J-V* characteristics are shown. A huge series resistance is observed for the cells without (orange) and with a thin protection layer (red), such that almost no current is extracted. This is explained by a blocking junction due to a P-diffused region below the i/p-junction at the rear. The cells with a thicker protection layer (green) follow the same characteristics of the SHJ reference cells (blue), meaning that the P diffusion is blocked completely. Note that the residual S-shape for the thick protection layer and the SHJ reference is explained by an ignition problem of the i-layer deposition. We conclude that an amorphous silicon oxide layer of appropriate thickness sufficiently blocks phosphorous diffusion of the POCl<sub>3</sub> annealing. This protection layer is now used frequently in the lab.

### 6.6.2 Transfer to textured surfaces and cleaning of the rear

Ultimately, the front contact must be applied to textured surfaces like the <111> oriented facets obtained by KOH etching of <100> oriented wafers. Since the surface area of a textured cell is increased compared to a planar surface, the deposition time must be accordingly adjusted. From experience in the fabrication of silicon heterojunction (SHJ) cells, a multiplication factor of 1.7 is recommended. In first tests on 230-μm-thick n-type wafers with a base resistivity of 3 Ω cm, the bilayer stack with 120 s mp-SiO<sub>x</sub>(n) and 210 s nc-Si(n) layer deposition time was scaled by 1, 1.4, 1.7 and 2. Interestingly, a good level of passivation was found already after annealing at 900 °C for 15 min before hydrogenation. Figure 6.11 shows effective lifetimes  $\tau$ , extracted at a carrier density of  $1 \cdot 10^{15} \text{ cm}^{-3}$ . Increasing the deposition time of both layers by a factor of 1 (black), 1.4 (red), 1.7 (blue) lead to an increase in passivation with best passivation for a factor of 2 (green) with  $\tau = 1033 \mu\text{s}$  and  $iV_{\text{OC}} = 690 \text{ mV}$ . After performing an FGA of 30 min at 500 °C an increase in passivation is observed for all scaling factors leading for the thickest sample to  $\tau = 1999 \mu\text{s}$  ( $iV_{\text{OC}} = 704 \text{ mV}$ ).

The symmetrical samples were then cut into quarters to investigate the influence of possible cleaning processes before the rear side processing (the plotted values in Figure 6.11 after FGA are for each quarter, whereas the values mentioned in the section before are measured in the middle of the wafer). For the cleaning, two different solutions were applied: either 10 min standard clean 2 (SC2) based on H<sub>2</sub>O<sub>2</sub>-HCl-H<sub>2</sub>O for metal impurity removal

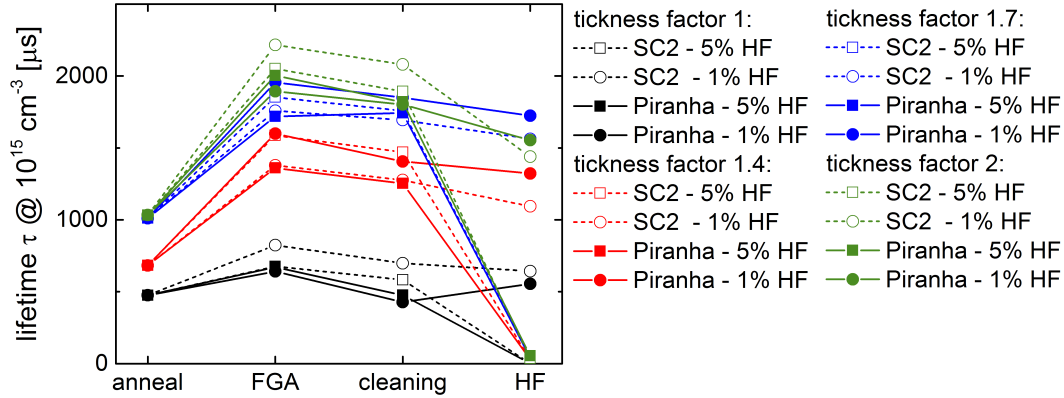


Figure 6.11 – Lifetime evolution on textured surfaces with varying thickness factor multiplying the deposition time of 120 s mp-SiO<sub>x</sub>(n) and 210 s nc-Si(n) layer going from flat substrates to textured ones. Two different cleaning procedures—SC2 (open symbols, dashed lines) and Piranha (filled symbols, solid lines)—are followed by two different dilutions of HF in water—5 vol.-% (squares) and 1 vol.-% (circles).

[Kern 1990, Itano 1993, Kern 1993] or 10 min in a so called piranha solution [Kern 1993] based on H<sub>2</sub>O<sub>4</sub>-H<sub>2</sub>O<sub>2</sub> for the removal of organics. In both cases, the surfaces get lightly oxidized. Both etching processes result in a slight decrease in lifetime (Figure 6.11) with no clear difference between the two. The cleaning was followed by a 20 s etch in hydrofluoric acid (HF). After etching in 5% solution, lifetimes below 60  $\mu\text{s}$  suggest a complete loss of passivation. Section 3.7 showed that this kind of etching penetrates the structure down to the wafer surface. After etching in 1% solution, passivation is not degraded as severely, but we note that the layer stack is more strongly affected by the SC2 clean than the Piranha solution.

To determine the maximal etching time in diluted HF (1 vol.-%), subsequent etching was performed tracking the lifetime at an excess-carrier density of  $1 \cdot 10^{15} \text{ cm}^{-3}$ , but without cleaning process after the FGA (Figure 6.12). In this experiment, etching was applied to mp-SiO<sub>x</sub>(n) layers without any covering layer (black), and with cover layers of  $\sim 17 \text{ nm}$  nc-Si(n) (blue), of  $\sim 10 \text{ nm}$  *a*-Si(n) (orange) and of  $\sim 20 \text{ nm}$  *a*-Si(n) (red), using  $\langle 111 \rangle$ -textured 230- $\mu\text{m}$ -thick n-type wafers with a base resistivity of 3  $\Omega \text{ cm}$ . The mentioned thicknesses of *a*-Si(n) are calculated from deposition rates extracted from thicker layers on flat substrates using a scaling factor of 1.7 for the use on textured surfaces. Sketches of this layer stack with SEM images of the corresponding surfaces can be found in section 3.8. The layer stack with an *a*-Si(n) seed layer is not investigated here since this is not yet optimized and performed poorly in terms of passivation. Amorphous silicon layers were chosen because we expected better coverage on the rough mp-SiO<sub>x</sub>(n) layer. Unfortunately, this is not the case as observed in Figure 3.15.

In Figure 6.12a a clear gain in etching stability is observed with the thicker cover layer whereas

## 6.7. Influence of mp-SiO<sub>x</sub>(n) and nc-Si(n) layer thickness on cell level

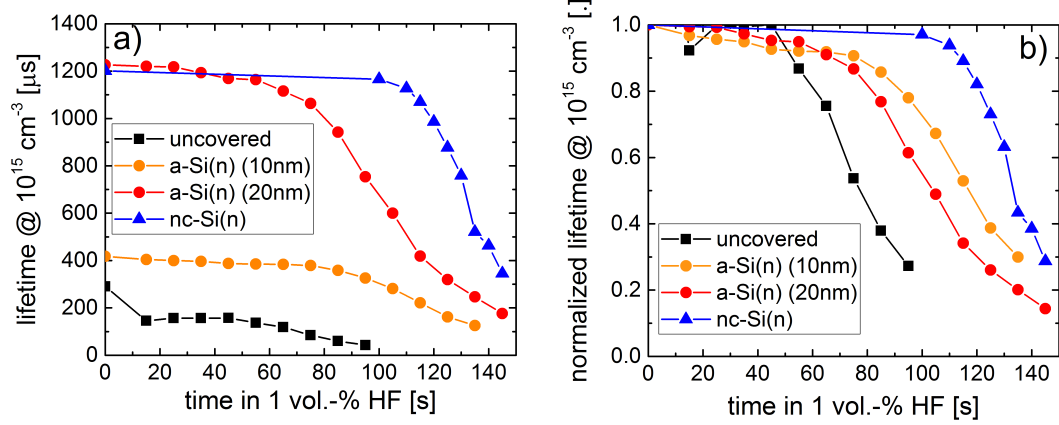


Figure 6.12 – Lifetime evolution on textured surfaces for subsequent etching in a solution of HF diluted in H<sub>2</sub>O (1 vol.-%) for the uncovered mp-SiO<sub>x</sub>(n) layer (black) compared to three different cover layers:  $\sim 10 \text{ nm } a\text{-Si}(n)$  (orange),  $\sim 20 \text{ nm } a\text{-Si}(n)$  (red), and  $\sim 17 \text{ nm } nc\text{-Si}(n)$ . Panel (a) shows the effective measured lifetimes whereas in (b) the values are normalized with respect to their starting value.

the 20-nm-thick layer perform after FGA similarly than the  $nc\text{-Si}(n)$  layer. In terms of stability we focus on the lifetime normalized with respect to its starting value after FGA shown in Figure 6.12b. As expected is the stability against HF of the uncovered layer limited to only about 40 s. Coverage by  $a\text{-Si}(n)$  leads to a slight increase to about 80 s independent of its thickness and another increase is reached by the  $nc\text{-Si}(n)$  cover. The higher stability of the  $nc\text{-Si}(n)$  layer can be explained by the better coverage of the mp-SiO<sub>x</sub>(n) layer as discussed in section 3.8.

## 6.7 Influence of mp-SiO<sub>x</sub>(n) and nc-Si(n) layer thickness on cell level

The series discussed in section 6.5 and section 6.4 was tested in hybrid solar cells. Planar 250- $\mu\text{m}$ -thick p-type wafers were used with a base resistivity of  $2 \Omega \text{ cm}$ , no protection layer at the rear was present during the annealing at  $900^\circ \text{C}$  for 15 min which was followed by an FGA. After a one-sided HF-etch, the  $a\text{-Si}(i)/a\text{-Si}(p)$  SHJ rear was deposited followed by an HF-etch (1 vol.-%) until the mp-SiO<sub>x</sub>(n)/ $nc\text{-Si}(n)$  showed hydrophobic behavior. 80 nm ITO was sputtered on the front and 130 nm on the rear. The solar cells were then finished by sputtering a silver reflector on the rear side and screen printing an Ag grid on the front, followed by curing for 30 min at  $210^\circ \text{C}$  in a belt furnace. A sketch of the finished cell can be found in Figure 5.8.

A strong loss in passivation was observed after HF-etch as well as induced by the sputtering of the front electrode, which is related to the effects presented in section 3.7. Thus, an extraction of  $V_{\text{OC}}$  at mpp is not meaningful ( $J$ - $V$  characteristics not shown); nevertheless, we can extract

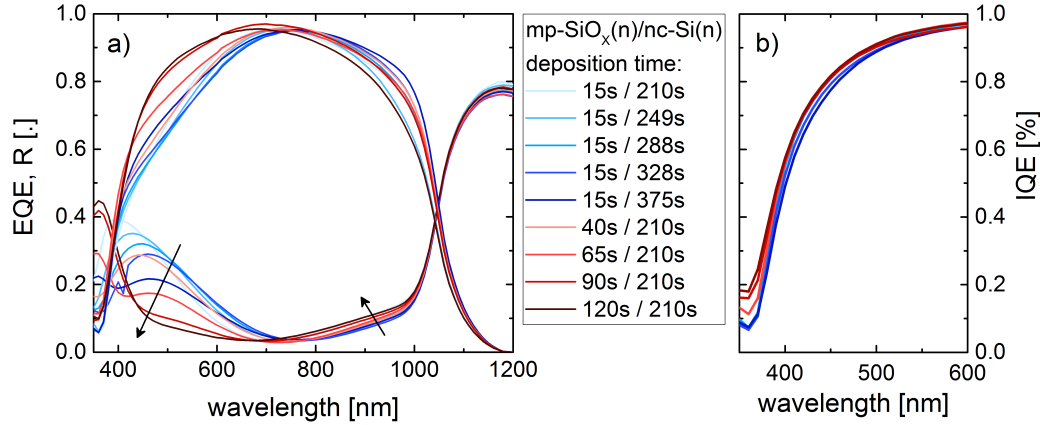


Figure 6.13 – (a) External quantum efficiency (EQE) and reflectance (R) for the series with varying mp-SiO<sub>x</sub>(n) (red) and nc-Si(n) (blue) deposition times, keeping the other one constant, and in (b), the calculated internal quantum efficiency for the range of 350–600 nm.

information on the optical properties since external quantum efficiency (EQE) measurements are carried out at short-circuit condition. Panel a) of Figure 6.13 shows that the EQE below 700 nm is strongly dominated by the reflectance, therefore the internal quantum efficiency ( $IQE = EQE / (1 - R)$ ) is shown in panel b). We restrict the data to the spectral region between 300 and 600 nm, for longer wavelengths it is dominated by recombination at the rear. In the IQE, increasing the nc-Si(n) deposition time leads to a decrease in IQE between 400–600 nm whereas an increase of the mp-SiO<sub>x</sub>(n) deposition time results in an very similar blue response for all thicknesses. This suggests that parasitic absorption in the mp-SiO<sub>x</sub>(n) layer is negligible, the observed absorption losses occur in nc-Si(n) cover layer.

The reflectance measurements were reproduced by simulations using OPAL [PVLighthouse 2018b, McIntosh 2012] for the whole series. Shading losses of 3% were subtracted from the measured reflectance in order to take into account the front grid which is not simulated in OPAL, subsequently the EQE was corrected by a factor of 1.03 for calculating the IQE. The layer stack was chosen as depicted in Figure 6.14, starting with the c-Si substrate

Superstrate		Air	▼	[ ]	
x Film 1	84	<input type="checkbox"/>	ITO	▼	Sputtered 1.0e20 [Hol13]
x Film 2	23	<input type="checkbox"/>	Custom	▼	nc-Si(n)
x Film 3	12	<input type="checkbox"/>	Custom	▼	mp-SiOx(n)
x Film 4	1.2	<input type="checkbox"/>	SiO2	▼	Thermal [Pal85e]
Substrate		Si	▼	Crystalline, 300 K [Gre08]	

Figure 6.14 – Layer stack used for reflectance modeling in OPAL. Here for the example of 120 s/210 s SiO<sub>x</sub>(n) using the thicknesses summarized in table 6.1.

## 6.7. Influence of mp-SiO<sub>x</sub>(n) and nc-Si(n) layer thickness on cell level

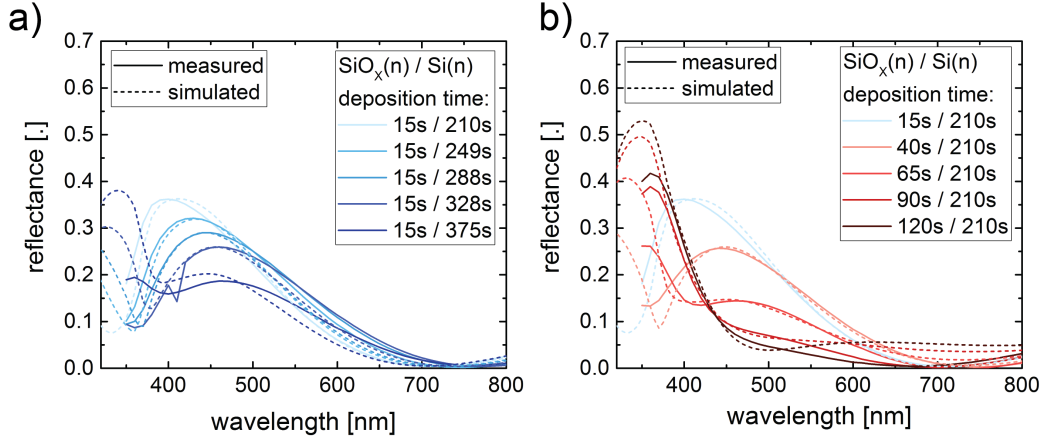


Figure 6.15 – The measured reflectance (solid line) together with the modeled reflectance (dashed line) obtained from simulations using OPAL [PVLighthouse 2018b] for the series varying the nc-Si(n) deposition time keeping the mp-SiO<sub>x</sub>(n) deposition time constant at 15 s (a, blue) and for the variation in mp-SiO<sub>x</sub>(n) deposition time keeping nc-Si(n) deposition at 210 s (b, red).

[Green 2008], covered by 1.2 nm SiO<sub>2</sub> [Palik 1998]. The bilayer stack was modeled using the  $n$  and  $k$  data obtained from the ellipsometry measurements of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack on the example of 120 s / 210 s (red and green curves in Figure 6.2 and Figure 6.4, respectively). For the ITO, the data from [Holman 2013] with a carrier density of  $1 \cdot 10^{20} \text{ cm}^{-3}$  was used.

The resulting simulations (dashed lines) are plotted together with the measured reflectances (without shading losses, solid lines) in Figure 6.15. For the simulations, the same materials were used for the whole series and only the thicknesses were adapted to the corresponding sample structure. We would like to remind the reader that this model is strongly simplified and that it meets only partly the requirements for this complex mixed-phase material such as its strong surface roughness and the absence of clear interfaces between the layers. From the structure of the mp-SiO<sub>x</sub>(n) layer presented in chapter 3 we would also expect a change in optical properties with increasing deposition time and therefore silicon content.

Nevertheless, the reflectance can be modeled quite adequately using the material properties found by ellipsometry. For the variation in nc-Si(n) deposition time, we note that the maxima of the fitted curves slightly offset towards higher wavelength for the thinner layers which changes to an offset towards lower wavelength with increasing thickness. Above 450 nm the trend is opposite with an offset of the curves to lower reflectance and wavelength. This trend is strongly depending on the ITO, for which literature values were taken which may differ slightly from the used ITO in the measurements. This can also be the reason for the shift of the minimum of the simulated curves of  $\sim 50 \text{ nm}$  to lower wavelength. The resulting modeled thicknesses for the whole series are summarized in table 6.1. The deposition time of 15 s

resulted in a mp-SiO<sub>x</sub>(n) layer with thickness of 0.5 nm with a good agreement within the nc-Si(n) thickness variation. From the deposition time we would have expected a thicker layer of 1–2 nm. The higher oxygen content in the beginning of the deposition resulting in a slight change in refractive index could be an explanation. The fitted thicknesses of the nc-Si(n) layers vary more strongly than expected. From the TEM images of 210 s nc-Si(n) on top of 120 s mp-SiO<sub>x</sub>(n) presented in chapter 3, a thickness of ~17 nm was determined. We relate this lower thickness partly to the HF etch penetrating the structure and to the roughness which end up in a not well defined interface with the ITO. This could also be the reason for the variation in ITO thickness which is depicting more changes in surface roughness than real variations in thickness.

Table 6.1 –

Thicknesses used for the simulations of the reflectance in OPAL using the model of Figure 6.14

deposition time mp-SiO <sub>x</sub> (n)/ nc-Si(n)	SiO <sub>2</sub> [nm]	mp-SiO <sub>x</sub> (n) [nm]	nc-Si(n) [nm]	ITO [nm]
15 s/210 s	1.2	0.5	10	85
15 s/249 s	1.2	0.5	14	87
15 s/288 s	1.2	0.5	17	88
15 s/328 s	1.2	0.5	21	90
15 s/375 s	1.2	0.5	27	85
40 s/210 s	1.2	2	17	88
65 s/210 s	1.2	5.5	21	85
90 s/210 s	1.2	9.5	23	85
120 s/210 s	1.2	12	23	84

For lower thicknesses of the mp-SiO<sub>x</sub>(n) (right side of Figure 6.15) the simulation represent the measurement well up to wavelengths of ca. 800 nm. For thicker mp-SiO<sub>x</sub>(n) layers, deviations of the model from the measurements are observed for longer wavelengths. The thicker the layer, the stronger the deviations, and the earlier (lower wavelength) their onset. We relate this to the hard interface used in the model which could not reflect the mixed-phase nature and therefore the smooth index change at the mp-SiO<sub>x</sub>(n)/ nc-Si(n) interface which is responsible for the low reflectance over a broad wavelength range. The thicknesses of the modeled mp-SiO<sub>x</sub>(n) layers are well in agreement with expected values from the deposition time with the 12 nm for 120 s. This is no surprise since this value was measured by TEM and consequently it was fixed for obtaining the *n* and *k* data in ellipsometry modeling. Nevertheless, the effective use of this data in combination with an ITO in finished solar cells strengthen the functionality of the obtained optical properties for the mp-SiO<sub>x</sub>(n) layer.

OPAL can also be used to analyze the transmission through the modeled layer stack— meaning the photon flux reaching the wafer — which would be represented by the IQE when

## 6.7. Influence of mp-SiO<sub>x</sub>(n) and nc-Si(n) layer thickness on cell level

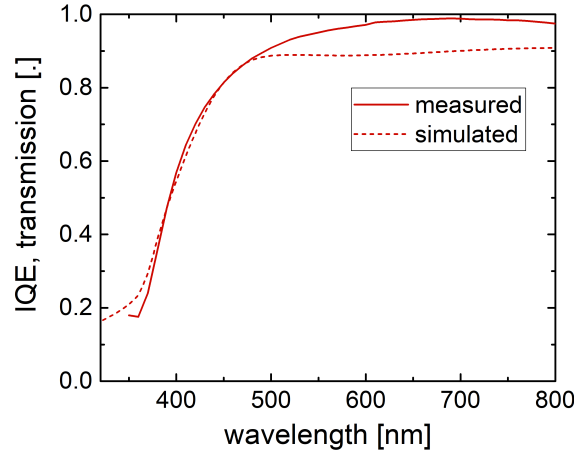


Figure 6.16 – The internal quantum efficiency (IQE) for 120 s / 210 s SiO<sub>x</sub>(n) (solid line) in comparison with the corresponding simulation in OPAL (dashed line) for the transmission through the layer stack reaching the wafer.

recombination effects are neglected. In Figure 6.16 the IQE of the sample with deposition times 40 s / 210 s (light red, solid line) and 120 s / 210 s (dark red, solid line) are plotted in comparison with the corresponding simulation in OPAL (dashed lines) for the transmission through the layer stack. The same model as presented before for the reflectance simulation was used for each of the layer stacks. For the sample 120 s / 210 s SiO<sub>x</sub>(n), the simulation reproduces well the measured IQE below 500 nm whereas the simulation remains at a constant value of 0.9 for longer wavelengths. Only part of the error can be explained by the reflectance which was seen in Figure 6.15 to be simulated too high (absolute  $\sim 0.05$ ). For 90 s / 210 s SiO<sub>x</sub>(n) the same behavior is observed (not shown here) whereas for all other samples the simulated transmission was far beyond a reproduction of the measured IQE.

Therefore the absorption losses of the layer stack are characterized differently. By convoluting the difference between the (1-R)-curve and the EQE with the solar spectrum AM1.5g and integrating, the current losses can be quantified. Since the interest is on losses on the front, wavelength range is restricted to 350–700 nm.

In Figure 6.17 the resulting losses  $J_{\text{abs}}$  are plotted as function of the deposition time for the variation in nc-Si(n) panel (a), and for mp-SiO<sub>x</sub>(n) in panel (b). As a guidance, the top-axis is set to the expected thickness as calculated from TEM images, i.e. 12 nm for 120 s of mp-SiO<sub>x</sub>(n) deposition and 17 nm for 210 s nc-Si(n) deposition time, assuming linear deposition rates. The 3% shading losses of the silver front fingers result in absolute losses of 0.6 mA/cm<sup>2</sup> between 350–700 nm. About  $\sim 0.11$  mA/cm<sup>2</sup> losses are assumed resulting from an OPAL simulation with 80 nm ITO thickness.

For the nc-Si(n) thickness variation (blue) a linear behavior is observed with a loss of

$0.4 \text{ mA/cm}^2$  per 10 nm. For the mp-SiO<sub>x</sub>(n) layer (red) only a small change in losses is observed with increasing thickness. Taking a linear increase from thinnest to thickest leads to a slope of  $0.07 \text{ mA/cm}^2$  per 10 nm, pointing towards very transparent layers. In Figure 6.17c, the absorption losses in the two individual layers are compared to *c*-Si (black, obtained from simulation in OPAL using *n* and *k* from [Green 2008]) with a slope of  $0.11 \text{ mA/cm}^2$  per 10 nm and reported values for poly-Si(n) (green, [Feldmann 2016]) with  $0.5 \text{ mA/cm}^2$  per 10 nm. Please notice that the reported value in [Feldmann 2016] compared the wavelength range 300–700 nm for its thickness series. The lower absorption of the nc-Si(n) layer compared to the reported poly-Si(n) layer could be due to an increased crystallinity as shown in section 3.3 which is achieved on one hand by using a plasma regime supporting crystallization already during deposition and on the other hand by using a higher annealing temperature. The low losses for the mp-SiO<sub>x</sub>(n) layer are promising and show the potential for the application on the front.

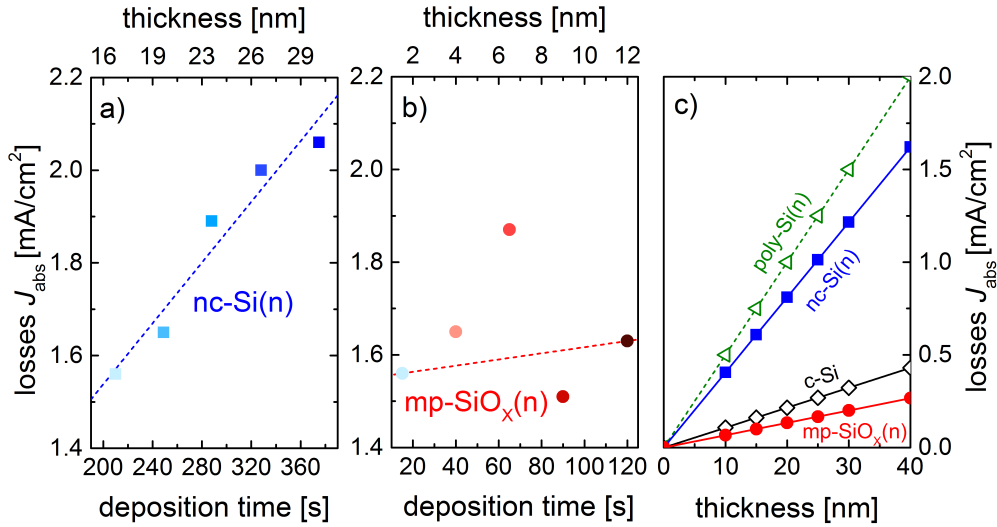


Figure 6.17 – (a) The current losses  $J_{\text{abs}}$  for the nc-Si(n) layer and (b) for the mp-SiO<sub>x</sub>(n) layer as a function of the deposition time and thickness. In (c) the linear increase in absorption with thickness is compared to literature values of *c*-Si [Green 2008] and poly-Si(n) [Feldmann 2016].

## 6.8 Co-annealed solar cells with SiO<sub>x</sub>(i/p) rear

On the basis of the mp-SiO<sub>x</sub>(n)/nc-Si(n) electron-selective emitter discussed here, a boron-doped SiO<sub>x</sub>(i/p) layer was developed for use as hole-selective emitter, using a similar thermal budget. The SiO<sub>x</sub> part of this layer is kept intrinsic due to a better performance which is the reason why it is called SiO<sub>x</sub>(i/p). More information on the development of this layer can be found in [Wyss 2018]. This gave us the opportunity to simplify the fabrication process as explained in section 2.2.2 and to deposit on one side the 120 s / 210 s mp-SiO<sub>x</sub>(n)/nc-Si(n)

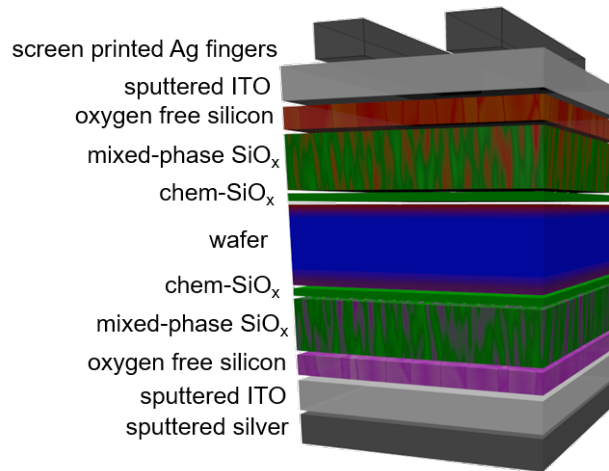


Figure 6.18 – Sketch of the finished co-annealed cell with a hole- and an electron-selective emitter on each side of the wafer.

bilayer and subsequently on the other side the  $\text{SiO}_x(\text{i/p})$  layer. Annealing them together with the rear contact at  $900^\circ\text{C}$  for 15 min in  $\text{N}_2$  atmosphere lead to the formation of a boron and a phosphorus-doped region within opposite sides of the wafer, followed by a FGA at  $500^\circ\text{C}$  for 30 min. The molecular hydrogen in the FGA is mainly improving the  $\text{SiO}_x(\text{n})$  whereas the  $\text{SiO}_x(\text{i/p})$  selective emitter is improving its passivation by hydrogenation using additional PECVD deposited  $\text{SiN}_x$  on both sides of the wafer followed by annealing on a hotplate at  $450^\circ\text{C}$  for 30 min in air. The  $\text{SiN}_x$  layer is a source of atomic hydrogen which is released during the hotplate annealing and diffuses to the wafer / chem- $\text{SiO}_x$  interface. The  $\text{SiN}_x$  is afterwards removed in a  $180^\circ\text{C}$  hot  $\text{H}_3\text{PO}_4$  solution for 30 min [Liu 2007]. After an HF-etch (1 vol.-%) until a hydrophobic n-side is reached, 80 nm ITO was sputtered on the front and 130 nm on the rear. The solar cells were then finished by sputtering a silver reflector on the rear side and screen printing an Ag grid on the front, followed by curing for 30 min at  $210^\circ\text{C}$  in a belt furnace. A sketch of the finished cell can be found in Figure 6.18.

Since these were the first co-annealed cells, the first goal was to figure out which polarization is more transparent to be placed at the front and whether a front-emitter or a rear-emitter performs better. To this end, each of the contact structure— $\text{SiO}_x(\text{i/p})$  and  $\text{SiO}_x(\text{n})$ —was placed on each side of planar wafers of both polarities, both with a thickness of  $280\ \mu\text{m}$  and a base resistivity of  $3\ \Omega\text{cm}$ . The resulting  $J$ - $V$  characteristics for the best cell on each wafer are shown in table 6.2 and Figure 6.19a, in cyan (p-type wafer) and blue (n-type wafer) having the  $\text{SiO}_x(\text{i/p})$  at the front, and in orange (p-type wafer) and red (n-type wafer) having the  $\text{SiO}_x(\text{n})$  at the front, respectively.

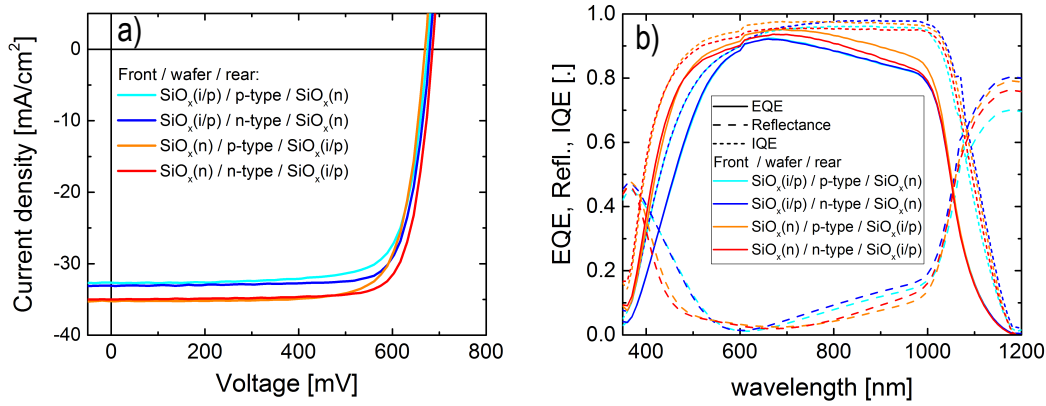


Figure 6.19 – (a)  $J$ - $V$  characteristics for the best cells of the four possible combinations using SiO<sub>x</sub>(i/p) and SiO<sub>x</sub>(n) on the two sides of either a p-type or an n-type wafer. (b) The EQE (solid line), reflectance (dashed line) and IQE (dotted line) of the four cells are shown.

The cells on n-type wafer show slightly better  $V_{OC}$  and  $FF$  compared to p-type, reaching values of 686 mV and 79.6%. The  $J_{SC}$  is clearly enhanced by more than 2 mA/cm<sup>2</sup> using the SiO<sub>x</sub>(n) contact at the front with 35.0 mA/cm<sup>2</sup> compared to the cells with SiO<sub>x</sub>(i/p) at the front with 32.9 mA/cm<sup>2</sup>. In Figure 6.19b the EQE (solid line), reflectance (dashed line) and the IQE (dotted line) are plotted for the four different cells. We observe a lower reflectance with the SiO<sub>x</sub>(n) over a broad wavelength range with a shift of the minimum to slightly higher wavelength. For both contacts, the reflectance above 600 nm is slightly lower for p-type wafer than n-type wafer. Apart from that the samples having SiO<sub>x</sub>(i/p) at the front show the same behavior in front and rear emitter design. For the samples having SiO<sub>x</sub>(n) at the front, the small difference in EQE below 500 nm is related to the difference in reflectance, ending up in the same IQE. Above 500 nm the EQE as well as the IQE are slightly decreased for n-type wafer. At first sight, one would relate this to front side recombination being more pronounced for the rear-emitter cell than the front emitter. However, since a slightly higher  $V_{OC}$  is observed for this sample, and since no passivation problems dominating one side are observed for the other samples, we doubt this explanation and further investigations would be needed to explain this difference.

Table 6.2 –  
 $J$ - $V$  characteristics of co-annealed cells shown in 6.19

front / wafer / rear	$V_{OC}$ [mV]	$J_{SC}$ [mA/cm <sup>2</sup> ]	$FF$ [%]	efficiency $\eta$ [%]
SiO <sub>x</sub> (i/p) / p-type / SiO <sub>x</sub> (n)	676	32.5	76.8	16.8
SiO <sub>x</sub> (i/p) / n-type / SiO <sub>x</sub> (n)	681	32.9	79.4	17.8
SiO <sub>x</sub> (n) / p-type / SiO <sub>x</sub> (i/p)	670	35.0	77.1	18.1
SiO <sub>x</sub> (n) / n-type / SiO <sub>x</sub> (i/p)	686	34.8	79.6	19.0

This series showed that co-annealed cells can reach high efficiencies on planar wafer with working passivation using the same thermal budget. The high  $FF$  of almost 80% are proof for excellent current extraction through the SiO<sub>x</sub>-based contacts. The SiO<sub>x</sub>(n) layer was found to be more transparent which we explain with its higher oxygen content. Additionally, the high  $J_{SC}$  of 35.0 mA/cm<sup>2</sup> is highly promising for a planar solar cell compared with an upper limit of 36.7 mA/cm<sup>2</sup> simulated with ray tracing [PVLighthouse 2018c] for a planar device using an ideal structure of nitride/wafer/nitride/Ag on a 250 μm wafer, including the same shading losses of 3%. And finally the efficiency of 19% for a planar device is encouraging for this co-annealed approach.

## 6.9 Influence of SiH<sub>4</sub> / CO<sub>2</sub> ratio on cell level

As we have seen in section 6.5, the transparency of the mp-SiO<sub>x</sub>(n) layer also depends on ratio of the precursor gases CO<sub>2</sub> and SiH<sub>4</sub>. To investigate this effect after annealing and on the cell level, co-annealed cells are processed with a SiO<sub>x</sub>(i/p) layer at the rear using 200-μm-thick n-type wafers with a base resistivity of 2 Ω cm. For the SiO<sub>x</sub>(n) layer at the front we deposited 120 s mp-SiO<sub>x</sub>(n) with varying ratios of SiH<sub>4</sub>/CO<sub>2</sub>, but we kept the hydrogen flux constant and a deposition time of 210 s was chosen for all nc-Si(n) layers. The co-annealed cells were fabricated and finished as described in the section before 6.8.

In Figure 6.20 the  $J$ - $V$  parameters are shown as a function of the used silane and CO<sub>2</sub> fluxes during PECVD deposition. For a flux of 15 sccm silane SiH<sub>4</sub>, the CO<sub>2</sub> flux is varied from 5 sccm (light green) to 20 sccm (dark green) and for 20 sccm silane between 10 and 20 sccm CO<sub>2</sub>. Please notice the overall slightly lower performance which was observed already when monitoring the lifetime at all process steps which could be related to a change in the base material.

Nevertheless, a clear trend is observed for increasing  $V_{OC}$  values for higher CO<sub>2</sub> fluxes, for the case of 15 sccm as well as for 20 sccm silane. We explain this by a beneficial effect of additionally available oxygen from the mp-SiO<sub>x</sub>(n) layer that enhances the structural stability of the chem-SiO<sub>x</sub>.

Focusing on the  $J_{SC}$ , the increased transparency with increased oxygen content observed in the as-deposited state in section 6.5 is also visible after annealing and in the finished cells. Even though we have to remark that the effect is increased and even dominated by the trend in  $V_{OC}$  as it gets visible taking the EQE measurements (Figure 6.21) into account. Whereas lower CO<sub>2</sub> fluxes decrease the EQE over the full wavelength range, the IQE shows an increase at long wavelength. This suggests recombination losses at the front side since this are rear emitter cells. Nevertheless, we can relate the increase in IQE at longer wavelength for increasing oxygen content to increased transparency of the layers. The reflectance is strongly decreasing below 550 nm with increasing oxygen content and opposite behavior between 550–750 nm. This shows exemplary the additional feature of this layer stack acting like a built-in double anti-reflection coating (ARC).

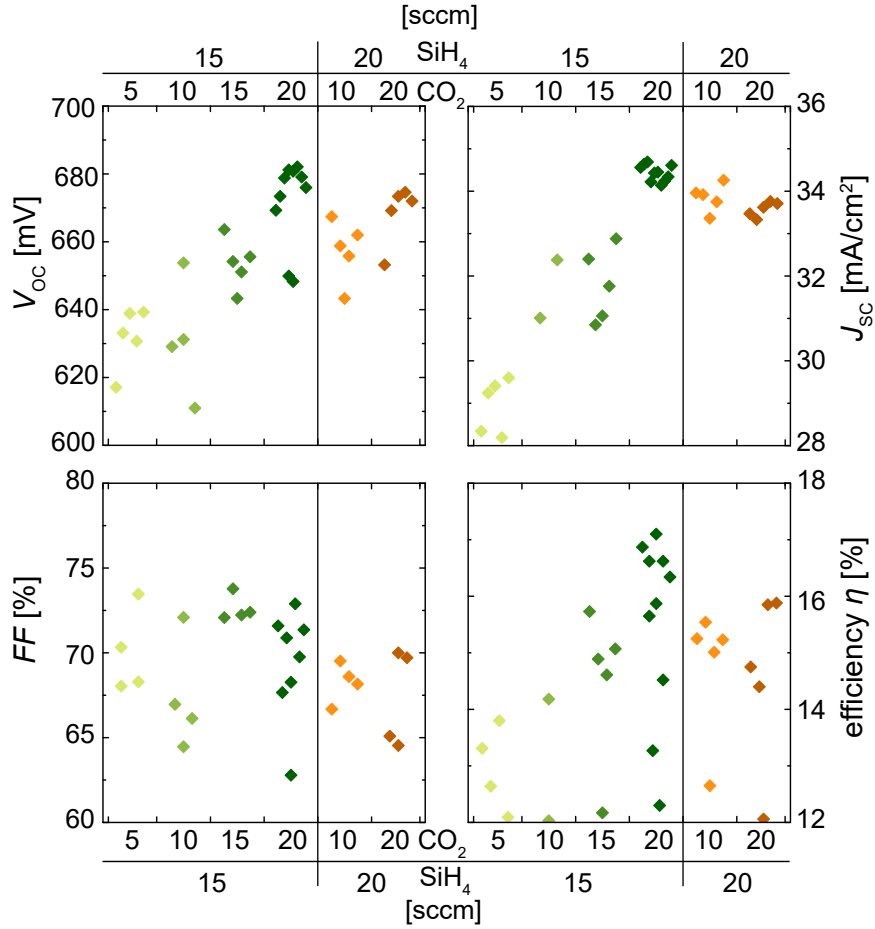


Figure 6.20 –  $J$ - $V$  characteristics as a function of the used  $\text{CO}_2$  fluxes during PECVD using 15 sccm silane (green) and 20 sccm (brown) silane in the mp- $\text{SiO}_x(\text{n})$  layer, all covered by the same nc-Si(n) layer.

The fill factor for this series is overall underperforming, while no clear trend with oxygen content is observed. The resulting conversion efficiency on the other side is clearly dominated by the  $V_{\text{OC}}$  and  $J_{\text{SC}}$  behavior resulting in an increased performance with higher oxygen content.

### 6.10 Co-annealed cells with textured surface, replacing nc-Si(n) by amorphous $\text{SiC}_x$

Since this layer stack targets front side application, it has to be applied on textured surfaces as a short estimation with Wafer ray tracer [PVLighthouse 2018c] shows. We simulate on a 250- $\mu\text{m}$ -thick wafer the same ideal device with nitride/wafer/nitride/Ag as used for comparison of planar devices in section 6.8 with 3% shadowing, but now we use a textured front side with randomly oriented pyramids (rear side still planar). Even though no new

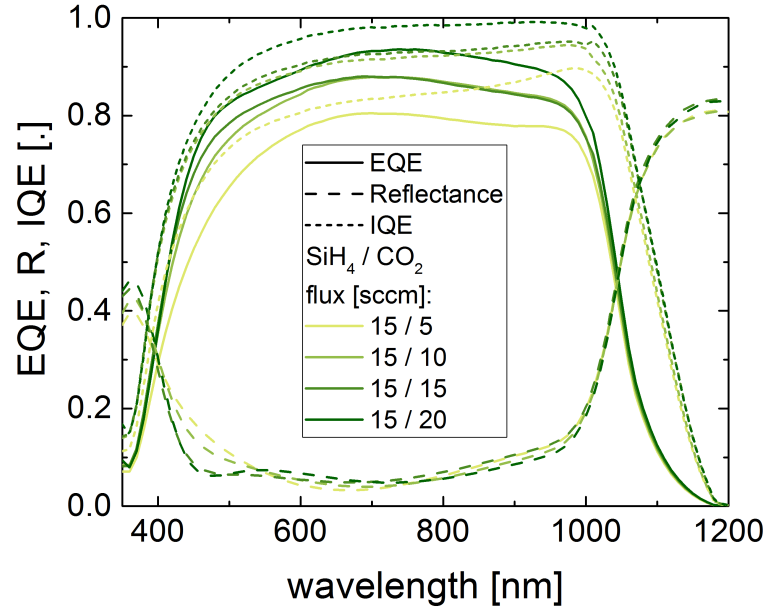


Figure 6.21 – EQE, reflectance and IQE for different CO<sub>2</sub> fluxes during PECVD deposition keeping the silane SiH<sub>4</sub> flux constant at 15 sccm.

optimization for this layer stack is done, an increase in  $J_{SC}$  by 11% from 36.7 mA/cm<sup>2</sup> (planar) to 40.9 mA/cm<sup>2</sup> and for double side textured cells an increase of even 13% up to 41.7 mA/cm<sup>2</sup> is observed. This boost in  $J_{SC}$  goes directly into a gain in efficiency which would result for our best planar cell presented in 6.8 to an efficiency of 21.1% ( $J_{SC} = 38.9$  mA/cm<sup>2</sup>) for one side textured and 21.5% ( $J_{SC} = 39.6$  mA/cm<sup>2</sup>) for double side textured cells, respectively. By optimizing the solar cell accordingly, a record current for single-junction *c*-Si solar cells of even 43.3 mA/cm<sup>2</sup> [Richter 2017] is reached using a 400-μm-thick absorber.

Passivating selective emitters on textured surfaces are demanding. Nevertheless, promising  $iV_{OC}$  values above 700 mV have been reached [Peibst 2017, Ingenito 2018b]. In section 6.6.2 we have seen that this layer stack is sensitive to fabrication processes (mainly HF) and we observed that textured surfaces are even more critical. Since we have observed a better HF stability with carbon-doped silicon (not shown here), the nc-Si(n) top layer (~17 nm) was replaced with an amorphous SiC layer with varying thicknesses of ~8 nm, ~12 nm, ~16 nm, and ~20 nm, respectively. The mp-SiO<sub>x</sub>(n) layer below was kept constant using 204 s of deposition time (1.7 · 120 s) to achieve an expected thickness of ~12 nm.

The experiment was carried out with 200-μm-thick n-type single-side-textured wafers with a base resistivity of 2 Ω cm. For comparison, cells with an mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack were processed on this wafer type as well as on a 250-μm-thick p-type wafer with the same base resistivity of 2 Ω cm.

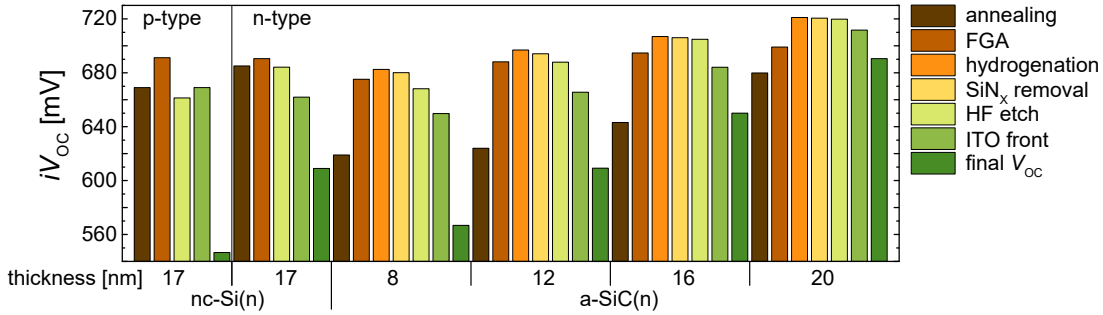


Figure 6.22 – Evolution of the  $iV_{OC}$  during the fabrication process comparing the mp-SiO<sub>x</sub>(n)/nc-Si(n) on textured p-type and n-type wafer replacing the nc-Si(n) layer by an amorphous SiC(n) layer on top of the mp-SiO<sub>x</sub>(n) with four different thicknesses, indicated on the x-axis.

To monitor the losses during the fabrication process, the passivation was measured and plotted in terms of  $iV_{OC}$  in Figure 6.22. After 15 min of annealing at 900 °C (brown), the nc-Si(n) capping layer on an n-type wafer showed best passivation with an  $iV_{OC}$  of 685 mV. The  $a$ -SiC(n) capping layers show increasing passivation with increasing thickness, leading to a similar value of 680 mV for the thickest one. After FGA (light brown), a similar level of passivation is achieved for all samples. The nc-Si(n) capping layer shows 691 mV for both wafer polarities, whereas the thickest  $a$ -SiC(n) already reaches 699 mV. Since the removal of SiN<sub>x</sub> on textured surfaces is challenging, this step was skipped for samples with nc-Si(n) capping layer. For  $a$ -SiC(n), the atomic hydrogenation using PECVD SiN<sub>x</sub> followed by 30 min of hotplate annealing at 450 °C (orange) increases the passivation further and interestingly stronger gains are observed for the thicker layers with a maximum gain of 22 mV, reaching 721 mV with 20 nm  $a$ -SiC(n). It was already observed for selective emitters based on  $a$ -SiC that layers with higher carbon content improving more strongly with atomic hydrogenation [Nogay 2016b, Ingenito 2018b]. Removing the SiN<sub>x</sub> by boiling (180 °C) H<sub>3</sub>PO<sub>4</sub> for 30 min (yellow) had very little impact whereas 60 s HF-etch (1 vol.-%, light green) decreased  $V_{OC}$  for the thinner  $a$ -SiC(n) layer by 12 mV whereas the thickest layer was not affected.

At this point the samples with nc-Si(n) capping layer entered the process again and whereas the sample on n-type wafer only lost 6 mV, a 30 mV loss on p-type wafer is observed. We relate this difference not necessarily to the difference in wafer polarity, but more to the sensitivity of this contact to HF and how many oxide channels (see section 3.7) were created during the annealing. Next, 80 nm ITO was sputtered on the textured front (green), leading to maximal losses of 22 mV for the nc-Si(n) capping which is similar to thin  $a$ -SiC(n) layers. On thicker  $a$ -SiC(n) capping layers ITO sputtering has a lower impact, resulting in a loss of 8 mV. At the rear, 130 nm of ITO covered by silver was sputtered. The cells were finished with screen-printed Ag fingers and a curing for 30 min at 210 °C.

The open-circuit voltage ( $V_{OC}$ ) of the finished cell (dark green) is added. A large difference

## 6.10. Co-annealed cells with textured surface, replacing nc-Si(n) by amorphous SiC<sub>x</sub>

between the  $iV_{OC}$  after the front-side ITO deposition and the measured  $V_{OC}$  is observed for the sample using the nc-Si(n) layer, whereas the loss is less and less pronounced as the  $a$ -SiC(n) thickness increases. Since the rear is the same for all cells, we do not expect a strong difference of losses coming from sputtering the rear ITO. Additionally measuring the pseudo  $V_{OC}$  ( $pV_{OC}$ ) gives very similar values within 5–10 mV to the  $V_{OC}$ . From measurements where the illumination extended either over the full wafer or only to the  $2 \times 2 \text{ cm}^2$  cell we conclude the losses are not based on a dark diode. Therefore we would relate the large difference between measured  $iV_{OC}$  after ITO sputtering and final  $V_{OC}$  to a low charge selectivity [Würfel 2015] in the contact using nc-Si(n) on textured surfaces, even though such a difference was not observed on planar cells.

The increase of charge selectivity with increasing thickness of the  $a$ -SiC(n) layer could be explained by more available P which increases dopant concentration and therefore decreases the hole-carrier density at the interface. It also leads to an increase in conductivity and therefore also to an increase in selectivity in an electron contact [Würfel 2015, Lachaume 2013]. Literature can be found explaining the effects of doping concentration and doped layer

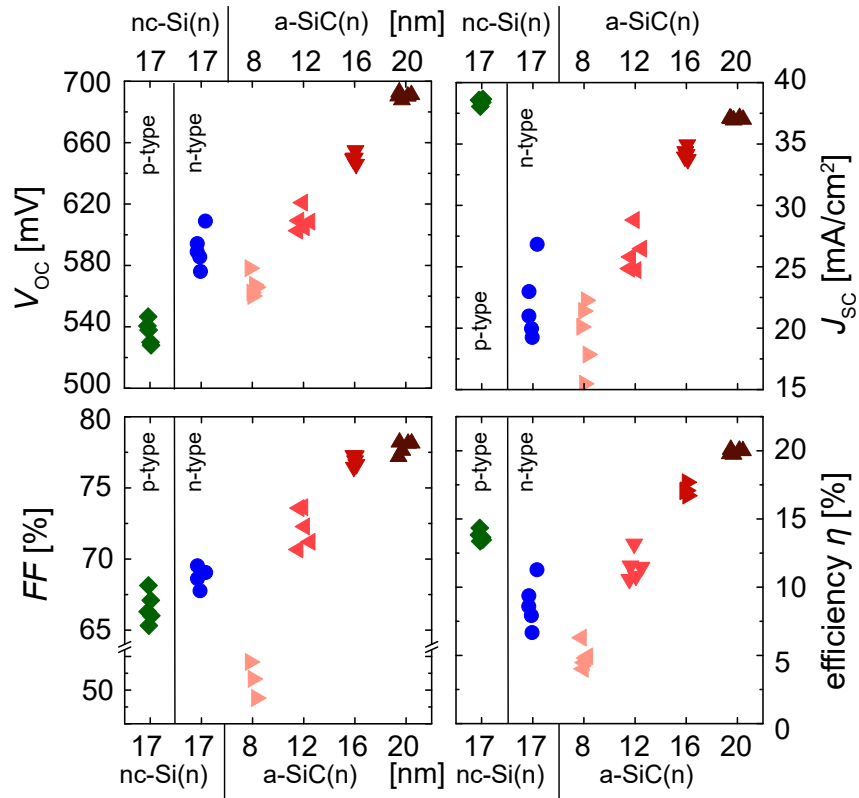


Figure 6.23 –  $J$ - $V$  characteristics of the mp-SiO<sub>x</sub>(n)/nc-Si(n) transferred to textured surfaces using a p-type (green) as well as an n-type wafer (blue) in comparison with a series replacing the nc-Si(n) capping layer by an  $a$ -SiC(n) layer (red) with 4 different thicknesses indicated at the x-axis.

thickness on the selectivity in heterojunction solar cells by modelling the workfunctions and the resulting band diagram [Bivour 2013, Bivour 2014, Lachaume 2013, Mikolášek 2017]. But to understand and explain the effects in this contact structure, the influence of inactive and active doping as well as the crystallinity of the layer need more investigations.

The  $J$ - $V$  characteristics of this series are shown in Figure 6.23. As seen before, the  $V_{OC}$  is strongly degraded for nc-Si(n) capping layer whereas for the  $a$ -SiC(n) the degradation is stronger the thinner the layer is. The  $J_{SC}$  is again strongly determined by the recombinations and therefore following the same trend as the  $V_{OC}$  with  $37.1 \text{ mA/cm}^2$  for 20 nm  $a$ -SiC(n) thickness. The nc-Si(n) in front emitter design shows  $J_{SC}$  up to  $38.7 \text{ mA/cm}^2$  with increased respond over the full wavelength range as can be seen in the EQE curve shown in Figure 6.24. The  $FF$  for the nc-Si(n) capping is between 65% and 70% for both wafer polarities with slightly higher behavior on the n-type wafer. For the  $a$ -SiC(n) capping, the  $FF$  is increasing with increasing thickness as well which could be related again to a higher amount of active P. The finished solar cells using the mp-SiO<sub>x</sub>(n)/nc-Si(n) on textured surfaces results in conversion efficiencies of 14.3% and 11.3% on p-type wafer and n-type wafer respectively, mainly limited by the low selectivity leading to a low  $V_{OC}$ . But replacing the nc-Si(n) by an  $a$ -SiC(n) layer, conversion efficiencies of up to 20.1% are reached using 20 nm layer thickness.

In Figure 6.24 the EQE, reflectance (R) and the resulting IQE are plotted for the analyzed series. The strong influence of recombination at the front is clearly visible by the reduced EQE whenever the layers are in rear emitter design, except the one with 20 nm  $a$ -SiC(n). Comparing this one with the front emitter design with nc-Si(n) capping layer, a lower response over the

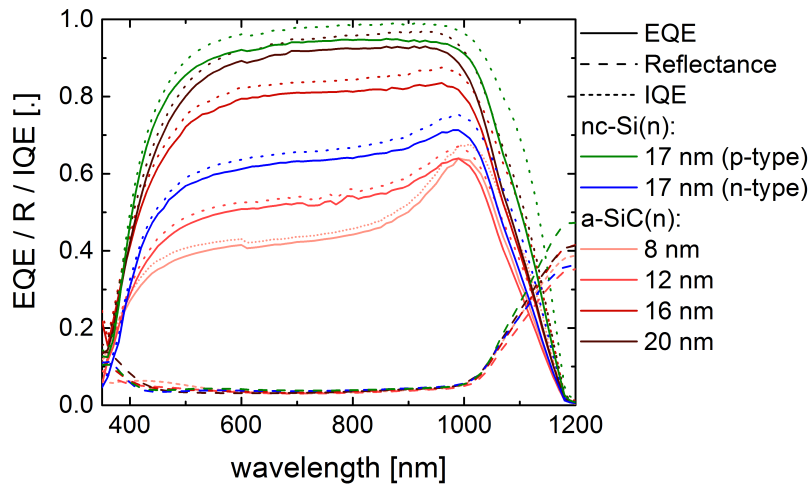


Figure 6.24 – The external quantum efficiency (EQE, solid lines), reflectance (R, dashed lines) and the corresponding internal quantum efficiency (IQE, dotted lines) for the mp-SiO<sub>x</sub>(n) layer capped with the nc-Si(n) layer on both wafer polarities in comparison with 4 cells for which the nc-Si(n) layer is replaced by an  $a$ -SiC(n) layer using 4 different thicknesses.

full wavelength range is observed mainly due to the thicker wafer that was used but in the blue part probably also due to an increased transparency. The anti-reflective behavior is well visible for all used capping layers giving a reflectance below 5% between 450–1000 nm including 3% shading losses.

## 6.11 Hybrid cells on textured surface

Hybrid cells were used on double-side-textured wafers due to a lack of boron-doped selective emitters on textured surfaces. Details on the fabrication of hybrid cells (front:  $\text{SiO}_x(\text{n})$  rear:  $a\text{-Si(i)}/a\text{-Si(p)}$  SHJ ) and a sketch of the final structure can be found in section 2.2.1. The optical losses on textured surfaces are investigated by a series of one, two, and three times the mp- $\text{SiO}_x(\text{n})$  deposition time of 204 s ( $1.7 \cdot 120$  s), leading to expected thicknesses of 12 nm, 24 nm, and 36 nm, respectively, covered by a constant 17 nm nc-Si(n) layer on top. The rear of the 200- $\mu\text{m}$ -thick p-type wafer ( $2 \Omega \text{ cm}$ ) was protected by the layer presented in section 6.6.1 during the annealing at 900 °C. The dwell times were varied between 15 min and 30 min. After an FGA, the protection oxide is removed by a one-sided HF-etch, followed by the  $a\text{-Si(i)}/a\text{-Si(p)}$  SHJ rear deposition. After another HF-etch (1-vol.%), 80 nm ITO was sputtered on the samples with 30 min of annealing dwell time whereas the samples with 15 min annealing dwell time got 990 nm boron-doped zinc oxide (ZnO:B) deposited by low-pressure chemical vapor deposition (LPCVD). LPCVD is known to be a smoother process leading to less damage, and is therefore investigated as alternative transparent conductive oxide (TCO). In chapter 5 we observed a lower impact of ITO sputtering on planar samples with a doping profile resulting from an annealing dwell time of 30 min compared to 15 min at 900 °C. All of the samples were finished with 130 nm rear ITO and a sputtered silver reflector before screen-printing the grid on the front side and curing for 30 min at 210 °C.

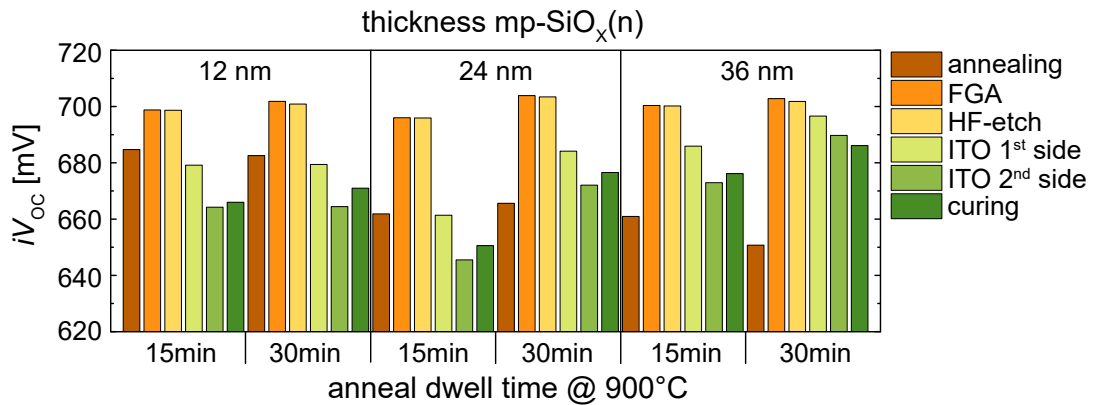


Figure 6.25 – Evolution of the  $iV_{OC}$  on textured symmetrical samples during the fabrication process using the mp- $\text{SiO}_x(\text{n})/\text{nc-Si}(\text{n})$  with three different thicknesses—12 nm, 24 nm, and 36 nm—for the mp- $\text{SiO}_x(\text{n})$  layer each annealed for either 15 min or 30 min at 900 °C.

The impact of ITO is shown in Figure 6.25. The evolution of the  $iV_{OC}$  is presented for symmetrical samples having the mp-SiO<sub>x</sub>(n)/nc-Si(n) on both sides undergoing the same fabrication steps as the cells. The three different thicknesses of the mp-SiO<sub>x</sub>(n) are indicated as well as the two different dwell times of 15 min and 30 min at 900 °C for each of them. Directly after annealing (brown), the passivation is decreasing with increasing mp-SiO<sub>x</sub>(n) layer thickness, whereas the longer annealing period of 30 min has only a slight effect. After FGA (orange) all samples level up to  $iV_{OC}$  between 700 mV and 706 mV which is not influenced by the followed HF-etch (1 vol.-%, yellow). The ITO sputter deposition (light green) leads to a loss of ~ 20 mV for a mp-SiO<sub>x</sub>(n) thickness of 12 nm independent of the dwell time. For the two thicker mp-SiO<sub>x</sub>(n) layers the beneficial effect of a longer dwell time is observed and thus confirms the findings on planar surfaces. The increase in thickness of the mp-SiO<sub>x</sub>(n) layer is beneficial since it decreases losses due to ITO sputtering. The same effects are observed after the ITO deposition on the second side (green), whereas the curing (dark green) recovers the passivation slightly by up to ~ 6 mV but can't compensate the losses appearing before. The only condition decreasing with curing is the thickest mp-SiO<sub>x</sub>(n) layer with 30 min dwell time, nevertheless it still performs best and show least degradation due to ITO.

For the LPCVD deposited ZnO:B no change in passivation is observed using symmetrical samples, neither after deposition, nor after curing afterwards, and is therefore a suitable candidate to replace ITO in terms of passivation.

The  $J$ - $V$  characteristics of the finished cells are plotted in Figure 6.26. The thickness of the mp-SiO<sub>x</sub>(n) layer is indicated on the x-axis as well as by color code and we would like to remind the reader that on top of the indicated thicknesses 17 nm nc-Si(n) layer is present leading to total thicknesses of 12 nm + 17 nm = 29 nm (light red), 24 nm + 17 nm = 41 nm (red), and 36 nm + 17 nm = 53 nm, respectively. We focus first on the samples with 30 min dwell time and ITO metallization (filled symbols, left side of the panels). The  $V_{OC}$  reproduces the findings observed before on symmetrical samples namely that 12 nm and 24 nm are not sufficient to avoid the losses in  $V_{OC}$ , whereas a clear increase is observed for 36 nm. The  $iV_{OC}$  values after ITO of the hybrid cell are slightly higher than for the symmetrical samples due to the highly passivated rear. Comparing the  $iV_{OC}$  values with the final  $V_{OC}$  values, the loss is clearly less pronounced. The increased annealing dwell time could be an explanation for the improved selectivity, but unfortunately the beneficial effect on  $V_{OC}$  with increasing thickness is compensated by a decreasing  $J_{SC}$ . The thinnest mp-SiO<sub>x</sub>(n) layer shows promisingly high  $J_{SC}$  of almost 40 mA/cm<sup>2</sup> (39.8 mA/cm<sup>2</sup>) without the use of any additional anti-reflection coating. By increasing the mp-SiO<sub>x</sub>(n) thickness, the  $J_{SC}$  decreases by ~0.75 mA/cm<sup>2</sup> per 10 nm additional mp-SiO<sub>x</sub>(n) layer thickness. The discussion on the current losses can be found a little further down together with the EQE in Figure 6.27 and OPAL simulations [PVLighthouse 2018b]. The  $FF$  is slightly increased for the thickest mp-SiO<sub>x</sub>(n) layer but remains clearly below the results on planar cells. The low  $FF$  can also be related to not optimized surface conditioning for the SHJ rear. This results in conversion efficiencies of 18% for the thickest mp-SiO<sub>x</sub>(n) layer and close by the thinnest with 17.8%. The thickness of 24 nm is slightly under performing, mainly due to  $V_{OC}$  and  $FF$ .

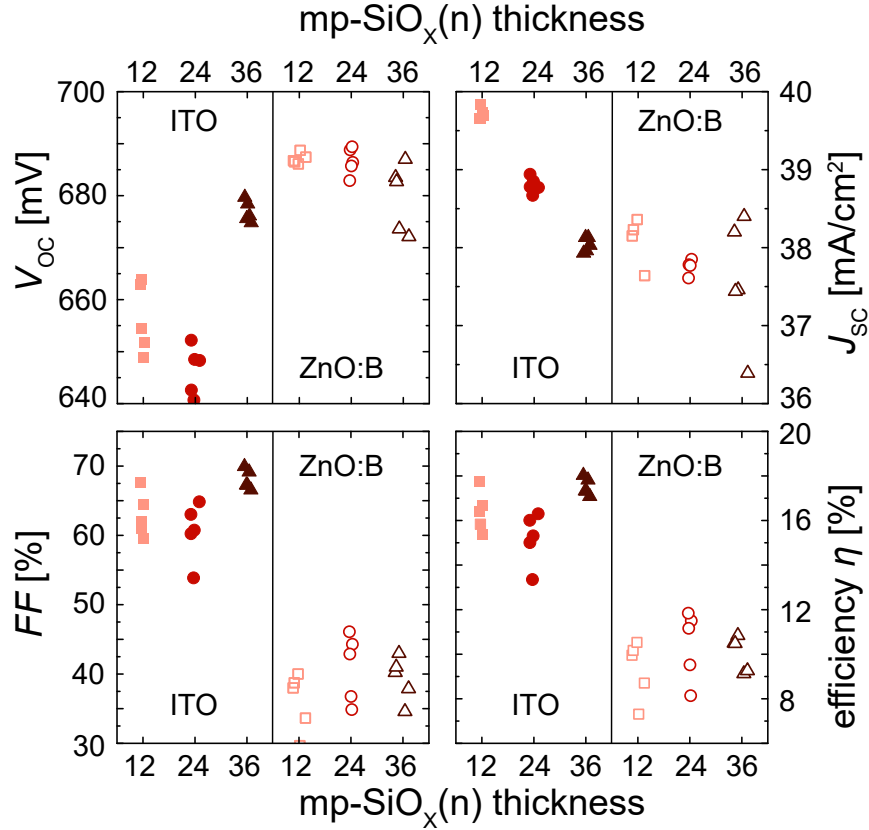


Figure 6.26 –  $J$ - $V$  characteristics of 12 nm (squares, light red), 24 nm (circles, red), and 36 nm (triangles, dark red)  $\text{mp-SiO}_x(\text{n})$  layer thickness covered by 17 nm  $\text{nc-Si}(\text{n})$ . ITO metallization (filled symbols) is compared with boron-doped ZnO:B (open symbols), please notice that an annealing treatment of 30 min at 900 °C was used for samples that afterwards got ITO whereas a treatment of only 15 min was used for the samples that got ZnO:B afterwards.

Using ZnO:B as the contact layer (open symbols, right side of panels), the  $V_{\text{OC}}$  is between 687 mV and 689 mV, independent of the thickness of the  $\text{mp-SiO}_x(\text{n})$  layer due to the smoother deposition technique. The  $J_{\text{SC}}$  values are lower than corresponding samples with ITO, they are rather similar for the thinnest and the thickest  $\text{mp-SiO}_x(\text{n})$  layer. In EQE (not shown here), it is observed that the response at short wavelengths is decreased with  $\text{mp-SiO}_x(\text{n})$  thickness, but the loss is compensated by a gain at longer wavelengths due to a lower reflection for the thicker layers above 800 nm. The main problem using ZnO:B is the lower conductivity and therefore the cells are limited by the  $FF$  below 50%, leading to efficiencies up to 12%.

The external quantum efficiency (EQE, solid lines) for the cells with ITO on the front are shown in Figure 6.27, together with the reflectance ( $R$ , dashed lines) and the corresponding internal quantum efficiency (IQE, dotted line). The reflectance for the thinnest  $\text{mp-SiO}_x(\text{n})$  layer (light red) includes the 3% metal coverage by the front grid. Increasing the thickness to 24 nm (red) and 36 nm

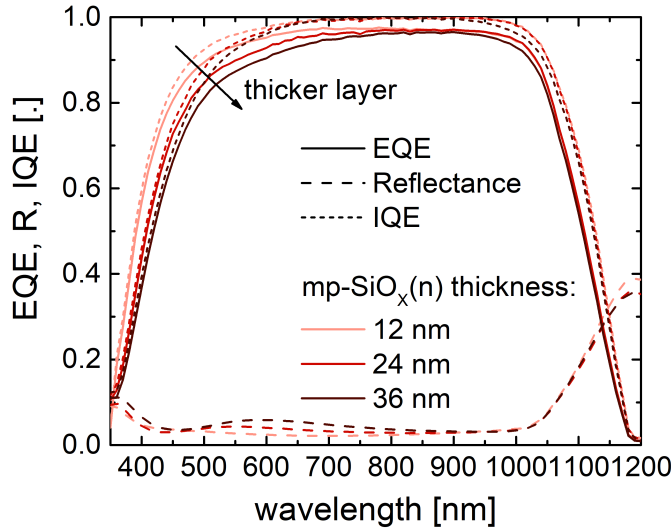


Figure 6.27 – The external quantum efficiency (EQE, solid lines), reflectance (R, dashed lines) and the corresponding internal quantum efficiency (IQE, dotted lines) for 12 nm (light red), 24 nm (red), and 36 nm (dark red) mp-SiO<sub>x</sub>(n) layer thickness capped with the same nc-Si(n) layer on textured surfaces.

(dark red), respectively, results in a slight increase of the reflectance between 500–800 nm due to a shift of the interference condition, leading also to increased parasitic absorption within the layer due to multiple passes. But this is not the main reason for the decrease in  $J_{SC}$  observed with increasing thickness. Especially below 500 nm a clear decrease in EQE as well as in the IQE is observed.

The IQE and reflectance of this series are reproduced by simulation with OPAL [PVLighthouse 2018b]. As before, 3% shading losses were subtracted from the measured reflectance and the EQE was corrected accordingly by a factor of 1.03 before calculating the IQE. The layer stack was chosen similar as depicted in Figure 6.14 starting with the *c*-Si substrate [Green 2008], covered by 1.2 nm SiO<sub>2</sub> [Palik 1998] and the mp-SiO<sub>x</sub>(n) layer using the *n* and *k* data from ellipsometry. The nc-Si(n) layer was replaced by an *a*-Si(n) layer ([Holman 2012]) and a *c*-Si layer [Green 2008] since using the *n* and *k* data of the nc-Si(n) found by ellipsometer lead to a too low transmission above 500 nm as observed already on planar (Figure 6.16) whereas the reflectance can be reproduced well also on textured. For the 80 nm layer ITO material properties published for a carrier density of  $1 \cdot 10^{20} \text{ cm}^{-3}$  were used [Holman 2013]. The surface is set to randomly oriented upright pyramids. The thicknesses for the individual layers are listed in table 6.3.

The IQE as well as the reflectance of the thinnest mp-SiO<sub>x</sub>(n) layer with an expected mp-SiO<sub>x</sub>(n) layer thickness of 12 nm are reproduced well using actually 12 nm mp-SiO<sub>x</sub>(n).

## 6.12. Temperature-dependent $J$ - $V$ characteristics

The 17 nm nc-Si(n) layer is reproduced by 2.5 nm  $a$ -Si(n) and 6 nm  $c$ -Si. For double the expected mp-SiO<sub>x</sub>(n) layer thickness (24 nm), the model gives a mp-SiO<sub>x</sub>(n) thickness of only 19 nm whereas 1.5 nm are added in the  $a$ -Si(n) layer and the  $c$ -Si layer is reduced to 5 nm. This is mainly related to the reflectance which increases too strongly between 500–800 nm when a thicker mp-SiO<sub>x</sub>(n) is chosen. We relate this to the hard index change at the interfaces in the model. In the transmission this is corrected by increasing the thickness of the  $a$ -Si(n) layer. The same trend is observed for the thickest mp-SiO<sub>x</sub>(n) layer, which increases in the model only by additional 4 nm whereas the  $c$ -Si layer is increased by another 0.5 nm. We relate the increase of the modeled  $a$ -Si(n) layer thickness with increasing mp-SiO<sub>x</sub>(n) deposition time also to the gradient of the silicon content in the mp-SiO<sub>x</sub>(n) layer during growth as was seen in chapter 3. This higher silicon content in the second 12 nm of growth compared to the first 12 nm are mainly responsible for the observed losses in  $J_{SC}$ .

Table 6.3 –  
Thicknesses used for the simulation of the reflectance and the transmission in OPAL on textured surfaces.

planed mp-SiO <sub>x</sub> (n)thickness	SiO <sub>2</sub> [nm]	mp-SiO <sub>x</sub> (n) [nm]	$a$ -Si(n) [nm]	$c$ -Si [nm]	ITO [nm]
12 nm	1.2	12	2.5	6	80
24 nm	1.2	19	4	5	80
36 nm	1.2	23	4.5	5	80

Nevertheless shows this series the transparency of this contact structure and the potential for the application on the front side with a  $J_{SC}$  of almost 40 mA/cm<sup>2</sup> with a 30-nm-thick electron-selective emitter.

## 6.12 Temperature-dependent $J$ - $V$ characteristics

The results of this section for planar cells were published in 2018 in *Solar Energy Materials and Solar Cells* [Mack 2018].

In order to examine potential transport barriers that photogenerated carriers may face when crossing the different interfaces in the different devices, we investigated the temperature-dependence of the  $J$ - $V$  curves. Such barriers might be caused by the addition of oxygen to the electron contact, and they manifest themselves in the  $J$ - $V$ ( $T$ ) curves as a positive temperature coefficient of the  $FF$  [Seif 2014]. The  $J$ - $V$ ( $T$ ) curves for the hybrid cell presented in section 5.6 with the mp-SiO<sub>x</sub>(n)/nc-Si(n) on the front (Figure 6.28a), red, rear emitter), as well as for a planar heterojunction cell (Figure 6.28b), blue, front emitter) were measured in intervals of 5 °C for temperatures from –100 °C to 75 °C. Both cells exploit the

same SHJ hole contact and identical ITO layers on the front and rear as well as the same 5% shading losses. With decreasing temperature, a strong S-shape is appearing for both solar cells at a temperature of +5 °C for the hybrid and at +35 °C for the SHJ cell.

The temperature dependence of the cell parameters of the two devices is shown in Figure 6.29: in red (empty circles) the planar hybrid device and in blue (empty triangles) the planar SHJ. The temperature-dependent  $J$ - $V$  characteristics for textured surfaces (filled symbols) are added as well using the cells presented in section 6.11 with a 24-nm-thick mp-SiO<sub>x</sub>(n) and a 17-nm-thick nc-Si(n) layer metallized by ITO (red, filled circles) and ZnO:B (green, filled circles), respectively. For comparison a textured standard SHJ cell from [Nogay 2016a] is added as well. Keep in mind that the temperature-dependent  $J$ - $V$  measurements are not calibrated absolutely (see section 6.2). Therefore, different cells can be compared only qualitatively; absolute values cannot be retrieved. At 25 °C the  $J$ - $V$  curve of the  $J$ - $V$ ( $T$ ) measurement is shifted by  $J_{SC} = 1.3 \text{ mA/cm}^2$  in comparison to the calibrated  $J$ - $V$  measurement with the Wacom system.

Figure 6.29 reveals that the general evolution for the two SHJ cells (planar and textured) is very similar, whereas the hybrid cells with the SiO<sub>x</sub>(n) front contact show different behaviors. The  $V_{OC}$  is increasing for all cells as they are cooled down from +75 °C. The  $V_{OC}$  of the flat SHJ cell shows a decreasing slope for temperatures below 0 °C and reaches around –90 °C a  $V_{OC}$  of 782 mV. For the textured SHJ cell the slope starts to decrease at around –30 °C. For both SHJ cells the  $V_{OC}$  reaches a maximum at around –75 °C for textured and at –95 °C for the flat SHJ cell, respectively. The  $V_{OC}$  of the planar hybrid cell shows a reduced slope when the temperature falls below –40 °C, but the  $V_{OC}$  does not reach a maximum in the investigated temperature range. The textured hybrid cell with a thicker mp-SiO<sub>x</sub>(n) layer, metallized with ITO, reduces the slope as well below –40 °C, but less pronounced ending up at –100 °C with a similar  $V_{OC}$

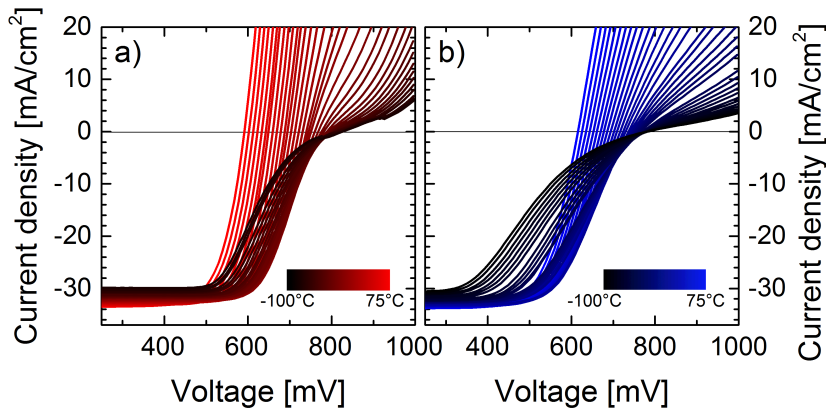


Figure 6.28 – Temperature-dependent  $J$ - $V$  measurements in the range from –100 °C to +75 °C (a) for the hybrid cell presented in section 5.6 with the mp-SiO<sub>x</sub>(n)/nc-Si(n) contact and (b) for a standard heterojunction cell (b) with a  $a$ -Si(i)/ $a$ -Si(p) front, both on flat substrates [Mack 2018].

as the planar cell. The textured hybrid cell with ZnO:B metallization shows a stronger decrease in slope, starting already at  $-10^\circ\text{C}$ .

The observed  $V_{\text{OC}}$  maximum of the SHJ cell and the reduced slope of the hybrid cells cannot be explained by the temperature dependency of the intrinsic-carrier density ( $n_i$ ) [Arora 1982]. Other effects like the temperature dependence of the surface passivation [Seif 2015b] or charge-carrier freeze-out have to be taken into account [Löper 2012]. A similar behavior was found for standard and advanced SHJ cells by Nogay et al. [Nogay 2016a] and Mikolášek et al. [Mikolášek 2017]. In their simulations Mikolášek et al. explained the roll-over behavior with a parasitic Schottky barrier at the interface of the transparent conductive oxide (TCO) and their carrier-selective contact. Furthermore, they showed that the  $V_{\text{OC}}$  roll-over shifts to higher temperatures with a decrease of the net doping of the  $a$ -Si:H contact layer. Similar effects might also explain the data of Figure 6.29, as the effective doping of the mp-SiO<sub>x</sub>(n)/nc-Si(n) contact

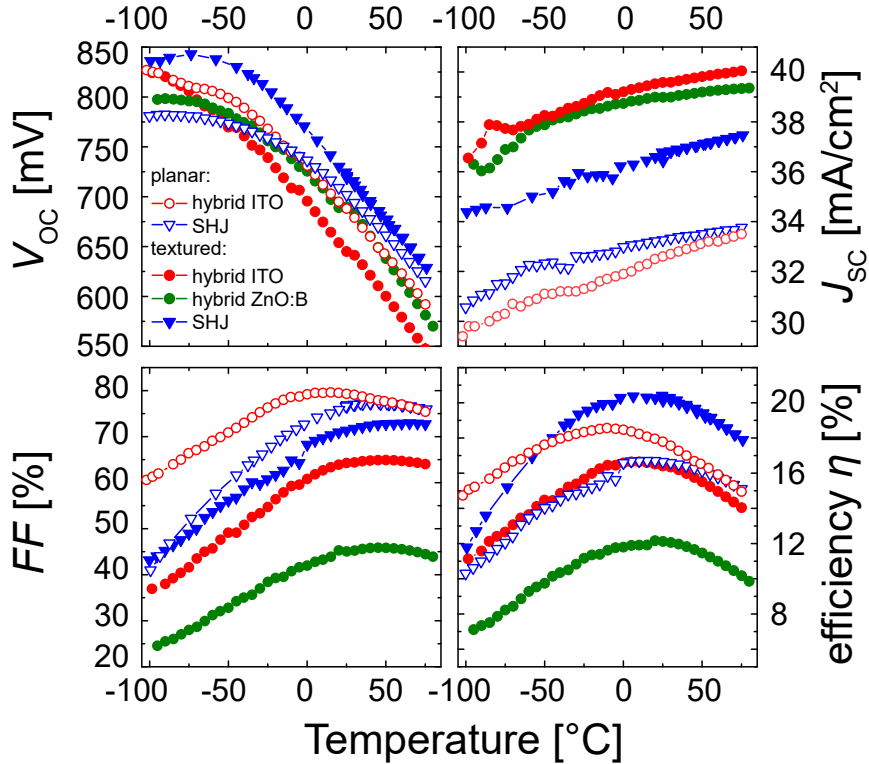


Figure 6.29 – Temperature dependence of the cell parameters for different hybrid cells presented so far in comparison with SHJ devices. Planar hybrid cell from section 5.6 with 12 nm mp-SiO<sub>x</sub>(n) and 17 nm nc-Si(n) with ITO metallization (red empty circles); textured hybrid cell from section 6.11 with 24 nm mp-SiO<sub>x</sub>(n) and 17 nm nc-Si(n) metallized by ITO (red filled circles) and metallized by ZnO:B (green filled circles). The cells are set in comparison with SHJ cells (blue triangles) on textured (filled symbols) as well as on planar (empty symbols) surfaces.

is  $> 1 \cdot 10^{20} \text{ cm}^{-3}$  and that of a standard *a*-Si(n) layer  $< 1 \cdot 10^{20} \text{ cm}^{-3}$  [Stuckelberger 2016a]. The finding that a barrier at the interface of the carrier-selective contact to the TCO is the main driver for the decreased slope in  $V_{OC}$  for lower temperature is supported comparing the two different TCOs on textured surfaces. For the hybrid cell with ITO almost no change in the slope is observed, whereas the same contact structure exhibits a strong decrease in slope when ITO is replaced by ZnO:B.

The increase in  $J_{SC}$  with temperature for all cells over the whole temperature range can be explained by a temperature dependence of the bandgap of the *c*-Si absorber and thus an increase in absorption in the infrared region [Riesen 2016, Bludau 1974, Green 2003]. Using the formula provided by Green et al. [Green 2008] for the absorption coefficient of *c*-Si as a function of temperature and for a single pass through the wafer, results in a linear increase in total generation of  $\approx 0.3 \text{ mA/cm}^2$  every  $10^\circ\text{C}$ , which fits well the experimental data.

The fill factor of the planar hybrid cell (red empty circles) is higher than the one of the planar SHJ cell (blue empty triangles). The *FF* of the planar hybrid cell rises slightly with decreasing temperature in the range from  $+75^\circ\text{C}$  to  $-10^\circ\text{C}$  before it decreases to 60% towards lower temperatures. The *FF* of both textured hybrid cells (red and green filled circles) are slightly increasing at higher temperatures, but already below  $+45^\circ\text{C}$  it starts to decrease for both metallizations. The SHJ cells (filled and empty blue triangles) show a temperature-dependent decrease for the *FF* in the whole investigated temperature range. For  $+75^\circ\text{C} > T > +35^\circ\text{C}$ , the decrease is slow for both SHJ cells, but it is getting more pronounced for  $T < +35^\circ\text{C}$  and is being stronger for the textured SHJ cell. The corresponding *J-V* curves in Figure 6.28 for the flat cells reveal that this behavior is related to the onset of the S-shape formation towards lower temperatures. Interestingly, the *FF* of the planar hybrid cell does not decrease as much as the *FF* of the planar SHJ cell. As both cells feature the same hole contact, we conclude that the transport mechanism for the planar SHJ contact is more affected by low temperatures than the  $\text{SiO}_x(\text{n})$  contact in the hybrid cell. But this behavior is only partly reproduced on textured surfaces.

The efficiency reveals a maximum at between  $5^\circ\text{C} < T < 20^\circ\text{C}$  for all cells except the planar hybrid cell with a maximum at  $-10^\circ\text{C}$  dominated by the *FF* behavior for this cell.

For the planar cells, we also extracted the series resistance ( $R_s$ ) at each temperature with the two curve method [Thongpron 2006, Pysch 2007b, Wolf 1963]. Figure 6.30 supports the trend of the *FF* with a higher series resistance of the SHJ cell than for the hybrid cell over the whole temperature range. Furthermore,  $R_s$  of the SHJ cell clearly increases as the cell is cooled down from  $+75^\circ\text{C}$  to  $-80^\circ\text{C}$ , with a steep increase between  $+10^\circ\text{C}$  and  $-10^\circ\text{C}$ . Conversely, it is nearly constant for the hybrid cell between  $+75^\circ\text{C}$  and  $+20^\circ\text{C}$  and its increase towards lower temperatures is much less pronounced than that for the SHJ cell. For low temperatures ( $T < -40^\circ\text{C}$ ) the temperature-dependent increase of  $R_s$  is becoming equal for both cells. In general the total series resistance can be approximated as the sum of the bulk resistance of the material, sheet resistance of the used TCO film and the contact resistance [Sachenko 2016].

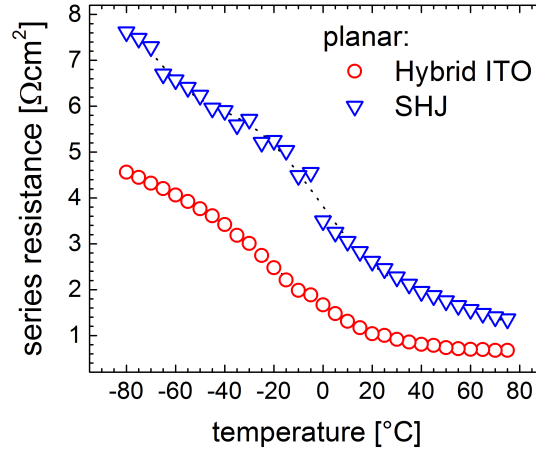


Figure 6.30 – Temperature dependency of the series resistance  $R_s$  determined by the comparison of  $J$ - $V$  curves at different illuminations for the planar SHJ (blue open triangles) and the planar  $\text{SiO}_x(\text{n})$  hybrid device (red open circles). The black dotted lines are polynomial fits as guidance for the eye [Mack 2018].

We assume that the series resistance is dominated here by the contribution of the passivating contact layer stack, i.e. by the total effect of the interfaces and layers between the  $c$ -Si wafer and the ITO film.

To explain the different behavior of the hybrid and the SHJ cell, we have to consider the different conduction mechanisms at a Schottky barrier [Schroder 1984, Yu 1970]. For low doping ( $N_{\text{dop}} < 1 \cdot 10^{17} \text{ cm}^{-3}$ ) the resulting current is due to thermionic emission (TE) over the barrier, whereas for high doping ( $N_{\text{dop}} > 1 \cdot 10^{19} \text{ cm}^{-3}$ ) the barrier becomes narrow and current flows by tunneling (FE, field emission). In the intermediate doping range ( $1 \cdot 10^{17} \text{ cm}^{-3} \ll N_{\text{dop}} \ll 1 \cdot 10^{19} \text{ cm}^{-3}$ ), thermionic field emission (TFE) is dominant. This is a combination of the two mechanisms mentioned before. The emission over the barrier in TE is thermally activated, whereas the FE is only weakly temperature-dependent. Since both cells feature the same hole-contact we relate the differences in  $FF$  behavior to the electron contact. As doping efficiency is lower in the doped layers of SHJ cells and both cells exhibit a Schottky barrier at the TCO/carrier-selective contact interface, we would expect to find a more pronounced temperature dependence of the series resistance for the hybrid cell. Comparing the  $FF$  of the two cells, as well as the series resistances given in Figure 6.29 and Figure 6.30, differences in the transport mechanism of the two contacts are visible. The SHJ is probably affected by thermionic field emission at low temperatures, as decreasing temperatures result in a strong decrease of  $FF$  and a fast increase of the series resistance. In case of the planar hybrid cell the dependence on temperature is less pronounced, leading to the conclusion that its transport mechanism is more related to field emission. For high temperatures, the  $FF$  and the series resistance of the cells approach each other, indicating that in this temperature range

the conduction mechanism is mainly dominated by thermionic emission of the carriers over the Schottky barrier with the ITO layer.

Recently a detailed study on the transport mechanism through chem-SiO<sub>x</sub> using an electron-selective SiC(n) contact was reported by Feldmann et al. [Feldmann 2018] in which the change from thermionic emission to field emission was related to the annealing temperature of the contact and explained by a partially rupture of the chem-SiO<sub>x</sub>.

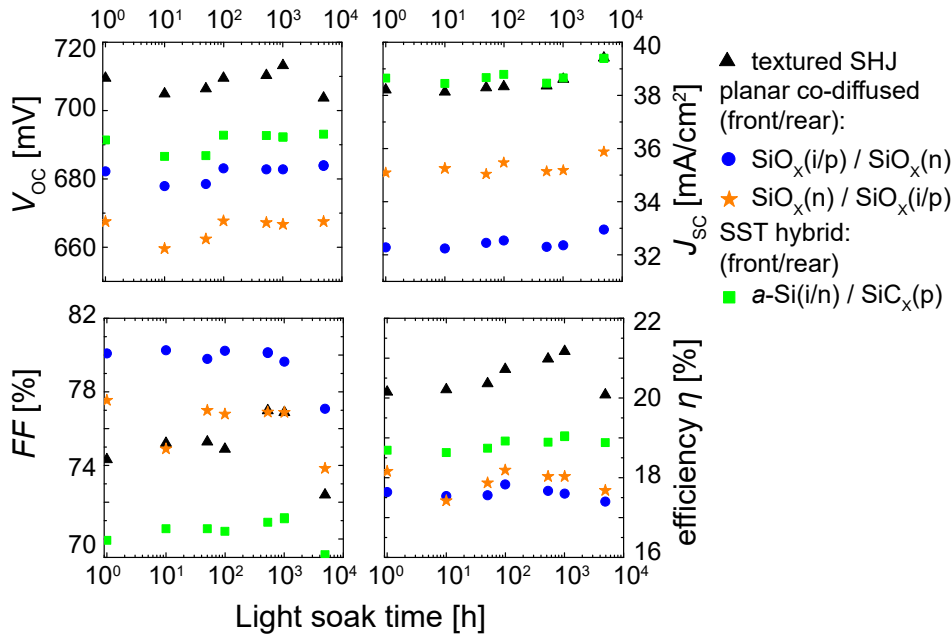


Figure 6.31 – Variation of the solar cell parameters upon light soaking for 5000 hours. Black triangles refer to a textured heterojunction reference, orange (stars) to a planar co-annealed cell with the SiO<sub>x</sub>(n) contact at the front and in blue (circles) with the SiO<sub>x</sub>(i/p) contact at the front both in the front emitter design (presented in section 6.8), and in green squares a single-side-textured hybrid cell presented in [Nogay 2017] with a SHJ *a*-Si(n) front side on a p-type wafer and a hole-selective SiC<sub>x</sub>(p) contact at the planar rear.

### 6.13 Reliability under light soaking

Reliability testing was carried out of the planar co-annealed front emitter cells presented in section 6.8 by exposing them to light soaking under continuous illumination equivalent to one sun, keeping the cell temperature at 30 °C. In Figure 6.31 the evolution of the *J*-*V* characteristics are plotted in orange (stars) with the SiO<sub>x</sub>(n) contact at the front and in blue (circles) with the SiO<sub>x</sub>(i/p) contact at the front both in front emitter design. Up to 1000 hours, no clear variation is observed with light soaking time for the co-annealed passivating SiO<sub>x</sub> contacts. For comparison, a textured heterojunction cell and a single-side-textured

hybrid cell were added. The hybrid cell featured a SHJ *a*-Si(n) front side on a p-type wafer and a hole-selective SiC<sub>x</sub>(p) contact at the planar rear [Nogay 2017]. Up to 1000 hours, the heterojunction cell (black triangles) shows a slight improvement which is governed by the  $V_{OC}$ . This behavior was observed on a variety of heterojunction solar cells [Kobayashi 2017]. Different to the Staebler-Wronski effect in thin-film silicon solar, it is a beneficial effect and it is not easily explained by an equilibrium of the defect pool because it is persistent, i.e. it remains after light-soaking and also after annealing [Ingenito 2018a]. A slight improvement is also observed in the solar cell with the annealed p-type passivating SiC<sub>x</sub>(p) rear contact (green squares), but it is possible that the improvement is related to the n-type amorphous front contact. In [Kobayashi 2017] it was reported that p- as well as n-type amorphous contacts show such an improvement. For light soaking times of more than 1000 hours, it is observed that the  $FF$  of all cells deteriorates. This is very likely related to the silver metallization which showed appreciable tarnishing since the cells were not encapsulated against the degradation by ambient air and by humidity.

### 6.14 Comparison of SiO<sub>x</sub>(n) versus SiC<sub>x</sub>(n) contact

Recently, [Ingenito 2018b] presented a series of co-annealed cells using a 12-nm-thick SiC<sub>x</sub>(n) contact on the front with variation in carbon content. A trade-off between high surface passivation (high C content) and more transparent layers (low C content) was found. We took the two cell with highest efficiency (high C content) and the one with the highest current (low C content), respectively, and set them in comparison with two cells with a SiO<sub>x</sub>(n) contact presented before: The hybrid cell with a mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack of a total thickness of ~ 30 nm (12 nm mp-SiO<sub>x</sub>(n) and 17 nm nc-Si(n)) presented in section 6.11; additionally, the best cell presented in this report (c.f. section 6.10) with 12 nm mp-SiO<sub>x</sub>(n) layer capped with 20 nm *a*-SiC(n) co-annealed with a SiO<sub>x</sub>(i/p) rear. All cells use a 200-μm-thick wafer with a base resistivity of 2 Ω cm, but the cell with a mp-SiO<sub>x</sub>(n)/*a*-SiC(n) stack is the only one in rear-emitter design. The hybrid cell is fabricated on a double side textured wafer whereas all others use a single-side-textured (SST) wafer.

In table 6.4 the  $J-V$  parameters are listed as well as the front layer and wafer polarities. The mp-SiO<sub>x</sub>(n)-layer-based cell with a nc-Si(n) capping performs poor in  $V_{OC}$  and  $FF$  due to the losses occurring during fabrication as reported earlier. Nevertheless, the highest current is observed for this cell despite its layer thickness of 30 nm. The *a*-SiC(n) capping layer reduces the losses in  $V_{OC}$  and  $FF$  but the parasitic absorption in 20 nm *a*-SiC(n) layer leads to severe losses in  $J_{SC}$ .

In Figure 6.32 the EQE (panel a, solid lines), reflectance (panel a, dashed lines) and the IQE (panel b) of the SiC<sub>x</sub>(n)-based cells are shown for a high C content (dark blue) and low C content (light blue), respectively. The area between the two curves are hatched to refer to the

Table 6.4 –

*J-V* characteristics of the hybrid cell using SiO<sub>x</sub>(n) on the front, in comparison with cells presented in [Ingenito 2018b] using a SiC<sub>x</sub>(n) contact at the front.

front layer wafer type	$V_{OC}$ [mV]	$J_{SC}$ [mA/cm <sup>2</sup> ]	$FF$ [%]	$\eta$ [%]
mp-SiO <sub>x</sub> (n)/nc-Si(n) p-type textured	663	39.7	62.0	17.8
mp-SiO <sub>x</sub> (n)/a-SiC(n) n-type SST	693	37.1	78.2	20.1
SiC <sub>x</sub> (n)-low C p-type SST	670	39.3	79.9	21.0
SiC <sub>x</sub> (n)-high C p-type SST	706	38.0	80.2	21.5

cells with a carbon content between the two. The mp-SiO<sub>x</sub>(n)/nc-Si(n) based layer with a nc-Si(n) cover (red) shows the highest EQE for longer wavelength due to the double-side-textured wafer, but also at shorter wavelength is the EQE increased compared to the SiC<sub>x</sub>(n)-based contacts. This is partly related to the low reflectance, which is also observed for the mp-SiO<sub>x</sub>(n)/a-SiC(n) layer (orange). In the IQE, the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack doesn't reach the low parasitic absorption of the 12-nm-thick SiC<sub>x</sub>(n) contact with low C content, which we relate mainly to the absorption within the 17-nm-thick nc-Si(n) cover layer.

## 6.15 Conclusion

In this chapter the optical properties of mp-SiO<sub>x</sub>(n) and nc-Si(n) were investigated in detail. Starting with the determination of the refractive index  $n$  and extinction coefficient  $k$  for the individual layers in the mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer stack by spectroscopic ellipsometry. For the mp-SiO<sub>x</sub>(n) layer, values for  $n$  as well as for  $k$  were found to be between the ones of SiO<sub>2</sub> and SiO<sub>1</sub> confirming the high oxygen content found in the structural analysis in chapter 3 and confirming its potential as a transparent layer. The nc-Si(n) layer showed a wavelength dependence closer to *c*-Si than *a*-Si with a higher  $n$  at 300 nm and 400 nm but still less pronounced than for *c*-Si.

A deeper analysis was performed on several parameters influencing the in-diffusion of phosphorus to the wafer during the annealing at 900 °C. We found an interesting relation between the depth and the surface concentration of the diffused profile and the wafer polarity as well as its base resistivity, pointing towards a different growth of chem-SiO<sub>x</sub> on varying base materials. A way of suppressing or intensify the diffusion to the wafer is presented by either a variation in the mp-SiO<sub>x</sub>(n) thickness or by introducing an intrinsic SiO<sub>x</sub>(i) layer of a certain thickness.

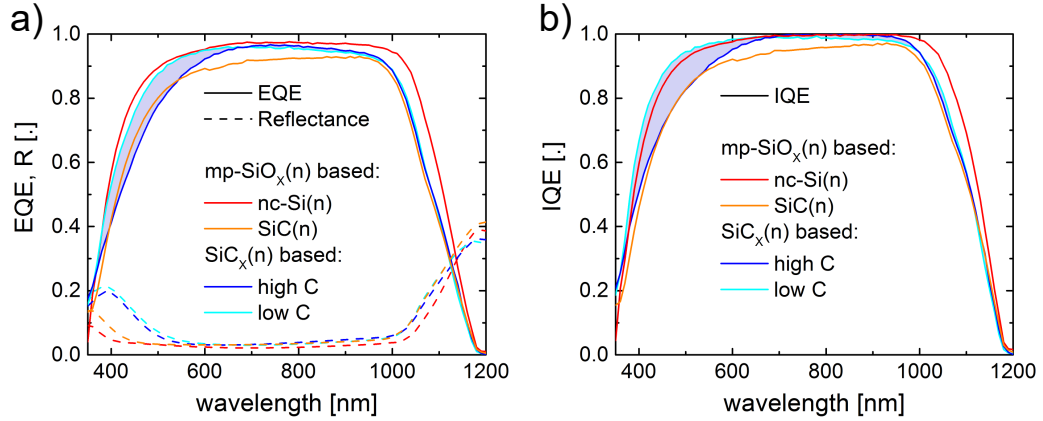


Figure 6.32 – (panel a, solid line) The EQE, (panel a, dashed line) the reflectance and (panel b) the IQE for the cells summarized in table 6.4. The hybrid cell with a 30-nm-thick mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack in red (double-side-textured, p-type wafer), a 32-nm-thick co-annealed cell with a mp-SiO<sub>x</sub>(n)/a-SiC(n) layer stack in orange (SST, n-type wafer), a 12-nm-thick co-annealed SiC<sub>x</sub>(n) cell with high C content in dark blue and low C content in light blue, respectively (SST, p-type, [Ingenito 2018b]). As guidance for the eye is the area between the low and high C content hatched in blue representing other C contents.

For the implementation into working solar cell devices, we tested the chemical stability against cleaning methods as well as hydrofluoric acid, and finally two ways of integration were presented: First in proof-of-concept hybrid cells together with a heterojunction *a*-Si(p) hole-contact, and second by co-annealed cells using a SiO<sub>x</sub>(i/p) hole-selective emitter with the same thermal budget as the SiO<sub>x</sub>(n) contact. For the hybrid cells, a protection layer based on an amorphous silicon oxide was developed against in-diffusion of impurities on the rear side.

On working planar hybrid cells the *n* and *k* values of the mp-SiO<sub>x</sub>(n) layer and the nc-Si(n) layer were tested by a variation of the thicknesses of the individual layers and modeling of the resulting reflectances by OPAL. Out of the thickness-dependent losses in the measured internal quantum efficiencies, the absorption losses were quantified to 0.4 mA/cm<sup>2</sup> per 10 nm within the nc-Si(n) layer and only 0.07 mA/cm<sup>2</sup> per 10 nm for the mp-SiO<sub>x</sub>(n) layer respectively.

In planar co-annealed cells, the high transparency in combination with a low reflectance showed the potential with a *J*<sub>SC</sub> of 35.0 mA/cm<sup>2</sup> without the usage of an additional anti-reflection coating. Additionally, the *FF* of almost 80% demonstrated efficient carrier transport through the mixed-phase layer. With a *V*<sub>OC</sub> of 686 mV, this resulted in a promising conversion efficiency of 19%.

Transferring the SiO<sub>x</sub>(n) layer to textured surfaces showed degradation during the fabrication process in co-annealed solar cells (rear side SiO<sub>x</sub>(i/p) on planar surface) which could be improved by replacing the nc-Si(n) layer by an a-SiC<sub>x</sub>(n) layer reaching conversion efficiencies

of up to 20.1%.

Finally, the  $\text{SiO}_x(\text{n})$  contact structure was applied to both-side-textured surfaces using the approach of hybrid solar cells reaching short-circuit current densities up to  $40 \text{ mA/cm}^2$  showing the potential as a transparent front side contact.

## 7 Highly crystalline silicon layers with fluorinated precursors

A second approach to obtain transparent layers for electron-selective emitters was developed by the use of phosphorus-doped microcrystalline silicon ( $\mu c$ -Si:F(n)) which is highly crystallized already in the as-deposited state. From the early work of this thesis on thin-film silicon solar cells (more details in chapter A) deposition regimes with increased crystallinity achieved by plasma-enhanced chemical vapor deposition (PECVD) are known using silicon tetrafluoride ( $\text{SiF}_4$ ) as an additional precursor. Indeed, highly crystalline layers are achieved already at annealing temperatures of 850 °C.

We report a beneficial effect of fluorine in the layers in terms of passivation reaching  $iV_{\text{OC}}$  values up to 730 mV on planar surfaces and 707 mV on textured ones without additional hydrogenation processes. A variation in hydrogen does not lead to significant changes in passivation, but it does result in a lower resistance against chemical treatments, especially when high hydrogen fluxes are used.

This approach is tested on cell level leading to short-circuit currents of 34.9 mA/cm<sup>2</sup> on planar and 39.9 mA/cm<sup>2</sup> on textured, respectively. On the other side is the transfer of the high passivation obtained on symmetrical samples to cell level more demanding.

### 7.1 Introduction

In the late 70's work was published using fluorinated precursors as an alternative method for the growth of amorphous silicon used in thin-film solar cells. At that time, the objective was to reduce instability problems associated with hydrogen [Ovshinsky 1978, Goodman 1979, Madan 1980]. In the following decades, several groups were working on this material, showing improved photo-conductivity, charge-carrier mobility, and an increased crystallinity [Bruno 1991, Shimizu 1987, Bruno 2009, Lejeune 2004, Tsu 1980, Tsu 1982, Cicala 2001, Hänni 2014, Dornstetter 2014b, Djeridane 2007]

The deposition regimes used within this work for the electron-selective emitters are based on the development by Simon Hänni within this laboratory on thin film solar cells [Hänni 2014].

We used precursor gases of Ar, H<sub>2</sub>, and SiF<sub>4</sub> as proposed by [Kasouit 2002, Vanderhaghen 2002] for the growth of fully crystallized layers in thin film transistor applications. A deposition where crystals already formed within the plasma contribute to the growth of the  $\mu c$ -Si:F layer [Kasouit 2004] as well as the preferential etching of the amorphous phase by fluorine atoms [Dornstetter 2014a]. A detailed study on the growth mechanism in  $\mu c$ -Si:F and the role of fluorine and hydrogen can be found in [Dornstetter 2014a, Dornstetter 2014b].

In the literature on micro-electronics, fluorine and other halogen atoms (Cl, Br,...) are reported to decrease the defect density at the Si/SiO<sub>2</sub> interface, similarly to hydrogen [Singh 1978, Wang 1992, Viridi 1991, Inoue 1989, Nishioka 1989, Isomae 1980]. Furthermore, fluorine effuses out of the amorphous matrix at higher temperature than hydrogen [Fang 1980] which is beneficial for the high processes temperature used in micro-electronics.

### 7.2 Experimental details

The investigation of passivating electron-selective contacts shown in this chapter are based on 250- $\mu$ m-thick 4-inch <100>-oriented 2  $\Omega$  cm p-type FZ silicon wafers. After cleaning using standard wet chemistry a  $\sim 1.2$  nm thin SiO<sub>x</sub> layer was formed on both sides by wet chemical oxidation [Asuha 2003, Grant 2009], from here on referred to as chem-SiO<sub>x</sub>. Subsequently, a thin phosphorus-doped  $a$ -Si(n) layer followed by a  $\mu c$ -Si:F(n) is deposited by PECVD using SiF<sub>4</sub>, H<sub>2</sub>, PH<sub>3</sub> and Ar as precursor gases. The SiF<sub>4</sub> and Ar fluxes were kept constant during this investigation. An annealing in argon atmosphere was performed in a tube furnace at various temperatures. The annealing was followed by a forming gas anneal (FGA, 4% H<sub>2</sub> in N<sub>2</sub>) for 30 min at 500 °C. A second hydrogenation was performed using PECVD deposited SiN<sub>x</sub> followed by an annealing on a hotplate at 450 °C for 30 min in air. The SiN<sub>x</sub> is afterwards removed in a 180 °C hot H<sub>3</sub>PO<sub>4</sub> solution for 30 min [Liu 2007] or by 12 min HF-etch (5 vol.-%). For cells, an additional HF-etch (1 vol.-%) was carried out before sputtering 80 nm ITO at the front and 130 nm at the rear. Finally, the solar cells were metallized by sputtering a silver reflector on the rear side and screen printing an Ag grid on the front, followed by curing for 30 min at 210 °C in a belt furnace.

Crystallization of the Si phases was characterized by Raman spectroscopy<sup>1</sup>. In order to avoid the signal from the underlying  $c$ -Si wafer, the measurement was carried out with a 325 nm laser, which has a Raman collection depth of only around 13 nm in  $c$ -Si [Carpenter 2017].

### 7.3 Passivation quality on planar surfaces

First, the influence of a variation in hydrogen and phosphine flux on the passivation quality was investigated. Planar 250- $\mu$ m-thick p-type wafers with a resistivity of 2  $\Omega$  cm were used. Since HF can be formed in a plasma of SiF<sub>4</sub> and H<sub>2</sub> [Dornstetter 2014a], an  $a$ -Si(n) layer

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<sup>1</sup>The Raman measurements were performed by Luca Antognini and are acknowledged by the authors.

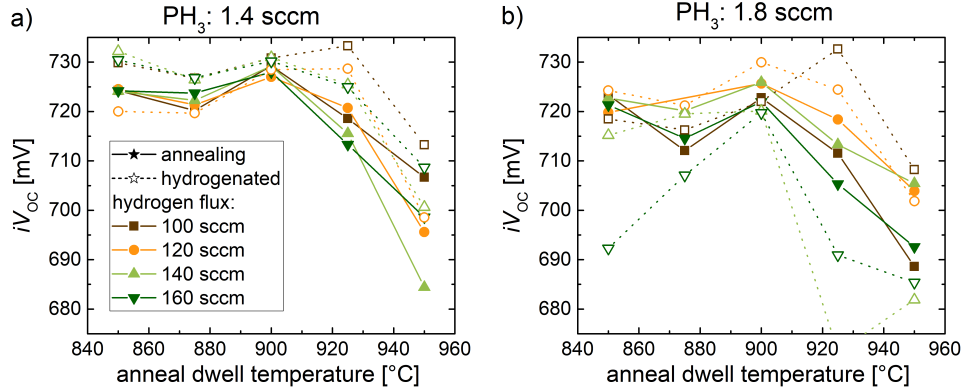


Figure 7.1 –  $iV_{OC}$  for planar symmetrical samples varying the hydrogen fluxes as a function of the anneal dwell time for a  $PH_3$  flux of (a) 1.4 sccm and (b) 1.8 sccm, respectively. Filled symbols represent the values directly after annealing, whereas open symbols represent values after hydrogenation.

of  $\sim 4$  nm was introduced to protect the chem-SiO<sub>x</sub>. Then, a  $\sim 16$  nm  $\mu c$ -Si:F(n) layer was deposited. The deposition rate for intrinsic  $\mu c$ -Si:F is influenced by the additional hydrogen as reported in detail in [Hänni 2014].

In Figure 7.1 the implied open-circuit voltages ( $iV_{OC}$ ) of symmetrical samples are plotted as a function of anneal temperature, using four different total hydrogen fluxes. Panels a) and b) show  $PH_3$  fluxes of 1.4 and 1.8 sccm, respectively. Since the phosphine precursor gas used for this experiment is diluted in hydrogen (2%), the hydrogen fluxes are adjusted so that the total hydrogen flux for corresponding samples between the two used  $PH_3$  fluxes are equal. The anneal dwell temperature is varied between 850 °C and 950 °C, whereas the heating ramp was kept as 10 °C/min, directly followed by a cooling ramp of 2 °C/min, i.e. without annealing dwell time. This means that Excellent passivation is reached for a broad variety of conditions.

We first focus on the case of lower  $PH_3$  flux (1.4 sccm). Directly after annealing (filled symbols, solid lines), the passivation is independent of the used hydrogen flux for annealing temperatures between 850 and 900 °C. At higher annealing temperatures, the passivation decreases and high hydrogen fluxes appear to have a detrimental influence. In all cases, hydrogenation improves the implied  $V_{OC}$  by ca. 5 to 10 mV. For the case of higher  $PH_3$  fluxes, similar trends are observed, best performance is also observed at 900 °C. In this case, there is a larger spread after hydrogenation and it yields no clear improvement. Especially samples with higher  $H_2$  fluxes loose in passivation by hydrogenation. This is mainly related to losses appearing during the removal of the SiN<sub>x</sub> which is more critical for the samples with a higher hydrogen and phosphine flux.

The impact of the different hydrogenation processes on the  $iV_{OC}$  are shown in more detail for representative annealing temperatures of 850 and 925 °C in Figures 7.2a and b respectively.

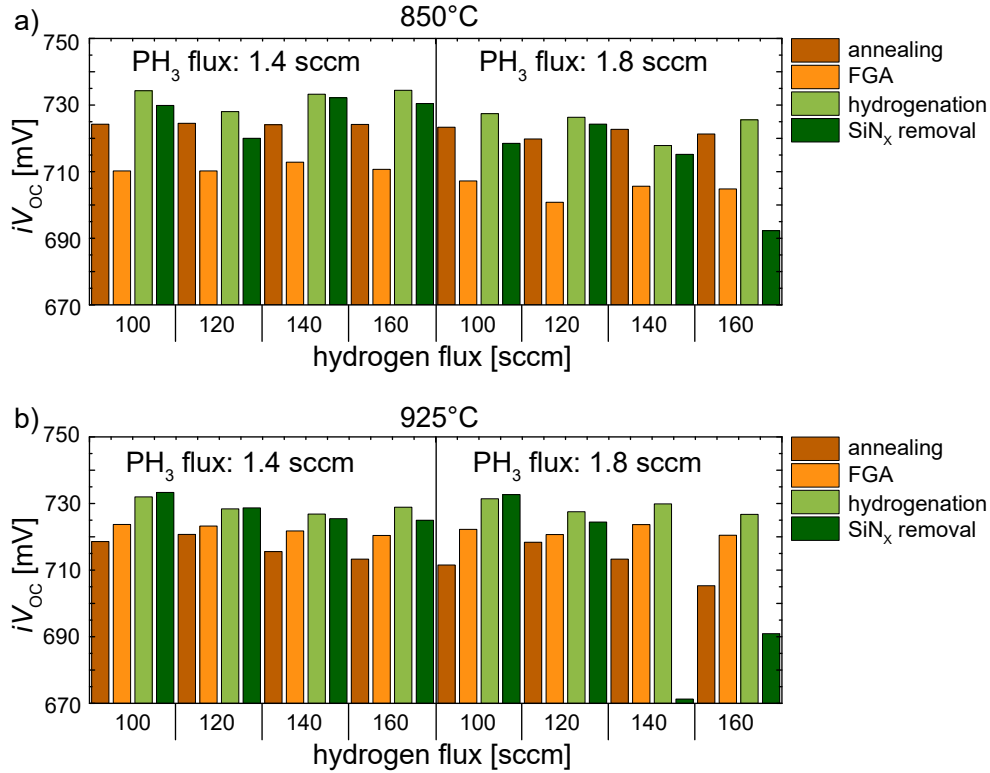


Figure 7.2 – The evolution of  $iV_{OC}$  for panar symmetrical samples annealed (a) at 850 °C and (b) at 925 °C, respectively, through hydrogenation processes varying the hydrogen fluxes for a  $PH_3$  flux of 1.4 sccm and 1.8 sccm, respectively.

For the case of the low annealing temperature, the FGA (orange) decreases the  $iV_{OC}$  after annealing (brown) by 10–20 mV for all conditions with a slightly lower loss for samples with 1.4 sccm  $PH_3$ . We interpret these losses by the assumption that molecular hydrogen cannot fully passivate recombination centers, whereas the temperature of 500 °C is already high enough to release some hydrogen (or probably fluorine). Interestingly, for the case of higher anneal dwell temperature (925 °C), FGA leads to a gain of 5–15 mV with a more pronounced gain for higher  $PH_3$  and  $H_2$  fluxes.

The atomic hydrogenation (light green) by  $SiN_x$  deposition followed by a hotplate anneal at 450 °C in air boosts the passivation for both cases to a similar level with a best value of 734 mV. The dark green column show that removing the  $SiN_x$  in boiling  $H_3PO_4$  for 30 min results in small losses for low  $PH_3$  and  $H_2$  fluxes, whereas the combination of high  $PH_3$  and high  $H_2$  fluxes leads to strong losses after the removal. We relate this to the more crystalline nature in the as-deposited state as was observed by Raman spectroscopy (c.f. section 7.4) which results in a more voidy crystallization during annealing and therefore to a penetration of the solution along the grain boundaries.

For the integration in solar cells, the stability of the passivation against hydrofluoric acid

(HF, 5 vol.-%) was tested for the example of a  $\text{PH}_3$  flux of 1.8 sccm,  $\text{H}_2$  flux of 120 sccm annealed at 875 °C. Figure 7.3 shows a slight decrease of 6 mV within the first 30 s, then the  $iV_{\text{OC}}$  remains stable at  $\sim 715$  mV before eventually after 3 min etching time the passivation decreases further to 705 mV. We conclude that the layer is stable enough for the usually used fabrication processes.

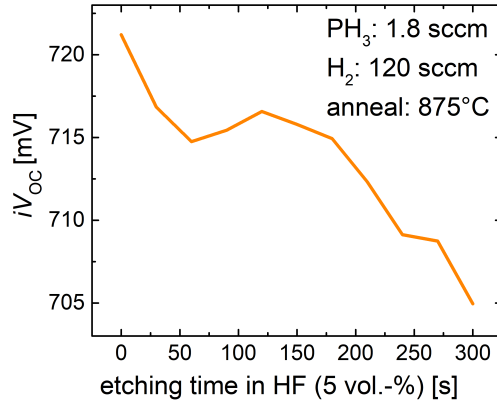


Figure 7.3 – Stability of passivation against hydrofluoric acid (5 vol.-%) for the case of a planar symmetrical sample using a  $\text{PH}_3$  flux of 1.8 sccm,  $\text{H}_2$  flux of 120 sccm annealed at 875 °C.

## 7.4 Crystallinity measured by Raman

The crystallinity of these layers in the as-deposited state were analyzed by Raman spectroscopy, as illustrated in Figure 7.4 for different  $\text{H}_2$  fluxes using a  $\text{PH}_3$  flux of 1.4 sccm (panel a) and of 1.8 sccm (panel b). Already in the as-deposited state, the Raman spectrum is dominated by the transverse optical (TO)  $c$ -Si phonon with a peak around  $520.5 \text{ cm}^{-1}$ . However, the

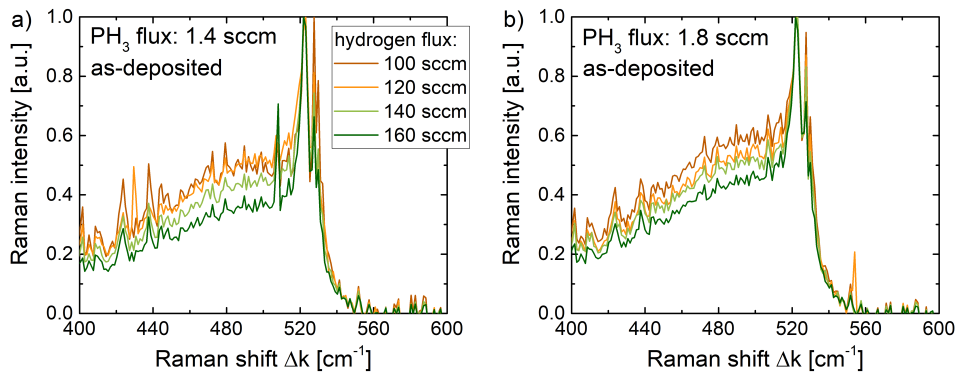


Figure 7.4 – The raman spectra for the as deposited state varying the hydrogen content using a  $\text{PH}_3$  flux of (a) 1.4 sccm and (b) 1.8 sccm, respectively.

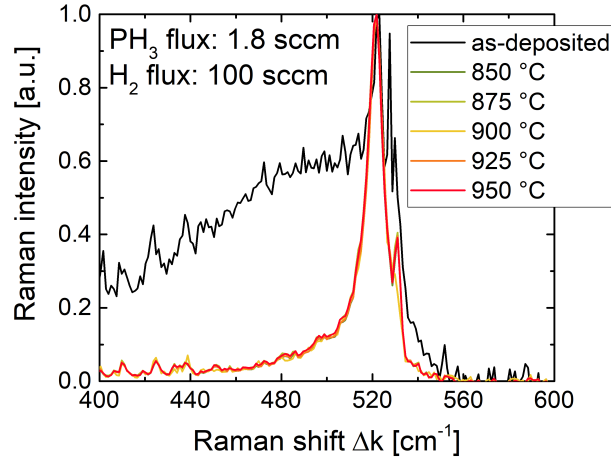


Figure 7.5 – The raman spectra varying the anneal dwell temperature for the case of a flux of 1.8 sccm PH<sub>3</sub> and 100 sccm H<sub>2</sub>.

signal still shows a pronounced shoulder at wavenumbers between 400 cm<sup>-1</sup> and 510 cm<sup>-1</sup> which can be attributed to an amorphous Si phase [Iqbal 1982]. As expected, by increasing the hydrogen flux from 100 sccm (brown) to 160 sccm (dark green) the *a*-Si phase is reduced. Comparing the two phosphine fluxes in panels (a) and panel (b), we observe a slightly more amorphous layer (higher *a*-Si contribution) for the case of 1.8 sccm. We would like to remind the reader that the hydrogen included in the phosphine flux is compensated meaning that the lower crystallinity using 1.8 sccm PH<sub>3</sub> is related to the additional P which contradicts reported results that found a beneficial effect of P on the crystallinity in deposited layers [Matsuda 1980, Shibata 1987, Nomoto 1990]. The different behavior could be related to the presence of fluorine, but further investigations are needed for a better understanding. Please notice that the peaks at 527 cm<sup>-1</sup> and 530 cm<sup>-1</sup> are measurement artifacts.

The influence of the anneal dwell temperature on crystallinity is shown in the Raman spectra in Figure 7.5 for the case of the layer that had the highest amorphous fraction in as-deposited state (PH<sub>3</sub>: 1.8 sccm, H<sub>2</sub>: 100 sccm). No difference is observed between annealing at 850 °C and 950 °C. For all annealing temperatures the amorphous contribution disappears, meaning that the layer crystallizes almost completely. Since the layers have an expected thickness of ~ 20 nm and the collection depth for the used laser (325 nm) is 13 nm [Carpenter 2017] we cannot exclude that below the highly crystalline layer an amorphous fraction is still present.

## 7.5 Doping profile

The resulting phosphorus doping profile after annealing is measured by electro capacitance voltage measurement (ECV) (Figure 7.6). Here, the measured doping profile starts at the

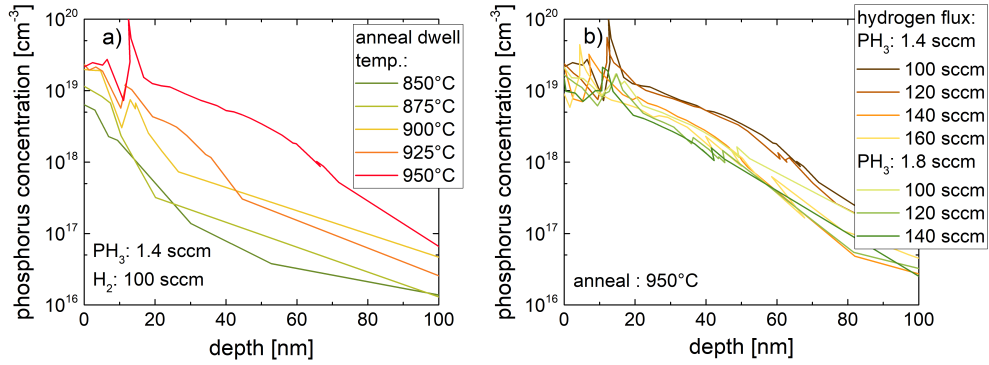


Figure 7.6 – The measured phosphorus doping profile whereas depth 0 nm is the surface of the  $\mu c$ -Si:F(n) layer. In (a) the doping profiles for a variation in anneal dwell temperatures are plotted for the case of a flux of 1.4 sccm  $\text{PH}_3$  and 100 sccm  $\text{H}_2$ . In (b) the anneal dwell temperature is set to 950 °C and the phosphine and hydrogen fluxes are varied.

layer surface. We assume the chem-SiO<sub>x</sub> / wafer interface to be at the peak appearing at around 12 nm resulting from the different etch-rate in the chem-SiO<sub>x</sub>. The concentration and thickness within the layer should be treated with care since the system is calibrated for  $c$ -Si and therefore not adequate within the layer. In panel (a), the doping profiles are shown for the variation in temperature on the example of a flux of 1.4 sccm  $\text{PH}_3$  and 1.8 sccm  $\text{H}_2$ . A low surface concentration as well as a shallow profile is observed for low annealing temperatures and both are increasing with anneal dwell temperature, as expected. In panel (b), the doping profiles for the case of an anneal dwell time of 950 °C are shown for a variation in hydrogen and phosphine flux. The highest surface concentration and the deepest profile is observed for a flux of 1.4 sccm  $\text{PH}_3$  and 100 sccm  $\text{H}_2$ . The surface concentration as well as the depth is decreasing with additional hydrogen. We relate this observation to a lower content of amorphous phase in this layers as observed in the Raman measurements. The amorphous phase can contain more P than  $\mu c$ -Si [Mostafa 2017], and therefore it is likely that it can release more into the wafer during annealing. It is surprisingly, that the higher phosphine flux used during deposition (1.8 sccm) leads to a lower surface concentration and a shallower profile than the flux of 1.4 sccm.

## 7.6 Passivation quality on textured surfaces

The promising passivation obtained on planar surfaces was transferred to textured surfaces using p-type wafers with a base resistivity of 2  $\Omega$  cm. The deposition time was again adjusted by a factor of 1.7 to end up with the same thicknesses as before for planar surfaces. The same range of hydrogen fluxes—100 sccm (brown squares), 120 sccm (orange circles), 140 sccm (light green upward pyramids), and 160 sccm (green downward pyramids)—is investigated and plotted in Figure 7.7 as a function of anneal dwell temperature for a  $\text{PH}_3$  flux of 1.4 sccm

(panel a) as well as 1.8 sccm (panel b). After annealing, for both phosphine fluxes, the lowest hydrogen flux performs best over the full anneal dwell temperature range with a clear optimum at 850 °C and a maximum  $iV_{OC}$  of 707 mV. The optimal performance for all samples is shifted by 50 °C towards lower temperatures and the decrease of passivation at higher temperatures is more pronounced than for planar surfaces.

Hydrogenation was performed again as for the planar samples first by a FGA leading as well to a slight loss in passivation of 5–10 mV for samples annealed at lower temperature (825 °C or 850 °C) whereas samples annealed at higher temperature gain by the FGA up to 20 mV. After atomic hydrogenation by the  $\text{SiN}_x$  layer followed by the hotplate annealing for 30 min at 450 °C (open symbols, measured before  $\text{SiN}_x$  removal), samples with higher anneal dwell temperature improve more and the ones annealed at 875 °C level up with the ones annealed at 850 °C. The maximal  $iV_{OC}$  of 713 mV was observed for a  $\text{PH}_3$  flux of 1.8 sccm and 160 sccm  $\text{H}_2$  annealed at 850 °C. The removal of the  $\text{SiN}_x$  lead to losses of at least 20 mV and the resulted  $iV_{OC}$  is in all cases below the value directly after annealing. Therefore, the hydrogenation needs some more investigations. However,  $iV_{OC}$  values of almost 710 mV without hydrogenation are promising to be used even without hydrogenation.

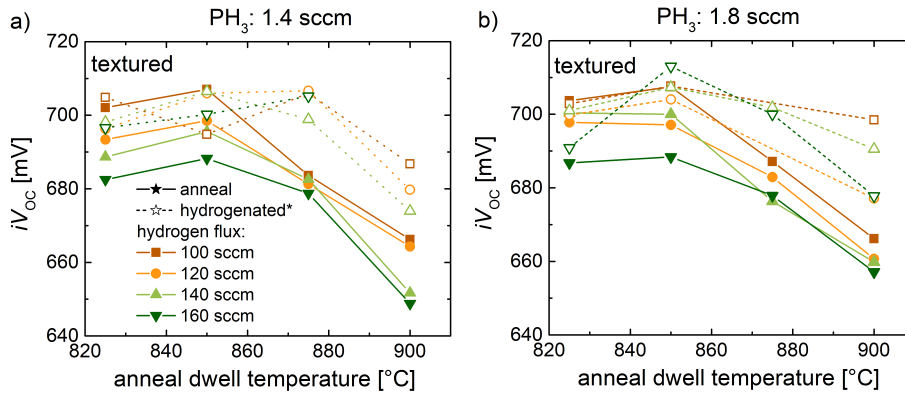


Figure 7.7 –  $iV_{OC}$  for textured symmetrical samples varying the hydrogen fluxes as a function of the anneal dwell time for a  $\text{PH}_3$  flux of (a) 1.4 sccm and (b) 1.8 sccm, respectively. Values directly after annealing are represented by filled symbols, whereas values after hydrogenation\* are represented by open symbols (here the values after hydrogenation\* are measured after the hotplate annealing, but before the removal of the  $\text{SiN}_x$  layer.)

## 7.7 Integration into planar co-annealed cells

As proof-of-concept, the  $\mu\text{c-Si:F(n)}$  electron-selective emitter is combined with two different hole-selective contacts with different thermal budgets to form planar co-annealed cells. First, the  $\mu\text{c-Si:F(n)}$  layer was deposited using 50 sccm  $\text{PH}_3$  together with 140 sccm  $\text{H}_2$  followed by a rear contact of boron-doped  $\text{SiC}_x(\text{p})$ <sup>2</sup> using an annealing of 850 °C for 0 min, so the heating is

<sup>2</sup>The  $\text{SiC}_x(\text{p})$  contact was developed by Gizem Nogay and more details can be found in [Nogay 2018].

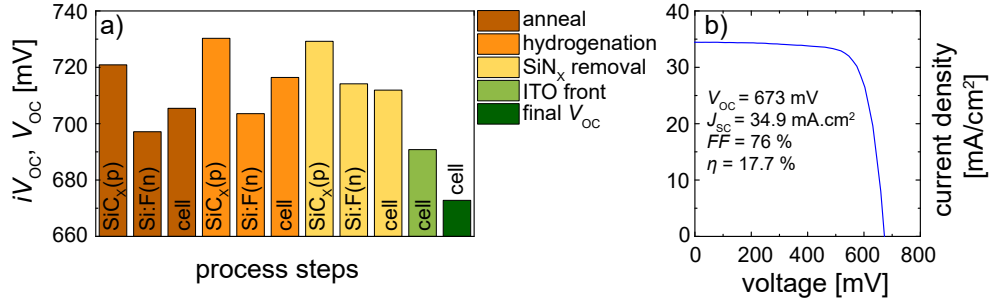


Figure 7.8 – (a) Evolution of the  $iV_{OC}$  after the fabrication steps towards a planar cell. Symmetrical samples with the rear layer ( $SiC_X(p)$ ) and the front layer ( $Si(n):F$ ), respectively, are in comparison with the cell precursor having one of each layer on the front, respectively the rear side. (b)  $J$ - $V$  characteristics of the best cell of this configuration.

directly followed by the cooling ramp.

In Figure 7.8a the evolution of the  $iV_{OC}$  is shown for the symmetrical samples as well as the cell. After annealing (brown), the rear  $SiC_X(p)$  resulted in an  $iV_{OC}$  of 721 mV, whereas the  $\mu c$ - $Si:F(n)$  showed only 697 mV<sup>3</sup>. Since the co-annealed cell precursor shows an  $iV_{OC}$  of 704 mV, we conclude that it is limited by the front. No FGA was used instead directly an atomic hydrogenation by  $SiN_x$  (orange), leading to a boost of the rear to 730 mV, the  $\mu c$ - $Si:F(n)$  front to 704 mV, and the cell precursor to 716 mV. The removal of the  $SiN_x$  (yellow) was done by a 12 min etch in HF (5 vol.-%) and lead to no change for the rear. The front is apparently improved, but we relate the observation to inhomogeneities or a different location of the measurement.

Sputtering the front ITO (light green) lead to a decrease of 20 mV and another 20 mV are lost to the final  $V_{OC}$  (dark green) measured by the  $J$ - $V$  characteristics plotted in Figure 7.8b for the best cell. The large difference between  $V_{OC}$  of 673 mV with respect to the measured  $iV_{OC}$  before metallization shows that further investigations are needed to understand why this contact is so vulnerable by the metallization. On the other side a high  $J_{SC}$  of 34.9 mA/cm<sup>2</sup> is reached for a flat cell design, showing the potential for this  $\mu c$ - $Si:F(n)$  layer as a front contact. Together with a  $FF$  of 76%, a conversion efficiency of 17.8% is achieved for this planar device.

A second approach used the  $SiO_X(i/p)$  rear contact presented in chapter 6. Here, the  $SiO_X(i/p)$  layer was deposited first, followed by the  $\mu c$ - $Si:F(n)$  on the opposite side, using 1.4 sccm  $PH_3$  and 140 sccm  $H_2$ <sup>4</sup>. The annealing was performed at 900 °C for 15 min in the PEO system.

Figure 7.9 shows the measured  $iV_{OC}$  after annealing (brown) for the cell precursor as well

<sup>3</sup>Other  $\mu c$ - $Si:F(n)$  layers deposited the same day showed strong inhomogeneities and also a lower performance as usual

<sup>4</sup>The order used here is not recommended as further experiments have shown that residual oxygen in the deposition chamber can influence following plasma regimes and the resulting layers when fluorine is used. A clear trend or explanation needs a deeper investigation and is beyond the scope of this thesis.

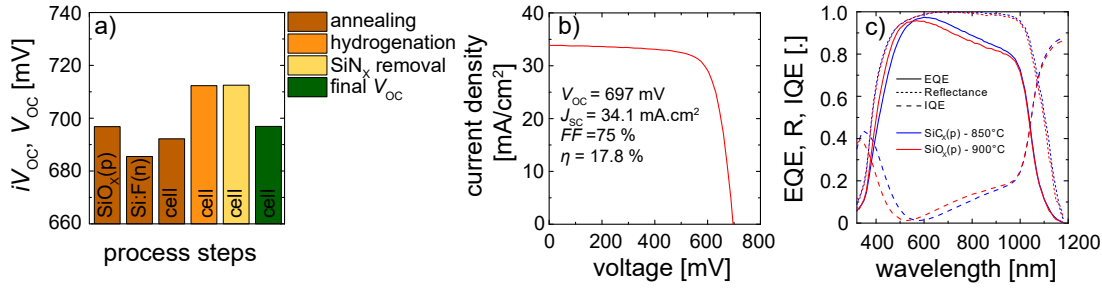


Figure 7.9 – (a) Evolution of the  $iV_{OC}$  after the fabrication steps towards a planar cell. Symmetrical samples with the rear layer ( $\text{SiO}_X(\text{i/p})$ ) and the front layer ( $\text{Si}(\text{n}):F$ ), respectively, are in comparison with the cell precursor having one of each layer on the front, respectively the rear side. (b)  $J$ - $V$  characteristics of the best cell of this configuration. (c) EQE, reflectance, and IQE of this cell in comparison with the cell presented in Figure 7.8.

as for symmetrical samples of the respective front or rear side. Symmetrical samples of the  $\text{SiO}_X(\text{i/p})$  intended for the rear and of the  $\mu\text{c-Si:F}(\text{n})$  intended for the front yield  $iV_{OC}$  values of 697 mV and 685 mV, respectively. Their combination yields an  $iV_{OC}$  of 692 mV for the cell precursor. The hydrogenation was again performed directly with atomic hydrogenation using  $\text{SiN}_X$  and a hotplate annealing (orange). This leads to an  $iV_{OC}$  of 713 mV of the cell precursor and the same value is measured after the removal of the  $\text{SiN}_X$  (yellow). The  $V_{OC}$  of the finished cell (dark green) is 697 mV, thus is only 16 mV below the measured  $iV_{OC}$  before metallization. We conclude that this cell configuration is more tolerant to metallization as the cell with the  $\text{SiC}_X(\text{p})$  rear contact. A possible explanation may be stronger in-diffusion as was observed for  $\text{SiO}_X(\text{n})$  contact presented in chapter 5.

The  $J$ - $V$  characteristics are presented in Figure 7.9b for the best cell with a  $J_{SC}$  of 34.1 mA/cm<sup>2</sup>, a  $FF$  resulting in an efficiency of 17.8%. The lower current compared to the cell presented before is due to a shift of the minimum in the reflectance towards longer wavelength as shown in Figure 7.9c. The measured EQE is therefore lower at wavelengths below 550 nm and higher above 550 nm for the cell annealed at 850 °C compared to the cell annealed at 900 °C. Nevertheless, IQEs are identical for both cells, suggesting that there are no differences in absorption within the  $\mu\text{c-Si:F}(\text{n})$  layer despite the different annealing temperatures. This is corroborated by the Raman spectra shown in Figure 7.5 that annealing at 850 °C renders the layers already highly crystalline.

## 7.8 Integration into co-annealed cells with textured surfaces

Since the  $\mu\text{c-Si:F}(\text{n})$  layers showed promising passivation also on textured surfaces, the process sequence and the influence of ITO sputtering was investigated on three different thicknesses of  $\mu\text{c-Si:F}(\text{n})$  layers. We used conditions of 1.4 sccm  $\text{PH}_3$  and 100 sccm  $\text{H}_2$  and aimed thicknesses of 20 nm, 30 nm, and 40 nm, respectively. In all cases, a 4-nm-thick protection layer of  $\alpha\text{-Si}(\text{n})$

## 7.8. Integration into co-annealed cells with textured surfaces

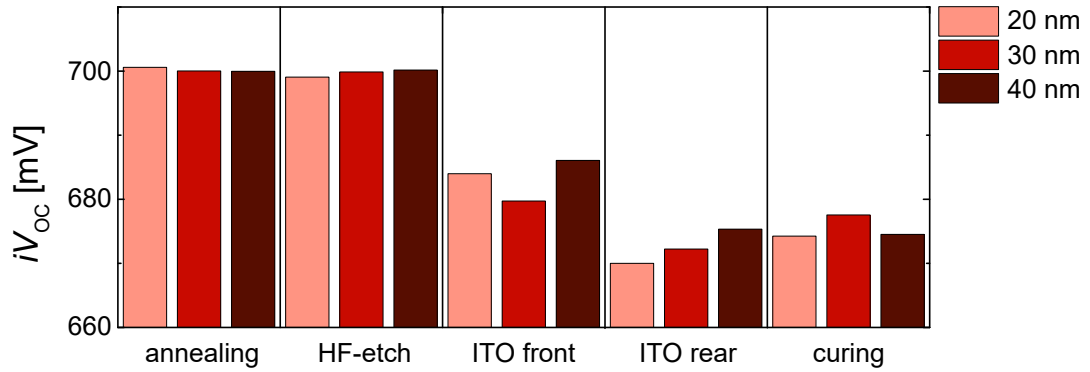


Figure 7.10 – (a) Evolution of the  $iV_{OC}$  during fabrication steps for symmetrical textured samples with three different thicknesses of  $\mu c\text{-Si:F(n)}$ .

was deposited without fluorine. The thicknesses were calculated assuming linear deposition rates and a factor of 1.7 when changing to textured surfaces.

Figure 7.10 shows the evolution of the  $iV_{OC}$  of symmetrical samples in light red (20 nm), red (30 nm), and dark red (40 nm) after the annealing at 850 °C. No influence of the thickness on the passivation is observed, but the measured  $iV_{OC}$  values of 700 mV are slightly below the value of 707 mV presented for the same conditions in section 7.6. Since hydrogenation did not yield an improvement in our earlier experiment, it was skipped here. A short HF-etch (1 vol.-%) of 60 s did not change the passivation, but deposition of 80 nm ITO on one side of the symmetrical samples lead to a decrease in  $iV_{OC}$  between 15 and 20 mV, the sample with the thickest layer losing least. After deposition of 80 nm ITO on the rear side, the  $iV_{OC}$  dropped by another 5 to 15 mV. Curing the samples at 210 °C for 30 min lead to slight improvements of up to 5 mV, but it could not mitigate the losses of ITO sputtering.

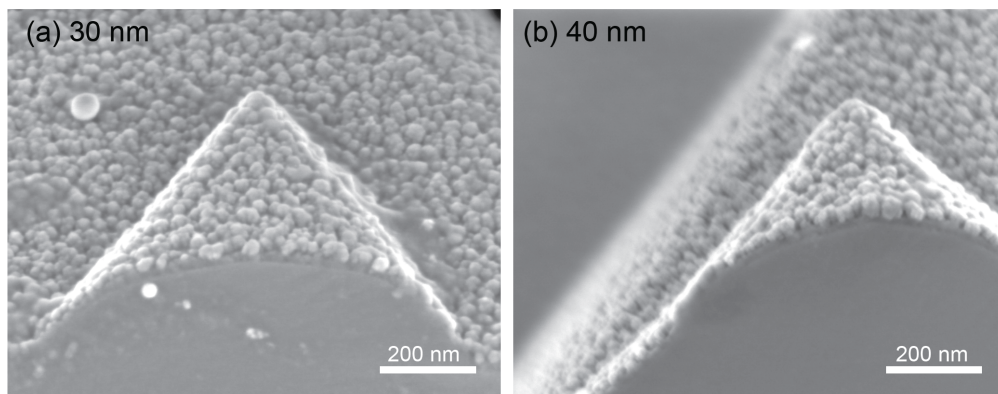


Figure 7.11 – Scanning electron micrographs for the two thicknesses (a) 30 nm and (b) 40 nm after annealing on textured surfaces.

The high losses by ITO sputtering are possibly related to the surface morphology of the layers after annealing. Figure 7.11 shows SEM images of the layers with targeted thickness 30 and 40 nm in panels (a) and (b), respectively. In a) large grains with diameters between 20–30 nm are observed. Below the grains, a thin layer is distinguishable which we relate to a thin amorphous silicon layer of a few nm. The chem-SiO<sub>x</sub> is beyond the resolution of SEM and is therefore not expected to be observed. In b) for the targeted thickness of 40 nm, the grain size is clearly enhanced up to 50 nm. In both cases, the presence of crystals that are much larger than the targeted layer thickness leads to a porous structure with empty spaces between the crystals. During chemical treatments like the removal of the SiN<sub>x</sub> layer or sputter processes like ITO deposition, the porous structure is likely penetrated and the underlying chem-SiO<sub>x</sub> becomes damaged. Since these layers showed a high resistivity against chemical treatments when deposited on planar surfaces (c.f. Figure 7.3), we expect that the formation of the granular structure is more pronounced on textured surfaces, or that penetration of impurity atoms appears mainly at the tips or valleys.

Nevertheless, first hybrid devices using these three different thicknesses were processed on both-side-textured p-type wafers. After the front PECVD deposition, a protection layer was deposited on the rear (for more details, see section 6.6.1). The samples were then annealed at 850 °C together with the symmetrical samples presented before. Without any hydrogenation, the protection layer was removed by a one sided HF-etch (Double-droplet method) before the *a*-Si(i)/*a*-Si(p)SHJ rear was deposited. After another HF-etch (1 vol.-%) for 60 s, two different front contacts were sputtered on the samples. One set received 80 nm of ITO, the second set received 87 nm of tungsten-doped indium oxide (IWO). At the rear, 130 nm ITO was sputtered for all of them together with a silver reflector. Due to practical reasons, the rear side deposition was done before the front side for the samples with IWO. The full set of samples was finished by a screen-printed silver grid and curing at 210 °C for 30 min. Additionally, one single-side-textured wafer is added which was deposited (20 nm) and annealed together with the others, but at the planar rear the SiC<sub>x</sub>(p) layer, presented in the section before (7.7), was deposited resulting in a co-annealed cell.

The *J*-*V* characteristics are shown in Figure 7.12. As expected from the results on symmetrical samples, the *V*<sub>OC</sub> is low for ITO metallization (filled symbols) with values around 670 mV compared to *iV*<sub>OC</sub> values after the SHJ rear deposition of ~ 710 mV independently of the *μc*-Si:F(n) thickness. No difference is observed for the co-annealed cell (blue stars). Sputtered IWO (open symbols) seems to result in slightly lower losses with a maximum of 688 mV for the thinnest layer and values of 677 mV and 676 mV for 30 nm and 40 nm, respectively.

The *J*<sub>SC</sub> is promisingly high for IWO metallized samples, reaching values between 39.92 and 39.72 mA/cm<sup>2</sup>. Thus, increasing the *μc*-Si:F(n) layer thickness by 20 nm yields minor absorption losses of only 0.2 mA/cm<sup>2</sup>.

The *FF* is slightly decreased for thicker layers in hybrid cells with ITO metallization. With a maximum of 65% it remains clearly below the results of planar cells. Interestingly for the

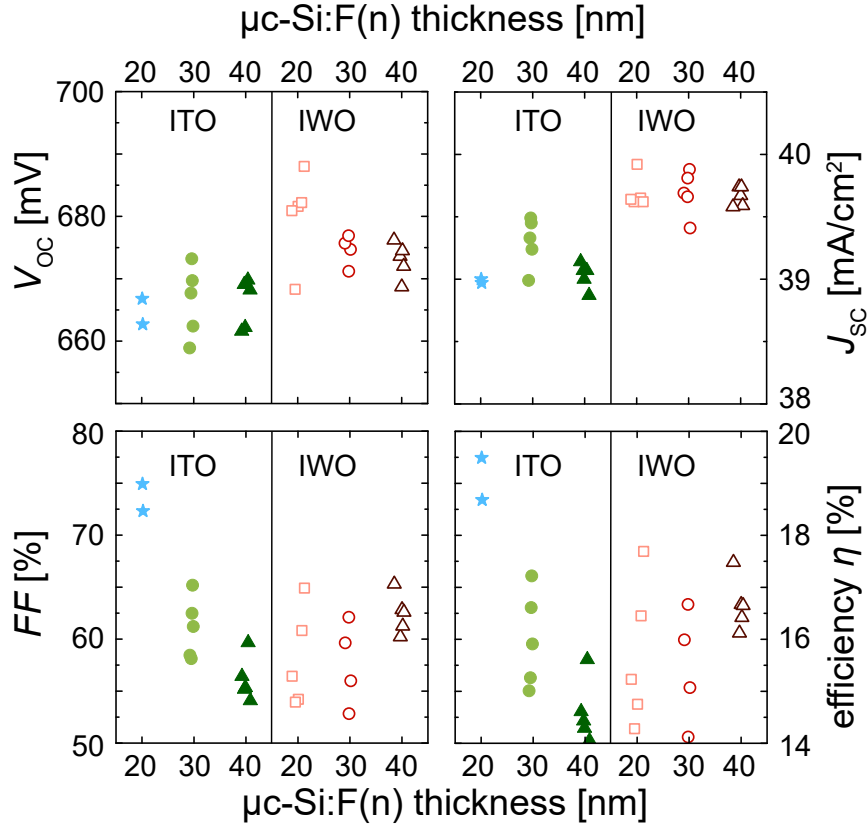


Figure 7.12 –  $J$ - $V$  characteristics using three  $\mu c$ -Si:F(n) layer thicknesses—20 nm, 30 nm, and 40 nm—metallized either by ITO (filled symbols) or by IWO (open symbols). Please notice that the sample with 20 nm  $\mu c$ -Si:F(n) metallized by ITO (blue stars) is a co-annealed cell with a  $\text{SiC}_X$  layer on the planar rear in contrary the other cells are double-side-textured hybrid cells.

co-annealed cell a  $FF$  of 75% is observed which hints towards poor performance of the SHJ rear. Due to the increased  $FF$  the single-side-textured co-annealed cells reaches the highest conversion efficiency of 19.5%, for which we would like to remind the reader that no hydrogenation process was applied. For the hybrid cells, the high current cannot compensate the losses in  $V_{OC}$  due to TCO deposition and the low  $FF$  leading to best efficiency of 17.7% for the thickest  $\mu c$ -Si:F(n) layer metallized by IWO.

In Figure 7.13 the EQE (solid line), the reflectance (R, dashed line) and the corresponding internal quantum efficiency (IQE, dotted line) are plotted, measured including the metal grid. In a) the cells metallized with ITO are shown, for which we would like to remind the reader that the cell with 20 nm  $\mu c$ -Si:F(n) layer thickness is a co-annealed cell on single-side-textured (SST) wafer with a planar rear. Below 800 nm, no difference is observed for the EQE 20 nm (blue) and 30 nm (light green), only at wavelength above 1000 nm the SST has a lower response which is mainly related to the higher reflectance due to the planar rear. Focusing on the reflectance, a small increase is observed below 600 nm for thicker layers, leading to a small

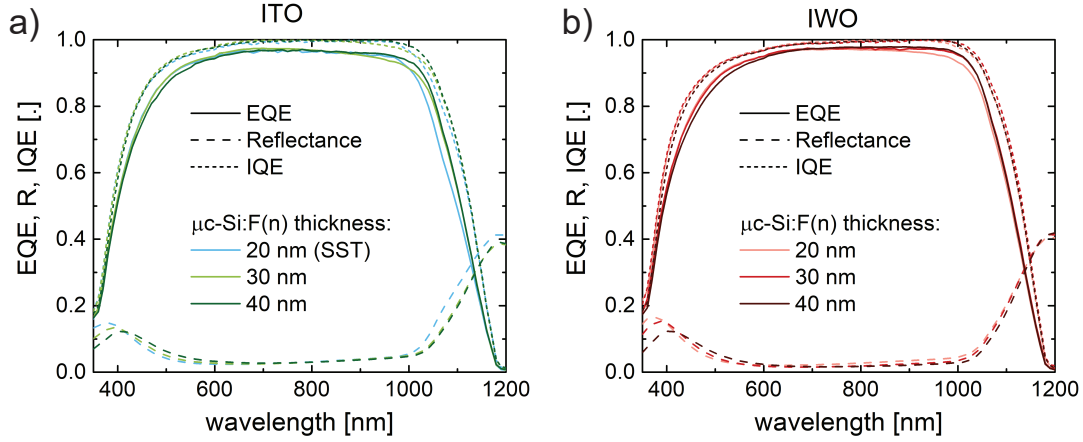


Figure 7.13 – The external quantum efficiency (EQE, solid lines), reflectance (R, dashed lines) and the corresponding internal quantum efficiency (IQE, dotted lines) for 20 nm, 30 nm, and 40 nm  $\mu\text{c-Si:F(n)}$  layer thickness metallized by ITO (a) or by IWO (b)

decrease in EQE for the sample with a layer thickness of 40 nm (dark green). The same trends are observed using IWO as metallization (Figure 7.13b). A small decrease in EQE below 700 nm which is mainly related to the reflectance, even though for the case of 40 nm a small decrease in IQE remains compared to the thinner layers.

## 7.9 Conclusion

In this chapter a second approach is presented to reach transparent selective emitters by using highly crystalline layer. Adding  $\text{SiF}_4$  to the precursor gases yields starting layers with low amorphous content that crystallize easily even at low annealing temperatures of 850 °C.

Additionally, we note a beneficial effect of fluorine in the layers in terms of passivation. We obtained  $iV_{\text{OC}}$  values up to 730 mV on planar surfaces and 707 mV on textured ones, directly after annealing without the need of an additional hydrogenation process.

First planar co-annealed cells are presented either with a  $\text{SiC}_x(\text{p})$  or  $\text{SiO}_x(\text{i/p})$  rear leading to high current whereas the transfer of the high passivation quality to cell level still needs some more investigations as well as an optimization in terms of  $FF$ .

Furthermore the layers are applied on textured surfaces in hybrid cells as well as co-annealed on the front of single-side-textured cells. Due to the texturing, currents up to 40  $\text{mA}/\text{cm}^2$  are achieved for three different thicknesses, including ~ 3% metallization area, pointing towards the high transparency and the potential of this material for front side applications.

## 8 Conclusions

In this chapter the conclusions of each chapter can be found and we summarize the whole work in section 8.2 followed by a perspective in 8.3.

### 8.1 Summary of each chapter

#### 8.1.1 Chapter 3: Mixed-Phase silicon oxide — Structure

In this chapter, the structure of the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack in the as-deposited state and the structural changes that occur during thermal annealing were investigated in detail. Raman measurements revealed the high crystallinity of the nc-Si(n) layer for different thermal budgets as well as the related stress release within the layer.

In a detailed analysis by TEM, the mixed-phase nature of the mp-SiO<sub>x</sub>(n) layer was investigated and two different growth regimes were identified: Region A with columnar silicon-rich phases and region B forming cones with an apex angle of  $\sim 75^\circ$  which is responsible for the high surface roughness. Using in-situ annealing inside the TEM in EDX mode revealed the redistribution of elements undergoing the structural change with temperature. The silicon-rich phases within the oxide matrix remain mainly amorphous whereas the nc-Si(n) top layer starts to crystallize at 750 °C. The oxygen content in the mp-SiO<sub>x</sub>(n) layer was found to be 50–60% at the chem-SiO<sub>x</sub>/wafer interface and to decrease gradually to around 25% towards the border with the nc-Si(n) layer. With increased temperature a slight increase within the mp-SiO<sub>x</sub>(n) layer was observed going along with a slight decrease in its thickness. The phosphorus content in the nc-Si(n) layer was higher compared to the mp-SiO<sub>x</sub>(n) layer in the as-deposited state and is shifting towards the wafer with annealing, leading to a higher content in the mp-SiO<sub>x</sub>(n) layer after annealing. The intrinsic chem-SiO<sub>x</sub> remains depleted of P before and after thermal treatment.

Silicon oxide channels through the entire layer stack were found to be one of the main reasons for the high sensitivity to chemical treatments. On textured surfaces, replacing the nc-Si(n)

## Chapter 8. Conclusions

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layer with  $a$ -Si led to less homogeneous coverage due to increased surface roughness, whereas introducing a seed layer of  $a$ -Si between chem-SiO<sub>x</sub> and mp-SiO<sub>x</sub>(n) layer demonstrated a clear decrease in surface roughness.

Therefore, we propose three strategies to reduce the formation of oxide channels and to improve chemical stability. (i) A reduction of the hydrogen content in the deposition regime might suppress the nucleation. It would be necessary to take care that the vertical silicon phases of region A are grown so that the nc-Si(n) layer can cover well the smoother surface. (ii) An increase of nucleation sites should reduce the distances between cones, such that they merge before the desired film thickness is reached as was demonstrated with the  $a$ -Si seed layer. However, this would lead to an increased silicon content which is detrimental for the transparency. (iii) A reduction of the residual oxygen in the tube furnace would decrease the oxidation at the surface and would probably suppress the formation of channels.

### 8.1.2 Chapter 4: Mixed-Phase silicon oxide — Influence of thickness and anneal dwell temperature

In summary, this chapter showed the beneficial effect of the addition of the mp-SiO<sub>x</sub>(n) layer between the chemical oxide and the nc-Si(n) layer to enhance thermal stability of surface passivation. In-diffusion of phosphorus creates a doping profile with surface concentration of  $3.92 \cdot 10^{20}$  atoms/cm<sup>3</sup>. Without any hydrogenation for defect passivation, emitter saturation current densities of 12.8 fA/cm<sup>2</sup> (n+/p-junction) and 10.7 fA/cm<sup>2</sup> (n+/n-junction) are reached. With forming gas annealing, an excellent surface passivation is achieved with emitter saturation current densities of 9.0 fA/cm<sup>2</sup> for n+/p-junction and 5.3 fA/cm<sup>2</sup> for n+/n junctions, respectively, yielding specific contact resistivities between 19 mΩ cm<sup>2</sup> and 86 mΩ cm<sup>2</sup>.

Additional insight into the current pathway of this passivating contact is gained by monitoring  $\rho_{c,TLM}$  and  $R_{SH,TLM}$  as the contact layers and the surface of the underlying wafer are gradually etched off. We find that the mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack does not significantly contribute to the measured resistivity.

### 8.1.3 Chapter 5: Mixed-Phase silicon oxide — Influence of initial doping concentration and anneal dwell time

We investigated the influence of the initial doping concentration and the anneal dwell time at 900 °C on electron-selective passivating contacts based on a highly phosphorus-doped mp-SiO<sub>x</sub>(n)/nc-Si(n) layer stack, and we related our findings to the properties of the junction. The results indicate a trade-off between reduced recombination due to a reduced density of minority carriers in the in-diffused region and the interface, and increased recombination by the Auger effect and at the defects created in the interfacial oxide.

Based on EDNA 2 simulations we discussed the impact of the doping profile on the relation between the emitter saturation current density  $J_0$  and the surface recombination velocity

SRV. The contact presented here exhibits a very similar dependence of SRV on phosphorus surface concentration as for passivation with dielectric layers reported in the literature. A deeper profile with a higher phosphorus concentration is less sensitive to the SRV and relies therefore less on chemical passivation of the interface. When using hydrogenation to optimize surface passivation it should be kept in mind that the negative influence of the ITO sputtering (causing surface passivation damage) may be stronger in case of a predominant chemical passivation. For our sputtering conditions, we find a  $J_0$  value of 12.1 fA/cm<sup>2</sup> for higher doping levels and we note that such P doping levels are also needed in our mixed-phase SiO<sub>x</sub> contacts to ensure a sufficient carrier transport through the layer.

Finally, we presented a planar proof-of-concept solar cell with a  $FF$  of 79.4%, a  $J_{SC}$  of 33.9 mA/cm<sup>2</sup> and a  $V_{OC}$  of 691 mV leading to a conversion efficiency of 18.6%.

This result points out that the use of high doping levels in the deposited layers enables an efficient current extraction whereas the nano-structure of the mixed-phase SiO<sub>x</sub> layer ensures a low level of parasitic absorption in the layers of our front-contact, enabling comparatively high short-circuit current density for our flat cells.

Additionally, we found that this layer stack is capable of strengthening the anti-reflection behavior of our ITO front contact.

### 8.1.4 Chapter 6: Mixed-Phase silicon oxide — optical analysis and cell integration

In this chapter the optical properties of mp-SiO<sub>x</sub>(n) and nc-Si(n) were investigated in detail. Starting with the determination of the refractive index  $n$  and extinction coefficient  $k$  for the individual layers in the mp-SiO<sub>x</sub>(n)/nc-Si(n) bilayer stack by spectroscopic ellipsometry. For the mp-SiO<sub>x</sub>(n) layer, values for  $n$  as well as for  $k$  were found to be between the ones of SiO<sub>2</sub> and SiO<sub>1</sub> confirming the high oxygen content found in the structural analysis in chapter 3 and confirming its potential as a transparent layer. The nc-Si(n) layer showed a wavelength dependence closer to  $c$ -Si than  $a$ -Si with a higher  $n$  at 300 nm and 400 nm but still less pronounced than for  $c$ -Si.

A deeper analysis was performed on several parameters influencing the in-diffusion of phosphorus to the wafer during the annealing at 900 °C. We found an interesting relation between the depth and the surface concentration of the diffused profile and the wafer polarity as well as its base resistivity, pointing towards a different growth of chem-SiO<sub>x</sub> on varying base materials. A way of suppressing or intensify the diffusion to the wafer is presented by either a variation in the mp-SiO<sub>x</sub>(n) thickness or by introducing an intrinsic SiO<sub>x</sub>(i) layer of a certain thickness.

For the implementation into working solar cell devices, we tested the chemical stability against cleaning methods as well as hydrofluoric acid, and finally two ways of integration were presented: First in proof-of-concept hybrid cells together with a heterojunction  $a$ -Si(p)

hole-contact, and second by co-annealed cells using a  $\text{SiO}_x(\text{i/p})$  hole-selective emitter with the same thermal budget as the  $\text{SiO}_x(\text{n})$  contact. For the hybrid cells, a protection layer based on an amorphous silicon oxide was developed against in-diffusion of impurities on the rear side.

On working planar hybrid cells the  $n$  and  $k$  values of the  $\text{mp-SiO}_x(\text{n})$  layer and the  $\text{nc-Si}(\text{n})$  layer were tested by a variation of the thicknesses of the individual layers and modeling of the resulting reflectances by OPAL. Out of the thickness-dependent losses in the measured internal quantum efficiencies, the absorption losses were quantified to  $0.4 \text{ mA/cm}^2$  per 10 nm within the  $\text{nc-Si}(\text{n})$  layer and only  $0.07 \text{ mA/cm}^2$  per 10 nm for the  $\text{mp-SiO}_x(\text{n})$  layer respectively.

In planar co-annealed cells, the high transparency in combination with a low reflectance showed the potential with a  $J_{\text{SC}}$  of  $35.0 \text{ mA/cm}^2$  without the usage of an additional anti-reflection coating. Additionally, the  $FF$  of almost 80% demonstrated efficient carrier transport through the mixed-phase layer. With a  $V_{\text{OC}}$  of 686 mV, this resulted in a promising conversion efficiency of 19%.

Transferring the  $\text{SiO}_x(\text{n})$  layer to textured surfaces showed degradation during the fabrication process in co-annealed solar cells (rear side  $\text{SiO}_x(\text{i/p})$  on planar surface) which could be improved by replacing the  $\text{nc-Si}(\text{n})$  layer by an  $\text{a-SiC}_x(\text{n})$  layer reaching conversion efficiencies of up to 20.1%.

Finally, the  $\text{SiO}_x(\text{n})$  contact structure was applied to both-side-textured surfaces using the approach of hybrid solar cells reaching short-circuit current densities up to  $40 \text{ mA/cm}^2$  showing the potential as a transparent front side contact.

### 8.1.5 Chapter 7: Highly crystalline silicon layers with fluorinated precursors

In this chapter a second approach is presented to reach transparent selective emitters by using highly crystalline layer. Adding  $\text{SiF}_4$  to the precursor gases yields starting layers with low amorphous content that crystallize easily even at low annealing temperatures of  $850^\circ\text{C}$ .

Additionally, we note a beneficial effect of fluorine in the layers in terms of passivation. We obtained  $iV_{\text{OC}}$  values up to 730 mV on planar surfaces and 707 mV on textured ones, directly after annealing without the need of an additional hydrogenation process.

First planar co-annealed cells are presented either with a  $\text{SiC}_x(\text{p})$  or  $\text{SiO}_x(\text{i/p})$  rear leading to high current whereas the transfer of the high passivation quality to cell level still needs some more investigations as well as an optimization in terms of  $FF$ .

Furthermore the layers are applied on textured surfaces in hybrid cells as well as co-annealed on the front of single-side-textured cells. Due to the texturing, currents up to  $40 \text{ mA/cm}^2$  are achieved for three different thicknesses, including  $\sim 3\%$  metallization area, pointing towards the high transparency and the potential of this material for front side applications.

## 8.2 Conclusion

### 8.2.1 Approach and structure

A novel approach for an electron-selective passivating contact was presented using plasma-enhanced chemical vapor deposition to grow a mixed-phase  $\text{SiO}_x$  of vertically oriented silicon filaments embedded in a silicon oxide matrix. The resulting layers combine high transparency and vertical conductivity. The proposed contact structure contains three layers, starting with an ultra-thin ( $\sim 1.2\text{ nm}$ ) chemically grown silicon  $\text{SiO}_x$  layer at the *c*-Si wafer surface, followed by a phosphorus-doped bilayer of the mixed-phase  $\text{SiO}_x$  (mp- $\text{SiO}_x(\text{n})$ ) and terminated by a nanocrystalline silicon (nc-Si(n)) layer which ensures contact to the metallization. The contact was analyzed in detail with respect to its structure and its change under thermal treatment. We differentiated two growth regions within the mp- $\text{SiO}_x(\text{n})$  layer, one with the vertically oriented silicon inclusions and a second one where the silicon phases have more lateral growth. The latter results in a locally increased thickness due to its higher deposition rate leading to a rough surface. Together with the oxide layer on top, which grows thermally during the annealing step, regions that are noticeably thinner can form detrimental vertical oxide channels through the whole mp- $\text{SiO}_x(\text{n})$ /nc-Si(n) layer stack. These oxide channels are the main reason for the high sensitivity to chemical treatments.

During thermal treatment, the mixed-phase nature with the silicon inclusions remain. The crystallization and the atomic distribution as well as their changes within the layers were analyzed in-situ during annealing leading to a better understanding of the phosphorus and oxygen redistribution as well as the nucleation sites. The phosphorus content in the nc-Si(n) layer is higher than that in the mp- $\text{SiO}_x(\text{n})$  layer in the as-deposited state and shifts towards the wafer with annealing, leading to a higher content in the mp- $\text{SiO}_x(\text{n})$  layer after annealing. The intrinsic chem- $\text{SiO}_x$  remains depleted of P before and after thermal treatment.

### 8.2.2 Passivation and cell integration

The potential of this contact structure was shown first on symmetrical test samples which reached saturation current densities below  $6\text{ fA/cm}^2$  on n-type and p-type wafers.

The limitations of this structure are its sensitivity to chemical treatments that are used during the fabrication process (especially on textured surfaces) and its sensitivity to sputter processes for metallization by ITO. Whereas sputter-induced damage on planar substrates could be reduced by higher doping and longer annealing dwell time, these treatments were not as beneficial on textured surfaces.

Nevertheless, implementing this contact in working proof-of-concept devices led to conversion efficiencies of 19.0% and 20.1% on planar and textured surfaces, respectively. Short-circuit current densities ( $J_{\text{SC}}$ ) of  $35.0\text{ mA/cm}^2$  (planar) and  $40.0\text{ mA/cm}^2$  (textured) confirmed the high transparency of this contact strategy, and revealed that the reflectance

is reduced over a broad wavelength range due to a smooth index transition that acts like a built-in double anti-reflection coating (ARC).

### 8.2.3 Fluorinated passivating contacts

A second approach to making transparent selective emitters by using a highly crystalline layer deposited from  $\text{SiF}_4$  was presented.  $iV_{\text{OC}}$  values of up to 730 mV on planar surfaces and 707 mV on textured ones indicate the passivation benefit of fluorine in the layers directly after annealing without the need for an additional hydrogenation process.

High currents were observed at the cell level, whereas the transfer of the high passivation quality from symmetrical test samples to cells is demanding as the integration requires additional processing steps. Nevertheless,  $J_{\text{SC}}$  values of  $40 \text{ mA/cm}^2$  were reached and the passivation quality demonstrated so far is still promising for integration in front-side applications.

## 8.3 Perspective

The potential of passivating contacts on planar rear surfaces has been shown by several groups in recent years. Its eventual transfer to industry is therefore just a question of time. This work addresses a generation of solar cells with passivating contacts at the front. Therefore, the transparency must be improved, and a better compatibility with textured surfaces must be demonstrated. The approaches shown are highly transparent and provide good surface passivation, but their applicability in solar cells still needs refinement to overcome the losses incurred by chemical treatments and by ITO sputtering.

For the  $\text{SiO}_x(\text{n})$ -based contact, we identified the surface roughness as one of the main reasons for chemical instability.

One possible mitigation would be to suppress the nucleation of larger Si-rich grains. This should be possible by reducing the hydrogen content in the deposition regime, but care should be taken that the fine-grained silicon phases are still present in the films.

A second possibility would be to increase nucleation sites, such that the distances between the formation of cones is reduced. In that case the cones merge together before the desired film thickness is reached. The feasibility of this approach was demonstrated with an  $a$ -Si seed layer, but the increased silicon content of this approach is detrimental for the transparency.

Alternatively, an  $a$ -SiC(n) capping layer replacing the nc-Si(n) layer was found to increase the chemical stability. However, this approach works only if the layer is thick enough for wetting and full coverage, and thus leads to increased parasitic absorption as well.

Additionally, silver paste fired through a nitride anti-reflection coating could replace the ITO.

In SHJ solar cells, the lateral conductivity of the ITO is needed for the current transport to the fingers, while in our contact structure this is not the case thanks to the in-diffused region present over the full wafer surface ensuring lateral conductivity. Since the mp-SiO<sub>x</sub>(n) layer showed very low parasitic absorption, the thickness could be increased so that the variation in depth of silver spiking through the nitride might not be detrimental if all the spikes were to end within the mixed-phase layer.



# A Passivated interfaces in fluorinated microcrystalline silicon thin film solar cells

We present here a study performed before the work on passivating contacts for crystalline silicon solar cells had started. The effect of a passivating buffer layer is studied in single-junction microcrystalline silicon ( $\mu\text{c-Si:F(i)}$ ) solar cells grown by plasma-enhanced chemical vapor deposition (PECVD) from a  $\text{SiF}_4/\text{H}_2/\text{Ar}$  precursor mixture. We present a strong increase in  $V_{\text{OC}}$  together with a high  $FF$  by implementing an amorphous buffer layer at the i-n interface of highly crystalline  $\mu\text{c-Si:F}$  thin film solar cells. In contrary to the previous chapters, no crystalline wafer is used and the  $\mu\text{c-Si:F(i)}$  layer is grown 650–1300 nm thick and used as solar cell absorber.

For readers who are not familiar with silicon-based thin film solar cells, the structure and working principle is sketched in section A.2 and explained in more detail in [Stuckelberger 2014, Hänni 2014].

The results of this chapter were published in 2015 as *proceeding to the Photovoltaic Specialist Conference (PVSC)* [Stuckelberger 2015].

## A.1 Introduction

In this chapter we present an excursion to silicon-based thin-film solar cells which were one of the main research areas of PV-Lab. In 2014, a world record efficiency of 10.7% was demonstrated for microcrystalline single-junction cells [Hänni 2014], and an efficiency of 12.6% was demonstrated with a micromorph tandem cell [Boccard 2014]. Soon after that, the activities on thin film silicon solar cells were stopped in response to the declining market of this technology. Nevertheless, silicon thin film solar cells have several advantages like the use of abundant materials, the lowest energy payback time of all types of solar cells, the possibility of fabricating large area flexible solar cells independently of shape, and a large variety of colors. However, the technology could not overcome its main drawbacks, i.e. its comparatively low efficiency which became an increasingly severe handicap. In an economic environment where the fabrication of the solar cell itself is not the main driver

for cost, but the installation and the module fabrication [Stuckelberger 2014], higher cell efficiency translates directly into decreased cost per produced power. Whereas technology lost the battle against *c*-Si for electricity generation in power plants, there is nevertheless a niche market for low-consumption devices. Some research groups pursue the development as demonstrated by the latest results with a triple-junction cells that reach efficiencies of 14% [Green 2017, Sai 2015].

Hydrogenated microcrystalline silicon ( $\mu c$ -Si:H) has shown the highest potential for high efficiencies within single-junction silicon-based thin film solar cells. Specifically, cells with an intrinsic layer deposited in a regime close to the amorphous/microcrystalline transition (Raman crystalline fraction  $R_c \sim 55$ –60%) are reported to reach a high open-circuit voltage ( $V_{OC}$ ). This is mainly due to a passivation of the grain boundaries by the amorphous fraction, but the poor transport in the amorphous matrix generally yields low  $FF$ , and the high amount of matrix material lowers the absorption coefficient [Zhang 2008, Mai 2005, Dornstetter 2014a, Droz 2004, Stuckelberger 2013]. Different studies showed promising results with highly crystalline absorber materials deposited by plasma-enhanced chemical vapor deposition (PECVD) using a mixture of  $\text{SiF}_4/\text{H}_2/\text{Ar}$  as precursor gases (henceforth, referred to as  $\mu c$ -Si:F) [Zhang 2008, Dornstetter 2014a, Dornstetter 2013, Hänni 2014]. These studies reported cells with efficiencies above 8% and obtained  $V_{OC}$  values which were not influenced significantly by the layer thickness. Maintaining  $V_{OC}$  values above 500 mV even for  $\sim 4$ - $\mu\text{m}$ -thick cells, indicates a high-quality material [Dornstetter 2013]. However, material quality is not the only limiting factor for  $V_{OC}$ , also interfaces play a crucial role [Yue 2008]. Different approaches with buffer layers have been shown to increase the performance in  $\mu c$ -Si:H cells. For example a silicon oxide layer at the p-i interface lowers efficiently the  $V_{OC}$  losses at lower illumination levels [Bugnon 2014]. Likewise, buffer layers of amorphous silicon (*a*-Si:H) at the i-n interface were reported to boost the  $V_{OC}$  [Hänni 2015]. Here, we study the effect of such buffer layers at the i-n interface, and investigate its effect on device performance when introduced in  $\mu c$ -Si:F cells with highly crystalline absorber layers ( $R_c > 85\%$ ). In addition, we compare it to the effect that the interlayer has on cells with standard  $\mu c$ -Si:H layers ( $R_c > 50\%$ ). Its influence on  $V_{OC}$  is analyzed to separate the bulk contribution to the one from the interface by exploring the interplay of the intrinsic absorber layer with different intrinsic buffer layer thicknesses. We demonstrate that the  $V_{OC}$  can be improved from 490 mV to over 510 mV by applying an optimal *a*-Si(i)/*a*-Si(n) interlayer at the  $\mu c$ -Si:F i-n interface.

### A.2 Experimental details

All technologies presented so far are based on a crystalline silicon wafer as absorber, whereas for silicon thin film, the whole solar cell is grown layer by layer leading to a structure as sketched in A.1. The cells were processed in superstrate p-i-n configuration. First a substrate (here a  $4 \times 4 \text{ cm}^2$  corning glass, but also flexible polymers are used) is covered by a  $5 \mu\text{m}$  boron-doped zinc oxide (ZnO:B) layer grown by low-pressure chemical vapor deposition (LPCVD). The as-grown surface of ZnO:B is textured with randomly oriented pyramids [Nicolay 2009, Fanni 2016].

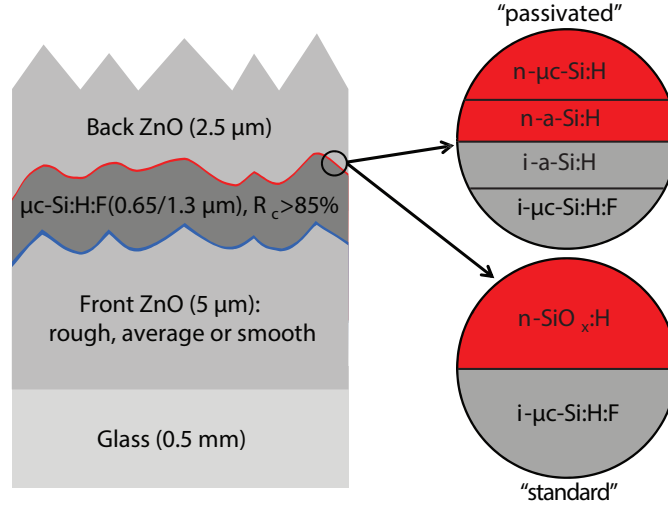


Figure A.1 – Sketch of the passivation layers present at the i-n interface compared to the not-passivated “standard” (adapted from [Hänni 2015]).

While the texture is essential for efficient light trapping, it is challenging to grow high-quality  $\mu c$ -Si:H layers on top of it. Accumulation of porous material in the valleys of the texture results in decreased solar cell performance [Python 2008]. Therefore the surface is smoothened by an Ar plasma treatment [Boccard 2012] with varying duration in order to control the surface roughness. A longer treatment (90 min) results in a smoother surface, leading to higher bulk quality with fewer zones of porous and defective material. This is followed by a PECVD deposition of  $p$ - $i$ - $n$  layers all grown subsequently in the system Kai-M. The rear electrode also a layer of ZnO:B grown by LPCVD. On each glass substrate, 16 cells with an area of 0.025 cm<sup>2</sup> are patterned by two steps; first, the rear electrode between the cells is etched in HCl, then the remaining areas of the rear electrode are used as hard mask to remove the silicon between the cells by dry-etching in a SiF<sub>6</sub>/O<sub>2</sub> plasma. More detailed information can be found in [Hänni 2014, Stuckelberger 2014].

In this contribution, a “passivated” silicon layer stack on top of the ZnO:B layer ( $\mu c$ -SiO<sub>x</sub>(p)/ $\mu c$ -SiO<sub>x</sub>(i)/ $\mu c$ -Si:F(i)/ $a$ -Si(i):H/ $a$ -Si(n):H/ $\mu c$ -Si(n):H) is introduced, sketched in Figure A.1, which also includes a  $\mu c$ -SiO<sub>x</sub> buffer layer at the p-i interface as reported by [Bugnon 2014]. The stack was deposited by PECVD using silane diluted in hydrogen, except for the intrinsic layer, where a precursor gas mixture of SiF<sub>4</sub>/H<sub>2</sub>/Ar with a high hydrogen dilution was chosen. We observe a Raman crystalline fraction of more than 85% as measured from the p-side. These cell architectures are compared to cells with non-passivated i-n interface, where the intrinsic layer is directly followed by a  $\mu c$ -SiO<sub>x</sub>(n) layer (“standard” in Figure A.1). We note that the use of the  $\mu c$ -SiO<sub>x</sub>(n) layer on the amorphous buffer layer results in low  $FF$ , therefore we revert to an n-layer made of  $\mu c$ -Si:H [Hänni 2015]. A 2.5 μm LPCVD-ZnO:B was used as back electrode. The cell areas were defined by lift-off patterning of the back electrode followed by a dry etching of the silicon to access the front electrode, leading to cells with a nominal

## Appendix A. Passivated interfaces in fluorinated microcrystalline silicon thin film solar cells

area of  $0.25 \text{ cm}^2$ . For the measured  $J$ - $V$  curves, a dual-lamp sun simulator was used operating under standard conditions (AM1.5g,  $1000 \text{ W/m}^2$ ,  $25^\circ\text{C}$ ). From these measurements  $FF$  and  $V_{OC}$  are deduced, whereas the short-circuit current density ( $J_{SC}$ ) was calculated from external quantum efficiency (EQE) measurements performed with a white dielectric back reflector if not otherwise mentioned. This calculated  $J_{SC}$  was then used to determine the conversion efficiency ( $\eta$ ). For the Reflectance measurement a Perkin Elmer Lambda 900 Spectrometer was used.

### A.3 Results and discussion

Table A.1 shows the cell performance for two different absorber thicknesses (650 nm and 1300 nm) each in “standard” as well as in “passivated” cell design for several surface roughnesses. For the thin devices, recombination at the interface influences the  $V_{OC}$  more than the bulk defect density, such that the impact of implementing a passivation layer on  $V_{OC}$  is much stronger than for the thicker device. Each of the four experiments summarized in Table A.1 includes an additional variation of the substrate roughness. Note that even the roughest one has already been smoothed for 20 min. Consequently, the density of porous zones in the bulk is low for all studied cells, resulting in a small variation of  $V_{OC}$  and  $FF$  with treatment time. Nevertheless, the influence of surface roughness is still visible in the photocurrent, therefore, the roughest substrate leads to the best performance. We find a conversion efficiency of 8.2% for both absorber thicknesses because the thicker sample can compensate the losses in  $FF$  and  $V_{OC}$  by a higher  $J_{SC}$  due to better collection at long wavelength.

Table A.1 –  
Cell parameters of devices on different types of substrate with and without an 8.5 nm buffer layer.

Cell design	Absorber thickness [nm]	ZnO:B treatment time [min]	Cell performance			
			$V_{OC}$ [mV]	$FF$ [%]	$J_{SC}$ [mA/cm <sup>2</sup> ]	$\eta$ [%]
"standard"	650 nm	20 min (rough)	490	72.9	22.5	8.0
		45 min (average)	488	74.4	20.8	7.5
		90 min (smooth)	489	74.9	16.7	6.1
"passivated"	650 nm	20 min (rough)	510	74	21.8	8.2
		45 min (average)	511	74.0	19.4	7.3
		90 min (smooth)	500	74.0	17.8	6.6
"standard"	1300 nm	20 min (rough)	468	68.2	24.9	8.0
		45 min (average)	480	70.5	23.7	7.9
		90 min (smooth)	467	70.7	21.2	7.0
"passivated"	1300 nm	20 min (rough)	481	68.8	24.7	8.2
		45 min (average)	480	69.7	23.6	7.9
		90 min (smooth)	475	67.9	21.6	6.9

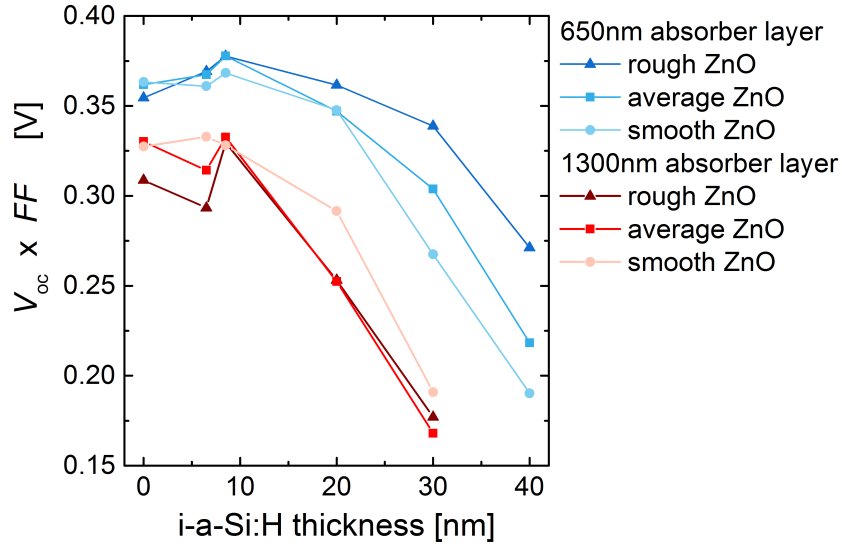


Figure A.2 – The change in  $V_{OC} \times FF$  as a function of the intrinsic buffer layer thickness, whereas the value at 0 nm represents the unpassivated “standard” cell design. For higher accuracy always the average of the 3 best cells per sample is compared [Stuckelberger 2015].

By increasing the thickness of the *a*-Si(i) buffer layer, the  $V_{OC}$  increases until it saturates at a certain thickness, indicating an optimum in surface passivation. The gain in  $V_{OC}$  coincides with a decreasing  $FF$ , therefore the  $V_{OC} \times FF$  product is introduced as a more significant parameter to assess the electrical performance of the solar cells. In Figure A.2, this quantity is plotted as a function of the intrinsic buffer layer thickness, whereas the value at 0 nm represents the unpassivated “standard” cell design with an n-layer containing oxygen. One can see a clear maximum at a layer thickness of 8.5 nm for both absorber thicknesses, less than half the thickness needed for cells of similar thickness grown from silane plasma [Hänni 2015].

The increase in  $V_{OC}$  for the passivated cell design goes along with a decrease in  $J_{SC}$  (Table A.1) due to a loss in generation between 450 nm and 650 nm, visible by the dip in the EQE spectra presented in Figure A.3. This reduced EQE is also present when measuring under reverse bias (−1V), which lets us assume that it is not due to collection problems. The reflectance ( $R$ ) of the cell, plotted in Figure A.3 as  $1-R$ , lets us rule out reflection losses as well. Further, the EQE was analyzed without back reflector (br). At short wavelengths, the onset of the “dip” in the passivated cell coincides exactly with the onset of transparency in the cell without back reflector, suggesting identical collection in the p-i region. Likewise, at long wavelengths the EQEs of the cell without back reflector are identical for front-and back-illumination, suggesting identical bulk collection. Therefore, we conclude that the “dip” is related to parasitic absorption in the n-buffer layer. In [Söderström 2012] a similar “dip” between 650 and 750 nm

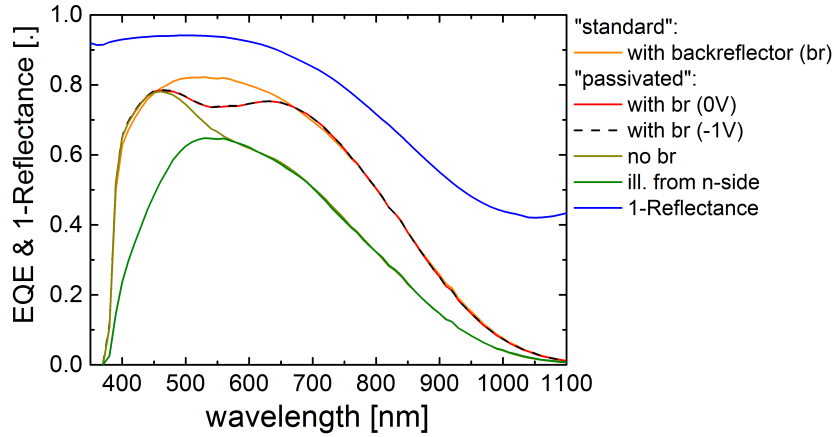


Figure A.3 – The EQE and 1–reflectance spectra of the thinner cell (650 nm) with a 8.5-nm-thick  $\alpha$ -Si(i)buffer layer, either measured with or without a white backreflector (br). When measuring under a reverse bias voltage of  $-1V$  (red, dashed) it is superimposed to the curve measured without voltage bias, indicating efficient collection. Additionally the cell was measured when illuminated from the n-side (green). For comparison the “standard” cell with same thickness is also plotted (orange) [Stuckelberger 2015].

was related to parasitic absorption in a layer of amorphous silicon at the back of the device. In our case, we attribute the occurrence at shorter wavelengths to the fact that our absorber layer is more crystalline and therefore more transparent in the visible range.

## A.4 Conclusion

In this study the importance of passivation of recombinative interfaces in highly crystalline thin-film Si solar cells is shown. We have demonstrated a strong increase in  $V_{OC}$  together with a high  $FF$  even for high superstrate roughnesses by implementing an amorphous buffer layer at the i-n interface of highly crystalline  $\mu c$ -Si:F thin film solar cells. We analyzed the reduced photocurrent due to parasitic absorption in the n-layer, which could be overcome by further optimization of the layer stack.

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# Publication list

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## Publications as first author in peer-reviewed journals

- **J. Stuckelberger**, G. Nogay, P. Wyss, A. Ingenito, C. Allebé, J. Horzel, B. Kamino, M. Despeisse, F. J. Haug, P. Löper and C. Ballif, "*Recombination Analysis of Phosphorous-Doped Nanostructured Silicon Oxide Passivating Electron Contacts for Silicon Solar Cells*", IEEE J. Photovoltaics **8**, 2, doi:10.1109/JPHOTOV.2017.2779871, (2018)
- I. Mack(\*), **J. Stuckelberger**(\*), P. Wyss, G. Nogay, Q. Jeangros, A. Ingenito, C. Allebé, J. Horzel, C. Allebé, M. Despeisse, F. J. Haug, P. Löper and C. Ballif, "*Properties of Mixed Phase Silicon Oxide Based Passivating Contacts with Enhanced Transparency for Silicon Solar Cells*", Solar Energy Materials and Solar Cells **181**, doi:10.1016/j.solmat.2017.12.030, (2018)
- **J. Stuckelberger**, G. Nogay, P. Wyss, Q. Jeangros, C. Allebé, F. Debot, X. Niquille, M. Ledinsky, A. Fejfar, M. Despeisse, F. J. Haug, P. Löper and C. Ballif, "*Passivating electron contact based on highly crystalline nanostructured silicon oxide layers for silicon solar cells*", Solar Energy Materials and Solar Cells **158**, doi:10.1016/j.solmat.2016.06.040, (2016)

## Publications as first author as conference proceedings

- **J. Stuckelberger**, G. Nogay, P. Wyss, M. Lehmann, C. Allebé, F. Debot, M. Ledinsky, A. Fejfar, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, "*Passivating contacts for silicon solar cells with 800 °C stability based on tunnel-oxide and highly crystalline thin silicon layer*", proceeding of the 43rd IEEE Photovoltaic Specialist Conference, Portland, United State of America, doi:10.1109/PVSC.2016.7750100, (2016)
- **J. Stuckelberger**, S. Hanni, B. Niesen, F.-J. Haug, C. Ballif "*Passivated interfaces in fluorinated microcrystalline silicon thin film solar cells*", proceeding of the 42rd

## Publication list

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IEEE Photovoltaic Specialist Conference, New Orleans, United State of America, [doi:10.1109/PVSC.2015.7356310](https://doi.org/10.1109/PVSC.2015.7356310), (2015)

## Conference presentations as first author

- **J. Stuckelberger**, P. Wyss, I. Mack, G. Nogay, Q. Jeangros, J. Horzel, C. Allebé, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, "*Phase-Separated SiO<sub>x</sub> Layers with Vertically Oriented Silicon Inclusions for Passivating Contacts in Silicon Solar Cells*", Oral presentation, E-MRS Spring Meeting, Strasbourg, France, (2017)
- **J. Stuckelberger**, G. Nogay, P. Wyss, Q. Jeangros, C. Allebé, J. Horzel, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, "*Recombination analysis of phosphorous-doped nanostructured silicon oxide passivating electron contacts for silicon solar cells*", Oral presentation, 26th International Photovoltaic Science & Engineering Conference, Singapore, (2016)
- **J. Stuckelberger**, G. Nogay, P. Wyss, X. Niquille, C. Allebé, F. Debrot, N. Roth, M. Ledinsky, A. Fejfar, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, "*Passivating electron contacts based on highly crystalline silicon layers for silicon solar cells*", Oral presentation, 6th Silicon PV, Chambéry, France, (2016)

## Patent

- P. Löper, **J. Stuckelberger**, C. Ballif, F.-J. Haug, P. Wyss, Patent Application PCT/EP2017/059194, (2017)

## Publications as co-author

- P. Wyss, **J. Stuckelberger**, G. Nogay, J. Quentin, I. Mack, X. Niquille, J. Horzel, C. Allebé, F. Debrot, M. Despeisse, F.-J. Haug, A. Ingenito, P. Löper, C. Ballif, "*Silicon-oxide mixed-phase interlayer fosters the thermal stability of poly-Silicon based passivating hole contacts for silicon solar cells*", manuscript in preparation, (2018)
- A. Ingenito, G. Nogay, **J. Stuckelberger**, P. Wyss, L. Gnocchi, C. Allebé, J. Horzel, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, "*Phosphorous-Doped Silicon Carbide as Front Side Passivating Contacts for Two-Sides Contacted Patterning Free c-Si Solar Cells*", Submitted to IEEE J. Photovoltaics, (2018)
- D. Mikulik, A.C. Meng, R. Berrazouane, P. Romero-Gomez, K. Tang, **J. Stuckelberger**, A. Fontcuberta i Morral, P. C. McIntyre "Surface Defect Passivation of Silicon Micro Pillars", Submitted to Adv. Materials Interfaces, (2018)
- G. Nogay, **J. Stuckelberger**, P. Wyss, E. Rucavado, C. Allebé, T. Koida, M. Morales-Masis, M. Despeisse, F. J. Haug, P. Löper and C. Ballif, "*Interplay of annealing temperature and*

*doping in hole selective rear contacts based on silicon-rich silicon-carbide thin films*", Solar Energy Materials and Solar Cells **173**, [doi:10.1016/j.solmat.2017.06.039](https://doi.org/10.1016/j.solmat.2017.06.039), (2017)

- G. Nogay, **J. Stuckelberger**, P. Wyss, Q. Jeangros, C. Allebé, X. Niquille, F. Debot, M. Despeisse, F. J. Haug, P. Löper and C. Ballif, "*silicon-rich Silicon Carbide Hole Selective Rear Contacts for Crystalline Silicon Based Solar Cells*", ACS Appl. Mater. Interfaces **8**, 51, [doi:10.1021/acsami.6b12714](https://doi.org/10.1021/acsami.6b12714), (2016)

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- G. Nogay, A. Ingenito, E. Rucavado, **J. Stuckelberger**, Q. Jeangros, P. Wyss, M. Morales-Masis, P. Löper, F.-J. Haug, C. Ballif, "*A Simple Process Flow for Silicon Solar Cells with Co-Annealing of Electron and Hole Selective Passivating Contacts*", Accepted as extended oral presentation, 7th World Conference on Photovoltaic Energy Conversion, Waikoloa, Hawaii, United State of America, (2018)
- G. Nogay, E. Rucovado, **J. Stuckelberger**, P. Wyss, Q. Jeangros, C. Allebé, J. Diaz, L. Ding, G. Christmann, S. Nicolay, M. Masis, M. Despeisse, P. Löper, A. Ingenito, F.-J. Haug, C. Ballif, "*SiCx Passivating Contacts for High Efficiency Silicon Solar Cells*", Oral presentation, 8th Silicon PV, Lausanne, Switzerland, (2018)
- A. Ingenito, P. Wyss, G. Nogay, Q. Jeangros, C. Allebé, S. Eswara, L. Korte, J. Horzel, **J. Stuckelberger**, M. Despeisse, F.-J. Haug, P. Löper and C. Ballif, "*Strategies for Integration of Passivating Contacts in Today's Manufacturing Processes*", Oral presentation, 8th Silicon PV, Lausanne, Switzerland, (2018)
- F.-J. Haug, P. Wyss, G. Nogay, **J. Stuckelberger**, A. Ingenito, I. Mack, C. Allebé, J. Horzel, M. Despeisse, P. Löper and C. Ballif, "*Passivating Contacts Based on Layers of Silicon-oxide and -carbide for c-Si Solar Cells*", Oral presentation, 27th International Photovoltaic Science & Engineering Conference, Kyoto, Japan, (2017)
- C. Allebé, A. Descoeudres, J. Horzel, A. Ingenito, G. Nogay, P. Wyss, **J. Stuckelberger**, P. Löper, F.-J. Haug, M. Despeisse, and C. Ballif, "*PECVD Layers for High and Low Temperature Improved Industrial Solar Cell Processes*", Oral presentation, 27th International Photovoltaic Science & Engineering Conference, Kyoto, Japan, (2017)
- A. Ingenito, G. Nogay, **J. Stuckelberger**, P. Wyss, C. Allebé, J. Horzel, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, "*Wide-band gap silicon carbide as front side carrier selective contact for silicon solar cells*", Oral presentation, 33rd European Photovoltaic Solar Energy Conference and Exhibition (EUPVSEC), Amsterdam, Netherlands, (2017)
- G. Nogay, M. Hyvl, M. Ledinsky, **J. Stuckelberger**, P. Wyss, Q. Jeangros, A. Ingenito, C. Allebé, M. Despeisse, A. Fejfar, F. J. Haug, P. Löper and C. Ballif, "*Locally Conductive Transport Channel Formation in High Temperature Stable Hole Selective silicon-rich*

## Publication list

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*Silicon Carbide Passivating Contact*", Oral presentation, 33rd European Photovoltaic Solar Energy Conference and Exhibition (EUPVSEC), Amsterdam, Netherlands, (2017)

- I. Mack, **J. Stuckelberger**, P. Wyss, G. Nogay, Q. Jeangros, J. Horzel, C. Allebé, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, "*Silicon Oxide/Silicon Layers as Passivating Contacts with Enhanced Transparency for High-Efficiency Silicon Solar Cells*", Oral presentation, Photovoltaic Technical Conference, Marseille, France, (2017)
- A. Ingenito, G. Nogay, P. Wyss, **J. Stuckelberger**, I. Mack, C. Allebé, J. Horzel, M. Despeisse, F. J. Haug, P. Löper and C. Ballif, "*Silicon-Oxide and Silicon-Carbide Layers as Passivating Contacts for Silicon Solar Cells*", Oral presentation, Workshop on Metallization of Crystalline Silicon Solar Cells, Konstanz, Germany, (2017)
- P. Löper, G. Nogay, P. Wyss, M. Hyvl, P. Procel, **J. Stuckelberger**, A. Ingenito, I. Mack, Q. Jeangros, M. Ledinsky, A. Fejfar, C. Allebé, J. Horzel, M. Despeisse, F. Crupi, F.-J. Haug, C. Ballif, "*Exploring silicon carbide- and silicon oxide-based layer stacks for passivating hole contacts for silicon solar cells*", Oral presentation, IEEE 44th Photovoltaic Specialist Conference , Washington DC, USA (2017)
- G. Nogay, **J. Stuckelberger**, P. Wyss, Q. Jeangros, C. Allebé, M. Despeisse, F. J. Haug, P. Löper and C. Ballif, "*Boron Doped silicon-rich Silicon Carbide for Passivating Rear Contacts*", Oral presentation, 7th Silicon PV, Freiburg, Germany, (2017)
- G. Nogay, P. Wyss, **J. Stuckelberger**, B.Paviet-salomon, A.Tomasi, C. Allebé (Presenter), J. Horzel, A. Ingenito, I. Mack, A. Descoeurdes, F.-J. Haug, P. Löper, M. Despeisse and C. Ballif, "*PECVD-based approaches for improved industrial solar cell processes.*", Oral presentation, NREL Workshop, Denver, USA, (2017)

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*Lausanne, July 2018*

Josua Stückelberger

# JOSUA STÜCKELBERGER

## Personal Data

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Birthday /-place  
Nationality

Allenmoosstrasse 66, 8057 Zurich  
28.11.1985 / Zürich, Switzerland  
Swiss



## Education

2014-2018  
  
  
  
2011-2013  
  
Master Thesis  
  
  
Semester Thesis  
  
  
  
2005-2011  
  
2005  
  
2004  
1998-2004

### PhD student with EPFL in Material Science

«Transparent Passivating Contacts for Front Side Application  
in Crystalline Silicon Solar Cells»  
*EPFL, Neuchâtel, CH*

### Msc ETHZ in Physics,

Majoring in: Solid state physics & Quantum electronics  
*ETH, Zurich, CH*

### «Effect of Sodium on Structural & Electronic Properties of Cu<sub>2</sub>ZnSn(S,Se)<sub>4</sub> Solar Cells»

Laboratory for Thin Films and Photovoltaics  
*Empa, Dübendorf, CH*

### «Investigation of a photoacoustic sensor based on a mid- infraredlight emitting diode»

Laser Spectroscopy and Sensing Lab  
*ETH, Zurich, CH*

### Bsc ETH in Physics,

*ETH, Zurich, CH*

### 2 Month language school (Advanced CAE)

*Cape Town, SA*

### Military training school

### Higher school certificate

Majoring in: Physics & Applied Mathematics  
*Kantonsschule Oerlikon, Zurich*

## Professional Activities

2013-2013  
  
  
  
2007-2013  
  
  
2006  
  
2005  
  
2002-2007

### Research associate

(Civil Service, Electricity consumption of building automation)  
*Lucerne University of Applied Sciences and Arts, Horw*

### Safety Officer

(control of handluggage & people, Screening)  
*Police of Canton Zurich, Zurich Airport*

### Safety Officer

*Custodio AG, Zurich Airport*

### Pizza courier

*Pizza Blitz, Zürich*

### Security und Stagehand

*Fortissimo AG, ZürichETH, Zurich*

## Language

German  
English  
French

Native Language  
highly proficient in spoken and written English  
good command in word and writing

## Skills

Computing  
Processing

OriginLab, Matlab, VBA, LaTeX, Adobe Illustrator  
PECVD, CVD, PVD,  
thermal treatments (<1000°C),  
chemical treatments (HF, HNO<sub>3</sub>, SC<sub>2</sub>, H<sub>3</sub>PO<sub>4</sub>),  
cleanroom experience

Characterizing

ECV, IV, EQE, R&T, SEM, EDX, XRD, Raman, Photoconductive  
Decay, FTIR, Ellipsometry

## Selected Publications

2018

Stuckelberger *et al.*, **Recombination Analysis of Phosphorus-Doped Nanostructured Silicon Oxide Passivating Electron Contacts for Silicon Solar Cells**, IEEE Journal of Photovoltaics  
[DOI: 10.1109/JPHOTOV.2017.2779871](https://doi.org/10.1109/JPHOTOV.2017.2779871)

2017

Nogay *et al.*, **Interplay of annealing temperature and doping in hole selective rear contacts based on silicon-rich silicon-carbide thin films**, Solar Energy Materials and Solar Cells  
[DOI: 10.1016/j.solmat.2017.06.039](https://doi.org/10.1016/j.solmat.2017.06.039)

2016

Stuckelberger *et al.*, **Passivating electron contact based on highly crystalline nanostructured silicon oxide layers for silicon solar cells**, Solar Energy Materials and Solar Cells  
[DOI: 10.1016/j.solmat.2016.06.040](https://doi.org/10.1016/j.solmat.2016.06.040)

2014

Sutter-Fella *et al.*, **Sodium Assisted Sintering of Chalcogenides and Its Application to Solution Processed Cu<sub>2</sub>ZnSn(S,Se) 4 Thin Film Solar Cells**, Chemistry of Materials  
[DOI: 10.1021/cm403504u](https://doi.org/10.1021/cm403504u)

more on Google scholar:

[goo.gl/Etnoka](https://goo.gl/Etnoka)

## Patents

2017

J.Stuckelberger *et al.* **Passivating contact and solar cell application thereof**  
[WO2017182472A1](https://patents.google.com/patent/WO2017182472A1)

## Oral presentations

2017

**Phase-Separated SiO<sub>x</sub> Layers with Vertically Oriented Silicon Inclusions For Passivating Contacts in Silicon Solar Cells**  
E-MRS Spring Meeting, Strasbourg, FR

2016

**Recombination Analysis of Phosphorus-Doped Nanostructured Silicon Oxide Passivating Electron Contacts for Silicon Solar Cells**

International PVSEC, Singapore

2016

**Passivating electron contacts based on highly crystalline silicon layers**

SiliconPV, Chambéry, FR

## Interests

Floorball (active member in club in Zürich)  
Volleyball (active member in club in Neuchâtel)  
Snowboard  
YMCA Group leader (10 years)  
Travelling through south-east asian countries

Neuchâtel, July 2018