Full-Area Passivating Contacts with High and Low Thermal Budgets: Solutions for High Efficiency c-Si Solar Cells

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Résumé

L'efficacité des cellules solaires industrielles à base de silicium cristallin est actuellement limitée par les pertes par recombinaison à l'interface métal/semiconducteur. Cette recombinaison de contact peut être minimisée en séparant le métal de la gaufrette de silicium cristallin en introduisant une couche tampon qui passive la surface de la gaufrette tout en permettant le transport sélectif d'un type de porteur de charge. De telles structures sont appelées contacts passivants sélectifs de porteurs. L'objectif principal de cette thèse est l'étude des contacts passivants sélectifs de porteurs fonctionnant avec des budgets thermiques faibles et élevés. Les contacts à faible budget thermique sont étudiés en utilisant une architecture de cellule solaire à base de silicium nommée hétérojonction (SHJ). Pour être pertinent d'un point de vue industriel, les contacts passivants à budget thermique élevé sont développés sur des gaufrettes de silicium de type-*p*.

Les contacts passivants sélectifs de porteurs en silicium microcristallin (μc-Si :H) adaptés à un budget thermique faible sont étudiés pour des cellules solaires de type SHJ. Il est démontré que, par rapport aux couches de silicium amorphes, les couches μc-Si :H améliorent les performances optiques et électriques des cellules solaires. Cependant, comme la cristallinité de couche augmente avec l'épaisseur, il existe un compromis entre la densité de courant de court-circuit et le facteur de forme. Ce compromis est évité en combinant un contact passivant sélectif aux trous fait d'oxyde de molybdène pour la partie frontale, avec un contact passivant sélectif aux électrons fait par dopage au phosphore μc-Si :H(*n*) à l'arrière. En appliquant une métallisation frontale en cuivre électro-déposé, une densité de courant de court-circuit de 38.9 mA/cm^2 et un facteur de forme de 80 % sont obtenus, se traduisant par une efficacité de 22.5 %.

Des contacts passivants sélectifs aux trous avec un budget thermique élevé sont développés en utilisant d'une couche d'oxyde chimique (SiO_x) et d'une couche de carbure de silicium dopée au bore qui est déposée dans des conditions riches en silicium [$SiC_x(p)$] par dépôt chimique en phase vapeur assisté par plasma. Il a été observé que l'introduction d'une couche intermédiaire Si(i) entre SiO_x et $SiC_x(p)$ est nécessaire afin de prévenir une réaction chimique entre les atomes de carbone et l'oxyde chimique. En utilisant cette structure, une valeur de tension de circuit ouvert implicite de 718 mV et une valeur de résistivité de contact spécifique de 17 mΩ cm^2 ont été obtenues. La structure de contact a été testée en réalisant des cellules solaires hybrides qui présentent un contact de trou arrière avec un budget thermique élevé et un contact d'électron frontal de type SHJ avec un budget thermique faible. Avec ce concept, le facteur de forme de 81.8 % est obtenu.

Afin d'améliorer d'avantage le contact sélectif aux trous, l'incorporation *in-situ* de fluor dans le contact dopé au bore [SiC_x:F(*p*)] est explorée. On observe que le fluor est réparti de manière uniforme dans la couche de SiC_x:F(*p*) après déposition. Lors du recuit, il diffuse vers la gaufrette de silicium et s'accumule à l'interface réduisant ainsi la densité de défauts. Avec l'ajout de fluor dans ce contact, de tensions en circuit ouvert implicite supérieures à 720 mV sont atteintes sans hydrogénation. Après hydrogénation, de tensions en circuit ouvert implicite jusqu'à 735 mV sont obtenues. Le potentiel de ce contact fluoré est également étudié en réalisant des cellules solaires composées de contacts passivants avec un budget thermique élevé. Pour cela, des couches sélectives aux électrons dopées *in-situ* au phosphore ont également été développées. Des cellules solaires planaires de type-*p* ont atteintes des valeurs impressionnantes de facteur de forme de 84 % et de tension en circuit ouvert de 727 mV. En s'adaptant au contact frontière pour les surfaces texturées, une efficacité de 22.6 % est obtenue.

Mots cléfs : cellules solaires au silicium cristallin, haute efficacité, PECVD, budget thermique, transport de porteur de charge, passivation de surface, silicium microcristallin, carbure de silicium riche en silicium, fluor.

Abstract

In recent years photovoltaics (PV) has been the fastest-growing energy source, mainly due to a tremendous drop of the system cost. Today more than 90 % of the global PV market is occupied by crystalline silicon (c-Si) solar cells, which are limited by recombination losses at the metal/semiconductor interface. This recombination path can be avoided by separating the metal from the c-Si wafer by introducing a buffer layer that electronically passivates the wafer surface while still allowing the flow of one type of carrier. Such structures are called carrier-selective passivating contacts. In the scope of this thesis, carrier-selective passivating contacts with low and high thermal budgets are investigated with the purpose of achieving a good understanding of the junction formation, working principle, limiting factors, and integration requirements. Silicon heterojunction (SHJ) solar cells are studied as representatives of solar cells processed with a low thermal budget. Solar cells with interfacial oxide and doped-silicon contacts are investigated as the concept for cells with high thermal budgets. To be industrially relevant, contact formation of the latter is studied with *p*-type wafers.

The carrier-selective passivating contacts based on microcrystalline silicon (μc-Si:H) are studied for SHJ solar cells with a low thermal budget. It is demonstrated that μc-Si:H layers improve the optical and electrical performance of the SHJ solar cells compared to cells with purely amorphous contacts. However, as the layer crystallinity increases with thickness, a trade–off between short-circuit current density and fill factor is encountered. By combining a molybdenum oxide front hole contact and a μc-Si:H(*n*) rear electron contact, this trade–off is avoided. Applying an electrodeposited copper front metallization, a short-circuit current density of 38.9 mA/cm^2 and a fill factor of up to 80 % are obtained leading to an efficiency of 22.5 %.

The passivating hole contacts with a high thermal budget are developed using a chemically grown thin oxide (SiO_x) and boron-doped silicon carbide ($SiC_x(p)$) that is deposited under Si-rich conditions by plasma-enhanced chemical vapour deposition. It is observed that introducing an undoped Si inter–layer between the SiO_x and $SiC_x(p)$ is necessary to prevent a chemical reaction between carbon atoms in the $SiC_x(p)$ and the adjacent SiO_x, and consequently to obtain a well-passivated SiO_x/c-Si interface. With this contact structure, an implied open-circuit voltage of 718 mV and a specific contact resistivity of 17 mΩ cm^2 are attained. The contact structure is tested at the device level by realizing proof-of-concept hybrid solar cells that feature a high-thermal-budget rear hole-selective contact and a low-thermal-budget SHJ front electron-selective contact. With this concept, a fill factor of 81.8 % is attained.

In an effort to improve the hole contact property further, *in-situ* incorporation of fluorine into

the boron-doped hole contact is explored. It is shown that, in the *as-deposited* state, fluorine is evenly distributed within the contact layer of SiC_x:F(*p*). Upon annealing, fluorine diffuses toward the c-Si wafer and accumulates at the interface where it reduces the defect states. With this contact structure, implied open-circuit voltage values above 720 mV are attained on *p*-type planar wafers before hydrogenation; this is improved to 735 mV with hydrogenation. The potential of the fluorinated hole contact is investigated at the device level by realizing both-sides-contacted co-processed solar cells with high-thermal-budget passivating contacts. For this purpose *in-situ* phosphorous-doped SiC_x(*n*) layers were developed as a front contact. Planar, both-sides-contacted *p*-type solar cells attain an impressive fill factor of 84 % and an open-circuit voltage of 727 mV. By adapting the front side to textured surfaces, conversion efficiencies of up to 22.6 % are achieved.

Keywords: crystalline silicon solar cells, high efficiency, PECVD, thermal budget, charge carrier transport, surface passivation, microcrystalline silicon, silicon rich silicon carbide, fluorine.

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List of abbreviations and symbols

Semiconductor Basics

n	Electron density
p	Hole density
n_i	Intrinsic carrier concentration
Δn	Excess electron density
Δp	Excess hole density
E_f	Fermi level
WF	Work function
FCA	Free carrier absorption
SCR	Space charge region
SRH	Shockley-Read-Hall
τ_{eff}	Effective minority carrier lifetime
S_{eff}	Effective surface recombination velocity
E_g	Bandgap energy
λ	Wavelength
k_B	Boltzmann constant

Materials

Ag	Silver
Al	Aluminum
a-Si:H	Hydrogenated amorphous silicon
a-Si:H(i)	Intrinsic hydrogenated amorphous silicon
a-Si:H(n)	n-type hydrogenated amorphous silicon
a-Si:H(p)	p-type hydrogenated amorphous silicon
μc-Si:H	Hydrogenated microcrystalline silicon
μc-Si:H(p)	p-type hydrogenated microcrystalline silicon
μc-Si:H(n)	n-type hydrogenated microcrystalline silicon
a-SiC_x	Amorphous silicon carbide
SiC_x(p)	p-type silicon carbide

$SiC_x(n)$	*n*-type silicon carbide
SiC_x:F(*p*)	*p*-type fluorinated silicon carbide
c-Si	Crystalline silicon
Cz	Czochralski
FZ	Float-Zone
SiN_x	Silicon nitride
SiO_x	Silicon oxide
Chem SiO_x	Chemical oxide
UV-O_3 SiO_x	Ultraviolet/ozone oxide
Therm SiO_x	Thermal oxide
TCO	Transparent conductive oxide
ZnO:B	Boron-doped zinc oxide
ZnO:Al	Aluminum-doped zinc oxide
ITO	Indium-tin-oxide
IWO	Tungsten-doped indium oxide
IO:H	Hydrogen-doped indium oxide
IO:Zr	Zirconium-doped indium oxide
MoO_x	Molybdenum oxide
ARC	Anti-reflective coating

Deposition Processes

PECVD	Plasma enhanced chemical vapor deposition
LPCVD	Low pressure chemical vapor deposition
PVD	Physical vapor deposition
RF	Radio frequency
VHF	Very high frequency
FGA	Forming gas annealing
CO_2	Carbon dioxide
D_2	Deuterium
H_2	Hydrogen
PH_3	Phosphine
TMB	Trimethylborane
BF_3	Boron trifluoride
SiH_4	Silane
CH_4	Methane
NH_3	Ammonia

Characterizations

FF	Fill factor
J_{sc}	Short-circuit current density

V_{oc}	Open-circuit voltage
η	Energy conversion efficiency
Suns V_{oc}	Quasi-steady-state open-circuit voltage
J-V	Current density–voltage
J	Current density
MPP	Maximum power point
R_s	Series resistance
R_{sh}	Shunt resistance
R_{sheet}	Sheet resistance
ρ_c	Specific contact resistivity
EQE	External quantum efficiency
IQE	Internal quantum efficiency
PLI	Photoluminence imaging
BSF	Back surface field
SE	Spectroscopic ellipsometery
RS	Raman spectroscopy
QSSPC	Quasi-steady-state photoconductance
TLM	Transfer length method
SEM	Scanning electron microscopy
TEM	Transmission electron microscopy
HR-TEM	High resolution transmission electron microscopy
STEM	Scanning transmission electron microscopy
HAADF	High-angle annular dark-field
EDX	Energy-dispersive X-ray spectroscopy
ECV	Electrochemical capacitance voltage
SIMS	Secondary-ion mass spectrometry
C-AFM	Conductive atomic force microscopy
GI-XRD	Grazing incident X-ray diffraction

Solar Cell Technologies

SHJ	Silicon heterojunction
PERC	Passivated emitter and rear cell
PERL	Passivated emitter and rear locally diffused cell
Poly-Si	Polycrystalline silicon
TOPCon	Tunnel oxide passivated contact
POLO	Polycrystalline silicon on oxide
PRC	Partial rear contact
IBC	Interdigitated back-contact

1 Introduction

This chapter first introduces a general context of *photovoltaics* (PV), gives an overview of different solar cell technologies and discusses their current market status. Following that, the fundamental operating principle of a solar cell is described together with the efficiency-limiting factors. In the final sections, the structure of this thesis and its main contributions to the research field of crystalline silicon solar cell technology are noted.

1.1 Photovoltaics as the ultimate solution for a clean future

Climate change, which is directly linked to the continuous increase in CO_2 emission, is one of the most important problems of mankind. Since anthropogenic emissions of CO_2 result mainly from the combustion of fossil fuels, energy consumption is placed at the center of the climate change debate. In 2017, 81 % of total global energy demand was met by fossil fuels such as coal, natural gas and oil whose creation took hundreds of millions of years in nature [IEA 2018]. This makes their use unsustainable, limited and also geologically accessible only in certain parts of the world. At the same time, the world energy demand is growing prominently: the International Energy Agency forecasts a 28 % rise in world energy consumption between 2015 and 2040, which is equivalent to adding another China and India on top of today's global demand [IEA 2017]. Under these circumstances, more sustainable and cleaner solutions are necessary.

In 2015, the United Nations Climate Change Conference in Paris agreed on a legally binding transition towards a low-carbon society. In the agreement, 194 states and the European Union officially recognized the need for a global response to climate change, and they committed to limit it. The goal of the agreement is to keep the rise in the global temperature in 2100 to less than 2 °C above pre-industrial levels and to pursue efforts that would limit the temperature increase to a more ambitious rise of only 1.5 °C. The Paris agreement defines the level of climate change that governments are willing to accept without interfering in economic development [Rogelj 2016]. This step has kicked off a transition towards clean energy production and has raised important possibilities for future renewable energy research and development. With

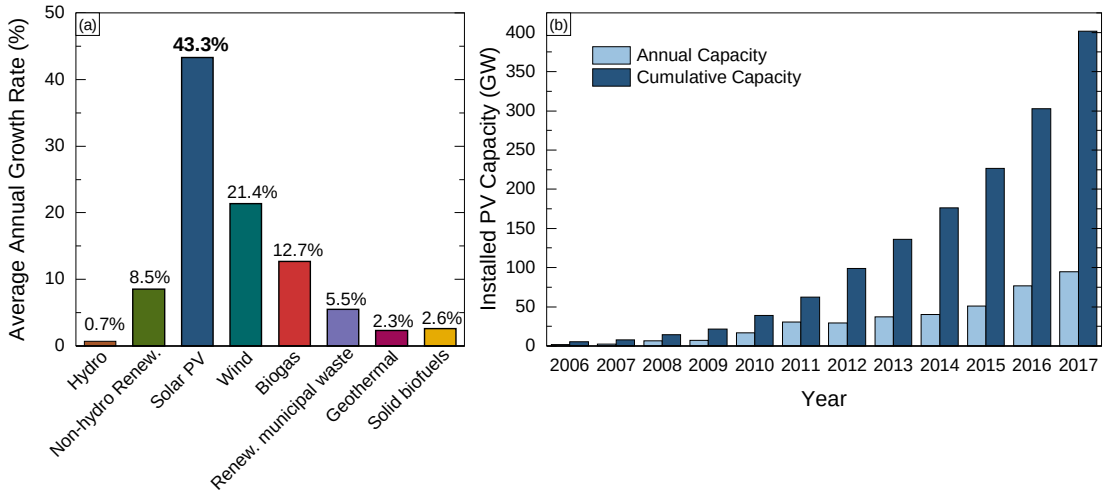

Figure 1.1 – (a) Average annual growth rates of electricity production from renewable energies between 1990 and 2016 in OECD countries. Data from [IEA 2017] (b) Global annual and cumulative installed PV capacity between 2006 and 2017. Source: GlobalData

this perception the research communities are challenged to develop new concepts with smart solutions to use the electricity wisely. Additionally, it puts a target on an individual basis to lower our energy consumption, and therefore to take part in building a sustainable and clean future for our planet.

In the member countries of Organization for Economic Cooperation and Development (OECD), the total primary energy supply from renewable sources increased from 272 million tonnes of oil equivalent (Mtoe) to 512 Mtoe from 1990 to 2016, representing an average annual growth rate of 2.5 %. Among the renewable energy sources PV energy has a great potential to supply large-scale energy demands all over the world. Particularly, the amount of energy arriving on earth from the sun is more than 30 times larger than the total reserve of coal and 10000 times larger the current energy consumption of humanity [Perez 2009]. Moreover, solar irradiation is natural, unlimited, free and abundant.

In recent years, PV energy experienced the highest growth rate since its cost is decreased drastically due to technological progress, strong market competition and better financing conditions. According to Swanson's learning curve, the PV production cost has been reduced by 24 % each time the cumulative production doubled over the last 36 years [Swanson 2006], [ITRPV 2017]. Today PV can produce electricity at costs in line with most of the conventional energy sources. As a consequence, electricity production from PV increased from 19 GWh in 1990 to 218283 GWh in 2016, achieving a 43.3 % annual growth rate, the fastest of all renewable electricity technologies [see Figure 1.1(a)]. In 2017, the global annual installed capacity of PV was 100 GW [see Figure 1.1(b)] with an average PV module price of < 0.4 €/Wp and it is projected to be between 400 and 600 GW in 2030. In Switzerland, Germany and Europe, 2.5, 6.9 and 3.4 %, respectively, of the total electricity was produced by PV in 2017. At this stage it is

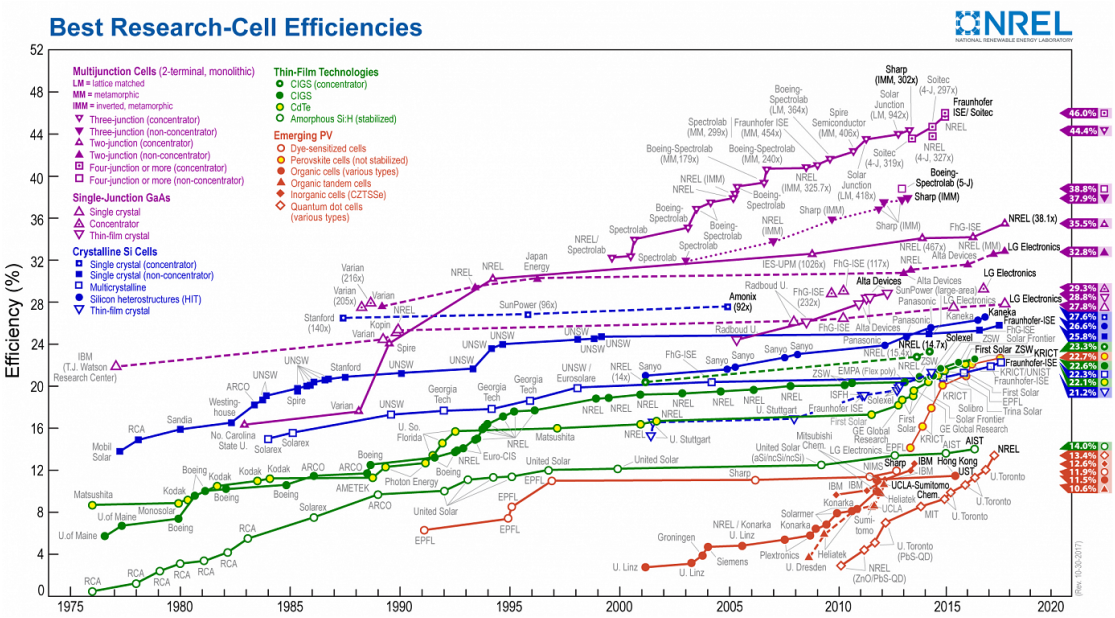

Figure 1.2 – Record-efficiency chart over the last 40 years for various photovoltaic technologies. This plot is courtesy of the National Renewable Energy Laboratory, Golden, CO, US [NREL 2017]

self-evident that PV technology has started to play a major role in global electricity production.

1.1.1 Overview of the different solar cell technologies

The history of PV started in 1839 when the French experimental physicist Edmond Becquerel discovered the photovoltaic effect, i.e. the direct conversion of light into electricity. Many years later, Albert Einstein postulated that the energy of light is carried by well-defined energy quanta, called photons. This finding led to the formulation of the wave function which explained the dissimilarities between different forms of solids such as metals, insulators and semiconductors. In metals, electrons are free, and therefore the electrical current flows readily. Insulators have a wide bandgap ($E_g > 2$ eV), i.e. an energy range where no electron states can exist, and the electronic states beyond the bandgap may have low mobility. Semiconductors also have a bandgap ($E_g \sim 0.5$–2 eV) and the current flow necessitates excitation of electrons across the bandgap. Depending on the extent of the bandgap, the energy from sunlight can be sufficient for excitation. Besides illumination, foreign atoms can also be incorporated to control the conductivity of semiconductors, making them very important materials for microelectronic and PV applications.

Figure 1.2 is the record efficiency chart of the National Renewable Energy Laboratory (NREL) which presents the progress in confirmed cell efficiencies fabricated using different technologies and materials over the last 40 years. The best conversion efficiency ever obtained for a PV device is 46 % with a four-junction solar cell based on III–V materials under 508 suns

concentration. Without concentration, similar cell structures demonstrated efficiencies of up to 38.8 %. However, their process complexity makes them extremely expensive and thus unsuitable for large-scale industrial applications. Up-to-date, notable efficiencies have been achieved with thin film CdTe and CIGS cells. Very recently, the PV research community showed enthusiastic interest in perovskite solar cells. As they exhibit a wide bandgap and high voltage, they are assumed to be a perfect candidate for the top cell of tandem devices with a crystalline silicon (c-Si) bottom cell. However, their high sensitivity to humidity and oxygen exposure is still a concern in terms of stability. Thus, it is important to note that the reported perovskite cell results represent initial efficiencies, without any information about the long-term stability, which is known to be a significant shortfall of this technology.

1.1.2 Today's market status

The market potential of PV depends strongly on the global price of electricity and on the production cost. The capital costs of PV systems consist of the module cost and the balance-of-system cost, which refers to all other components and services needed to make a PV system operational, such as the inverter, land usage, mounting structure, cabling costs etc. For many years the module represented the largest share of the system cost, but the situation has changed in the last years and now the balance-of-system cost accounts for more than half of the capital cost. In this case there are two pathways to continue reducing the cost per generated kWh: Up-scaled and thus more cost-effective module production or increased energy conversion efficiency at constant fabrication costs. Since the cost of PV installation is area-dependent (balance-of-system cost) and can be reduced by higher efficiencies, there is still a strong motivation to increase device efficiency to be able to further progress in cost reduction.

Due to their competitive cost, high efficiencies, well understood nature and long-term module-level reliability, single-junction c-Si and poly-Si technologies hold a dominant position in the global PV market. The best efficiency of 26.7 % has been obtained with back-contacted silicon heterojunction technology, followed by an efficiency of 25.8 % for cells with traditional contacting on both the front and rear sides. These results were obtained with high-quality *n*-type monocrystalline float-zone wafers. For a large-area *p*-type multicrystalline cell, an efficiency of 22 % has been confirmed using passivated emitter and rear cell (PERC) technology. As the focus of this thesis is crystalline silicon-based solar cells, more detailed information on the different technologies together with their advantages and disadvantages will be given below. Before doing so, some basic working principles are introduced and the efficiency-limiting factors are discussed for different technologies.

1.2 Fundamental operating principle of a solar cell

The working mechanism of solar cells depends on optical interactions (absorption and carrier generation), carrier dynamics (lifetime and recombination) and transport of charge carriers

(drift and diffusion). Generally two basic steps are distinguished:

- Generation of the electron-hole pair (photogeneration)
- Separation and collection of the generated electrons and holes

1.2.1 Photogeneration and charge separation

Generation of the electron-hole pair is strongly related to the energy of the incoming photon (E_{ph}) and the bandgap (E_g) value of the illuminated semiconductor. E_g of a semiconductor is defined as the difference between the highest energy level of the valance band (E_v) and the lowest energy level of the conduction band (E_c). When the energy of the incoming photon is higher than or equal to E_g, the photon can be absorbed, meaning that a valance electron from the valance band can be released and get excited to the conduction band; in the process it leaves behind a hole (positive charge). In the case of $E_{ph} > E_g$, the extra energy is released to the lattice as heat, which is called the thermalization process. If the photon energy is lower than E_g, it cannot be absorbed and it cannot generate electron-hole pairs. The photon absorption in the material is described by the wavelength-dependent absorption coefficient according to Lambert-Beer's law. The photogeneration process takes place efficiently in direct-bandgap materials (i.e. gallium arsenide) where the highest point of E_v is aligned with the lowest point of E_c in the momentum space of the electronic dispersion diagram. Whereas for the materials with an indirect bandgap (i.e. silicon), excitation of a valance electron requires both the energy provided by a photon and the momentum provided by a lattice vibration (phonon).

Under condition of thermal equilibrium, the intrinsic carrier density (n_i) in the semiconductor is defined as $n_i^2 = np$, where the densities of electrons (n) and holes (p) can be expressed as:

$$n = n_0 = N_c e^{\frac{E_f - E_c}{k_B T}} \qquad p = p_0 = N_v e^{\frac{E_v - E_f}{k_B T}} \tag{1.1}$$

Here, E_f is the Fermi energy, N_v and N_c are the effective densities of states in the valence band and in the conduction band, respectively, k_B is the Boltzmann constant, and T is the temperature of the semiconductor. Under illumination, following the photon absorption and photogeneration, the carrier densities are redefined with the injected excess-carrier concentrations $\Delta n = \Delta p$ as follows:

$$n = n_0 + \Delta n = N_c e^{\frac{E_{fn} - E_c}{k_B T}} \qquad p = p_0 + \Delta p = N_v e^{\frac{E_v - E_{fp}}{k_B T}} \tag{1.2}$$

$$n_i = \sqrt{N_c N_v} e^{\frac{E_v - E_c}{2 k_B T}} \tag{1.3}$$

$$np = n_i^2 e^{\frac{E_{fn}-E_{fp}}{k_B T}} \tag{1.4}$$

Here, E_{fn} and E_{fp} are the *quasi-Fermi levels* of electrons and holes. Since the illuminated case represents a non-equilibrium state, the concentrations of electrons and holes differ from their respective values in equilibrium. If the bands are regarded separately, the occupation of states in the conduction band can still be described by E_{fn} and E_{fp}, which are the electrochemical potential of electrons and holes, respectively. The free energy of the system is then defined by the splitting of the hole and electron *quasi-Fermi levels*, which corresponds to the maximum voltage that a solar cell can build up, i.e. its implied voltage (iV):

$$\frac{E_{fn}-E_{fp}}{q} = iV = \frac{k_B T}{q} ln\left(\frac{(n_0+\Delta n)(p_0+\Delta p)}{n_i^2}\right) \tag{1.5}$$

In reality, the implied voltage is further decreased by the recombination effects since they reduce the density of excess carriers. Finally, in order to separate and extract the photogenerated carriers, a driving force that propels electrons and holes to the contacts is necessary. In one dimension, diffusion and drift contribute to the current density of electrons (J_n) and holes (J_p), as follows:

$$J_n = +qD_n\frac{dn}{dx} - q\mu_n n\frac{d\varphi}{dx} = \mu_n n\frac{dE_{fn}}{dx} \tag{1.6}$$

$$J_p = -qD_p\frac{dp}{dx} - q\mu_p p\frac{d\varphi}{dx} = \mu_p p\frac{dE_{fp}}{dx} \tag{1.7}$$

Here, D_n and D_p are diffusion constants for electrons and holes, respectively, μ_n and μ_p indicate the respective mobilities and φ is the electrical potential. The first term includes the distribution function of the electron and hole concentration over the semiconductor (dn/dx or dp/dx). In the case of a non-uniform carrier density distribution, the gradient of the chemical potential leads to a current driven by diffusion. The second term includes the expression of $d\varphi/dx$ denoting the gradient of the electrical potential in the semiconductor which leads to the current driven by drift. The combination of these electrical potential and chemical potential gradients generates the abovementioned force that is necessary to obtain current flow. Both forces lead to a net force which is the gradient of the electrochemical potentials, also called *quasi-Fermi levels* as mentioned before. In case the *quasi-Fermi levels* vary with position — the derivative terms dE_{fn}/dx and dE_{fn}/dx are not equal to zero — a current flows inside the semiconductor and the overall current density is equal to sum of J_n

and J_p:

$$J_{Total} = J_n + J_p = \frac{\sigma_n}{q}\frac{dE_{fn}}{dx} + \frac{\sigma_p}{q}\frac{dE_{fp}}{dx} \tag{1.8}$$

1.2.2 Recombination mechanisms

Recombination is the opposite process of the charge-carrier generation which annihilates excess carriers by demoting the electrons to a lower energy level. The time interval between generation and recombination is characterized by the minority-carrier lifetime, which determines how long an electron can stay in the conduction band before recombining. The injection-dependent excess-carrier lifetime — called minority-carrier lifetime as well — is used to quantify the recombination losses in a solar cell and is expressed in terms of the ratio of a volumetric recombination rate (U) to the excess-carrier concentration (Δn). The ultimate effect of the recombination process is a limitation of the maximum voltage available from the device and thus a reduction of the cell efficiency. Therefore, a quantitative description of the recombination rate in the absorber — here silicon — as a function of the dopant density and the carrier injection level is important to predict the limitations for the solar cell performance. Recombination pathways can be classified into two basic categories: bulk-related and surface-related recombinations.

Bulk recombination

The bulk of the semiconductor is governed by three fundamental recombination pathways that influence the bulk lifetime: radiative band-to-band recombination, Auger recombination and Shockley-Read-Hall (SRH) recombination which can be also called defect or impurity recombination through states within the bandgap in the bulk. Among these, radiative and Auger recombination are intrinsic processes that cannot be prevented as they are inherent to the material, whereas SRH is classified as an extrinsic process as it is linked to the presence of defect states in the forbidden gap, caused by lattice defects or contaminants such as impurities or doping.

(i) Radiative band-to-band recombination : In radiative recombination (direct band-to-band transition), an excited electron recombines with a hole by the emission of a photon. The recombination rate (U_{rad}) is proportional to the density of holes times electrons and is expressed as:

$$U_{rad} = B(np - n_0 p_0) = B(np - n_i^2) \tag{1.9}$$

Here, B is the radiative recombination coefficient linked to the material, n and p are the

electron and hole concentrations, and n_0 and p_0 are the equilibrium concentrations. It can be seen that the key driver for recombination is the deviation between the actual carrier density and the equilibrium carrier density. Accordingly, the radiative lifetime of minority carriers is then given by:

$$\tau_{rad} = \frac{1}{B(n_0 + p_0) + B\Delta n} \tag{1.10}$$

For low-injection conditions ($\Delta n << p_0 + n_0$), the radiative lifetime of minority carriers is dominated by the doping concentration, thus τ_{rad} reduces with doping. Conversely in high-injection condition ($\Delta n >> p_0 + n_0$), the radiative lifetime of minority carriers is dominated by the excess-carrier density, thus τ_{rad} reduces with Δn.

However, owing to the indirect bandgap of silicon, radiative recombination requires the participation of a phonon to conserve momentum which reduces the probability. Hence, radiative recombination is not the dominant recombination mechanism in crystalline silicon solar cells which is reflected by the small B value around 4.7×10^{-15} $cm^{-3}s^{-1}$ at 300 K. Nevertheless, radiative recombination is useful for photoluminescence (PL) imaging since the luminescence intensity is a measure of the strength of other recombination mechanisms and thereby provides a powerful method for characterization.

(ii) Auger recombination : This intrinsic recombination is a three-body process in which the excess energy produced by the recombination of an electron and a hole is transferred to a free charge carrier that then thermalizes back to the band edge. As two electrons and one hole, or two holes and one electron take part in Auger recombination, the process scales with the square of the carrier concentration and thus becomes the predominant recombination mechanism at high excess-carrier densities or high doping concentrations. The Auger recombination rate and corresponding lifetime expression for n-type silicon are given by:

$$U_{Auger} = C_n(n^2 p - n_0^2 p_0) + C_p(np^2 - n_0 p_0^2) \tag{1.11}$$

$$\tau_{Auger,low} = \frac{1}{C_n N_D^2} \qquad \tau_{Auger,high} = \frac{1}{(C_n + C_p)\Delta n^2} \tag{1.12}$$

C_n and C_p are Auger coefficients. At low injection levels, the Auger-related minority-carrier lifetime (τ_{Auger}) strongly depends on the doping whereas at high injection levels, τ_{Auger} is proportional to the inverse square of the excess-carrier density.

In the literature this traditional Auger theory was found to be in good agreement with measured lifetimes of highly doped silicon. For lower dopant concentrations, however, the predicted lifetimes significantly exceed the measured lifetimes. Hangleiter and Hacker attributed this

deviation to Coulomb interactions of mobile charge carriers [Hangleiter 1990]. To account for Coulomb-enhanced Auger recombination, Altermatt proposed to multiply the Auger coefficients C_n and C_p with enhancement factors [Altermatt 2006]. More information can be found in the literature [Kerr 2002], [Richter 2012]. Overall, Auger recombination ultimately dominates the behaviour of high-voltage cells, such as heterojunction cells which will be explained more elaborately in the following sections.

(iii) Shockley-Read-Hall recombination : SRH recombination occurs via electronic defect states within the bandgap — the forbidden gap — of the semiconductor, which might be introduced by impurities, doping or lattice defects, such as vacancies or dislocations.

In general, the defect states are classified into two categories according to their positions (E_t) within the bandgap. The defect states close to the conduction (or valance) band edge can capture an electron (or a hole), but there is a high probability that the captured charge will be thermally emitted back to the conduction (or valance) band rather than being annihilated by recombination. These states are referred to as trap states. If the defect energy level is closer to the middle of the energy gap, the occupation probabilities with electrons and holes becomes similar. Since both electrons and holes can be captured, such states behave as recombination centers which are detrimental to cell performance. A statistical model to calculate the recombination rate of a single defect level was presented by Shockley and Read [Shockley 1952], and independently by Hall [Hall 1952]:

$$U_{SRH} = \frac{\upsilon_{th} N_t (np - n_i^2)}{\frac{1}{\sigma_p}(n + n_1) + \frac{1}{\sigma_n}(p + p_1)} \tag{1.13}$$

$$n_1 = n_i e^{\frac{E_t - E_i}{k_B T}} \qquad p_1 = n_i e^{\frac{E_i - E_t}{k_B T}} \tag{1.14}$$

Here, υ_{th} is the thermal velocity of the charge carriers, N_t is trap density, σ_n and σ_p are capture cross sections that define the probability that the defect state captures an electron or a hole, E_i is the intrinsic energy level and E_t is energy level for defect states. Assuming charge neutrality ($\Delta n = \Delta p$), the related lifetime can be expressed as follows:

$$\tau_{SRH} = \frac{\frac{1}{\sigma_p}(n_0 + n_1 + \Delta n) + \frac{1}{\sigma_n}(p_0 + p_1 + \Delta p)}{\upsilon_{th} N_t (p_0 + n_0 + \Delta n)} \tag{1.15}$$

At high injection levels ($\Delta n = \Delta p >> n_0$ and p_0), the related minority-carrier lifetime does no longer depends on the energy level of the defect states nor on the doping concentration:

$$\tau_{SRH,high} = \frac{1}{\sigma_n \upsilon_{th} N_t} + \frac{1}{\sigma_p \upsilon_{th} N_t} = \tau_{n0} + \tau_{p0} \tag{1.16}$$

Whereas at low injection levels ($\Delta n = \Delta p << n_0$ and p_0) for an n-type semiconductor where $n \sim N_D$, the lifetime is expressed as follows:

$$\tau_{SRH,low} = \frac{1}{\sigma_n v_{th} N_t}\left(\frac{p_1}{N_D}\right) + \frac{1}{\sigma_p v_{th} N_t}\left(1 + \frac{n_1}{N_D}\right) \tag{1.17}$$

Thus, the SRH minority-carrier lifetime depends on the doping concentration, properties of the defect states such as the capture cross section and the energy level. Especially under illumination, the SRH recombination mechanism becomes dominant for solar cells if they are produced from defective material such as Czochralski-grown or multicrystalline silicon wafers. Contrary to intrinsic radiative and Auger recombinations, extrinsic SRH bulk recombination can be avoided with high-purity materials such as float-zone monocrystalline silicon wafers.

The inverse minority-carrier bulk lifetime (τ_{Bulk}) (recombination rate) can be written as the sum of all inverse bulk lifetimes; radiative lifetime ($\tau_{Radiative}$), Auger lifetime (τ_{Auger}), Shockley-Read-Hall lifetime (τ_{SRH}):

$$\frac{1}{\tau_{Bulk}} = \frac{1}{\tau_{Radiative}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \tag{1.18}$$

Thus, τ_{Bulk} depends on the three recombination processes explained above and it is dominated by the shortest lifetime value.

Surface recombination

The surface of a crystalline semiconductor commonly has some interruptions of the crystal lattice periodicity, i.e. dangling bonds — unpaired outer-shell electrons. These interruptions cause localized electronic defect states in the bandgap which act as recombination centers, also referred as interface defect states. Even though surface recombination is classified separately, it can be treated as a special case of SRH recombination. Different from the bulk SRH recombination, surface-related defect states do not occupy a single energy level but rather form a set of defect states distributed across the bandgap. Since surface recombination occurs via defect states that capture both electrons and holes, it is described by SRH theory in analogy to defect recombination in the bulk. The surface recombination rate per unit area and time, U_s ($\mathrm{cm^{-3}\ s^{-1}}$), is defined as:

$$U_s = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_p} + \frac{p_s + p_1}{S_n}} \tag{1.19}$$

$$S_n = \sigma_n v_{th} N_{it} \qquad S_p = \sigma_p v_{th} N_{it} \tag{1.20}$$

Here, n_s and p_s are the surface concentrations of the electrons and holes, respectively. S_n and S_p are the surface recombination velocities of the electrons and holes. N_{it} is the surface — interface — defect density. As the wafer surface holds a large number of defect states at various energy levels, N_{it} is reformulated by an energy-dependent interface defect density (D_{it}) with a relation of $N_{it} = \int_{E_v}^{E_c} D_{it}(E)dE$, thus the capture cross sections become energy dependent as well.

$$U_s = v_{th}(n_s p_s - n_i^2) \int_{E_v}^{E_c} \frac{D_{it}(E)dE}{\frac{n_s+n_1(E)}{\sigma_p(E)} + \frac{p_s+p_1(E)}{\sigma_n(E)}} \tag{1.21}$$

In order to account for band bending in the vicinity of the surface , i.e. due to a surface charge, the concept of an effective surface recombination velocity (S_{eff}) was introduced; in this case the excess-carrier density is taken at the edge of the space charge region where the bands are still flat [Aberle 2000]. S_{eff} can be described as the ratio of the surface recombination rate U_s and the excess-carrier density at a distance d from the surface where the flat band condition holds:

$$S_{eff} = \frac{U_{s,x=d}}{\Delta n_{x=d}} \tag{1.22}$$

S_{eff} typically ranges from 10^7 cm/s for a direct metal/silicon contact to below 10 cm/s for a passivated surface. As the annihilation of excess carriers by surface recombination is very efficient, it is one of the most important recombination mechanisms for crystalline silicon solar cells. Therefore, it is crucial to mitigate its contribution. To that end different approaches can be followed :

- Minimize the interface defect density (D_{it}) and therefore recombination sites. This mechanism is referred to as *chemical passivation* and it is achieved by saturating the silicon dangling bonds at the surface which can be done with various layers such as silicon dioxide (SiO_2), hydrogenated amorphous silicon (a-Si:H), etc. Additional dangling bonds may often be passivated by hydrogen atoms as well, sourced either from within the passivating overlayer itself or externally via annealing in a hydrogen mixture. As mentioned above, the surface recombination rate is directly proportional to the interface defect density, which is approximately on the order of 10^{13} cm^{-2} for non-passivated crystalline silicon [Aberle 2000]. According to the literature it is possible to obtain interface defect densities as low as 10^9 cm^{-2} with the growth of a high-quality thermal SiO_2 and subsequent annealing in a hydrogen atmosphere [Jin 2007]. Pankove *et al.* proposed to cover the surface with low-temperature-grown intrinsic a-Si:H for passivation purposes in 1979 [Pankove 1979]. Today a-Si:H yields a quasi-perfect electronic passivation with defect densities as low as 10^7 cm^{-2}.
- Alternatively, the defect density might stay constant, but the recombination rate can

be reduced by decreasing the minority-carrier density at the surface by band bending underneath the surface. This mechanism is called *charge-assisted passivation*. In this case, the absence of one charge-carrier species limits the recombination event of the electron-hole pair. The band bending can be attained either by introducing diffused or induced junctions or by the presence of recombination-inactive fixed charges, Q_f, near the interface. The most commonly used passivation layers working according to this principle are thermally grown silicon oxide (SiO_x) [Kerr 2002] and plasma enhanced chemical vapor deposition (PECVD) based silicon nitride (SiN_x) [Hezel 1981], [Leguijt 1994] which both exhibit fixed positive charges. Thus, they can be employed to passivate *n*-type surfaces by repelling the minority carriers — in this case holes — away from the interface. In 2001, Schmidt *et al.* proposed a SiO_x/SiN_x stack structure as a passivation layer, and reported that this stack structure showed high passivation quality and better thermal stability compared to single SiN_x layer passivation [Schmidt 2001]. Another important layer that can provide efficient surface passivation is aluminum oxide (Al_2O_3) [Hoex 2008]. However, a post-deposition annealing at moderate temperatures (~ 425 °C) is necessary to activate the passivation properties. It has been demonstrated that the annealing step drastically increases the fixed negative charge density in the layer and decreases the interface defect state density in parallel. Owing to the very high density of negative fixed charges, Al_2O_3 can provide high-quality *charge-assisted passivation* for *p*-type surfaces [Dingemans 2009], [Dingemans 2010].

After an insight into how to minimize surface recombination, finally by combining all the recombination parameters presented above, the effective minority-carrier lifetime can be expressed as follows:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Bulk}} + \frac{2S_{eff}}{W} \tag{1.23}$$

Here, W is the wafer thickness. As a symmetric sample structure was assumed, the surface-related term S_{eff}/W is multiplied by the factor of 2. Today well optimized bulk material is industrially available for crystalline solar cells. Because of that and the actual trend towards thinner solar cells, surface passivation is getting more research attention.

1.2.3 Diode equation and *J-V* parameters

Following electron-hole pair generation, net current flow is generally created by introducing a semi-permeable contacts that selectively collect one type of photogenerated carrier while blocking the other type [Wurfel 2009]. In c-Si solar cells, a typical way to achieve this is applying different doping to the front and the rear surfaces. By doing so, the *p*-side will have a higher conductivity for holes than for electrons, which consequently establishes a selective hole contact, and the inverse in the case for the selective electron contact [Wurfel 2015]. Since the wafer is generally doped with one type, this yields necessarily a *p-n* junction. Under

illumination, the ideal *J-V* characteristic is typically described by a superposition of the photogenerated current (J_L) and the recombination current in the opposite direction resulting in the well-known one-diode model:

$$J(V) = J_L - J_0\left(e^{\frac{qV}{nk_BT}} - 1\right) \tag{1.24}$$

Here, J_0 is the saturation current density that reflects the recombination and n is the diode ideality factor which is equal to 1 for the diffusion currents in an ideal *p-n* junction. There are two special modes of operation, namely short-circuit (SC) and open-circuit (OC) conditions. In the short-circuit condition, the excess carries travel from one contact to another via the external load without confronting any resistance. As excess carriers do not stay in the device, no *quasi-Fermi level* splitting occurs, consequently no voltage is generated. In this condition ($J_{(V=0)} \approx J_{sc} \approx J_L$), the device delivers its maximum current which is called the short-circuit current density (J_{sc}). In the open-circuit condition, no excess carriers are extracted from the device, and therefore it delivers its maximum voltage which is called the open-circuit voltage (V_{oc}). The ideal diode characteristics can be rearranged as follows:

$$V_{oc} = \frac{nk_BT}{q} ln\left(\frac{J_{sc}}{J_0} + 1\right) \tag{1.25}$$

As the one-diode model neglects recombination in the depletion region of the junction, the two-diode model is frequently used to describe deviations from the ideal behaviour. The two-diode model is simply the equivalent circuit of the basic solar cell but modified to include a second diode with a different diode quality factor, as well as the impact of series and parallel resistances:

$$J(V) = J_L - J_{01}\left(e^{\frac{qV-J(V)R_s}{n_1k_BT}} - 1\right) - J_{02}\left(e^{\frac{qV-J(V)R_s}{n_2k_BT}} - 1\right) - \frac{V - J(V)R_s}{R_{sh}} \tag{1.26}$$

The first diode with an ideality factor of n_1 and a saturation current of J_{01} is linked to the band-to-band recombination which dominates the regime of higher voltages and thus open-circuit conditions. Therefore, it affects mainly the V_{oc} of the cell. Typically, n_1 is close to 1. The second diode with an ideality factor of n_2 and a saturation current of J_{02} is linked to recombination in the depletion region — space charge region — which dominates at lower voltages and thus near maximum power point conditions. Therefore, it affects mainly the operating conditions of the cell. The ideality factor of the recombination processes should be equal to 2, but in reality n_2 is often found to be larger than 2. In addition to the second diode, resistive losses are also introduced in Equation 1.26. R_s and R_{sh} are the series and shunt resistances, respectively. The series resistance denotes the electrical resistance of a solar cell that includes the different contributions from the metallic contact grids, bulk resistance of the c-Si wafer, and contact resistances. The shunt resistance denotes the carrier paths other than those injected by the

p-n junction, also called leakage currents [McIntosh 2001].

Overall, the superposition of opposing currents does not accurately reflect the real charge-carrier transport in a solar cell, as it cannot be applied to some cases such as large series resistance and high-injection conditions. Nevertheless, the basic one-diode model and the extended two-diode model are useful to model the *J-V* characteristics of solar cells and to improve the understanding of the limiting parameters. In general the performance of a solar cell is determined with four main parameters that are extracted from the diode equation. Two of them, V_{oc} and J_{sc}, were already briefly mentioned above. Here a summary of their function and dependency is given:

- **The short-circuit current density (J_{sc})** is the maximum current that the solar cell can deliver when it is short circuited and the entire current is extracted. It is determined mainly by the spectrum of the incident light and the optical properties (i.e. absorption and reflection) of the solar cell. In the ideal case — considering only spectral mismatch losses without any recombination — the maximum achievable J_{sc} with c-Si solar cells is determined to be around 43.3 mA/cm^2 for a 110-μm-thick c-Si wafer [Richter 2013]. For thicker c-Si wafers, the maximum achievable J_{sc} is higher due to the increased photon absorption.

- **The open-circuit voltage (V_{oc})** is the maximum voltage that the solar cell can deliver at open circuit without current flowing through the external circuit. The direct relation of the V_{oc} with the saturation current density (J_0) and photogenerated current density (J_L) was given in Equation 1.25. As J_L typically has small variations, V_{oc} is mostly determined by J_0, consequently by the intrinsic and extrinsic recombination mechanisms that reduce the achievable excess-carrier density. Therefore, to be able to reach high V_{oc} values, recombination in the solar cell should be as small as possible. Assuming an ideal case, a theoretical V_{oc} limit was determined to be 761 mV for a 110-μm-thick c-Si wafer [Richter 2013]. With thinner wafers, higher V_{oc} values could be obtained, due to the lower bulk recombination and more efficient electron-hole pair extraction, provided that the surfaces are well passivated and the current density is not compromised.

- **The fill factor (*FF*)** is the ratio between the maximum power generated by a solar cell and the product of the V_{oc} and J_{sc} as given in Equation 1.27. It describes the "squareness" of the *J-V* curve and reflects charge-carrier transport and recombination losses under operating conditions. However, note that the *FF* can depend on many internal mechanisms of a solar cell and it is a challenge to define direct correlations. In this thesis, rather than maximizing the efficiency, understanding and minimizing transport- and recombination-related losses are the major concerns. Accordingly, the *FF* is in the center of interest of this work.

$$FF = \frac{V_{mpp} \cdot J_{mpp}}{V_{oc} \cdot J_{sc}} \tag{1.27}$$

Nevertheless, under the assumption that the solar cell is an ideal diode, it is possible to determine the *FF* as a function of V_{oc} as follows [Green 1981]:

$$FF = \frac{v_{oc} - ln(v_{oc} + 0.72)}{v_{oc} + 1} \qquad v_{oc} = V_{oc}\frac{q}{k_B T} \tag{1.28}$$

- **The conversion efficiency (η)** is the ratio of the output power at maximum power point and the incident power of the light (P_{in} which is equal to 1000 W/m^2). The efficiency is the most important output parameter of a solar cell since it quantifies the maximum electrical energy that can be generated under a given illumination:

$$\eta = \frac{V_{oc} \cdot J_{sc} \cdot FF}{P_{in}} \tag{1.29}$$

The performance of solar cells is defined by the combination of V_{oc}, *FF* and J_{sc}. However, it is important to note than there is often a trade–off between them and in many cases maximizing one comes at the expense of lowering one or even both of the others.

1.2.4 Shockly-Queisser-limit for single-junction c-Si solar cells

In 1961, Shockley and Queisser calculated the theoretical efficiency limit that can be attained with a c-Si solar cell based on a semiconductor with given bandgap energy [Shockley 1961]. They considered a detailed thermodynamic balance between incident and generated power density assuming radiative recombination as the only recombination mechanism. With this assessment the theoretical limit was determined as 30 % at the temperature of 300 °K for the spectrum of a 6000 °K blackbody [Shockley 1961] and 33 % for a spectrum of AM1.5 (one-sun illumination) [Swanson 2005]. However as c-Si has an indirect bandgap, radiative recombination is clearly not the predominant mechanism. Instead, there are considerable non-radiative intrinsic losses originating from Auger recombination. By assuming an ideal absorber and taking into account the non-radiative losses, Tiedje *et al.* determined the efficiency limit to be 29.8 % for a 100-μm-thick c-Si wafer [Tiedje 1984]. They also pointed out that even at one-sun illumination the dominant intrinsic loss mechanism for c-Si solar cells is Auger recombination. More recently by following the narrow-base approximation that assumes constant *quasi-Fermi-level* splitting so as the recombination rate throughout the cell — valid only if the minority-carrier diffusion length is longer than the wafer thickness — and using a revised Auger parametrization, Richter *et al.* reassessed the theoretical efficiency limit to be 29.4 % for a 110-μm-thick undoped c-Si wafer [Richter 2013]. The other calculated output parameters of the ideal cell under one-sun illumination are as follows: V_{oc} of 761.3 mV, J_{sc} of 43.3 mA/cm^2 and *FF* of 89.3 %.

1.3 Conventional solar cells and efficiency limitations

The current PV market is dominated by so-called aluminum back surface field (Al-BSF) *p*-type c-Si solar cell with diffused homojunctions, reaching a share above 70 % due to its simple fabrication [Glunz 2012]. In this section, the detailed process flow, structure and efficiency limitations of this industrial c-Si solar cell technology are discussed.

A typical Al-BSF cell scheme is depicted in Figure 1.3(a). The process sequence starts with wet chemical texturing to maximize light coupling and cleaning of either a multicrystalline silicon (mc-Si) *p*-type wafer — market share of 60 % — or monocrystalline silicon (mono-Si) *p*-type wafer — market share of 35 % — [ITRPV 2018]. This step is followed by diffusion of the *n*-type front contact in an atmosphere of phosphorus oxychloride ($POCl_3$) to create a *p*-*n* junction. The front sheet resistance after the phosphourous diffusion is usually in the range of 60 to 100 Ω/□ [Schultz 2008]. The annealing for the $POCl_3$ diffusion also causes impurity gettering and bulk lifetime enhancement which is especially important for mc-Si wafers as they manifest higher impurity levels accumulated at the grain boundaries with respect to mono-Si. After the removal of the phosphorus glass grown during the $POCl_3$ diffusion and the etching of the diffused layer on the wafer edges, a ~ 75-nm-thick PECVD-based anti–reflection–coating (ARC) layer — SiN_x — is applied to the front side to minimize front reflection. Following that the front- and rear-metallization are carried out by screen–printing pastes, employing silver (Ag) for the front metallic grid and Aluminum (Al) for the rear side. During a subsequent thermal treatment step at 850 °C for a few seconds (so-called firing), the Ag paste sinters through the ARC and makes contact to the *n*-type doped region. At the same time, the Al paste at the rear melts and forms a rear–reflector. A part of the Al mixes with the silicon to form a eutectic liquid. Upon cooling, the silicon solidifies incorporating the saturation concentration of aluminum. This yields a heavily aluminum-doped *p*-type region at the rear of the wafer, the so-called aluminum back surface field (Al-BSF) which also gives its name to the cell architecture. Additionally, during the firing process hydrogen is released from the SiN_x and diffuses through the silicon wafer, improving its bulk properties further by passivating electrical defects.

The heavily doped regions of the emitter and of the BSF are beneficial for the V_{oc} of the solar cell as they partially inhibit the recombination of minority charge carriers at the highly defective metal/semiconductor interfaces. However, increasing doping concentrations in those regions creates a trade–off as an intensive doping level also introduces excessive Auger recombination. Additionally, it leads to bandgap narrowing which increases the intrinsic carrier concentration in the highly doped regions and thus reduces the maximum obtainable splitting of the *quasi-Fermi levels* [Slotboom 1976]. The issue can be mitigated to some extent by introducing a selective-emitter design at the front side of the Al-BSF cells. In this design, the dopant density is kept low across the non-metallized regions to minimize Auger recombination of the passivated surface, but it is increased under the metal contacts in order to ensure low contact resistivity.

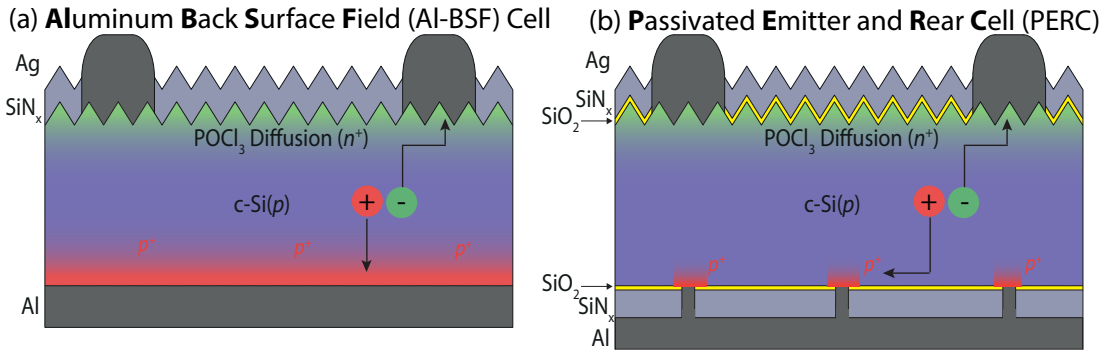

Figure 1.3 – Schematic cross section of a typical (a) aluminum-diffused back-surface-field c-Si solar cell and (b) passivated emitter and rear cell. Adapted from [De Wolf 2012a]

The process of the diffused junction cells is simple, robust and low cost; however, the cell efficiencies are strongly limited by the high minority-carrier recombination at the metal/semiconductor interfaces, resulting in fairly low V_{oc} values of ca. 640–645 mV and *FF* values in the range of 80 to 81 %. With J_{sc} values between 38–38.5 mA/cm^2, an ultimate efficiency limit of ca. 20 % can be projected for Al-BSF solar cells. As the low efficiency limit brings along the necessity of larger area integration, the advantage of low production costs is then lost because of the additional system integration cost. To overcome this shortfall, recently the PV industry has started directing its attention to other approaches that yield efficiency improvements with minimum changes to the existing production lines of this mainstream technology. In that way, the production costs would not be impacted significantly.

1.4 Strategies to overcome the limitations

As the main limitation of industrial solar cells originates from the metal/absorber interface, it needs to be carefully designed to avoid excessively large recombination losses. There are two different pathways to mitigate the minority-carrier recombination at this interface:

I. Reducing the metal contact area: One approach is to use local point contacts for carrier collection on the rear side instead of a full-area metallization. For this purpose, Blakers *et al.* proposed the concept of the PERC [Blakers 1986] which is illustrated in Figure 1.3(b), and demonstrated a conversion efficiency of 22.8 %. Contrary to an Al-BSF, the rear side of PERC cells employs a locally opened passivation layer reducing the highly defective metal-absorber interface area and consequently the related recombination rate. In the design of Blakers *et al.*, the local rear passivation is provided by a thermally grown passivating oxide while the local openings are defined by photolithography. Back then, the industry was reluctant to adopt the concept and instead ramped up the Al-BSF process with low-cost, *p*-type multicrystalline wafers.

The concept of localized contacts was further improved by minimizing Auger recombination

associated with high doping concentrations. This was achieved by restricting the doping at the rear of the wafer to the small areas underneath the contacts, resulting in the passivated emitter, rear locally diffused (PERL) cell which reached an efficiency of 25 % in 1999 [Zhao 1999]. However, localizing the diffusion and aligning it with the contact areas makes the process rather complicated. Additionally, several advanced techniques such as inverted pyramids [Blakers 1986], electrodeposited front contacts and a double ARC [Green 1990] [Zhao 1998] were employed. Thus the process complexity of this design is a main obstacle that limits its compatibility with an industrial mass production line. Furthermore, the concept of localized contact areas still ultimately limits the cell efficiency by recombination as evidenced by the V_{oc} value of 706 mV in the PERL cell.

Recently more and more manufacturers started to adapt the PERC concept to the requirements of mass production to push the conversion efficiency of commercial solar cells. To that end, the device design of Blakers *et al.* is modified by replacing the thermal SiO_2 rear passivating layer with Al_2O_3 and a SiN_x capping layer which is necessary to protect the Al_2O_3 during the local contact formation at the rear by a laser firing [Benick 2011]. Thanks to the high throughput of the laser-opening process and tailored aluminum screen-printing pastes, the PERC concept became a viable option for industry. The forecasts predict that it will replace the mainstream concept within the coming years; in 2018, 45 % of the total installation is expected to be in the PERC design. The industrial charm of PERC lies in a merely evolutionary upgrade of existing production lines, hence offering a low cost-of-ownership solution.

Today the industrial PERC cells exhibit conversion efficiencies in the range of 21 % in mass production which leads to ca. 1–1.2 % of absolute efficiency gain with respect to Al-BSF (both on mono-Si) [ITRPV 2018]. In February 2018, a conversion efficiency of 23.6 % was demonstrated with industrial *p*-type large-area mono PERC cells [LONGi 2018]; however, the other parameters of this cell are still not known. Indeed, the V_{oc} limitation of Al-BSF cells may be improved from typically 640 to 670 mV with the PERC concept. However, the V_{oc} values far above 700 mV in the current world-record devices suggest that it will ultimately remain as a limiting factor also for PERC concept. Additionally, the conversion efficiency of the PERC architecture is inherently limited by the two-dimensional charge-carrier flow defined by the geometry of the patterned rear contact as well as a trade–off between minimized recombination and series resistance due to the fact that a reduced contact area fraction also leads to increased series resistance.

II. Implementation of a passivating contact: An alternative approach is to introduce a layer stack system between the c-Si and the metal electrode, which effectively suppresses charge-carrier recombination by passivating the defect states at the c-Si surface and simultaneously provides a good selective contact to one type of charge carrier. A layer stack system that fulfils these two requirements is called a carrier-selective passivating contact or passivating contact in short. The most important advantages of this approach are the full-area process possibility that simplifies its application, low recombination losses due to the absence of direct

metal/absorber contact and efficient charge-carrier extraction. The working principles and alternative pathways for passivating contacts will be explained in the following section more elaborately as they are the main focus of this thesis.

1.5 Carrier-selective passivating contacts

Generally, a carrier-selective passivating contact consists of a thin buffer layer for full-area surface passivation capped with an additional doped layer that selectively collects one carrier type, and a metallization scheme for current extraction. Carrier selectivity can originate from a stack of an insulating buffer layer with a doped layer on top of it, or a highly doped region within the c-Si wafer together with a passivating buffer layer and an additional doped layer on top. In both cases, the buffer layer should provide chemical or charge-assisted passivation, low bulk defect density, and good charge-carrier transport. There are different approaches to meet these requirements; based on the process temperatures they can be roughly classified as low thermal budget (< 250 °C) and high thermal budget (> 750 °C). A prime example of passivating contacts produced with a low thermal budget is the silicon heterojunction (SHJ). An example of a high thermal budget approach is the metal-insulator-semiconductor (MIS) system in which a thin interfacial oxide layer is sandwiched between the absorber and a metal. There is also the semiconductor-insulator-semiconductor (SIS) concept in which the metal is replaced by a highly or degenerately doped semiconductor.

1.5.1 Low thermal budget: Silicon heterojunction solar cells

The prominent approach that meets the requirements for passivating contacts is the a-Si:H/c-Si heterojunction. The term heterojunction describes the case that two materials with different composition or morphology form a junction. One of the earliest reports on a SHJ solar cell was by Fuhs *et al.* [Fuhs 1974], but nowadays this cell concept is associated with Sanyo — now Panasonic — that developed and patented the heterojunction with intrinsic thin-film (HIT) technology [Tanaka 1992]. In 1991, Wakisaka *et al.* demonstrated the displacement of the metallic contacts away from the c-Si surface by inserting a stack of wide-bandgap intrinsic and doped a-Si:H layers with a transparent conductive oxide (TCO) layer on top [Wakisaka 1991]. A schematic of the SHJ solar cell is represented in Figure 1.4. The fabrication of SHJ cells requires the use of *n*-type mono-Si wafers since there is no high-temperature treatment for impurity gettering or the deactivation of boron-oxygen defects. The surface passivation is provided by intrinsic amorphous silicon [a-Si:H(*i*)] deposited on both sides of the wafer [Descoeudres 2011b], and carrier selectivity is achieved by *in-situ* doped a-Si:H layers deposited with PECVD. The *n*- and *p*-type doped a-Si:H layers are applied to form electrical contacts to the electrons and holes in the wafer, respectively. To enhance lateral transport of the collected carriers toward the metallic grids as well as to improve light in-coupling, TCO is sputtered on top of the doped a-Si:H layers on both sides of the wafer [De Wolf 2012a], [Holman 2013]. Finally a silver (Ag) reflector is sputtered onto the rear. The TCO on the rear

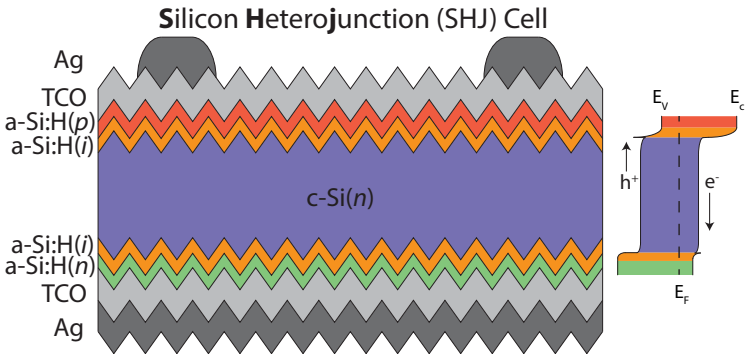

Figure 1.4 – Schematic cross-sectional view of a typical silicon heterojunction solar cell. Adapted from [De Wolf 2012a]

side between the doped layer and the Ag is not needed for charge extraction, but it is essential to avoid the excitation of evanescent waves in the metal contact and consequently to increase the internal reflectance at the rear surface. As the surface passivation of SHJ contacts is prone to degradation upon annealing at temperatures above 250 °C, this technology requires more sophisticated back-end processing. To that end, special Ag pastes with a low curing temperature are used for metallic front grid. The most important advantages of this technology are its simple process flow for both-sides-contacted SHJ devices and its high conversion efficiency potential. When these two advantages are combined, this technology can be cost competitive in regard to others. [Meyer-Burger 2014], [Ballif 2014].

Owing to the high-quality chemical passivation property of a-Si:H, this technology enables extremely high V_{oc} values as the interface states are reduced and the defective doped layer is screened from the absorber. A V_{oc} value of 750 mV was reported experimentally for a 98-μm-thick c-Si wafer, which is already very close to the theoretical limit of 761 mV for a 110-μm-thick c-Si wafer. Another important factor that defines the performance of the SHJ solar cell is the optimization of the various hetero-interfaces such as a-Si:H/c-Si and TCO/a-Si:H(p/n), as they lead to unfavourable energy barriers, the so-called band offsets (ΔE_v or ΔE_c) that impede the transport of majority carriers in the contacts. The charge carriers should overcome these transport barriers by thermionic emission, field emission (via tunneling) or thermionic field emission. The dominant transport mechanism mainly depends on the doping concentration of the doped a-Si:H layers as well as the overlaying TCO. Nevertheless, the reported *FF* values of the SHJ cells provide evidence that all the hetero-interfaces and their band offsets can be carefully engineered to minimize the impact of transport barriers for the operating conditions of solar cells.

The most important drawback of the SHJ solar cell technology is the parasitic optical absorption in the front TCO and a-Si:H layers, especially in the blue part of the spectrum. Accordingly the maximum reported J_{sc} value with both-sides-contacted SHJ technology is ca. 40.8 mA/cm^2 [Adachi 2015]. The best way to cope with this limitation is to use an interdigitated back-contacted (IBC) cell design where both electron and hole collectors are placed at the rear side

of the device. This architecture enables maximal light coupling into the wafer by eliminating the front metal grid shadowing and minimizing parasitic absorption at the front. With that concept J_{sc} values of up to 42.7 mA/cm^2 have been reported [Yamamoto 2017]. However, it can require sophisticated masking processes during the device fabrication to decrease electrical shading losses [Reichel 2011] which pose a major obstacle to industrialization. Nevertheless, Sunpower commercialized this IBC-SHJ cell structure, and recently Kaneka-Japan has announced a remarkable world record efficiency of 26.7 % using the IBC-SHJ concept [Yamamoto 2017].

1.5.2 High thermal budget: c-Si solar cells with oxide and poly-Si contact

In the 1970's, the metal-insulator-semiconductor (MIS) structure was explored for solar cell devices due to its simplicity and the better V_{oc} performance compared to standard *p-n* homojunction cells. A thin dielectric insulator — SiO_2 (< 2 nm to allow charge-carrier transport via tunneling) — was used as a buffer layer and an Al metal contact was deposited in a grid pattern on top of the insulator. Carrier selectivity was introduced by the work function mismatch in between the metal and the semiconductor. MIS cells showed efficiencies of up to 17.6 % [Godfrey 1979]. Nevertheless, due to the requirement of either a full-area thin metal layer or a grid–like structure at the front, this type of solar cell structure was eventually abandoned [Green 1974], [Shewchun 1974].

Inspired by the enhanced current gain in bipolar junction transistors (BJT) with polycrystalline silicon (poly-Si) emitters, in 1984, Kwark *et al.* developed a passivating contact based on a thin chemical oxide and a semi-insulating polycrystalline silicon (SIPOS) on top for solar cell applications [Kwark 1984]. SIPOS is a disordered material composed of doped poly-Si and silicon oxide prepared by atmospheric pressure chemical vapour deposition (LPCVD). Afterwards, the samples were annealed at 900 °C in order to activate the dopant and make the layers suitable for use as emitter contacts. They managed to reduce the emitter saturation current down to $\sim$ 10 fA/cm^2, i.e. by a factor of fifty compared to a conventional emitter structure with a metallic contact. Consequently, a V_{oc} of 720 mV on a 50 μm-thick *p*-type float-zone c-Si wafer was reported [Yablonovitch 1985]. Nevertheless, the authors did not attain good fill factors due to the poor conductivity of the SIPOS layer.

In 1990, Gan *et al.* performed detailed calibrations for the poly-Si emitter with a thermally grown interfacial oxide and compared it with the chemical oxide. They reported that the thermal oxide appeared to be more robust to high-temperature annealing whereas the chemical oxide was found to break up at lower temperatures [Gan 1990]. They formed the junctions with a two-step approach: a layer of poly-Si deposited without *in-situ* doping was first annealed at high temperature; the dopant diffusion was applied as a second step. They found that the temperature and duration of the first annealing step is crucial for the contact resistance of the junction and interpreted their findings by a breakup of the interface oxide. They suggested that the current transport across the junction is dominated by the current flow through the

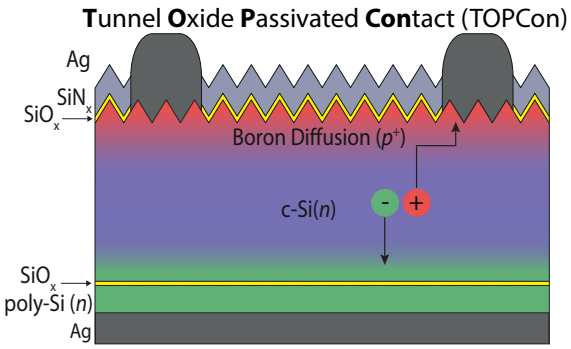

Figure 1.5 – Schematic cross-sectional view of the cells with a tunnel oxide passivating electron contact at the rear and a boron-diffused homojunction at the front.

nanoscale breakups in the oxide rather than by tunneling. Recently this approach has been revisited under the name of poly-Si on oxide (POLO) junction and very low saturation current density as well as the contact resistivity values are reported [Römer 2014]. The POLO junction relies on a relatively thick — 2 to 4 nm — thermal oxide and an approximately 100-nm-thick layer of poly-Si which is *ex-situ* doped by ion implantation. The structure is then subjected to a high-temperature treatment (> 1000 °C) to deliberately form local breakups, so-called pinholes, in the oxide for carrier transport. Recently, by applying electron- and hole-selective POLO junctions on a *p*-type c-Si wafer in IBC design, a record efficiency of 26.1 % was demonstrated [Haase 2018]. The rest of the cell parameters are presented in Table 1.1.

In parallel to this development, the tunnel oxide passivating contacts (TOPCon) concept was proposed by Fraunhofer ISE in 2014 [Feldmann 2014a], [Feldmann 2014c], [Feldmann 2014d], [Feldmann 2014e]. The TOPCon structure consists of a chemically or photo-chemically grown ultra-thin — 1.2 to 1.6 nm — SiO_x buffer layer together with an approximately 20-nm-thick *in-situ* doped layer of a-Si. After deposition of the doped a-Si layer by PECVD, the contact is annealed at temperatures in the range of 800 to 900 °C and subsequently re-hydrogenated with atomic hydrogen generated by remote plasma in the temperature range of 400–450 °C where atomic hydrogen can readily diffuse into c-Si. Combining this contact structure with a standard boron-diffused homojunction at the front side, as illustrated in Figure 1.5, a world-record efficiency of 25.8 % for *n*-type both-sides-contacted c-Si solar cell was established. The output parameters of this cell are shown in Table 1.1 as well.

Even though the POLO and TOPCon junctions seem to be similar structures, the physical working mechanism of each structure was claimed to be different. The charge-carrier transport in the TOPCon structure is explained with the tunneling model, whereas for the POLO junction it is explained with the pinhole model. At the time of writing this thesis, mentioned subject is one of the most debated topics in the c-Si solar cell community. The current agreement accepts that both mechanisms take place, depending on the annealing temperature, oxide type and integrity. Regardless of the underlying process, the most important advantage of this kind of contact scheme is perfect full-area passivation without posing any transport barrier to

Table 1.1 – V_{oc}, J_{sc}, *FF* and efficiency of different c-Si solar cell architectures.

Cell	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	**Efficiency** [%]
p-type PERL [Zhao 1998]	706	42.7	82.8	25.0
p-type POLO IBC [Haase 2018]	727	42.6	84.3	26.1
n-type TOPCon [Richter 2017]	724	42.9	83.1	25.8
n-type SHJ [Adachi 2015]	738	40.8	83.5	25.1
n-type SHJ IBC [Yamamoto 2017]	738	42.7	84.9	26.7

the majority carriers of the contacts.

Table 1.1 summarizes the reported world-record efficiencies with various cell architectures. Except for the *p*-type PERL, all are obtained with the passivating contact concept. Additionally, apart from the *n*-type SHJ from Adachi *et al.*, all the rest require complex fabrication steps, including some patterning and photolithography and consequently are not yet compatible with industrial applications.

1.6 Motivation and objectives

A fundamental limitation of the mainstream technology can be circumvented by using carrier-selective passivating contacts which suppress minority-carrier recombination while maintaining an efficient majority-carrier transport. Therefore, they are the key requirement to reach ultimate solar cell efficiencies for single-junction c-Si–based technologies. The main objective of this thesis is to develop an advanced understanding of the physical working principle and related limitations of the passivating contact structures for high-efficiency c-Si solar cells, using high and low thermal budgets. Following that, the second objective, which is closely linked to the first, is to utilize the gained understanding to improve solar cell performance with a particular focus on minimizing resistive losses, consequently improving the *FF*.

The investigation is initiated with the low-thermal-budget approach using the standard SHJ solar cell configuration. To that end, different carrier-selective contact layers are studied and the effects on transport barriers at the hetero-interfaces due to different doping efficiencies as well as microstructures are investigated. After facing limited *FF* values due to high specific contact resistivities, in particular with hole-selective *p*-type contacts, an approach with a high thermal budget is embraced. This is motivated by the fact that a high degree of crystallinity can be achieved with thermal treatment at elevated temperatures, leading to reduced specific contact resistivity and sheet resistance. In this context, the target of this thesis is defined as the development of novel passivating contacts that extract charge carriers efficiently (high *FF*) and provide good surface passivation over the full area (high V_{oc}). Certainly the necessary developments are coupled with the need to gain good understanding and knowledge of the

thermal budget required for passivating contact formation, phase separation, crystallization, chemical reactions and hydrogen diffusion/effusion. Additionally, a hole-selective contact is developed with the aim to offer an alternative solution for the BSF contact strategy at the rear side of industrial homojunction *p*-type c-Si solar cells. To this end, compatibility with established thermal processes for industrial solar cells such as contact firing and $POCl_3$ diffusion was defined as a main requirement. In keeping with the ambition of being industrially relevant, the development of high-temperature contacts was performed on *p*-type wafers since they are more easily available, i.e. market share of 95 %, and more cost-effective than *n*-type wafers.

As mentioned, the recent integrations of the high-temperature SiO_x/poly-Si–based passivating contacts (TOPCon and POLO-IBC) comply with a rather complex manufacturing process. Thus the industrialization of these technologies would require major changes. On the contrary, our goal is to adopt industrially compatible fabrication technologies and simple process flows with a limited number of process steps using the parallel-plate PECVD technique which is proven to have high throughput and extensive process versatility.

1.7 Structure of the thesis

After a general introduction to the working principle, limiting factors, recombination mechanisms for the state-of-the-art c-Si solar cells in the current Chapter, the remaining of this thesis is structured as follows:

- **Chapter 2** introduces the main solar cell fabrication tools and the most frequently used characterization techniques in the scope of this thesis together with descriptions of the corresponding terms and technological implications.
- **Chapter 3** discusses the potential optical and electrical benefits of replacing *in-situ* doped amorphous silicon with microcrystalline silicon layers as carrier-selective contacts, using a low-thermal-budget SHJ solar cell design.
- **Chapter 4** addresses the transition to a high-thermal-budget approach with the development and optimization of the hole-selective passivating contact based on chemically grown thin SiO_x and *in-situ* boron-doped silicon-rich silicon carbide [$SiC_x(p)$]. The structural evolutions upon thermal treatment as well as the electrical contact properties and surface passivation quality are investigated.
- **Chapter 5** demonstrates the integration of the developed high-temperature hole-selective contact to proof-of-concept hybrid solar cells as a rear contact, using a standard low-temperature SHJ front contact made of intrinsic a-Si:H and phosphorus-doped amorphous silicon [a-Si:H(*n*)].
- **Chapter 6** presents a pathway to improve the surface passivation quality of the boron-doped hole-selective contact by replacing the standard trimethylboron (TMB) dopant

gas with boron trifluoride (BF_3) during the PECVD process. Aiming to assess the function of fluorine, its distribution in the contact structure after thermal treatment is studied elaborately in test structures.

- **Chapter 7** covers the optimization of an electron contact based on interfacial SiO_x and phosphorous-doped $SiC_x(n)$, targeting front-side application. Following that, the developed hole and electron contacts with high thermal budget are tested at the device level, using a patterning-free, simple fabrication process based on co-processed junction formation in a single annealing step for both polarities.
- **Chapter 8** summarizes the main results obtained in the scope of this thesis and proposes a perspective on future development with possible integration pathways towards industrialization.

1.8 Contribution to the field

This thesis contributes to the research field of highly efficient c-Si solar cells that consist of carrier-selective passivating contact structures in several ways.

- To improve optical transparency and charge-carrier transport in low-thermal-budget SHJ solar cells, doped a-Si:H carrier-selective layers are replaced with microcrystalline silicon (μc-Si:H) layers. We demonstrate that:
  - The μc-Si:H layer shows conical growth revealing an increased crystalline area fraction with thickness. Consequently the specific contact resistivity decreases with thickness.
  - Thermionic emission can be minimized by replacing a-Si:H layers with μc-Si:H. Particularly, the difference is more pronounced for *p*-type contacts which limits the *FF*. By replacing a-Si:H(*p*) with μc-Si:H(*p*), the *FF* value is improved from 77.3 to 79.3 %.
  - The μc-Si:H layer can provide a J_{sc} gain of up to 1.5 mA/cm^2. However a clear trade–off between J_{sc} and *FF* is observed since a good electrical contact can be obtained only if the μc-Si:H layer thickness is above a certain limit, whereas the increased thickness eliminates its optical advantage.
  - Cu-plated SHJ cells featuring a highly transparent MoO_x hole-selective front contact and a relatively thick μc-Si:H(*n*) electron-selective rear contact can benefit from both improved front transparency and decreased specific contact resistivity, leading to J_{sc} values of up to 38.9 mA/cm^2 and *FF* values of up to 80 %.
- As a higher degree of crystallization can be achieved with thermal treatment, we focus on passivating contacts with a high thermal budget. To that end, *p*-type hole-selective passivating contacts based on a SiO_x and $SiC_x(p)$ layer stack on *p*-type wafers are developed. We show that:

  - It is beneficial to introduce an intrinsic silicon [Si(i)] inter–layer between chemically grown SiO_x and boron-doped $SiC_x(p)$ to protect the SiO_x from a chemical reaction with weakly incorporated carbon atoms.
  - The optimum Si(i) layer thickness depends on the carbon concentration in the $SiC_x(p)$. For a higher carbon concentration, a thicker Si(i) layer is needed to obtain a low recombination current.
  - The potential of the developed contact is investigated by realizing hybrid cells featuring a front SHJ electron contact and a SiO_x/Si(i)/$SiC_x(p)$ rear hole contact. With this concept *FF* values of up to 81.8 % are attained.

- To further improve the surface passivation of the hole contact with a high thermal budget, an *in-situ* fluorine incorporation is explored. We show that:
  - Upon annealing, fluorine accumulates at the interface regions of the contact and passivates interface defects. This is the first demonstration of an *in-situ* boron-doped and fluorinated hole contact that reveals excellent surface passivation even without subsequent hydrogenation.

- Phosphorus-doped $SiC_x(n)$ layers with a high thermal budget are developed and optimized as a front contact. By combining this with SiC_x:F(p), we demonstrate that:
  - Planar both-sides-contacted p-type solar cells, featuring full-area SiC_x:F(p) rear and $SiC_x(n)$ front contacts, co-processed in a single annealing step, yield excellent *FF* values of 84 % and V_{oc} of 727 mV.
  - With front-side-textured cells, promising conversion efficiencies of up to 22.6 % are demonstrated. This is the highest reported efficiency for this kind of solar cells.

Overall, our findings especially about contact structures based on interfacial SiO_x and doped silicon draw a great interest from the scientific community as this technology is seen as an upcoming mainstream after the PERC era. The obtained results exhibit a clear roadmap about how to improve the charge-carrier transport in solar cells that employ passivating contacts. Apart from the topics summarized here, contributions to other investigations are also provided in the framework of internal and external collaborations. The developed μc-Si:H layers in the scope of this thesis were used to design a novel tunnel-IBC-SHJ concept which eliminates the need to pattern the hole-selective layer and simplifies the back-contacted device fabrication [Tomasi 2017]. Again the same μc-Si:H layers are used in perovskite/silicon monolithic tandem devices as a recombination junction instead of TCO [Sahli 2017]. Also recently, our both-sides-contacted cells featuring a SiC_x:F(p) rear and $SiC_x(n)$ front contact, prepared on front-side-textured, rear-side-planar p-type wafers are used as a bottom cell for perovskite/silicon two-terminal monolithic tandem devices and efficiencies above 25 % are achieved[1].

[1] This work will be part of an upcoming publication by Sahli *et al.*

2 Experimental details: Fabrication and characterization techniques

This chapter introduces the experimental details and methods. First, the most frequently used fabrication processes and relevant tools are described briefly. Following that, we discuss details of the characterization techniques that are employed to determine the properties of the passivating contacts as well as the performance of the solar cells.

2.1 Fabrication technologies

The fabrication of test structures for passivating contacts and of complete cells requires several process steps. These can be classified into the following three main categories; (i) sample preparation, (ii) junction formation and (iii) metallization. In this thesis both, low and high thermal budgets are explored to produce passivating contacts. Despite their different thermal budgets, there are some common fabrication processes used for both approaches such as wet chemical processes (texturing and cleaning), plasma-enhanced chemical vapour deposition (PECVD) and metallization. If not stated otherwise, the process descriptions given in this section cover both approaches and differences are mentioned in the text.

2.1.1 Sample preparation

For the investigations performed in this thesis either planar or textured high-quality monocrystalline float-zone (FZ) wafers from Topsil or Siltronic AG were used.

Wet-chemical processes: Texturing and cleaning

After wafer washing, saw damage — micro-cracks and dislocations — on the wafer surface is removed by etching in a concentrated potassium hydroxide (KOH) solution to obtain good electronic quality. Following that, with a second KOH bath at temperatures of around 80 °C, micron-scale random pyramids are formed by anisotropic etching, resulting in an increased surface area by a factor of ~ 1.7. These pyramids reduce the reflectivity of the surface effectively

and consequently increase the in-coupling of photons into c-Si [Hahn 2014]. When polished wafers are needed, the surface planarization should be realized after this step. Following the texturization (or planarization), the wafers are subjected to a RCA cleaning sequence composed of standard clean 1 and 2 (SC-1 and SC-2)[1]. The SC-1 solution consists of H_2O, hydrogen peroxide (H_2O_2), ammonium hydroxide (NH_4OH) and it removes organic contaminants from silicon surface while dissolving the existing oxide and forming a new one. The SC-2 solution consists of H_2O, H_2O_2, hydrochloric acid (HCl) and it removes metallic contaminants [Kern 1990]. Immediately before standard silicon heterojunction (SHJ) cell processing, native oxide formed on the c-Si wafer surface during the cleaning, is removed using a 5 % diluted hydrofluoric acid (HF) solution until the c-Si surface is terminated by hydrogen and becomes hydrophobic. For the passivating contact structures with high thermal budget, additional chemical processes are necessary and they are addressed in the following section.

Interfacial oxide growth

The passivating contact structure with a high thermal budget is based on thin interfacial oxide (SiO_x) and doped silicon layer on top. Here we discuss the growth of thin SiO_x layer which has two main functions of (i) providing good chemical passivation and (ii) preventing the epitaxial crystallization of the doped silicon layer on c-Si during thermal treatment which would otherwise deteriorate drastically the c-Si surface passivation. The use of SiO_x as an interfacial layer for this kind of contact structure is motivated by the fact that c-Si/SiO_x is a well-studied interface which leads to low interface defect density, additionally it has low positive fixed charge density [Reed 1988]. As SiO_x is an insulator, forming an ultra-thin SiO_x is an important requirement to obtain efficient charge-carrier transport. Thermal annealing in a mixed O_2/N_2 ambient is the most common oxidation method. There are also various wet chemical techniques to form thin SiO_x layers at low temperature, such as oxidation in a bath of hot nitric acid (HNO_3) at 80–110 °C or in ozonized deionized-water (DIO_3). Alternatively, it can be formed in a dry ozone atmosphere under an UV radiation. Despite the fact that thermal oxidation process is known to produce high quality oxides, it is not preferred as it is difficult to precisely control the thickness and obtain thin oxides. In this thesis, we mainly use the chemical SiO_x that is grown in hot HNO_3 bath. Additionally some results are obtained with UV-O_3 oxide generated by photo-oxidation using a mercury (Hg) vapour lamp, more detail about this process can be found in Appendix C.

Prior to chemical SiO_x growth in HNO_3, the native oxide formed during the cleaning process is completely removed by HF as this oxide is not reproducible due to the fact that cleaning solutions (SC-1 and SC-2) alter their chemical composition within hours due to the thermal decomposition of H_2O_2 leading to a problem in oxide reproducibility [Kern 1990]. Following that the chemical SiO_x is formed in 69 wt % HNO_3 solution at 80 °C by submerging the wafers for 10 minutes. Oxidation of c-Si surface with HNO_3 proceeds as a high concentration of atomic

[1] The wet-chemical processing for saw-damage removal and wafer texturing are carried out at the PV-Center of the Swiss Center for Electronics and Microtechnology (CSEM).

oxygen with a strong oxidizing power is produced by its decomposition [Kobayashi 2003]:

$$2HNO_3 \rightarrow 2NO + H_2O + 3O \tag{2.1}$$

Here the atomic oxygen is the oxidizing species that diffuses through the growing SiO_x layer and reacts at the c-Si/SiO_x interface. After 10 minutes, the thickness of the SiO_x is observed to be stable and very homogeneous throughout the c-Si wafer as it is a self-limiting process with very good reproducibility [Kobayashi 2003].

2.1.2 Junction formation

This section describes the process tools used to form junctions that provide surface passivation and carrier selectivity simultaneously. For SHJ cells with low thermal budget, the junction formation is realized by depositing intrinsic and doped layers using PECVD, whereas the passivating contacts with high thermal budget require additional processes such as thermal treatment and interface hydrogenation after the deposition of the doped layers.

Plasma-enhanced chemical vapour deposition

The final step of sample preparation (section 2.1.1) depends on the applied thermal budget. For low temperature SHJ cells, after a HF-dip that removes the native SiO_x, the surface is ready for the next process. In that context, the hydrogenated intrinsic amorphous silicon [a-Si:H(*i*)] layer is deposited on both sides of the wafer which provides quasi-perfect chemical passivation. Following that, *in-situ* phosphorous-doped hydrogenated amorphous silicon [a-Si:H(*n*)] and *in-situ* boron-doped hydrogenated amorphous silicon [a-Si:H(*p*)] layers are deposited on the opposite sides of the wafer as electron- and hole-selective contacts, respectively. At this stage, the SHJ cell precursors exhibit excellent surface passivation and the ability to separate the charge carriers. Therefore, they are ready for the final process step which is necessary for charge-carrier collection — metallization. For the high temperature approach, the *in-situ* doped layer is deposited directly on the SiO_x. Different from SHJ technology, the contact structures are not yet functional at this stage; they provide neither surface passivation, nor charge-carrier separation. In its *as-grown* state, the chemical SiO_x provides only poor surface passivation and the deposited doped layers can be seen as a dopant reservoir which has significant importance for the next steps to "*activate*" the contact structure.

The PECVD technique has several advantages such as one-side processing, good control of the layer microstructure and the possibility to alloy the layer composition in a wide range i.e. amorphous silicon nitride (a-SiN_x:H), amorphous silicon oxide (a-SiO_x:H) or amorphous silicon carbide (a-SiC_x:H). Additionally, layer properties such as doping concentration, crystallinity, bandgap, hydrogen content, etc. can be controlled easily with the plasma parameters, i.e. power, pressure, temperature, excitation frequency and ratio of the precursor gases.

In general, plasma can be described as an ionized gas that includes a mixture of electrons, neutral atoms, ions, free radicals and molecules at many different levels of excitation. It is also called *glow discharge* as energy transfer from electrons to gas precursor molecules occurs via collisions, causing a radiation in the visible part of the spectrum [Lieberman 1994]. For plasma ignition, a reactor chamber is filled with a precursor gas of desired pressure, and then ionized by an electric field. This is known as cold plasma because there is no thermal equilibrium in between temperatures of the gas (T_g) and the electrons (T_e), where $T_e > T_g$ [Konuma 1992]. Under this non-equilibrium condition, chemical reactions are initiated by collisions of highly energetic electrons and gas molecules, thus facilitating the deposition at relatively low temperatures (~ 200 °C) [Smith 1995].

The PECVD reactors used in this thesis contain two parallel electrodes with capacitive excitation of the plasma. The distance between the electrodes is an important parameter that impacts the layer quality as it defines the mean free path of radicals before they reach to the substrate surface. The typical spacing used in this work is the range of 13 to 15 mm. These two electrodes are connected to a power supply coupled to a frequency generator and driven by an alternating electrical field at a specific excitation frequency and power. One of the electrodes holds the substrate; the second contains a shower head through which precursor gases are sent into the reaction zone. In our PECVD design, the parallel electrodes are additionally sealed in so-called *plasma-box* which is used to create pressure difference between the main chamber and the plasma box, consequently preventing the diffusion of contaminants from the main chamber walls into the reaction zone [Perrin 2000], [Stueckelberger 2014], [Seif 2015a], [Geissbühler 2015a]. The introduced process gas flows are controlled by mass flow controllers and the chamber pressure is control by a butterfly valve situated between the chamber and the pumping unit. The layer thickness is controlled by the plasma duration where the deposition rate is determined by the various competing surface reactions such as desorption, adsorption, dissociation.

In the scope of this these three different PECVD reactors are used frequently for different purposes. A single wafer research tool with cluster configuration from INDEOtec (Octopus-I) is used for the a-Si:H and the μc-Si:H layers applied to SHJ solar cells (presented in Chapter 3). This system is composed of four different chambers to avoid cross-contamination. One chamber is dedicated to a-Si:H(*i*) passivation layers, another is dedicated to doped a-Si:H layers; both chambers are operated at an excitation frequency of 40.68 MHz. The third chamber is dedicated to doped μc-Si:H layers and operated at an excitation frequency of 13.56 MHz. The second system is a large-area reactor from TEL solar (KAI-M) with two separate deposition chambers dedicated to intrinsic and doped layers. The development of passivating contacts with high thermal budget was mainly carried out in the chamber dedicated to doped layers with an excitation frequency of 40.68 MHz. Finally a PECVD reactor build in-house (XL) with excitation frequency of 81.36 MHz is used to deposit SiN_x as a hydrogen donor layer for high thermal budget contacts.

Thermal treatment

After depositing the doped silicon-based layers by PECVD, the passivating contacts with high thermal budget are subjected to a thermal treatment. This is performed in a quartz tube furnace under either Ar or N_2 atmosphere at elevated temperatures (> 750 °C) with a heating and cooling ramp of 10 °C/min and 2 °C/min, respectively. There are three main functions of this annealing step:

- First, during the annealing process dopant atoms diffuse through the thin SiO_x into the bulk c-Si and introduce favorable band bending within the c-Si that shields the minority carriers from the c-Si/SiO_x interface, therefore facilitating a selective carrier extraction. At this stage, finding the optimum annealing temperature is curial as extensive dopant diffusion is accompanied with Auger recombination and bandgap narrowing effect.
- Second, the stoichiometry and the integrity of the interfacial SiO_x can be changed upon annealing, depending on the type of the SiO_x and thermal treatment temperature. In literature, it is reported that some atomic defects (e.g. O vacancies) in the oxide start to cluster, yielding a local thinning of the oxide and eventually pinhole formation [Hermle 2018]. A strong perforation of the oxide is also reported for exaggerated thermal budgets which yields a poor surface passivation quality.
- Last but not least, it leads to a partial crystallization of the doped silicon-based layer which has only an amorphous phase in *as-deposited* state. This is beneficial as crystallized silicon has superior electrical properties compared to amorphous silicon such as higher mobility and a higher doping efficiency which leads to lower contact resistivities with TCOs or metals, thus relaxing the constrains on metallization design. Likewise, lower parasitic absorption in crystalline material also improves the optical properties.

Even though hydrogen effuses out during the thermal treatment, some contact structure reveals decent surface passivation quality immediately after annealing. Especially for the electron-selective contacts, phosphorous diffusion often does not deteriorate the SiO_x/c-Si interface and its diffusion provides efficient charge-induced surface passivation. However, if the SiO_x/c-Si interface is not well preserved and some defect states are introduced during the thermal treatment, additional interface treatments are necessary to obtain good surface passivation.

Hydrogenation

Interface defect states can be reduced by hydrogen passivation. Forming gas (4 % H_2 in N_2) annealing (FGA) is one of the most recognized methods for re-hydrogenation of passivating contact structures produced with high thermal budget [Aberle 1992]. At the beginning of our development, we also used the FGA method, however it was observed that especially for hole-selective contact in which the boron diffusion through the SiO_x introduces significant

amount of defect states at the SiO_x/c-Si interface, molecular hydrogenation is not effective. Based on this observation, an atomic hydrogenation method was tested, using a SiN_x overlayer as hydrogen source. To that end, SiN_x layers were deposited in the in-house built PECVD reactor and hot plate annealing was performed at 450 °C for 30 min to diffuse the hydrogen from the SiN_x overlayer through the contact stack and incorporate it at the SiO_x/c-Si wafer interface. With this method efficient hydrogenation was obtained, probably due to the higher mobility of atomic hydrogen in silicon.

2.1.3 Metallization

This section covers both passivating contact structures with low and high thermal budgets as the similar transparent conductive oxide (TCO) and metal layers are employed to collect the separated charge carriers.

Transparent conductive oxide and metal deposition

Magnetron sputtering is the most prominent deposition technique for TCO deposition. It is a physical vapour deposition (PVD) technique in which layers are deposited from single atoms or small clusters. Normally no surface reactions take place during layer formation, and it provides excellent film uniformity, good thickness control and surface adhesion. Sputtering is based on a kinetic process where atoms are ejected from a target by bombardment with energetic ions, commonly Ar^+. After ejection from the target, formation of layers on the substrate surface occurs by condensation of sputtered atoms. Secondary electrons are emitted from target due to the ion bombardment and they are very significant to maintain the discharge. In magnetron sputtering configurations, a magnetic field parallel to the target surface is generated to increase the density of secondary electrons in the plasma region and consequently to increase the sputtering yield. The plasma may be maintained by either RF or DC excitations. DC excitation can be used only for conductive targets, whereas RF excitation can be used for both conductive and non-conductive targets.

In this thesis, the sputtering technique is mainly used to deposit indium tin oxide (ITO) and silver (Ag). The deposition is carried out through a shadow mask that defines the solar cell area and test patterns such as the one for TLM measurement. During ITO sputtering, oxygen is added in addition to Ar in order to avoid oxygen depletion of the deposited film. The partial pressure of the oxygen has an important effect on the ITO conductivity as it controls the densities of oxygen vacancies within the ITO. Depending on the application of the ITO layers — front or rear of the cell — the necessary requirements differ which is discussed more elaborately in the following chapters. Additional to ITO, alternative sputtered TCO layers are also tested in this thesis such as tungsten-doped indium oxide (IWO), zirconium-doped indium oxide (IO:Zr), aluminium-doped zinc oxide (ZnO:Al).

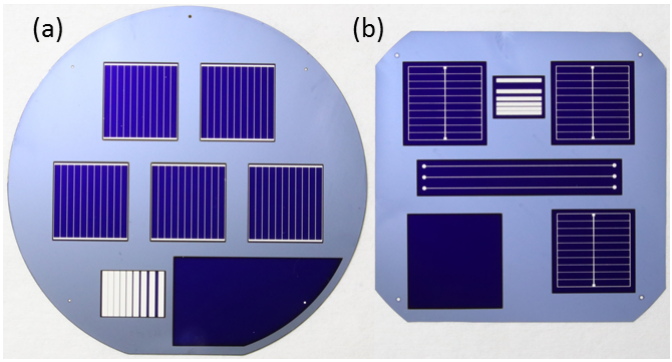

Figure 2.1 – The front grid design (a) new design and (b) old design.

Screen-printing of the front contact

In the scope of this thesis, the front-grid metallization was mainly realized via screen-printing of an Ag paste which is suitable for curing at low temperatures (~ 200 °C). The Ag paste is applied in an automated screen-printer (XH STS from EKRA) through a screen which consists of a metallic mesh covered by a resist with local openings. This step is followed by curing of the Ag paste on a belt furnace at 210 °C for 30 min [De Wolf 2012b], [Geissbühler 2015a]. The front-grid design used in this thesis consists of nine internal fingers placed 2.1 mm apart connected with either a central busbar, old design with 5 % shading loss [see Figure 2.1(b)], or with two external busbars, new design with 3 % shading loss [see Figure 2.1(a)].

2.2 Material characterization techniques

To gain better understanding of the working principle of the developed passivating contacts, their microstructural and electrical properties were investigated by means of various methods. The most frequently used characterization techniques in this thesis are described briefly in this section.

Spectroscopic ellipsometry

Spectroscopic ellipsometry (SE) is a powerful and non-destructive technique to evaluate a wide range of layer properties such as thickness, crystallinity, composition, size, roughness, bandgap, optical and dielectric constants. The SE measurement technique is based on the fact that the polarization state of light changes after reflection from a sample surface, thus enabling to deduce the optical parameters.

Unpolarized white light from a xenon arc lamp is used as an illumination source. First, a collimator converts the light to a collimated beam and a polarizer makes the light linearly polarized. Upon reflection from the sample, p-(parallel to plane of incidence) and s-(perpendicular to plane of incidence) polarizations change in phase and amplitude. SE measures two param-

eters Psi (Ψ) and Delta (Δ), which describe the amplitude ratio and the phase difference between *p*- and *s*-polarizations, respectively. These parameters are measured additionally as a function of the light energy. Thus, the change in polarization state (ρ) is identified by the analyser in terms of Δ and Ψ which are related to the ratio of the Fresnel reflection coefficients R_p and R_s for *p*- and *s*-polarized light:

$$\rho = \frac{R_p}{R_s} = tan(\Psi)e^{i\Delta} \tag{2.2}$$

With SE it is also possible to determine refractive index (n) and extinction coefficient (k), consequently, the complex refractive index ($N = n + ik$) and the complex dielectric function ($N^2 = \varepsilon = \varepsilon_r + i\varepsilon_i$). The real and imaginary parts of dielectric function represent the in-phase ($\varepsilon_r = n^2 - k^2$) and out-of-phase ($\varepsilon_i = 2nk$) components of the dielectric response of a material. The in-phase component results in dispersion whereas the out-of-phase component results in absorption. It is important to note that the SE measurement is an indirect characterization technique, which requires fitting of the measured Δ and Ψ spectra, modelling of the dielectric function and the construction of an optical model for data analysis. There are different dielectric function models for fitting and an adequate model has to be chosen according to the optical properties of the sample. For instance, in the case of $k \sim 0$, Cauchy or Sellmeier models are commonly used, but if there is free carrier absorption, the Drude model is preferred. In addition, there are various models such as the Lorentz model, Tauc-Lorentz model and other, dielectric function models that can be applied to specific material systems. More detailed information about the technique and dispersion models can be found in [Fujiwara 2007a].

An important constraint of the SE measurement is the surface roughness which should be minimum since rough surfaces reduce the reflected light intensity, leading to noisy measurements. For that reason, either glass or planar c-Si wafers are used as a substrate in this work. Another critical parameter is the incidence angle at which the measurement is performed. It strongly depends on the Brewster angle, thus the refractive index ratio of the investigated media. For the air/glass interface, the Brewster angle is around 56° whereas for air/c-Si, it is close to 74° with respect to the surface normal. Hence, a measurement angle of 70° can be used for both substrates in the case of single angle measurement. In our case, mainly variable angle SE measurements are performed at 50–60–70° for glass and at 60–70–80° for c-Si substrates [Stueckelberger 2014].

In this work, the measurements were carried out with SE UVISEL from Horiba Jubin Yvon, and subsequent fittings were performed with the software DeltaPsi2 from the same supplier. The measurements are mainly performed for a-Si:H and μc-Si:H layers either in *as-deposited* or annealed states in the whole accessible energy range from 0.6 to 6 eV. The system includes infrared (IR) and UV/VIS monochromators that changes at 880 nm (1.4 eV) to cover the mentioned spectrum. To determine the crystalline volume fraction of the mixed phase silicon layer, the imaginary part of dielectric function is especially significant. Figure 2.2(a) illustrates the way of monitoring the phase transition from amorphous to single-crystalline silicon using

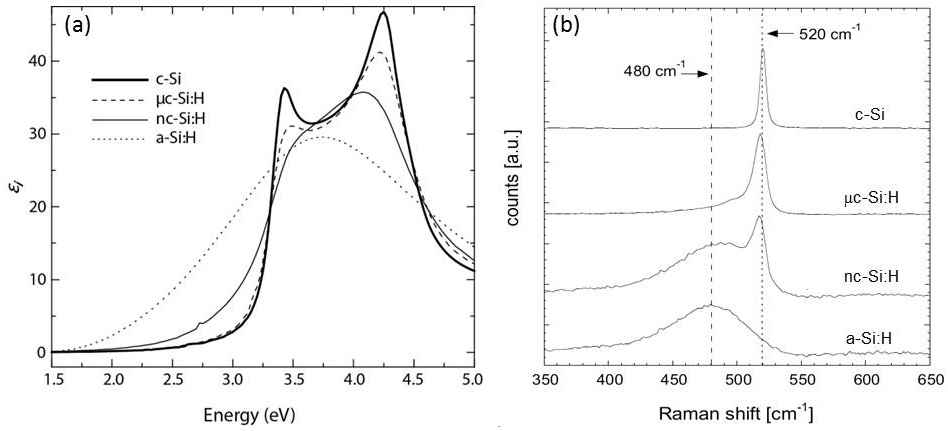

Figure 2.2 – (a) Reference SE data of the imaginary dielectric function ε_i for phase transition from a-Si:H to c-Si [Filonovich 2009]. (b) Reference RS data for phase transition from a-Si:H to c-Si [Droz 2003], [Droz 2004]. Adapted from [Nogay 2013].

the ε_i values as a function of energy. Commonly, for a-Si:H layers the Tauc-Lorentz model is applied whereas for μc-Si:H layer the Kato-Adachi model is preferred. For more detail see [Stueckelberger 2014], [Seif 2015a].

Raman spectroscopy

Raman spectroscopy (RS) is an analytical technique that gives an indirect information on elemental composition, crystallinity and stress of the metarial. In this work, RS is mainly used to define the crystalline fraction of the passivating contact structures either in *as-deposited* or annealed state. The technique relies on a frequency change of photons after inelastic interactions with vibration modes in the sample. If the scattered photon has the same frequency or energy as that of the incident light, the interaction process is called as elastic or Rayleigh scattering. If the scattered photon has different frequency or energy than that of the incident light, the process is called inelastic scattering. When the incident photon gains energy in the interaction by absorbing a phonon, the frequency of the scattered photon shifts up and this process is referred to as anti-Stokes shift. If the incident photon losses energy in the interaction by emitting a phonon, the frequency of scattered photon shifts down; this process is referred as Stokes shift. Generally, the anti-Stokes scattering is less probable than that of Stokes scattering. When a monochromatic excitation is used, these two Raman lines are shifted symmetrically with respect to the Rayleigh line at $\Delta\upsilon = 0$ cm^{-1}. The frequency shift observed in scattering is directly related with the vibrational energy of chemical bonds within the material. Hence, analysis of the scattered frequencies reveals information about the structure of the scattering medium. In crystalline structures local bonds have well-defined energies with long-range orders. As shown in Figure 2.2(b), c-Si reveals one peak originated from transverse optical (TO) mode of Si–Si vibrations in the crystal. It is located at 520 cm^{-1} with full width half maximum (FWHM) of ~ 4 cm^{-1}. In disordered amorphous material such

as a-Si:H, a wider distribution of bonding energies is observed, the corresponding spectrum exhibits thus a broad peak at 480 cm^{-1} with FWHM in the range of 50 to 60 cm^{-1} [Droz 2004]. As nanocrystalline silicon is a mixed-phase material which consists of both crystalline and amorphous phases, it reveals a sharp but asymmetric peak with a shoulder at 480 cm^{-1}. The crystalline fraction of this kind of layers can be calculated by taking the deconvolution of the Raman spectra using three Gaussian peaks centered at 480, 510 and 520 cm^{-1}. An additional peak at 510 cm^{-1} represents the defective part of the crystalline phase associated with grain boundaries. The Raman crystallinity is then deduced as the ratio of the integrated area for the crystalline phase related peaks to total area of the three peaks [Droz 2004].

In the scope of this thesis either a InVia REXLEX (Renishaw) or a MonoVista CRS+ (S& I) were used. The most important parameter of the measurement is the wavelength of the excitation laser as it determines penetration depth, thereby the collection depth of the Raman signal (i.e. high-energy photons are absorbed relatively fast, therefore measured signal gives an information about the region close to the surface). In both systems an excitation wavelength of 325 nm was used in order to probe regions close to the surface.

Grazing incidence X-ray diffraction

X-ray diffraction (XRD) is a technique that gives access to the crystallography of the measured sample. It relies on the diffraction of X-rays at the periodic atomic structure of crystals. Crystals are formed of unit cells whose dimensions are called lattice parameter. However, since X-ray radiation has a large penetration depth into the material, it is not trivial to characterize thin layers without penetrating to the substrate. This drawback can be eliminated using grazing incidence (GI) angle XRD technique. This method is applied at very low incidence angles (0.1–3°) to increase the path of incoming X-rays through the layer of interest, thereby enhancing the output signal by reducing the contribution of the substrate. During the collection of a diffractogram, the incident angle of the X-ray is kept constant, while a detector is sweeping an angular path around the sample surface. In this wok, the crystallinity of selected contact layers after annealing was analyzed by grazing-incidence X-ray diffraction spectroscopy (GI-XRD) using a Bruker D8 Discover Tool with a Cu Kα (λ = 1.542 Å) radiation source at a fixed incidence angle of 0.3°.

Transmission electron microscopy

Transmission electron microscopy (TEM) works on the same basic principle as standard light microscopy except the fact that it uses electrons instead of photons. As the wavelength of electrons is much smaller than that of photons, TEM can provide much higher magnification and resolution when visualizing a sample. The TEM technique relies on the interaction between an electron beam with energy in the range of 80 to 300 keV and a thin electron-transparent specimen. The components of the TEM can be categorized as the illumination system, the objective lenses, and the imaging system. The illumination system consists of

the electron gun that produces a beam of electrons, and the condenser lenses that transfer the electrons towards the specimen. Once the electron beam reaches to the region where the objective lens and specimen are situated, it is partially transmitted through the thin specimen, depending on how transparent the specimen is to electrons. The objective lens focuses the portion of the beam that is emitted from the specimen into an image. The thinner the specimen, the more electrons it can transmit and the more information can be obtained. These demands become less strict as the beam voltage increases, but this is offset by the production of electron beam damage. Following the interaction of the electrons with the specimen, the image is magnified and projected onto a viewing screen or a camera. TEM system has to be kept under vacuum to ensure that electrons do not scatter or collide with any matter except the specimen.

In the scope of this thesis, different modes of TEM are used to investigate the microstructural and compositional evolution of the passivating contact structures. These include bright-field mode (BF), dark-field mode (DF), high-resolution transmission electron microscopy (HRTEM), scanning transmission electron microscopy (STEM) in conjunction with energy dispersive X-ray spectroscopy (EDX) and electron energy loss spectroscopy (EELS). More detailed information about these measurement modes can be found in [Williams 2008]. The system specifications used in this work are given in the relevant sections throughout the thesis[2].

Photoluminescence imaging

Photoluminescence (PL) imaging is a versatile technique that measures spatial variation of the effective minority carrier lifetime by imaging the band-to-band emission from c-Si. It is based on the illumination of the sample and detecting the emitted light from the band-to-band radiative recombination using a CCD camera coupled with a filter that eliminates the signal of the light source. In the obtained image, bright regions correspond to high material quality in which only the radiative recombination takes place, whereas dark regions are dominated by non-radiative recombination processes related to defects and impurities. Since PL imaging is an extremely fast and contactless technique, it is a wide-spread method for process monitoring by research institutes and manufacturers [Trupke 2005],[Trupke 2006], [Trupke 2012].

Electrochemical capacitance-voltage

The doping profiles of the passivating contact structure with a high thermal budget are investigated with an electrochemical capacitance-voltage (ECV) technique. ECV measures the electrically active dopant concentration while electrochemically etching the sample. For the measurement, the sample is situated in contact with an electrolyte solution, in our case 0.1 M ammonium fluoride (NH_4F) that creates a Schottky junction with the sample. Consequently, a

[2]All the TEM measurements presented in this thesis are performed by Dr. Quentin Jeangros. The contribution is gratefully acknowledged.

depletion is formed that contains ionized donors and possibly electrically active defects or traps. This depletion region behaves as a capacitor and the voltage dependent capacitance is expressed as follows:

$$\frac{1}{C^2} = \frac{2(V_{fb} - V_a)}{q\varepsilon_r\varepsilon_0 N A^2} \tag{2.3}$$

Here, V_{fb} is the flat band potential, V_a is the applied voltage, ε_0 is the vacuum permittivity, ε_r is the relative permittivity of the sample, q is the elementary charge, and A denotes the contact area between the electrolyte and sample. By varying the applied voltage, the charge-carrier density at the edge of the junction depletion can be written as follows:

$$N = \frac{C^3}{q\varepsilon_r\varepsilon_0 A^2 \left(\frac{dC}{dV}\right)} \tag{2.4}$$

Here, dC/dV is the slope of the $C-V$ curve at the edge of the depletion layer. The parameters C and dC/dV are obtained by applying a negative DC voltage overlaid with a small AC signal and used to determine the electrically active carrier concentration N at the edge of the space charge region. When the semiconductor is positively polarised, the electrolyte etches the sample. The quantity of the etched material is determined by integrating the current and applying the law of Faraday. A doping profile is obtained by successive etchings and capacitance measurements. ECV is a practical and relatively cheap technique; however, an inaccurate definition of the etched depth and etched area can occasionally impact its precision [Wu 2008]. Further information about the technique can be found in literature [Blood 1986], [Sermage 2016].

Transfer length method

The electrical quality of the passivating contacts is evaluated by specific contact resistivity measurements using the transfer length method (TLM). In this method, an array of metallic contact pads separated by various distances, are deposited on a continuous semiconductor layer as illustrated in Figure 2.3(a). Following that, the total resistance between pads is deduced with Ohm's law by applying a voltage and measuring the resulting current. By plotting the measured total resistance as a function of the pad spacing and applying a linear fit, one can extract the sheet resistance (R_{sheet}) and contact resistance (R_c) values from the slope and the intersection with the ordinate, respectively. According to Berger's TLM theory, R_c can be expressed as a function of R_{sheet} with the following equation [Berger 1972]:

$$R_c = \frac{\sqrt{R_{sheet}\rho_c}}{W} coth\left(L\sqrt{\frac{R_{sheet}}{\rho_c}}\right) \tag{2.5}$$

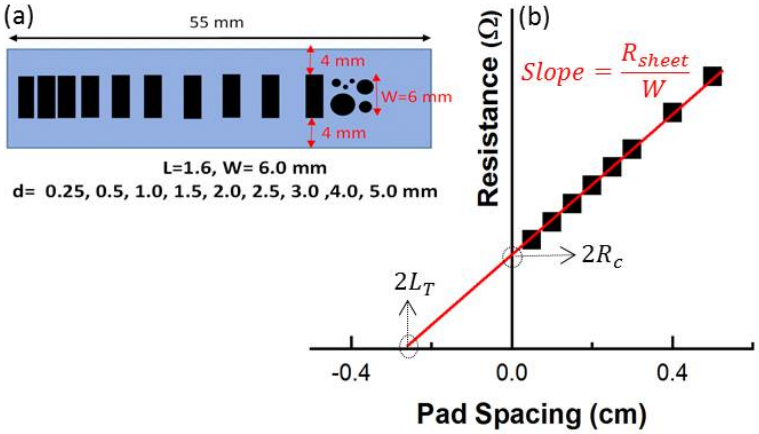

Figure 2.3 – (a) Top-view schematic of the TLM pattern used in this work, (b) Total resistance as a function of pad spacing.

Here, W denotes the length of the contact pad, L is the width of the contact pad and ρ_c is the specific contact resistivity between the layer of interest and the overlying metallic pad. As the R_c depends on the contact geometry, often ρ_c is preferred to characterize the contact performance [Vinod 2011]. The ρ_c can also be expressed in terms of R_{sheet} by the following relation:

$$L_T = \sqrt{\frac{\rho_c}{R_{sheet}}} \tag{2.6}$$

Here L_T is the transfer length that is described as the shortest length needed for the current to be efficiently injected from the semiconductor to the contact pad or vice versa. It is determined from the intersection of the linear fit with the abscissa — pad spacing — as demonstrated in Figure 2.3(b). It is important to note that to obtain a reliable extraction of electrical contact parameters by the TLM method, the contact width L should be wider that L_T [Schroder 2006].

2.3 Device characterization techniques

Quasi-Steady State Photoconductance

The passivation quality of the contact structures is quantified by means of quasi-steady state photoconductance (QSSPC) measurements. This technique works by injecting a known excess charge-carrier density (Δn) by illumination with a flash lamp. The density of the injected carrier-plasma can be measured without contact via its reflectivity for microwaves and its decay in dark yields the effective lifetime (τ_{eff}). Repeating the measurement with different intensities of the flash-lamp yields the dependence of τ_{eff} on the injection level Δn. The effective lifetime τ_{eff} contains information on the recombination both at the c-Si wafer

surfaces as well as in the bulk [Sinton 1996a], [Kerr 2002].

$$\tau_{eff}(\Delta n) = \frac{\Delta n}{G(t) - \frac{d\Delta n}{dt}} \tag{2.7}$$

Here, $G(t)$ is the photogeneration rate that depends on illumination intensity, absorption fraction of the sample and wafer thickness. Depending on the time constant of the flash lamp (t_f) either a transient measurement ($t_f << \tau_{eff}$) or a quasi-steady state measurement ($t_f >> \tau_{eff}$) can be carried out. In case of a transient measurement, the generation rate is neglected and long effective carrier lifetimes can be measured. In a quasi-steady state mode, the photogeneration rate has to be taken into account while the term $d\Delta n/dt$ is neglected and short effective carrier lifetimes can be measured [Nagel 1999].

The quasi-steady-state photoconductance data implicitly include information about the short-circuit current versus open-circuit voltage characteristic of the measured structure. The short-circuit current is implied by the irradiance. The excess-carrier density implies an open-circuit voltage, thereby the *quasi-Fermi level* splitting. By assuming a linear relationship between illumination light intensity I_L (suns) and current density [$J = J_{sc}(1 - I_L)$], an implied *J-V* curve can be constructed. The implied solar cell parameters — iV_{oc} and *iFF*— represent upper limit of the measured structure. The iV_{oc} is associated with the lifetime at high injection levels ($\sim 10^{16}$ cm^{-3}) at one sun condition, whereas the *iFF* is associated with the lifetime at low injection levels ($\sim 10^{15}$ cm^{-3}) at implied maximum power point condition. The latter parameter, *iFF*, gives an information about the *FF* losses arising from charge-carrier recombination in the c-Si wafer and at its surface.

In this thesis, a WCT-120-TS lifetime tester from Sinton Instruments is used to determine the abovementioned parameters. The measurements are mainly conducted in transient mode. As the method is contactless, fast and non-destructive, it was routine to control the performance of the developed passivating contacts after each process step.

Suns-Voc

The Suns-V_{oc} is a common technique to measure the photogenerated voltage of the metallized cells as a function of illumination light intensity — suns —. Similar to QSSPC method, the sample is exposed to a flash lamp that generates monotonically decaying illumination intensity, therefore a varying *quasi-Fermi level* splitting in the solar cell. The V_{oc} and illumination intensity are monitored by a voltmeter and a calibrated photodiode, respectively [Sinton 2000]. The current, J, is calculated considering a linear relationship between J_{sc} which is measured from light *J-V* and given as an input to the measurement system, and I_L — the relation is specified in previous section. With these inputs, a pseudo *J-V* curve can be plotted and pseudo-V_{oc} and pseudo-*FF* values can be extracted. As the measurements are performed in open-circuit condition, there is no current flow across the cell. Consequently, the pseudo *J-V*

curve is free of transport related losses such as the contribution of the series resistance (R_s), however it is sensitive to shunts. One possible way to determine the R_s of the solar cell is to extract the voltage difference (ΔV) between the standard light J-V curve measured at one sun and pseudo J-V curve measured with suns-V_{oc} at the maximum power point of the light J-V. With that, R_s can be deduced from the ratio of ΔV and J_{mpp} [Pysch 2007]. Additionally, it has been shown that suns-V_{oc} measurements at very high illuminations can be used to probe the presence of a parasitic Schottky diodes which reveals itself with a turn-over above a certain illumination level [Glunz 2007], [Bivour 2013].

Current-voltage measurement

The most fundamental technique to determine the solar cell performance is to measure its current-voltage (J-V) characteristic under standard test conditions (STC). These conditions are specified as a cell temperature of 25 °C and an irradiance of 100 mW/cm^2 — one sun — with an air mass 1.5 (AM1.5G, corresponding to spectrum where the sun is about 41° above the horizon). This measurement is also called light J-V and enables to assess the cell parameters, i.e. energy-conversion efficiency, short-circuit current (J_{sc}), open-circuit voltage (V_{oc}) and fill factor (FF). The physical meanings of these parameters are given in Chapter 1. Practically, these parameters are measured by illuminating the solar cell and sweeping the voltage in a given range (typically −0.1 to 0.8 V) with a sourcemeter (Keithley-2601A) while recording the generated electrical current simultaneously.

In this work, a Wacom WXS-90S-5,AM1.5G class AAA solar simulator which comprises xenon

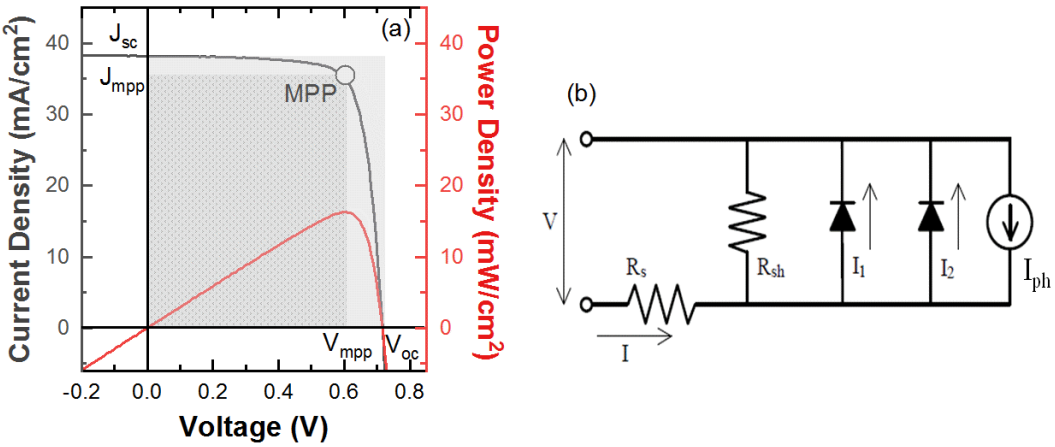

Figure 2.4 – (a) Typical one-sun J-V curve — grey — and power density curve — red — with corresponding cell parameters. (b) Equivalent circuit model of solar cell using two-diode model [McIntosh 2001].

and a halogen lamps to respectively cover the blue and red part of the solar spectrum, is used as an illumination source. Additionally, some filters are integrated to the system to mimic the solar spectrum more precisely. Prior to measurements, a reference measurement is carried out with a calibration cell and the J_{sc} of the tested device is corrected accordingly. Following the calibration step, the cell is placed on a temperature-controllable vacuum chuck coated with gold. A shadow mask is aligned to the cell area to avoid illumination of the entire wafer. The chuck temperature is controlled with Peltier elements cooled by a water chiller. The rear contacting is realized through the conductive chuck while for the front side contacting, probes are placed on the busbars. To avoid any possible contribution from the probe resistances, a four-probe configuration is employed. Figure 2.4(a) shows a typical light *J-V* curve together with corresponding cell parameters. A solar cell can be described as a current generating diode and its equivalent circuit with a two-diode model is depicted in Figure 2.4(b). More detailed information about the working principle and two-diode model can be found in Chapter 1.

External and Internal Quantum Efficiency

The external quantum efficiency (EQE) is the ratio of the number of collected charge carriers in the solar cell to the number of incident photons at a given wavelength (λ). It is a significant term that reveals how efficiently a solar cell can convert the photons to the photogenerated carriers and how efficiently they can be collected. The measurement is carried out by illuminating the solar cell with a monochromatic light source and by measuring the photo-current I_{ph} generated by the solar cell. The photon flow is usually determined by measuring the EQE of a calibrated photodiode under the same light source. In general, the shape of the EQE curve is determined by optical and electrical losses such as reflection, parasitic absorption and recombination losses. The photons with high energies are absorbed in the first few nm — depending on the optical properties of the front layer — in the solar cell, thus the blue part of the spectrum gives information on losses at the front side of the cell. Photons with low energies can travel through the cell and bounce back and forth between the rear and front before being absorbed or re-emitted. This part of the spectrum can thus provide information on losses originated from both the front and rear side of the cell. By performing the EQE measurement in short circuit condition, the photocurrent density $J_{sc|EQE}$ can be determined more accurately compared to standard one-sun light *J-V* measurement, with the following relation:

$$J_{sc|EQE} = -q \int_{\lambda_1}^{\lambda_2} EQE(\lambda) \Phi_{ph,\lambda}^{AM1.5} d\lambda \tag{2.8}$$

Here, $\Phi_{ph,\lambda}$ is the spectral photon flux and q is the elementary charge. For c-Si based solar cells, the spectral region of interest extends from 310 to 1200 nm. At higher wavelengths, photon energies are lower than the bandgap of the c-Si absorber and therefore can no longer be absorbed. Assessment of the J_{sc} with EQE measurement has an advantage of being independent of the spectral shape of the used light source. The current losses in the solar cell can

be studied more in detail by determining the internal quantum efficiency (IQE) as it permits to examine the collection of the photogenerated charge carriers by excluding the reflectance (R) losses. The IQE can be deduced from the EQE using the following relation:

$$IQE(\lambda) = \frac{EQE(\lambda)}{1 - R(\lambda)} \tag{2.9}$$

The IQE is defined as the ratio of the number of collected charge carriers over the number of photons that is absorbed by the cell. This helps to identify the losses apart from the reflection such as collection losses and parasitic absorption. Equation 2.9 shows that the extraction of the IEQ required the reflectance of the solar cell. In this work, IQE-SCAN (pv-tools) and a built in-house setup are used for the measurements. The pv-tool system uses a white halogen light source which is monochromated and chopped with a frequency of 230 Hz. The spot area is 2 cm × 2 cm. The cell is connected to a chuck at the rear and electric probe is placed at the front in order to measure the generated current under the illumination at various wavelengths. Following that, R can be measured from the same region by placing an integrating sphere on top of the illuminated area. The in-house built setup is based on a Horiba micro HR grating monochromator allowing a spectral range from 310 to 1200 nm and white halogen light source. In this system the illumination spot area is 1 mm × 2 mm which enables to perform the measurement by focusing between two fingers of the front grid. More information about in-house built setup can be found in previous works [Stueckelberger 2014], [Geissbühler 2015a]. The reflectance and transmittance spectra of the solar cells are measured using a PerkinElmer Lambda900 UV-Vis-IR spectrometer.

3 Low thermal budget: Microcrystalline silicon carrier-selective contacts

Summary

In this chapter, we investigate the potential of doped microcrystalline(μc-Si:H) layers as an alternative carrier-selective contact for silicon heterojunction solar cells. We show that the replacement of doped amorphous silicon with μc-Si:H is beneficial for device performance. Optically, we observe an improved J_{sc} when they are applied to the front side. Electrically, we observe a lower contact resistivity, as well as higher *FF* values. The cell parameter analysis, performed in a temperature range from −100 to +80 °C, reveals that the use of a hole-collecting μc-Si:H(*p*) layer suppresses the transport barrier, maintaining *FF* values in the range of 70 % at −100 °C, whereas it drops to 40 % for the standard amorphous doped layers investigated here. The same analysis also reveals a saturation onset of the V_{oc} at −100 °C in case of using doped μc-Si:H layers, whereas with doped amorphous layers a saturation onset is observed at −60 °C. These findings hint at a reduced importance of the parasitic Schottky barrier at the interface between the transparent electrodes and the selective contact in the case of μc-Si:H layer implementation. In the final part, we combine a μc-Si:H(*n*) rear contact with a molybdenum oxide hole-selective front contact. The front metallization is realized with copper plating, a *FF* of up to 80 % and efficiency of up to 22.5 % are demonstrated.

This chapter is partially based on a paper published in *IEEE Journal of Photovoltaics* and reproduced with permission from [Nogay 2016a].

3.1 Introduction and motivation

Silicon heterojunction (SHJ) solar cells have drawn significant attention in recent years thanks to their high power-conversion efficiencies and low temperature coefficient [Ballif 2014],

[De Wolf 2012a]. These devices use c-Si wafers as optical absorbers, while the device fabrication procedure relies largely on thin-film deposition technology at low temperatures, offering a flexible platform for new device architectures. In this context, Kaneka reported a world-record efficiency of 26.7 % for a single-junction c-Si–based solar cell, using SHJ contacts in an interdigitated back contact (IBC) design in 2017 [Yamamoto 2017]. This architecture enables maximal light coupling into the wafer by eliminating the front metal grid shadowing and by minimizing parasitic absorption at the front. However, it can require sophisticated masking processes during device fabrication to integrate both electron and hole contacts at the rear side of the cell. In a simpler implementation, pioneered by Sanyo (now Panasonic), SHJ solar cells feature electron and hole collectors at opposite sides of the wafer [Tanaka 1992]. With this design, Kaneka achieved a 25.1 % conversion efficiency for a similar large-area device, evidencing that the simplicity of this architecture can come at an acceptable efficiency penalty compared to its IBC counterpart [Adachi 2015].

Standard SHJ solar cells usually employ doped a-Si:H layers as carrier-selective contacts, overlaying the intrinsic a-Si:H layer that provides quasi-perfect chemical passivation to the wafer interface [Olibet 2007], [De Wolf 2012b]. The performance of the solar cell strongly depends on the net doping concentration of these carrier-selective layers. Ideally, it should be sufficiently high in order to:

- Introduce band bending in the c-Si wafer, creating the incentive for selective carrier collection. For the junction-forming contact, e.g. the *p*-type contact on *n*-type wafers, the doping concentration should ideally be strong enough to pull the surface of the wafer into inversion, effectively resulting in a buried homojunction.
- Support low contact resistivity and good charge-carrier transport to the overlaying TCO providing a decreased work function mismatch [Bivour 2012], [Tomasi 2014]. Otherwise, the insufficiently doped contact layer becomes partially depleted by the degenerately doped overlaying TCO.

However, high doping cannot be achieved with a-Si:H layers, since introducing too much dopant in the layers would also introduce additional defects that counteract the effective doping of a-Si:H layers [Street 1985]. High defect densities render the doped layers in SHJ devices "*dead*" from a carrier-collection perspective, since most of the carriers generated in these layers will not be collected, causing a loss in short-circuit current density (J_{sc}) [Holman 2012]. Additionally, defects generated within the doped layer can detrimentally affect the passivation of the c-Si wafer interfaces, even in the presence of intrinsic buffer layers [De Wolf 2009], [Schulze 2011]. These factors create a trade–off between fill factor (*FF*) and open-circuit voltage (V_{oc}) in standard SHJ devices. A possible way to tackle this problem is to replace the doped a-Si:H layers with transparent high work function materials, such as molybdenum oxide (MoO_x) [Battaglia 2014], [Geissbühler 2015b], [Bullock 2016]. Alternatively, they can also be replaced with silicon-based mixed-phase variations that have a higher doping efficiency compared to a-Si:H,and superior processing resilience and stability compared to most

transparent high work function materials explored so far [Ding 2012], [Ghahfarokhi 2014], [Seif 2014], [Mazzarella 2015], [Watahiki 2015]. In this context, the motivation of this work is to investigate the implementation of hydrogenated microcrystalline (μc-Si:H) layers to the SHJ cell structure. Compared to their a-Si:H counterparts, a key benefit of μc-Si:H layers is their higher doping efficiency thanks to the crystalline phase. μc-Si:H layers also have a lower absorption coefficient throughout the visible range of the spectrum; therefore, replacing the front a-Si:H collection layer with μc-Si:H can potentially provide an additional gain in J_{sc}.

3.2 Experimental details

For the experiments presented in this chapter, we used 250-μm-thick *n*-type float-zone <100> c-Si wafers with a resistivity of 3 Ω cm. They were textured in potassium hydroxide, chemically cleaned and dipped in 5 % diluted HF to remove native oxide right before starting the solar cell production process. Subsequently, 5- to 6-nm-thick intrinsic a-Si:H passivation layers were deposited using a parallel-plate plasma-enhanced chemical vapor deposition (PECVD) system operated at 40.86 MHz with silane (SiH_4) and hydrogen (H_2) as process gases. Further details can be found in [Descoeudres 2011a]. The substrate temperature was fixed at 200 °C for a-Si:H layer depositions. The dimensions of the reactor are 15 cm × 16 cm for the electrode area and 15 mm for the inter electrode gap. Following deposition of the symmetric passivation layers, carrier-selective contact layers were deposited. As a hole-selective contact, either a-Si:H(*p*) or μc-Si:H(*p*) was deposited by adding trimethylboron (TMB) to the process gases. For an electron-selective contact, either a-Si:H(*n*) or μc-Si:H(*n*) was deposited by adding phosphine (PH_3) to the process gases. In line with our earlier investigation on the growth of very thin μc-Si:H layers [Seif 2015a] [Seif 2016], the substrate temperature was reduced to 180 °C and the excitation frequency was set to 13.56 MHz. An improved trade–off between the deposition rate and film crystallinity was found by using high pressure (> 5 mbar) and relatively high power density (0.21 W/cm^2), resulting in rates of 0.049 nm/s for μc-Si:H(*p*) and 0.024 nm/s for μc-Si:H(*n*). Prior to deposition of the doped μc-Si:H layer, a thin intrinsic μc-Si:H was introduced as a nucleation layer to subsequently initiate the growth of the highly crystalline doped μc-Si:H layer. For this nucleation layer, identical deposition conditions as for the doped layers were used, but the dopant gases were omitted. To extract the collected carriers efficiently and increase the light in-coupling in the wafer, 70- and 200-nm-thick indium tin oxide (ITO) layers were sputtered onto the front and rear sides of the cells, respectively. The solar cell size was determined by depositing the ITO layers through a 2.2 cm × 2.2 cm shadow mask. A silver reflector/contact was sputtered onto the rear side and silver paste was screen-printed to realize the front metallization grid, followed by curing for 25 minutes at 190 °C on a belt furnace under ambient atmosphere.

For thickness and crystallinity determination, the deposited layers were characterized using spectroscopic ellipsometry (SE, HORIBA Jobin Yvon, UVISEL), using a fitting model explained in [Wernerus 2014]. The layer crystallinity was also measured by Raman spectroscopy using a 325 nm UV laser that has a collection depth of 10 nm in c-Si. The surface passivation properties

were investigated by the quasi-steady-state photoconductance (QSSPC) technique, giving access to the effective minority-carrier lifetime at different excess minority-carrier densities, and the resulting implied open-circuit voltage (iV_{oc}) values [Sinton 1996a]. The transfer length measurement (TLM) technique with contact pads array with variable distances was applied to extract the specific contact resistivity values using *in-situ* shadow masking for sputtering the contact pads [Berger 1972]. Additionally, the temperature dependence of the contact resistivity for both *p*- and *n*-type contact layers was measured in the temperature range from 10 to 80 °C.

Ambient temperature current voltage (*J*-*V*) characteristics of the cells were measured with a source meter (Keithley-2601A), using an AAA solar simulator (Wacom) calibrated to 100 mW cm^{-2} illumination. For temperature-dependent *J*-*V* measurements, a hybrid light-emitting diode (LED)–halogen lamp solar simulator built in house with a temperature-controllable chuck was used in the temperature range from −100 to +80 °C. LEDs with different colors were used to cover the blue-green part while halogen lamps were used to cover the red/infrared part of the solar spectrum. Finally, the cell parameters were monitored over the full temperature range. Detailed information about the temperature-dependent *J*-*V* measurement setup can be found in [Riesen 2016].

3.3 Microstructural analysis

The microstructure of c-Si(*n*)/a-Si:H/μc-Si:H(*p*) and c-Si(*n*)/a-Si:H/μc-Si:H(*n*) stacks were investigated using high resolution transmission electron microscopy (HRTEM) performed in a Cs-corrected FEI Titan Themis microscope operated at 200 kV with a beam current of about 100 pA. The TEM samples were prepared using a focused ion beam (FIB) lift-off technique in a Zeiss Nvision 40 with a final ion milling at acceleration voltage of 2 kV to reduce Ga-induced surface damage. For this investigation double side mechanically polished <111> oriented

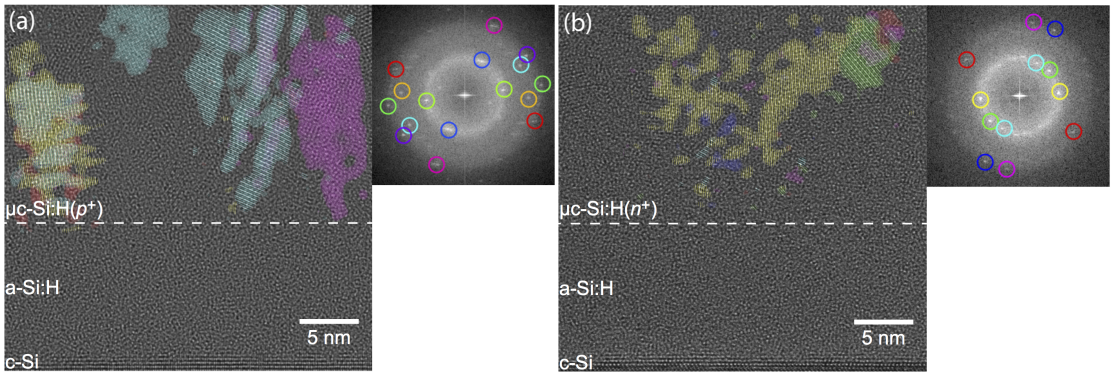

Figure 3.1 – High-resolution TEM micrographs of (a) c-Si/a-Si:H/μc-Si:H(*p*) and (b) c-Si/a-Si:H/μc-Si:H(*n*) stacks along with corresponding Fourier transforms and colored inverse Fourier transforms of the μc-Si:H layers (computed from regions above the dashed lines) from selected reflections. Adapted with permission from [Nogay 2016a]. Copyright ©2016, IEEE.

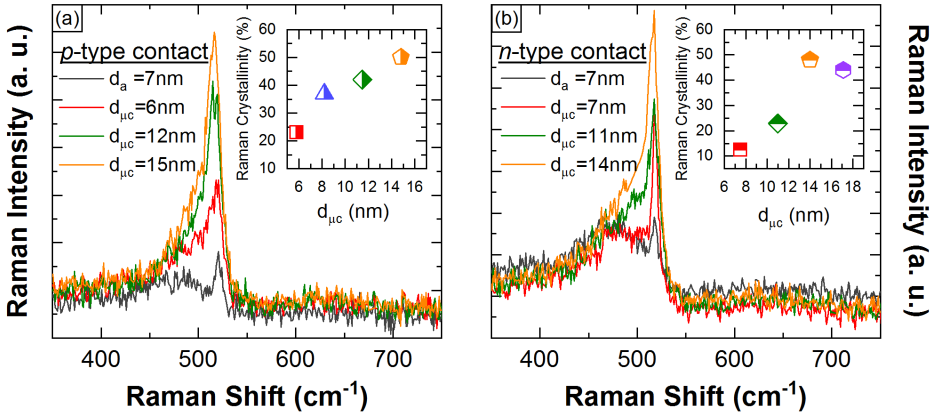

Figure 3.2 – Raman spectra of the (a) hole-selective *p*-contact and (b) electron-selective *n*-contact for different thicknesses on random pyramids. Insets calculated Raman crystallinity as a function of μc-Si:H layer thicknesses ($d_{\mu c}$).

n-type c-Si wafers are used. As in the case of using textured wafers, the interfaces would not be edge-on — parallel to the electron beam — and the different layers might artificially overlap in the projected image. This would unduly complicate the interpretation of the results.

HRTEM micrographs and related colored inverse Fourier transforms of the selected reflections for the doped microcrystalline layers grown on intrinsic a-Si:H layer are shown in Figure 3.1. It is observed that for both *p*- and *n*-type layers microcrytalline growth is initiated in the first nm and than the crystalline fraction gradually increases along the growth direction. In parallel to that, the larger ensembles of crystalites with identical orientation develop a conical characteristic within the amorphous matrix. It was previously reported by Vetterl *et. al.* that the growth of μc-Si:H layers starts from nucleation centers at the layer-substrate interface and that the diameter of crystalline grains increases with thickness, leading to the conical grain shape as observed in Figure 3.1 [Vetterl 2000]. Consequently, these micrographs reveal that the developed layers show decent crystalline fraction despite the fact that they are fairly thin.

In order to verify the trend of increased crystalline fraction with μc-Si:H layer thickness observed in HRTEM micrographs, Raman spectroscopy measurements were performed. For this analysis textured wafers with approximately 5-nm-thick a-Si:H(*i*) passivation layer were used as substrate and doped layers were deposited on top to mimic the real SHJ cell structure. Figure 3.2(a) reveals the Raman spectra of the μc-Si:H(*p*) layer for different thicknesses indicated by $d_{\mu c}$ together with reference a-Si:H(*p*) layer indicated by d_a. The inset of Figure 3.2(a) presents the calculated Raman crystallinity as a function of $d_{\mu c}$. Even though a 325 nm UV laser is used to limit the laser penetration into the c-Si wafer, the Raman spectrum of the 7-nm-thick a-Si:H(*p*) layer shows a small shoulder appearing at 521 cm^{-1} which indicates a contribution from the c-Si wafer. Since this sample is fully amorphous, only one

peak positioned at 480 cm^{-1} is expected. For the μc-Si:H(p) layer a clear trend of increased crystalline fraction with $d_{\mu c}$ is visible which is in line with the conclusion drawn from HRTEM micrograph shown in Figure 3.1(a). Figure 3.2(b) shows Raman spectra of the μc-Si:H(n) layer for different thicknesses together with a reference a-Si:H(n) layer. In the inset of the Figure 3.2(b) calculated Raman crystallinity as a function of $d_{\mu c}$ is presented. Crystallinity is also increasing with μc-Si:H(n) layer thickness which is also in line with the HRTEM micrograph shown in Figure 3.1(b).

3.4 Electrical properties

In the following, we investigate the benefits of the increased net doping associated with μc-Si:H layers, compared to their a-Si:H counterparts. For this, we study the specific contact resistivity (ρ_c) of full electron- and hole-selective contact structures including the TCO. In order to clarify the effect of the crystallinity as well as the doping, the thickness of the μc-Si:H contact layers was altered in a wide range. For the electron-selective contact, the investigations were preformed using textured n-type c-Si wafers as a base, whereas for hole-selective contact textured p-type c-Si wafers were used in order to have high-low junctions rather than p-n junctions. The samples used here feature a-Si:H passivation layers on both sides, followed by the contact structure on one side only *i.e.* "a-Si:H/ n-type c-Si wafer / a-Si:H/ μc-Si:H(n) [or a-Si:H(n)] /ITO /Ag" and "a-Si:H/ p-type c-Si wafer / a-Si:H/ μc-Si:H(p) [or a-Si:H(p)] /ITO /Ag" that mimics the structure used in the real devices. The samples were annealed at 190 °C for 25 minutes before the characterization to imitate the curing which is necessary after screen printing of the front Ag grids.

Measured ρ_c values as a function of μc-Si:H(p) layer thickness — on random pyramid textured wafer — together with reference sample that employs 7.2-nm-thick a-Si:H(p) is shown in Figure 3.3(a). Extremely high ρ_c value of 3.65 Ω cm^2 is observed for the 6-nm-thick μc-Si:H(p) layer. For 8-nm-thick μc-Si:H(p) layer, the ρ_c is almost equal to the reference a-Si:H(p) case. With increasing μc-Si:H(p) thickness, the ρ_c is decreasing further, presumably due to enhanced doping efficiency as the layer develops more crystalline nature. Consequently, if the μc-Si:H(p) layer is thicker than 8 nm, it outperforms the a-Si:H(p) electrically by exhibiting ρ_c as low as 0.4 Ω cm^2.

Figure 3.3(b) exhibits the measured ρ_c values as a function of μc-Si:H(n) layer thickness — on random pyramid textured wafer — together with reference sample that employs 7.5-nm-thick a-Si:H(n). The same general trend of lower ρ_c with increasing μc-Si:H(n) thickness is also evident for electron-selective μc-Si:H contacts. For the thickness of 7.5 nm, μc-Si:H(n) represents much higher ρ_c of 0.7 Ω cm^2 compared to its a-Si:H counterpart. However; if the μc-Si:H(n) layer is thicker than 8–9 nm, it outperforms the a-Si:H(n) electrically by exhibiting ρ_c as low as 0.03 Ω cm^2. Overall, these measurements confirm that it is possible to improve the electrical performance of the SHJ devices if the optimum thickness of the μc-Si:H is integrated to the cells as a carrier-selective contact. A tentative interpretation for the lower ρ_c with

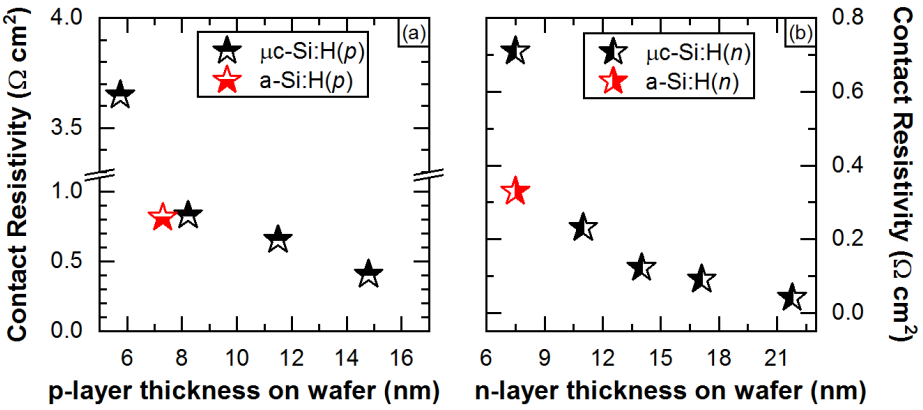

Figure 3.3 – Contact resistivity values measured with TLM method as a function of (a) μc-Si:H(p) and (b) μc-Si:H(n) layers thicknesses together with reference a-Si:H doped layer for both contacts.

increased thickness can thus be improved crystallization as well as the doping efficiency. A better doping efficiency leads to narrower barrier width at the interface between the doped contact layer and the TCO which facilitates the tunneling of the charge carriers.

To understand the above mentioned phenomenon of narrower barrier width with higher doping concentration in detail, we studied the temperature dependence of the ρ_c values for different contacts. To that end, we prepared and compared following sample structures in the temperature range of 10 to 80 °C *i.e.* "n-type c-Si wafer / a-Si:H/ 7-nm-thick a-Si:H(n) vs. n-type c-Si wafer / a-Si:H / 16-nm-thick μc-Si:H(n)" and "p-type c-Si wafer / a-Si:H / 7-nm-thick a-Si:H(p) vs. p-type c-Si wafer / a-Si:H / 13-nm-thick μc-Si:H(p) layer stacks, each time capped with the same ITO/Ag as an overlayer and annealed at 190 °C for 25 minutes. For clarity, we refer to them as a-Si:H and μc-Si:H stacks, respectively, and denote their associated ρ_c values as ρ_{c-a} and $\rho_{c-\mu c}$ hereinafter.

The results for the temperature range from 10 to 80 °C are given in Figure 3.4(a) for the electron-selective contact on c-Si(n) wafer. They show a clear differences between ρ_{c-a} and $\rho_{c-\mu c}$. At room temperature $\rho_{c-\mu c}(n)$ is eight times lower with respect to $\rho_{c-a}(n)$, representing a tremendous gain. By plotting the respective conductance — inverse contact resistivity — of the samples for each temperature in an Arrhenius plot we can extract the activation energies E_a of the contact resistance. For the μc-Si:H stack a value of E_a = 0.077 eV is obtained which is much smaller than E_a = 0.284 eV measured for a-Si:H stack. The $\rho_{c-a}(n)$ significantly decreases with temperature, whereas for $\rho_{c-a}(n)$ the temperature effect is much less pronounced, indicating that efficient temperature-independent tunnelling transport occurs in case of the μc-Si:H/ITO/Ag stack, whereas carrier transport across the a-Si:H/ITO/Ag stack features a large thermionic component. The necessity of having an additional thermionic component indicates the existence of an upward band bending at the doped layer and TCO interface,

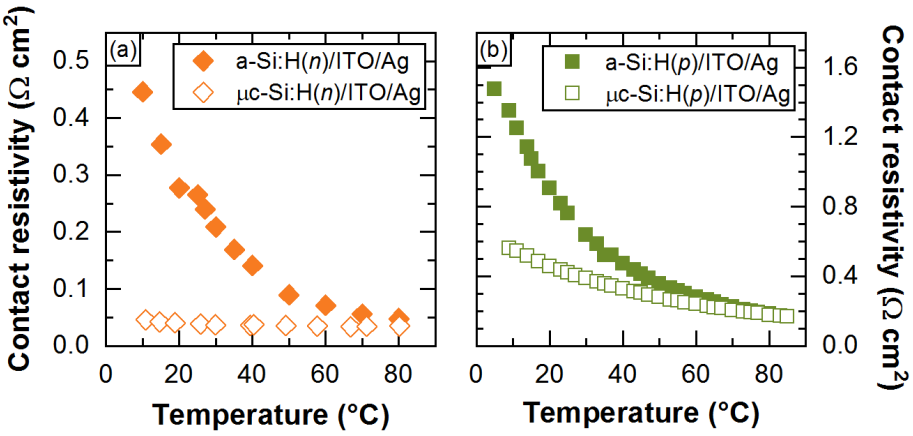

Figure 3.4 – Temperature-dependent contact resistivity values for a-Si:H (filled symbols) and μc-Si:H layer (open symbols) for (a) electron contact and (b) hole contact. Adapted with permission from [Nogay 2016a]. Copyright ©2016, IEEE.

creating a transport barrier for electrons. Generally, an upward band bending at the interface between two materials can be caused either by interfacial Fermi level pinning or by a TCO work function which — in the case of an electron contact — is higher than the work function of the doped layer. For most metal semiconductor interfaces, the Fermi-level is strongly pinned at the interfaces. In such a case the barrier height does not depend on the doping concentration within the semiconductor; however, the opposite is true for the barrier width (i.e. depletion width), [Schroder 2006] where the higher the doping concentration, the narrower the space charge region and the barrier width becomes. Therefore, in the case of the a-Si:H/ITO/Ag stack, the transport mechanism through the barrier at the interface between a-Si:H and TCO is dominated by thermionic field emission which requires thermally excited carriers either to reach the energy level at which the barrier is sufficiently narrow for tunnelling, or to overcome the barrier completely. When the semiconductor is highly doped, that barrier becomes sufficiently narrow near the conduction band edge which enables electrons to tunnel through directly. Hence, our temperature-dependent observations suggest that when μc-Si:H(n) layers are applied as an electron collector, tunnelling becomes the dominant transport mechanism.

Figure 3.4(b) shows the temperature-dependent contact resistivity measurement for the hole-selective contact that is deposited on p-type c-Si wafer with intrinsic a-Si:H passivation layer on top. A similar, but less pronounced, temperature behaviour is visible also when a-Si:H(p) is compared with μc-Si:H(p). At room temperature $\rho_{c-\mu c}(p)$ is two times lower than $\rho_{c-a}(p)$ which represents an important gain.

In overall, we conclude that for electron- as well as hole-selective μc-Si:H contacts, the charge-carrier transport is dominated by a temperature-independent tunnelling mechanism instead of thermionic emission which is the dominant charge-carrier transport mechanism in the case of using doped a-Si:H layer as a carrier-selective contact.

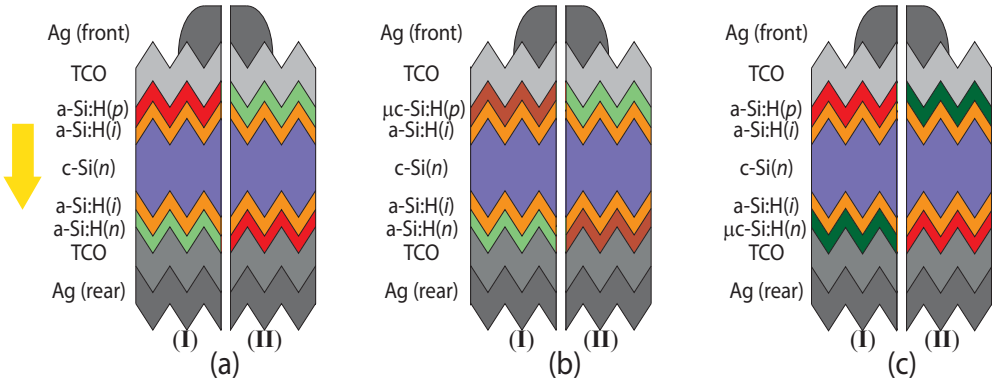

Figure 3.5 – The arrow indicates the direction of the incident light coming to the cell; (a) is the standard SHJ cell with a-Si:H doped layers, (b) modified cell with μc-Si:H layer for hole collection, (c) modified cell with μc-Si:H layer for electron collection. (**I**) indicates the front hole collection, (**II**) indicates the rear hole collection scheme. Adapted with permission from [Nogay 2016a]. Copyright ©2016, IEEE.

3.5 Integration into SHJ solar cells

In this section the differences between a-Si:H and μc-Si:H carrier-selective contacts applied to the SHJ solar cell structures are discussed. Throughout our experiments, we fabricated one of the carrier-selective contact from doped μc-Si:H, while keeping all other layers as in our standard SHJ device to unambiguously investigate the potential of μc-Si:H layer as a hole- and electron-selective contact separately. Sketches of the device structures realized during this investigation are depicted in Figure 3.5.

3.5.1 Microcrystalline silicon as a hole-selective front contact

This section is devoted to investigate and analyse the differences between an a-Si:H and a μc-Si:H hole-selective contact layer applied to the standard SHJ solar cell configuration. To that end, we produced SHJ cells with different thicknesses of either a-Si:H(p) [Figure 3.5(a) **I**] or μc-Si:H(p) [Figure 3.5(b) **I**] layers at the front side. The thicknesses of the layers were extracted by fitting SE data of the reference samples deposited on glass substrates. The obtained values were divided by a factor of 1.7 to estimate the thicknesses on the random pyramid textured wafers.

Figure 3.6(a) shows that V_{oc} is not affected in the thickness range investigated here, which is consistent with previous reports [Fujiwara 2007b] [Holman 2012]. Figure 3.6(b) shows that the slope of J_{sc} values as a function of p-layer thickness is 1.6 times steeper for the a-Si:H layers (-0.08 mA cm^{-2}/nm) than the slope obtained for the μc-Si:H layers (-0.05 mA cm^{-2}/nm). Thus, reducing the thickness of the μc-Si:H(p) layers down to the same 12-nm-thick a-Si:H(p) layers yields a J_{sc} gain up to 1.5 mA/cm^2 compared to a-Si:H(p). A similar gain has also been reported

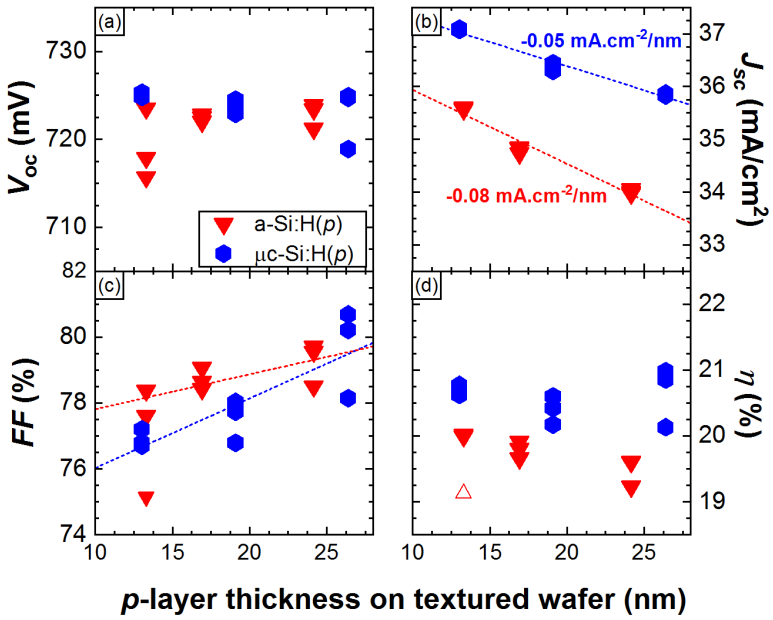

Figure 3.6 – The output characteristics of solar cells exhibiting different thicknesses of either a-Si:H(p) or μc-Si:H(p) layers at the front side. The lines are linear fits to the data. Adapted with permission from [Nogay 2016a]. Copyright ©2016, IEEE.

by Ghahfarokhi *et al.* on polished c-Si wafers, using μc-Si:H(p) layers [Ghahfarokhi 2014]. Furthermore, for the devices tested here, the *FF* values increase with the thicknesses of the μc-Si:H(p) layer due to the enhanced crystallinity of thicker p-layers. The Raman crystallinity of the layers increases from 39 to 48 % for 13- to 26-nm-thick layers, respectively. Since the crystalline phase is assumed to be doped more efficiently than the amorphous phase, increasing the thickness is leading to a lower contact resistivity to the TCO layer as it is also shown in Section 3.4 which results in higher *FF* values.

We also observe a slight increase in *FF* with increasing a-Si:H(p) layer thickness. Since all three samples have similar iV_{oc} and *iFF* values, we presume that this *FF* gain is not originating from better passivation due to the use of thicker layers. Holman *et al.* also observed a similar trend [Holman 2012]. One possible reason can be that increasing the doped layer thickness between ITO and the passivation layer favors the band bending inside the wafer, and thus the hole collection. According to Bivour *et al.*, the incentive of thin p-type layers to collect holes is strongly dependent on the work function at the TCO/a-Si:H(p) interface [Bivour 2013]. As a consequence, it is necessary to use either TCOs with high work function or contact layers above a given critical thickness in order to attain enough built-in potential and reach reasonable efficiencies [Haug 2012].

It is important to note that the a-Si:H(p) layer used in this work has a refractive index of 3.9

at 633 nm and dark conductivity of 2.46×10^{-6} 1/Ω cm which is slightly lower than typical values in the literature. This might indicate that the doping concentration of our standard a-Si:H layer is relatively low. Our μc-Si:H(p) layer has a refractive index of 3.4 at 633 nm which is close to reported values and dark conductivity of 0.34 1/Ω cm.

We conclude from this thickness series that doped μc-Si:H(p) layers may improve optical performance of SHJ devices by providing a gain in J_{sc}up to 1.5 mA/cm^2 due to the their higher transparency compared to a-Si:H(p) layers and that they improve the current extraction because of their better doping efficiency compared to a-Si:H(p) layers.

3.5.2 The effect of inverted device polarity

Another important design parameter for the simple both-sides-contacted SHJ device is its polarity *i.e.* the hole contact may be placed either at the front or rear of the device thanks to the process flexibility of SHJ technology [Descoeudres 2013]. Inspired by the promising results presented in previous Section 3.5.1, we investigated whether devices with inverted polarity may equally benefit from doped μc-Si:H layers at their front side [*i.e.* μc-Si:H(n)]. Prior to investigating the effect of front electron-selective contact replacement with μc-Si:H layer, we investigated the effect of inverted polarity by realizing fully amorphous reference cells. As mentioned before, traditionally the hole contact is placed at the front side of the SHJ solar cells [Taguchi 2000] [Taguchi 2014]. However according to the literature, inverting the polarity may have several advantages compared to classic SHJ design:

1. In general, carriers collected at the front of a solar cell need an efficient lateral transport towards the front metal grids. In SHJ cells, this is usually provided by the front transparent conductive oxide (TCO), which ideally needs to combine low sheet-resistance with minimal parasitic absorption. However, for a device collecting majority carriers at the front, the c-Si wafer can be used equally well as transport channel. Consequently, as most high-efficiency devices are fabricated from n-type c-Si wafers, a device that collects electrons at the front can significantly relax the requirements on the front TCO, enabling the use of materials with lower free-carrier density, and thus higher transparency in the near IR.

2. The surface passivation properties of the electron collecting a-Si:H *i/n* stack is usually superior to the hole collecting *i/p* stack, and can be more easily thinned down without much loss in passivation. Thus, the inverted polarity can contribute an additional gain in J_{sc}.

3. Window layers with wide bandgap can couple more light into the wafer. Electronically, opening the bandgap mainly results in increased valence band offsets, leaving the conduction band offsets largely unchanged. Therefore, in case of electron contacts, they can be integrated in the front side of the cell structure without incurring significant transport barriers to the charge carriers.

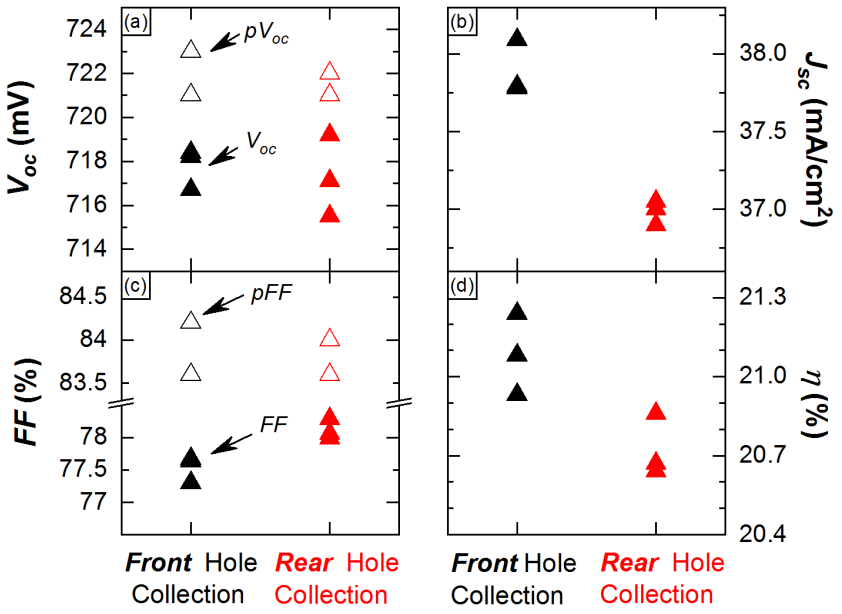

Figure 3.7 – Device parameters for two standard SHJ cell configurations (filled symbols); hole contact at the front or rear. Open symbols represent the pV_{oc} and *pFF* at one-sun. Adapted with permission from [Nogay 2016a]. Copyright ©2016, IEEE.

4. The electron mobility is approximately three times higher than the hole mobility within the c-Si wafer. Combined with the first argument, this offers an opportunity to increase the pitch of the metallic fingers at the front grids and to reduce shadowing losses originated from these front metal grids.

To confirm the above mentioned advantages, we first compare two standard SHJ cells with hole contact at the front and rear using exclusively a-Si:H doped layers [Figure 3.5(a) **I** and Figure 3.5(a) **II**].

The cell parameters of these two configurations are presented in Figure 3.7. It is observed that the V_{oc} is not affected significantly by the device polarity. Conversely, J_{sc} is lower in the case where holes are collected at the rear compared to standard design. This can be largely attributed to the fact that we used identical layer stacks in both device designs, meaning that electron-selective a-Si:H(*n*) layer was optimized by targeting the rear side while hole-selective a-Si:H(*p*) layer was optimized by targeting the front side of the SHJ cells. Consequently, from an optical perspective, the a-Si:H(*n*) layer is probably too thick to be used at the front side, leading to increased absorption and an associated loss in J_{sc} .

Remarkably, we observe approximately 1 % absolute gain in *FF* when the hole collecting layer is implemented at the rear side of the SHJ cells. Previously, Bivour *et al.* also reported the *FF*

gains for this polarity configuration and explained it with the existence of the additional lateral current path within the *n*-type c-Si wafer for the electron transport, which assists the lateral current transport of the front TCO [Bivour 2014b]. In our case, both cells have a *pFF* of 83.6 % which means that the difference in *FF* originates from series resistance losses. Additionally, the measured pV_{oc} values are in the range of 721 to 723 mV at one sun which indicates that the surface passivation is very similar for both polarities.

Overall, the conversion efficiency is dictated by the 1 mA/cm^2 loss in J_{sc} when the hole collecting layer is placed at the rear. However, most likely it can be fully overcome by simply thinning down the *i*/*n* stack or possibly replacing it with doped μc-Si:H layer.

3.5.3 Microcrystalline silicon as an electron-selective front contact

After confirming the fact that the inverted polarity design provides some advantages for the transport and *FF* parameter of the SHJ cells, we wanted to assess the potential of μc-Si:H(*n*) layers for this device polarity. Therefore we compare the cells with different thicknesses of either a-Si:H(*n*) [see Figure 3.1(a) **II**] or μc-Si:H(*n*) [see Figure 3.1(c) **II**] as electron collecting layers.

Figure 3.8(b) demonstrates that J_{sc} drops linearly with increasing thickness as it is also observed in section 3.5.1. This is a direct consequence of parasitic visible and UV light absorption. Notably the slope of the J_{sc} values as a function of the *n*-layer thickness is 1.8 times steeper for a-Si:H(*n*) layers (−0.11 mA cm^{-2}/nm) than the slope obtained for μc-Si:H(*n*) layers (−0.06 mA cm^{-2}/nm). This moderate slope means either better transparency or better collection efficiency in the sample that include μc-Si:H layers, or both. Consequently reducing the thickness of the μc-Si:H(*n*) layers to the same thickness as a-Si:H(*n*) layers would yield a J_{sc} gain of up to 1.2 mA/cm^2 for the 12-nm-thick *n*-layer.

Within the investigated range, there is no explicit trend for V_{oc} and *FF*, only the thinnest a-Si:H(*n*) provides lower V_{oc} value compared to other cells [see Figure 3.8(a)]. This may be related to the fact that we are close to the critical thickness necessary for adequate surface passivation. It was reported that if the thickness of the a-Si:H(*n*) is smaller than a critical value, then photoconductive decay lifetime measurements yield low effective minority carrier lifetimes, indicating the recombination losses due to reduced field effect passivation [Tomasi 2016b]. Overall, the performance of the SHJ devices is dominated by the decrease in J_{sc} associated with the increased layer thickness.

From the obtained results in here and in section 3.5.1, we conclude that there is a clear optical profit of having doped μc-Si:H layers as a carrier selective contact, rather than doped a-Si:H at the front of SHJ cells, irrespective of their precise polarity.

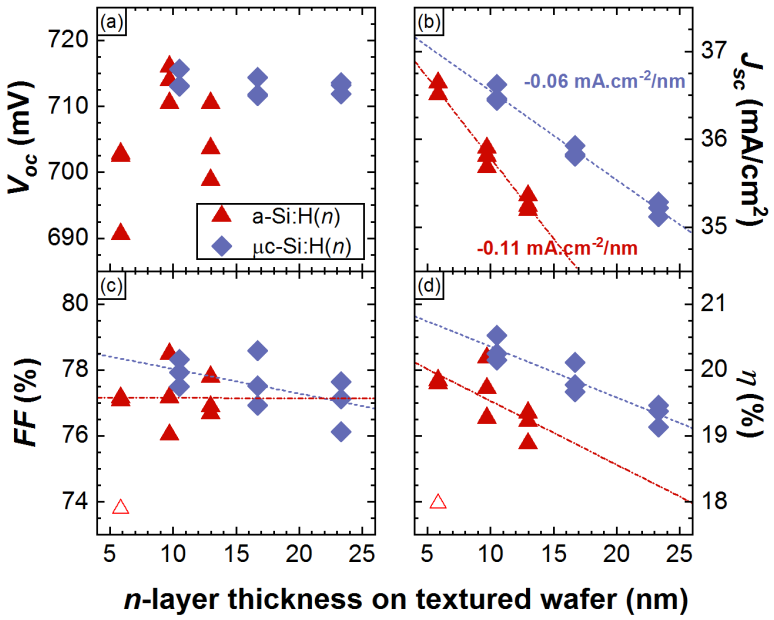

Figure 3.8 – The output characteristics of solar cells exhibiting different thicknesses of either a-Si:H(n) or μc-Si:H(n) layers at the front side. The lines are linear fits to the data and the open symbols were excluded from the fit. Adapted with permission from [Nogay 2016a]. Copyright ©2016, IEEE.

3.5.4 Optimized cell results

After verifying the optical and electrical benefit of the μc-Si:H layers separately, we implemented the optimized μc-Si:H layers into cell structures by keeping one of the contacts as an a-Si:H doped layer. The obtained cell parameters are shown in Table 3.1 for different cell structures.

Table 3.1 – Summary of the parameters for the SHJ solar cells with inverted polarity. Adapted with permission from [Nogay 2016a]. Copyright ©2016, IEEE.

Cell	V_{oc}[mV]	J_{sc}[mA/cm^2]	*FF*[%]	Efficiency [%]
Best reference cell	717	36.9	78.1	20.7
Ref cell from same run	717	36.7	77.3	20.3
Front side μc-Si:H(n)	719	37.1	78.4	20.9
Rear side μc-Si:H(p)	721	36.9	79.3	21.1

All the cells presented in this section have the hole contact at the rear side. Reference cells have a-Si:H(p) at the rear and a-Si:H(n) at the front as a contact layer, and reported values are averages of three 2 cm × 2 cm cells on the same wafer. It is also important to note that the

layer thicknesses are so far mainly optimized for the *FF* gain rather than for J_{sc} gain. For a-Si:H doped layers, the optimized thickness on textured surface was 7 nm; whereas, for μc-Si:H layers, it is 13 nm in order to obtain a sufficiently high crystallinity on the random pyramid textured wafers.

According to the measured cell parameters, replacing the a-Si:H doped layer with its μc-Si:H counterpart enables up to approximately 1.5 % relative *FF* gain compared to our best reference cell with this configuration and 2.6 % relative *FF* gain compared to the reference cell produced in the same run. We explain this gain by the lower contact resistivity associated with μc-Si:H collection layers as indicated in section 3.4. This is corroborated by the fact that the cells with doped μc-Si:H layers show lower R_s values of 1.01 and 0.83 Ω cm^2 for μc-Si:H(p) and μc-Si:H(n), respectively. On the other hand, the R_s of our best reference cell is 1.29 Ω cm^2. Notably, these promising results were achieved maintaining high V_{oc} values in excess of 720 mV and SHJ solar cells with good conversion efficiencies between 20.9 and 21.1 % were achieved.

3.5.5 Temperature dependency of the cell parameters

Finally, to investigate the dominant carrier transport mechanism in finished cells featuring either a-Si:H or μc-Si:H contacting layers in more detail, we performed temperature-dependent light *J-V* measurements from −100 °C up to +80 °C in order to probe the transport barrier that photogenerated carries may face during the collection across the different device interfaces.

The temperature dependence of the cell parameters is presented in Figure 3.9. Here, for standard SHJ cells, we observe that the *FF* slightly rises with decreasing temperatures in the temperature range of 25–80 °C, intriguingly assuming its maximum (FF_{max}) at about room temperature, and then decreases at lower temperatures down to 40 % as seen in Figure 3.9(a). The corresponding *J-V* curve reveals that this is related to the appearance of a strong *S*-shape at lower operating temperatures. Strikingly, the three different cell designs show very different trends in the low temperature range; when the electron collection side is replaced by μc-Si:H(n), the FF_{max} shifts to 0°C and the *FF* drops much less towards lower temperatures (65 % at −100 °C). Based on this observation, we conclude that the appearance of the *S*-shape can be "delayed" to lower temperature by the integration of a μc-Si:H(n) layer. In other words, the performance of devices featuring μc-Si:H(n) layers is superior at low temperatures, compared to that of devices featuring a-Si:H(n) layers. Similarly, after the replacement of the hole collection side by μc-Si:H(p) layer, the drop in *FF* at low temperature is further reduced (dropping to 70 % at −100 °C) with the FF_{max} at −40 °C.

Figure 3.9(b) shows that the J_{sc} increases linearly with raising temperature. Mainly because the bandgap shrinks with increasing temperature due to the fact that vibrations stretch the interatomic distance. Additionally, phonon assisted excitation as well as sub-gap absorption processes are enhanced in the red part of the solar spectrum [Bludau 1974], [Sin 1984], [Seif 2015b].

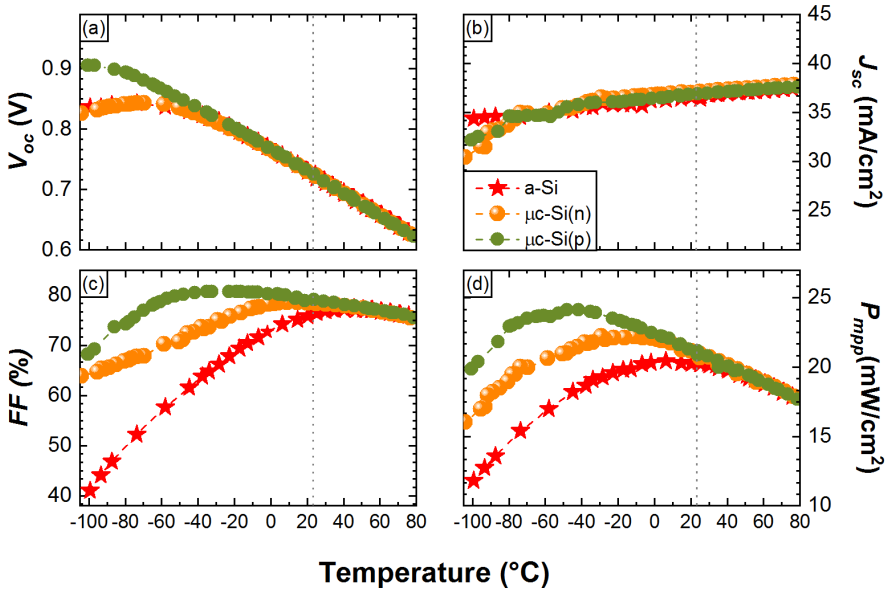

Figure 3.9 – Extracted cell parameters measured at different temperatures for three cells; (a) all a-Si:H SHJ solar cell — red stars —, (b) the cell with μc-Si:H(n) layer at the front — orange spheres —, and (c) the cell with μc-Si:H(p) layer at the rear — green circles. Adapted with permission from [Nogay 2016a]. Copyright ©2016, IEEE.

Figure 3.9(c) reveals that for the standard cell the V_{oc} continues to increase by lowering the temperature down to about −60 °C, where it then saturates. The V_{oc} of the cell that includes μc-Si:H(n) behaves very similarly to the reference cell, featuring a similar saturation effect at low temperatures. Considering now the data of the μc-Si:H(p) based devices, a first striking feature is that their saturation in V_{oc} at low temperatures occurs only at about −100 °C.

The fundamental *textbook* relation between V_{oc} and temperature (T) is explained by the direct dependence of the intrinsic carrier density (n_i) on T. With decreasing temperature, n_i decreases exponentially and the implied V_{oc} — varying logarithmically with n_i — increases linearly. However; to explain the observed low temperature behaviour of the V_{oc} and its saturation in particular, other effects such as charge accumulation [Rath 2012] and freeze-out of the carriers [Löper 2012] must be considered. Mikolasek *et al.* reported a similar low temperature behaviour of *FF* and V_{oc} parameters for standard SHJ cells that employ doped a-Si:H layers as carrier-selective contacts [Mikolášek 2017]. In their simulation study, they investigated the impact of the parasitic Schottky barrier at TCO/a-Si:H carrier-selective contact interface and the net doping of the selective contact on the behaviour of the V_{oc} at low temperatures. They reported a linear increase of V_{oc} with a decrease of temperature in the case when no Schottky barrier is present, *i.e.* an ideal Ohmic contact, and a shift of the V_{oc} saturation region to higher temperature with an increase of Schottky barrier and a

decrease of net doping. Their simulations support our findings cogently. Only for the cell with μc-Si:H(n) layer, it is not possible to see a difference in V_{oc} saturation with respect to the standard cell. Since the contact resistance of the TCO/μc-Si:H(n) interface is virtually temperature independent [c.f. (Figure3.4 (a))], we conclude that the behaviour of the cell is governed by the TCO/a-Si:H(p) contact.

Additionally, Bivour *et al.* investigated the effect of the net doping of the contact layers by exposing the SHJ cells to high illumination intensities at room temperature — to drive the contacts towards the high injection conditions — and probing the suns-V_{oc} [Bivour 2014a]. They observed that with increased doping, the V_{oc} loss at high illumination becomes less pronounced and they explained that with the suppressed Schottky barrier effect.

To sum up, this impressive variation of cell performances at extremely low temperatures confirms that it is possible to suppress the transport barrier effect that all standard a-Si:H SHJ cells are subject to. Transport becomes less temperature dependent when highly doped and conductive carrier-selective contact layers are used and carriers can overcome the barriers more easily by tunneling with a reduced thermionic component. This also results in higher *FF* values in the final SHJ solar cells.

3.5.6 Combination of microcrystalline rear electron contact with transition metal oxide front hole contact

In the previous sections we proved that both electron- and hole-selective μc-Si:H contact layers can lead to a notable optical gain. However, to be able to observe the benefit in electrical performance of the device, they need to be deposited above certain thicknesses. This requirement brings along a trade–off between J_{sc} and *FF* once the carrier-selective μc-Si:H contact layers are applied to front side of the SHJ solar cells. An alternative solution for front side application is using highly transparent transition metal oxides (TMOs) with appropriate work function as front layers, in particular hole-selective sub-stoichiometric molybdenum oxide (MoO_x, x < 3) with bandgap of ~ 3 eV [Battaglia 2014], [Geissbühler 2015a], [Bivour 2015]. In our laboratory it was already demonstrated that MoO_x based devices can have an improved optical response in the blue part of the spectrum and a promising *FF* value especially when they are combined with suitable Cu-plating front metallization [Geissbühler 2015b]. In this final part of the chapter, we present solar cells that combine a front hole-selective MoO_x layer[1] with a rear electron-selective μc-Si:H(n) contact to benefit from both the enhanced front transparency and improved rear contact resistivity which could lead to high efficiency solar cells with high J_{sc} and high *FF* while maintaining a decent V_{oc}.

The process flow for cell production started as described in Section 3.2 of this Chapter. After removing the native oxide with 5 % diluted HF solution, the a-Si:H(i) passivation layers were deposited on both side of the wafers in PECVD reactor. This was followed by the deposition

[1] The results presented in this section were obtained with the help of J. Geissbühler who performed the MoO_x deposition and Cu-plating. Contribution is gratefully acknowledged.

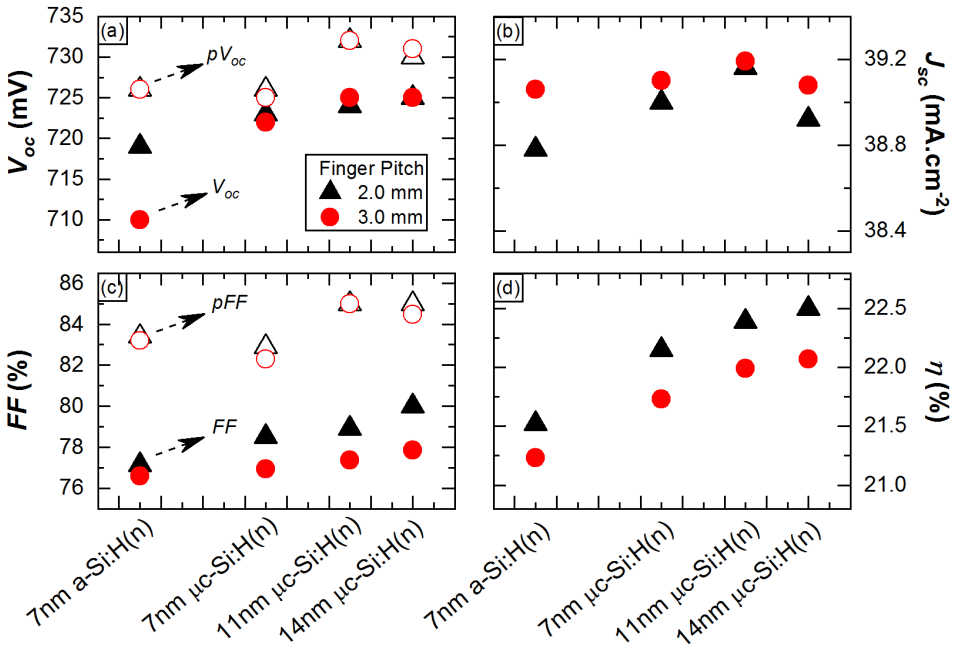

Figure 3.10 – Extracted parameters for the solar cells that employ the same MoO_x front hole contact and various rear electron contacts such as standard 7-nm-thick a-Si:H(n), 7-nm-thick μc-Si:H(n), 11-nm-thick μc-Si:H(n) and 14-nm-thick μc-Si:H(n) layers. Cu-plating is performed for front metallization using two different finger pitches.

of electron-selective rear contact layers of either a-Si:H(n) or μc-Si:H(n) with PECVD. Immediately after the PECVD step, the cells were transferred to a thermal evaporator in order to prevent surface oxide formation on the a-Si:H(i) passivation layer. Stoichiometric MoO_3 powder was used as source for thermal evaporation from a resistively heated molybdenum boat[2]. A deposition rate between 0.3 and 1 Å/s was used to grow approximately 7-nm-thick MoO_x layer. The thickness was measured by spectroscopic ellipsometry using reference layers grown on glass substrate. The obtained thickness was divided by a factor of 1.7 to estimate the thickness on wafers with random pyramid texture. Since MoO_x films are very sensitive to air exposure and temperature treatment [Irfan 2012], [Geissbühler 2015b], the cells were straightaway transferred to the sputtering tool to deposit the front TCO which consisits of an IO:H/ITO bilayer and the rear ITO/Ag stack [Barraud 2013]. Ultimately, the front sides of the cells were metallized using Cu-plating which shows better compatibility with MoO_x films as it does not require any thermal treatment. This metallization technique is also reducing significantly the finger width (~ 20 μm) compared to our standard screen-printing (~ 70–80 μm). Consequently, it reduces the optical front grid shadowing [Geissbühler 2014], which

[2]The results presented in this section were obtained with the help of J. Geissbühler who performed the MoO_x deposition and Cu-plating. Contribution is gratefully acknowledged.

would yield an additional J_{sc} gain for the finished cell[3].

The obtained parameters for the SHJ solar cells that employ the same MoO_x hole-selective front contact and various electron-selective rear contacts are shown in Figure 3.10. For comparison, one cell is prepared with 7-nm-thick a-Si:H(*n*) rear contact while for the other three cells the μc-Si:H(*n*) rear contact layer thickness is varied from 7 to 14 nm. Two different finger pitches of 2 and 3 mm are used during the Cu-plating for front metallization. More detailed information on the Cu-plating process can be found in [Geissbühler 2015a]

Figure 3.10(a) shows that in general the V_{oc} of the cells that employ rear μc-Si:H(*n*) layers is higher than the standard a-Si:H(*n*) counterpart. Besides, the V_{oc} is improving with increased μc-Si:H(*n*) thickness. The same V_{oc} trend is visible for both finger pitches. A possible explanation for this trend can be the fact that as the μc-Si:H(*n*) deposition recipe is highly hydrogen rich, more hydrogen can reach the a-Si:H(*i*) passivation layer and strengthen the surface passivation with increased plasma exposure time. Figure 3.10(b) shows that the obtained J_{sc} values are around 39 mA/cm^2 for all cells, the finger pitch of 3 mm yields an additional gain in J_{sc} because of lower shading losses. If we compare this design with the reference that has a fully amorphous front hole and a screen printed Ag front metallization (c.f. Section 3.5.2), it provides a substantial gain in J_{sc} ca. 1 mA/cm^2. In addition, a remarkable gain in *FF* is observed when the a-Si:H(*n*) rear side is replaced with μc-Si:H(*n*), especially for the 14-nm-thick layer where a *FF* of 80 % is obtained. The increase in *FF* as a function of μc-Si:H(*n*) thickness can be explained with the improved crystallinity and decreased contact resistivity as presented in Section 3.4 of this Chapter. In general, the *FF* values are higher for the SHJ cells with finger pitch of 2 mm because there are more Cu fingers at the front and they are more closely spaced, resulting in more efficient current extraction. Overall, the final conversion efficiency trend for the presented devices is dictated by the *FF* and it shows outstanding improvement when a 14-nm-thick μc-Si:H(*n*) rear contact layer is used.

Table 3.2 – Summary of the parameters for the Cu-plated SHJ solar cells with finger pitch of 2 mm and feature MoO_x hole front selective contact and various electron-selective rear contacts as indicated in the first column.

Cell	V_{oc}**[mV]**	J_{sc}**[mA/cm^2]**	***FF*[%]**	**Efficiency [%]**
Ref. with 7 nm a-Si:H(*n*) rear contact	719	38.8	77.1	21.5
7 nm μc-Si:H(*n*) rear contact	723	39.0	78.6	22.2
11 nm μc-Si:H(*n*) rear contact	724	39.2	78.9	22.4
14 nm μc-Si:H(*n*) rear contact	725	38.9	80.0	22.5

The obtained cell parameters for the Cu-plated SHJ solar cells with finger pitch of 2 mm are summarized in Table 3.2 for clarity. Except for the reference cell with MoO_x front and a-Si:H(*n*) rear contact, all the cells that feature MoO_x front and μc-Si:H(*n*) rear contact reach

[3]The results presented in this section were obtained with the help of J. Geissbühler who performed the MoO_x deposition and Cu-plating. Contribution is gratefully acknowledged.

conversion efficiencies above 22 %. With the above mentioned *FF* and J_{sc} improvements, an energy-conversion efficiency of 22.5 % for a 4 cm^2 SHJ solar cell with V_{oc} of 725 mV, J_{sc} of 38.9 mA/cm^2 and *FF* of 80 % is demonstrated.

3.6 Conclusions

First, we show that the growth of μc-Si:H layers starts from nucleation seeds and that the diameter of the microcrystalline grains increases with thickness, leading to a conical grain shape and improved crystallinity. In general, replacing the doped a-Si:H layer with μc-Si:H yields lower specific contact resistivities with the ITO/Ag when the thickness of the μc-Si:H layer is greater than 9 nm. Additionally, the contact resistivity decreases further with thickness thanks to the increased crystallinity — doping efficiency — as well as the higher contact area between the crystalline phase and the ITO layer, which leads to a more efficient charge-carrier collection. It is also observed that charge-carrier transport at low temperatures is more efficient with doped μc-Si:H layers, as the contact resistivity becomes increasingly dominated by temperature-independent tunnelling and the thermionic component is diminished.

At the device level, we demonstrate that doped μc-Si:H(*p*) hole-selective front contacts have a clear potential to improve the optical performance of SHJ devices by providing a J_{sc} gain of up to 1.5 mA/cm^2 due to their higher transparency. Then, the effect of inverted polarity — rear hole collection — is investigated experimentally by realizing fully a-Si:H reference cells. Inspired by the promising *FF* values obtained with inverted polarity, we implement μc-Si:H(*n*) electron-selective front contacts for the SHJ cells. With this design, a J_{sc} gain of up to 1.2 mA/cm^2 is obtained. These results demonstrate that μc-Si:H layers can be used as a replacement for doped a-Si:H layers in highly efficient SHJ cells, improving the optical performance while maintaining excellent passivation and providing high *FF* values due to the lower ρ_c.

By performing temperature-dependent *J-V* measurements we show that the observed V_{oc} saturation at low temperatures may be attributed to the Schottky barrier effect at the interface between the doped selective contact layer and the TCO, which can be suppressed by introducing a μc-Si:H(*p*) hole-selective layer. In this context, we note that the temperature-dependent *J-V* and ρ_c measurements are highly promising methods to obtain a deeper understanding of the transport mechanism in complex cell structures with multiple hetero-interfaces and potential transport barriers.

In the final part of this chapter, Cu-plated SHJ cells featuring a highly transparent MoO_x hole-selective front contact and a μc-Si:H(*n*) electron-selective rear contact were presented. As the cells benefit from increased front transparency and the reduced rear contact resistivity, a conversion efficiency of 22.5 % is reached for a 4 cm^2 SHJ solar cell with a V_{oc} of 725 mV, J_{sc} of 38.9 mA/cm^2 and *FF* of 80 %. Even though attaining the *FF* of 80 % is a significant improvement compared to the fully amorphous reference SHJ cells investigated here, it is still fairly low with respect to the theoretical *FF* limit.

In practice, the cells with a μc-Si:H layer can be a good candidate for low-temperature applications since their efficiency maximum is at lower temperatures compared to standard SHJ cells. Additionally they might be also interesting for the application field where high illumination is required thanks to their higher doping efficiencies. Another prominent application of the same μc-Si:H layers presented here is their integration to a novel tunnel-IBC device concept where patterning and alignment complexity are minimized considerably. The promising results were achieved thanks to the functionalized microstructure of the μc-Si:H layer. More detail about this work can be found in [Tomasi 2016a] and [Tomasi 2017]. Additionally, the μc-Si:H layer developed here was also employed as a recombination junction in two-terminal monolithic perovskite/SHJ tandem solar cells providing mitigated shunt paths due to its low lateral conductivity in contrast to its high vertical conductivity [Sahli 2017].

4 High thermal budget: Silicon-rich silicon carbide as hole-selective contacts

Summary

This chapter presents the development and optimization of a hole-selective passivating contact with a high thermal budget. The contact structure consists of a chemically grown thin silicon oxide (SiO_x) that is capped with an *in-situ* boron-doped silicon-rich silicon carbide [$SiC_x(p)$] layer and annealed at temperatures above 750 °C. Transmission electron microscopy reveals that the thin chemical SiO_x disappears upon thermal annealing at 900 °C, leading to degraded surface passivation. We interpret this in terms of a chemical reaction between poorly incorporated carbon atoms in the $SiC_x(p)$ layer and the adjacent SiO_x. By inserting an intrinsic silicon inter–layer between the chemical SiO_x and the $SiC_x(p)$ layer, the reaction is prevented. This is evidenced by improved surface passivation for an optimized inter–layer thickness of 10 nm and also confirmed with transmission electron microscopy. A tentative theory of charge-carrier transport is discussed in accordance with the obtained results.

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4.1 Introduction and motivation

In the previous chapter, it was found that replacing doped amorphous layers with microcrystalline layers is beneficial for the *FF* values of standard SHJ solar cells due to reduced specific contact resistivities. Motivated by this trend, we aimed to further increase the crys-

talline fraction of the doped layers. As a higher degree of crystallization can be achieved by thermal treatment, we turned towards a high-thermal-budget approach. In this context, poly-Si [De Graaff 1979], [Fossum 1980], [Tarr 1985], [Gan 1990], TOPCon [Feldmann 2014a], [Feldmann 2014c], [Feldmann 2014d], [Feldmann 2014e] and POLO [Römer 2014] contact structures are considered to be attractive alternatives to SHJ contacts as they ensure not only a perfect full-area surface passivation but also a higher doping efficiency, a lower contact resistivity, and a lower parasitic absorption in the poly-Si layer thanks to the thermal treatment that leads high crystallinity. Additionally, high-temperature contacts can feature lower sheet resistance than that of the SHJ contacts; therefore their application can relax some of the constraints on the electrode design such as the metal grid, TCO, etc.

The high-temperature approach uses silicon oxide (SiO_x) as a thin buffer layer capped with doped Si layers. Charge-carrier selectivity is promoted by an in-diffused region at the c-Si wafer, which is obtained by annealing of the layer stack at temperatures above 750 °C. Recently, a remarkable efficiency of 25.8 % was demonstrated using a similar structure as a rear electron-selective passivating contact in an *n*-type solar cell with a front boron-diffused homojuction [Richter 2017]. The contact structure consists of a chemically or photo-chemically grown ultra-thin SiO_x buffer layer capped with a phosphorus-doped amorphous silicon [a-Si:H(*n*)] layer deposited by plasma-enhanced chemical vapour deposition (PECVD). After a hydrogenation step to passivate electronic defects, this contact structure yields an emitter saturation current density (J_0) of 4 fA/cm^2 and a contact resistance of 50 mΩ cm^2. Analogous structures were used for hole-selective contacts using boron-doped amorphous silicon [a-Si:H(*p*)], resulting however in slightly lower performance compared to electron-selective contacts. Their lower performance is commonly explained by the high surface recombination velocity occurring at boron-diffused surfaces that are passivated with SiO_x and additional defect creation by boron diffusion through the SiO_x layer [Maritan 1985], [Yamamoto 1999]. An additional practical complication of hole-selective passivating contacts is the blistering of the a-Si:H(*p*) layer, which poses severe processing restrictions to the deposition and thermal annealing processes [Nemeth 2016]. In the literature, for *in-situ* doped layers deposited by PECVD, J_0 values of around 50 fA/cm^2 and implied open-circuit voltages (iV_{oc}) of 680 mV have been reported [Feldmann 2014b]. Using ion implantation techniques, slightly better results with a J_0 of 22 fA/cm^2 and iV_{oc} of 696 mV have been demonstrated [Reichel 2015]. Yang *et al.* reported iV_{oc} value of 704 mV for a boron-implanted poly-Si passivating contact on chemical SiO_x before any subsequent hydrogenation [Yang 2016]. Impressively low J_0 values of 3.8 fA/cm^2 with *p*-type poly-Si on an *n*-type wafer using ion implantation technique on thermally grown SiO_x were shown [Larionova 2017]. Also, Nemeth *et al.* reported an iV_{oc} of 700 mV with hole-selective contact as a high-low junction using a thermal SiO_x as a thin buffer oxide [Nemeth 2016]. Yan *et al.* demonstrated an approach to form *p*-type passivating contacts based on PECVD of undoped a-Si followed by thermal diffusion of boron from a BBr_3 source and attained J_0 values of 16 fA/cm^2 [Yan 2016]. With *p*-type poly-SiO_x on an *n*-type wafer, Yang *et al.* demonstrated an iV_{oc} of 709 mV with corresponding J_0 values of 15.6 fA/cm^2 [Yang 2018]. The potential of the gallium-doped poly-Si as an alternative to boron-doped poly-Si using *n*-type wafers and

ion implantation was explored by Young *et al.* iV_{oc} values of > 730 mV with corresponding J_0 values of < 5 fA/cm^2 were reported; however, despite the excellent surface passivation, this contact suffers from high contact resistivities between the gallium-doped poly-Si layer and metal [Young 2017].

Here we present the development of *in-situ* boron-doped hole-selective passivating contacts with a high temperature budget. The contact structure consists of a triple layer stack comprising a chemically grown SiO_x, an intrinsic silicon [Si(i)] inter–layer, and a boron-doped silicon-rich silicon carbide [$SiC_x(p)$] layer. The stack of Si(i) and $SiC_x(p)$ was deposited by PECVD technique. Compared to LPCVD, the PECVD process has the advantage of one-side processing, and the possibility of *in-situ* doping which is much simpler than ion implantation. The choice of SiC_x is motivated by several advantages: (i) the material is more resilient to blistering than a-Si:H when deposited on chemical SiO_x, (ii) C–H bonds are more stable than Si–H bonds with respect to hydrogen effusion, (iii) SiC_x is stable in the standard wet-chemical solutions used in Si solar cell fabrication, and (iv) the optical properties of the SiC_x can be tuned by varying the C concentration. Because of (iii), the rear contact can also serve as rear-side protection through the entire cell process, providing large processing flexibility. To be compatible with industrial applications and propose an alternative rear contact to the mainstream technologies, the developments were performed on *p*-type wafers.

4.2 Experimental details

In this chapter passivating hole-selective contacts were investigated using symmetric structures based on either 280-μm-thick double-side-polished 4-inch *p*-type float zone <100> c-Si wafers with a resistivity of 2.8 Ω cm or 250-μm-thick chemically polished 4-inch *p*-type float-zone <100> c-Si wafers with a resistivity of 2 Ω cm. After standard wet-chemical cleaning, a thin SiO_x layer (~ 1.2 nm) was formed by wet-chemical oxidation using 69 wt % diluted HNO_3 solution at 80 °C referred to henceforth as "chemical SiO_x" [Asuha 2002], [Asuha 2003], [Asuha 2004]. Subsequently, ~ 30-nm-thick $SiC_x(p)$ — amorphous in the *as-deposited* state — was deposited on both sides by PECVD operated at 40.86 MHz with silane (SiH_4), hydrogen (H_2), trimethylboron (TMB) and methane (CH_4) as process gases. The substrate temperature was 200 °C and the power density was 0.06 W/cm^2. The samples were then annealed in an inert gas atmosphere in the temperature range of 800 to 925 °C. This was followed by a hydrogenation step to passivate electronic defects at the chemical SiO_x/c-Si wafer interface either with forming gas annealing (FGA, 4 % H_2 in N_2) at 500 °C or with SiN_x as a hydrogen donor layer. In the latter case, a SiN_x layer was deposited by PECVD and a hot-plate annealing at 450 °C was performed for 30 min which was then followed by stripping the SiN_x in 5 % diluted HF.

The surface passivation properties were investigated by quasi-steady-state photoconductance (QSSPC) decay measurements, giving an access to the effective minority-carrier lifetime as a function of the excess minority-carrier density and the resulting iV_{oc} values [Sinton 1996b]. The method of Kane and Swanson was applied to extract the emitter saturation current density

(J_0) at an excess-carrier density of 5 × 10^{15} cm^{-3} [Kane 1985]. The spatial homogeneity of the passivation was analyzed using photoluminescence imaging (PLI). The transfer length measurement (TLM) technique with a linear contact-pad array was applied to extract the contact resistivity on a *p*-type wafer [Berger 1972]. The structural changes occurring upon annealing either at 800 or 900 °C were characterized using transmission electron microscopy (TEM) performed in either an FEI Titan Themis or an FEI Tecnai Osiris, both operated at 200 kV. In addition to the acquisition of high-resolution (HR)TEM micrographs, scanning TEM (STEM) images were recorded using a high-angle annular dark-field (HAADF) detector and were combined with energy-dispersive X-ray spectroscopy (EDX) to obtain a chemical assessment of the layers of interest. For this purpose, TEM lamellae were prepared from samples after deposition and annealing at 800 or 900 °C, respectively, using the conventional focused ion beam (FIB) lift-out technique in a Zeiss Nvision 40 workstation. The crystallinity of the contact layers after annealing was studied by grazing incidence X-ray diffraction (GI-XRD) using a Bruker D8 Discover Tool with the Cu-Kα (λ = 1.542 Å) radiation source at a fixed incidence angle of 0.3°. Additional to GI-XRD, Raman spectroscopy was performed using a 325 nm UV laser that has a collection depth of 10 nm in c-Si to study the crystallinity of the contact layers close to the surface. To define the locally resolved conductivity of the contact structure, conductive atomic force microscopy (C-AFM) measurements were performed in peak force C-AFM mode (known as PF-TUNA)) using Dimension Icon AFM with a PtIr-coated antimony-doped c-Si conductive tip (CSG01/Pt) with a radius of < 35 nm.

4.3 Results and discussions

4.3.1 Structural properties of the contact upon annealing

The structure of the hole-selective contact and its evolution upon thermal treatment was investigated by TEM. STEM HAADF images together with corresponding EDX maps and line scans for the contact structure in *as-deposited* state and after annealing for 5 min at 800 and 900°C are shown in Figure 4.1. The EDX data confirms that the thin dark line observed at the c-Si wafer interface in the STEM HAADF images corresponds to the chemical SiO_x. In the *as-deposited* state, depicted in Figure 4.1(a), a clearly defined, sharp interface is observed between the c-Si wafer and the chemical SiO_x. After annealing at 800 °C, the contact structure preserves the sharp interface [see Figure 4.1(b)]. After annealing at 900 °C revealed in Figure 4.1(c), however, the chemical SiO_x layer at the c-Si wafer interface is not present any more. Carbon (C) appears to be incorporated into the recrystallized Si layer that presents epitaxial re–growth on the c-Si wafer [see Figure 4.2(a)]. The HRTEM micrograph and corresponding Fourier transform also highlight the presence of stacking faults along the (111) crystallographic planes — seen as streaks in the reciprocal space transform. These stacking faults are likely induced by thermal stressing due to the presence of C in the Si lattice [Liu 2002], [Brillson 2002]. In addition to c-Si reflections, a reflection at 4 nm^{-1}, which corresponds to the (111) planes of cubic (beta-) SiC, is also measured in the Fourier transform [see Figure 4.2(a)].

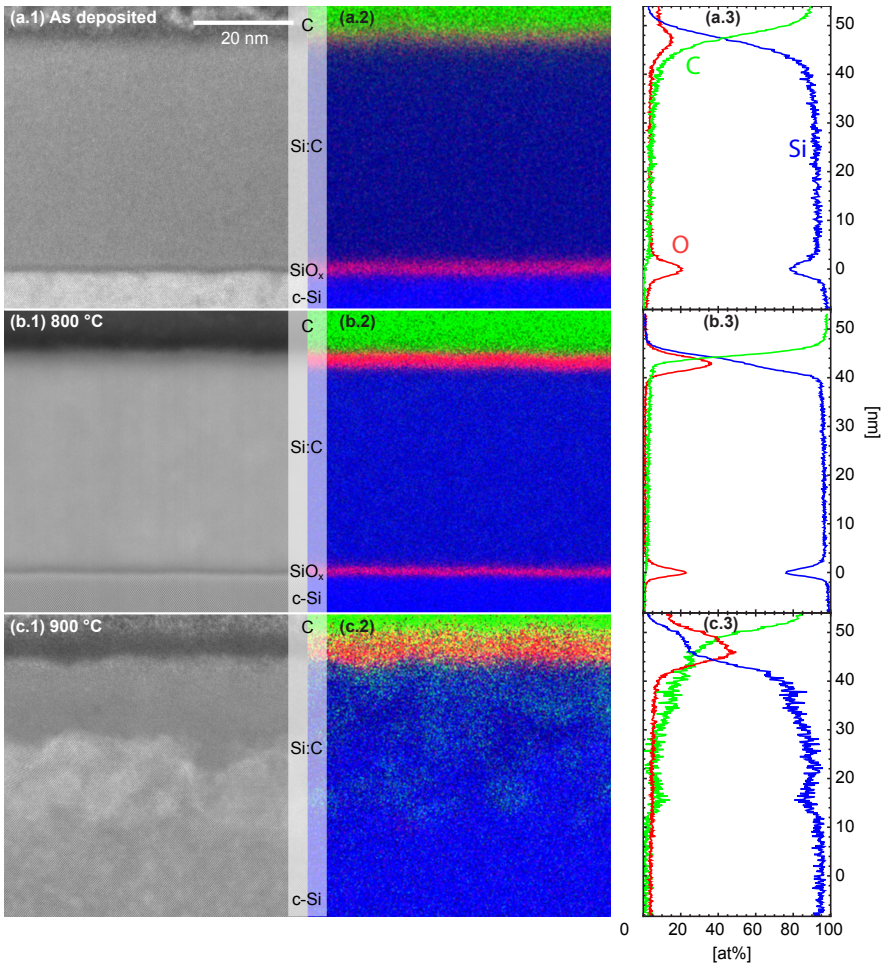

Figure 4.1 – STEM-HAADF micrographs (left), corresponding EDX maps (middle), and EDX line scans (right, quantified using the Cliff-Lorimer methods [Cliff 1975]) of the c-Si wafer / SiO_x / $SiC_x(p)$ contact structure. (a) *As-deposited*, and after thermal annealing for 5 minutes at (b) 800 and (c) 900 °C. Adapted with permission from [Nogay 2016b]. Copyright ©2016, American Chemical Society.

Furthermore, the crystallinity of the structures was investigated by GI-XRD technique. Figure 4.2(b) shows the diffraction patterns of the samples annealed at 800 and 900 °C. The peaks appearing at diffraction angles of 28.4°, 47.4°, 56.3° are attributed to the (111), (220) and (311) reflections of Si crystals. The expected reflections of cubic SiC at 35.4°, 60.0°, 71.8°, which correspond to the (111), (220) and (311) planes, respectively, are also indicated in Figure 4.2(b). The full width half maxima (FWHM) of the Si related peaks — excluding the (111) peak arises mainly from the wafer — are narrower for the sample annealed at 900°C, which is the signature of a larger mean crystallite size [Patterson 1939]. Additionally, after annealing at 900 °C a peak at 35.4°, which corresponds to the (111) reflection from cubic SiC, becomes visible, confirming the formation of SiC crystallites as observed in the TEM micrograph [c.f. Figure 4.2(a)]. The results are in agreement with previous studies, which also reported a degraded

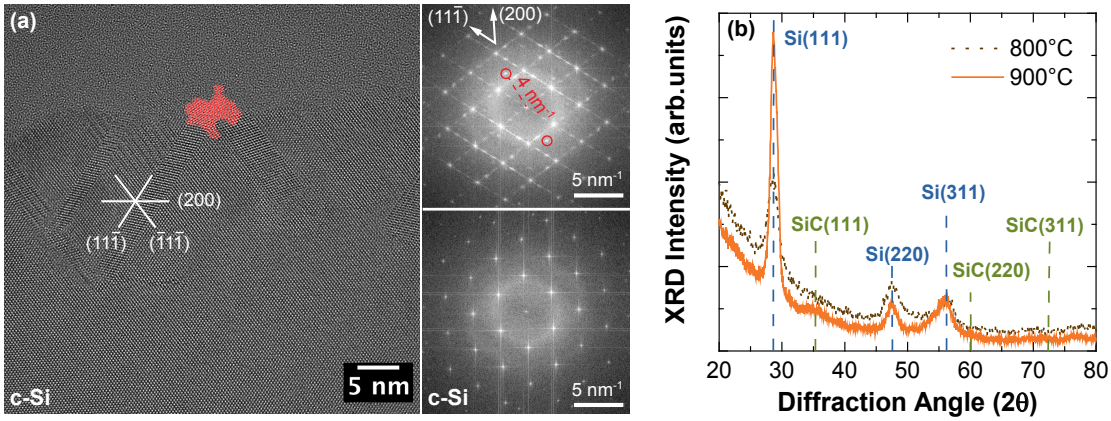

Figure 4.2 – (a) HRTEM image of the sample annealed at 900 °C together with Fourier transforms computed from the recrystallized SiC_x region containing stacking faults (top right) and at the position of the c-Si wafer (bottom right) (b) GI-XRD diffractograms after annealing at 800 and 900°C. The dashed lines indicate the positions of the Si (111), (220) and (311) reflections at 28.4°, 47.4° and 56.3° and of the cubic SiC (111), (220) and (311) reflections at diffraction angles of 35.4°, 60.0°, 71.8°. Adapted with permission from [Nogay 2016b]. Copyright ©2016, American Chemical Society.

surface passivation after annealing at temperatures above 875 °C due to a local breakup of the SiO_x buffer layer with epitaxial re–growth of the deposited Si layer [Wolstenholme 1987]. However, to the best of our knowledge, there is no report showing the complete disappearance of the SiO_x layer after a thermal treatment at 900 °C.

Chemical bonding in a SiC_x layers prepared by PECVD technique strongly depends on the deposition parameters and related plasma regime [Bullot 1987], [Beyer 1987]. Especially in the low power "*starving plasma*" regime identified by Solomon *et al.* [Solomon 1988], the decomposition probability of CH_4 is much lower than that of SiH_4, therefore CH_4 is dissociated only by the reaction of the CH_4 molecules with the species created by the decomposed SiH_4 [Winters 1975], [Schnitt 1983]. Since there is no primary decomposition of CH_4, C atoms are incorporated in the layer mostly as CH_3 groups. As these establish only one bond to the Si network, they are only poorly incorporated in the lattice. Upon heating, hydrogen effuses from the amorphous network at temperatures far below 800 °C [Beyer 1987], leaving "dehydrogenated" C atoms that are only bond to one Si atom. Overall, it suggests that the SiO_x layer reacts with the loosely bond C according to at least one of the reactions [Schroder 1986];

$$zC + xSiO_2 \rightarrow xSi + yCO \tag{4.1}$$

$$3C + SiO_2 \rightarrow SiC + 2CO \tag{4.2}$$

Consequently, the oxygen would effuse in gaseous form as CO or CO_2. While the reported reaction temperatures are higher than the annealing temperature employed here, it should be noted that in our study the C source is in immediate contact with the chemical SiO_x layer and that the total O quantity is rather low. Upon thermal annealing of $SiC_x(p)$ layers, SiC crystallites are usually observed as soon as Si crystallites are detected despite the higher crystallization energy of SiC. This effect is explained by the heterogeneous nucleation of SiC at the Si crystals lowering the activation energy for crystalline growth [Summonte 2014]. While O effuses from the layer bounding in CO or CO_2, the remaining C forms SiC which may be partially incorporated into the layer during its epitaxial re–growth as evidenced by the high density of stacking faults. The chemical SiO_x layer is still visible in the TEM images after annealing at 800 °C. However as the chemical SiO_x layer vanishes after annealing at 900 °C for 5 min, we speculate that also after annealing at 800 °C for 5 min, the chemical SiO_x layer has likely already been weakened by reaction with C since the symmetrical lifetime sample employing this contact structure attains only to an iV_{oc} of 685 mV.

4.3.2 The effect of intrinsic silicon inter–layer

As structural defects act as recombination centers, an intact interface between the chemical SiO_x and c-Si wafer is indispensable for good surface passivation. To mitigate the chemical reaction of the chemical SiO_x with the C from the deposited $SiC_x(p)$ layer mentioned in Section 4.3.1, we introduce an additional intrinsic Si [Si(i)] inter–layer in between the chemical SiO_x and the $SiC_x(p)$ layer. Figure 4.3 shows the iV_{oc} and J_0 values for the contact structures that have different inter–layer thicknesses after annealing at 800°C with a dwell time of 5 min. It is observed that the Si(i) inter–layer boosts the iV_{oc} from 685 mV up to 708 mV and lowers the J_0

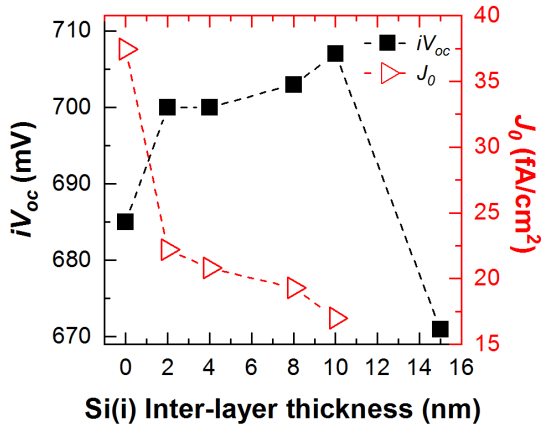

Figure 4.3 – The impact of the intrinsic Si inter–layer thicknesses on iV_{oc} and J_0 of the contact structure after annealing at 800 °C for 5 minutes and subsequently hydrogenating with SiN_x. Adapted with permission from [Nogay 2016b]. Copyright ©2016, American Chemical Society.

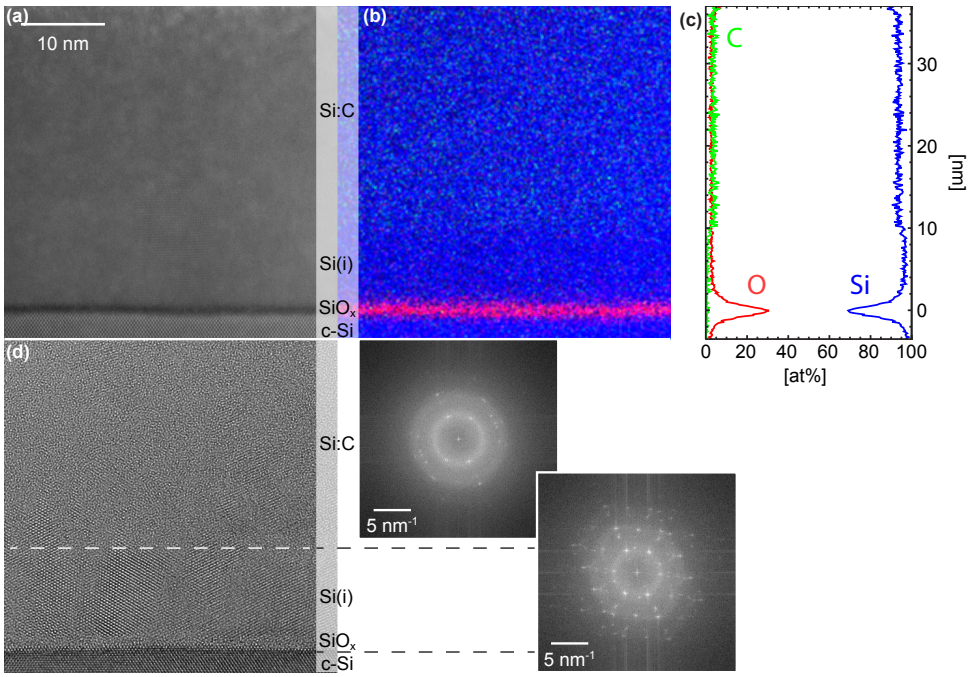

Figure 4.4 – TEM characterization of the c-Si wafer/chemical SiO_x/ intrinsic Si inter–layer / $SiC_x(p)$ contact structure after annealing at 800 °C for 5 minutes. (a) STEM HAADF image, (b) EDX map together with (c) EDX line scan and (d) HRTEM micrograph along with Fourier transforms computed at the position of both the inter–layer (bottom) and the $SiC_x(p)$ (top). Adapted with permission from [Nogay 2016b]. Copyright ©2016, American Chemical Society.

down to 17 fA/cm^2 for the sample with a 10-nm-thick inter–layer. Based on the diffusivity of C in Si [Goetzberger 1994], we assume that for very thin Si(i) inter–layer, C atoms can still reach the chemical SiO_x, which might explain the lower performance of the samples with 2- and 4-nm-thick Si(i) inter–layer. When the Si(i) inter–layer thickness increases further from 10 to 15 nm, the iV_{oc} shows a drastic decay to 670 mV. We tentatively explain this with a reduced dopant in-diffusion from the $SiC_x(p)$ layer to the c-Si wafer leading to insufficient band bending that fails at shielding the minority carriers from the SiO_x/c-Si interface effectively. Corresponding J_0 values show an agreement with the iV_{oc} values and decrease with increasing Si(i) inter–layer thickness.

The microstructure of a sample with 10-nm-thick Si(i) inter–layer after annealing at 800 °C is depicted in Figure 4.4. The HAADF image shows a sharp and well preserved chemical SiO_x/c-Si interface, and the SiO_x layer is clearly resolved in the EDX map as well. The EDX map further shows that C concentration in the top most layer is 4.8 ± 1 %, while the C content in the Si(i) inter–layer is below the detection limit. According to the Fourier transform computed from the HRTEM micrograph [see Figure 4.4(d)], the Si(i) inter–layer is highly crystalline after the annealing process. Based on these findings, we speculate that the presence of the Si(i) inter–layer hinders the reaction of the chemical SiO_x with C from the $SiC_x(p)$ layer and thus preserves an intact interface between the chemical SiO_x and the c-Si wafer with excellent

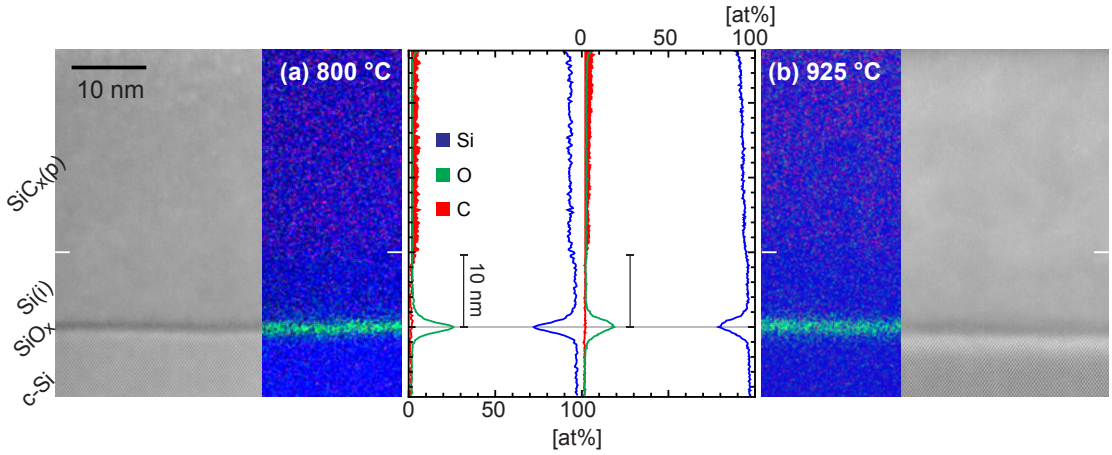

Figure 4.5 – STEM HAADF micrographs together with corresponding EDX mapping and line scans that exhibit the concentration profiles of Si, O, C for the sample produced with TMB flow of 1.5 sccm and annealed at (a) 800 and (b) 925 °C for 0 min. Quantification was performed using the Cliff-Lorimer method [Cliff 1975].

surface passivation as shown in Figure 4.3.

With the objective to confirm our interpretation, structural characterization of the sample that consists of 10-nm-thick Si(i) inter–layer and annealed at 925 °C was also studied by TEM. Figure 4.5 shows the STEM HAADF micrographs together with corresponding EDX mapping and line scans that exhibit the concentration profiles of Si, O, C for the sample annealed at (a) 800 and (b) 925 °C for 0 min. The micrograph of the sample annealed at 800 °C is added only for direct comparison. Figure 4.5(b) reveals that even after annealing at 925 °C, the presence of 10-nm-thick Si(i) inter–layer prevents the SiO_x annihilation. This is in clear contrast to the observation in section 4.3.1 [cf. Figure 4.1(c)] where no inter–layer was used. Therefore, TEM analysis supports our interpretation.

4.3.3 The role of molecular and atomic hydrogenation

Most passivating contacts based on thin SiO_x layers require re-introduction of hydrogen after the high-temperature annealing step in order to decrease the recombination active defect states at the interface. After the annealing, the partially crystallized layer stack and the chemical SiO_x feature a high defect density and it is presumed that these defects also need to be passivated to achieve good passivation. Hence, the hydrogen passivation requires diffusion of hydrogen through the partially crystallized layer stack to the chemical SiO_x/c-Si wafer interface and chemical incorporation of hydrogen at this interface, in the chemical SiO_x layer and in the partially crystallized layer stack. FGA is one of the most recognized methods for re-hydrogenation of such contact structures [Aberle 1992] and impressively high iV_{oc} values

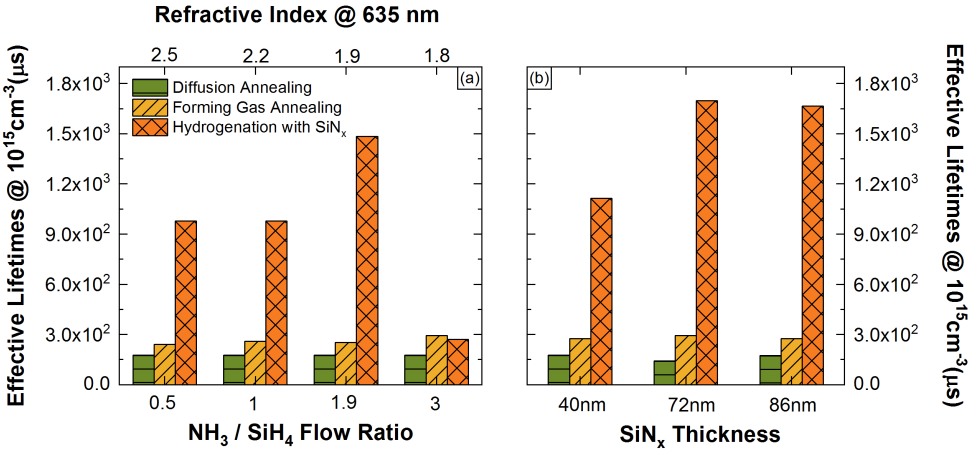

Figure 4.6 – Evolution of the effective lifetime values of symmetric sister samples after annealing for boron in-diffusion, after FGA and after an additional hydrogenation from SiN_x overlayers. (a) The effect of the NH_3/SiH_4 flow ratio during the 60-nm-thick SiN_x deposition, (b) the impact of the SiN_x thickness for layers deposited with a NH_3/SiH_4 flow ratio of 1.9. Adapted with permission from [Nogay 2017]. Copyright ©2017, Elsevier.

have been reported for forming gas annealed *n*-type poly-Si contacts on *n*-type c-Si wafer [Yan 2015], [Stuckelberger 2016].

Figure 4.6 shows the evolution of the effective lifetime values along the contact formation process for our contact prepared with a TMB flow of 1.5 sccm. After diffusion annealing, we observe rather low effective lifetimes around 160 μs. After subsequent annealing in forming gas at 500 °C for 30 min, an improvement in lifetime to 250 μs is observed, which is, however, a moderate increase in view of other reported values for similar hole-selective contacts based on chemical SiO_x and boron-doped layer hydrogenated via FGA [Yan 2016]. In contrast to most structures reported in the literature, our stack features a silicon-rich silicon carbide layer — C concentration 4.8 ± 1 % — instead of pure Si layer. Recent investigations of stoichiometric SiC and recrystallized silicon-rich silicon carbide layers showed that annealing in molecular hydrogen does not affect the electronic defect density in either case [Schnabel 2015]. However, successful passivation of electronic defects was shown in the same study for silicon-rich silicon carbide layers upon exposure to atomic hydrogen. The less pronounced effect observed for stoichiometric SiC layers exposed to atomic hydrogen was attributed to a lower diffusivity of hydrogen in SiC than in silicon or more efficient hydrogen capture in silicon-rich silicon carbide by silicon crystallite grain boundaries. Motivated by the passivation of our contact by atomic hydrogen, we used SiN_x layers as a hydrogen source and annealing at 450 °C for 30 min to diffuse the hydrogen from the SiN_x overlayers through the contact stack and incorporate it at the chemical SiO_x/c-Si wafer interface. In a first step, we deposited a 60-nm-thick SiN_x overlayer on the samples after forming gas annealing using various NH_3/SiH_4 ratios from 0.5 (refractive index of 2.5 at 635 nm) to 3 (refractive index of 1.8 at 635 nm). Figure 4.6(a) shows

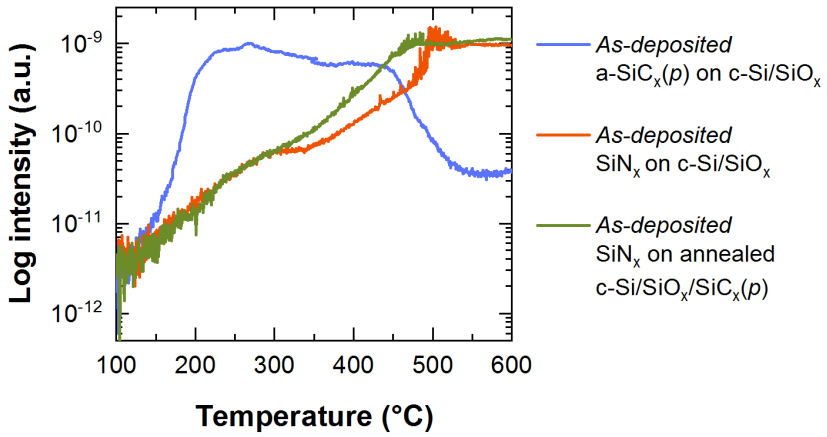

Figure 4.7 – TDS spectra of *as-deposited* a-$SiC_x(p)$ on SiO_x/c-Si (blue curve), SiN_x on SiO_x/c-Si (orange curve), and SiN_x on $SiC_x(p)$ /SiO_x/c-Si (green curve), with the $SiC_x(p)$ previously annealed at 800 °C for m/Z = 2 (H_2). Adapted with permission from [Nogay 2017]. Copyright ©2017, Elsevier.

an impressive improvement of the effective lifetime after atomic hydrogenation. Note that these values were measured after etching the SiN_x with 5 % diluted HF solution, ensuring that the observed effect does not originate from possible fixed charges contained in the SiN_x layer. Consequently, SiN_x acts as a hydrogen source and 450 °C annealing induces hydrogen diffusion through the *p*-contact stack to the chemical SiO_x/c-Si wafer interface. Figure 4.6(a) reveals that the optimal NH_3/SiH_4 flow ratio of 1.9 results in the highest effective minority-carrier lifetime. In a second step, we optimized the SiN_x hydrogen donor layer further by investigating the effect of the SiN_x thickness, as presented in Figure 4.6(b). With increased layer thickness, first the lifetime value increases until reaching a maximum and decreasing again. We attribute the increase to the augmented hydrogen reservoir, but cannot conclude on the reason of the decrease for thickness higher that 72 nm.

To investigate the role of hydrogenation more in detail, we performed TDS measurements on the (i) an *as-deposited* a-$SiC_x(p)$ layer on c-Si with SiO_x, (ii) a SiN_x layer deposited on a c-Si wafer with SiO_x, and (iii) a SiN_x layer deposited on a $SiC_x(p)$ layer that was previously annealed at 800 °C. For this measurement, only one-side deposited samples were prepared. Before the measurements samples were kept one hour at room temperature under low pressure to desorb as much as possible the water absorbed on the c-Si wafer surface and the chamber walls, until reaching a base pressure of 5.25×10^{-10} Torr. For the measurement, samples were heated with a halogen lamp from room temperature to 690 °C substrate temperature at a rate of 20 °C/min. Effusing species were identified by quadrupole mass spectrometry. The effusion spectra of H_2 are shown in Figure 4.7. The *as-deposited* a-$SiC_x(p)$ contact layer shows hydrogen effusion mainly in the temperature range of 200–500°C which is in line with previously reported effusion spectra of SiC_x layers [Beyer 1985]. The hydrogen effusion spectra

of the SiN_x on c-Si wafer and deposited on $SiC_x(p)$ reveal that irrespective of the substrate, the observed hydrogen effusion shows the same characteristic up to the 300 °C, which is close the SiN_x deposition temperature. The high hydrogen effusion, but slower desorption rate compared to the $SiC_x(p)$, confirm the role of SiN_x as a hydrogen reservoir. Above 300 °C, stronger effusion is seen for the SiN_x layer prepared on the $SiC_x(p)$ layer compared to the SiN_x prepared on the bare c-Si wafer. This may indicate that hydrogen diffusion towards the underlying wafer is impeded by the $SiC_x(p)$ layer. We interpret the flat plateau observed at temperatures exceeding 475 °C for the two samples with SiN_x layer as an artifact originated by a limited pump speed and resulting H_2 saturation of the chamber beyond that threshold.

4.3.4 Process optimization

Impact of CH_4 flow

In order to optimize the contact structure further, the optimum Si(i) inter–layer thickness of 10 nm was selected. The effect of the CH_4 process gas flow during the deposition of the a-$SiC_x(p)$ layer was investigated, while keeping all other process parameters constant. The dependence of the iV_{oc} and J_0 on CH_4 flow is shown in Figure 4.8 for samples annealed for 5 min at temperatures of 800, 825 and 850 °C. For all investigated CH_4 flows, the best annealing temperature is defined as 800 °C. J_0 is decreasing with increasing CH_4 flow for the samples annealed at 850 °C, but is worse than all other investigated conditions. In general, the passivation deteriorates with annealing temperatures higher than 800 °C due to either more pronounced in-diffusion of the boron that increases the Auger recombination or the

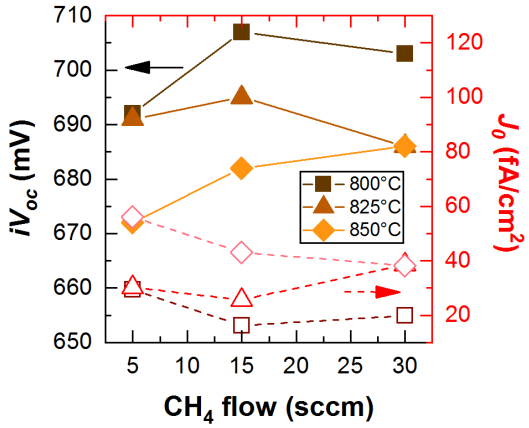

Figure 4.8 – Measured iV_{oc} (filled symbols) and J_0 (open symbols) of the contact structure annealed at different temperatures and subsequently hydrogenated with SiN_x, as a function of the CH_4 flow. Adapted with permission from [Nogay 2016b]. Copyright ©2016, American Chemical Society.

increased defect states at the chemical SiO_x/c-Si wafer interface due to the reaction of C with the chemical SiO_x. We note that it might be also the combination of both effects. Even though the Si(i) inter–layer is introduced to protect the chemical SiO_x interface, at high temperatures, C may still diffuse through the intrinsic layer and reach the chemical SiO_x. For the latter, among the samples annealed at 800 and 825 °C, the best results were achieved with a CH_4 flow of 15 sccm which is selected for further optimization.

Impact of doping concentration and annealing conditions

The effect of boron doping concentration in the $SiC_x(p)$ layer on the surface passivation and ρ_c was investigated as a function of annealing conditions. Figure 4.9(a–c) shows the iV_{oc} values for samples produced by varying the TMB flow during the doped layer deposition from 0.2 to 1.9 sccm and annealed at temperatures of 775 to 900 °C with various annealing dwell times. For TMB flows of 1 and 1.5 sccm, optimum passivation is attained after annealing at 800 °C for dwell time of 5 min, leading to an iV_{oc} of 718 mV. Whereas, for lower TMB flows such as 0.2 and 0.5 sccm, optimum passivation is reached with annealing at 850 °C for 0 min, which leads to an iV_{oc} value of 716 mV. We tentatively explain this shift in optimum condition with the fact that for decreased doping concentration, a higher annealing temperature is required to obtain efficient boron in-diffusion through the chemical SiO_x to strengthen the favourable band bending that shields the minority carriers from the chemical SiO_x/c-Si interface, thereby reduces the recombination current. For the samples produced with high TMB flows such as 1.5 and 1.9 sccm, the dwell time does not make a significant difference in iV_{oc} when the samples are annealed at 800 and 825 °C, whereas for the annealing temperature of 850 °C the passivating quality degrades drastically after 15 min [see Figure 4.9(c)]. For this dwell time, the longest used in this series, the best performance is obtained for samples produced with lower TMB flows except the sample with 0.2 sccm and annealed at 800 °C [see Figure 4.9(c)]. It is also perceived that with 900 °C annealing, regardless of the annealing dwell time, the iV_{oc} drops drastically, possibly due to temperature-induced local disruptions of the chemical SiO_x and pinhole formation which leads to epitaxial re–growth of the PECVD layer with the c-Si wafer. Additionally, strong boron in-diffusion might also deteriorate the chemical SiO_x/c-Si wafer interface.

The corresponding J_0 values for the samples shown in Figure 4.9(a–c) are presented in Figure 4.9(d–f). In general, J_0 values exhibit the same trends observed for iV_{oc} with values as low as 11 fA/cm^2. This value should be seen with respect to total area weighted J_0 values for the rear side of industrial p-type PERC solar cells around 35 fA/cm^2 which is marked with a grey dotted line in Figure 4.9(d–f). Thus, the reported passivating hole-selective contact clearly outperforms the conventional rear side of p-type c-Si solar cells. Effective specific contact resistivities which include the contribution of the c-Si wafer/$SiC_x(p)$, $SiC_x(p)$ /ITO and ITO/Ag interfaces, were characterized using the Berger structure. To investigate a possible impact of the current path, measurements were performed before and after etching of the region around the contact pads as well as the inter pad regions. Figure 4.9(g–i) show the ρ_c values measured

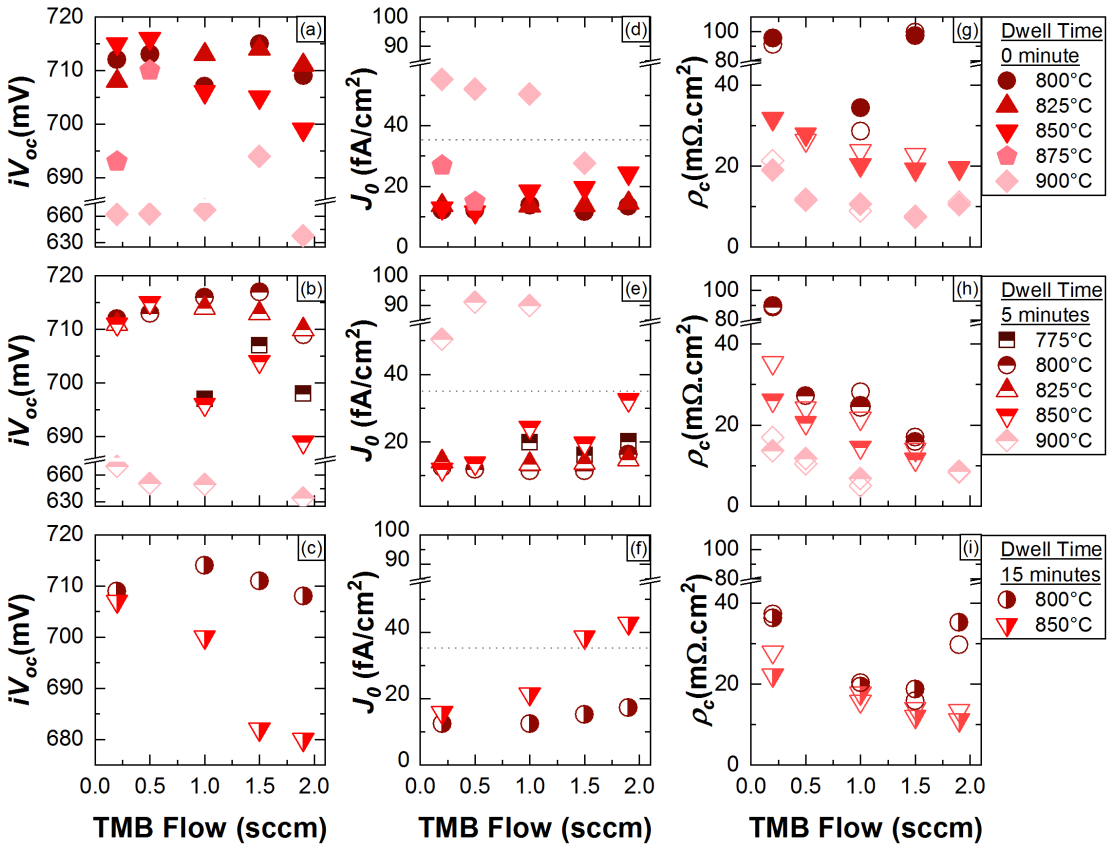

Figure 4.9 – Measured iV_{oc} as a function of TMB flow used during the deposition of the $SiC_x(p)$ for different annealing dwell temperatures with dwell time of (a) 0, (b) 5, and (c) 15 min. Corresponding J_0 values (d–f). Measured ρ_c values as a function of TMB flow used during the deposition of the $SiC_x(p)$ for different annealing dwell temperatures with dwell time of (g) 0, (h) 5, and (i) 15 min. Adapted with permission from [Nogay 2017]. Copyright ©2017, Elsevier.

before etching by filled symbols whereas open symbols denote the ρ_c values measured after etching. It is observed that etching of the inter-pad regions leads only to minor changes of the measured ρ_c values. This can be explained by the fact that the partially crystallized $SiC_x(p)$ layer contributes much less to the conductivity than the c-Si. Consequently, the current path is mainly inside the c-Si wafer even when the $SiC_x(p)$ layer is not etched. For all investigated dwell times, ρ_c decreases with increased annealing temperature. Similar to the case of high annealing temperatures, the chemical SiO_x might become disrupted to form pinholes or its thickness might vary locally, such that localized current paths open up for the charge carriers. With increased annealing temperature the density of such areas is likely to increase and result in the lower ρ_c. Even though there is some discrepancy for some of the samples prepared with TMB flow of 1.5 sccm and annealed at 800 °C for 0 min [Figure 4.9(g)] and sample prepared with TMB flow of 2 sccm and annealed at 800 °C for 15 min [Figure 4.9(i)], in general with increasing boron doping concentration, the ρ_c decreases irrespective of the annealing dwell times. The mentioned discrepancy might originate from processing inaccuracies during the

sputtering through the shadow mask, sometimes resulting in inhomogeneous contact pad widths, and therefore improperly defined pad distances. The lowest ρ_c reached was 6.84 mΩ cm^2 with the sample produced with a TMB flow of 1 sccm and annealed at 900 °C for 5 minutes [see Figure 4.9(h)]. However, this sample shows very poor passivation quality with iV_{oc} of 650 mV, as seen in Figure 4.9(b). The highest ρ_c measured is 97.26 mΩ cm^2 for the sample produced with TMB flow of 0.2 sccm and annealed at 800 °C for 0 min [see Figure 4.9(g)]. According to Figure 4.9(a), this sample has an iV_{oc} of 712 mV. The optimal condition for both good passivation quality and low ρ_c is attained with the sample produced with 1.5 sccm TMB flow and annealed at 800 °C for 5 minutes dwell time leading to iV_{oc} of 718 mV and ρ_c of 17 mΩ cm^2.

The term selectivity, how efficiently the minority carriers are shielded and majority carriers are extracted, was a qualitative term until Brendel *et al.* proposed a quantitative definition which could provide a figure of merit for electron and hole contacts that is helpful in designing solar cells and in identifying the efficiency limiting components [Brendel 2016]. We also calculated the selectivity (S_{10}) of our contact using their quantification,

$$S_{10} = \frac{V_{th}}{J_0 \rho_c} \tag{4.3}$$

where V_{th} is the thermal voltage at a temperature of 298.15 °K. According to this definition the selectivity of our contact is 14.1, which is higher than the value of 13 for screen-printed and fired Al-doped local back surface field contacts used at the rear side of industrial *p*-type solar cells. Consequently, the TLM measurements show that the presented layer stack provides not only excellent surface passivation but also sufficiently low contact resistivity for full-area contacts, in other words it exhibits great selectivity. These excellent results demonstrate that boron-doped $SiC_x(p)$ is a promising material to realize hole-selective contacts in combination with an interfacial chemical SiO_x and an additional Si(i) inter–layer.

4.3.5 Doping profiles

As it is mentioned before the formation of a highly doped region within the wafer is beneficial to obtain good surface passivation and efficient charge-carrier extraction as it introduces band bending in the c-Si and facilities selectively the carrier transport. To investigate the boron evolution in our contact structure with annealing, we performed secondary ion mass spectroscopy (SIMS) and electrochemical capacitance voltage (ECV) measurements. In general, SIMS determines the total dopant concentration, whereas ECV measures the concentration of the electrically active dopants. During the SIMS analysis, the mass is determined by mass spectrometry using O_2^+ ions with an energy of 1 keV as primary ion. Boron profiles for the sample annealed at 800 and 850 °C for 5 minutes with and without Si(i) inter–layer are depicted in Figure 4.10(a).

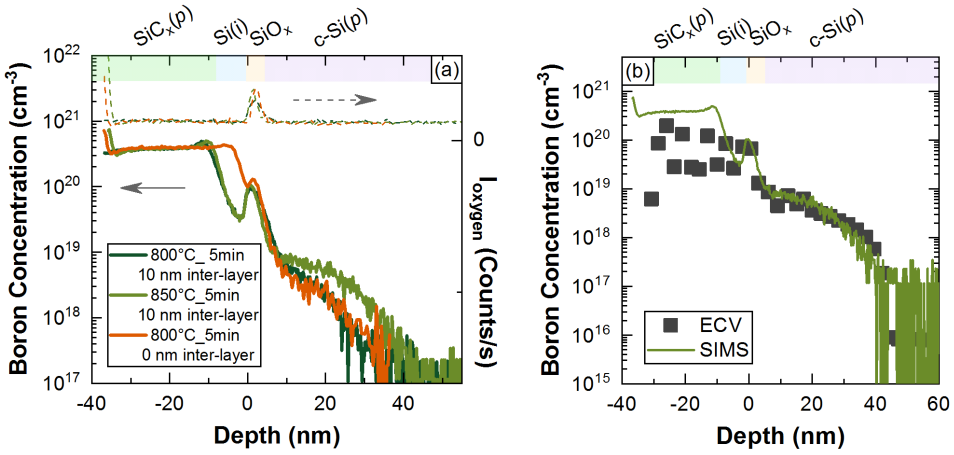

Figure 4.10 – (a) Doping profile measured by SIMS for the samples with TMB flow of 1.5 sccm and annealed at two different annealing temperatures of 800 and 850 °C for 5 min with and without Si(i) inter–layer. (b) Comparison of the data obtained from SIMS and ECV measurements for the $SiC_x(p)$ with 10 nm inter–layer and annealed at 850 °C for 5 min.

As the SIMS measurements were calibrated to a c-Si reference, it does not give the exact amount of boron incorporated into the $SiC_x(p)$ layer. Besides, the depth of the profiles are converted from sputtering time using the rate determined on the c-Si reference by assuming a homogeneous sputter rate in c-Si and $SiC_x(p)$ layer. Whereas the sputtering rate for $SiC_x(p)$ is known to be lower than c-Si, moreover since the crystalline nature of the layers depends on the annealing temperature, the rate is expected to be different for the $SiC_x(p)$ layers subjected to different thermal treatments. Nevertheless the part of the measured doping profiles that lies in the c-Si region is reliable. The oxygen peak, shown by dashed lines, was used to identify the chemical SiO_x/c-Si wafer interface and the zero position of the depth profiles were placed to its maximum. The negative side of the graph represents the deposited layer with PECVD while the positive side denotes the c-Si(p) region as indicated on the top of the Figure 4.10(a). According to SIMS data, the boron concentrations in the layers show essentially no differences after annealing, but the samples comprising a 10-nm-thick inter–layer show a dip at the position corresponding to Si(i) inter–layer indicating a lower boron concentration at that region. The sample annealed at 850 °C shows slightly deeper profile compared to the ones annealed at 800 °C. More importantly, comparing the samples with and without inter–layer, annealed at 800 °C, it is seen that introducing a 10-nm-thick Si(i) inter–layer does not affect the boron profile within the c-Si wafer significantly. This indicates that the better surface passivation obtained by introducing inter–layer is not originated from reduced Auger recombination in the diffused region. Instead, it is evidencing a decreased recombination velocity at the chemical SiO_x/c-Si wafer interface. This finding supports our interpretation about the function of the Si(i) inter–layer in Section 4.3.2, i.e. it hinders the chemical reaction of the C atoms from $SiC_x(p)$ layer with the adjacent chemical SiO_x and assists to maintain an intact SiO_x/c-Si wafer

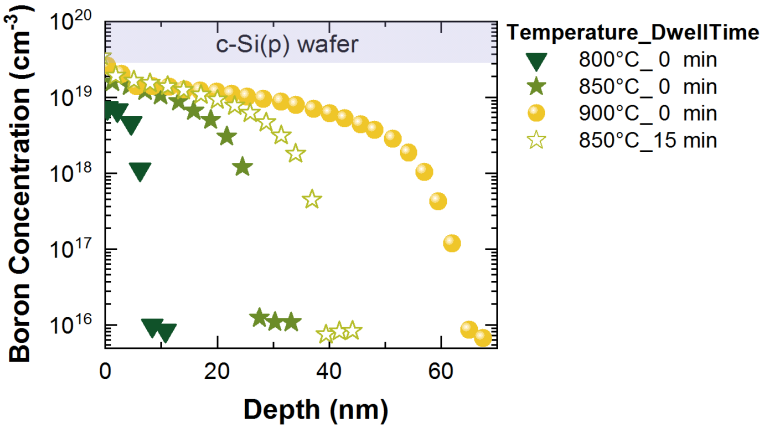

Figure 4.11 – Doping profile within the wafer measured by ECV for different annealing dwell temperatures and dwell times for the contact that was produced with a TMB flow of 1.5 sccm. Adapted with permission from [Nogay 2017]. Copyright ©2017, Elsevier.

interface.

The boron doping profile obtained from SIMS measurement for the sample with 10 nm inter–layer and annealed at 850 °C for 5 min is compared with the corresponding boron profile obtained from ECV in Figure 4.10(b). The ECV profile shows a strong fluctuation for the measurement of $SiC_x(p)$ layer which can be related to a complication in the electrochemical etching of the $SiC_x(p)$ layer. Another explanation can be that these fluctuations in the highly doped layers might be due to the partially amorphous and partially crystalline nature of the layers where high impurity concentrations at grain boundaries and lower concentrations within the grains are probed simultaneously. This effect is only visible in ECV since it probes electrically active dopants. It is also plausible to assume that especially in the $SiC_x(p)$ region some of the dopant atoms are inactive because they are trapped at grain boundaries which explains the higher boron concentration measured by SIMS in $SiC_x(p)$ layer. Besides that, the ECV profile agrees well with the measured SIMS profile, especially within the c-Si region.

Figure 4.11 shows the doping profiles of the samples prepared with TMB flow of 1.5 sccm within the *p*-type c-Si wafer measured by ECV for different annealing dwell temperatures. As distinct from the samples presented in Figure 4.10, here the samples were annealed for the dwell time of either 0 or 15 min. Please note that within a surface region of about 30 nm from the surface (corresponding to the PECVD deposited layer stack and not shown here), all samples exhibit a similar behaviour for all investigated temperatures, and all are affected by fluctuations similar to the one represented in Figure 4.10(b). According to the ECV measurements, electrically active dopant concentrations of the layers are in the range of 2×10^{20} cm^{-3}. In general, the doping profiles show a moderate boron concentration tail into the c-Si wafer, which is deeper for the higher diffusion temperatures, reaching a depth of 70 nm after annealing at 900 °C. As expected, the sample annealed at the lowest temperature — 800 °C — shows the lowest

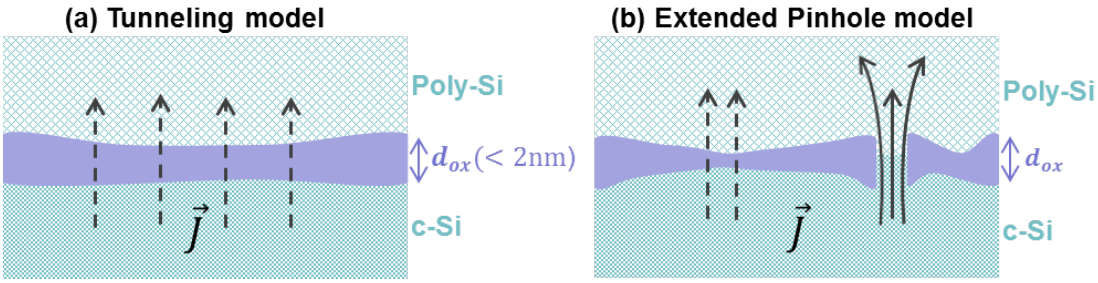

Figure 4.12 – Simplified sketch of the two proposed transport mechanisms in the literature. Dash line indicates tunneling through the oxide while solid line indicates direct current flow via local SiO_x breakups.

doping concentration within the wafer and a very shallow diffusion profile. For the samples annealed at 850 °C, we also investigated the effect of annealing dwell time. Figure 4.11 shows that with increasing dwell time, diffusion depth increases approximately 10 nm. Overall, the diffusion profiles in the bulk presented here are comparable with the literature values obtained by applying *in-situ* boron-doped layer as a dopant source for in-diffusion [Krügener 2016], however, distinctively they show a drop with an extremely steep tail to the bulk concentration of ca. 1×10^{16} cm^{-3}.

4.3.6 Short theory: Possible transport mechanism

Before discussing the charge-carrier transport mechanism for our structure, we give a short overview over the proposed transport models for the analogous structures such as Semi-Insulating Polycrystalline Silicon (SIPOS), poly-Si emitters, TOPCon, POLO, etc. We note that although the base structures of the abovementioned contacts are similar, the process steps diverge significantly, especially in terms of the SiO_x thickness and the thermal budget, which makes it difficult to formulate a unique theory on the underlying physical transport mechanism.

The poly-Si emitter was first developed for bipolar junction transistors (BJT) in the 1970s where a remarkable current gain enhancement was achieved when the conventional phosphorus diffusion was replaced with a doped poly-Si emitter; it quickly became a key element for high-speed devices. Its successful implementation attracted attention to explore the physical working principle in detail. Soon after different carrier transport models have been proposed to explain its extraordinary performance such as; (i) grain boundary mobility model, (ii) dopant segregation model, (iii) oxide tunneling model and (iv) oxide breakup model. A detailed explanation of these models together with a critical discussion can be found in [Post 1992]. However, unfortunately still today the transport mechanism of the poly-Si contact is not well understood. Among the abovementioned models, the oxide tunneling model and the oxide breakup model have become widely accepted and used extensively to explain the transport phenomenon of the recent contact structures in solar cells such as TOPCon and POLO.

The tunneling model explains the charge-carrier transport via direct tunneling through thin interfacial oxides with thicknesses < 2 nm as sketched in Figure 4.12(a). It was first proposed by de Graaff *et al.* [De Graaff 1979], and later modified by Eltoukhy *et al.* [Eltoukhy 1982]. In the model, one-dimensional time-independent tunneling probability, which is solved using a Wentzel-Kramer-Brillouin approximation, is given by the following equations:

$$P_{t,h} \approx \exp\left(-\frac{2}{\hbar} d_{ox} \sqrt{2 q m_h^* \Phi_h}\right) \tag{4.4}$$

$$P_{t,e} \approx \exp\left(-\frac{2}{\hbar} d_{ox} \sqrt{2 q m_e^* \Phi_e}\right) \tag{4.5}$$

Here, d_{ox} denotes the oxide thickness, m_h^* and m_e^* are the effective tunneling masses for holes and electrons, respectively. Φ_h and Φ_e are height of the energy barriers for holes and electrons, respectively. q is the elementary charge and $\hbar$ is the reduced Plank constant. According to this definition, the tunneling probability increases exponentially with decreased oxide thickness, barrier height and effective tunneling mass. By performing numerical simulations for carrier-selective electron contacts featuring thin oxides, Steinkemper *et al.* investigated the influence of the doping concentration and the crystallinity of the doped-Si layer, together with the effect of in-diffusion within the absorber, effective surface recombination velocity at the SiO_x/c-Si interface and oxide thickness [Steinkemper 2015]. Their model accounts for tunneling through the oxide and provides a qualitative prediction of the *FF* and V_{oc} behaviour for devices that employ a rear poly-Si–based electron-selective TOPCon contact and boron diffusion at the front. Their findings are also in a good agreement with experimental results. Recently by means of temperature-dependent *J-V* measurements on dedicated test structures, Feldmann *et al.* showed that electron-selective TOPCon contact with an intact SiO_x — annealed at 800 °C — showed an exponential increase of the contact resistance towards lower temperatures which is described very well with the metal-insulator-semiconductor (MIS) theory if tunneling of charge carriers through the SiO_x is taken into account [Feldmann 2018]. They also observed that TOPCon contacts with partly disrupted SiO_x — annealed at 900 °C — did not show an exponential increase in contact resistance towards low temperatures, but that the *J-V* characteristics of those devices were governed by the temperature dependence of the wafer conductivity.

While the electron contacts are well described by the direct tunneling model, one weakness of the tunneling model is the fact that it is unable to explain why poly-Si hole-selective contacts exhibit charge-carrier transport that is as good as poly-Si electron-selective contacts, even though a band-offset asymmetry is present at the SiO_x/c-Si interface. This phenomenon was also observed back in the 1980s for *p-n-p* transistors. According to the tunneling model, a slight current gain enhancement would come at the expense of a very high emitter resistance for *p-n-p* transistors, however, this was not reflected by the experimental results. Because of this discrepancy, as a complement to the tunneling mechanism, another model based on

a direct charge-carrier transport through localized disruption in the interfacial oxide was proposed first by Gan and Swanson [Gan 1990]. They suggested that depending on the size and density of these breakups, the transport through these local openings can be much higher than the transport due to tunneling. Lately, inspired by this model, Peibst *et al.* proposed a simple analytic pinhole model to describe the current transport in their POLO device which employs relatively thick thermally grown SiO_x. Their model focuses on the transport regime that both majority and minority carriers flow through the local oxide breakup — so-called pinhole — regions, and it shows that based on the assumption of circular pinholes in the oxide and hemispherical regions of high doping in the underlying c-Si layer, it is possible to simultaneously obtain low contact resistance and good surface passivation [Peibst 2014]. Recently, the model was extended to include structural changes in SiO_x that lead to local thickness reductions in where the tunneling probability increases [Peibst 2016]. A simplified schematic of this transport mechanisms is illustrated in Figure 4.12(b). Moreover, the same research group developed a technique not only capable of visualizing pinholes but also capable of quantifying the pinhole density [Tetzlaff 2017b]. To that end, they selectively etched the doped poly-Si layer with 15 % tetramethylammonium hydroxide (TMAH) solution at 80 °C while keeping the interfacial SiO_x as it is, thereby solution also etched the underlying c-Si wafer locally where the pinholes are located.

4.3.7 Conductive atomic force microscopy

In order to investigate the SiO_x integrity and possible transport mechanisms, locally resolved conductivity of the developed contact structure was monitored by means of conductive atomic force microscopy (C-AFM) which combines the high spatial resolution of the AFM and the ability to determine the local electrical current following through the sample[1]. Contacting was done using the c-Si wafer as a grounded electrode and the conductive tip to apply constant negative bias voltage which is called V_{app} hereinafter. The C-AFM setup uses the deflection signal of the tip as height feedback; therefore the current signal is independent of the feedback loop. The impact of various parameters such as oxide thickness, doping concentration and annealing temperature is investigated. For the measurements, symmetric test samples were prepared in order to trace their surface passivation in parallel. Prior to C-AFM measurements, the samples were dipped in 5 % diluted HF for 1 min to remove the surface oxide that had grown during the thermal annealing process. Note that all the contact structures investigated here consist of 10-nm-thick Si(i) inter–layer in between $SiC_x(p)$ and chemical SiO_x.

Impact of applied voltages

The mapping of the local conductivity is performed by applying various negative bias voltages to the sample via the conductive tip. To that end, the sample was prepared with a TMB flow of 1.5 sccm and subsequently annealed at 800 °C for 5 min; to probe the impact of the applied bias

[1] The C-AFM measurements were performed by M. Hyvl from Institute of Physics of the Czech Academy of Sciences, Prague. Contribution is gratefully acknowledged.

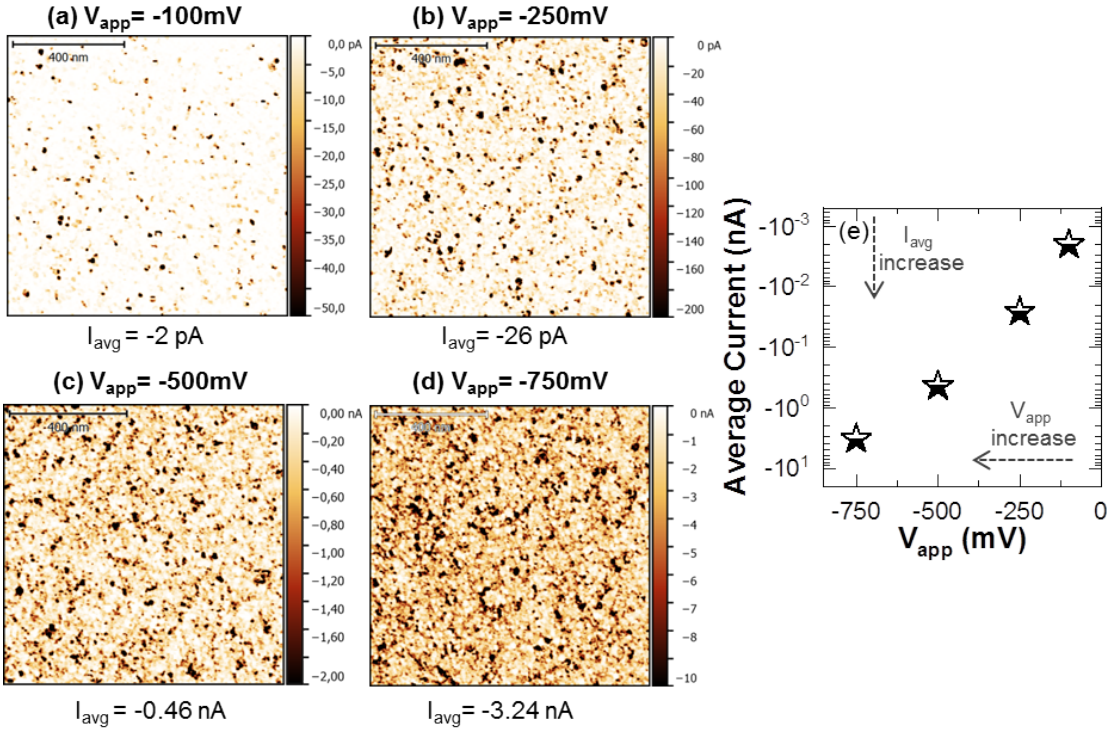

Figure 4.13 – C-AFM current maps of the sample prepared with TMB flow of 1.5 sccm and annealed at 800 °C. The current maps taken with (a) −100, (b) −250, (c) −500 and (d) −750 mV; dark areas indicate the conductive regions due to negative applied voltages.(e)Detected average current computed from images (a–d) as a function of applied bias voltage.

voltage, it is changed from −100 to −750 mV during the C-AFM imaging. Samples annealed at 800 °C were chosen for this analysis to minimize the lateral surface conductivity effect of the doped layer.

Figure 4.13 shows the C-AFM current maps taken with applied voltage of (a) −100, (b) −250, (c) −500 and (d) −750 mV. It is important to note that images demonstrated for visual comparisons should be treated with caution since the current scale bars are different for each image. Even so, the current maps reveal that with applied voltage, the conductive spot density is increasing. For all current maps, the conductive spot size is changing from 5 to 40 nm. To represent the data numerically, the average detected current is calculated from the corresponding C-AFM images and presented in Figure 4.13(e). It reveals the average current is increasing with applied voltages, but only the absolute values of the applied voltages and detected average current should be taken into consideration for comparison. In Figure 4.13(e), the applied bias voltage value is increasing from right to left and the average current is increasing from top to bottom. These measurements indicate that an increase in V_{app} activates or induces more conductive spots. Thus, only the samples taken with same V_{app} should be compared to have reliable results from C-AFM technique.

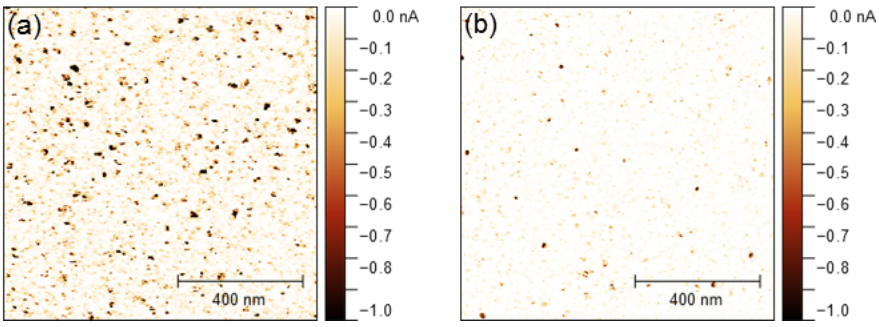

Figure 4.14 – C-AFM current maps of the sample prepared with TMB flow of 1.5 sccm on (a) 1.2-nm-thick SiO_x and (b) 1.8-nm-thick SiO_x taken with V_{app} of −500 mV. Samples were annealed at 800 °C for 0 min.

Impact of oxide thickness

Since the C-AFM technique is open for misinterpretation especially for complex systems with multiple interfaces, we can give only a tentative interpretation of the observed effects. C-AFM is a surface sensitive technique and therefore limited by the lateral conductivity of the deposited top layer, which has to be small in order to enable the required resolution. Aiming to clarify whether the observed conductive spots in the current maps are related with interfacial SiO_x or not, a dedicated experiment was performed. To that end, samples with two different interfacial SiO_x thicknesses were prepared. The first sample features a 1.2-nm-thick SiO_x which corresponds to our standard chemically grown SiO_x. The second sample features a 1.8-nm-thick SiO_x which was produced by performing 20 min UV-O_3 treatment on both sides in addition to the chemical SiO_x. Following the SiO_x growth, both samples received the same PECVD layer prepared with a TMB flow of 1.5 sccm and they were subsequently annealed at 800 °C for 0 min at the same conditions. Figure 4.14 reveals C-AFM current maps taken at −500 mV for the samples with (a) 1.2- and (b) 1.8-nm-thick SiO_x. It is also important to point out the fact that V_{app} used here can be classified as high and induce some conductive spots as seen in previous part [see Figure 4.13]. Since the preparation conditions were identical, the temperature-induced structural changes — layer crystallinity and conductivity — are assumed to be comparable. Therefore the observed difference can thus be attributed to the different interfacial SiO_x thicknesses. It is observed that the reference sample with the 1.2-nm-thick SiO_x reveals more conductive spots compared to the sample with the 1.8-nm-thick SiO_x. This can be explained with the fact that with increased SiO_x thickness, the carrier transport through the SiO_x is hindered, leading to the decreased transport channel density through the layer which can be related to a decreased tunneling probability and also a reduced pinhole density, or a combination of both mechanisms. Inefficient carrier transport for the sample with 1.8-nm-thick SiO_x is also spotted via a contact resistivity that cannot be measured with TLM whereas the contact resistivity value of the sample with 1.2-nm-thick SiO_x is around 90 mΩ cm^2. Overall, this observation approves that the C-AFM current mapping can be used to monitor the influence of interfacial SiO_x in the contact scheme.

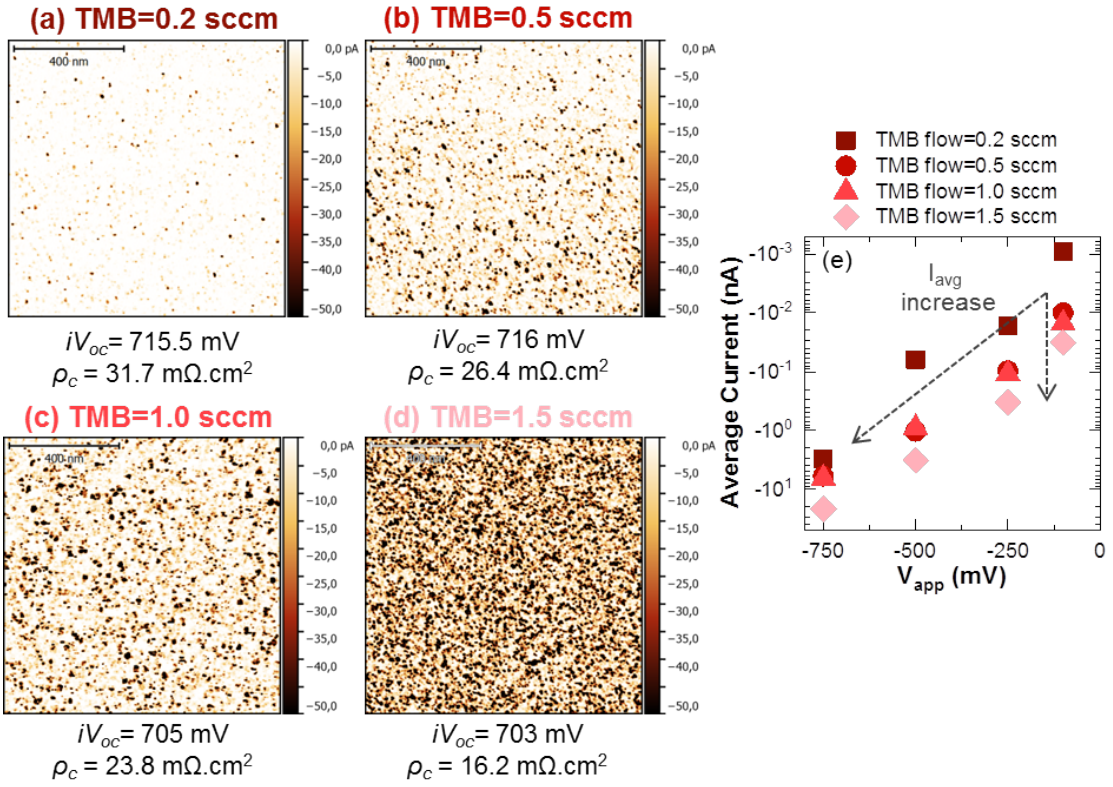

Figure 4.15 – C-AFM current maps taken by V_{app} of −100 mV for the samples prepared with different TMB flows of (a) 0.2, (b) 0.5, (c) 1.0 and (d) 1.5 sccm and annealed at 850 °C for the same annealing dwell time.(e) Detected average current computed from images (a–d) as a function of V_{app}.

Impact of doping concentration

In this part, the impact of the initial doping concentration within the $SiC_x(p)$ layer to the localized conductivity is enquired. C-AFM current maps taken at −100 mV for the samples deposited with different TMB flow and subsequently annealed at 850 °C for 0 min are shown in Figure 4.15(a–d). The numerical presentation of the average detected current calculated from the corresponding C-AFM images as a function of V_{app} is depicted in Figure 4.15(e). The measured iV_{oc} and ρ_c values are noted at the bottom of the current maps for convenience of the interpretation. It is clearly visible that with increased initial doping concentration the density of the conductive spots is increasing, which correlates with deteriorated passivation quality causing a drop of iV_{oc} from 716 to 703 mV. This trend of enhanced average current with initial doping concentration is explicit regardless of the V_{app} values used here. In parallel, the carrier transport is improved as evidenced by the reduced contact resistivity values with increased doping concentration. From a structural point of view, it was reported that varying the boron doping concentration in a small range, as it is the case here, does not affect grain growth significantly [Kim 1988]. Especially for the layers alloyed with C, the effect of doping

on crystallization can be assumed as negligible since the crystallinity of the layer is mainly determined by annealing temperature and C concentration of the layer. Thus, the conductive spot density difference with doping cannot be correlated with the grains of the crystallized layer. A possible reason behind the iV_{oc} drop could be the enhanced boron in-diffusion through the chemical SiO_x layer which also rises the interface defect state density at the SiO_x/c-Si wafer interface as well as the surface recombination velocity. Reduced contact resistivity may originate from the higher doping concentration of the doped layer that can lead to a better electrical contact in between $SiC_x(p)$ and ITO. Another possibility is that the increased boron content leads to a more pronounced breakup, thus bigger pinholes or conductive channels.

Impact of annealing temperature

The annealing temperature is an important parameter that influences the properties of the contact structure in many aspects simultaneously such as crystallinity of the PECVD layer, the integrity and morphological change of the SiO_x, the depth and quantity of diffused dopants, etc. Here the study of local transport characteristics is performed on *as-deposited* and annealed samples at different temperatures for dwell time of 0 min. The samples were produced with a TMB flow of 1.5 sccm.

C-AFM current maps at −100 mV for the (a) *as-deposited* sample and annealed samples at (b) 800, (c) 850 and (d) 925°C are shown in Figure 4.16. The numerical presentation of the average detected current calculated from the corresponding C-AFM images as a function of V_{app} is depicted in Figure 4.16(e). The measured iV_{oc} and ρ_c values are noted at the bottom of the current maps for convenience. In *as-deposited* state, the sample shows very low conductivity, it is also important to note that at this stage, our contact does not show any surface passivation. This is related to the defective nature of the chemically grown SiO_x which benefits from annealing and requires additional hydrogen passivation to decrease the defect density at the chemical SiO_x/c-Si wafer interface to attain good surface passivation. The measured current maps show that the average current is increasing with increased annealing temperature together with the density of the conductive spots represented by the black dots. According to section 4.3.4, annealing temperatures over 875 °C lead to a severe drop of the surface passivation quality; the iV_{oc} value of this sample is 645 mV whereas for the one annealed at 800 °C it is 716 mV. It was previously reported by many research groups that thermal treatment at elevated temperature > 900 °C can lead to extensive pinhole formation in the chemical SiO_x leading epitaxial re–growth of the deposited layer with the same crystalline orientation as the substrate, thereby the wafer is in direct contact with the defective doped layer through the pinholes [Wolstenholme 1987], [Maeda 1989], [Feldmann 2018]. Therefore, the observed iV_{oc} drop can be attributed to the fact that after annealing at 925 °C, the chemical SiO_x may be completely pinhole ridden and the wafer surface is no longer passivated. After annealing at 800 °C, a ρ_c value of ~ 29 mΩ cm^2 is reached and it is further reduced down to ~ 1 mΩ cm^2 by increasing the annealing temperature to 925 °C. This improvement in ρ_c can be thus

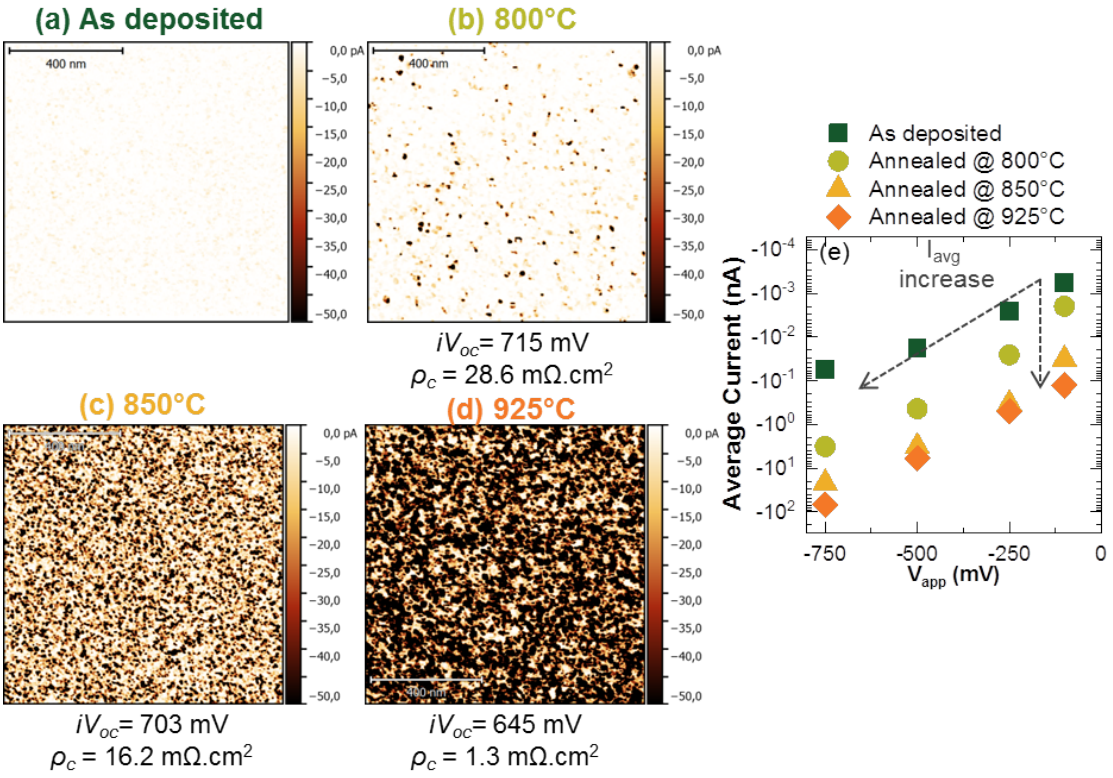

Figure 4.16 – C-AFM current maps taken by applied bias voltage of −100 mV for the samples prepared with TMB flow 1.5 sccm: (a) *As-deposited* and annealed at (b) 800, (c) 850 and (d) 925 °C for the dwell time of 0 min.(e) Detected average current computed from images (a–d) as a function of V_{app}.

explained with more efficient tunneling due to the locally decreased SiO_x thickness, or with more pronounced pinhole formation that increases the direct contact area, both mechanisms can also take place simultaneously.

4.3.8 More insight on structural evolution

Aiming to draw more reliable conclusion about the C-AFM results, a detailed investigation on the microstructural evolution of the contact structure upon annealing was acquired with Raman spectroscopy[2] and TEM.

The onset of the transition from the amorphous Si to the crystalline Si phase of the $SiC_x(p)$ layer upon thermal treatment was studied by Raman spectroscopy. The samples were produced with a TMB flow of 1.5 sccm and annealed for the same dwell time of 0 min. The measured Raman signal is dominated by the structural properties of the region close to the surface

[2]The Raman spectroscopy measurements were performed by M. Ledinsky from Institute of Physics of the Czech Academy of Sciences, Prague. Contribution is gratefully acknowledged.

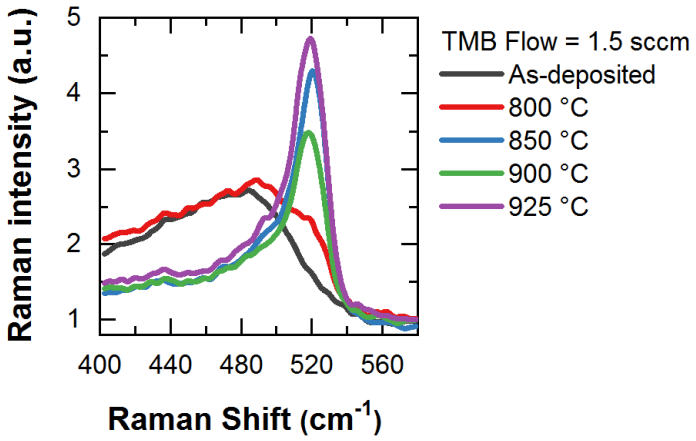

Figure 4.17 – Raman spectra of the *as-deposited* and annealed samples at different temperatures for 0 min.

of the recrystallized layer as a 325 nm UV laser with collection depth of ~ 10 nm was used. In the *as-deposited* state, Figure 4.17 reveals a broad peak at 480 cm^{-1} which indicates the amorphous nature of the deposited layer. For the sample annealed at 800 °C, the Raman spectrum shows a broad peak at about 480 cm^{-1} together with a small rise at 520 cm^{-1}, which indicates the existence of nanocrystals in the amorphous matrix. With increasing annealing temperature to 850 °C and above, the crystalline phase related peak at 520 cm^{-1} becomes more prominent. Additionally, there is an asymmetry with a shoulder towards lower wavenumbers that indicates the presence of an amorphous matrix. Overall, after thermal treatment the contact structure becomes partially crystallized.

Figure 4.18 shows a structural characterization of the samples annealed at 800 and 925 °C, the same samples as in the Raman study, with TEM. The HRTEM micrograph of the sample annealed at 800 °C reveals that the Si(i) inter–layer is more strongly crystallized as the $SiC_x(p)$ layer, probably due to the inhibition of the crystallization process by C. Figure 4.18(b) presents the HRTEM micrograph of the sample annealed at 925 °C, in this case both inter–layer and $SiC_x(p)$ show fairly high crystalline fraction as seen in the corresponding Fourier transforms. Despite the presence of the SiO_x layer, in this annealing condition the obtained iV_{oc} value is only 645 mV which means that almost no surface passivation is left. A closer inspection in Figure 4.18(c) shows that the SiO_x layer is locally disintegrated by pinhole formation, thus creating a direct contact between the c-Si wafer and the re-crystallized layer.

4.3.9 Discussion and a tentative picture for the carrier transport

In the light of these structural investigations, it is important to point out that the samples annealed at temperatures above 850 °C become highly crystalline, consequently their sheet

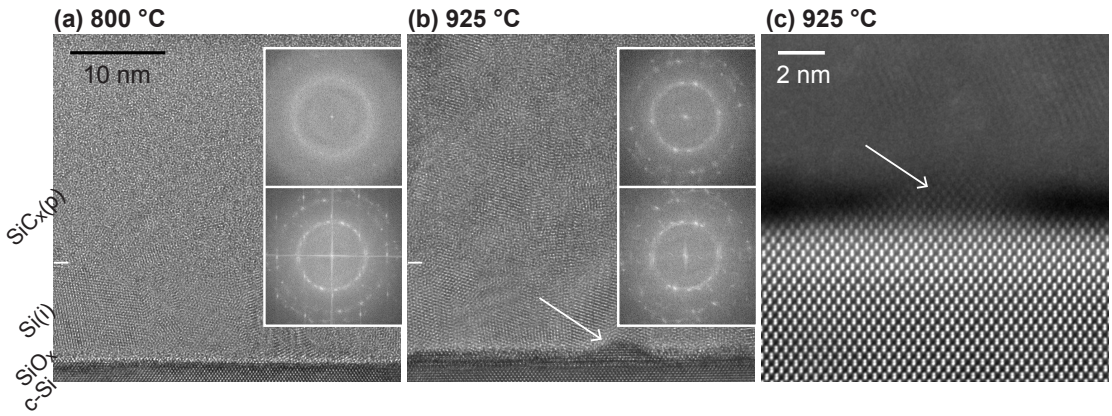

Figure 4.18 – HRTEM micrographs of sample produced with TMB flow of 1.5 sccm and annealed at (a) 800 and (b) 925 °C for 0 min together with Fourier transforms computed from at the position of both the inter–layer — bottom — and the $SiC_x(p)$ — top. (c) STEM HAADF micrograph of the indicated region in (d) taken with higher magnification.

resistance (R_{sheet}) decreases. Low R_{sheet} can explain the strong saturation observed in Figure 4.16(c) and (d) which makes the interpretation of the C-AFM current maps unfeasible. The R_{sheet} value of the layer annealed at 925 °C, measured on a purposely made test sample with 20 nm thermally grown SiO_x, is 11600 Ω/□. This R_{sheet} value is in good agreement with literature values of 15000 Ω/□ measured for TOPCon structure [Kokbudak 2017]. As this value is not very high, we speculate that for the sample annealed at 925 °C, it is not feasible to see the effect of pinholes with C-AFM since the density of the pinholes is too high — one almost every 20 nm along the 1D probing volume of TEM —, hence the measured current is likely to have contribution from more than one pinhole. For the sample annealed at 800 °C, it might be possible to trace the pinholes if they are apart from each other. However Figure 4.16(b) reveals very close distances in between conductive spots. Another possibility can be the fact that the conductive spots reveals the change of local surface conductivity. Thus, with C-AFM it is not easy to derive a solid interpretation and the measurement is not reliable for the highly crystallized contacts. Nevertheless, the presented images follow a meaningful trend of increased conductive spot density with increased doping concentration, increased temperature and decreased SiO_x thickness. The observed non-uniform current distribution at the surface suggests a non-homogenous SiO_x disruption (local thickness reduction or pinhole) that would assist local carrier transport either via tunneling or direct local contacts. It appears that the transport may take place through preferential local transport channels formed within the deposited layer upon thermal treatment, starting from the region where SiO_x thickness reduces or pinholes formed.

To sum up, in the *as-deposited* state of the discussed contact structure, SiO_x is perfectly intact as seen in Figure 4.1(a). Upon annealing, some atomic defects, e.g. O vacancies, in the SiO_x

start to cluster, yielding a local thinning and ultimately complete breakup, so-called pinhole formation. This thermally activated process strongly depends on the initial atomic defect concentration in the SiO_x and also its stoichiometry. Interface reactions between the SiO_x and the Si-based layer might also play an important role which could explain the different behaviour of our contact with and without Si(i) inter–layer and the reaction of the C atoms with chemical SiO_x leading to its complete annihilation. In general, the current flow is enhanced in regions with thinner SiO_x due to increased tunneling probability. If the SiO_x is locally thinned down enough or even disappears, the localized direct current flow takes place, and current crowding in the c-Si dominates the resistance. It is observed that exaggerated thermal budgets (T > 850 °C for chemical SiO_x , T > 950 °C for thermal SiO_x) yield a strong perforation of the SiO_x, and consequently a poor surface passivation quality. The observation of pinholes / re-crystallized areas in TEM as seen in Figure 4.18(c) can be accepted as an indication to that. In literature it was reported that the optimum annealing conditions depend strongly on the SiO_x, e.g. stoichiometric and/or thicker oxides can tolerate higher annealing temperatures before exhibiting pinholes [Gan 1990], [Moldovan 2015]. In principle, higher annealing temperatures are preferable as they improve (i) the crystallinity of the deposited layer and (ii) the passivation quality of the c-Si/SiO_x interface by lowering the density of the defect states. On the other hand, strong pinhole formation that damages the surface passivation has to be avoided. Whether the few pinholes contribute significantly or not to the total current transport depend on the SiO_x thickness. Thinner oxides may also allow sufficient tunneling in the unaltered regions, which than can dominate the charge-carrier transport.

4.4 Conclusions

In this chapter the development of a thermally stable hole-selective passivating contact using *in-situ* doping is presented. The contact structure consists of a chemically grown SiO_x/Si(i) inter–layer/$SiC_x(p)$ layer stack. Detailed structural analysis showed that a C-free Si(i) inter–layer is needed to prevent a chemical reaction between carbon atoms in the $SiC_x(p)$ layer and the adjacent SiO_x. The optimum inter–layer thickness is determined to be 10 nm, resulting in the best surface passivation and low specific contact resistivity of the high-low junction after the thermal treatment. Doping profiles measured with SIMS revealed that introducing an inter–layer does not significantly change the diffusion depth in the c-Si wafer. Instead it probably decreases the recombination current at the chemical SiO_x/c-Si wafer interface. It is also shown that the hydrogenation process is essential to obtain good surface passivation. Hydrogenation using a SiN_x overlayer is found to be more efficient than forming gas annealing for the presented passivating contact. Following further optimization of the carbon concentration, doping concentration and annealing conditions, two optimum conditions for symmetric lifetime test samples are presented: (i) a sample prepared with a TMB flow of 1.5 sccm and annealed at 800 °C for 5 min attaining an iV_{oc} value of 718 mV (J_0 of 11.5 mA/cm^2) and ρ_c of 17 mΩ cm^2, and (ii) a sample prepared with a TMB flow of 0.5 sccm and annealed at 850 °C attaining an iV_{oc} value of 716 mV (J_0 = 11.6 mA/cm^2) and ρ_c of 28 mΩ

cm^2. As the developments were performed on a *p*-type c-Si wafer, this contact would be an ideal replacement for PERC designs in industrial solar cells that employ a diffused $POCl_3$ front side. Indeed, such a design eliminates the need for laser structuring of the passivation layer, which is currently necessary at the rear of PERC.

The charge-carrier transport mechanism for the $SiC_x(p)$ contact is investigated by means of C-AFM and TEM. It is found that after thermal treatment local conductive spots are observed in C-AFM. The density of the conductive spots increases with increased doping concentration, increased temperature and decreased SiO_x thickness. In the case of subjecting the samples to thermal treatment at temperatures above 850 °C, the C-AFM image is probably saturated due to the low sheet resistance of the doped contact layer and high areal density of the pinholes that are located close to each other. Thus it is not possible to clarify the effect of the pinholes. In contrast, for the samples annealed at 800 °C, it might be still feasible to see the impact as we detect the difference in the current map when the SiO_x thickness is changed. We tentatively interpret that these conductive points observed on the samples annealed at 800 °C might not indicate the pinholes directly but the localized preferential charge-carrier transport in regions where the SiO_x is thinner or even absent (i.e. at the position of a pinhole formed as a result of thermal treatment).

5 Hybrid concept: Solar cells with boron-doped silicon-rich silicon carbide as rear contacts

Summary

The potential of the contact structure based on a chemically grown thin oxide, an intrinsic silicon [Si(i)] inter–layer, and an *in-situ* boron-doped silicon-rich silicon carbide [$SiC_x(p)$] layer is investigated at the device level by realizing proof-of-concept hybrid solar cells. A standard silicon heterojunction contact made of an intrinsic amorphous silicon passivation layer and a phosphorus-doped amorphous silicon electron-selective layer is employed as a front contact in the hybrid cell structure. After optimization of the process flow and contact structure, a conversion efficiency of up to 22.3 % with a V_{oc} of 707 mV, *FF* of 81.8 % and J_{sc} of 38.6 mA/cm^2 is achieved on a *p*-type c-Si wafer. The influence of the Si(i) inter–layer between the chemical SiO_x and $SiC_x(p)$ layers is assessed at the cell level. It is observed that the optimum Si(i) inter–layer thickness depends on the carbon concentration in the $SiC_x(p)$ layer. Temperature-dependent *J-V* measurements are performed to study the impact of the different carbon concentrations in the developed rear contact.

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5.1 Introduction and motivation

A primary factor that limits the conversion efficiency of commercial homojunction c-Si solar cells is the voltage loss due to the recombination of charge carriers at the direct metal/semi-

conductor contact. A conventional way to mitigate this loss is to introduce a highly doped region below the metal contact that reduces the minority-carrier density and consequently charge-carrier recombination. This approach is already in use for commercial aluminum back surface field (Al-BSF) solar cells. Reducing the recombination losses further can be accomplished by restricting the metallized contact area as in passivated emitter and rear cell (PERC) technology. This is currently an emerging concept at the industrial level as it promises an efficiency gain while still being compatible with existing production lines. However, a reduced contact area fraction also leads to increased series resistance; as a consequence, PERC technology is inherently limited by a trade–off between reduced recombination and increased series resistance. In other words, they suffer from a trade–off between V_{oc} and *FF*. Apart from that, the realization of PERC requires additional fabrication steps for deposition and patterning of an insulating layer, which increases the process complexity. Potentially, the abovementioned limitations can be overcome by using passivating contacts which are applied to the full-area without the need for patterning.

Based on the results obtained in Chapter 4, the full-area hole-selective passivating contact prepared by PECVD with *in-situ* doping clearly outperforms the conventional rear side of *p*-type c-Si solar cells in terms of selectivity and surface passivation. In order to validate its applicability at the device level, proof-of-concept hybrid solar cells are realized. The hybrid solar cells feature chemical SiO_x/Si(i)inter–layer/SiC_x(*p*) for the rear contact and a standard silicon heterojunction (SHJ) front contact made of intrinsic amorphous silicon [a-Si:H(*i*)] and phosphorus-doped amorphous silicon [a-Si:H(*n*)]. The use of a heterojunction contact at the front side is motivated by the fact that a-Si:H(*i*) provides quasi-perfect chemical passivation to the front surface and the V_{oc} of the cells would be limited by the rear contact. This gives an opportunity to determine the possible V_{oc} gain that can be achieved in the case of integrating our contact to industrial *p*-type solar cells. Additionally, since the front-side processing temperature does not surpass 200 °C, it provides a suitable architecture to explore properties of the rear junction at the cell level without altering its properties. On the other hand, the *FF* of the hybrid cell is likely limited by the contact resistivity of the amorphous contact layer to the front TCO. Nevertheless, the proof-of-concept solar cells are a useful vehicle to demonstrate the promising surface passivation and electrical properties of the presented junction at the device level.

5.2 Solar cell fabrication: First attempt

Following the detailed analysis of the symmetric test samples presented in the Chapter 4, selected samples were further processed to form solar cells. The process flow for cell fabrication and a sketch of the final hybrid solar cell structure are depicted in Figure5.1. The process flow started with standard chemical cleaning and the formation of wet chemically grown SiO_x in 68 wt % HNO_3 at 80 °C for 10 min. Subsequently, a layer stack consisting of a 10-nm-thick Si(i) inter–layer and an ~ 20-nm-thick *in-situ* boron-doped SiC_x(*p*) layer was deposited on both sides by plasma-enhanced chemical vapour deposition (PECVD). Both layers are amorphous

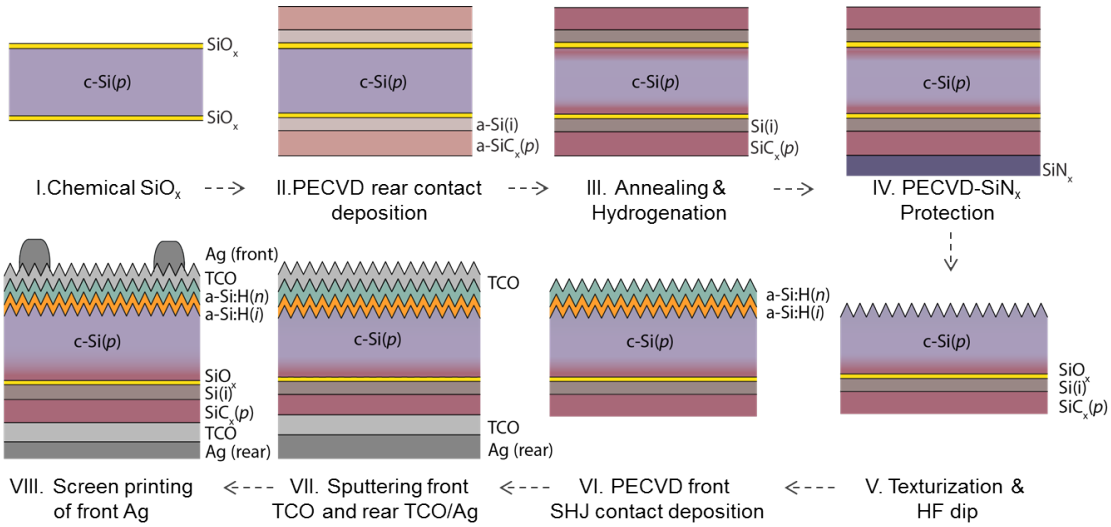

Figure 5.1 – Process flow for cell fabrication and final device structure. A diffused buried junction in the c-Si(p) wafer created by in-diffusion of boron from the $SiC_x(p)$ layer. The structural change of the deposited layers upon annealing are indicated in the sketch by a change in the colors. Layers are not drawn to scale.

in their *as-deposited* state. Following the PECVD step, the samples were annealed in inert gas atmosphere using heating and cooling ramps of 10 and 2 °C/min, respectively, to form in-diffused buried junctions and to crystallize the PECVD layers. The furnace was opened at 660 °C and the samples were hydrogenated to passivate electronic defects at the chemical SiO_x/c-Si wafer interface. In Figure 5.1 steps I, II, and III show the preparation of symmetric test samples which were used to measure the effective-lifetime curves. After this stage, selected samples were further processed to form solar cells. To that end, the rear side of the samples was protected with PECVD deposited SiN_x, the layer stack and the diffused region on the front side was etched back and textured in a potassium hydroxide solution as presented in Figure 5.1 with steps IV and V. After removal of the rear SiN_x protection layer, the wafers were wet chemically cleaned according to the RCA procedure [Kern 1990] and dipped in 5 % diluted HF to remove the native oxide. Subsequently, a 7-nm-thick intrinsic a-Si:H passivation layer and a 6-nm-thick phosphorus-doped a-Si:H(n) electron-selective contact layer were prepared by PECVD on the textured front side. To extract the collected carriers efficiently and to increase the light in-coupling into the wafer, 70- and 116-nm-thick transparent conductive oxide — here, indium tin oxide (ITO) — were sputtered onto the front and rear sides of the cells, respectively. All given thicknesses represent reference thicknesses measured on planar surfaces. The active cell area was defined by depositing the ITO layers through a 2.2 cm × 2.2 cm shadow mask. A full-area silver reflector/contact was sputtered onto the rear side, and silver paste was screen-printed to realize the front metallization grid, which is then followed by curing for 25 min at 190 °C in a belt furnace.

For the first demonstration, two different dopant — TMB — flows were used. The iV_{oc} and

Table 5.1 – iV_{oc} and J_0 values of cells A and B after a-Si:H(*i*/*n*) deposition and summary of the completed hybrid cells parameters. Adapted with permission from [Nogay 2016b]. Copyright ©2016, American Chemical Society.

Cell	iV_{oc} [mV]	J_0 [fA cm^{-2}]	V_{oc} [mV]	J_{sc} [mA cm^{-2}]	*FF* [%]	Efficiency [%]
Cell A	713	12.8	678.0	36.95	77.2	19.4
Cell B	717	12.3	694.7	37.20	79.1	20.4

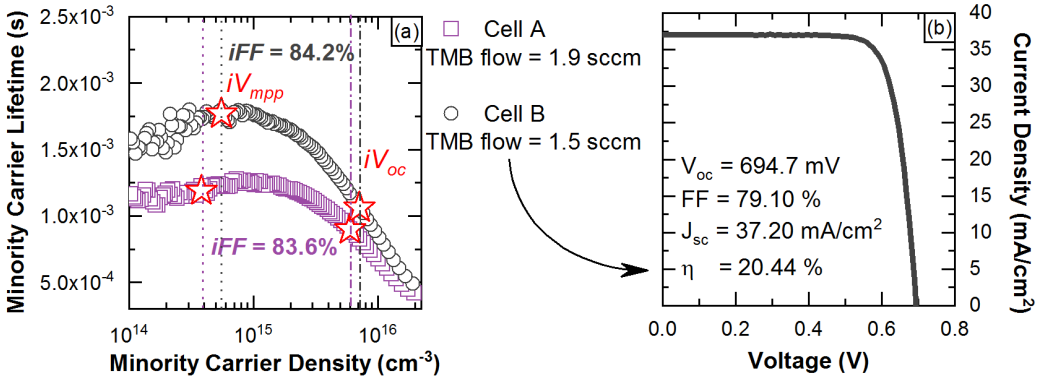

Figure 5.2 – (a) Effective carrier lifetimes of the samples after a-Si:H(*i*/*n*) front side PECVD deposition as a function of the excess-carrier density together with associated implied voltages at maximum power point — dotted line — and open circuit conditions — dash-dot line. (b) Light *J*-*V* characteristic of the cell B. Adapted with permission from [Nogay 2016b]. Copyright ©2016, American Chemical Society.

J_0 values after deposition of the a-Si:H(*i*/*n*) layer stack together with *J*-*V* parameters of the completed hybrid cells are given in Table 5.1 for the best cells out of three on each wafer. The characteristic form of the lifetime curve can reveal direct information on the nature of the surface passivation and make it possible to discern the influence of band bending — repelling the minority carriers from the surface — and defect passivation — saturation of the Si dangling bond on the surface. Leendertz *et al.* reported that with reduced interface defect density, the lifetime curve shifts upward while maintaining its basic shape, whereas in the case of having insufficient band bending — or fix charges —, lifetime curve reveals tailing at low-injection level ($\Delta n < 10^{15}$ cm^{-3}) [Leendertz 2011]. In Figure 5.2(a), the injection dependence of the minority-carrier lifetimes for the samples after deposition of the a-Si:H(*i*/*n*) front side together with the associated implied *FF* (*iFF*) and implied V_{oc} (iV_{oc}) at maximum power point and open-circuit conditions are shown. The expression "implied" is used for quantities derived from the injection-dependent lifetime measurements. After deposition of the a-Si:H(*i*/*n*) stack on the front side, for both samples, tailing is observed at low-injection level which implies a weak minority-carrier repelling. Even though the tailing is slightly more pronounced for cell B prepared with a 1.5 sccm TMB flow, the same sample also shows better chemical passivation. Overall, both cells prepared with TMB flows of 1.9 sccm (cell A) and 1.5 sccm (cell B) yield an

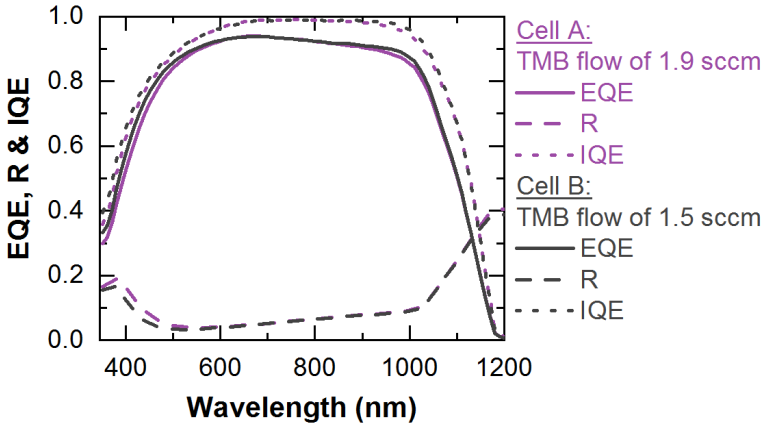

Figure 5.3 – EQE, R, and IQE spectra of cell A and cell B. Adapted with permission from [Nogay 2016b]. Copyright ©2016, American Chemical Society.

iV_{oc} value of above 710 mV and a J_0 value of around 13 fA/cm^2. However, cell A, the cell with the more heavily doped SiC$_x$(p) layer at the rear side, has slightly inferior cell parameters. The observed difference between iV_{oc} and final V_{oc} is 35 mV for cell A and 23 mV for cell B. This could be related to non-optimized fabrication processes that detrimentally reduces the surface passivation quality. Furthermore, for the carrier extraction point of view, a contact resistivity value of 17 mΩ cm^2 was measured for the sample prepared with a TMB flow of 1.5 sccm on the p-type wafer.Assuming that this were the only contribution to the series resistance, the *FF* should be reduced by 0.04 % with respect to the *iFF*. However, the measured *FF* is very likely limited by the standard SHJ electron contact at the front which has a contact resistivity of 200 mΩ cm^2 measured on the n-type wafer, c.f. Chapter 3 section 3.4.

In terms of optics, both cells are expected to behave similarly since they were processed with the same fabrication steps. Nevertheless, the texturization might differ because they were processed on different days using a process that was not optimized for this purpose. Figure 5.3 depicts the EQE, R, and IQE spectra for the cells A and B. Cell A exhibits a considerably higher R in the blue part of the spectrum, which is the signature of a non-optimized front texturization. This yields a reduced J_{sc} and it could also have negative impact on V_{oc} and *FF*. The J_{sc} of 37–38 mA/cm^2 is typical value for standard SHJ solar cells — without a second anti-reflective coating — and it is limited by parasitic absorption in the a-Si:H layers on the front side. For IR-wavelengths, the lower spectral response of the sample with higher doping concentration can be explained with slightly higher recombination losses.

In conclusion, the application of the chemical SiO$_x$/Si(i) inter–layer/SiC$_x$(p) contact structure allows good rear passivation and demonstrates a decent cell performance, enabling V_{oc} = 694.7 mV and *FF* = 79.1 %. Compared to PERC cells, the presented rear eliminates the need for patterning processes and showed convincing V_{oc} values already on the first attempt. However, its non-optimized fabrication procedure requires many process steps and sample

manipulations that cause significant and undetermined losses. Hence, we conclude that the process flow has to be improved to show the real potential of the rear contact structure presented here.

5.3 Solar cell fabrication: Improved process

Aiming for improved solar cell parameters, the cell manufacturing process was simplified by using front-side-textured wafers from the beginning. The simplified process flow together with the final hybrid cell scheme is depicted in Figure 5.4. After standard wet-chemical cleaning, protective SiN_x layer was deposited on the rear side of the bare c-Si wafer by PECVD, restricting the texture etch to the front side. After stripping off the SiN_x, the wafers were cleaned and chemically oxidized in HNO_3 as described in section 5.2. PECVD deposition of the Si(i)/SiC_x(p) was performed to the rear side of the cells followed by annealing and hydrogenation. From here on a different annealing furnace was used and furnace opening temperature was set to 720 °C. The effect of protecting the front side of the cells with a thick, PECVD deposited SiO_x sacrificial layer was also investigated — not shown here — but no significant difference was observed in between the cells processed with or without SiO_x front protection. Following the hydrogenation step, the samples were further cleaned in piranha solution — 3:1 mixture of sulphuric acid (H_2SO_4) with hydrogen peroxide (H_2O_2) — and dipped in 5 % diluted HF to remove the native oxide. The simplification is made possible by the chemical stability of the SiC_x(p) layer at the rear. The rest of the process is identical with the first version described in section 5.2. Thanks to the simplified process, the number of steps so as the sample manipulation was reduced significantly. A shortfall of the improved process flow is the fact that the lifetime curves cannot be measured before front a-Si:H(i/n) deposition due to the high recombination current of the unpassivated front side.

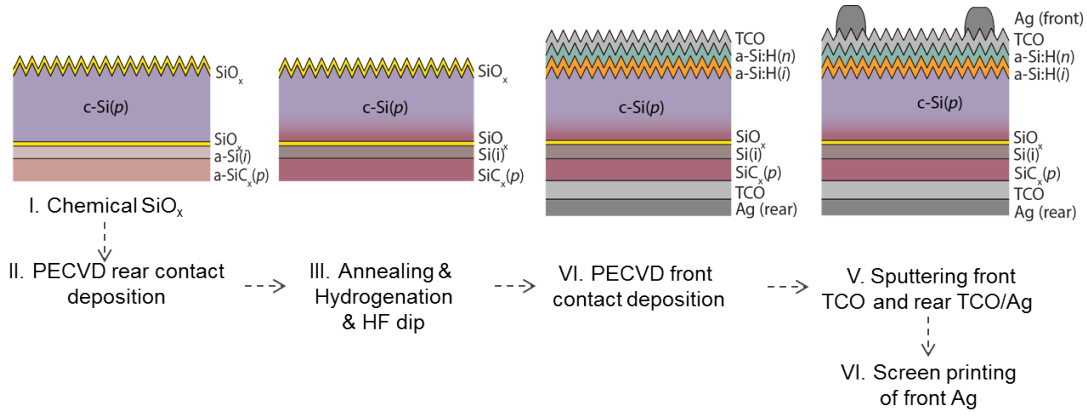

Figure 5.4 – Improved process flow for cell fabrication and the final hybrid device structure. Layers are not drawn to scale.

5.4 Results and discussion: Impact of TCO and deposition parameters

In this section, first the impact of TCO deposition on the hole-selective SiO_x/Si(i)/SiC_x(*p*) contact layer is determined. To that end, the injection-dependent lifetime characteristics of symmetric test structures are probed before and after TCO deposition as well as after curing the samples at low temperatures (< 300 °C). Then, the impact of different deposition parameters, such as doping concentration, annealing dwell temperature, SiC_x(*p*) layer thickness, SiC_x(*p*) carbon concentration and Si(i) inter–layer thickness in the rear contact structure are investigated on device level, using the hybrid cell concept with simplified process flow. Finally, the charge-carrier transport of the hybrid cells that feature rear contacts with different carbon concentration is investigated by means of temperature-dependent light *J*-*V* measurements in a large temperature range from −80 to +80 °C with 5 °C intervals. Tracking the light *J*-*V* characteristic of the cells at low temperatures provides insight in the transport barriers that photogenerated carries may confront during collection across the different device interfaces.

5.4.1 The effect of transparent electrodes on the surface passivation

For the standard SHJ solar cells, the front TCO is necessary to ensure good lateral transport of the charge carriers to the metallic grid while the rear TCO is essential to mitigate the coupling of evanescent waves to the metal rear reflector, so-called plasmonic losses [Holman 2012]. As the TCO layers have a significant role in SHJ solar cells, the impact of their deposition on surface passivation was widely investigated for various TCOs using several deposition methods [Demaurex 2014a], [Macco 2014], [Tomasi 2016b]. Earlier, it was reported that TCO sputtering may damage the underlying a-Si:H surface passivation layer and increase the carrier recombination either in the form of deep-defects — Si dangling bonds — [De Wolf 2008] or due to insufficient band bending within the c-Si. The cause of such sputter-induced defects can be attributed to the plasma luminescence and/or ion-bombardment during the sputtering process, while the issue of band bending can be attributed to work function mismatch in between the doped layer and the TCO. It was also established that subsequent low-temperature annealing, so-called curing, recovers the surface passivation substantially. Tomasi *et al.* reported that the electrical properties of TCO layers can affect significantly the surface passivation of SHJ contacts. It was found that highly doped TCOs should be avoided to contact a-Si:H(*p*) layers whereas they can be beneficial to contact a-Si:H(*n*) layers due to the reduced and increased work function mismatch, respectively [Centurioni 2003], [Tomasi 2016b]. It was also seen that the effect of TCO deposition is less detrimental for a-Si:H(*n*) layers than a-Si:H(*p*) in standard *n*-type SHJ solar cells. Inspired by these observations, the effect of TCO deposition on our hole-selective passivating contact based of chemical SiO_x/Si(i) inter–layer/SiC_x(*p*) layers stack is studied.

In this experiment, an extended investigation is performed with various TCOs such as sputtered tungsten-doped indium oxide (IWO), aluminum-doped zinc oxide(ZnO:Al), indium tin

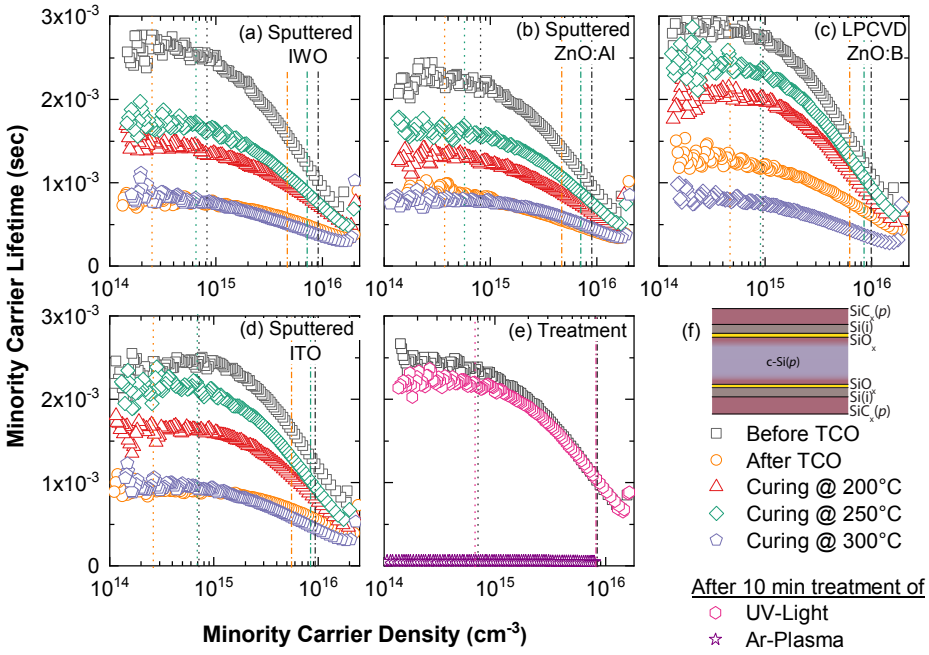

Figure 5.5 – Measurements of minority-carrier lifetime characteristics as a function of excess minority-carrier density for p-type c-Si wafer featuring a symmetric chemical SiO_x/Si(i)/$SiC_x(p)$ hole selective passivating contact after depositing (a) IWO, (b) ZnO:Al, (c) ZnO:B, (d) ITO overlayer, as well as after curing at different temperatures. (e) The effect of 10 min UV light treatment and 10 min argon plasma treatment on the lifetime characteristic of the symmetric test sample. Dotted lines and dash-dot lines denote iV_{mpp} and iV_{oc} , respectively for the lifetime curves with corresponding color.

oxide (ITO) and low pressure chemical vapor deposited (LPCVD) boron-doped zinc oxide (ZnO:B)[1]. Symmetric test samples featuring chemical SiO_x/Si(i)/$SiC_x(p)$ layers stack on FZ p-type c-Si wafers, as depicted in Figure 5.5(f), were prepared and the TCO layers were deposited on both sides. Figure 5.5 reveals the evolution of the injection-dependent lifetime characteristics before and after TCO deposition with grey and orange open symbols, respectively. Dotted lines and dash-dotted lines denote associated implied voltages at maximum power point (iV_{mpp}) and open-circuit condition (iV_{oc}), respectively for the lifetime curves with corresponding color — for clarity only the values for before TCO, after TCO and the best recovery condition of curing at 250 °C are marked. For all TCOs investigated here, a drastic drop is observed in both iV_{oc} — high-injection level — and iFF — low-injection level — after the TCO depositions, regardless the employed technique. For all sputtered TCOs, the measured iV_{oc} values of 728–730 mV drop to 708–710 mV while the iFF values drop from 85.9 to 84.5 %. For LPCVD ZnO:B, the iV_{oc} drops to 716 mV and the iFF to 85.1 %, meaning that the reduction is still noticeable but less severe. Generally, LPCVD is classified as an ultra-soft deposition

[1] IWO, ZnO:Al and ZnO:B depositions were performed by J. Diaz and L. Ding from CSEM. Their contribution is gratefully acknowledged.

technique as it is devoid of plasma radiation and ion bombardment, encountered in plasma based deposition processes such as sputtering. Succeeding the TCO overlayer deposition, samples were cured at the temperatures of 200, 250 and 300 °C for 10 min on a hot plate. With curing at 200 °C, a slight improvement is observed in lifetime curves, the best recovery is obtained with curing at 250 °C for all samples investigated here. Especially the samples with ITO and ZnO:B reveal better recovery than those with IWO and ZnO:Al. After curing the sample with LPCVD ZnO:B at 250 °C, iV_{oc} of 726 mV and *iFF* of 85.7 % are reached while for the sample with ITO iV_{oc} value of 725 mV and *iFF* of 85.5 % are achieved. Annealing at 300 °C leads to severe degradation not only of iV_{oc} but also of the lifetime at low-injection level.

In an attempt to assess the role of plasma luminescence — UV exposure — and ion bombardment on the surface passivation, a dedicated experiment was performed where one part of a sample was exposed directly to argon plasma while the other part was covered with quartz glass that has 10 % transparency at 7.8 eV. The exposure was performed at room temperature and substrate temperature remained below 70 °C. In a similar experiment with standard SHJ solar cells, it was reported that the co-deposited lifetime samples show a 27 % reduction in lifetime at an excess carrier density of 10^{15} cm^{-3} when they are covered by quartz glass and a 96 % reduction in lifetime when they are exposed to direct argon plasma [Demaurex 2014b]. Figure 5.5(e) exhibits that UV light exposure affects our passivating contact less significantly; it causes a 2 mV loss in iV_{oc} and less than 1 % loss in *iFF*, which can be considered in the range of the QSSPC measurement error. Conversely, exposing the sample to direct argon plasma for 10 min is detrimental for surface passivation.

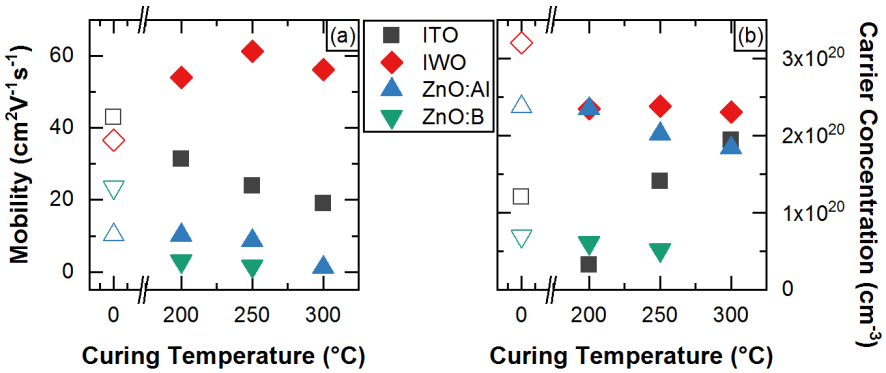

Figure 5.6 – Mobility and carrier concentrations extracted from Hall measurement for ITO, IWO, ZnO:Al and ZnO:B layers: *As-deposited* (open symbols) and as a function of curing temperatures for 10 min (filled symbols).

The TCOs used in this experiment were designed for the rear side application. As the rear TCO is covered by metallic layer, it is not an important requirement to have a good lateral transport within the TCO. Consequently, higher resistivities and lower carrier concentrations can be tolerated which allows the use of more transparent layers and thus improve the J_{sc} values [Holman 2013]. Additionally, the mobility and carrier density of the TCO can be signifi-

cantly altered by annealing at temperatures of around 200 °C. Figure 5.6 shows the electrical characteristic of the sputtered TCOs obtained from Hall measurement on reference samples deposited on glass substrate. Note that the properties of the TCOs can vary depending on the substrate. The zero position indicates the measured values for *as-deposited* samples indicated with open symbols. Compare to IWO and ZnO:Al, Figure 5.6 reveals that ITO has higher mobility and the lower carrier concentration in *as-deposited* state. Upon annealing for 10 min, the mobility of the ITO is decreasing gradually with augmenting annealing temperature. Conversely, IWO exhibits an improved mobility, reaching its optimum value of 62 $cm^2V^{-1}s^{-1}$ after annealing at 250 °C, in parallel to that its carrier concentration diminishes. ZnO:Al used in this experiment shows low mobility and high carrier concentration before and after annealing. LPCVD ZnO:B reveals a decent mobility value and the lowest carrier density in its *as-deposited* state, whereas after curing the mobility values drop to the values lower than the rest. Table 5.2 shows the measured ρ_c values after curing at 250 °C for 10 min. For all sputtered TCOs, fairly low ρ_c values below 20 mΩ cm^2 is obtained, whereas for LPCVD ZnO:B, the measured ρ_c value is rather high for possible device integration.

Table 5.2 – Summary of the TCO thicknesses and measured ρ_c for SiO_x/Si(i) inter–layer/SiC_x(p) contact after curing at 250 °C.

	IWO	**ZnO:Al**	**ZnO:B**	**ITO**
TCO Thickness [nm]	87	63	990	92
ρ_c **[mΩ cm^2]**	19.5	11.3	174.4	19.5

Based on the results obtained here, ITO appears to be the best option among the tested TCOs for surface passivation since it recovers quite efficiently. In parallel to that, it reveals low ρ_c values of 15.6 and 19.5 mΩ cm^2 after curing at 200 and 250 °C, respectively. ITO sputtering leads to an iV_{oc} loss of 5 mV while the IWO and ZnO:Al sputtering leads up to 11 mV loss. Even though the iV_{oc} difference before TCO deposition and after curing is slightly lower for the LPCVD ZnO:B, it reveal high ρ_c values. Thus, ITO has superior electrical properties compared to ZnO:B, especially for the thicknesses below 1 μm. From an electrical point of view, IWO presents the most promising mobility value after annealing at 250 °C which also leads to an optimum recovery with respect to surface passivation. We note that 2 mV of the total iV_{oc} loss might be originate from UV exposure and the rest might be due to the work function mismatch in between the doped layer and the TCO. Since the degradation in surface passivation is also observed for LPCVD deposited layers, we conclude that the samples presented here does not necessarily suffer from sputtering damage alone, even though it might have slight contribution.

5.4.2 Doping concentration and annealing temperature

After determining the most convenient TCO to use in our device architecture, proof-of-concept hybrid solar cells were realized using the simplified fabrication process described in section

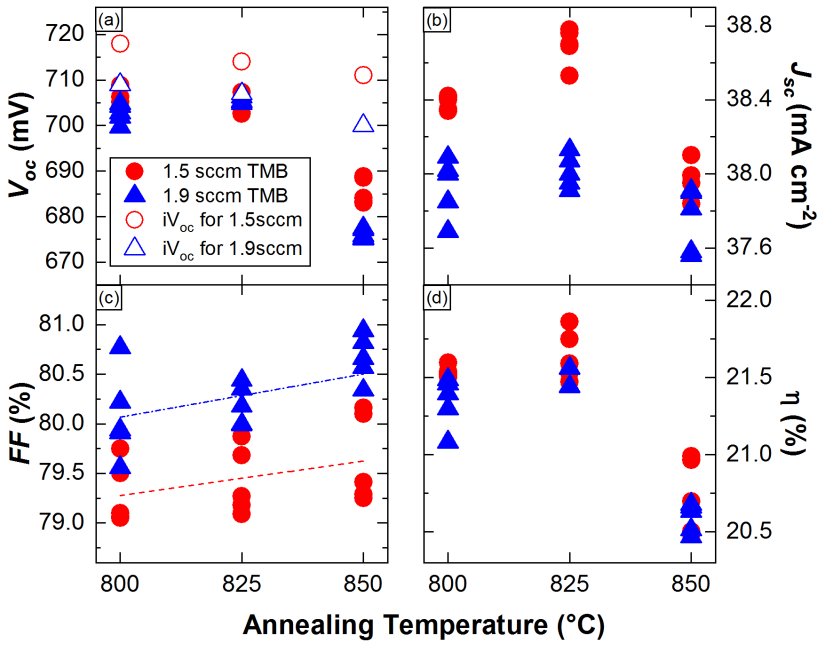

Figure 5.7 – Output characteristics of the hybrid solar cells exhibiting the boron-doped $SiC_x(p)$ layer produced with the TMB flow of either 1.5 or 1.9 sccm and annealed at dwell temperatures of 800, 825, and 850 °C for 5 min. Adapted with permission from [Nogay 2017]. Copyright ©2017, Elsevier.

5.3. In a first set of cells, the impact of doping concentration and annealing temperature were investigated more systematically. The rear side of the cells presented in this section comprise 10-nm-thick Si(i) inter–layer between the chemical SiO_x and the 20-nm-thick $SiC_x(p)$. Figure 5.7 shows the obtained output characteristics of the hybrid cells featuring a boron-doped layer produced with a TMB flow of either 1.5 or 1.9 sccm and annealing at temperatures of 800, 825, and 850 °C for 5 min. The measured iV_{oc} values for the symmetric test samples of rear contacts prepared in parallel to the cell process are indicated with open symbols in Figure 5.7(a).

It is observed that the symmetric test samples produced with a TMB flow of 1.5 sccm show ~ 10 mV higher iV_{oc} values compared with the ones produced with 1.9 sccm for all annealing conditions. Figure 5.7(a) further shows that the V_{oc} values are mostly following the observed iV_{oc} trend for the rear side contact as the V_{oc} is limited by the rear. For the annealing temperatures of 800 and 850 °C, the V_{oc} of the cells with TMB flow of 1.5 sccm are higher, while for those annealed at 825 °C, both doping conditions exhibit almost the same V_{oc} values. Overall, for the cells annealed at 800 and 825 °C, the difference between iV_{oc} and V_{oc} is changing from 2 to 10 mV, for the cells annealed at 850 °C this difference is higher than 20 mV. The iV_{oc} values measured before the metallization are in line with the iV_{oc} values for the symmetric test samples of the rear contact, e.g. for the sample with TMB flow of 1.5 sccm and annealed at 800 °C, an iV_{oc} value of 717 mV with a corresponding J_0 of 9.9 fA/cm^2 is measured. Based on results

from section 5.4.1, ~ 1 mV of the iV_{oc} and V_{oc} difference before and after TCO deposition may originate from the UV exposure of the rear contact. A possible interpretation for the rest may be a combination of work function mismatch and the formation of dark diode. The latter is relevant to the fact that passivating contacts were deposited on the full-area, however a 2.2 cm × 2.2 cm metallic shadow mask was used to determine the active cell area during TCO deposition and also a 2 cm × 2 cm black mask is used for the light *J-V* measurements. Since the lateral conductivity of the rear $SiC_x(p)$ increases with increasing annealing temperature, the area of the dark diode is increased accordingly. Another possible reason for the more pronounced difference in between iV_{oc} and V_{oc} for the sample annealed at 850 °C might be the stronger boron in-diffusion into the c-Si wafer that leads to lower dopant concentration within the $SiC_x(p)$ layer and consequently a higher work function mismatch in between TCO and doped layer. The best V_{oc} value reached in this set is 709 mV with the cell produced with a TMB flow of 1.5 sccm and annealing at 800 °C for 5 min.

According to Figure 5.7(b), the obtained J_{sc} values are higher for the samples produced with 1.5 sccm TMB flow. Since all the hybrid cells presented here have similar front sides, we presume that the difference is associated with the recombination losses which are greater for the samples with higher doping concentration. This effect is also observed for the cells produced in first demonstration presented in section 5.2 (see Figure 5.3). The measured J_{sc} is much higher for the sample with 1.5 sccm TMB flow and annealed at 825 °C compared to the rest. This might be due to the fact that even though the same sputtering parameters are used for the front ITO depositions, it is possible to observe some fluctuations in the layer properties from one deposition to another. Thus it is difficult to exclude that the front ITO may be more transparent for this specific cell compared to the rest.

Figure 5.7(c) shows the *FF* values as a function of annealing temperature for two different TMB flows. It is observed that the cells produced with TMB flow of 1.9 sccm show higher *FF* for all annealing conditions compared with the 1.5 sccm. The observed trend is consistent with the trend in specific contact resistivities extracted from TLM measurements (c.f. Chapter 4, Section 4.3.4). With increasing doping concentration in $SiC_x(p)$, more efficient carrier extraction is obtained due to the improved contact properties between TCO and $SiC_x(p)$. For both TMB flows investigated here, the *FF* increases with annealing temperature, also in agreement with the observed trend for ρ_c values in Chapter 4. This might be due to the improved crystallinity of the $SiC_x(p)$ and enhanced boron in-diffusion that reinforces the band bending in the c-Si so as the carrier extraction. The best *FF* reached in this set is 80.9 % with the cell produced by using a TMB flow of 1.9 sccm and annealing at 850 °C for 5 min. Nevertheless, it is important to point out that the V_{oc} of this cell is fairly low, in the range of 675 to 680 mV.

Overall, the cells produced with 1.5 and 1.9 sccm show similar efficiency, especially for the annealing temperatures of 800 and 850 °C since the lower V_{oc} and J_{sc} values for the cells prepared with 1.9 sccm TMB flow are compensated by their higher *FF* values. The best hybrid cell from this series reaches a conversion efficiency of 21.9 %. While the J_{sc} of 38.7 mA/cm^2 is still limited by parasitic absorption of the front side scheme, the V_{oc} of 707 mV and FF of 79.9

% highlight the excellent passivation as well as the efficient majority-carrier transport of this hole-selective passivating contact.

5.4.3 Doped layer thickness

In this section we address the impact of the rear hole-selective passivating contact thickness on *p*-type hybrid cell performance. To that end, the rear contacts of the cells were prepared with chemical SiO_x, 10-nm-thick Si(i) inter–layer and $SiC_x(p)$ layer with various thicknesses. Based on the results from the previous section, a TMB flow of 1.5 sccm, an annealing temperature of 825 °C, and a dwell time of 5 min were chosen, as they correspond to optimized conditions. The cells were manufactured using the simplified process flow described in section 5.3. The obtained cell parameters are depicted in Figure 5.8 as a function of total Si(i) and $SiC_x(p)$ layer — Si(i) layer thickness is kept constant as 10 nm for all samples. The grey symbols represent the cells produced in the same run while the red symbols show the best cell parameters obtained in a previous run using the total rear contact thickness of 30 nm (10 nm of Si(i) and 20 nm of $SiC_x(p)$). Open symbols in Figure 5.8(a) and (c) indicate the implied values derived from injection-dependent minority-carrier lifetime curves for the cell precursors before metallization.

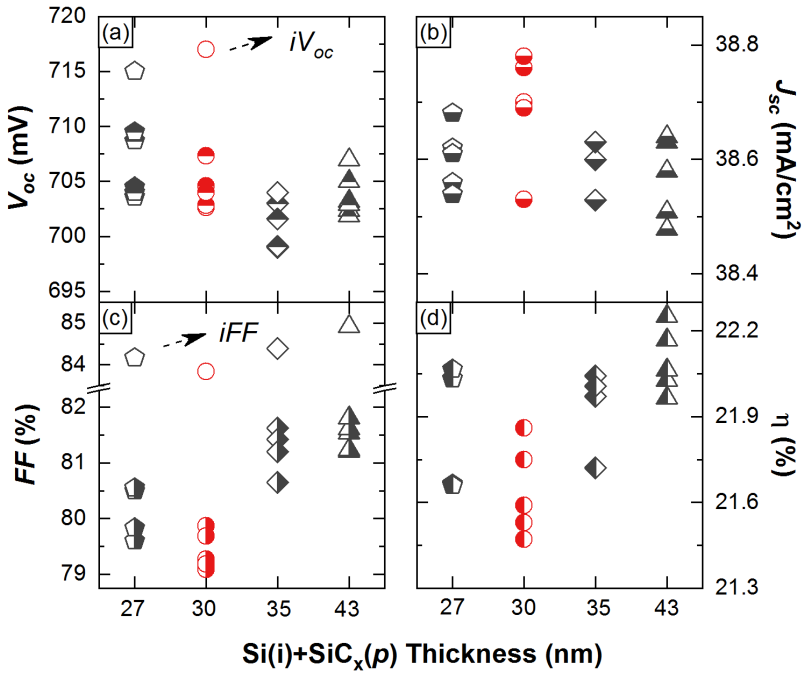

Figure 5.8 – Output characteristics of the hybrid solar cells exhibiting the rear contact composed of chemical SiO_x, 10-nm-thick Si(i) inter–layer and $SiC_x(p)$ layer with various thicknesses prepared with TMB flow of 1.5 sccm and annealed at dwell temperature of 825 °C for 5 min. Open symbols represent the implied V_{oc} and implied *FF* measured before metallization.

Figure 5.8(a) shows a decreasing trend of V_{oc} with increasing total rear contact thickness. Surprisingly, this is contradictory to the reported trend for standard SHJ solar cells in where the V_{oc} increases until a critical *p*-layer thickness and remains constant thereafter [Fujiwara 2007b], [Tanaka 1992]. We also reported stable V_{oc} trend with increasing hole-selective contact thicknesses for both amorphous and microcrystalline contact layers in Chapter 3. Based on this observation, it is safe to assume that the working principle of our high temperature contact differs from standard SHJ. The observed trend for high temperature contacts can be ascribed to the enhanced dopant reservoir with increased $SiC_x(p)$ thickness which leads to stronger boron in-diffusion and augmented interface defect density, resulting in suboptimal chemical passivation. Overall, the hybrid cell featuring total rear contact thickness of 27 nm, yields the best V_{oc} value of 709.5 mV. Strikingly, the difference in between iV_{oc} before metallization and the measured V_{oc} of the cell mitigates profoundly with increased total contact thickness. Based on symmetric test structures, we concluded in section 5.4.1 that the sputtering damage may contribute to the observed difference in between iV_{oc} and V_{oc}, even though it might not be the only reason. From the behaviour seen in Figure 5.8(a) we can plausibly conclude that sputtering damage is reduced with increased thickness of the $SiC_x(p)$ layer.

Regarding the J_{sc} values, a stable trend with total rear-contact thickness is observed in Figure 5.8(b). Knowing that all the cells presented here employ the same front SHJ electron contact and ITO, this trend is expected. Only the cells with 30-nm-thick rear contact that stick out, was processed in different run and possible process discrepancy may explain this small variation.

In terms of *FF*, there is an explicit trend with total rear hole contact thickness in Figure 5.8(c), once again with the exception of the cells featuring 30-nm-thick rear contact processed in different run. A similar trend was also reported for standard SHJ solar cells not only via numerical simulations but also experimentally (see Chapter 3). The incentive of *p*-type layers to collect holes is strongly dependent on the work function at the interface between the TCO and the boron-doped layer. As a consequence, it is necessary to use either TCOs with high work function, or contact layers above certain thickness in order to attain enough built-in potential and to extract the carriers efficiently in standard SHJ cells. It is unlikely that this interpretation applies to the present case since the crystallized layers have much higher doping efficiency than the amorphous layers discussed in Chapter 3. We attribute the observation rather to an enhanced dopant reservoir in thicker $SiC_x(p)$ layers that leads to stronger boron in-diffusion and thus reinforces the band bending in the c-Si. For the cells with 27- and 30-nm-thick rear contacts, the lifetime curves reveal a slight tailing at low injection levels which is translated to lower *iFF* values (84.1 and 83.8 %, respectively) compared to cells with 35- and 43-nm-thick rear contacts (84.4 and 84.9 %, respectively). On the finished devices, the cell with 43 nm total rear contact yields a measured *FF* value of 81.8 % which is the highest *FF* we obtained with our hybrid cell concept.

On the whole, the cells with total rear contact thickness of 27 and 35 nm yield similar efficiencies since the lower V_{oc} of the cell with 35 nm rear contact is compensated with the gain in *FF*. Notably, the conversion efficiency trend is dictated by the *FF*. It is observed that increasing the

thickness of the $SiC_x(p)$ layer is beneficial to improve the device performance. The excellent efficiency potential of our rear passivating contact is highlighted by conversion efficiencies up to of 22.3 %, based on V_{oc} of 707 mV, *FF* of 81.8 % and J_{sc} of 38.6 mA/cm^2 using simplified hybrid cell process.

5.4.4 The impact of carbon concentration on temperature dependency

The influence of the carbon concentration in the $SiC_x(p)$ layer was investigated at the cell level by realizing the hybrid cells featuring the same heterojunction electron-selective front contact and rear contact composed of chemical SiO_x, 10-nm-thick Si(i) inter–layer and $SiC_x(p)$ with various carbon concentrations. In order to change the carbon concentration in the $SiC_x(p)$ layer, the CH_4 to SiH_4 ratio was altered from 0.2 to 1.1. Figure 5.9 presents the extracted cell parameters from one-sun *J-V* measurements as well as the pseudo V_{oc}, *FF* and conversion efficiency values measured with suns-V_{oc} — indicated with red starts. With increasing carbon concentration, the V_{oc} exhibits increasing trend probably due related band gap widening and increased band offsets. This effect also manifests itself in Figure 5.9(c) with the *FF* trend as a function of carbon concentration. The higher pseudo-*FF* but lower final *FF* measured from the hybrid cell featuring rear contact realized with high carbon concentration points out the increased series resistance.

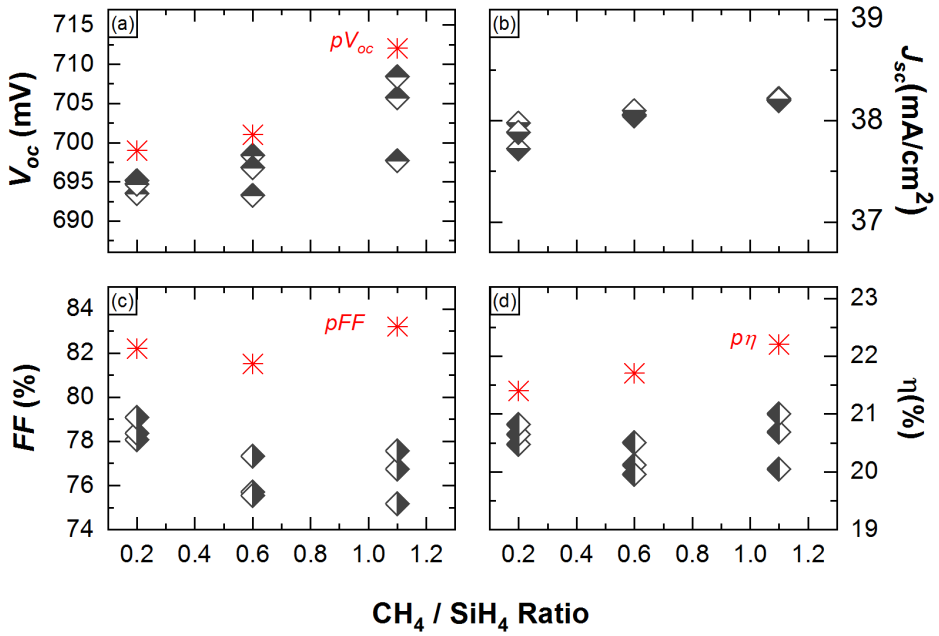

Figure 5.9 – Extracted hybrid cell parameters from one-sun *J-V* measurements as a function of CH_4 to SiH_4 ratio. Pseudo values extracted from the suns-V_{oc} measurements, are indicated with red stars.

In order to gain a better understanding of the underlying charge-carrier transport mechanism in hybrid cells, temperature-dependent *J-V* measurements were performed in the range from −80 to +80 °C with 5 °C intervals. As noted in Chapter 3, the low temperature behaviour of the V_{oc} and *FF* may provide an insight to the transport barrier effect that photogenerated carriers might be confronted with during the collection. Under the assumption of a one-diode model, temperature dependence of V_{oc} can be determined in terms of J_0 and J_{sc} as following [Jensen 2000], [Dupre 2016]:

$$V_{oc}(T) \approx \frac{nk_BT}{q} \ln\left(\frac{J_{sc}}{J_0}\right) \tag{5.1}$$

where J_{sc} and J_0 are short-circuit current density and dark saturation current density respectively. T is temperature, n is the diode ideality factor, q is the elementary charge, k_B is the Boltzmann constant. Since J_0 is proportional to the intrinsic carrier concentration (n_i) which in turn decreases exponentially with decreasing T, the V_{oc} increases linearly with decreasing T. Defining the *FF* as a function of T is fairly complicated as it depends on variables such as discontinuities at band structure such as band offsets, defect states in the materials and at the interfaces, distribution of the charge-carrier density in the cell. Without taking into account details of these effects, the *FF* can still be related to the V_{oc} and T via the shape of the exponential relationship by the following empirical equation [Green 1981], [Green 1982b], [Dupre 2015]:

$$FF(T) \approx \frac{V_{oc} - (k_BT/q)\ln(qV_{oc}/k_BT + 0.72)}{V_{oc} + k_BT/q} \tag{5.2}$$

The cells employing the hole-selective passivating rear contacts compose of a 10-nm-thick Si(i) inter–layer and $SiC_x(p)$ with three different C concentrations were prepared by altering the CH_4 / SiH_4 flow ratio. Extracted cell parameters as a function of temperature for the hybrid cells are shown in Figure 5.10. The V_{oc} of the three different solar cells behaves similarly and increases linearly towards lower temperature following the trend predicted by Equation 5.1. The hybrid cell featuring the rear contact produced with CH_4 / SiH_4 ratio of 0.2 demonstrates the lowest V_{oc}. In the meantime, at room temperature V_{oc} manifests increasing trend with C concentration as revealed in Figure 5.10(a). This can be the outcome of the fact that increasing C concentration accompanying by the widening of the bandgap which results in higher valence band offset [Brown 1997], [Hayashi 1988]. In addition to that the doping efficiency of the $SiC_x(p)$ layer is expected to be lower for the sample with higher C concentration which can also explain the higher V_{oc} value as the corresponding Auger recombination may be projected to be lower. Figure 5.10(c) shows that the J_{sc} increases linearly with temperature mainly due to temperature-induced bandgap narrowing, which results in enhanced phonon-assisted excitation and correspondingly increased band-to-band absorption coefficient across the spectrum [Green 2003]. Our interpretation of increased valence band offset with C concentration may also explain well the *FF* behaviour of the hybrid cells at room temperature which

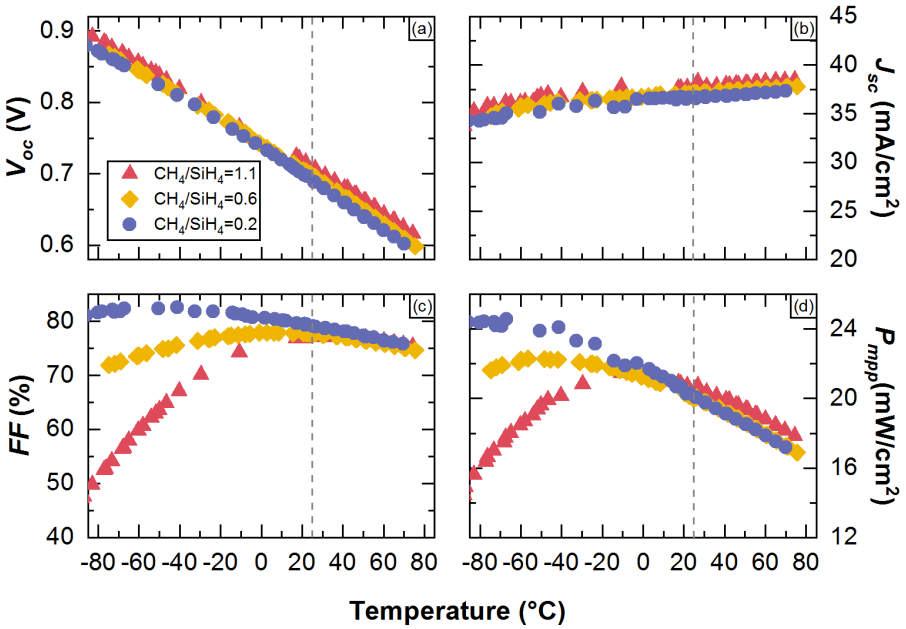

Figure 5.10 – Extracted cell parameters as a function of temperature for the hybrid cells featuring the hole-selective passivating rear contact with three different C concentrations in $SiC_x(p)$. Dash line indicates the room temperature.

discloses improved *FF* with decreased C concentration [see Figure 5.10(c)]. Strikingly, the three hybrid cells show very different *FF* trends in the low temperature range. As the only differentiation in between the cells is the C concentration of the rear contacts, we relate the different temperature behaviour of the *FF* with that. Upon an increase in C concentration, *FF* exhibits more pronounced drop toward lower operation temperatures. The drop in *FF* with increasing C concentration indicates a requirement for a high thermionic energy component that supports the charge-carrier transport. Concordantly, the doping efficiency is decreasing so as the dopant concentration in diffused region leading to suboptimal band bending that is accompanied by less efficient tunneling transport and more thermionic energy demand.

Previously in chapter 3, it was shown that the low temperature behaviour of the standard SHJ solar cells exhibits a saturation of V_{oc} which can be retarded by replacing the hole-selective a-Si:H(p) contact with μc-Si:H(p). The observed behaviour was indicating that the Schottky barrier effect is more pronounced for the boron-doped hole-selective contact. Here, in the investigated temperature range the V_{oc} does not show any saturation. We interpret this finding with a higher doping efficiency in the crystallized layers which narrows the Schottky barrier between the *p*-type layer and the ITO even more. Similar to SHJ cells, also the hybrid cells show a decrease of *FF* at low temperatures. This drop becomes more pronounced with the increased carbon concentration of the rear $SiC_x(p)$ contact, probably due to the increased band offsets at the hetero-interfaces that affect strongly the charge-carrier transport.

5.4.5 Si(i) inter–layer thickness and carbon concentration

Previously, the improved surface passivation by introducing a 10-nm-thick Si(i) inter–layer between chemical SiO_x and $SiC_x(p)$ was discussed by means of symmetric test samples. A possible interpretation for the function of the Si(i) inter–layer was given as preventing the chemical reaction between carbon atoms in the $SiC_x(p)$ layer and the adjacent chemical SiO_x. The aim of this section is to validate this interpretation at the device level by employing the hybrid concept.

With the goal of relating the effect of carbon concentration and the necessary Si(i) inter–layer thickness, two sets of hybrid solar cells were prepared. For the first set, the flow ratio of the methane to silane (CH_4 / SiH_4) was fixed to 1.1 (hereafter referred as high C concentration as it is higher than the one used for the previous sections) and Si(i) inter–layer thickness was changed from 3 to 12 nm. For the second set the CH_4 / SiH_4 flow ratio was fixed to 0.2 (hereafter referred as low C concentration as it is lower than the one used for the previous sections) and Si(i) inter–layer thickness was changed from 0 to 10 nm. The total hole-selective contact thickness was kept constant in both sets. It is important to note that PECVD deposition recipe used here comprises of two phases: (i) the first phase of deposition includes only SiH_4 and H_2 flows; after the plasma ignition the duration of this step defines the Si(i) inter–layer thickness, (ii) in the second phase, the TMB and CH_4 flows are switched on respectively with less than an 1 sec delay in between while the plasma is still on; the duration of this phase defines the $SiC_x(p)$ thickness. This means that even if the time is set to 0 min for the first phase, the chemical SiO_x might still be exposed to short SiH_4/H_2 plasma that may lead to an extremely thin Si(i) inter–layer growth without any carbon and boron.

The obtained cell parameters are shown in Figure 5.11. For the samples prepared with the high C concentration — CH_4 / SiH_4 = 1.1 —, the surface passivation quality improves with increased Si(i) inter–layer thickness achieving its optimum V_{oc} value of 712 mV with 10-nm-thick Si(i) inter–layer [see Figure 5.11(a)]. Upon further increase in thickness to 12 nm, the V_{oc} drops below 700 mV, probably due to suboptimal boron in-diffusion and correspondingly a low band bending in c-Si. This trend is also in-line with the iV_{oc} trend obtained with symmetric test structures presented in Chapter 4. For the low carbon concentration — CH_4 / SiH_4 = 0.2 —, the optimum Si(i) inter–layer thickness is found to be 3 nm, yielding a V_{oc} value of 710 mV. Based on these findings, we tentatively conclude that in the case of high C concentration in $SiC_x(p)$ layer, the necessary Si(i) inter–layer is higher to prevent the diffusion of carbon towards the SiO_x/c-Si interface where it weakens the chemical passivation of SiO_x. Thus, our tentative interpretation about the function of the Si(i) inter–layer is corroborated here at the cell level. Introducing a Si(i) inter–layer between the chemical SiO_x and the $SiC_x(p)$ is beneficial to boost the V_{oc} of the hybrid cells. Yet the necessary thickness to obtain the best V_{oc}, depends on the carbon concentration of the $SiC_x(p)$ layer.

According to Figure 5.11(b), J_{sc} does not disclose any clear trend with neither C concentration nor the Si(i) inter–layer thickness of the rear hole-selective passivating contact. On the other

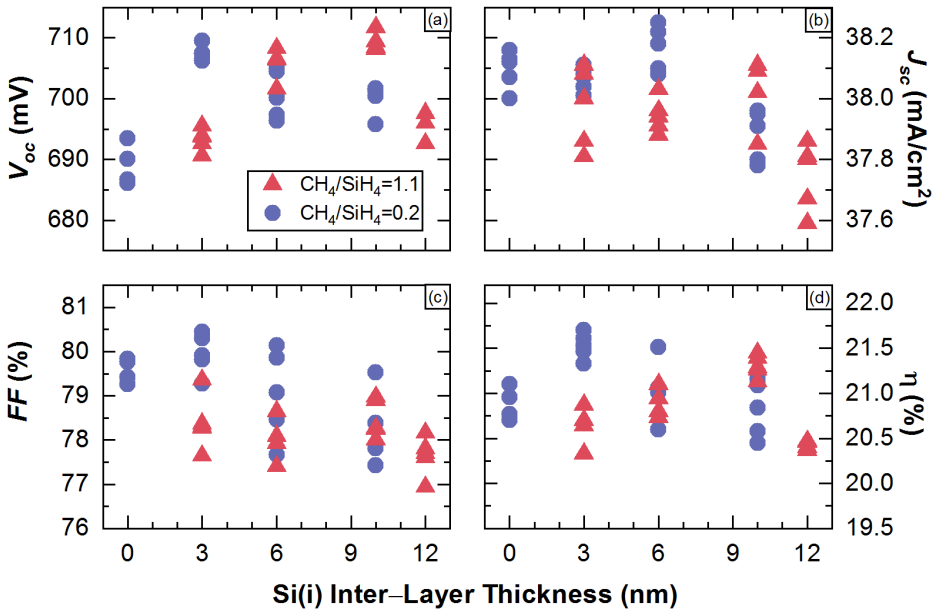

Figure 5.11 – Output characteristics of the hybrid solar cells exhibiting the rear contact composed of chemical SiO_x, Si(i) inter–layer with various thicknesses and $SiC_x(p)$ layer with two different carbon concentration. $SiC_x(p)$ prepared with TMB flow of 1.5 sccm and annealed at dwell temperature of 800 °C for 5 min.

hand, hybrid cells featuring rear contacts with low C concentration manifest higher *FF* values, probably due to the fact that the crystallinity of the rear contact layer with high C concentration is lower, as C inhibits the crystallization. Similar to our findings in Chapter 4, we can conclude from Figure 5.11 that higher the crystallinity of the doped layer yields lower contact resistivity between the doped layer and the TCO. The best *FF* achieved in this experiment is 80.5 % with the rear contact produced with low C concentration and Si(i) inter–layer thickness of 3 nm. Overall with both C concentrations decent conversion efficiencies above 21.5 % are reached; however, their optimum Si(i) inter–layer thicknesses are found to be different.

5.5 Conclusions

We present a process flow to realize proof-of-concept hybrid solar cells featuring a high-thermal-budget rear hole contact based on chemical SiO_x/Si(i)/$SiC_x(p)$ and a low-thermal-budget front electron contact based on a-Si:H(*i*/*n*). Correspondingly, the effect of TCO deposition on surface passivation of the rear contact is investigated with symmetric test samples. It is found that irrespective of the deposition technique, applying a TCO overlayer provokes a strong drop in lifetimes. It is observed that curing at low temperatures is necessary to recovery this drop. Among the tested TCOs, ITO is found to be the most promising option as it benefits

effectively from the curing step while providing good electrical properties.

At the cell level, it is shown that the hybrid solar cell concept is beneficial to demonstrate the potential of the our high-thermal-budget hole contact. By realizing systematic variations at the rear hole contact, clear trends in cell parameters are observed which are then used to interpret its working principle. It is found that rear contact structures with a low doping concentration exhibit higher V_{oc} but lower *FF* values in the annealing temperature range of 800 to 850 °C. Increased $SiC_x(p)$ layer thickness is necessary to improve the *FF* values, probably due to the increased majority-carrier concentration in the c-Si wafer underneath the chemical SiO_x, resulting in stronger band bending in the c-Si. The best cell obtained with the hybrid concept has a conversion efficiency of 22.3 % with a V_{oc} of 707 mV, *FF* of 81.8 % and J_{sc} of 38.6 mA/cm^2.

Furthermore, the temperature dependency of the hybrid cells suggests that our hole-selective contact with a high-thermal-budget does not suffer from the Schottky barrier effect between the TCO and the boron-doped layer. However, the carrier transport suffers from the band discontinuities, especially at low temperatures when the carbon concentration is increased excessively. Finally, our finding from Chapter 4 that a carbon-free Si(i) inter–layer is needed to protect the passivating SiO_x layer is confirmed at the cell level by demonstrating that the optimum thickness of the inter–layer depends on the carbon concentration in the overlaying $SiC_x(p)$.

6 Fluorinated boron-doped hole-selective contacts

Summary

The transport of boron through the oxide supposably introduces defects at the oxide/c-Si interface and thus increases the recombination current. In this chapter, it is shown that this shortfall can be compensated by incorporating fluorine into the boron-doped hole-selective passivating contact layer during PECVD process. According to SIMS and EDX measurements, in the *as-deposited* state, fluorine is evenly distributed throughout the layer. Upon annealing at around 800–850 °C, it accumulates at the defective interfaces and enhances surface passivation, which is evidenced by iV_{oc} values above 720 mV without any hydrogenation. Such high iV_{oc} values suggest a reduced density of defect states[1] at the oxide/c-Si wafer interface. After subsequent hydrogenation an iV_{oc} value of 735 mV (with a corresponding J_0 of 4.9 fA/cm^2) is reached. To the best of our knowledge this is the highest reported value obtained with an *in-situ* boron-doped hole-selective contact on a *p*-type wafer[2].

6.1 Introduction and motivation

The suboptimal performance of the boron-doped hole-selective contact is commonly explained by the high surface recombination velocity that occurs at boron-diffused surfaces passivated with SiO_x, and by additional defect creation due to the transport of boron during diffusion. In the previous chapters using standard trimethylboron (TMB) as a dopant precursor, we have demonstrated promising iV_{oc} values of up to 718 mV with a corresponding J_0 of

[1] In this chapter we refer frequently to results of the bipolar transistor community where transport phenomena are often related to the density of interfacial trap states (D_{it}). The terms "trap" and "defect" may be used interchangeably.

[2] The results presented in this chapter will be the part of an upcoming publication by Nogay *et al.*

11.5 fA/cm^2. However the performance of the hole-selective contact is still far lower than that of electron-selective contacts fabricated with the same approach (iV_{oc} > 740 mV; J_0 < 3 fA/cm^2 [Richter 2017]). Hence there is still significant potential to improve the performance of the hole-selective passivating contacts.

The approach employed here to improve contact quality is inspired by the Si-based bipolar transistor technology, which uses poly-Si layers to contact the emitter. The poly-Si/c-Si interface requires a chemical interface treatment and a thermal annealing. The emitters of *p-n-p* poly-Si–emitter bipolar transistors (also called p^+ poly-Si gate devices) are commonly manufactured by implanting BF_2 into an undoped poly-Si layer prepared by low-pressure chemical vapour deposition (LPCVD) at around 600 °C. Subsequently, boron is diffused into the underlying c-Si through the thin interfacial SiO_x upon annealing at temperatures > 900 °C. This process results in an elevated concentration of fluorine in the poly-Si, which was shown to have a significant effect on the structure of the poly-Si during the subsequent emitter drive-in. The threshold voltage stability was found to be strongly affected by the fluorine concentration. Therefore, in the 1980s, the MOSFET community investigated the effect of fluorine in great detail. Since the structure is very similar to our contact, we briefly summarize the reported effects of fluorine here:

- In the *as-deposited* state, the dangling bonds at the SiO_x/c-Si interface give rise to trapping states which act as recombination centres for minority carriers as illustrated in Figure 6.1(a). Upon thermal treatment, fluorine diffuses through the SiO_x and reduces the interface trap density (D_{it}) by passivating the dangling bonds associated with paramagnetic trivalent Si atoms and SiO_x complexes at the SiO_x/c-Si interface as illustrated in Figure 6.1(b) [Wright 1989], [Virdi 1991], [Ono 1993]. Therefore, it can reduce the surface recombination velocity as well [Castaner 1998]. This function of fluorine was reported to be linked to its high electronegativity [Joannopoulos 1984].
- Fluorine stimulates the in-diffusion of boron by enhancing its penetration through the

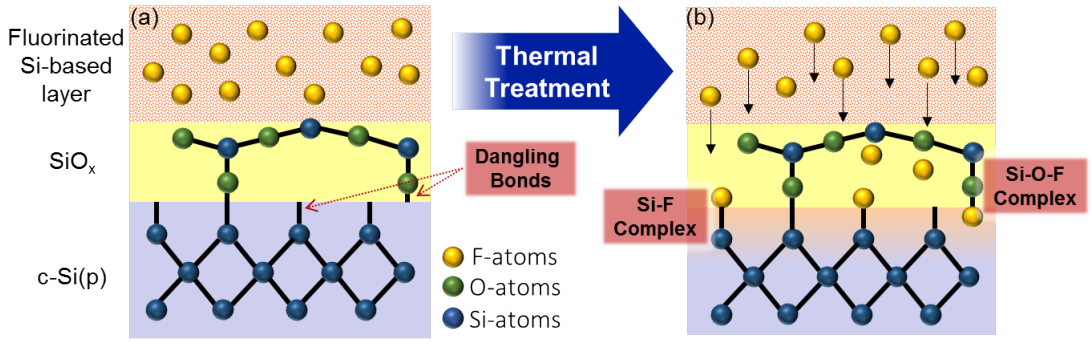

Figure 6.1 – Schematic illustration of the passivation of dangling bonds by fluorine as a result of the formation of Si–F and Si–O–F complexes. Sample structure (a) before and (b) after thermal treatment. Adapted from [Moiseiwitsch 1994].

SiO_x into the underlying c-Si [Sung 1989], [Tseng 1992a]. The buried junction depth of the BF_2 implanted device was reported to be larger than that of devices implanted only with B. This was explained by the fact that fluorine can bind to the dangling bonds in the SiO_x and reduce the interaction of the boron with unsaturated bonds; consequently, boron becomes much more mobile in the SiO_x [Lu 1989].

- The breakup of the interfacial SiO_x layer can be accelerated by fluorine. This phenomenon is explained by the formation of Si–O–F complexes [see Figure 6.1(b)] which could result in a weakening of the bonding structure of the interfacial SiO_x layer, allowing it to become more prone to breaking up at a lower temperature [Wolstenholme 1987], [Williams 1992], [Moiseiwitsch 1994] [Wu 1994]. This can also have a direct effect on the previous bullet point as deeper boron diffusion is expected where the oxide breakup occurs.

Historically, fluorinated precursor gases were first proposed as an alternative to manufacture amorphous silicon (a-Si:H) with improved material quality as evidenced by a lower density of states at the Fermi level which leads to better doping efficiencies [Ovshinsky 1979], [Madan 1980]. Following that, they were adopted for microcrystalline layer depositions for Si-based thin-film solar cell applications [Shibata 1987]. It was reported that incorporation of fluorine enhances the crystallinity of the thin films in the corresponding deposition regime as the amorphous phase is preferentially etched by fluorine ions [Kasouit 2004]. In 1986, Guha *et al.* proposed to use BF_3 to produce fluorinated microcrystalline *p*-type layers in PECVD which lead to high quality layers with improved dark conductivity and low optical loss [Guha 1986].

In light of these inspiring results, we explore the impact of fluorine incorporation into boron-doped silicon-based passivating contacts for c-Si solar cell applications. In this respect, the dopant precursor TMB is replaced by the fluorinated boron dopant source BF_3 during the PECVD process. The fluorinated layers are deposited in the amorphous phase to minimize the process complexity and to maximize fluorine incorporation. The microstructural properties of the hole-selective contact are studied extensively before and after thermal treatment with a particular interest on the evolution of the fluorine distribution. The change in the chemical composition of the thin SiO_x upon annealing is explored simultaneously. Last but not least, the impact of different process parameters, such as the carbon and doping concentration of the contact layer as well as the annealing temperature on surface passivation, is investigated using symmetric test structures before and after subsequent hydrogenation.

6.2 Experimental details

Passivating contacts were investigated using 200-μm-thick chemically polished 4-inch *p*-type float-zone <100> c-Si wafers with a resistivity of 2 Ω cm. After wet-chemical cleaning, a thin SiO_x layer (~ 1.2 nm) was formed in HNO_3 as explained in previous chapters. Subsequently, *in-situ* doped layers were deposited on both sides by paralle-plate PECVD at 40 MHz using SiH_4,

CH_4 and BF_3 as precursor gases. The samples were then annealed in an inert gas atmosphere at temperatures between 800 and 925 °C. This was followed by a hydrogenation process.

The structural changes of the contact upon annealing were analyzed by scanning transmission electron microscopy (STEM). To that end, thin lamellae were extracted using the conventional focused ion beam (FIB) lift-out method in a Zeiss NVision40 workstation. The lamellae was further thinned by gallium ion milling using a voltage of 2 kV. STEM images were recorded using a high-angle annular dark-field (HAADF) detector and were combined with energy-dispersive X-ray spectroscopy (EDX) to obtain a chemical assessment of the layers of interest (at 200 kV, beam current between 80 and 200 pA, using a double Cs-corrected FEI TITAN Themis microscope). In addition, electron energy-loss spectroscopy (EELS) was performed at 80 kV with a beam current of 100 pA (convergence and collection semi-angles of 28 and 60 mrad, respectively). Boron and fluorine distribution profiles were obtained with secondary ion mass spectroscopy (SIMS) using a CAMECA SC-Ultra instrument with O_2^+ — for boron — Cs^+ — for fluorine — primary ions with 1 keV impact energy. A primary ion beam with low energy was used to rapidly reach equilibrium sputtering as well as the necessary ionization conditions to avoid primary beam collisional mixing that would drive the dopant deeper into the layer. All the depth profiles were acquired with the same instrumental settings and analytical conditions such that the profiles can be compared directly. After finishing the acquisition, the depths of the SIMS sputtering craters were measured with a KLA-Tencor P17 profilometer. The sputtering time was converted to depth in nanometers assuming a linear erosion rate through the different layers. The electrochemical capacitance-voltage (ECV) technique was employed to measure the diffusion profiles of electrically active boron atoms within the c-Si wafer using 0.1 M ammonium fluoride (NH_4F) solution as an etchant. The surface passivation quality was determined by minority-carrier lifetime measurements with Sinton lifetime tester WCT-120-TS in transient mode. The specific contact resistivity values were extracted by means of TLM.

6.3 Results and discussion

6.3.1 Lifetime evolution upon annealing and impact of hydrogenation

The importance of atomic hydrogenation for the contact structure produced with TMB precursor was shown in Chapter 4. With an attempt to have direct comparison between TMB and BF_3 based contacts, the evolution of the effective lifetime curves after annealing for contact formation, after hydrogenation with forming gas annealing (FGA) and after hydrogenation with SiN_x overlayer are depicted in Figure 6.2. For the latter case, the SiN_x was etched off with diluted HF before the measurements. For the TMB based contact, the lifetime value is fairly low after the contact formation annealing which leads to dopant in-diffusion and PECVD layer crystallization. While at the same stage with the BF_3 based contact, effective lifetime value above 2.5 ms at 1×10^{15} cm^{-3} and iV_{oc} value above 720 mV is reached [see Figure 6.2(b)]. In both cases, rather slight lifetime improvement is monitored after the hydrogenation with FGA.

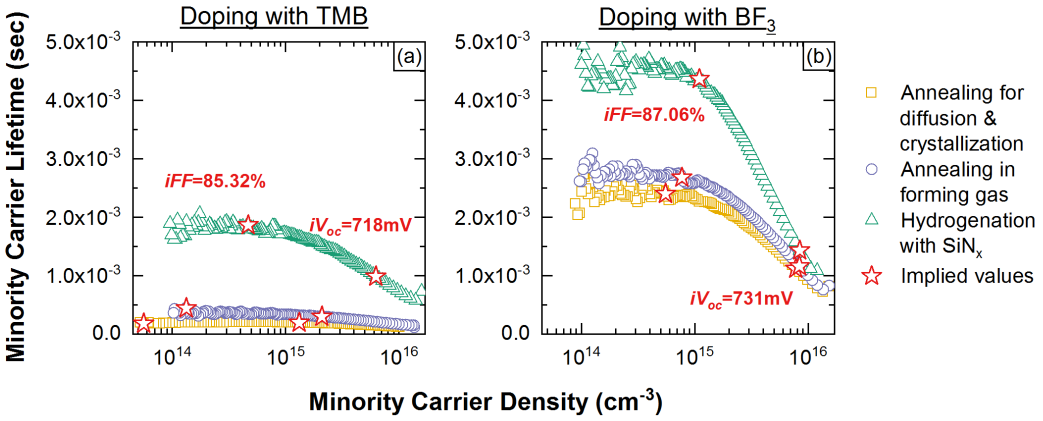

Figure 6.2 – Evolution of the minority-carrier lifetime curves as a function of excess-carrier density with (a) TMB and (b) BF_3 dopant precursors. Lifetimes at open-circuit and maximum power point conditions are indicated with stars for each step. Implied V_{oc} and implied *FF* values are given after hydrogenation with SiN_x overlayer — measurements performed after stripping off the SiN_x overlayer.

Conversely, atomic hydrogenation with SiN_x overlayer improves the low- and high-injection parts of the lifetime curves for both contact structures. With BF_3 doping, impressive iV_{oc} value of 731 mV and *iFF* value of 87.06 % are attained.

Based on the obtained results, it is explicit that the presence of fluorine in the contact structure is beneficial for surface passivation. We can tentatively conclude that fluorine has an effective function of reducing the interface trap density by terminating dangling bonds. This is also in accordance with the results of Virdi *et al.* who reported a decrease in the D_{it} at the SiO_2/c-Si wafer interface by an order of magnitude when fluorine ions were implanted at a dose of 1 $\times$ 10^{16} cm^{-2} [Virdi 1991]. Wright *et al.* also measured similar D_{it} decline employing fluorine [Wright 1989]. Additionally, Nishioka *et al.* reported a reduced D_{it} trend with increasing dose of implanted fluorine [Nishioka 1989].

At this point it is important to mention that the contact structure produced with BF_3 precursor, hereafter referred as SiC_x:F(*p*), does not comprise any intrinsic silicon inter–layer as the surface passivation is already in a good level. One possible reason for the high performance of the contact without any inter–layer could be the fact that real CH_4 flow is much lower compared to the one used for TMB–based contact. Another explanation may be that fluorine can compensate simultaneously the negative effect of carbon on the chemical SiO_x which was interpreted by a possible chemical reaction leading to deteriorated surface passivation as presented in the Chapters 4 and 5. Since the impact of FGA is found to be negligible, from now on only the SiN_x overlayer is employed for hydrogenation process.

6.3.2 Structural evolution upon annealing

A comprehensive study about the structural evolution of the contact upon annealing is performed with Raman and TEM characterizations.

Raman spectroscopy

The measured Raman spectra for the *as-deposited* and annealed samples produced with BF_3 flow of 0.7 sccm are depicted in Figure 6.3.

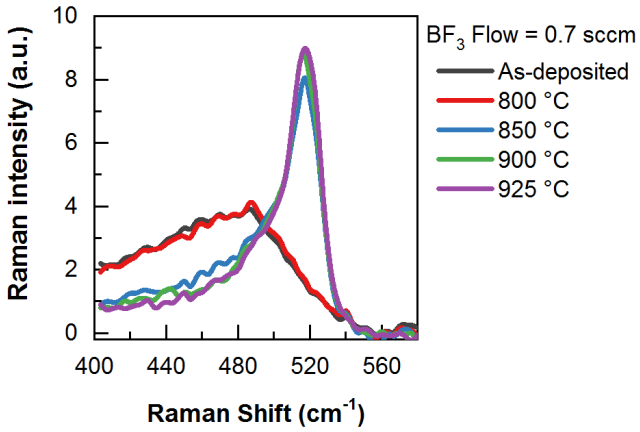

Figure 6.3 – Raman spectra for the *as-deposited* and annealed samples in the temperature range of 800 to 925 °C. Samples were produced with BF_3 flow of 0.7 sccm. 325 nm UV laser was used as an excitation source for measurements.

In the *as-deposited* state, the contact structure exhibits a broad peak at 480 cm^{-1} which is attributed to amorphous silicon. After annealing at the 800 °C, SiC_x:F(p) preserves its amorphous nature as evidenced with the broad peak at 480 cm^{-1}. At this point it is important to note that the measurements are performed with a 325 nm UV-laser whose collection depth is ~10 nm. Thus, the Raman spectra provides microstructural information only for the region close to the surface, yet no information as regards the interface region can be obtained. With further increase in the annealing temperature to 850 °C and above, the contact structure shows a pronounced sharp peak at 520 cm^{-1} which is attributed to the crystalline silicon phase while the asymmetric characteristic of the peak towards lower wavenumbers suggests the presence of an amorphous matrix.

Concerning the general trend in measured Raman spectra, the hole-selective SiC_x:F(p) contact differs slightly from the TMB–based Si(i)/SiC_x(p) contact. The onset of the crystallization for the TMB–based Si(i)/SiC_x(p) contact is already visible after annealing at 800 °C (see Figure 4.17 in Chapter 4) whereas in the case of SiC_x:F(p) contact only an amorphous contribution is prominent. After annealing at higher temperatures, the crystallinity of the TMB–based

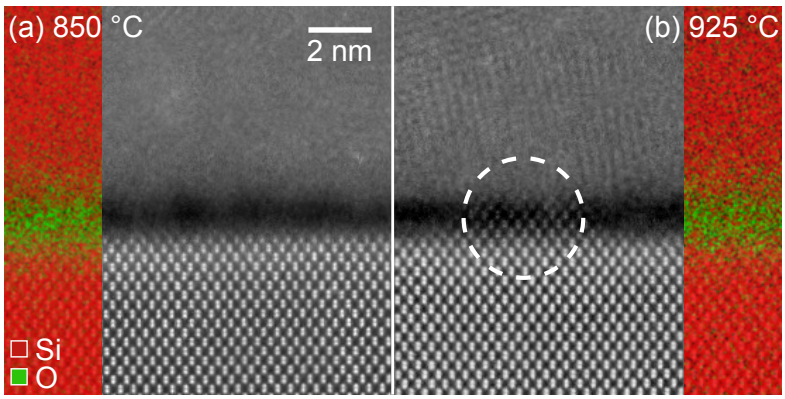

Figure 6.4 – STEM-HAADF micrographs of the samples produced with a BF_3 flow of 0.7 sccm, annealed at (a) 850 and (b) 925 °C and corresponding EDX maps for silicon (Si, in red) and oxygen (O, in green). A pinhole, i.e. a protrusion of c-Si, is circled in (b).

Si(i)/SiC_x(*p*) contact gradually increases with annealing temperature whereas for the BF_3–based SiC_x:F(*p*) contact, the crystallinity appears to change at threshold temperature and remains fairly similar afterwards.

Transmission electron microscopy

The structural changes after annealing were also investigated by STEM, with a particular interest on the interfaces. STEM-HAADF micrographs as well as the EDX mappings for the SiC_x:F(*p*) contact structure produced with a BF_3 flow of 0.7 sccm and annealed at two difference temperatures are shown in Figure 6.4. According to the EDX maps, the thin (~1 nm) continuous dark region distinguishable at the c-Si wafer interface in both images corresponds to the chemical SiO_x. After annealing at 850 °C, the contact structure preserves its integrity, revealing a continuous chemical SiO_x layer. At 925 °C, the SiO_x layer appears to be still present along most of the interface, but it breaks up locally and forms pinholes. Figure 6.4(b) reveals an epitaxial re-crystallization of the contact layer over the area of the pinhole. The apparition of lattice planes within the doped layer shows that the contact layer annealed at 925 °C is more crystalline compared to the one annealed at 850 °C. It is important to note that, even if no pinholes could be observed by TEM after annealing at 850 °C, their presence cannot be fully excluded. However, it is clear that the density of pinholes is significantly higher at 925 °C as many pinholes could be observed within the 5-μm-long TEM lamella. Recently, Wietler *et al.* proposed a method to magnify the nanometer-size pinholes in the interfacial SiO_x by combining the selective etching of their poly-Si layer as well as the underlying c-Si with tetramethylammonium hydroxide (TMAH) and probing the sample either with an optical microscopy or with a scanning electron microscopy [Wietler 2017]. By applying this method, Tetzlaff *et al.* reported the existence of pinholes with an areal density of 2.2×10^8 cm^{-2} for the BF_2 implanted *p*-type sample with chemical SiO_x annealed at 800 °C [Tetzlaff 2017a]. Considering the reported areal pinhole density for structure similar to the ones presented here, the

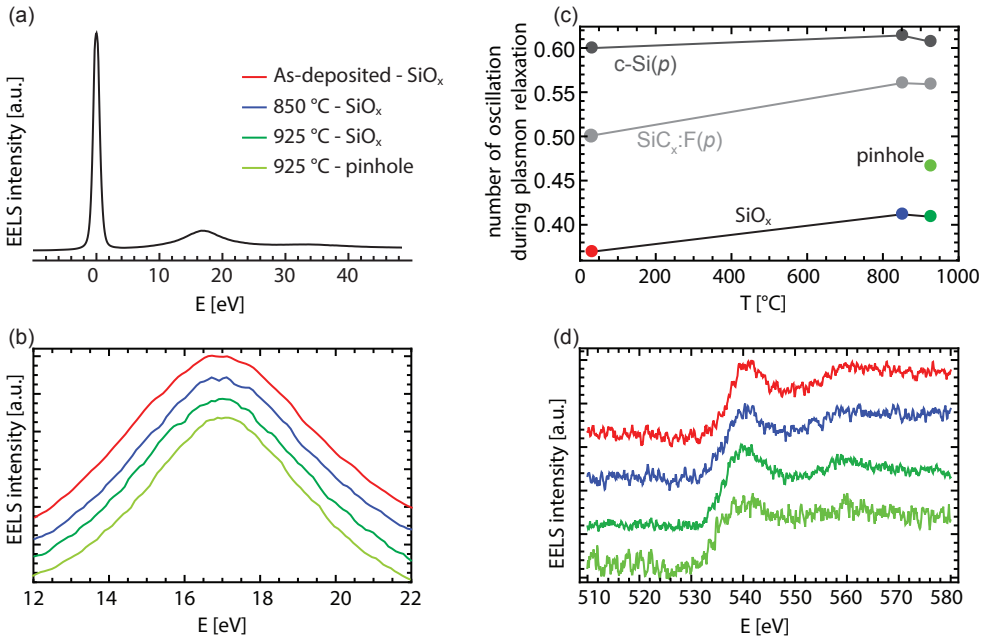

Figure 6.5 – (a) Representative EELS spectrum. (b) Magnified view of the bulk plasmon peaks. (c) Number of oscillation during the plasmon relaxation as a function of annealing temperature derived from the width of the bulk plasmon peaks.(d) Oxygen K-edge spectrum for the *as-deposited* and annealed samples taken at the position of SiO_x as well as the pinhole region where the SiO_x breaks up upon annealing at 925 °C.

probability of finding pinholes within the one-dimensional region of interest investigated by TEM after annealing at 850 °C appears to be rather small.

With an attempt to assess the structural and chemical changes in thin SiO_x due to the different thermal treatments, electron energy-loss spectroscopy (EELS) analysis was performed for *as-deposited* and annealed samples. For the sample annealed at 925 °C, two positions with different chemical SiO_x integrity, i.e. an intact region and a region with pinhole, are examined. EELS measures the loss in kinetic energy of the electron beam after its interaction with the sample[3]. Figure 6.5(a) is a representative EELS spectrum taken from the contact structure including the zero- and low-loss regions. The intense peak appearing at 0 eV is called the zero-loss peak and presents electrons with an energy loss too small to measure. The full width half maximum (FWHM) of zero-loss peak indicates that the energy resolution is 1 eV for this measurement. The peak located in the range 10 to 20 eV is linked to bulk plasmon energy-losses, which originates from inelastic scattering with valence electrons.

Figure 6.5(b) shows a magnified view of the bulk plasmon losses taken at position of the SiO_x layer, both in the *as-deposited* and annealed states at 850 and 925 °C. The measurement is taken at the position of the chemical SiO_x, however, the energy of the plasmon peak measured here is close to that of Si — 16.7 eV for Si, 23 eV for SiO_2 [Couillard 2008] — probably due to

[3] An excellent review about EELS technique can be found in [Egerton 2009]

the delocalization effect (in the 1–2 nm range, [Egerton 2009]) which blurs the contribution of the SiO_x itself at low energy-losses. Thus, even though the STEM probe is placed within the oxide layer, is still provides information about the neighbouring c-Si and SiC_x:F(p) layer. While the position in energy of the plasmon peak cannot be used to assess any changes in density or chemistry of the oxide, its width appears to provide details on the overall crystallinity/quality of the contact stack, especially when combined with data taken at the position of the other layers.

The number of oscillations during the plasmon relaxation time for *as-deposited* and annealed samples are extracted from the plasmon peak width — using methodology as reported in [Duchamp 2013] — and demonstrated in Figure 6.5(c). The relaxation time (τ) represents the time for plasma oscillations to decay in amplitude by a factor of 0.37, while the number of oscillations that occur within this time is $\omega_p \tau / 2\pi$, here ω_p is plasmon frequency. The measured number of oscillations at the position of c-Si remains constant before and after annealing at around 0.6, which is in agreement with the literature value of 0.7 for c-Si [Egerton 1986]. It is important to note that the numbers smaller than 1 suggests strong damping. In the *as-deposited* state, a lower number of oscillations is measured for SiO_x ($\sim$ 0.36) and SiC_x:F(p) ($\sim$ 0.5) due to their amorphous nature together with the presence of hydrogen and other elements (such as carbon and fluorine), which generally act as scattering centers to the oscillating plasmon [Duchamp 2013]. Upon annealing at 850 and 925 °C, the bulk plasmon peaks become narrower and the number of oscillations increases, which is linked to the crystallization of the contact layer and the effusion of elements. Overall, the obtained results are indicating an improved crystal quality. When going from the intact region to the pinhole region on the sample annealed at 925 °C, the width of the plasmon peak also decreases which translates into a clear rise in the number of oscillations for SiO_x contribution as the presence of pinhole promotes the crystallization of the contact structure even further.

Figure 6.5(d) reveals the core-loss region where the losses arise from interaction with core electrons. The shoulder at 540 eV is attributed to the energy-loss region of the oxygen K-edge where the energy-losses are found to be more localized [Muller 1999]. The oxygen K-edge peak position and its shape provide information about the changes in the oxide chemistry and the oxidation states. It is observed that the oxygen K-edge peaks display similar characteristics in the *as-deposited* and annealed states, which indicates that the oxide chemistry is not changing significantly upon annealing in those regions where it remains intact. The small oxygen content found at the position of the pinhole itself comes from superimposing SiO_x regions below or above the pinholes whose diameter is a few nm compared to depth of the TEM lamella which is about 50 nm. Hence, SiO_x either remains chemically unchanged — at least within the sensitivity of EELS — or it breaks up leading to epitaxial regrowth of the Si atoms with the orientation of the underlying c-Si wafer.

In order to characterize the distribution of fluorine, carbon and oxygen in the contact structure, STEM HAADF, EDX maps were recorded in the *as-deposited* and annealed states [see (Figure 6.6(a)–(c)]. Figure 6.6(d) to (f) show the background-subtracted line profiles extracted from

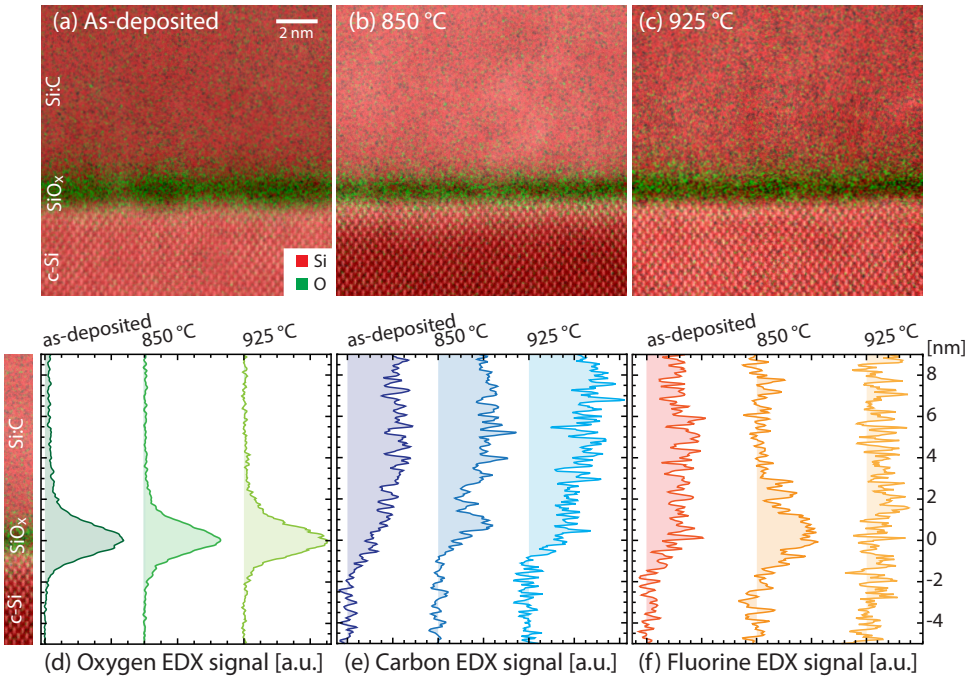

Figure 6.6 – STEM HAADF micrographs together with corresponding EDX maps for (a) *as-deposited* sample as well as the samples annealed at (b) 850 and (c) 925 °C. Related EDX line profiles for (d) oxygen, (e) carbon and (f) fluorine.

the EDX maps. For oxygen, there is an explicit signature of the SiO_x layer in between the SiC_x:F(*p*) contact and c-Si wafer which does not change for the investigated temperatures here. Similarly, the carbon distribution is clearly visible within the deposited layer and does not evolve with annealing as seen in Figure 6.6(e). Regarding fluorine, Figure 6.6(f) reveals a uniform distribution throughout the SiC_x:F(*p*) layer in *as-deposited* state. Interestingly, after annealing the picture is changing drastically. For the sample annealed at 850 °C, fluorine peak positioned at the SiO_x region comes into prominence in the EDX line scan. This can be explained with the incorporation of the fluorine atoms either in the SiO_x or at the interfaces (SiC_x:F(*p*)/SiO_x and SiO_x/c-Si). Similar observation of the fluorine segregation in the SiO_x region was also reported by several research groups for fluorine implanted MOSFET devices. By performing a dedicated experiment, Ono *et al.* revealed that the fluorine segregation is restricted to a narrow interface region, and they conclude that it resides within the SiO_x layer since they could not detect the fluorine peak when the oxide was completely removed by HF solution [Ono 1993]. A possible interpretation can be the fact that after annealing, fluorine accumulates at the interfaces with the SiO_x and reduces the interface trap states by bonding to dangling bonds. This effect can also explain the excellent surface passivation obtained with SiC_x:F(*p*) contacts even without subsequent hydrogenation (see section 6.3.1). With further increase in annealing temperature to 925 °C, Figure 6.6(f) shows that the fluorine concentration decreases significantly, possibly due to out-diffusion.

6.3.3 Doping profiles

Impact of annealing temperature

Aiming to develop better understanding for the function of fluorine and its distribution upon annealing, in addition to EDX analyses, SIMS measurements were performed[4]. In parallel, boron profiles were also recorded as it was reported that fluorine has significant influence on boron in-diffusion. The samples were prepared with a BF_3 flow of 0.7 sccm and the dwell time was fixed to 0 min.

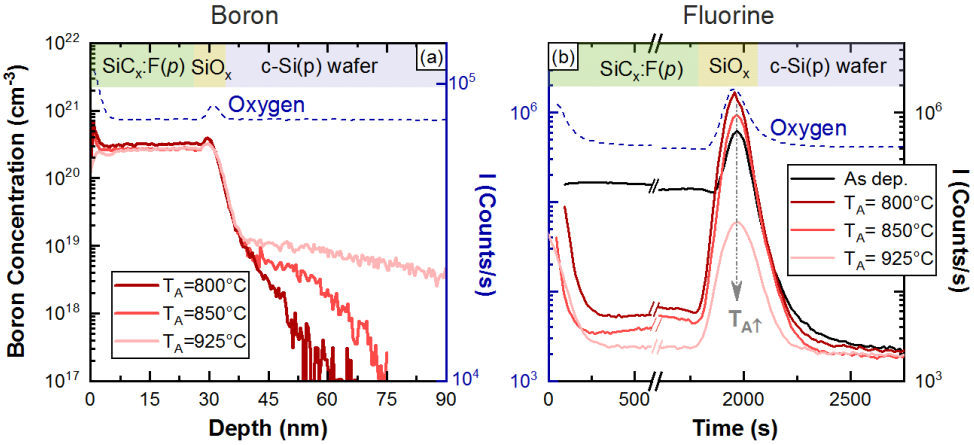

Figure 6.7 – (a) Boron depth profiles for the annealed samples, (b) fluorine profile for *as-deposited* and annealed samples measured by SIMS. The extent of oxygen peak was used to delineate the chemical SiO_x/c-Si wafer interface.

The layout of the different layers in the contact structure is illustrated on the top part of the Figure 6.7 for clarity. The oxygen peak is used to locate the chemical SiO_x/c-Si wafer interface as the etching rate for the SiC_x:F(*p*) differs with annealing temperature. It is important to note that oxygen plays an important role in the efficiency of boron-ionization, leading to an enhanced boron signal in the presence of oxygen. Figure 6.7(a) reveals that increasing annealing temperature results in deeper boron in-diffusion in the c-Si wafer as expected. Annealing at 800 °C leads to ~ 20–25 nm in-diffused region while annealing at 850 °C deepens the profile to ~ 35–40 nm. According to Figure 6.7(b), fluorine atoms show a uniform distribution in the doped layer with a small accumulation at the SiO_x layer already in *as-deposited* state. Following annealing at 800 °C, the fluorine concentration is drastically decreasing in the SiC_x:F(*p*) layer; the fluorine peak position remains unchanged in SiO_x, however the peak intensity and its FWHM enhance strongly. With increasing temperature, the overall fluorine concentration gradually reduces both in the SiC_x:F(*p*) layer and in the SiO_x. All in all, the SIMS

[4]SIMS measurements were performed by S. Eswara from Luxembourg Institute of Science and Technology. Contribution is gratefully acknowledged.

measurements are consistent with EDX, yet they provide more precise information thanks to higher atomic detection limit of SIMS technique.

As mentioned before, literature reports that SiO_x layers act as favourable site for the gettering of fluorine atoms as observed already in *as-deposited* state for our samples. Wright *et al.* proposed a two-step model to describe the bonding behavior of fluorine. In the initial phase of the annealing, fluorine migrates from the doped-Si layer through the SiO_x towards the c-Si and bonds to interfacial dangling bonds. This would lead to segregation of fluorine at the doped layer/SiO_x and SiO_x/c-Si wafer interfaces. Following the saturation of the interface regions with fluorine, additional incorporation occurs in the bulk of the SiO_x. The fluorine then breaks the Si–O bonds and displace oxygen by forming Si–F bonds. Ultimately the free oxygen atoms diffuse to the interfaces and oxidize the silicon further [Wright 1989]. Since the binding energy of Si–F is much higher (~ 5.73 eV) than the binding energy of Si–H (~ 3.18 eV), it can be expected to be more immune to external effects.

In parallel, the existence of fluorine within SiO_x increases the boron diffusivity and assists the boron diffusion through the SiO_x. Thus, it enhances boron penetration into c-Si, preventing the boron segregation in the SiO_x layer which may be detrimental for surface passivation. This phenomenon is described extensively in [Sung 1989].

Fluorine accumulation sites in thick oxide

Aiming to resolve the accumulation sites of the fluorine — either in the SiO_x or at the interfaces (poly-Si/SiO_x and SiO_x/c-Si) —, Tseng *et al.* performed a dedicated experiment by increasing

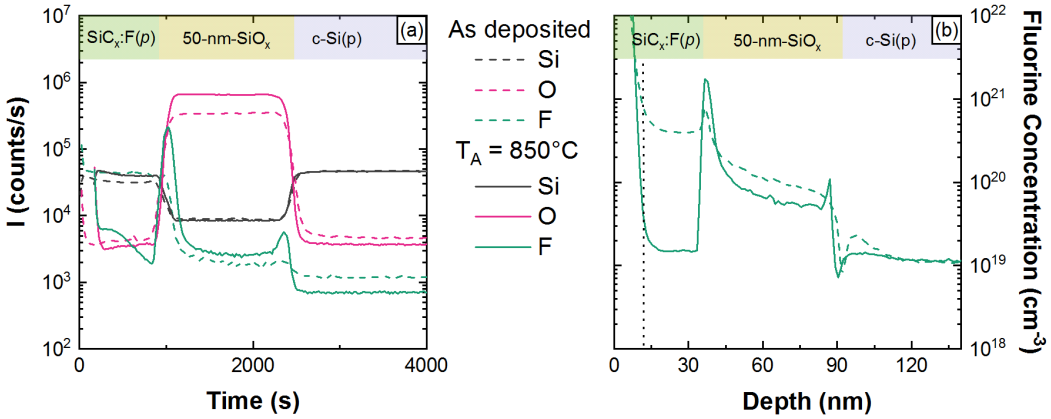

Figure 6.8 – (a) Si, O and F profiles measured by SIMS for the samples featuring 50-nm-thick thermal SiO_x and 30-nm-thick SiC_x:F(*p*) layer on top. The measurements were performed for *as-deposited* sample as well as for the sample annealed at 850 °C for 0 min. (b) The evolution of the quantified fluorine concentration upon annealing.

the gate oxide thickness from 1.25 to 50 nm and measuring SIMS. With 50-nm-thick gate oxide they could resolve the existence of two peaks, one at the poly-Si/SiO_x interface, and another one at the SiO_x/c-Si wafer interface [Tseng 1992b]. Inspired by this experiment which was performed for bipolar transistors produced with BF_2 implantation to undoped LPCVD poly-Si layer, we performed a similar experiment. To that end, the 50-nm-thick thermally grown SiO_x was produced and SiC_x:F(p) layer was deposited on top with PECVD. SIMS measurements were performed for the samples both in *as-deposited* state and after annealing at 850 °C for 0 min dwell time.

Figure 6.8(a) shows the measured Si, O and F profiles as a function of sputtering time before and after annealing with dash and solid lines, respectively. The layout of the different layers in the test structure is illustrated on the top part of the Figure 6.8 for clarity. According to the measured profiles, the Si and O signals does not reveal significant change with annealing. Regarding the fluorine, in *as-deposited* state uniform distribution within the layer is observed as seen previously in EDX analysis. Upon annealing, the fluorine signal weakens in the SiC_x:F(p) layer and become more dominant at the interface regions both in SiC_x:F(p)/SiO_x and SiO_x/c-Si. Figure 6.8(b) reveals the quantified fluorine concentration with respect to sputtering depth. As the fluorine pollution is induced by the gold coating of the sample, the quantification in the first 10-nm region — indicated with dotted line — is not valid. The fluorine concentration within the SiC_x:F(p) layer is determined as higher than 5×10^{20} cm^{-3}. However, it is important to note that quantification was performed by using reference c-Si sample with a known fluorine concentration, therefore it is prone to error as the sputtering yield differs in different matrix. Upon annealing, fluorine is diffusing from the SiC_x:F(p) layer

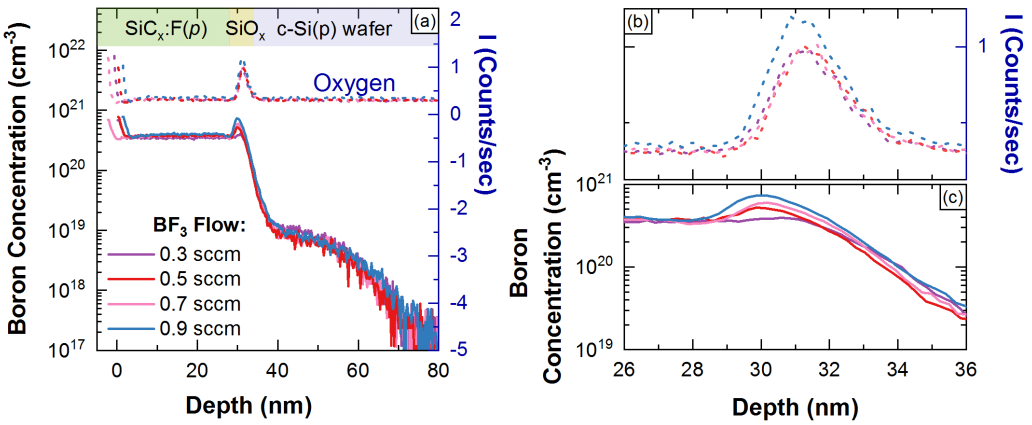

Figure 6.9 – (a) Boron profiles measured by SIMS for the samples prepared with various BF_3 flows and annealed at 850 °C for the same dwell time of 0 min. The extent of O peak was used to delineate the chemical SiO_x/c-Si wafer interface. A magnification of the O and B signals in the panels (b) and (c), respectively.

toward the SiO_x and accumulates at the defective interfaces revealing two pronounce peaks; one at SiC_x:F(p) /SiO_x interface and another one at SiO_x/c-Si interface.

Impact of doping concentration

To explore the mentioned stimulation of the boron in-diffusion due to the fluorine more elaborately, three samples were produced with different BF_3 flow and then annealed at the same temperature of 850 °C for the same dwell time of 0 min. The measured boron profiles by SIMS are depicted in Figure 6.9(a) and a magnification of the oxygen and boron signals at the SiO_x/c-Si wafer interface region are shown in Figure 6.9(b) and (c), respectively. Over the investigated BF_3 flow range from 0.3 to 0.9 sccm, the depth of the buried junction does not exhibit any visible discrepancy. It is therefore quite possible that such a small variation in the BF_3 flow does not change the doping concentration of the layer significantly, making the annealing temperature a more predominant factor that defines the buried junction depth. Magnifying the interfacial region in Figure 6.9(c), a clear trend of enhanced boron concentration at the SiO_x region with increased BF_3 flow is found. The effect of this accumulation with different BF_3 flows on surface passivation of the contact structure will be discussed in one of the following sections more elaborately. We note that as it is not feasible to control the boron and fluorine concentration separately during the PECVD deposition, it is not feasible to resolve the effect of fluorine on boron diffusion in our contact system.

Electrically active dopants

Figure 6.10 shows the electrically active boron profiles in the c-Si(p) measured by ECV for the samples produced with two extreme BF_3 flows used for this work — (a) 0.3 and (b) 0.9 sccm.

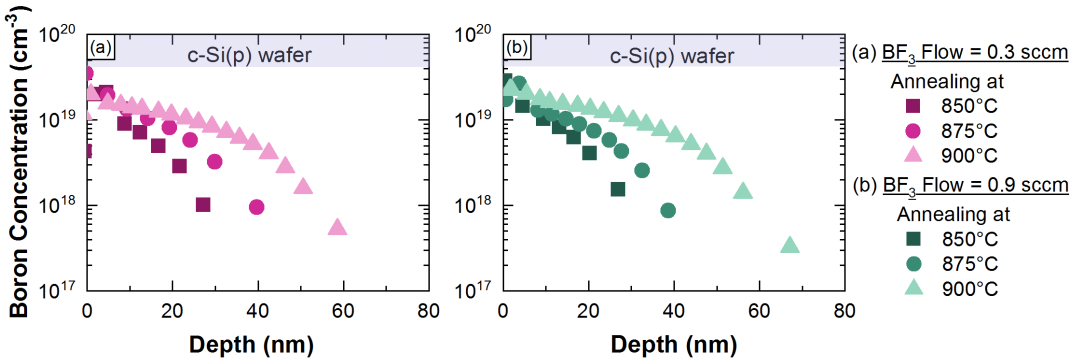

Figure 6.10 – Electrically active boron depth profiles in the c-Si(p) wafer measured by ECV technique for the samples prepared with BF_3 flow of (a) 0.3 and (b) 0.9 sccm. The samples were subsequently annealed at 850, 875 and 900 °C for the same annealing dwell time of 0 min.

The samples were subsequently annealed at various temperatures for the same annealing

dwell time of 0 min. As the measured concentrations within the partially crystallized doped layers fluctuate strongly, this part is excluded for clarity. The buried junction depth increases gradually with annealing temperature from 850 to 900 °C for both doping concentrations. After annealing at 850 °C, both samples show a depth of ~ 35 nm, at 875 °C the depth enhances to ~ 45 nm and for the samples annealed at 900 °C it becomes almost 70 nm. On the whole, we conclude that the used differences in the doping concentration of the layer do not yield a significant variation in the buried junction depth which is in accordance with the SIMS measurements presented in Figure 6.9(a). Additional to that the measured boron profiles with ECV and SIMS are rather similar.

6.3.4 Influence of carbon concentration

Following the detailed investigation about the compositional evolution of the fluorinated boron-doped contact structure upon annealing, its surface passivation quality was determined with QSSPC measurements using symmetric lifetime samples on *p*-type wafers. In parallel, the specific contact resistivities were measured for some of the samples by the TLM method. First of all, in order to study the influence of carbon concentration in the SiC_x:F(*p*) layer, the CH_4 flow was changed in a wide range during the PECVD process, while the other parameters were kept constant. It is observed that the CH_4 flow does not have significant effect on deposition rate as it is mainly determined by the SiH_4 flow. Therefore, the same deposition time is used for all samples presented here.

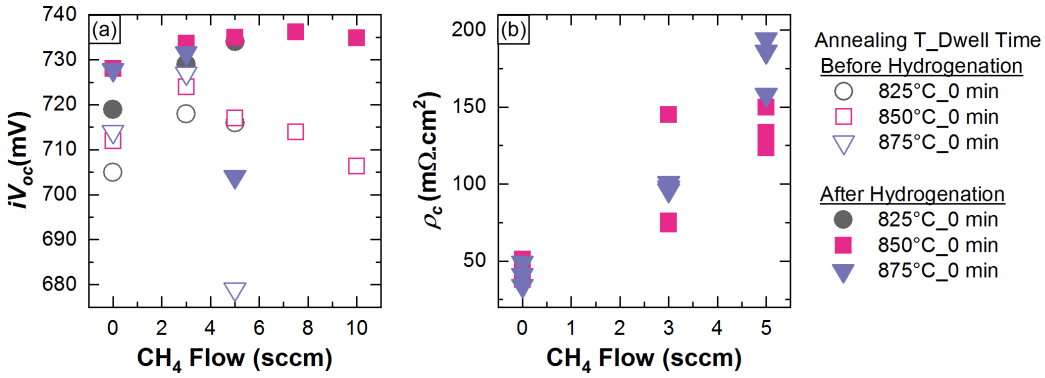

Figure 6.11 – Measured (a) iV_{oc} before hydrogenation — open symbols —, after hydrogenation — filled symbols — and (b) ρ_c values as a function of CH_4 flow for the sample produced with BF_3 flow of 0.3 sccm, annealed at 825, 850 and 875 °C for dwell time of 0 min.

Figure 6.11(a) reveals the measured iV_{oc} values before and after hydrogenation for the samples produced with fixed BF_3 flow of 0.3 sccm and varying CH_4 flow in the range of 0 to 10 sccm. Subsequent annealing was performed at 825, 850 and 875 °C for dwell times of 0 min. Concerning the samples prepared without CH_4 flow — CH_4 = 0 — , the iV_{oc} values before

hydrogenation are 705, 712 and 714 mV for annealing at 825, 850 and 875 °C, respectively. After hydrogenation, the overall trend remains same yet the measured iV_{oc} values exhibit an improvement by ~ 15 mV, reaching to iV_{oc} of 729 mV. By introducing a small CH_4 flow of 3 sccm, a clear upturn is observed for all annealing conditions, both before and after hydrogenation, attaining iV_{oc} values up to 735 mV. By increasing the CH_4 flow to 5 sccm, the passivation quality shows degradation which is particularly more pronounced for the sample annealed at 875 °C. After hydrogenation, samples annealed at 825 and 850 °C improve beyond 730 mV whereas the sample annealed at 875 °C reaches only to iV_{oc} of 704 mV. For CH_4 flows higher than the 5 sccm — high carbon concentrations — , only the samples annealed at 850 °C were probed. Without hydrogenation, iV_{oc} tends to decrease with CH_4 flow while after hydrogenation it shows initially a slight improvement up to 736 mV and eventually a saturation for higher carbon concentrations.

The obtained results suggest that the samples with higher carbon concentration benefit more from hydrogen-induced defect passivation. Two possible interpretations can explain the observed trend with increasing carbon concentration in the SiC_x:F(*p*); first the layer itself become more defective, second more carbon atoms can diffuse toward to SiO_x/c-Si wafer interface and react with SiO_x as well as provoke additional interface defects states. In all cases, low carbon concentration ensures a low defect density.

Measured ρ_c values are plotted over CH_4 flow in Figure 6.11(b) for the samples produced with CH_4 flows < 7 sccm and annealed at temperatures > 825 °C. The samples with high carbon concentration and annealed at low temperature exhibit fairly high ρ_c values and the measurements are prone to error due to the strong deviations, therefore they are not presented here. It is observed that the lowest ρ_c values are obtained with carbon-free boron-doped fluorinated layers after annealing at 850 and 875 °C. With increasing carbon concentration in the layer, the measured ρ_c is increasing systematically, probably due to the bandgap widening and related increase in band offset. As the definition of a good contact requires of good surface passivation and low contact resistivity, the most promising conditions for contact formation are identified as CH_4 flow of 5 sccm and annealing temperature of 850 °C.

6.3.5 Influence of doping concentration and annealing temperature

The optimization of the contact formation is not trivial due to the presence of several interrelated parameters. After determining the approximate optimum for the CH_4 flow as a 5 sccm in the previous section 6.3.4, the impact of BF_3 flow on surface passivation of the contact structure after annealing at various temperatures are presented in this section. Another motivation of this experiment was to resolve the effect of enhanced boron concentration at the SiO_x region with increased BF_3 flow observed in section 6.3.3 [see Figure 6.9(c)]. To that end symmetric test structures featuring SiC_x:F(*p*) layer with various boron and fluorine concentrations were prepared on *p*-type planar wafers.

Figure 6.12 depicts iV_{oc} values before and after hydrogenation as a function of BF_3 flow for the

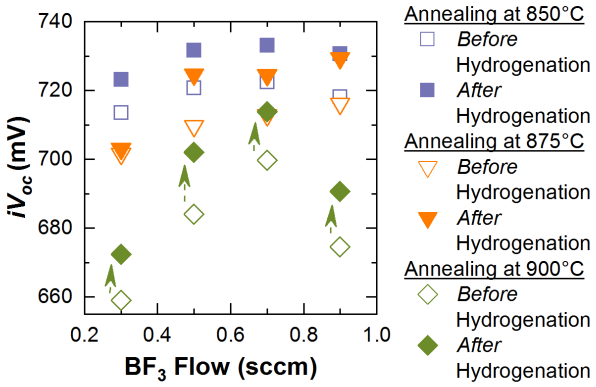

Figure 6.12 – Measured iV_{oc} values before (open symbols) and after (filled symbols) hydrogenation as a function of the BF_3 flow for the samples annealed at 850, 875 and 900 °C for 0 min.

samples annealed at 850, 875 and 900 °C. It is observed that the worst surface passivation is obtained for the samples prepared with BF_3 flow of 0.3 sccm for all annealing temperatures investigated here. Note that a flow of 0.3 sccm BF_3 was the condition used for the experiment performed in the previous section to find the optimum carbon concentration. With increasing BF_3 flow, an overall trend of improved surface passivation is observed. By examining more closely, it is seen that the samples annealed at 850 °C show an optimum at BF_3 flows of 0.5 and 0.7 sccm, reaching iV_{oc} values above 720 mV before hydrogenation. In essence, the doped layers, the SiO_x layer and the SiO_x/c-Si interface feature high defect densities upon annealing, presumably due to the boron diffusion. Hence, the observation of iV_{oc} > 720 mV already after annealing for contact formation suggests that fluorine reduces the interface trap density by passivating the dangling bonds as already mentioned in section 6.3.1. After hydrogenation of the samples annealed at 850 °C, iV_{oc} values up to 735 mV (J_0 = 4.9 fA/cm^2) are attained with the SiC_x:F(p) layer produced using the BF_3 flow of 0.7 sccm. The obtained results suggest that the enhanced boron concentration at the SiO_x region with increased BF_3 flow, which was monitored in section 6.3.3 for the samples annealed at 850 °C, does not have significant effect on the surface passivation, probably due to the presence of fluorine and its positive impact.

For the samples annealed at 875 °C, the measured iV_{oc} values are slightly lower but still around 730 mV, exhibiting a trend of improvement with increasing BF_3 flow. It is also perceived that with annealing at 900 °C, the iV_{oc} drops drastically. This is probably due to the more pronounced boron diffusion, as revealed in Figure 6.7(a) and Figure 6.10, which increases both Auger recombination and the number of defect states at the SiO_x/c-Si interface. Another possible reason could be the out-diffusion of the fluorine at this annealing temperature. However, it is still important to point out the fact that even after annealing at 900 °C, the iV_{oc} values up to 712 mV are attained which is not possible when TMB is employed as a dopant gas.

Overall, subsequent hydrogenation seems to be beneficial for all samples, leading to a gain up to 10 mV for the samples annealed between 850–875 °C, and up to 20 mV for those annealed at 900 °C. One hypothesis is that the sample annealed at 900 °C has more interface defects and can thus benefit more from hydrogen-induced defect passivation.

6.4 Conclusions

In this chapter, the effect of incorporating fluorine into the *in-situ* boron-doped hole-selective passivating contact was explored. Comparing the evolution of the minority-carrier lifetime curves, it is observed that the symmetric test samples prepared with the BF_3 dopant precursor clearly outperform those prepared with TMB. It is also shown that fluorinated hole contacts attain fairly high lifetimes even without any substantial hydrogenation. Compared to TMB–based hole contact, fluorinated contacts benefit less from hydrogenation while their overall performance is superior as evidenced by a measured iV_{oc} of 731 mV and *iFF* of 87 %. This observation is attributed to the fact that fluorine reduces D_{it} at the chemical SiO_x/c-Si wafer interface.

Microstructural changes are investigated by means of Raman spectroscopy and TEM. In the *as-deposited* state and after annealing at 800 °C, the fluorinated hole contact exhibits only an amorphous phase, while it shows strong crystalline phase after annealing at 850 °C and above. The chemistry of the SiO_x is found to be insensitive to annealing as long as it is intact. By evaluating the compositional changes in the SiC_x:F(*p*) layer and SiO_x interfaces with EDX and SIMS, it is found that the fluorine accumulates at the SiO_x interfaces. The obtained results suggest that the fluorine segregation at the SiO_x interfaces may help to passivate the interface defect states that are not terminated by hydrogen-induced defect passivation. This may be because the Si–F binding energy is much higher than that of Si–H.

The SiC_x:F(*p*) contact layer was further optimized in terms of carbon concentration, annealing temperature, boron-doping concentration together with the corresponding fluorine concentration. The optimum contact property is obtained with a CH_4 flow of 5 sccm and a BF_3 flow of 0.7 sccm leading to an iV_{oc} value of 735 mV with a corresponding J_0 of 4.9 fA/cm^2 after hydrogenation. The values obtained here are the best reported values for *in-situ* boron-doped hole-selective passivating contacts with a high thermal budget on *p*-type wafers.

7 Integration of the fluorinated hole contacts in c-Si solar cells

Summary

Following the promising results obtained in Chapter 6, here the potential of the fluorinated hole contact is investigated at the device level. To have a lean fabrication process, first an *in-situ* phosphorous-doped silicon carbide electron contact that can attain low recombination currents for the same annealing condition as the fluorinated hole contact is developed for front side. With this electron contact, iV_{oc} values of up to 746 mV (corresponding to J_0 of 4.2 fA/cm^2) are demonstrated on a planar *p*-type c-Si wafer. After the separate optimization of both polarities, the solar cells are realized by employing a simple approach based on a single co-annealing step that serves to form the junction of both contacts simultaneously. With this approach, planar both-sides-contacted *p*-type solar cells reaching a V_{oc} of 727 mV and a *FF* of 84 % are obtained. To increase the conversion efficiency, the front phosphorous-doped silicon carbide layer is adapted to textured surfaces by replacing the chemical oxide with UV ozone oxide. Finally, front-side-textured and rear-side-planar *p*-type solar cells are realized by replacing the standard ITO with an IO:Zr layer. The optics of the selected cells are further improved by applying a second anti-reflective coating of MgF_2 and efficiencies of up to 22.6 % are attained[1].

7.1 Introduction and motivation

The main advantages of the passivating contact scheme based on a thin oxide (SiO_x) and a heavily doped Si-layer (so-called TOPCON, poly-Si or POLO) are the following: (i) a full-area surface passivation without introducing a noticeable barrier to the charge-carrier transport and (ii) a compatibility with industrial high-temperature processes such as firing and $POCl_3$ diffusion. However, it is still not well defined how these contacts can be integrated into a solar cell with a simple manner. Different strategies have been demonstrated, based on either (i) the combination of a diffused homojunction front side with a poly-Si electron-selective

[1] The results presented in this Chapter will be part of an upcoming publication by Nogay *et al.*

rear contact which led to a world-record efficiency of 25.8 % for both-sides-contacted *n*-type c-Si solar cells [Richter 2017] or (ii) the integration of both electron- and hole-selective contacts in an interdigitated-back-contacted solar cell architecture which led to another world-record efficiency of 26.1 % for *p*-type c-Si solar cells [Haase 2018]. These are very promising results, yet the fabrication processes of both architectures are rather complicated and far from industrialization. An alternative option is to realize the front and rear contacts with thin SiO_x and doped Si-based layers; this is particularly attractive as it would minimize the need for structuring steps, enabling a lean fabrication process. Recently, both-sides-contacted poly-Si–based solar cells were demonstrated on *n*-type wafers with an efficiency of 22.3 % using ion-implanted poly-Si [Peibst 2017]. The process step at high temperature for dopant diffusion and crystallization is one of the main advantages of the abovementioned technologies. For Czochralski (CZ) as well as multicrystalline materials, this step can be used for impurity gettering from the bulk and to deactivate thermal donors. Crystallization of the deposited layers promoted by the thermal treatment reduces the contact resistivity to the metallization as the crystalline phase can accommodate a large number of active dopants. Additionally, poly-Si-based contacts feature a lower sheet resistance, and therefore relax the constraints on the electrode — metal grid and TCO — design. Finally, another potential benefit of the high crystallinity is the reduced optical parasitic absorption as already demonstrated in Chapter 3 for traditional silicon heterojunction solar cells.

Motivated by these potential advantages, an *in-situ* phosphorous-doped SiC_x–based passivating contact is developed to provide a full-area front contact with low surface recombination velocity and low contact resistivity. A major objective is the use of a thermal treatment similar to one used to form the SiC_x:F(*p*) rear contact, such that a single annealing step can be applied to co-process both contacts simultaneously. The effect of applying various TCOs on surface passivation is investigated for both contacts with symmetric test structures. As the conversion efficiency can be increased by light trapping through the use of textured wafers, the process for the front SiC_x(*n*) is adapted to textured surfaces by replacing the chemical SiO_x with UV-O_3 oxide. The application of Zr-doped In_2O_3 — hereafter referred as IO:Zr — as an alternative to ITO is investigated in order to monitor if the superior electrical and optical properties of the layer would manifest themselves at the device level. Motivated by the fact that light reflection at the front surface can be reduced by adding a second anti-reflective coating layer with a low refractive index, an 85-nm-thick MgF_2 layer is thermally evaporated to the front side of the solar cells.

7.2 Experimental details

Passivating contacts were investigated using 200-μm-thick chemically polished 4-inch *p*-type float-zone <100> c-Si wafers with a resistivity of 2 Ω cm. For front-layer development, a thin SiO_x layer (~ 1.2 nm) was formed in a hot HNO_3 solution and *in-situ* phosphorous-doped SiC_x(*n*) layers were deposited by parallel-plate PECVD. The samples were then annealed in an inert gas atmosphere at temperatures between 800 and 900 °C. This was then followed by a

hydrogenation process. The decay of the photoconductance was used to measure the effective minority-carrier lifetime as a function of the excess minority-carrier density and to determine the values of iV_{oc} and *iFF*. The method of Kane and Swanson was applied to extract J_0 at an excess-carrier density of 5×10^{15} cm^{-3}. Structural changes of the SiC_x layers were investigated with Raman spectroscopy. The impact of different TCOs and their deposition processes on surface passivation was investigated. The mobility and free-carrier concentration of the TCO layers were measured by Hall effect in the Van der Pauw configuration using an HMS-5000 instrument. The thickness of the interfacial SiO_x and of the doped layers was determined by variable-angle spectroscopic ellipsometry in the spectral range of 0.6 to 6 eV.

To integrate the developed passivating contacts into the solar cells, both-sides-contacted *p*-type solar cells featuring front SiC_x(*n*) and rear SiC_x:F(*p*) were prepared either on planar or on front-side-textured wafers by co-annealing. The process flow for cell manufacturing is depicted in Figure 7.1. The interfacial SiO_x layer was formed after wet-chemical cleaning, either in a hot HNO_3 solution or by photo-oxidation using a mercury lamp as a UV source. Subsequently, *in-situ* doped layers were deposited on both sides by parallel-plate PECVD for solar cell precursors. The samples were then subjected to a thermal treatment at temperatures above 800 °C in an inert gas atmosphere for 0 min dwell time. This was followed by a hydrogenation process. Following the preparation of the cell precursors, TCO layers were sputtered onto both sides. A silver reflector was sputtered onto the rear side and silver paste was screen printed to form the front-grid metallization, followed by a curing step at 210 °C for 30 minutes. Current density-voltage (*J*-*V*) characteristics of the cells were measured with a source meter (Keithley, 2601A), using an AAA solar simulator (Wacom) calibrated to 100 mW cm^{-2} illumination. Additionally, suns-V_{oc} measurements were performed to obtain the pseudo *J*-*V* curves without the contribution from the series resistance.

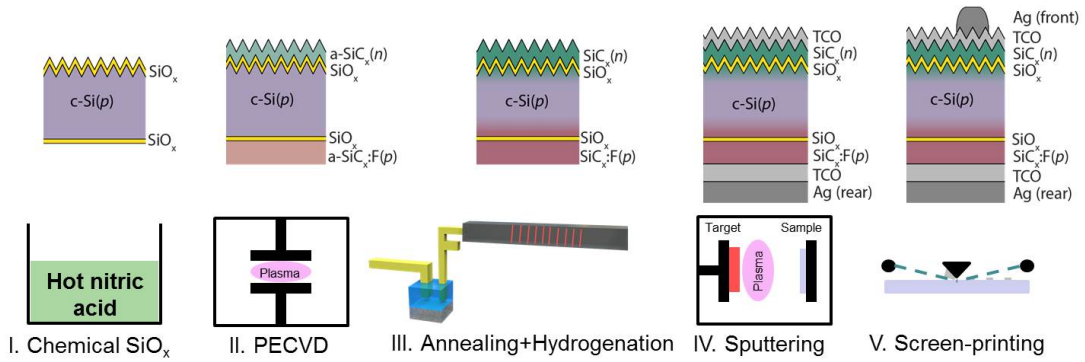

Figure 7.1 – Process flow for cell fabrication and final device structure. The in-diffused regions and structural change of the deposited layers upon annealing are indicated in the sketch by a change in the colors. Layers are not drawn to scale.

7.3 Phosphorus-doped silicon carbide as a front layer

With the intention of avoiding potential *FF* limitation from the SHJ front contact and having a lean fabrication process, we targeted a cell structure featuring passivating contacts with high thermal budget at both front and rear sides. To that end, the development of a phosphorous-doped $SiC_x(n)$ layer compatible with the thermal treatment similar to the one for rear SiC_x:F(p) layer were carried out. In Chapter 6, the optimum annealing condition was found to be 850 °C for 0 min for SiC_x:F(p). Here as a first step, symmetric test samples with $SiC_x(n)$ were realized on planar p-type c-Si wafers to investigate the optimal conditions for junction formation[2].

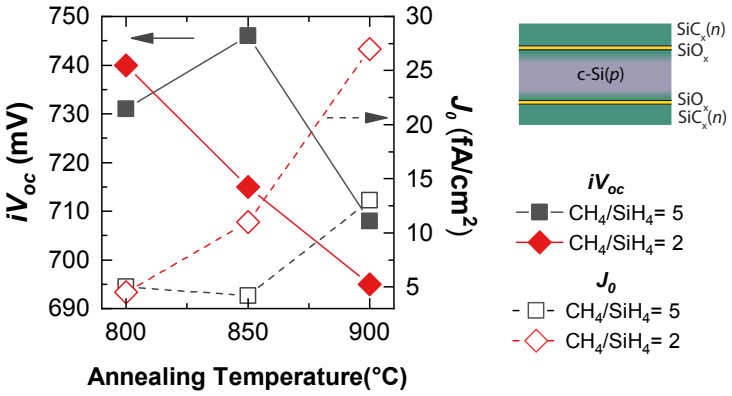

Figure 7.2 – iV_{oc} (filled symbols with solid lines) and J_0 (open symbols with dashed lines) of $SiC_x(n)$ samples prepared with two different CH_4 to SiH_4 ratios as a function of annealing temperature. Schematic of the symmetric test structure on top right.

Figure 7.2 shows iV_{oc} and J_0 values for symmetric test structures employing $SiC_x(n)$ layers prepared with two different CH_4 to SiH_4 ratios as a function of annealing temperature. It is observed that after thermal treatment at 800 °C, the sample with lower carbon concentration ($CH_4/SiH_4 = 2$, $iV_{oc} = 740$ mV) shows better surface passivation compared to the sample with high carbon concentration ($CH_4/SiH_4 = 5$, $iV_{oc} = 731$ mV). For the sample produced with a ratio of 2, the surface passivation quality is decreasing drastically with annealing temperature, as evidenced by a drop in iV_{oc} from 740 to 700 mV. A possible interpretation for this drop is an increased Auger recombination due to the more prominent phosphorous in-diffusion. For both carbon concentrations, the annealing at 900 °C appears to be detrimental with respect to surface passivation, probably due to local breakup of the SiO_x and pinhole formation. Following the thermal treatment at 850 °C, the sample with the high carbon concentration exhibits an optimum surface passivation quality, reaching an iV_{oc} value of 746 mV which corresponds to J_0 value of 4.2 fA/cm^2.

[2]The results presented in this section were obtained in collaboration with A. Ingenito, manuscript is under preparation. Contribution is gratefully acknowledged.

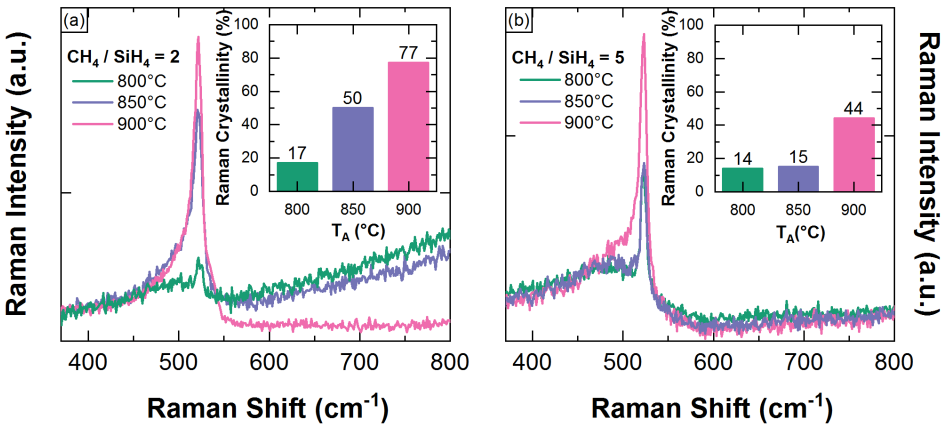

Figure 7.3 – Raman spectra of the $SiC_x(n)$ contacts produced with two different CH_4 to SiH_4 ratios as a function of annealing temperature. Insets show the calculated Raman crystallinities in percentage.

The microstructural evolution of the $SiC_x(n)$ layers upon annealing were studied with Raman spectroscopy. Figure 7.3 shows the Raman spectra of the samples prepared with CH_4 to SiH_4 ratio of (a) 2 — low carbon concentration — and (b) 5 — high carbon concentration. For both conditions, the samples were annealed at 800, 850 and 900 °C. It is observed that the samples prepared with the ratio of 2, the peak at the 520 cm^{-1} that corresponds to the crystalline phase, is only slightly visible after annealing at 800 °C. With further increase in temperature, the peak becomes more pronounced indicating a gradual increase of the crystallized volume fraction in the $SiC_x(n)$ layer. The inset of the Figure 7.3(a) presents the calculated Raman crystallinity values that exhibit a rise from 17 to 77 % by augmenting the annealing temperature from 800 to 900 °C. The Raman spectra for the samples produced with the ratio of 5 and annealed at different temperatures are depicted in Figure 7.3(b). It is observed that the samples reveal a weaker crystallinity compared to the $SiC_x(n)$ layer produced with lower carbon concentration. After annealing at 800 and 850 °C, the layer crystallinity remains almost the same, reaching a Raman crystallinity of only 14 and 15 %, as seen in inset. With annealing at 900 °C, the crystallinity increases to 44 %. This observation suggests that the increased carbon concentration in the $SiC_x(n)$ layer results in a retarded crystallization.

Based on the obtained results, we conclude that the samples with low carbon concentration reveal better performance at 800 °C while the optimum temperature appears to be 850 °C for the sample with high carbon concentration. This can be explained with the fact that increased carbon concentration reduces the doping efficiency of the $SiC_x(n)$ layer. Hence annealing at higher temperature is needed to increase the dopant in-diffusion from the doped layer to c-Si to provide sufficient band bending and therefore prevent injection of minority carriers from c-Si into the $SiC_x(n)$ contact layer more effectively. Due to the superior performance of the $SiC_x(n)$ contact structure produced with high carbon concentration ($CH_4/SiH_4 = 5$) upon

annealing at 850 °C, it is selected for cell integration. Hereinafter, all the presented planar *p*-type solar cells feature the same $SiC_x(n)$ front layer composition.

7.4 Results and discussion I: Planar solar cells

At the first stage, since the optimization of SiC_x:F(*p*) and $SiC_x(n)$ layers were performed on planar surfaces, both-sides-contacted planar *p*-type solar cells with 2 cm × 2 cm area were realized. The process flow is described in section 7.2 (see Figure 7.1).

7.4.1 The effect of front layer thickness

With the goal of determining the optimum front layer thickness, a set of cells featuring the same SiC_x:F(*p*) rear contact and $SiC_x(n)$ front contact with various thicknesses were realized, using 70 and 116 nm of ITO as front and rear TCO, respectively. The thickness of front $SiC_x(n)$ layer was altered from 11 to 24 nm as measured after the thermal treatment by means for spectroscopic ellipsometry. The extracted cell parameters from the one-sun *J*-*V* characteristics as a function of $SiC_x(n)$ front contact thickness are shown in Figure 7.4. The iV_{oc} and *iFF* values derived from the minority-carrier lifetime curves measured from the cell precursors before the metallization are indicated in Figure 7.4(a) and (c) with pink stars.

Prior to metallization, all both-sides-contacted planar *p*-type solar cells reveal iV_{oc} values between 737 and 739 mV which correspond to total J_0 values of 4.8–5.0 fA/cm^2. The pseudo V_{oc} values extracted from suns-V_{oc} measurement are 728 mV for the best cell out of five on each wafer that features different thickness. Figure 7.4(a) shows that the final V_{oc} values are in range of 720 to 725 mV for most of the cells. Thus, they are not affected by the $SiC_x(n)$ thickness significantly except the cell featuring the thinnest front layer that reveals strong V_{oc} inhomogeneity across wafer compared to the rest. Overall, the difference between iV_{oc} and V_{oc} is ca. 13 mV and remains unaffected by the thickness variation.

According to Figure 7.4(b), J_{sc} exhibits a linear dependence on $SiC_x(n)$ layer thickness and it decreases gradually due to the increasing parasitic absorption as the front layer gets thicker. By calculating the slope of this gradual decline, the related J_{sc} loss is determined to be approximately 0.12 mA/cm^2 per nm. The EQE curves shown in Figure 7.4(f) provide a consistent description for the trend of decreased J_{sc} with increased thickness, exhibiting prominent lost at short wavelengths below 600 nm when going from 11- to 24-nm-thick $SiC_x(n)$ front layer. Except for very short wavelengths below 400 nm, no variation is detected in the reflection data of the presented cells.

Regarding the *FF* values, before metallization the *iFF* values are increasing slightly but systematically from 86.5 to 87.2 % with $SiC_x(n)$ front layer thickness. However the final *FF* values of the cells are in the range of 81 to 82 % and they do not exhibit a clear trend with thickness. The pseudo *FF* values extracted from suns-V_{oc} measurement are increasing incrementally

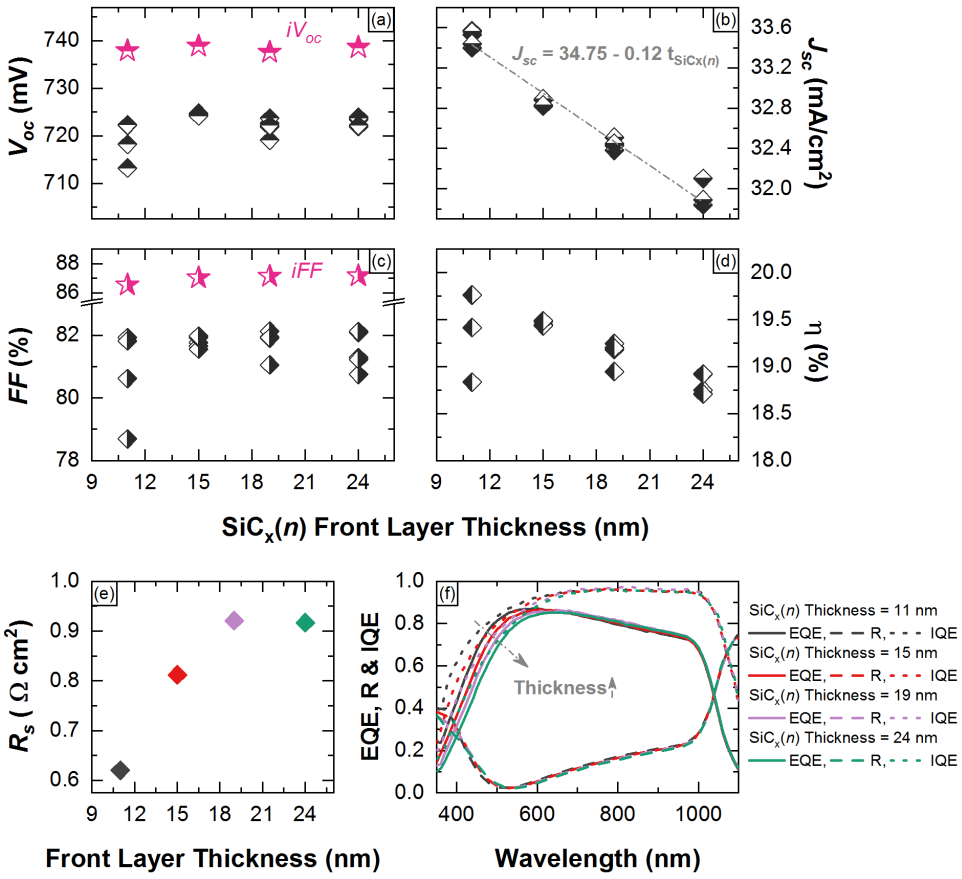

Figure 7.4 – (a) V_{oc}, (b) J_{sc}, (c) *FF*, and (d) efficiency of the of the both sides-contacted solar cells with different SiC$_x$(n) front layer thicknesses extracted from one-sun *J*-*V* characteristics. The implied values before metallization are indicated with stars in panel (a) and (c). (e) Calculated total series resistance by comparing suns-V_{oc} curve with one-sun *J*-*V* curve. (f) EQE, R and IQE of the cells.

from 84.3 to 85.3 %. Additionally, the total series resistances (R_s) of the cells were determined under illumination conditions by calculating the voltage difference of the suns-V_{oc} and the one-sun *J*-*V* data at maximum power point. The extracted values are plotted in Figure 7.4(e) as a function of SiC$_x$(n) thickness. It is observed that the R_s value is 0.62 Ω cm^2 for the cell with 11-nm-thick SiC$_x$(n) front layer. When the thickness of the SiC$_x$ layer is increased to 15 nm, R_s increases to 0.81 Ω cm^2 and it reaches to a value of 0.92 Ω cm^2 for 19- and 24-nm-thick SiC$_x$(n) front layers. We therefore conclude that the cells with thick front layers suffer more from the losses related with the series resistance.

Overall, the conversion efficiency is dictated by the J_{sc} trend showing a linear decrease with increasing SiC$_x$(n) front layer thickness. Even though the sample with thinnest SiC$_x$(n) layer reveals the lowest R_s, as the *FF* and iV_{oc} values suffer from strong fluctuations, the 15-nm-thick

$SiC_x(n)$ is selected for the further optimization experiments.

7.4.2 The effect of TCO deposition on surface passivation

In an attempt to assess the contribution of the TCO deposition on the observed difference between iV_{oc} before metallization and final V_{oc} of the solar cells, dedicated experiments were performed. To that end the impact of TCO deposition on $SiC_x(n)$ front contact and SiC_x:F(p) rear contact was studied separately to identify the related losses more precisely. For both experiments, planar p-type c-Si wafers were used and doped layers were symmetrically deposited on both sides of the wafers. Following the annealing at 850 °C and subsequent hydrogenation, various TCOs such as sputtered tungsten-doped indium oxide (IWO), aluminum doped zinc oxide (ZnO:Al), indium-tin-oxide (ITO) and low pressure chemical vapor deposited (LPCVD) boron-doped zinc oxide (ZnO:B) were applied symmetrically[3]. Prior to TCO depositions, the samples were dipped in 5 % diluted HF solution for 1 min to remove the native SiO_x. After the TCO deposition, samples were cured at temperatures of 200, 250 and 300 °C for 10 min on a hot plate in air ambient. Additionally, the role of plasma luminescence — UV exposure — and ion bombardment on the surface passivation were investigated for both contacts with dedicated experiments similar to the one described in Chapter 5.

Front $SiC_x(n)$ contact

Figure 7.5 shows the evolution of the injection-dependent lifetime characteristics for p-type c-Si wafers featuring a symmetric chemical $SiO_x/SiC_x(n)$ electron-selective passivating contact — as depicted in panel (f) — after depositing (a) IWO, (b) ZnO:Al, (c) ZnO:B, (d) ITO overlayer, as well as after curing at different temperatures. The measured iV_{oc} and iFF values for the symmetric test structures were 742–743 mV and 87.5–87.7 % before applying the TCO. The dark-grey and orange open symbols represent the measurements performed before and after TCO deposition, respectively. For all sputtered TCOs investigated here, a drastic drop is observed in both iV_{oc} — high-injection level — and iFF — low-injection level — right after the depositions. For the sample coated with LPCVD ZnO:B, only a prominent tailing at the low-injection level is detected whereas the iV_{oc} value appears to be unaffected significantly as shown in Figure 7.5(c). After curing at 200 °C, a slight but deficient improvement is observed in lifetime curves, nevertheless tailing at the low-injection level is preserved. After curing at 250 and 300 °C, a strong recovery in high-injection level — iV_{oc} — is observed for all sputtered TCOs while still presenting a strong tailing at the low injection. The sample with LPCVD ZnO:B exhibits more efficient recovery with curing at 250–300°C in low injection.

Aiming to clarify the reason of the tailing at the low-injection level, the same measurements were performed after etching the TCOs with diluted HCl solution. Since it was observed that the samples with the sputtered TCOs reveal extremely low sheet resistance values as

[3]IWO, ZnO:Al and ZnO:B depositions were performed by J. Diaz and L. Ding from CSEM. Their contribution is gratefully acknowledged.

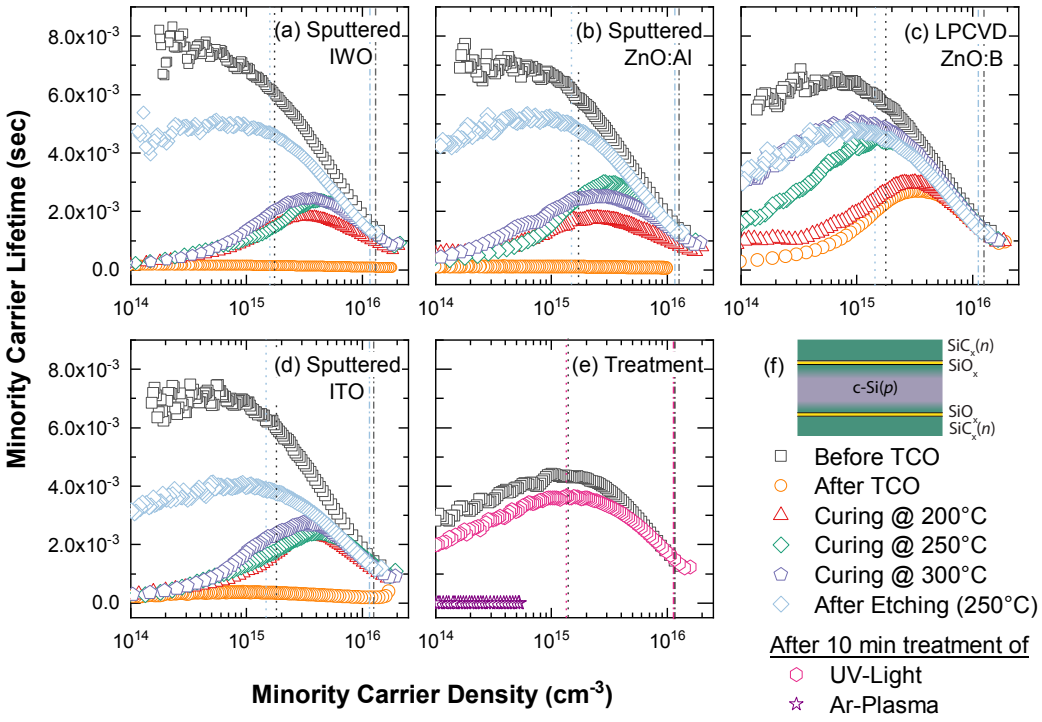

Figure 7.5 – Measurements of minority-carrier lifetime characteristics as a function of excess-carrier density for *p*-type c-Si wafer featuring a symmetric chemical $SiO_x/SiC_x(n)$ electron-selective passivating contact after depositing (a) IWO, (b) ZnO:Al, (c) ZnO:B, (d) ITO overlayer, as well as after curing at different temperatures. (e) The effect of 10 min UV-light treatment and 10 min argon-plasma treatment on the lifetime characteristic of the symmetric test sample. Dotted lines and dash-dotted lines represent maximum power point and open-circuit conditions, respectively for the lifetime curves with corresponding color. (f) Sketch of the symmetric test structure.

determined by the QSSPC measurements, it is possible that the photogenerated carriers of the QSSPC measurement are shielded by the conductive TCO, and consequently the observed effects could be the measurement artifacts or shunting of the front and rear TCOs. Indeed, after etching of the TCOs the tailing effect disappears for all sputtered samples (for clarity only the curves for the samples cured at 250 °C and etched are plotted in Figure 7.5 with light-blue open symbols as this was the best recovery condition for most of the TCOs investigated here).

The sample with LPCVD ZnO:B behaves differently since the tailing disappears already for the cured samples. We propose an explanation related to the properties of ZnO:B. In the *as-deposited* state the sheet resistance (R_{sheet}) of the ZnO:B is 41 Ω/□ which is comparable with the other TCOs. For this case, the tailing at low-injection level is related to shielding of the QSSPC signal by the free carriers in the ZnO:B layer. However, its R_{sheet} becomes 460 Ω/□ after curing at 200 °C which is already much higher than the other TCOs investigated

here, and after curing at higher temperatures, R_{sheet} of ZnO:B reaches to the high values that are above the limit of the four-point-probe measurement. Thus, the true behaviour of the photogenerated carriers in Si is measurable through the ZnO:B when it lost its conductivity by curing. Consequently, the etched sample shows a lifetime characteristic very similar to the one after curing at 300 °C.

Dotted and dash-dotted lines denote the injection levels associated to the implied voltages at maximum power point and at open-circuit condition, respectively. The colours are related to the corresponding lifetime curves before TCO deposition and after stripping off the TCO. By comparing these two cases, the iV_{oc} loss after TCO deposition is determined as 3 mV for ZnO:Al, 4 mV for ITO, 4 mV for ZnO:B and 5 mV for IWO. In the same way the *iFF* loss is determined to be 0.4 % for ZnO:Al, 1.0 % for ITO, 0.6 % for ZnO:B and IWO.

Figure 7.5(e) shows that UV light exposure affects $SiC_x(n)$ contacts only slightly, leading to ~ 1 mV loss in iV_{oc} and less than 0.2 % loss in *iFF*. This can be considered in the range of the QSSPC measurement error. Conversely, exposing the sample to direct argon plasma for 10 min is found to be quite detrimental for surface passivation.

Rear SiC_x:F(*p*) contact

A systematic experiment similar to the one presented in previous section was also performed for the symmetric test structures featuring chemical SiO_x/SiC_x:F(p) contact in order to study TCO related V_{oc} losses of the rear hole contact. To that end, the test structures were prepared symmetrically on planar *p*-type wafers, the schematic of the sample structure is depicted in Figure 7.6(f).

Injection-dependent lifetime curves were measured at different stages of the process such as before TCO deposition, after depositing (a) IWO, (b) ZnO:Al, (c) ZnO:B, (d) ITO, and after curing at different temperatures for 10 min. The iV_{oc} and *iFF* values extracted from the lifetime curves for the symmetric test structures before TCO depositions were 738 mV and 86 %, respectively. Figure 7.6 shows that after sputtering IWO and ZnO:Al, the lifetimes are degrading drastically both at high- and low-injection level, whereas for ITO the drop appears to be less severe. The measured iV_{oc} values drop 38 mV for IWO, 42 mV for ZnO:Al and 11 mV for ITO. It is seen that also the sample with LPCVD ZnO:B exhibits a slight loss in effective lifetime after deposition — iV_{oc} drop of 6 mV. In terms of recovery, the trend is similar to the case of TMB–based contacts presented in Chapter 5 and to the $SiC_x(n)$ front layer presented in the previous section. The SiC_x:F(p) contact shows the best recovery after curing at temperature of 250 °C for all the TCOs investigated here — represented with green open symbols. Only IWO reveals very similar performance after curing at 250 and 300 °C, while for the rest slight decrease of the lifetime curves both in high- and low-injection levels is observed after curing at 300 °C.

The effective lifetimes at maximum power point and open-circuit conditions are represented with dotted lines and dash-dotted lines, respectively, the colours refer to the corresponding

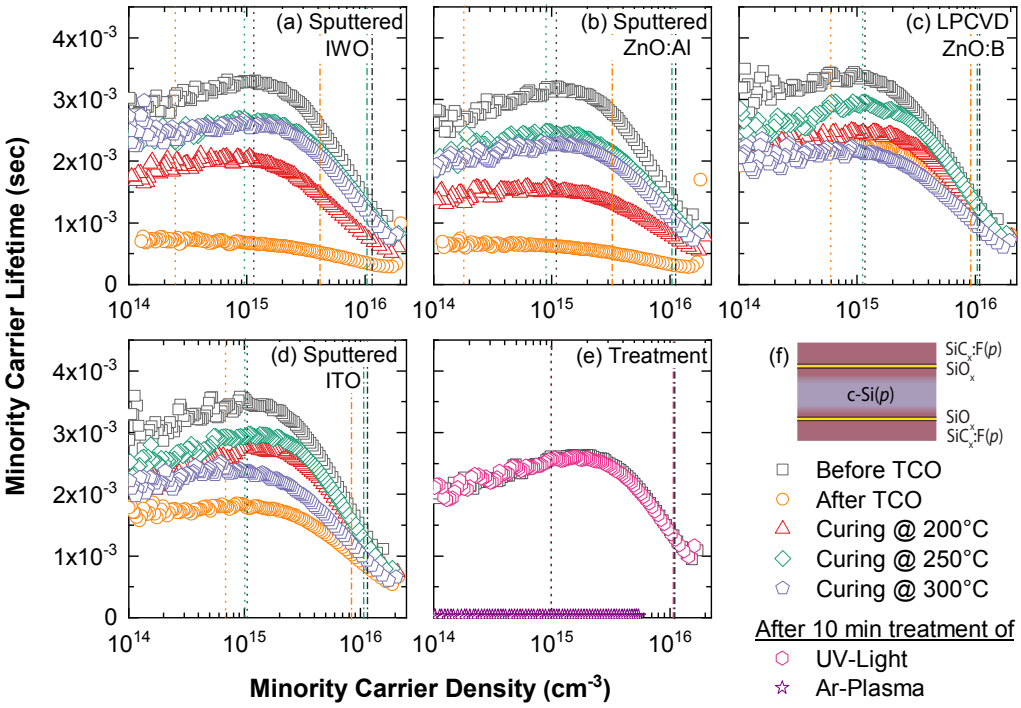

Figure 7.6 – Measurements of minority-carrier lifetime characteristics as a function of excess-carrier density for *p*-type c-Si wafer featuring a symmetric chemical SiO_x/SiC_x:F(*p*) hole-selective passivating contact after depositing (a) IWO, (b) ZnO:Al, (c) ZnO:B, (d) ITO overlayer, as well as after curing at different temperatures. (e) The effect of 10 min UV-light treatment and 10 min argon-plasma treatment on the lifetime characteristic of the symmetric test sample. Dotted lines and dash-dotted lines represents maximum power point and open-circuit conditions, respectively for the lifetime curves with corresponding color. (f) Sketch of the symmetric test structure.

colour of the lifetime curves. The severe drop becomes more visible by determining the shift of the dark-grey (before TCO) and orange (after TCO) dotted and dash-dotted lines toward the lower injection levels. For better clarity, the effective lifetimes at maximum power point and open-circuit conditions are shown only for the samples cured at 250 °C with green lines since this represents the best recovery condition. By comparing the lifetime curves before TCO and after curing at 250 °C, the iV_{oc} loss is determined as 5 mV for ZnO:Al, 4 mV for ITO, 2 mV for ZnO:B and 5 mV for IWO. In the same way the *iFF* loss is determined to be 0.7 % for ZnO:Al, 0.4 % for ITO, 0.5 % for ZnO:B and 0.7 % for IWO. Figure 7.6(f) reveals that 10 min UV exposure has no effect on the lifetime curve of the chemical SiO_x/SiC_x:F(*p*) contact structure whereas also for this type of contact the exposure to direct argon plasma is quite detrimental for the surface passivation.

To assess the electrical performance of the SiC_x:F(*p*) contact with different TCOs, the specific

Table 7.1 – Summary of the TCO thicknesses and measured ρ_c for SiC_x:F(p) contact after curing at 250 °C.

	IWO	**ZnO:Al**	**ZnO:B**	**ITO**
TCO Thickness [nm]	87	63	990	92
ρ_c **[mΩ cm^2]**	56.8	95.1	221.3	23.3

contact resistivity (ρ_c) that compromises of the contributions from different interfaces such as Ag/TCO, TCO/SiC_x:F(p), SiC_x:F(p)/SiO_x, SiO_x/c-Si(p) as well as the in-diffused region were measured with the TLM method. As the goal is to determine the best TCO candidate with respect to electrical properties, the different contributions were not identified separately. Table 7.1 demonstrates the thicknesses of the TCOs deposited for this investigation as well as the measured ρ_c values after curing at 250 °C. It is observed that the lowest contact resistivity is obtained with ITO which is determined as 23.3 mΩ cm^2, whereas the highest value is measured for the ZnO:B as 221.3 mΩ cm^2. Assuming that the ρ_c value was the only contribution to the series resistance, the *FF* should be reduced by 1 % (absolute) with respect to the *iFF* in the case of replacing ITO with ZnO:B. Consequently, regarding the surface passivation and electrical properties, ITO is defined as a best option to use for SiC_x:F(p) contacts among the investigated TCOs here. Comparing the impact of TCO deposition on the SiC_x:F(p) contact with the TMB–based Si(i)/SiC_x(p) contact, it is observed that SiC_x:F(p) reveals less degradation in terms of surface passivation, however it exhibits slightly higher contact resistivity values.

7.4.3 The impact of deposition parameters of the rear contact

In this section, the influence of different deposition parameters such as doping concentration, carbon concentration and annealing temperature for a SiC_x:F(p) hole-selective passivating contact is investigated at the device level. To have a reliable comparison, the front SiC_x(n) layer as well as the applied front/rear ITO were kept constant. The process flow for the cell fabrication is described in section 7.2 and depicted in Figure 7.1.

Doping concentration

The impact of doping concentration as well as the related fluorine concentration were studied by changing the BF_3 flow from 0.3 to 0.9 sccm during the rear SiC_x:F(p) contact deposition. The both-sides-contacted planar p-type solar cells featuring SiC_x(n) front contact were annealed at 850 °C for 0 min and hydrogenated using thermal release of hydrogen from a SiN_x layer. Figure 7.7 shows the extracted cell parameters from one-sun J-V curves together with implied values extracted from minority-carrier lifetime curves represented with green stars.

Figure7.7(a) reveals that the V_{oc} values of the cells are following the trend of iV_{oc} values measured from the cell precursors before metallization. The cell produced with the BF_3 flow

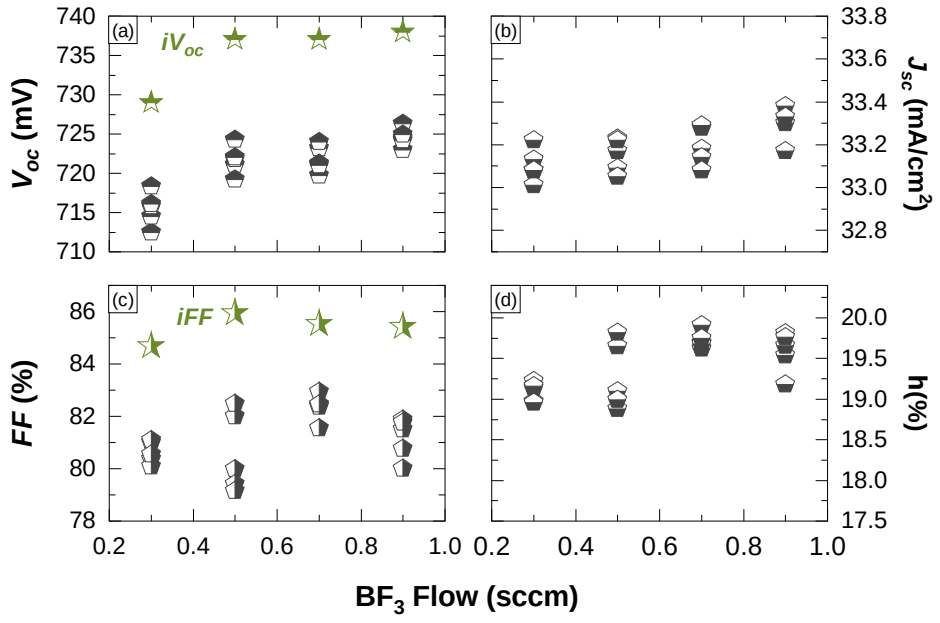

Figure 7.7 – (a) V_{oc}, (b) J_{sc}, (c) *FF*, and (d) efficiency of the of the both sides-contacted solar cells employing the same SiC_x(*n*) front contact and the SiC_x:F(*p*) rear contact prepared with different BF_3 flow. Implied values extracted from the minority lifetime curves before metallization are indicated with green stars in the panels (a) and (c).

of 0.3 sccm shows the lowest V_{oc} values with some fluctuation in the range of 710 to 720 mV. With increasing BF_3 flow, the iV_{oc} values measured before metallization as well as the final V_{oc} values are increasing. The difference in between iV_{oc} and V_{oc} is determined as 10–13 mV for the cells presented in this section. As it was demonstrated in previous sections, the TCO deposition can only partially be responsible for the V_{oc} loss observed in the final devices. A more detailed loss analysis will be presented shortly after for a similar cell structure.

Regarding the J_{sc}, all the planar *p*-type cells exhibit similar values except the one prepared with BF_3 flow of 0.9 sccm which shows slightly better J_{sc}. The reason for this trend is not clear, however it is important to note that the presented range is quite small and our front ITO deposition is prone to some process related fluctuations.

Figure 7.7(c) reveals that *iFF* of the cell precursors before metallization are around 85–86 %. The final *FF* values indicate an optimum at 0.7 sccm BF_3 flow reaching impressive *FF* value of 83 %. Overall, the conversion efficiencies of the presented cells are in the range from 19.5 to 20 % for the BF_3 flows above 0.3 sccm revealing stronger fluctuation for the cells produces with BF_3 flow of 0.5 and 0.9 sccm. The best cell of this series attains a conversion efficiency of 19.9 % with V_{oc} of 721 mV, J_{sc} of 33.3 mA/cm^2 and *FF* of 83 %.

Carbon concentration

To further optimize the both-sides-contacted planar *p*-type solar cells featuring SiC_x(*n*) front electron contact and SiC_x:F(*p*) rear hole contact, the influence of the carbon concentration within the SiC_x:F(*p*) layer was studied. To that end, the ratio of the CH_4 to SiH_4 flow was varied from 0.25 to 0.80, the ratio employed in previous sections was 0.33. Two sets of solar cells were prepared to assess additionally the impact of annealing temperatures, here 850 and 875 °C for 0 min dwell time. For the rear SiC_x:F(*p*) layer deposition, a 0.7 sccm BF_3 flow was used. The front as well as the rear TCO were made of ITO. Figure 7.8 shows the measured output characteristics of the cells.

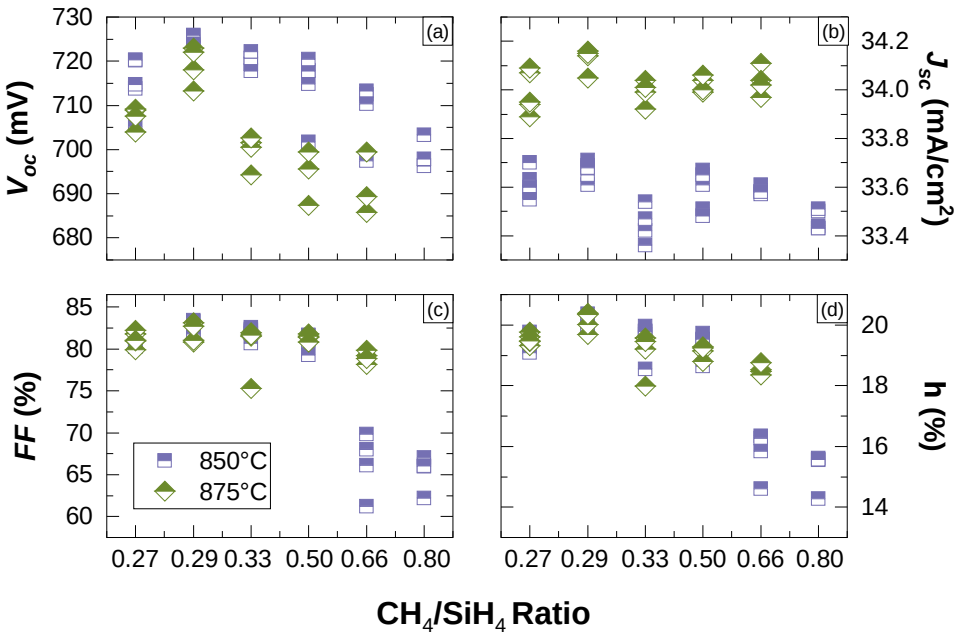

Figure 7.8 – The cell parameters extracted from one-sun *J*-*V* characteristic of the both sides-contacted solar cells featuring the same front contact and SiC_x:F(*p*) rear contacts prepared with different CH_4 to SiH_4 ratios — carbon concentrations.

It is observed that there is a clear optimum of the V_{oc} for CH_4/SiH_4 ratio of 0.29, reaching maximum values of 726 and 723 mV for the cells annealed at 850 and 875 °C, respectively. According to Figure 7.8(a) further increase in CH_4/SiH_4 ratio results in a gradual drop which appears to be more drastic for the cells annealed at 875 °C. A similar trend was also presented for the iV_{oc} values measured from the symmetric test structures with SiC_x:F(*p*) contact layer on both sides of the *p*-type c-Si wafer in Chapter 6. Prior to hydrogenation, the measured iV_{oc} values of the cell precursors produced with the ratio of 0.29 was 714 and 706 mV after annealing at 850 and 875 °C, respectively. Following the hydrogenation process, the extracted iV_{oc} values reached to the values of 735 and 733 mV. Overall, the cell annealed at higher temperature benefits more from the hydrogen-induced defect passivation.

The crystalline fraction of the front $SiC_x(n)$ contact layer increases with annealing temperature, accordingly the parasitic absorption of the front layer reduces. Figure 7.8(b) reveals that the cells annealed at 875 °C reach higher J_{sc} values compared to the ones annealed at 850 °C. The maximum J_{sc} difference measured is 0.6 mA/cm^2. Apart from that, the J_{sc} values seem to be not affected by the variation of the carbon concentration of the rear SiC_x:F(p) contact layer. The highest J_{sc} obtained is 34.1 mA/cm^2 which is promising considering the fact that these are planar solar cells with very poor light in-coupling.

In Chapter 6 it was shown that the ρ_c increases with carbon concentration of the SiC_x:F(p). At the cell level, it is observed that the *FF* attains maximum values of 83.4 and 83.2 % after annealing at 850 and 875 °C, respectively for the CH_4/SiH_4 ratio of 0.29 [see Figure 7.8(c)]. With further increase in carbon concentration, *FF* reveals a gradual decrease which can be attributed to the bandgap widening and corresponding increase in band offsets that aggravates the charge-carrier collection. The extracted *iFF* from the effective lifetime curves of the cell precursors before metallization were 86.9 and 86.5 % for the precursors produced with the ratio of 0.29, annealed at 850 and 875 °C, respectively. For higher carbon content related to ratios of 0.66 and 0.80, *FF* degrades severely to values below 70 %. For both annealing temperatures very similar *FF* trends as a function of carbon concentration are obtained.

Overall conversion efficiency trend is mostly dominated by the *FF* as the lower V_{oc} values are compensated by the higher J_{sc} values measured for the cells annealed at 875 °C for 0 min. The highest efficiency is attained with the ratio of 0.29 resulting in 20.4 % for both annealing conditions but with different cell parameters. The cell annealed at 850 °C attains V_{oc} of 726 mV, J_{sc} of 33.7 mA/cm^2 and *FF* of 83.4 % while the cells annealed at 875 °C attains V_{oc} of 718 mV, J_{sc} of 34.1 mA/cm^2 and *FF* of 83.2 %. The notably high *FF* values above 83.2 % indicate a reduced series resistance in SiC_x:F(p) rear contact layers with lower carbon concentrations, even though the decrease is little, it appears to be effective.

Annealing temperature

As a final optimization parameter the influence of the annealing temperature was investigated in a wide range by altering the annealing temperature from 825 to 900 °C. To obtain better statistics, the same experiment was performed for two different doping concentrations, BF_3 flow of 0.7 and 0.9 sccm. The CH_4/SiH_4 ratio of 0.29 was used for the cells produced for this experiment. Figure 7.9(a–d) reveals the output characteristics of the both-sides-contacted planar *p*-type cells as a function of the annealing temperature.

Figure 7.8(a) shows that the highest V_{oc} of 727 mV is reached with the sample featuring a SiC_x:F(p) layer prepared using a BF_3 flow of 0.7 sccm and annealing at 850 °C. Before metallization, the cell precursor reveals a good iV_{oc} of 717 mV before hydrogenation and 739 mV after hydrogenation. With a further increase in annealing temperature, the V_{oc} decreases in agreement with the iV_{oc} trends presented in Figure 7.2 in this chapter for front $SiC_x(n)$ contacts and Figure 6.11 in Chapter 6 for SiC_x:F(p) rear contacts. The observed drop in V_{oc} at the device

level is originated probably from the structural disruption of the chemical SiO_x — or even pinhole formation — due to the thermal treatment at high temperatures and increased local dopant in-diffusion that enhances the Auger recombination.

Similar to the observation in the previous section, also here J_{sc} is increasing with annealing temperature due to the enhanced crystallinity and hence transparency of the front $SiC_x(n)$ layers. However it is seen that in this run the related enhancement is less pronounced. A possible reason for this discrepancy might be process related fluctuations and slightly different ITO properties. For the cells featuring the same rear contact layer after annealing at 850 °C, the best J_{sc} value obtained was 33.7 mA/cm^2 in the previous section, whereas here it is measured as 33.5 mA/cm^2, which indicates the fact that the front ITO was slightly less transparent or simply thicker.

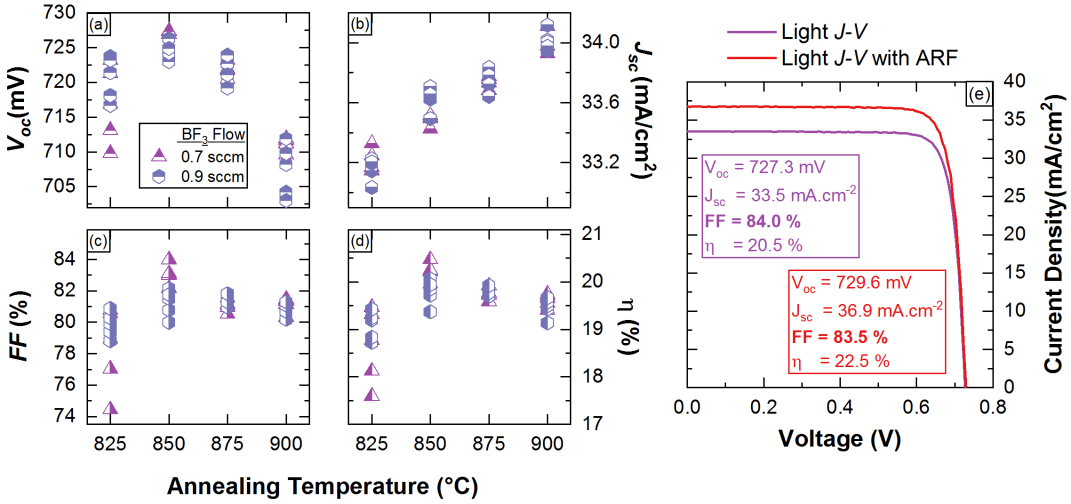

Figure 7.9 – (a–d) The measured cell parameters of the both-sides-contacted planar cells annealed at different temperatures for two different BF_3 flow of 0.7 and 0.9 sccm.(e) The *J-V* characteristics of the best cell measured with and without microtextured anti-reflective foil.

The trend of *FF* is depicted in Figure 7.9(c). After annealing at 825 °C, the cells reveal the lowest *FF* values for both doping concentrations. With increasing annealing temperature, the *FF* optimum is observed at 850 °C, higher temperatures appear to result in a slight degradation. The cell produced with BF_3 flow of 0.7 sccm attains to a remarkable value of 84 %. A possible reason can be slightly higher ITO conductivity mentioned already in the discussion of the difference in J_{sc} between Figure 7.8 and 7.9. By comparing the *J-V* curves from suns-V_{oc} and light *J-V* measurement R_s is extracted as 0.6 Ω cm^2.

The final conversion efficiencies of the cell show an optimum of V_{oc} and *FF* after annealing at 850 °C. The cell featuring the rear SiC_x:F(p) produced with BF_3 flow of 0.7 sccm yields an efficiency of 20.5 % after annealing at 850 °C, its *J-V* characteristic is shown in Figure 7.9(e) by the purple curve. The same cell was also measured by applying a microtextured anti-reflective

foil at the front to attenuate the interference pattern, and thus to determine the full efficiency potential [Escarré 2012], [Ulbrich 2013]. With minimized front reflection, the J_{sc} improvement up to 36.9 mA/cm^2 is observed. Correspondingly the V_{oc} increases by 2.3 mV and the *FF* reveals 0.6 % relative loss due to the increased resistive losses; overall device performance attains to conversion efficiency of 22.5 %.

7.4.4 Application of IO:Zr as front TCO

To replace ITO with another TCO featuring better electrical and optical properties, IO:Zr has been tested on device level as a front TCO. In the experiment, both sides-contacted planar *p*-type solar cells featuring a $SiC_x(n)$ front contact and a SiC_x:F(*p*) rear contact produced with BF_3 flow of 0.7 sccm and CH_4/SiH_4 ratio of 0.29 were used. The cells were annealed at 850 °C for 0 min. As rear TCO, 100-nm-thick ITO was applied while as front TCO, IO:Zr with different oxygen concentrations were sputtered[4].

The TCO development is done in a small lab-scale sputtering tool. During the development, a reference glass sample was placed at the center of the substrate holder and the oxygen flow was varied from 0.5 to 1.6 sccm, aiming to find the optimum deposition conditions for front side applications. The obtained electrical parameters are listed in Table 7.2 for 100-nm-thick layers. In the *as-deposited* state IO:Zr exhibits only an amorphous phase, yet after annealing at 200 °C it shows large crystals that leads to high mobility values above 100 cm^3/Vs. More detailed information about IO:Zr layer can be found in [Rucavado 2018]

Table 7.2 – Summary of the IO:Zr property with oxygen flow after annealing at 200 °C on hot plate under air ambient. The values marked with asterisk were measured from the reference glass samples deposited with cells but place at the edge of the sample holder.

Oxygen flow [sccm]	**Thickness [nm]**	**Mobility [cm^2/Vs]**	**Free-carrier density [cm^{-3}]**
0.5	100 / 83*	75 / 60.5*	4.1×10^{20} / 2.9×10^{20}*
1.1	100 / 85*	105 / 66.8*	2.5×10^{20} / 2.1×10^{20}*
1.6	100 / 85*	100 / 48.3*	1.5×10^{20} / 1.3×10^{20}*

During the TCO deposition on the cells, a reference glass sample was placed at the edge of the substrate holder. The measured electrical parameters for the reference samples are given in Table 7.2 and marked with asterisk. The target thickness was 85 nm for front side. It was also observed that the electrical properties of the IO:Zr films depend strongly on the substrate position during the deposition, accordingly the measured mobilities are slightly lower for the reference samples as they were place to edge as well as they were slightly thinner.

Figure 7.10 shows the output characteristics of the cells featuring the front IO:Zr with different oxygen content. The extracted iV_{oc} and *iFF* values from the minority-carrier lifetime curves

[4]The development and deposition of the IO:Zr layers were done by E. Rucavado. Contribution is gratefully acknowledged.

of the cell precursor before metallization are indicated with green stars in panel (a) and (c). The solar cell precursors reveal iV_{oc} values between 739 and 740 mV. It is observed that the difference between iV_{oc} before metallization and final V_{oc} does not change significantly with oxygen content.

For the cell produced with lower oxygen flow, the obtained J_{sc} values are fairly comparable with the cells produced by employing ITO as a front TCO. According to Figure 7.10(b), with increasing the oxygen flow during the sputtering process the J_{sc} exhibits drastic improvement, resulting in values above 34.4 mA/cm^2. The reason of this improvement is a reduction in free-carrier absorption in the spectral range of 600 nm to 1000 nm — EQE, R and IQE were measured but not shown here. The gain is not originated from the spectral response in the blue part due to the fact that the applied layer thickness was 85 nm for IO:Zr and 60 nm for ITO. It is important to note that this is the highest current value obtained in the scope on this thesis for planar cells without double anti-reflective coating. The value above 34.4 mA/cm^2 can be classified as a promising value for planar solar cells, especially compared with an upper limit of 36.5 mA/cm^2 simulated with Wafer ray tracer [Lighthouse] for an ideal planar device using nitride/c-Si wafer/nitride/Ag on a 200-μm-thick c-Si wafer including 3 % shading losses.

We note that more transparent IO:Zr layers obtained by increasing the oxygen content does

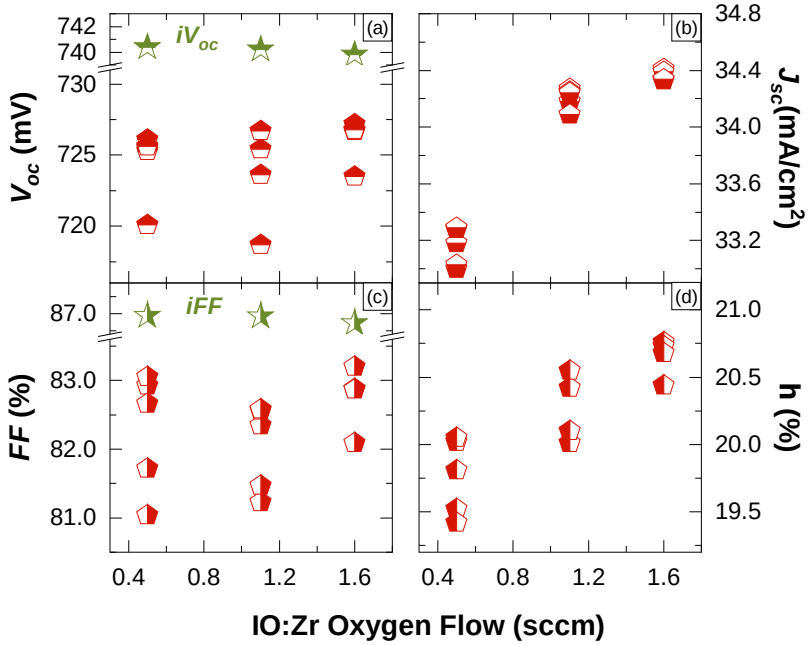

Figure 7.10 – The extracted cell parameters from one-sun J-V characteristic for the cells prepared by varying the oxygen concentration of the front IO:Zr. Measured implied values before metallization are indicated with stars.

not come at the expense of reduced *FF* as seen in Figure 7.10(c). Before metallization the extracted *iFF* values are around 86.7–86.9 %. It appears the best *FF* of 83.2 % is obtained with the cell featuring IO:Zr layer produced with the oxygen flow of 1.6 sccm. However a clear conclusion cannot be drawn since the *FF*s of the cells exhibit some fluctuation, probably due to the inhomogeneous IO:Zr deposition throughout the 4-inch c-Si wafer as it is mentioned before.

The conversion efficiency of the cells exhibits an increasing trend with oxygen content of the front IO:Zr [see Figure 7.10(d)]. The best cell reaches to the efficiency value of 20.8 % with V_{oc} of 727 mV, J_{sc} of 34.4 mA/cm^2 and *FF* of 83.2 %. To the best of our knowledge, this value is one of the highest conversion efficiency obtained with planar *p*-type c-Si solar cells without double anti-reflective coating.

7.4.5 Dark diode losses

Previously, it was mentioned that the impact of TCO deposition is only partially responsible for the V_{oc} losses. To assess the other reasons for the observed difference between iV_{oc} before metallization and the final V_{oc}, a more detailed analysis was performed during the fabrication process of the planar solar cells. To that end the illumination level dependence of the implied- and pseudo-V_{oc} values were monitored after each step of the process. The suns-V_{oc} measurement was performed with and without black-mask (2 cm × 2 cm). In parallel to that, the photoluminescence-images (PLIs) were recorded in order to visually monitor the surface passivation damage and recovery.

Figure 7.11(a) reveals the illumination-dependent V_{oc} curves at different process steps. The measured iV_{oc} from the cell precursor before metallization is 738 mV, the corresponding PLI is depicted in Figure 7.11(b). After ITO deposition the iV_{oc} drops to 710 mV, the degradation of the surface passivation is clearly visible in corresponding PLI [see Figure 7.11(c)]. Following the screen printing of the front silver grids and curing, the planar *p*-type cell reaches a V_{oc} of 726 mV and *FF* of 82.8 %. The 16 mV recovery of V_{oc} is also empirically visible in the corresponding PLI in Figure 7.11(d). By measuring the suns-V_{oc}, the pseduo-V_{oc} values are determined as 728 and 733 mV with and without masking the cells, respectively. This difference in the pseduo-V_{oc} values clearly indicates a contribution of a dark diode which is related to the fact that both passivating contacts are deposited on the full wafer area whereas the active cell area is defined by sputtering the TCO through a 2.2 cm × 2.2 cm shadow mask. Normally, a 2 cm × 2 cm black mask is used during the *J*-*V* measurements, resulting in a dark diode that is in parallel with the illuminated cell area.

The loss related with the dark diode formation is determined to be > 5 mV on pseudo-V_{oc} and > 0.4 % on the pseudo-*FF*. As it was reported in previous sections, a loss of ~ 4 to 5 mV originates from TCO deposition. Since there is a difference of ~ 10 mV between iV_{oc} before metallization and final V_{oc}, a loss of 2 to 3 mV in V_{oc} is still undetermined.

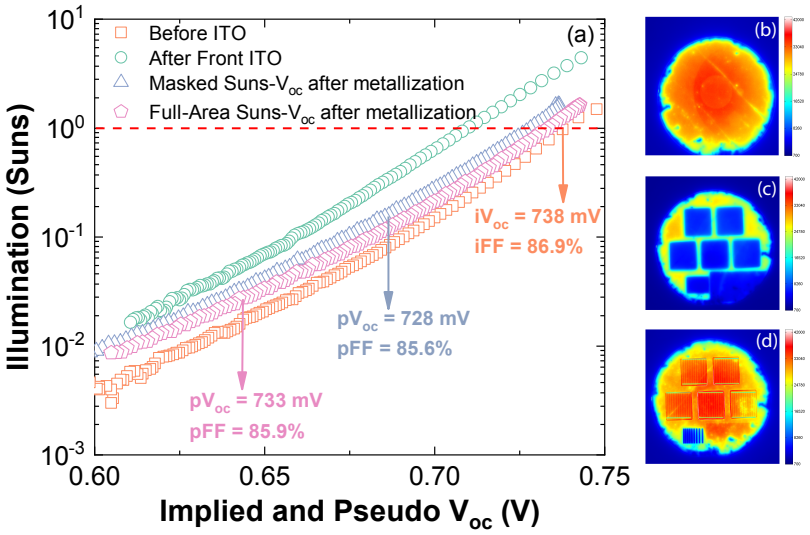

Figure 7.11 – (a) Illumination level dependence of the implied and pseudo voltages measured at different steps during the cell fabrication. Photoluminescence images (b) before metallization, (c) after metallization and (d) after curing for front screen-printed Ag paste.

7.5 Results and discussion II: Cells with textured front and planar rear

Following the verification of the excellent surface passivation and charge-carrier extraction achieved with planar cells, the front contact was further transferred to textured surfaces to improve the light in-coupling and to overcome the efficiency limitation originated from J_{sc}.

It is essential to note that transferring the *p*-type contact layer to textured surfaces is more challenging as it suffers more from the difference in the c-Si/SiO_x recombination velocity for <111> and <100> surface orientation. The MOSFET community reported that the interface trap state density at SiO_2/c-Si <111> is about five to ten times higher than that at SiO_2/c-Si <100> [Cooper 1974], [Schulz 1983], [Kato 2006]. Additionally, oxide growth rate might differ with the surface orientation leading to a non-uniform pyramid coverage as textured surfaces are composed of <111> planes and <110> edges [Barycka 1995]. Owing to these challenges, no report about the successful transfer of the hole-selective contacts to textured surfaces is published in literature yet. Larionova *et al.* reported 700 mV for the thermally grown SiO_x capped with ion-implanted *p*-type poly-Si after an additional hydrogenation with SiN_x [Larionova 2017]. However, they did not comment on the contact resistivity values in their publication, thus the selectivity of the presented structure is questionable.

To that end, 200-μm-thick front-side-textured, rear-side-planar *p*-type c-Si wafers with 2 Ω cm resistivity were used for solar cell fabrication. UV-O_3 oxide was grown by exposing both sides

of the wafers to UV radiation of a Hg lamp for 2 min which leads to an oxide thickness of ~1.2 nm. The deposition time for $SiC_x(n)$ front layer was increased to obtain 15-nm-thick layer on textured surface. Following the SiC_x:F(p) rear contact deposition, the samples were annealed at 850 °C for 0 min and subsequently hydrogenated with SiN_x overlayer performing hot-plate annealing at 450 °C for 30 min. Immediately before the TCO deposition, the cell precursors were dipped in 5 % diluted HF to remove the SiN_x layer as well as the potential native SiO_x that might be grown on the surface of the contacts during the thermal treatment.

7.5.1 Solar cells with different TCOs

A preliminary test performed by applying standard ITO as front and rear TCO to the front-side-textured cell precursor. The obtained parameters with this cell are indicated in Figure 7.12 with pink stars. The best cell attains to a V_{oc} of 718 mV, a J_{sc} of 38.03 mA/cm^2, a *FF* of 79.7 % and an efficiency of 21.8 %. As one of the efficiency-limiting parameters for this cell appears to be J_{sc} due to high parasitic absorption in the ITO and $SiC_x(n)$, the ITO is replaced with IO:Zr to reduce optical losses, in a first experiment only for the front side of the cells. Additionally to investigate the potential J_{sc} improvement by minimizing the parasitic absorption of the front $SiC_x(n)$ layer, its thickness is reduced to 10 nm — indicated with purple triangles in Figure 7.12.

Here we compare the cells with different $SiC_x(n)$ front layer thickness featuring the same IO:Zr front and ITO rear TCOs. Before metallization the iV_{oc} - *iFF* values were extracted from lifetime curves using an optical factor of 0.9 as 729 mV – 85.4 % for the cell with standard $SiC_x(n)$ front and 722 mV – 86.2 % for thin $SiC_x(n)$ front layer. Following that the IO:Zr front and ITO rear TCOs were sputtered on the cell precursors. It is observed that in the case of using 10-nm-thick $SiC_x(n)$, the V_{oc} reaches to 704 mV while for the standard 15-nm-thick $SiC_x(n)$ layer V_{oc} is around 714 mV. A possible interpretation can be that by thinning down the doped layer, the reservoir of dopant atoms in the layer decreases, leading to insufficient dopant diffusion. It is also seen that the difference between iV_{oc} before metallization and final V_{oc} is slightly higher for thinner $SiC_x(n)$ front — 18 mV for thin $SiC_x(n)$, 16 mV for standard $SiC_x(n)$ —, suggesting that the contact is more prone to degradation during TCO deposition. The dark diode losses are determined to be 6 mV for both cells. Overall, it is observed that the textured surfaces are more sensitive to the damage caused by the TCO deposition.

Figure 7.12(b) reveals a clear J_{sc} improvement with implementing front IO:Zr compared to the cells featuring ITO on both sides. Regarding the impact of $SiC_x(n)$ layer thickness, it is seen that with decreased thickness from 15 to 10 nm, J_{sc} gain up to 0.8 mA/cm^2 can be achieved due to the reduced front parasitic absorption. This observation indicates a clear trade–off in between V_{oc} and J_{sc}, thinning down the SiC_x front layer leads to higher J_{sc} values, on the other hand it causes a significant loss in V_{oc}. Thus, the cells end up at the similar efficiencies.

Impressively high mobility values were already reported for IO:Zr in Table 7.2, therefore it is expected that its superior electrical transport properties would be translated in to high

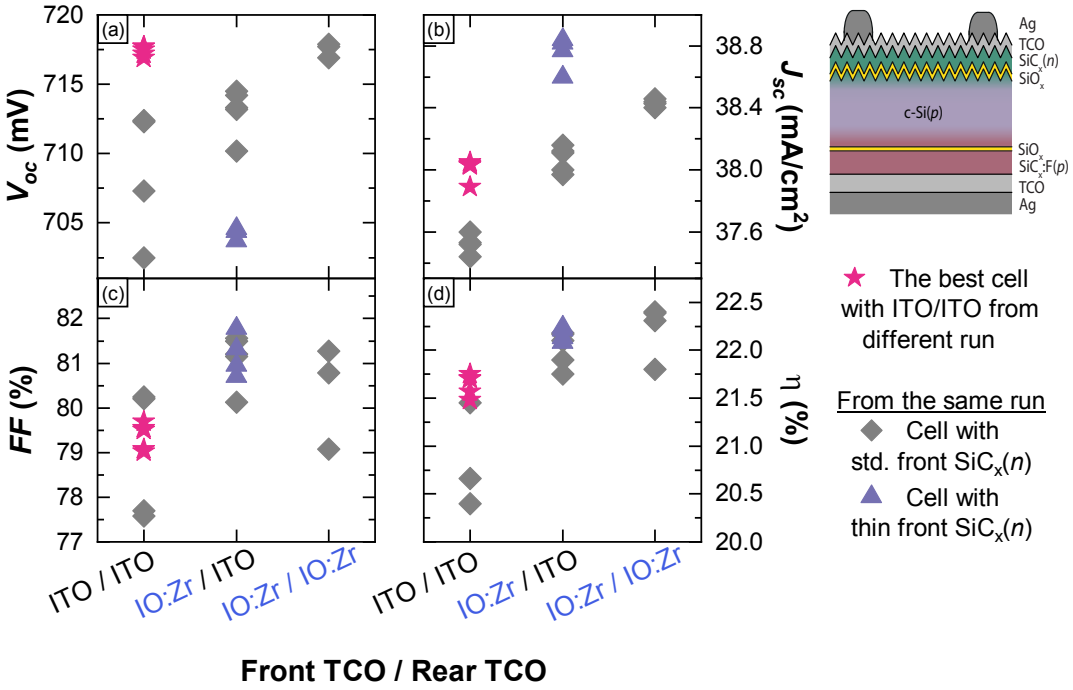

Figure 7.12 – Cell characteristics of the both-sides-contacted, front-side-textured, rear-side-planar cells with various TCOs. Grey and purples symbols are the cells from the same batch employed front $SiC_x(n)$ layer with standard and thinner thicknesses respectively while the pink stars are the best ITO/ITO cell from different run.

FF values at the device level. Compared to the cells with ITO on both sides, the *FF* values reveal improvement with IO:Zr. The best *FF* of 81.8 % is reached with the cell featuring thin $SiC_x(n)$ front layer. The measured pseudo *FF* from suns-V_{oc} is 83.8 % and the calculated dark diode loss is around 0.8 %. The reason of the lower *FF* values of these cells compared to fully planar cells presented in previous sections might be related with the UV-O_3 oxide which is supposed to be denser with respect to chemical SiO_x. Consequently, less efficient carrier transport manifests itself with low *FF*. We note that here all the optimizations were performed with chemical SiO_x thereby observed *FF* limitation in front-side-textured cells with UV-O_3 oxide can be probably overcome by simply increasing the annealing temperature or annealing dwell time or doping concentration of the SiC_x layers.

Figure 7.12 shows that the application of IO:Zr is beneficial for both electrical and optical performance of the front-side-textured *p*-type solar cells. The most pronounced effect is observed for the J_{sc}, thanks to the higher optical transparency of IO:Zr compared to ITO. After replacing the front and rear ITO with IO:Zr, a conversion efficiency of 22.4 % is achieved with V_{oc} of 717 mV, *FF* of 81.3 % and J_{sc} of 38.4 mA/cm^2.

7.5.2 The impact of magnesium fluoride as anti-reflective coating

With the intention of minimizing the reflection, selected front-side-textured *p*-type solar cells were subjected to second anti-reflective layer of 85-nm-thick thermally evaporated MgF_2.

Table 7.3 – Summary of the parameters for the both-sides-contacted front-side-textured *p*-type solar cells with MgF_2 double anti-reflective coating (ARC).

Cell	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	Efficiency [%]
Standard front $SiC_x(n)$	719.0	38.3	80.9	22.3
After MgF_2	719.6	38.8	80.9	22.6
Thin front $SiC_x(n)$	704.6	38.6	81.8	22.2
After MgF_2	704.7	39.2	81.7	22.6

The obtained cell parameters before and after the MgF_2 deposition are summarized in Table 7.3. Comparison of the J_{sc} values indicates a gain of 0.5–0.6 mA/cm^2 due to the second ARC. The highest J_{sc} achieved is 39.2 mA/cm^2 with the cell featuring 10-nm-thick $SiC_x(n)$ front layer, IO:Zr as a front TCO and ITO as a rear TCO. In combination with the V_{oc} of 704.7 mV and the *FF* of 81.7 %, this cell yields a conversion efficiency of 22.6 %. The cell with standard 15-nm-thick $SiC_x(n)$ front layer, IO:Zr as front and rear TCOs also attains to 22.6 % with V_{oc} of 719.6 mV, *FF* of 80.9 % and J_{sc} of 38.8 mA/cm^2.

7.6 Conclusion

In this chapter, first an electron-selective passivating front contact based on $SiO_x/SiC_x(n)$ was developed to be co-processed with the SiC_x:F(p) hole-selective rear contact. For the SiC_x:F(p), an iV_{oc} of 735 mV was reached after annealing at 850 °C (presented in Chapter 6). With the $SiC_x(n)$ exposed to the same thermal process as the SiC_x:F(p), an impressively high iV_{oc} value of 746 mV is demonstrated.

The impact of various TCO depositions on the surface passivation was investigated extensively with symmetric test structures using *p*-type c-Si wafers. Following the TCO deposition, a drastic drop in effective lifetimes and partial recovery after curing at 250 °C are found for both contacts. It is observed that the SiC_x contact reveals a strong tailing at low injection when the lifetime curves are measured with a TCO overlayer, whereas it disappears when the measurements are performed after stripping off the TCO. Overall, for both $SiC_x(n)$ front and SiC_x:F(p) rear contacts, ~ 4–5 mV loss in iV_{oc} is monitored due to the TCO deposition.

Several process parameters of the SiC_x:F(p) rear contact were varied to determine their influence at the device level. The optimum BF_3 flow and CH_4/SiH_4 ratio are defined to be 0.7 sccm and 0.29, respectively. Both-sides-contacted planar *p*-type solar cells, featuring a full-area SiC_x:F(p) rear and $SiC_x(n)$ front contact, co-processed in a single annealing step and

coated with ITO, yield an excellent *FF* of 84 % and V_{oc} of 727 mV. A *FF* of 84 % reveals the great potential of the approach presented here.

The $SiC_x(n)$ front contact was subsequently transferred to textured surfaces. With front-side-textured cells, efficiencies of 21.8 % were reached using ITO. Replacing the ITO with IO:Zr decreases optical and transport losses resulting in efficiencies of up to 22.4 % on textured *p*-type wafers with a simple process flow. By applying a MgF_2 ARC to further reduce the reflection losses, a conversion efficiency of 22.6 % is attained. It is important to note that as the presented cells are screen printed, they can naturally be made bi-facial and all the advanced metallization technologies such as multi-wire interconnection or multi-busbar can be applied. Thus the proposed cell architecture yields promising conversion efficiencies with room for improvement and exhibits good potential for industrialization.

8 Summary and perspectives

This chapter addresses the main results achieved during this thesis and draws a roadmap for future development. First, the conclusions reported in the previous chapters are summarized. Then, the general perspectives that aim at further improvement of the conversion efficiencies using passivating contacts as well as the possible cell integration strategies for industrialization are discussed.

8.1 Summary

In this thesis, carrier-selective passivating contacts with low and high thermal budgets were investigated for high-efficiency c-Si solar cells.

The study was initiated using the well-established SHJ technology, as it is accepted to be a prime example of the application of passivating contacts. The target of the work was to improve both the optical and electrical performance of SHJ solar cells using passivating contacts with a low thermal budget. To that end, doped a-Si:H was replaced by μc-Si:H as the carrier-selective contact layer. In Chapter 3, it was shown that employing μc-Si:H layers is one way to decrease the ρ_c values due to the presence of crystalline phases with high doping efficiency. However, the thickness of the layer should be above a certain threshold value ($\sim$ 9 nm) as the nanocrystal growth evolves in a conical shape with an increasing nanocrystalline grain diameter as a function of thickness, therefore total crystallinity improves with thickness. With temperature-dependent measurements, it was shown that the thermionic component of charge-carrier transport as well as the Schottky barrier effect at the interface of the doped layer and the TCO can be reduced with μc-Si:H layers. Additionally, it was demonstrated that the optical performance of SHJ devices can be improved with μc-Si:H layers, and consequently a J_{sc} gain of up to 1.5 mA/cm^2 can be obtained due to their low absorption coefficients over the visible range. However at this stage we encountered two opposing trends. On the one hand, the layer thickness should be kept as thin as possible since light absorbed in the doped layer does not contribute to the photocurrent. On the other hand, if the layer is too thin, it does not contain enough active dopants to build up the electrostatic potential of the junction.

Table 8.1 – Performance summary of the realized solar cells in this thesis.

Front- / Rear- Contacts		Cell Parameters			
Contact Layers	**Thermal Budgets**	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	η [%]
a-Si:H(*p*) / a-Si:H(*n*)	low / low	717.0	36.9	78.1	20.7
MoO_x / μc-Si:H(*n*)	low / low	725.0	38.9	80.0	22.5
a-Si:H(*n*) / SiC_x(*p*)	low / high	707.0	38.6	81.8	22.3
SiC_x(*n*) / SiC_x:F(*p*)	high / high	704.7	39.2	81.7	22.6
SiC_x(*n*) / SiC_x:F(*p*)*	high / high	727.3	33.5	84.0	20.5

* Both-sides-planar cell

To overcome this limitation we fabricated Cu-plated SHJ cells featuring a highly transparent MoO_x hole-selective front contact and a μc-Si:H(*n*) electron-selective rear contact. With this approach, an increased front transparency and a reduced contact resistivity were observed. In Table 8.1 the evolution of the realized cell performances in the scope of this thesis is shown. Compared to our *n*-type SHJ cell with amorphous doped layers, a notable gain in *FF* from 78.1 to 80.0 % was demonstrated mainly due to reduced ρ_c values.

Chapter 4 was devoted to the development of hole-selective passivating contacts that are more tolerant to high-temperature processes, i.e. high-thermal-budget contacts. The motivation was manifold but the focus was mainly to improve the *FF* beyond the values obtained using contact structures with a low thermal budget and to propose alternative rear contacts to industrial PERC solar cells. The contact structure consists of a chemically grown SiO_x and *in-situ* doped SiC_x(*p*) layer prepared in a PECVD tool on *p*-type c-Si wafers. This was then followed by a thermal treatment at temperatures between 800 and 900 °C to *activate* the contacts. Hydrogen that passivates the interface defects effuses out from the sample at these temperatures, and it was shown that atomic re-hydrogenation is crucial to obtain good surface passivation, as it effectively terminates the dangling bonds formed at the SiO_x/c-Si interface. By performing structural characterization, it was demonstrated that a carbon-free Si(i) inter–layer is needed to prevent a chemical reaction between carbon atoms in the SiC_x(*p*) layer and the adjacent SiO_x. The optimum inter–layer thickness was found to be related to the carbon concentration of the SiC_x(*p*) layer. In Chapter 5 it was shown that with increasing carbon concentration the necessary optimum thickness to obtain good surface passivation increases. With that approach, very promising iV_{oc} values of up to 718 mV (J_0 of 11.5 fA/cm^2) were obtained. Strikingly, rather low contact resistivity values below 20 mΩ cm^2 were attained compared to standard SHJ hole-selective contacts with a low thermal budget; for a-Si:H(*p*), ρ_{c-a} values around 1 Ω cm^2, and for μc-Si:H(*p*), $\rho_{c-\mu c}$ values around 0.4 Ω cm^2 were found in Chapter 3. In light of investigations performed with C-AFM and TEM on the microstructural evolution of the contact upon annealing, the working principle of the contact structure was discussed and tentatively explained in the final part of the Chapter 4.

Motivated by the low ρ_c values obtained with the high-thermal-budget hole contact, we investigated its potential at the device level in Chapter 5. To that end, a hybrid cell concept was proposed. The hybrid cells featured the developed rear hole contact and a standard SHJ front contact made of an a-Si:H(*i*) passivation layer and an a-Si:H(*n*) electron contact layer with a low thermal budget. The use of a heterojunction front contact was motivated by the fact that a-Si:H(*i*) provides quasi-perfect chemical passivation, and the V_{oc} of the cells would be limited by the rear contact. This gives an opportunity to determine the possible V_{oc} gain that can be achieved by integrating our contact into industrial *p*-type solar cells. With the hybrid solar cell concept, the potential of our high-thermal-budget hole contact based on a chemical SiO_x/Si(i) inter–layer /SiC_x(*p*) was demonstrated. By realizing systematic variations at the rear contact, clear trends in cell parameters were observed, which were then used to determine its working principle. After optimizing the process flow and the rear contact structure at the cell level, this hybrid approach merging low and high thermal budgets resulted in a conversion efficiency of 22.3 % and *FF* of 81.8 % on *p*-type wafers [see Table 8.1]. Hence, the low ρ_c values compared to standard heterojunction contacts manifested themselves with improved *FF* far beyond 80 % to almost 82 %. Nevertheless, the measured *FF* was most likely still limited by the standard SHJ front contact, whose specific contact resistivity was measured as 200 mΩ cm^2, c.f. Chapter 3 section 3.4.

In Chapter 6, the impact of fluorine incorporation into boron-doped passivating hole contacts was explored. To that end, the dopant precursor TMB was replaced by the fluorinated boron dopant source BF_3 during the PECVD process. It has been shown that the fluorine accumulates at the SiC_x:F(*p*)/SiO_x and SiO_x/c-Si(*p*) interfaces and reduces the interface defect states by terminating the dangling bonds. The fluorine accumulation was resolved clearly in both STEM and SIMS measurements while its function of terminating dangling bonds was interpreted by the obtained iV_{oc} values of > 720 mV (J_0< 10 fA/cm^2) already without substantial hydrogenation. By applying atomic hydrogenation, an iV_{oc} value of 735 mV (J_0 of 4.9 fA/cm^2) was attained with samples annealed at 850 °C. To the best of our knowledge, these values are the best reported values for hole-selective contacts produced with *in-situ* doped PECVD layers on *p*-type c-Si wafers. Additionally, it was shown that fluorinated contacts do not require a Si(i) inter–layer between the SiO_x and SiC_x:F(*p*), as the surface passivation is already sufficient without it. One possible interpretation is that fluorine may compensate simultaneously for the negative impact of the carbon on the chemical SiO_x, which was discussed in Chapters 4 and 5. Additionally, the structural and chemical changes of the thin SiO_x after the different thermal treatments were assessed with STEM coupled with EDX and EELS. It was shown that the chemistry of the thin SiO_x does not change significantly upon annealing if the SiO_x does not rupture. If it does rupture, the overall crystallinity increases in the region where the SiO_x breaks up, and pinholes form.

Finally in Chapter 7, the potential of the developed fluorinated hole contact was investigated at the device level. To avoid possible *FF* limitations that may originate from a SHJ contact, both-sides-contacted co-processed solar cells with high-thermal-budget contacts were fabricated instead of the hybrid concept. For this purpose, *in-situ* phosphorous-doped SiC_x(*n*) layers

were developed for use as a front contact. To have a lean fabrication process, the front contact was developed for co-annealing with the SiC_x:F(*p*) contact whose optimum thermal treatment was found in Chapter 6 to be 850 °C. For this condition, symmetric SiC_x(*n*) reference samples reached an iV_{oc} value of 746 mV with a corresponding J_0 of 4.2 fA/cm^2. Subsequently, full-area SiC_x:F(*p*) rear contacts and SiC_x(*n*) front contacts were co-processed with a single annealing step on planar *p*-type c-Si wafers. The best planar cell attained an impressive *FF* of 84 % and a V_{oc} of 727 mV [see Table 8.1]. This *FF* value confirmed that using high-thermal-budget contacts with low contact resistivities is key to ensure efficient charge-carrier collection from c-Si solar cells. We note that this *FF* is among the highest values reported with c-Si solar cells. Moreover, it was shown that employing IO:Zr instead of ITO as the front TCO provides a gain in J_{sc} without causing any significant drop in *FF*, as it exhibits both high mobility and transparency. With the purpose of increasing the conversion efficiency further, the SiC_x(*n*) front layer was adapted to textured surfaces by replacing the chemical SiO_x with UV-O_3 SiO_x. After replacing the ITO with IO:Zr, efficiencies of up to 22.4 % were achieved on single-side-textured *p*-type wafers with a patterning-free simple process flow. By applying an additional MgF_2 anti-reflective coating to further reduce the front reflection losses, a conversion efficiency of 22.6 % was demonstrated. Even though it is a promising efficiency, there is still a strong potential to improve it further by optimizing the contact structure on UV-O_3 oxide as it is the main reason for lower *FF* values on the textured surfaces.

8.2 Perspectives

Upgrade of standard cell architectures

Figure 8.1 shows a general perspective about the evolution of industrial c-Si solar cell technologies. Today, the Al-BSF technology still dominates the PV market, but industrial PERC concepts are emerging faster than expected. They lead to improved conversion efficiencies thanks to the reduced metal/semiconductor area at the rear; however, the recombination losses at the rear of the PERC concept are still a limiting factor. Therefore it is crucial to propose novel concepts to cell manufacturers that have integration possibility without the need for radical changes in the production lines. Under these circumstances, application of our passivating contacts is an option to increase the conversion efficiency of industrial c-Si solar cells beyond the PERC concept while requiring few upgrades to existing production lines.

In light of the developments presented in this thesis, our short-term perspective is to provide an upgrade to the rear side of industrial PERC solar cells. The upcoming solar cell design may employ a front homo-junction fabricated by phosphorous diffusion, but the conventional V_{oc}-limiting rear contact should be replaced by a full-area passivating contact with a high thermal budget. For this purpose, the hole-selective passivating contacts presented in this thesis show great potential, as their processing temperatures are compatible with those employed for diffusion and drive-in of phosphorous front junctions. However, we note that the necessary duration for drive-in is longer than 30 min at around 850 °C, thereby our TMB-based contact

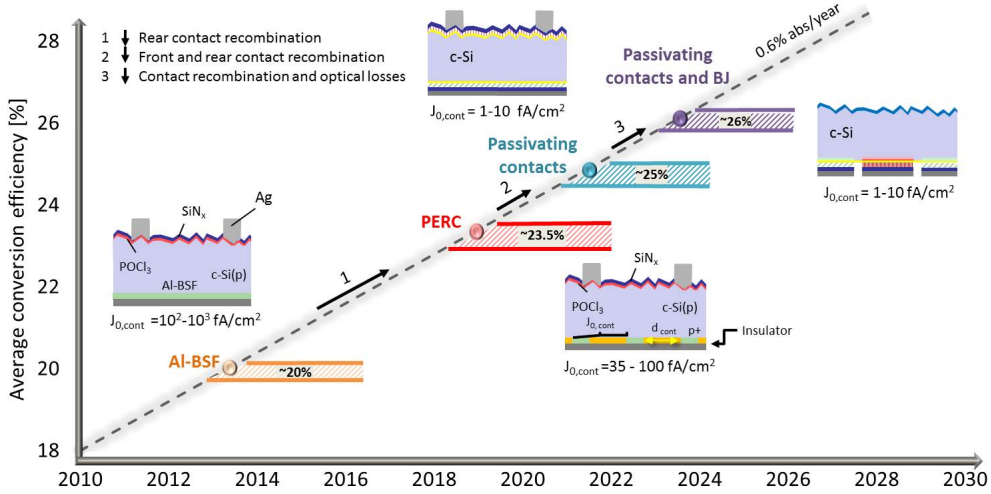

Figure 8.1 – Ultimate prospective evolution of c-Si solar cell technologies as a function of years [Ingenito 2018] Source: M. Hermle, Solar Industry Forum, EU PVSEC 2017

may not be able to show its full potential after such a treatment and it may be necessary to further improve its stability by alloying it with oxygen during PECVD. Alternatively, the BF_3-based contact is more resilient to higher temperatures and longer dwell times. Thus, it would be a perfect candidate for the rear contact. In terms of manufacturing, our passivating contact requires the growth of a thin SiO_x layer and the deposition of a highly doped layer on the rear side. Formation of SiO_x can be integrated into one of the existing cleaning process, whereas the doped layer requires an additional deposition step by PECVD. Even though the BF_3-based contact shows great performance without hydrogenation, we presume that, after front-contact firing, additional hydrogenation may be necessary. Alternatively, special firing through SiN_x could be designed to compensate for hydrogen effusion during the firing process to avoid this potential problem. Overall, this integration route would add one or two more steps to the existing process flow. Nevertheless, efficiencies above 23 % can be expected realistically with this approach. Additionally, preliminary tests were performed by employing industrial *p*-type CZ wafers as well as *n*-type FZ wafers and very similar performances are obtained.

Roadmap toward efficiency improvement

Our long-term perspective is that the solar cell architecture that combines a front homojunction and a full-area rear passivating contact will eventually be limited by charge-carrier recombination at the front-side metallization. Therefore, new concepts will be needed on a medium timeframe to mitigate these losses. At this stage, we believe that our both-sides-contacted solar cells featuring full-area passivating contacts with a high thermal budget can be proposed as a solution. As demonstrated in this thesis, they can provide excellent surface passivation and charge-carrier transport at the same time. This architecture may also be an

appealing alternative as it places fewer restrictions on back-end processing, and it facilitates the use of indium-free low-cost TCOs. Additionally, both-sides-contacted solar cells can be made bifacial, which is currently gaining an important market share as it reduces the levelized cost of electricity [Kopecek 2018]. To do so, it will be crucial to adapt *p*-type layers to textured surfaces. To that end, alternative interfacial layers and hydrogenation processes should be tested, which was not done in this thesis. One important disadvantage of this kind of architecture is its high front parasitic free-carrier absorption. This problem can be solved by developing highly transparent layers with a versatile PECVD technique either by alloying the layers with oxygen or finding a multilayer stack that can be crystallized strongly upon thermal treatment. Detailed information about this kind of layer can be found in [Stuckelberger 2018]. In our solar cell structure presented here, the J_{sc} is moderate and its improvement should be one of the prime objectives while still following the simple co-processing approach. Here our perspective would be to follow two methods to reduce the front parasitic absorption:

- **Localized passivating contact :** Passivating contacts with improved transparency can probably be achieved by first depositing a very thin, full-area passivating front contact and then locally thickening the region underneath the metal fingers. This can be done by using a hard mask during the PECVD process. The application of this simple and cost-effective *in-situ* patterning technique has already been demonstrated for IBC-SHJ cells in our laboratory [Tomasi 2016a]. Such a masked deposition does not require an additional process step but only a different wafer holder. Hence, it opens the way for a massive simplification of the fabrication process of localized contacts for c-Si solar cells. Surely, in our case it requires additional testing and optimization of the layer properties (i.e. thickness, microstructure, chemical composition, etc.), when the deposition is performed through the hard mask. This approach would allow for high doping below the metallic contacts, ensuring low resistive losses when the TCO is employed, while strongly minimizing parasitic absorption between the front fingers. Consequently, this strategy may permit J_{sc} values similar to homo-junction emitters and thus lead to conversion efficiencies above 24.5 %. Alternatively, only one deposition through the mask can be done for the front side and metallic fingers can be placed over those regions, but in that case a way to locally passivate the remaining front areas must be investigated. Another option to decrease front parasitic absorption could be a slight *etch-back* of the regions in between the fingers after a full process including the metallization.

- **Interdigitated-back-contacted cell design :** The most elegant way of reducing the front parasitic absorption is to simply situate both contact polarities at the rear side of the solar cells in an IBC design. However, the IBC c-Si solar cells based on high-thermal-budget passivating contacts presented thus far have been fabricated using several expensive photolithography steps and multiple thermal treatments. Our vision is to give a simple and cost-effective fabrication process perspective that could eventually be merged with industrial applications. To that end, we use a versatile and high-throughput PECVD technique that allows tremendous process flexibility such as controlling the microstruc-

ture and elemental composition of the layer during the fabrication process. Here, we propose a procedure where the full rear surface is covered with interfacial SiO_x and the two contact polarities are deposited through a hard mask followed by one thermal treatment to form the junctions with different polarities simultaneously. We note that, in this design, some important parameters, such as the size of the electron- and hole-collecting fingers, their separation, etc., must be investigated in great detail [Reichel 2011]. We believe that with this simplified IBC design, efficiencies above 25 % can be achieved.

Advanced integration: Tandem solar cells

Recently perovskite/c-Si tandem solar cells have drawn considerable attention as they are promising candidates for the next generation of silicon photovoltaics. Their charm lies in the fact that they can reach efficiencies above the single-junction limit at low cost.

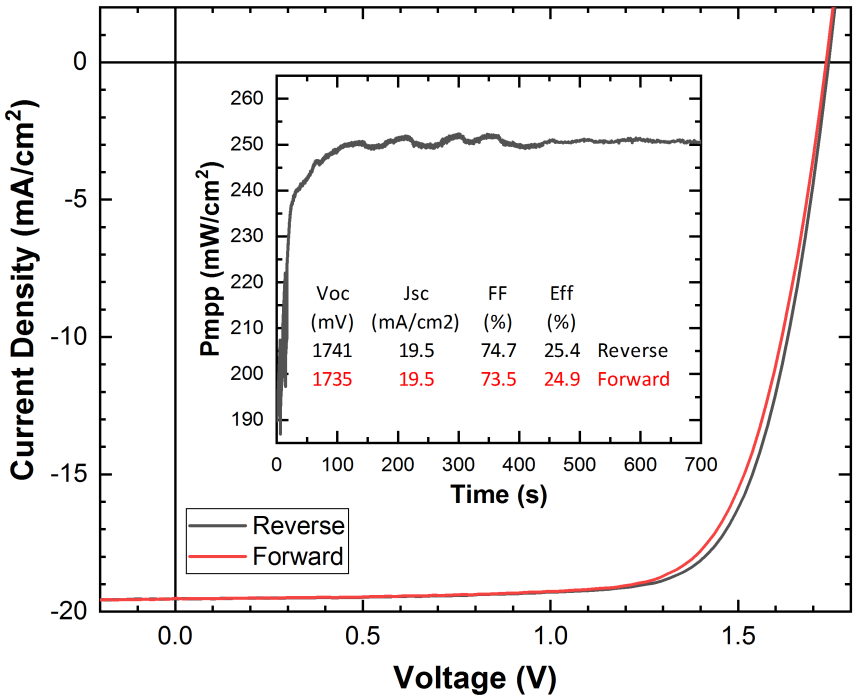

Figure 8.2 – *J-V* characteristic of the perovskite/both-sides-contacted high-thermal-budget cells in the monolithically integrated two-terminal tandem configuration with an aperture area of 1.43 cm^2.

So far, most of the work has focused on using SHJ solar cells as the bottom cell [Werner 2016a], [Bush 2017]. However the ability to employ higher process temperatures could also allow for the use of inorganic perovskites that require higher formation temperatures (i.e. NiO_x, TiO_x, etc.) and bring some flexibility to the perovskite process [Werner 2016b], [Wu 2017]. Motivated by this, the developed both-sides-contacted *p*- type c-Si solar cells featuring passivating contacts with a high thermal budget were also tested as a potential bottom cell in the

monolithically integrated two-terminal tandem configuration. With this design, conversion efficiencies above 25 % were obtained on the first try as shown in Figure 8.2. We believe this result can be further improved by optimizing the perovskite and c-Si cell interface[1]. With perovskite/c-Si tandem solar cells, efficiencies of up to 30 % are feasible.

[1] The detailed information about this work will be given in an upcoming publication by Sahli *et al.*

A Relation between lifetime and implied efficiency

The lifetime is a parameter of overarching importance because it is accessible contact-free and non-destructive through a measurement of the photoconductance. It is measurable already on the bare wafer and it remains measurable throughout almost all of the subsequent processing steps. It is normally called "effective lifetime" because it contains contributions from recombination at defect states in the bulk and at the surface. Focussing on these two effects and neglecting additional limitations due to the Auger effect and radiative recombination which are relevant for very high injection. In the case of well-passivated surfaces ($\tau_{surface} \sim \tau_{bulk}$), the effective lifetime of a symmetric sample can be expressed as follows (eq. 11 in [Richter 2012]):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Bulk}} + \frac{2S_{eff}}{W} \tag{A.1}$$

Here, W is the wafer thickness and S_{eff} is the surface recombination velocity. Symmetric means that both sides of the wafer are covered with the same structure. Whereas such samples would not occur in the final cell process, they are very valuable for characterization. The surface recombination velocity can be distinguished from bulk recombination because it depends on the injection level Δn (eqns. 9 and 10 in [Kane 1985]):

$$S_{eff} = \frac{J_0 \Delta n}{q n_i^2} \tag{A.2}$$

Here, q and n_i^2 are the elementary charge and the intrinsic carrier density, respectively. The formula defines the saturation current density J_0 which is a fundamental parameter to describe the recombination properties of the surface or a contact structure. A saturation current density can also be defined for recombination effects in the bulk of the wafer. Once J_0 is known, the implied open circuit voltage (iV_{oc}) can be estimated with two simple assumptions for the diode quality factor n (e.g. a value of 1.1) and for the short circuit current density J_{sc} of the

final device (e.g. 40 mA/cm^2).

$$iV_{oc} = \frac{nk_BT}{q} ln\left(\frac{J_{sc}}{J_0}\right) \tag{A.3}$$

Here, k_B and T are the Boltzmann constant and the absolute temperature, respectively. Note that the saturation current densities are additive quantities when they have the same exponential relationship between current and voltage, we can express J_0 as $J_0 = J_{0,surf} + J_{0,bulk}$. For cells where the shunt and series resistance are negligible the ideal (FF_0) depends only on the open-circuit voltage divided by nkT/q where kT/q is the thermal voltage and n is the diode ideality factor (eq. 2 in [Green 1982a]):

$$FF_0 = \frac{v_{oc}+1}{1.015v_{oc}+5.7} \qquad v_{oc} = V_{oc}\frac{q}{nk_BT} \tag{A.4}$$

Whereas J_0 describes recombination in very general terms even without contact, the contact resistivity ρ_c requires the connection to an external circuit, ideally for a measurement with the transfer length method (TLM). The contact resistivity acts as series resistivity R_s that will reduce FF_0 to a more realistic value FF_s (Table 1 in [Green 1982a]):

$$FF_s = FF_0\left(1 - 1.1\frac{R_s \cdot J_{sc}}{V_{oc}}\right) + \frac{\left(\frac{R_s \cdot J_{sc}}{V_{oc}}\right)^2}{5.4} \tag{A.5}$$

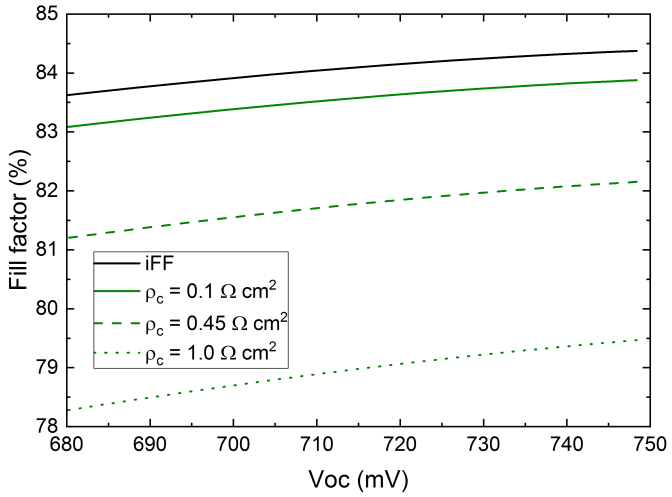

Figure A.1 – Idealized *FF* for contact resistivity ρ_c of zero (black) and for ρ_c values between 0.1 and 1.0 Ω cm^2 (green).

As revealed in Chapter 3, compared to amorphous *p*-type layers that have contact resistivities

in the range of 1.0 Ω cm^2 to 1.5 Ω cm^2 with the ITO front contact, microcrystalline *p*-type layers have contact resistivities between 0.45 Ω cm^2 and 0.5 Ω cm^2. Figure A.1 shows that these seemingly minor differences can have a massive impact on *FF*. For zero contact resistance the so-called implied *FF* depends only on the V_{oc} and varies in a narrow band between 83.5% and 84.5%. For a contact resistivity of 1.0 Ω cm^2, the FF_s is reduced to values between 78% and 79%. Microcystalline *p*-type layers show potential to reach the range between 81% and 82% because of their lower contact resistivities as we also experimentally demonstrated.

Finally, the projection of an upper limit of the efficiency is obtained by multiplying all three cell parameters as follows:

$$\eta = V_{oc} \cdot J_{sc} \cdot FF_s \tag{A.6}$$

Using numerical approximations (Equations A.4 & A.5) for the relation between V_{oc} and *FF* without and with series resistance under the assumption of n is 1.1 and J_{sc} is 40 mA/cm^2, the efficiency contours in Figure A.2 is obtained. Once J_0 and ρ_c of a contact structure are measured, its location on the graph can tell immediately whether a contact strategy will be limited by recombination or resistance and, more importantly for development, where improvements should aim at.

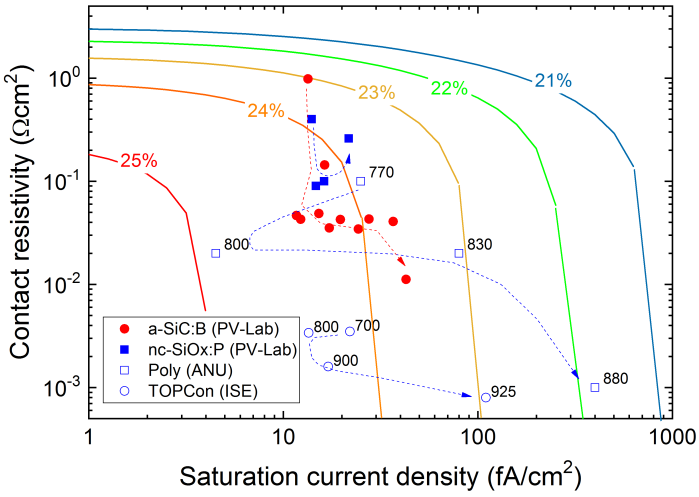

Figure A.2 – Contours of upper efficiency limits related to saturation current and resistance of the contact (full lines). Full squares and circles correspond to *n*- and *p*-type passivating contacts developed at PV-Lab. Open symbols denote literature-data labelled with the given process temperatures. Dashed lines are to guide the eye.

B Structural comparison of low and high thermal budget contacts

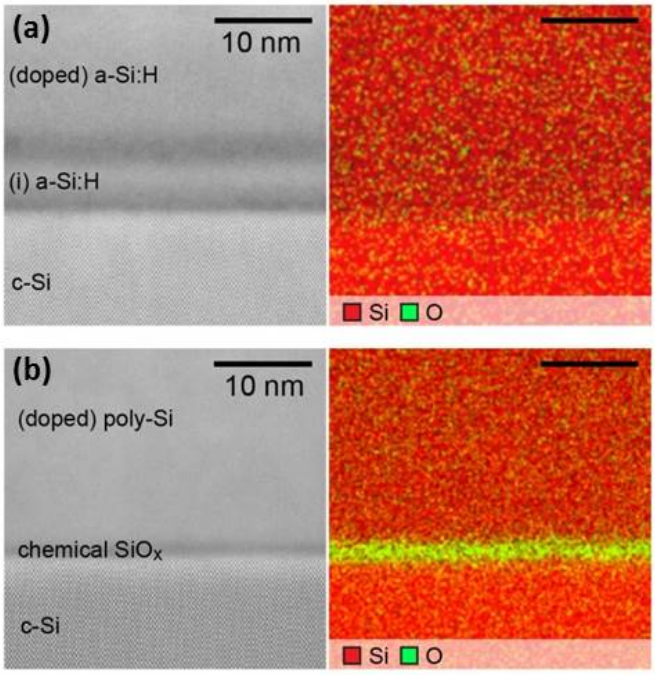

Figure B.1 – STEM-HAADF micrographs with corresponding EDX maps of (a) a low-thermal-budget SHJ contact and (b) a high-thermal-budget contact based on chemical SiO_x and doped-Si layer.

C Replacing chemical oxide with UV ozone oxide

The surface passivation quality of the high-temperature contacts is strongly influenced by the structural properties of the thin SiO_x layer. One alternative to standard wet-chemical SiO_x grown in hot HNO_3 solution, is a dry-grown UV ozone (O_3) oxide (referred as UV-O_3 oxide) which can be produced ultra thin as well. Compared to standard chemical SiO_x, UV-O_3 oxide is environmental friendly, cost effective and preferable in terms of safety. In the literature, it was reported that UV-O_3 oxide shows superior interface characteristics compared to chemical SiO_x as it enables damage-free oxidation and more efficient dangling bond saturation thanks to the more reactive oxygen radicals [Fink 2009], [Khalilov 2012]. Recently, a detailed analysis performed with XPS and TEM measurements evidenced that the stability of the surface passivation strongly depends on the stoichiometry of the SiO_x layer. It was reported that UV-O_3 oxide can tolerate higher thermal treatment temperatures compared to wet chemically grown SiO_x, as the structure of the UV-O_3 oxide is found to be denser, less defective and closer to that of stoichiometric SiO_2 [Moldovan 2014],[Moldovan 2015].

In this work, UV-O_3 oxide was generated by photo-oxidation using a mercury (Hg) vapour lamp with emission lines at 184.9 and 253.7 nm (Jelight, UVO-Cleaner 42). The UV radiation at 184.9 nm dissociates the molecular oxygen of the ambient atmosphere to atomic one by a photochemical reaction which subsequently forms O_3 by reacting with molecular oxygen. In the meantime, the UV radiation at 254 nm is absorbed by O_3, leading to decomposition into O_2 and oxygen radicals. Consequently, when both UV wavelengths are present, atomic oxygen is continuously generated, and O_3 is continually formed and dissociated. If the O_3 decomposition occurs sufficiently close to the surface of the c-Si wafer, it leads to surface oxidation. Additionally, the reactive atomic oxygen radical species can diffuse through the SiO_x layer and incorporate at the interface by saturating sub-stoichiometric species.

In an attempt of determining the UV-O_3 oxide growth rate, the exposure duration was varied from 10 to 300 sec. Prior to UV-O_3 oxide growth, *p*-type planar c-Si wafers were dipped in 5 % diluted HF to remove the native oxide. The UV exposure was performed for both sides of the wafers in order to have perfectly symmetric thicknesses. Additional measurement was performed for a duration of 120 sec after single side treatment to define the difference.

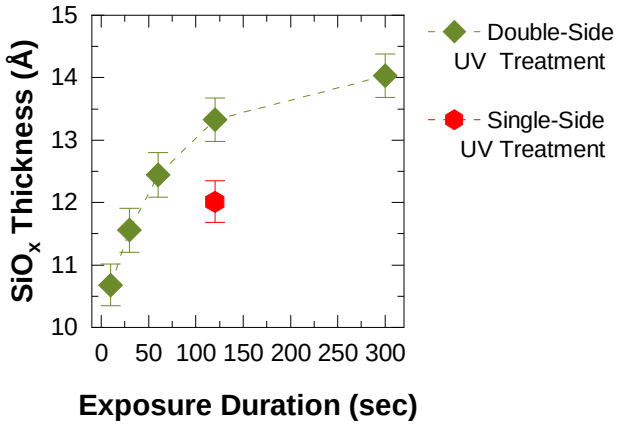

Figure C.1 – Measured UV-O_3 oxide thickness as a function of exposure time executed on both sides of the wafers indicated with green symbols and single side of the wafer indicated with red symbol.

Variable angle spectroscopic ellipsometry measurements were performed immediately after the UV-O_3 oxide growth to minimize any further oxidation in air. For the fitting procedure the native oxide model proposed in the material library of the DeltaPsi2 Software was used. Even though the spectroscopic ellipsometry can only give a rough estimation as the measurements were performed under air ambient in which ultra thin oxides such the ones investigated here, continue growing, it enables to obtain qualitative comparison.

Figure C.1 reveals the measured UV-O_3 oxide thickness as a function of UV exposure duration. It is observed that the thickness increases with exposure duration, reaching to 14 Å after 5 min treatment — the standard thickness reached with chemical SiO_x is 12 Å on *p*-type wafer and 14 Å on *n*-type wafer. Comparing the measured thicknesses after single-side and double-side UV treatment, it is observed that during the UV exposure the SiO_x grows not only on the side that is facing to the UV source but also on the opposite side leading to almost 1.5 Å thickness difference. After 10 min and longer UV exposure, the measured thickness saturates around 16 Å. In literature it was reported that the thickness of the UV-O_3 oxide is self-saturating but the density of the SiO_x increases and its composition becomes more stoichiometric with longer exposure [Moldovan 2014]. In Chapter 4, we also reported that in the case of keeping 12 Å thick chemical SiO_x on the surface of the *p*-type wafer and performing further 20 min UV exposure on both sides, only 18 Å thick SiO_x layer can be obtained.

The UV-O_3 oxide was also implemented to *p*-type planar solar cells featuring SiC_x(*n*) front and SiC_x:F(*p*) rear contact, annealed at 850 °C for 0 min. The impact of the annealing temperature was investigated by fabricating one cell with UV-O_3 oxide annealed at 875 °C. To assess the influence of the double side UV exposure, its duration was changed from 5 to 20 min. The measured cell parameters as a function of exposure duration are depicted in Figure C.2

together with the one of the best reference cell that employs chemical SiO_x in order to draw a comparison. ITO was applied as front and rear TCO due to the possibility of the batch processing — four cells can be processed with decent uniformity at the same run.

With increasing exposure duration, the V_{oc} decreases gradually according to Figure C.2(a). This can be explained with the fact that UV-O_3 oxide layer becomes slightly thicker and denser, thus the in-diffusion of the majority carriers of the contact layers into the c-Si reduces. Consequently, an insufficient band bending leads to the accumulation of the minority carriers close to UV-O_3 oxide/c-Si interface and increased recombination current. It is important to note that possibly the optimum annealing temperature is higher for the UV-O_3 oxide layer that is produced with long exposure duration in order to obtain sufficient dopant in-diffusion. More elaborate investigation has to be performed to determine the optimum, however this was not done in the scope of this thesis. Moldovan *et al.* reported that UV-O_3 oxide yields excellent surface passivation on planar and textured surfaces after annealing their TOPCon structures at 900 °C. With standard chemical SiO_x, the optimum condition was reported as 800 °C for TOPCon contact and strong degradation was reported after annealing at 900 °C [Moldovan 2015]. Nevertheless, in our case it is observed that with 5 min treatment, a V_{oc} value above 725 mV is attained. With annealing at 875 °C, a slight drop in V_{oc} is observed for the cell featuring UV-O_3 oxide produced with 5 min UV exposure.

Figure C.2(b) shows that the measured J_{sc} values are higher in the case of employing UV-O_3 oxide layers compared to standard chemical SiO_x. This might be related with the less defective nature of the UV-O_3 oxide which might lead to less free carrier absorption. With increased annealing temperature for the samples exposed to 5 min UV treatment the J_{sc} increases, probably due to the improved front layer transparency.

Employing chemical SiO_x, an impressive *FF* value of 84 % was obtained with planar cells as indicated with red star in Figure C.2(c). With UV-O_3 oxides, the obtained *FF* values appear to be much lower. It is observed that with increasing UV exposure time, the *FF* reveals a drastic drop from 82 to 73 %. This loss can be associated with a lower passivation quality. Additionally as the SiO_x layer become thicker and denser with increased UV exposure duration the tunneling probability of the charge carriers decreases. Consequently, less efficient transport is observed as manifests itself with a low *FF* value. Nevertheless, we note that the transport mechanism here strongly depends on the SiO_x structure and stoichiometry. Upon annealing, atomic defects in the SiO_x start to cluster, yielding a local thinning of the SiO_x and eventually pinhole formation which leads to an enhanced current flow in regions with thinner SiO_x. In the case of using a thick and dense SiO_x layer, e.g. thermal SiO_x, higher annealing temperatures are necessary to obtain efficient transport to manipulate the SiO_x structure accordingly. In this respect, the low *FF* limitation observed here probably can be overcome by simply increasing the annealing temperature.

As revealed in Figure C.2(d), the peak conversion efficiency is attained with short UV exposure times for the investigated annealing temperature of 850 and 875 °C. It is also observed that

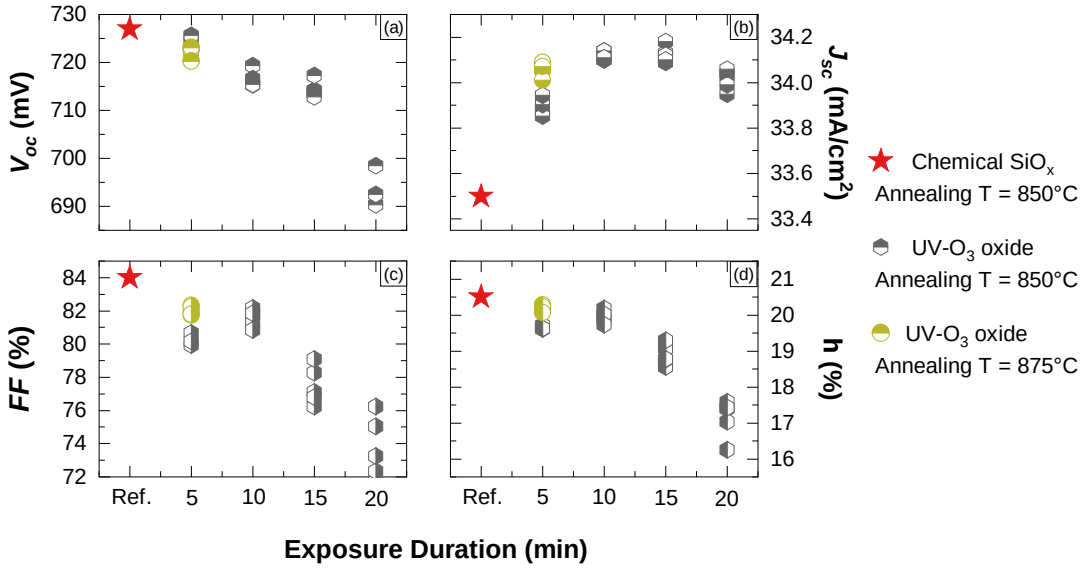

Figure C.2 – (a) V_{oc}, (b) J_{sc}(c) *FF*, and (d) efficiency of the both-sides-contacted solar cells featuring the UV-O_3 oxides prepared by varying the exposure duration executed on both sides of the wafers. The best parameters obtained with reference chemical SiO_x is indicated with red star for comparison.

the samples with UV-O_3 oxide produced by UV exposure of 2 min on both sides reveals very similar cell parameters but slightly higher *FF* value compared to the one of 5 min — not shown here for the clarity of the graph. The UV-O_3 oxide is employed for adapting the front $SiC_x(n)$ layer to the textured surfaces as it was reported in the literature that when it comes to textured surfaces, UV-O_3 oxides are preferable over chemical SiO_x due to their higher stability and favorable interface stoichiometry [Feldmann 2015].

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