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Characterization and Modeling of 28 nm Bulk CMOS Technology down to 4.2 K

(Invited Paper)

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***Abstract*—This paper presents an experimental investigation, compact modeling, and low-temperature physics-based modeling of a commercial 28 nm bulk CMOS technology operating at cryogenic temperatures. The physical and technological parameters are extracted at 300, 77, and 4.2 K from DC measurements made on various geometries. The simplified-EKV compact model is used to accurately capture the DC characteristics of this technology down to 4.2 K and to demonstrate the impact of cryogenic temperatures on the essential analog figures-of-merit. A new body-partitioning methodology is then introduced to obtain a set of analytical expressions for the electrostatic profile and the freeze-out layer thickness in field-effect transistors operating from deep-depletion to inversion. The proposed physics-based model relies on the drift-diffusion transport mechanism to obtain the drain current and subthreshold swing, and is validated with the experimental results. This model explains the degradation in subthreshold swing at deep-cryogenic temperatures by the temperature-dependent occupation of interface charge traps. This leads to a degradation of the theoretical limit of the subthreshold swing at deep-cryogenic temperatures.**

***Keywords*—28 nm bulk CMOS, cryoelectronics, cryogenic, interface charge traps, MOS transistor modeling, slope factor, 4.2 K**

I. Introduction

Outstanding characteristics have been reported for advanced CMOS technologies operating at cryogenic temperature in terms of on-state current, leakage current, subthreshold swing, and transconductance [1]–[8]. This represents an excellent opportunity to use such advanced technologies to design and implement a quantum computing control system (including multiplexers, LNAs, and RF oscillators) and introduce it inside the refrigerator together with the qubits [9]–[12]. For solid-state qubits, the qubit control system could even be co-integrated on the same chip, in a planar or 3D-configuration [13], [14]. This would facilitate the scale-up to hundreds of qubits—to show exponential speed-up over conventional computing on specific problems [15]—by mitigating wiring challenges and reducing the thermal-noise contribution from a control system operated at room temperature. Furthermore, a higher performance of qubit information processing, combined with a lower power consumption, is expected from an advanced CMOS process. The extremely-high transit frequency in a 28 nm technology can be traded-off for a lower thermal-noise dissipation towards the qubits by shifting the bias-point to weak inversion. However, finding the optimal trade-off in the design of cryo-CMOS circuits is challenging due to the lack of MOS transistor models valid down to cryogenic and deep-cryogenic temperatures (typically 4.2 K or even below for quantum computing applications). Developing a physics-based model for MOS transistors operating below 77 K [16], [17] and above the zero-Kelvin approximation [18], has been held up by the numerical difficulties of modeling and simulation in this temperature range [19]–[21]. The intrinsic carrier concentration becomes extremely small at $\approx$ 4.2 K, which has its inevitable root in the exponential temperature scaling of the Fermi-Dirac and Boltzmann statistics. In addition, the measured subthreshold swing at 4.2 K (11 mV/dec) is much worse than the one predicted by the theoretical limit, $U_T \ln 10$ (0.8 mV/dec) [2], [22]. This degradation in subthreshold swing translates into a strong increase of the slope factor [2], and cannot be correctly modeled with the available compact models.

In this work, a commercial 28 nm bulk CMOS technology is first experimentally characterized (Sec. II). The cryogenic trends in the analog figures-of-merit are then discussed relying on the simplified EKV empirical model (Sec. III). Finally, a new physics-based model for deep-cryogenic operation is developed (Sec. IV). The proposed model allows to obtain insight in the cryo-electrostatics, and explains the discrepancy between the theoretical limit and the actual value of the subthreshold swing at deep-cryogenic temperatures through the Fermi-Dirac occupation probability of the interface charge traps.

II. Measurement Results and Characterization

A wire-bonded sample chip from a 28 nm bulk CMOS process is depicted in Fig. 1a. Table I shows the dimensions of the devices under investigation. After measurements at room temperature (RT), a dip-stick was used to immerse the samples into liquid nitrogen (77 K) and liquid helium (4.2 K). The transfer characteristics were measured in the saturation regime (drain-to-bulk voltage $|V_{DB}|$ = 0.9 V, Figs. 1b-f) and the linear regime ($|V_{DB}|$ = 20 mV, Figs. 1g-i), as well as the output characteristics (Sec.III). The subthreshold swing, SS, is one of the main parameters in low-power design. From the transfer characteristics it can be observed that the SS improves significantly at 77 K and 4.2 K compared to RT, for all devices. This improvement in SS is illustrated in Fig. 2a for the measurements in saturation. It should be noted that the SS in the linear regime is similar to its saturation value at 4.2 K (by comparing e.g. Figs. 1b and 1h). However, Fig. 2a highlights that the SS decreases only to 11 mV/dec at 4.2 K ($-85\,\%$) for long channel nMOS ($L = 1\,\mu\text{m}$) instead of the theoretical

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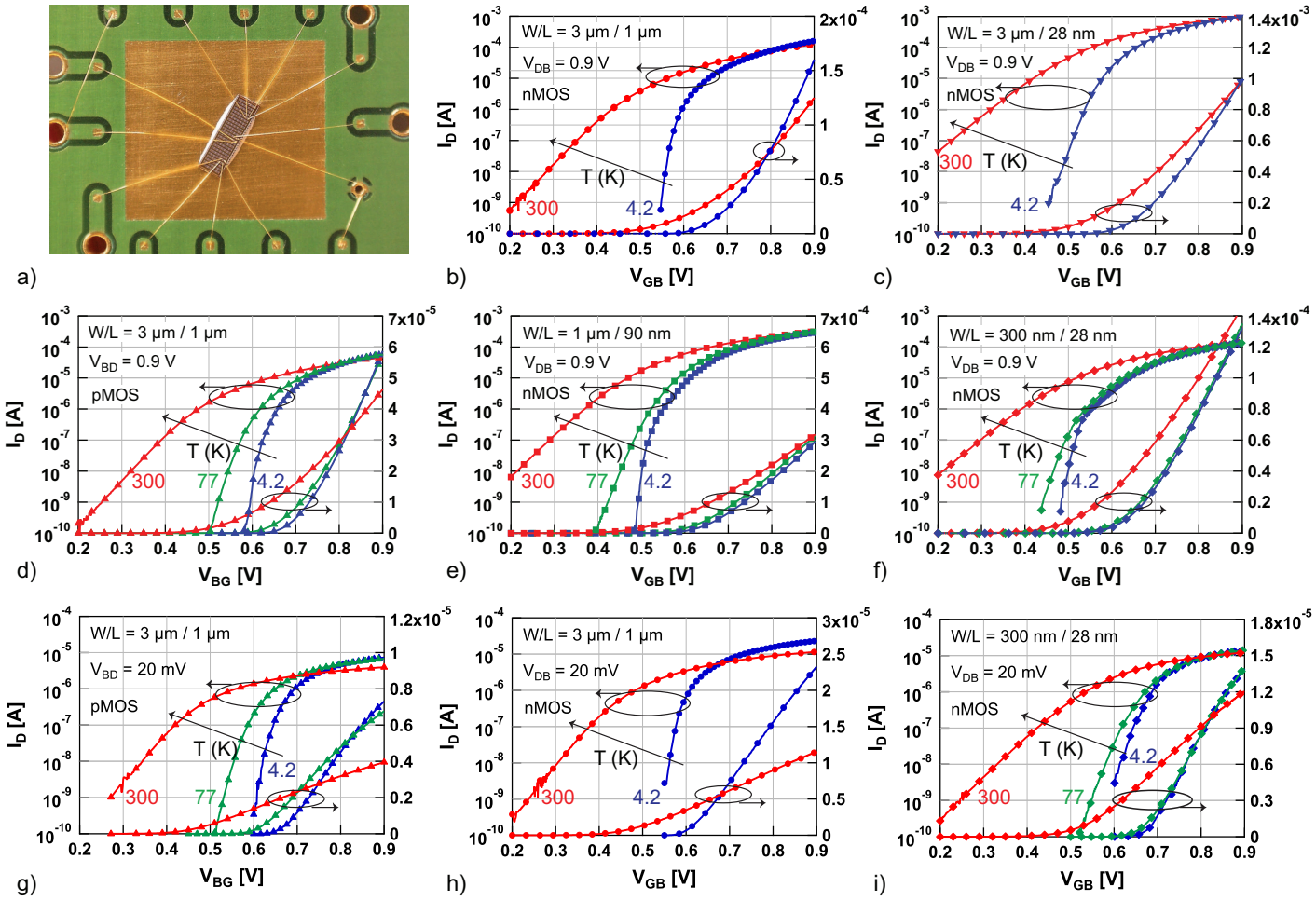

Fig. 1. a) Sample chip, wire-bonded with Au-wire bonds and glued to a standard PCB, b)-f) Transfer characteristics measured on a 28 nm bulk CMOS process in saturation ($|V_{DB}|$ = 0.9 V), and g-i) linear regime ($|V_{DB}|$ = 20 mV): b) nMOS $W/L = 3$ µm / 1 µm at 300 K and 4.2 K in saturation, c) nMOS $W/L = 3$ µm / 28 nm at 300 K and 4.2 K in saturation, d) pMOS $W/L = 3$ µm / 1 µm at 300, 77 and 4.2 K in saturation, e) nMOS $W/L = 1$ µm / 90 nm at 300, 77 and 4.2 K in saturation, f) nMOS $W/L = 300$ nm / 28 nm at 300, 77 and 4.2 K in saturation, g) pMOS $W/L = 3$ µm / 1 µm at 300, 77 and 4.2 K in linear, h) nMOS $W/L = 3$ µm / 1 µm at 300 K and 4.2 K in linear, and i) nMOS $W/L = 300$ nm / 28 nm at 300, 77 and 4.2 K in linear. The gate-to-bulk voltage (V_{GB}) is increased with a step size of 1 mV to accurately resolve the steep subthreshold swing at 4.2 K. Marker symbols denote the device type shown in Table I, and colors refer to the temperature, red: room temperature (300 K), green: liquid nitrogen temperature (77 K) and blue: liquid helium temperature (4.2 K).

limit of 0.8 mV/dec, predicted by $U_T \ln 10$ with $U_T \triangleq kT/q$ the thermal voltage. This high value of SS at 4.2 K hints on a shift deviating upward parallel to $U_T \ln 10$ (see Sec. IV). The deviation between the ideal and the actual scaling of the SS is measured by the slope factor, n, according to $SS = nU_T \ln 10$. Fig. 2b shows a strong temperature dependency of n in the deep-cryogenic regime: at 77 K, n is still near its RT-value, i.e. 1.6 compared to 1.47, however, at 4.2 K, n attains a value of 20 (for nMOS $W/L = 300$ nm/ 28 nm). The impact of this increase on analog design will be discussed in Sec.III, and its physical origin will be explained in Sec. IV. In short channel nMOS ($L = 28$ nm), the SS reaches only 28 mV/dec at 4.2 K (-68 % compared to RT) due to short-channel effects also present at 4.2 K. Promising for analog design, the transconductance in saturation, $G_{m,sat}$, improves at 4.2 K (e.g. $\times$ 1.3 for nMOS, W/L= 3 µm/ 28 nm) as shown in Fig. 2c. The threshold voltage, V_{th}, extracted from $G_{m,sat}$, increases by about $\approx$0.1-0.2 V with respect to its RT-value (Fig. 2d) due to the shift of the Fermi-level in the bulk and the scaling of the Fermi-Dirac occupation function with temperature (Sec. IV). Based on the measurements in the linear regime, the Y-function method [23] was used to extract the low-field mobility (μ_0). Fig. 2e illustrates the strong improvement (e.g. $\times$ 3 for nMOS, L = 1 µm) at 4.2 K due to a reduction in the phonon scattering. The on-state current ($|V_{GB}|$ =0.9 V), plotted in Fig. 2f, is increased at 4.2 K only for the long devices.

TABLE I. MEASURED DEVICES (28 NM BULK CMOS PROCESS)

Symbol	Type	W/L
●	nMOS	3 µm / 1 µm
▲	pMOS	3 µm / 1 µm
■	nMOS	1 µm / 90 nm
▼	nMOS	3 µm / 28 nm
◆	nMOS	300 nm / 28 nm

III. SIMPLIFIED EKV MODELING AND ANALOG FIGURES-OF-MERIT

In this section the focus lies on the measurements in saturation since in analog circuits, most devices are actually

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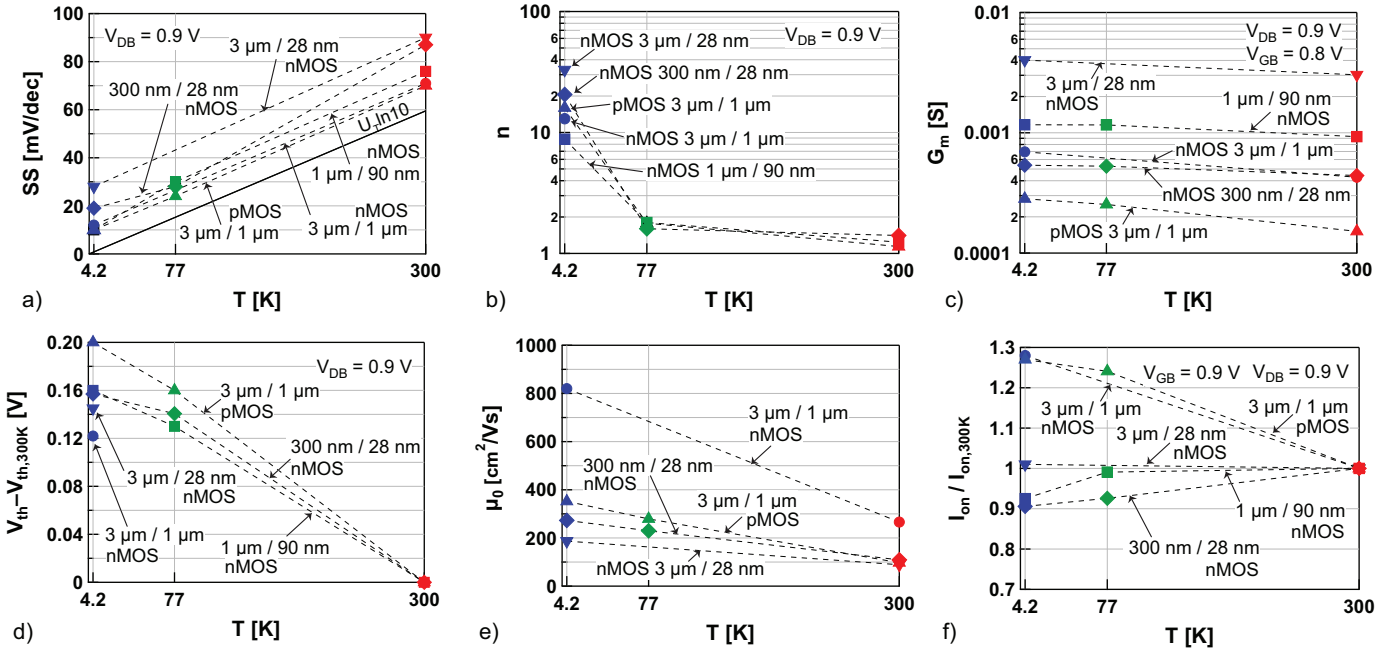

Fig. 2. Physical and technological parameters versus temperature at 300, 77 and 4.2 K, a) Subthreshold swing, indicating a parallel deviation from the theoretical limit ($U_T \ln 10$) instead of bending to 0 near 0 K, b) Corresponding strong rise of the slope factor at deep-cryogenic temperatures, c) Transconductance-increase with decreasing temperature, d) Threshold voltage shift of $\approx$ 0.1-0.2 V at 4.2 K for all devices, extracted from $G_{m,sat}$ at V_{DB} = 0.9 V and V_{GB} = 0.9 V, e) Low-field mobility extracted using the Y-function method [23], f) On-state current referred to its RT-value.

biased into saturation. The analog figures-of-merit are obtained using the simplified and normalized EKV compact model [24]–[26]. For long devices, this model relies on the following three parameters: the slope factor n, the threshold voltage V_{T0}, and the specific current $I_{spec} = I_{spec\square} W/L = 2(W/L)n\mu C_{ox} U_T^2$. For short-channel devices, the model relies additionally on the saturation length, L_{sat}, referring to the part of the channel that is in full velocity saturation [24]–[26]. The physical parameters extracted in Fig. 2 can be used to obtain initial guesses for these model parameters. Fig.3a and 3b demonstrate that the transfer characteristics of a long and short device are accurately captured down to 4.2 K, when using a strongly increased slope factor n. We emphasize that the values for the model parameters n and V_{T0} match the extracted values in Figs. 2b and 2d. The extracted model parameter I_{spec}, a measure of the current delimiting the above and sub-threshold regimes, is found to decrease by one order of magnitude from RT to 4.2 K. Fig. 3c plots the normalized current efficiency, $G_m n U_T / I_D$ versus $IC \triangleq I_{D,sat}/I_{spec}$, which is an essential figure-of-merit for low-power analog design indicating how much transconductance the device can deliver for a given current [24]–[26]. It is used to optimize circuits in terms of power, gain, noise and linearity [27]–[29]. Here it is shown that the G_m/I_D-design methodology based on this characteristic can also be employed down to 4.2 K. The characteristic shows a lower impact of velocity saturation at 4.2 K ($IC > 10$) and a decrease of L_{sat} from 6 nm at RT to 3 nm at 4.2 K (L = 28 nm) explained by the phonon scattering reduction. Note that Fig. 3c demonstrates that the properly normalized G_m/I_D is not only invariant over technologies [25], [26], but extends its universality to cryogenic temperatures. As evidenced by the output characteristics in Fig. 3d and 3e, no kink effect [30], [31] is observed for this 28 nm bulk CMOS technology below the standard supply voltage of 0.9 V, and the output conductance, G_{ds}, remains practically constant with respect to temperature. This results in an increased intrinsic gain, G_m/G_{ds}, at 77 K ($\times$ 1.2) and 4.2 K ($\times$ 1.3, for nMOS, W/L =300 nm/ 28 nm) in Fig. 3f. The transit frequency, $F_t = G_m/(2\pi C_{gg})$, with C_{gg} the total gate capacitance, follows the increase in the transconductance (Fig. 2c) when accounting for the fact that the capacitances are not strongly dependent on temperature [32]. The F_t of a 28 nm bulk CMOS technology at RT already reaches $\approx$ 300 GHz. This is much higher than the F_t required by the qubit control and read-out circuits [14], [33]. This excess F_t at cryogenic temperature can be traded-off for a lower power consumption by shifting the operating points to weak inversion resulting in less heat dissipation therefore relaxing the cooling power budget. However, the strong increase of n at deep-cryogenic temperature (e.g. 4.2 K) has a direct impact on this trade-off. If the circuit would be designed to reach the same F_t as at RT, the current reduction factor in weak inversion, using $G_m = I_D/(nU_T)$, is $I_{D,RT}/I_{D,cryo} = (300/T[K])(n_{RT}/n)$, where T and n represent the values at cryogenic temperatures. Ideally, if n would stay the same at 4.2 K as at RT, the current reduction factor would be 71. Unfortunately, due to the strong increase of n at 4.2 K mentioned above, the current reduction is only 5.2 for W/L = 300 nm / 28 nm (n = 20), and as low as 3.2 for W/L = 3 µm / 28 nm (n = 33). Therefore, the dramatic increase of n strongly mitigates the current saving expected at cryogenic temperature when biasing the device in weak inversion.

To explain this important increase of n on physical grounds, in the next section a physics-based model valid down to deep-cryogenic temperature (4.2 K) is developed for different regions of operation, from deep-depletion to strong inversion. The bandgap, incomplete ionization, carrier mobility,

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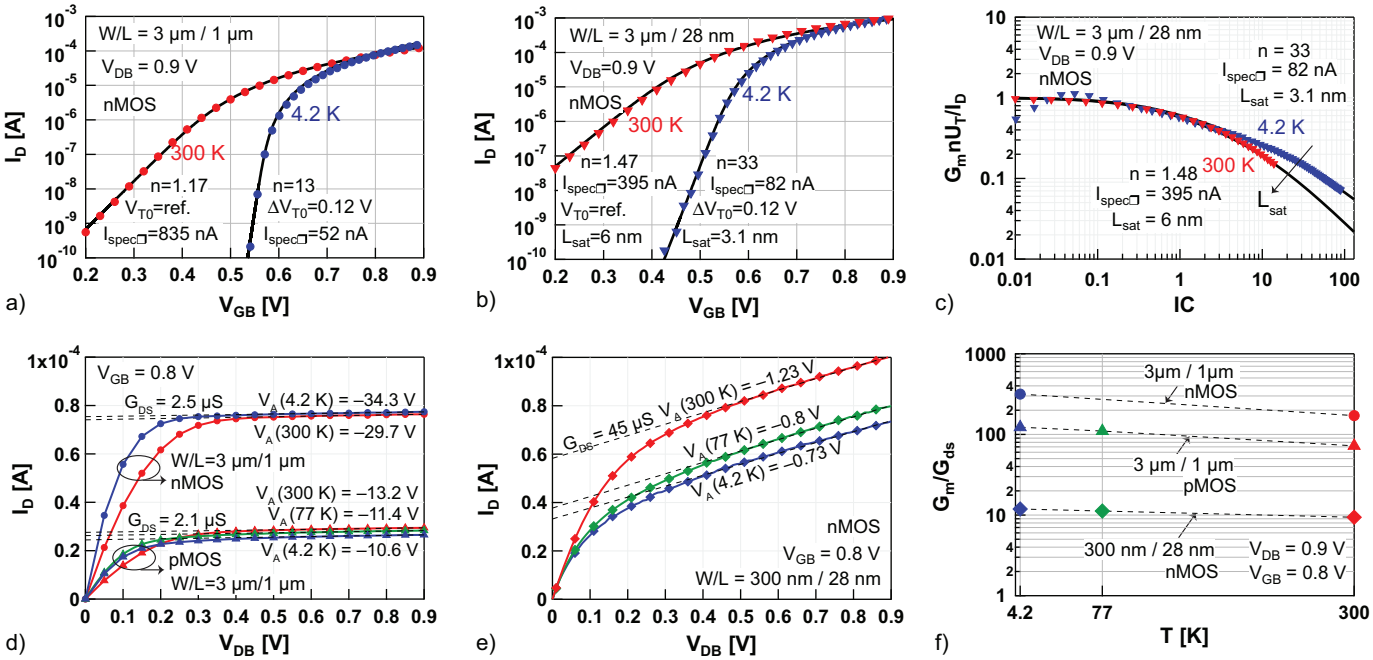

Fig. 3. Simplified EKV compact modeling and impact on analog figures-of-merit down to 4.2 K, a)-b) Comparison of the model (solid lines) with the measured transfer characteristics (markers) for a) long nMOS $W/L = 3\ \mu m / 1\ \mu m$, and b) short nMOS $W/L = 3\ \mu m / 28$ nm, c) Normalized current efficiency versus the inversion coefficient for nMOS $W/L = 3\ \mu m / 28$ nm, indicating a reduced velocity saturation at 4.2 K, d)-e) Measured output characteristics for long channel nMOS and pMOS ($W/L = 3\ \mu m / 1\ \mu m$), and for short channel nMOS ($W/L = 300$ nm / 28 nm), indicating no kink effect below 0.9 V. The extracted output conductances, G_{ds}, and Early voltages, V_A, are shown, f) Increase in the intrinsic gain at 77 and 4.2 K compared to RT.

and interface charge traps are all temperature-dependent, and expected to play important roles in explaining the characterized temperature dependencies of the subthreshold swing, slope factor, threshold voltage, and on-state current. The derivation focuses on a long device operating in the linear regime.

IV. Physics-based cryo-MOSFET Modeling

The simplified EKV model used in Sec.III is empirical and requires a different set of parameters for each device geometry and each temperature. As a first step towards the development of a general physics-based cryo-MOS model, a fundamental investigation of the cryo-electrostatics, governed by freeze-out and field-assisted ionization, is described here.

A. Cryo-electrostatics in MOSFET

In this study, we model a long n-channel silicon MOSFET, with gate length, L, and width, W. In [34] we verified that the mobile carrier concentrations in a non-degenerated semiconductor are still non-degenerate at deep-cryogenic temperatures, and can thus be estimated by the Boltzmann statistics down to this temperature range. Therefore, merging the Boltzmann statistics with the 1D Poisson equation in the vertical direction (y) in a MOSFET, yields

$$\frac{\partial^2 \psi(y)}{\partial y^2} = -\frac{q}{\varepsilon_{si}} \left(-n_i e^{\frac{\psi - V_{ch}}{U_T}} + n_i e^{-\frac{\psi}{U_T}} - N_A^- \right), \qquad (1)$$

where ψ is the potential, q the elementary charge, ε_{si} the silicon permittivity, and V_{ch} the channel voltage. The first two terms on the RHS of (1) denote the electron and hole mobile charge densities with n_i the intrinsic carrier concentration, and the last term is the ionized dopant concentration N_A^-. The incomplete ionization of the dopants can be taken into account in (1) according to

$$N_A^- = N_A \times f(E_A) = \frac{N_A}{1 + g_A e^{\frac{E_A - E_F}{kT}}}, \qquad (2)$$

where $f(E_A)$ is the Fermi-Dirac occupation probability of the acceptor energy E_A, corresponding to the ionization of the acceptor dopants. The acceptor-site degeneracy factor, g_A, is equal to four due to fourfold degeneracy (heavy/light hole, spin up/down) [35], [36]. Solving (1) might be feasible using an extended arithmetic precision to avoid convergence problems due to the extremely small value of n_i, e.g. at 4.2 K $\approx 10^{-678}$ cm^{-3} [34], lying outside the range of IEEE double precision arithmetic ($10^{-308} - 10^{308}$) starting from below $T \approx 8$ K. However, this is computationally more demanding in numerical TCAD simulations [20]. Hence, numerical techniques have been proposed in the literature to ease convergence problems [20], [37], [38]. Here, an analytical approach is proposed to obtain the electrostatics at cryogenic temperature. Relying on the introduced method of body-partitioning, equation (1) is solved analytically. This results in explicit solutions for the potential profile and charge densities across the MOSFET-body. The proposed expressions are then implemented with an extended arithmetic precision. As explained next, the MOSFET-body is partitioned into electrostatic layers which are parallel to the current transport direction.

B. Body-partitioning

Fig. 4 clarifies the body-partitioning approach for different regions of operation: flatband (Fig. 4a), deep-depletion (Fig. 4b), depletion (Fig. 4c), and inversion (Fig. 4d). As the

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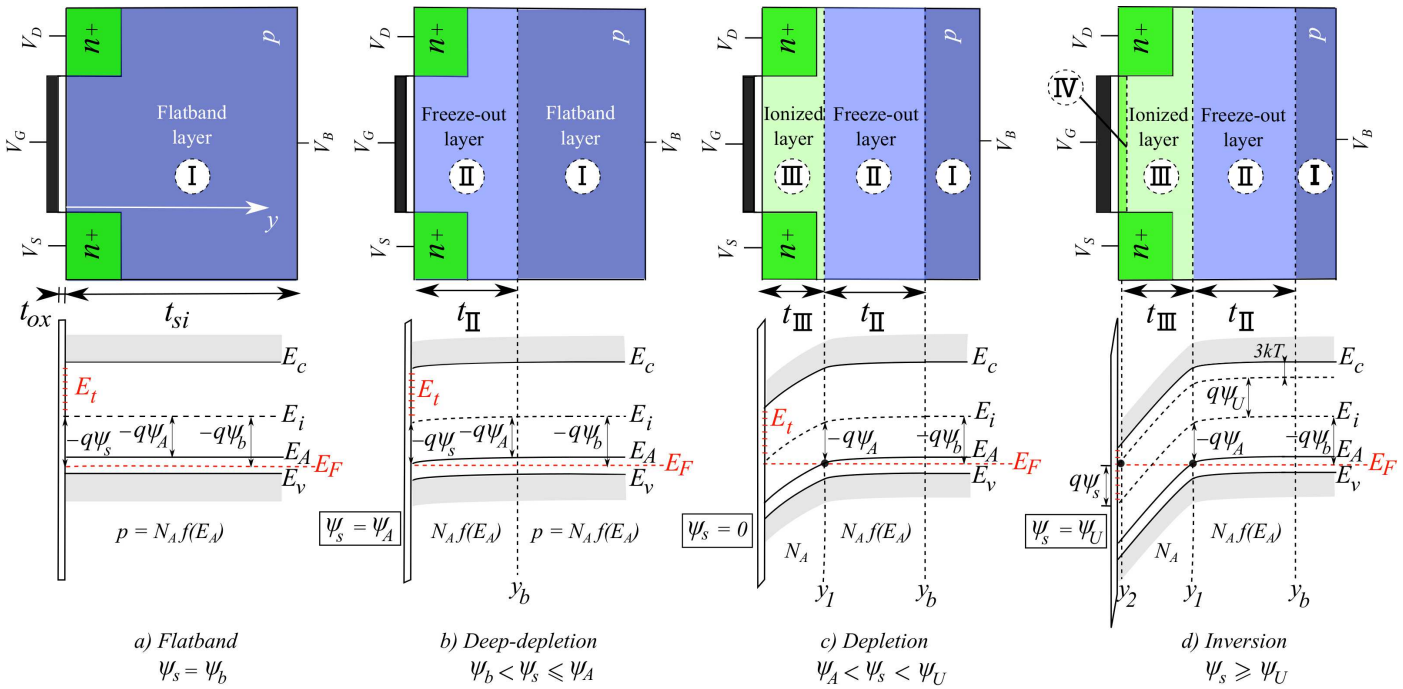

Fig. 4. Body-partitioning methodology applied to a long MOSFET operating in the linear regime at deep-cryogenic temperatures. The Fermi-level, E_F, and the interface trap energy levels, E_t, are indicated in red. Depending on the position of the bands with respect to E_F, different layers can be distinguished: a) flatband condition, only the flatband layer exists, and E_F is positioned below the acceptor energy, E_A, for sufficiently low cryogenic temperature (see Table II) resulting in incomplete ionization or even freeze-out based on (2), b) deep-depletion, a new layer forms, called the freeze-out layer, where E_A is bent but still above E_F, c) depletion, E_A is bent below E_F leading to complete ionization in layer III, the ionized layer, d) inversion, at the surface an inversion layer (layer IV) starts to form when E_F comes with $\approx 3kT$ near E_c at the surface. Note that the quasi-Fermi-potential is not taken into account in this figure.

surface potential, ψ_s, increases, as soon as entering a new region of operation, an additional layer appears under the surface. For instance, when the device is operating in inversion mode, the body is partitioned in the following different layers: I) the bulk ($y_b < y < t_{si}$), II) the freeze-out layer ($y_1 < y < y_b$), III) the ionized layer ($y_2 < y < y_1$), and IV) the inversion layer ($0 < y < y_2$), where t_{si} is the thickness of the silicon, y_1 represents the position at which E_A crosses E_F, and y_2 represents the position at which E_F crosses $E_c - 3kT$. Thanks to this partitioning, the 1D Poisson equation in (1) can then be solved analytically in each layer separately. Imposing the continuity conditions at the layer boundaries,

- **Surface:** $\psi_{\mathrm{IV}}(0) = \psi_s$ and $\mathbf{E}_{\mathrm{IV}}(0) = \mathbf{E}_s$
- **Boundary IV–III:** $\psi_{\mathrm{IV}}(y_2) = \psi_{\mathrm{III}}(y_2) = \psi_2$ and $\mathbf{E}_{\mathrm{IV}}(y_2) = \mathbf{E}_{\mathrm{III}}(y_2)$
- **Boundary III–II:** $\psi_{\mathrm{III}}(y_1) = \psi_{\mathrm{II}}(y_1) = \psi_1$ and $\mathbf{E}_{\mathrm{III}}(y_1) = \mathbf{E}_{\mathrm{II}}(y_1)$
- **Boundary II–Bulk:** $\psi_{\mathrm{II}}(y_b) = \psi_b$ and $\mathbf{E}_{\mathrm{II}}(y_b) = 0$

where $\psi_b \triangleq (E_F - E_i)/q$ in layer I, $\psi_1 = \psi_A \triangleq (E_A - E_i)/q$, and $\psi_2 = \psi_U \triangleq (E_c - E_i)/q - 3U_T$. The energy levels E_c and E_i are respectively the conduction band and intrinsic energy. It is assumed that the distance between E_A and the valence band, E_v, remains independent of the temperature (i.e. $E_A - E_v =$ 0.045 eV for boron-doped silicon), and therefore ψ_A follows the bandgap temperature-dependency. This dependency is not strong in the cryogenic regime [39], as shown in Fig. 5a. Next, we consider each operational regime separately, and solve the 1D Poisson-Boltzmann equation for an additional layer.

1) Flatband ($\psi_s = \psi_b$): As illustrated in Fig.4a, the potential is constant across the semiconductor, i.e. $\psi_{\mathrm{I}} = \psi_s = \psi_b$. Imposing a constant potential value, i.e. ψ_b, in equation (1) and neglecting the electron carrier concentration lead to

$$n_i e^{-\frac{\psi_b}{U_T}} = \frac{N_A}{1 + g_A e^{\frac{\psi_A - \psi_b}{U_T}}}, \quad \textbf{(Layer I)} \tag{3}$$

where $E_A - E_F$ was replaced by $E_A - E_i + E_i - E_F$ in the exponential term of (2). Equation (3) leads to an explicit expression of ψ_b as a function of temperature and doping concentration, given by

$$\psi_b = U_T \ln \frac{n_i}{N_A} + U_T \ln \left(\frac{1 + \sqrt{1 + 4 \frac{N_A}{n_i} g_A e^{\frac{\psi_A}{U_T}}}}{2} \right) \tag{4}$$

Fig. 5a shows the temperature and doping dependencies of ψ_b. The condition $\psi_b < \psi_A$ guarantees that E_F is positioned below E_A in the flatband condition (Fig.4a). As illustrated in Fig. 5a, for a sufficiently low cryogenic temperature, T_c, ψ_b lies under ψ_A. Note that T_c increases for higher doping concentrations (Table II). Below T_c, the ionization probability in (2) is extremely low, leading to substantial incomplete ionization or even freeze-out in the bulk. Freeze-out is assumed to occur as soon as $E_A = E_F$, where 20% of the dopants are ionized due to the degeneracy factor, i.e. $g_A = 4$, in (2). In Fig.5b, the thermal ionization probability, $1/\{1 + g_A \exp[(\psi_A - \psi_b)/U_T]\}$, is plotted for $N_A = 10^{18}\,\mathrm{cm}^{-3}$ and $g_A = 4$.

Increasing the gate voltage above the flatband potential, an additional layer forms where freeze-out can still happen, as explained next.

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TABLE II. FREEZE-OUT CRITICAL TEMPERATURE

Doping concentration	T_c
$N_A = 10^{18}\,\mathrm{cm}^{-3}$	140 K
$N_A = 10^{16}\,\mathrm{cm}^{-3}$	70 K
$N_A = 10^{14}\,\mathrm{cm}^{-3}$	45 K
$N_A = 10^{12}\,\mathrm{cm}^{-3}$	30 K

2) Deep-depletion ($\psi_b < \psi_s \leqslant \psi_A$): The bands bend downward until E_A reaches E_F at the surface ($\psi_s = \psi_A$). An additional layer, called the freeze-out layer, occurs where $E_A \geqslant E_F$. It should be noted that this condition leads to freeze-out when kT is very low for deep-cryogenic temperatures (see (2)). The exponential term on the RHS of (2) is dominant when U_T is small and $E_A > E_F$. Therefore, using a Maxwell-Boltzmann approximation for the Fermi-Dirac ionization probability of the dopants, and neglecting the hole density in (1), leads to

$$\frac{\partial^2 \psi_{\mathrm{II}}(y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si} g_A} e^{\frac{\psi_{\mathrm{II}} - \psi_A}{U_T}} \quad \textbf{(Layer II)} \tag{5}$$

After some mathematical manipulation (see Appendix), the electric field in the freeze-out layer is given by

$$\mathbf{E}_{\mathrm{II}}(\psi_{\mathrm{II}}) = \kappa \sqrt{e^{\frac{\psi_{\mathrm{II}}}{U_T}} - e^{\frac{\psi_b}{U_T}}}, \tag{6}$$

where $\kappa = \sqrt{2qN_A U_T \exp(-\psi_A/U_T)/(g_A \varepsilon_{si})}$ and with a given value of ψ_b obtained from (4). The continuity of the electric field at the boundary between the freeze-out and flatband layers ($y = y_b$) is satisfied by $\mathbf{E}_{\mathrm{II}}(y_b) = 0$. Integrating once (6) (see Appendix), the potential profile in this layer is expressed as

$$\psi_{\mathrm{II}}(y) = \psi_b + U_T \ln\left\{\tan^2\left[\sigma(y_b - y)\right] + 1\right\}, \tag{7}$$

with $\sigma = \kappa\sqrt{\exp(\psi_b/U_T)}/(2U_T)$. Similarly, the potential continuity at the boundary between the freeze-out and flatband layers ($y = y_b$) is satisfied by $\psi_{\mathrm{II}}(y_b) = \psi_b$. Imposing the potential continuity at the silicon-oxide/silicon interface ($y = 0$), $\psi_{\mathrm{II}}(0) = \psi_s$, leads to the thickness of the freeze-out layer as a function of ψ_s,

$$t_{\mathrm{II}} = y_b = \frac{1}{\sigma} \arctan \sqrt{e^{\frac{\psi_s - \psi_b}{U_T}} - 1} \tag{8}$$

It is worth noting that the maximum freeze-out layer thickness occurs when $\psi_s = \psi_A$, which then does not depend on ψ_s anymore, i.e.

$$t_{\mathrm{II,max}} = \frac{1}{\sigma} \arctan \sqrt{e^{\frac{\psi_A - \psi_b}{U_T}} - 1} \tag{9}$$

Fig. 5c plots the maximum freeze-out layer thicknesses for different doping concentrations versus temperature below the freeze-out critical temperature, T_c, of a given doping (see Table II). Above T_c, the freeze-out layer vanishes since $E_F > E_A$ (Fig.5a). Combining the Boltzmann statistics for $f(E_A)$ with the expression for $\psi_{\mathrm{II}}(y)$ given by (7) and then integrating over y (see Appendix), the frozen charge density per unit area is given by

$$Q_{\mathrm{II}}(y) = -\frac{\zeta}{\sigma} \tan\left(\sigma(y_b - y)\right) + 2\zeta(y_b - y), \tag{10}$$

where $\zeta = qN_A \exp\left[(\psi_b - \psi_A)/U_T\right]/g_A$. At the end of the deep-depletion operation regime, when $\psi_s = \psi_A$, the maximum thickness of the freeze-out layer, as expressed by (9), has been reached. The maximum total charge density in the freeze-out layer, Q_{II}, can be written as $-(\zeta/\sigma)\tan(\sigma t_{\mathrm{II,max}}) + 2\zeta t_{\mathrm{II,max}}$.

Increasing the gate voltage further, an additional, ionized layer will shift the freeze-out layer downwards due to the band bending.

3) Depletion ($\psi_A < \psi_s < \psi_U$): The increase of ψ_s above ψ_A pushes E_F above E_A at the surface. This band bending helps completely ionizing the dopants below the silicon-oxide/silicon interface, i.e. field-assisted ionization [40]. Fig. 5d plots the profile of the ionization probability for dopants near the surface, $f_s(E_A)$, with respect to T and $\psi_s - \psi_b$. As illustrated in this figure, already for $\psi_s - \psi_b > 0.1$ V above flatband (well below inversion mode), complete ionization of the dopants happens at the interface for all temperatures. Note that this is the primary reason explaining why the MOSFET operates properly even at deep-cryogenic temperatures (4.2 K), in contrast with bulk conduction devices such as the bipolar transistor [41]. The potential at the boundary between the freeze-out and ionized layers ($y = y_1$), where E_A crosses E_F, is equal to ψ_A, which is a *floating* potential due to the highly-resistive freeze-out layer [42]. Moreover, the position of this boundary (y_1) *floats* with increasing ψ_s, as will be derived next. It should be highlighted that the transition between the freeze-out and completely ionized layers happens sharply at cryogenic temperatures.

Next, assuming complete ionization in the ionized layer, the electric field and potential profile in this layer are obtained from

$$\frac{\partial^2 \psi_{\mathrm{III}}(y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \quad \textbf{(Layer III)} \tag{11}$$

Integrating once and twice, yields the electric field and potential respectively,

$$\mathbf{E}_{\mathrm{III}}(y) = -\frac{qN_A}{\varepsilon_{si}}(y - y_1) + \mathbf{E}_1, \tag{12}$$

$$\psi_{\mathrm{III}}(y) = \frac{qN_A}{2\varepsilon_{si}}(y - y_1)^2 - \mathbf{E}_1(y - y_1) + \psi_A, \tag{13}$$

where the electric field and potential continuity conditions at y_1, are respectively fulfilled by $\psi_{\mathrm{III}}(y_1) = \psi_A$ and $\mathbf{E}_{\mathrm{III}}(y_1) = \mathbf{E}_1$, with $\mathbf{E}_1$ obtained from (6) when $\psi_{\mathrm{II}} = \psi_A$. The surface boundary condition imposed by $\psi_{\mathrm{III}}(y = 0) = \psi_s$, leads to the ionized layer thickness:

$$t_{\mathrm{III}} = y_1 = \frac{\varepsilon_{si}}{qN_A}\left(\sqrt{\mathbf{E}_1^2 - \frac{2qN_A}{\varepsilon_{si}}(\psi_A - \psi_s)} - \mathbf{E}_1\right) \tag{14}$$

As can be found from this equation, the ionized layer thickness is a function of the surface potential, leading to the floating point y_1 where E_A crosses E_F. Fig. 5e shows the ionized layer thickness as a function of ψ_s at $T = 4.2$ K for different doping concentrations. At a given value of ψ_s, the ionized layer thickness is reduced for higher doping concentration. It should be noticed that for higher ionized layer thicknesses, the entire device becomes fully ionized, pushing the freeze-out and flatband layers out of the device (e.g. FD-SOI, and nanowires).

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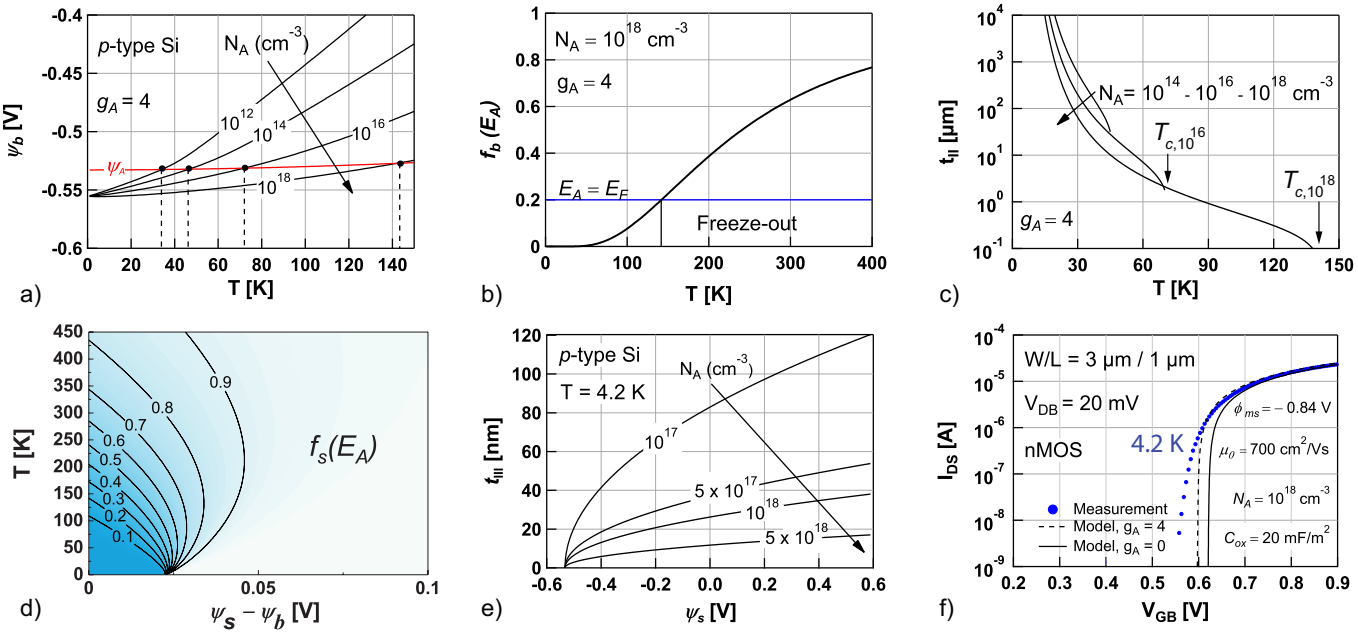

Fig. 5. Physics-based MOSFET modeling at deep-cryogenic temperatures, a) Bulk potential as a function of temperature for different doping concentrations. Crossing points with ψ_A indicate the critical cryogenic temperatures, T_c, where E_F is positioned at E_A in the bulk (layer I). Below this temperature, freeze-out can occur for the specific doping (see Table II), b) Thermal ionization probability in the bulk (layer I). No field-assisted ionization (due to band bending) is possible in layer I, c) Maximum freeze-out layer thickness ($t_{\mathrm{II,max}}$) for different doping concentrations versus temperature below T_c, d) Ionization probability at the surface as a function of temperature (thermal ionization) and surface potential (field-assisted ionization), demonstrating that complete ionization is a valid approximation even for deep-cryogenic temperatures when sufficiently above flatband. Freeze-out under the gate ($f_s(E_A) < 0.2$) is only possible for $T < 150\,K$ and close to flatband ($\psi_s \approx \psi_b$), e) Ionized layer thickness (t_{III}) for different doping concentrations, f) Comparison of the measured drain current at 4.2 K for nMOS $W/L = 3\,\mu\mathrm{m}/1\,\mu\mathrm{m}$ (markers) in the linear regime, and the model (solid lines), indicating that incomplete ionization ($g_A = 4$) cannot degrade the subthreshold swing at 4.2 K.

The total charge density per unit area in the ionized layer can be calculated as

$$Q_{\mathrm{III}}(y) = -qN_A(y_1 - y) \tag{15}$$

The maximum total charge density in this layer, Q_{III}, is given by $-qN_A t_{\mathrm{III}}$ when $y = 0$. Increasing the gate voltage to the most positive potentials, the silicon body is partly inverted and an additional, inversion layer is formed.

4) Inversion ($\psi_s \geqslant \psi_U$): More band bending leads to an additional crossing point where E_F meets $E_c - 3kT$. The Fermi-Dirac occupation probability is approximately zero for energy levels $3kT$ above E_F. Therefore, an inversion layer starts forming when $\psi_s = \psi_U \triangleq (E_c - E_i)/q - 3U_T$ (see Fig. 4d). It is assumed that the inversion layer has a negligible thickness y_2 (charge sheet approximation). Neglecting fixed dopant and hole concentrations in the inversion layer, the Poisson-Boltzmann equation is given by

$$\frac{\partial^2 \psi_{\mathrm{IV}}(y)}{\partial y^2} = \frac{qn_i}{\varepsilon_{si}} e^{\frac{\psi_{\mathrm{IV}} - V_{ch}}{U_T}} \quad \textbf{(Layer IV)} \tag{16}$$

Once integrating (16) (see Appendix), the electric field in the inversion layer is obtained,

$$\mathbf{E}_{\mathrm{IV}}(\psi_{\mathrm{IV}}) = \sqrt{\mathbf{E}_s^2 + \frac{2qn_iU_T}{\varepsilon_{si}}\left(e^{\frac{\psi_{\mathrm{IV}} - V_{ch}}{U_T}} - e^{\frac{\psi_s - V_{ch}}{U_T}}\right)} \tag{17}$$

The electric field continuity condition at $y = 0$ is satisfied by $\mathbf{E}_{\mathrm{IV}}(\psi_s) = \mathbf{E}_s$. Imposing the electric field continuity condition at the boundary between the inversion and ionized layers, $\mathbf{E}_{\mathrm{IV}}(\psi_U) = \mathbf{E}_2$, yields

$$\mathbf{E}_s = \sqrt{\mathbf{E}_2^2 + \frac{2qn_iU_T}{\varepsilon_{si}}\left(e^{\frac{\psi_s - V_{ch}}{U_T}} - e^{\frac{\psi_U - V_{ch}}{U_T}}\right)}, \tag{18}$$

where for a given temperature and doping concentration, $\mathbf{E}_2$ can be obtained from the electric field continuity condition, $\mathbf{E}_{\mathrm{III}}(y_2) = \mathbf{E}_2$, and is given by

$$\mathbf{E}_{s,\mathrm{depl}} = \mathbf{E}_2 = \mathbf{E}_1 - \frac{qN_A}{\varepsilon_{si}} t_{\mathrm{III}} \tag{19}$$

Next, the Gauss law links the electric field at the interface to the sum of the charge densities in the different layers:

$$-\varepsilon_{si}\mathbf{E}_s = Q_{\mathrm{II}} + Q_{\mathrm{III}} + Q_{\mathrm{IV}} \tag{20}$$

Therefore, the mobile charge density per unit area, Q_m, is given by $Q_m = -\varepsilon_{si}\mathbf{E}_s - Q_{\mathrm{II}} - Q_{\mathrm{III}}$. Relying on this relation and drift-diffusion transport, analytical expressions for the drain-to-source current, slope factor, and subthreshold swing are derived in the linear regime, and compared with the cryogenic measurements in the next section.

C. Drain current, slope factor, and subthreshold swing

Relying on the drift-diffusion transport mechanism [34], for small drain-to-source voltage, V_{DS}, the drain current is expressed as $I_{DS} = \mu(W/L)Q_m V_{DS}$, with μ the electron-carrier mobility, assumed constant along the channel. The total drain current obtained from the measurements at 4.2 K and

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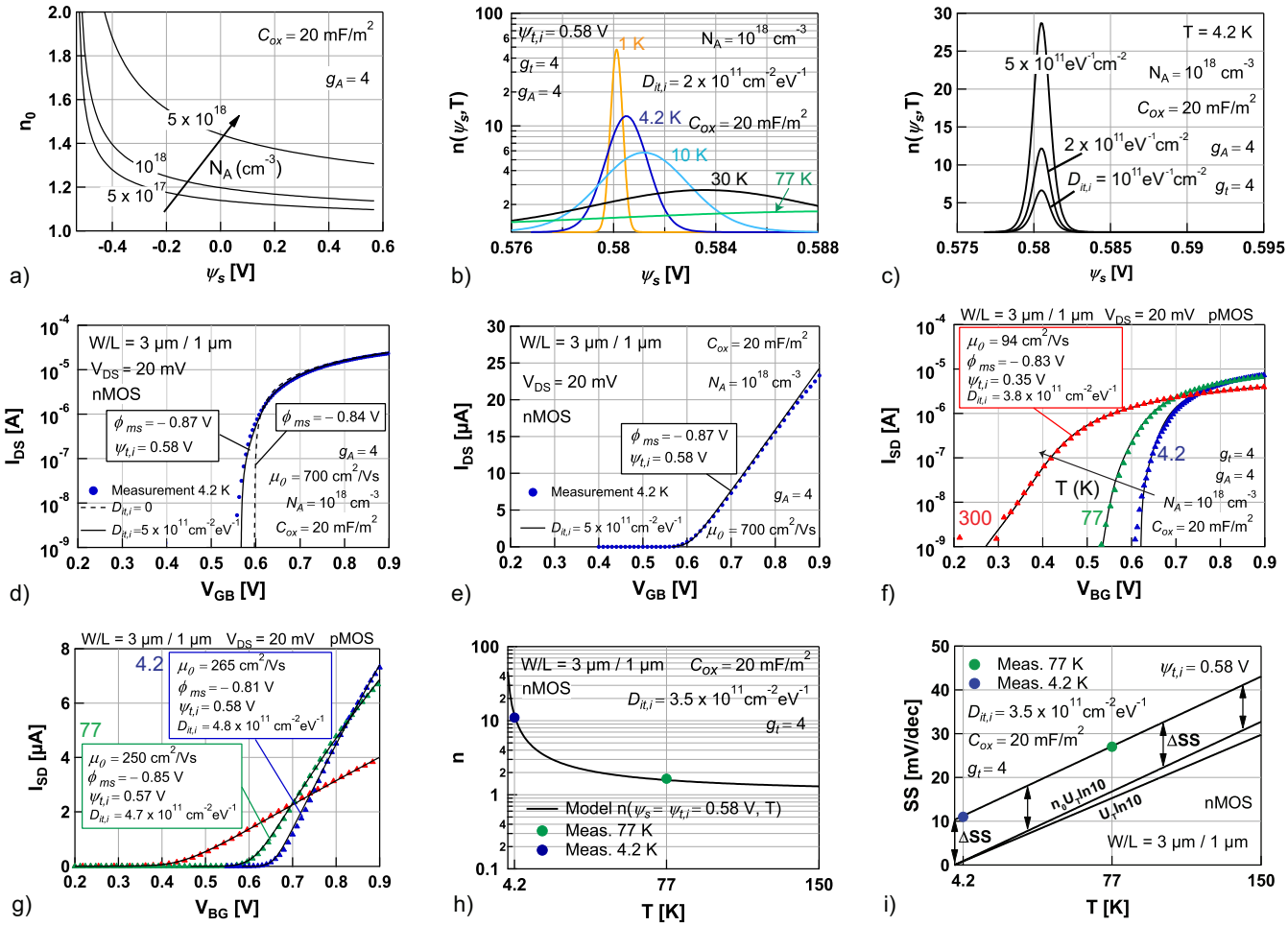

Fig. 6. Physics-based modeling the degradation of the subthreshold swing at deep-cryogenic temperatures, a) Slope factor without interface traps, n_0, cannot exceed 1.4 for long devices doped below the degenerate limit and operating in inversion mode ($\psi_s > 0.4$ V), b) Temperature-dependent slope factor, n, with one interface trap ($\psi_{t,i} = 0.58$ V) at 1, 4.2, 10, 30, and 77 K, exceeding a value of 10 at 4.2 K for $D_{it,i} = 2 \times 10^{11}$ eV^{-1} cm^{-2}, c) Temperature-dependent slope factor n at 4.2 K for increasing $D_{it,i}$-values ($\psi_{t,i} = 0.58$ V), d) Comparison of the measured linear transfer characteristics of nMOS $W/L = 3\,\mu\text{m}/1\,\mu\text{m}$ at 4.2 K (in log-scale) and the model without interface traps (dashed line) and with an interface trap at $\psi_{t,i} = 0.58$ V (solid line), e) Model from (d) with interface trap (solid line) plotted in linear scale. Mobility reduction at high V_{GB} is not included, f)-g) Model validation in logarithmic (f) and linear (g) scales at 4.2, 77 and 300 K for pMOS $W/L = 3\,\mu\text{m}/1\,\mu\text{m}$ in the linear regime (V_{DS}=20 mV, see Fig.1g). Markers indicate the measurements and solid lines denote the derived physics-based model. Insets show the used physical model-parameters at 4.2, 77 and 300 K. In addition, the used mobility reduction factor, θ, is 0.4 (4.2 K), 0.8 (77 K), and 0.35 (300 K). The used charge-threshold voltage, V_t, is 0.8 V (4.2 K), 0.7 V (77 K) and 0.6 V (300 K), h) Interface trapping explains the observed increase of n (markers, Fig.2b) by a hyperbolic temperature dependency ($\propto 1/U_T$), i) Theoretical limit of the subthreshold swing down to deep-cryogenic temperatures, $SS = n_0 U_T \ln 10 + \Delta SS$, where n_0 is the slope factor without interface traps (not exceeding 2), and ΔSS the shift due to interface charge traps assuming a temperature-independent $D_{it,i}$-value. Markers denote the extracted SS-values from the measurements at 77 and 4.2 K in Fig.2a.

from the proposed model are compared in Fig. 5f for nMOS $W/L = 3\,\mu\text{m}/1\,\mu\text{m}$ at $V_{DS} = 20$ mV. Markers denote the measurements, and the solid and dashed lines are respectively corresponding to the model assuming complete ionization ($g_A = 0$) or including incomplete ionization ($g_A = 4$). The electron mobility is assumed constant over the effective value of gate voltage ($\mu = 700\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$). As it can be understood from this figure, the degradation in subthreshold swing from its theoretical value (0.8 mV/dec) to the measured 11 mV/dec, cannot be explained by including incomplete ionization in the model. Since Boltzmann statistics is still valid at deep-cryogenic temperatures [34], the subthreshold swing, SS is given by $U_T \ln 10(\partial V_{GB}/\partial\psi_s)$ where $\partial V_{GB}/\partial\psi_s$ corresponds to the slope factor, n_0, obtained by $1+\varepsilon_{si}(\partial \mathbf{E}_{s,\text{depl}}/\partial\psi_s)/C_{ox}$ with $(\partial \mathbf{E}_{s,\text{depl}}/\partial\psi_s) = \sqrt{2qN_A/\varepsilon_{si}}/(2\sqrt{\psi_s - \psi_A + \eta})$ and $\eta = \mathbf{E}_1^2\varepsilon_{si}/(2qN_A)$. As observed in Fig. 6a, in inversion mode this slope factor cannot exceed two, when the semiconductor is doped below the degenerate limit. Moreover, even though the slope factor depends on η, it does not strongly depend on temperature. However, relying on $SS = n_0 U_T \ln 10$, n_0 is required to be around 10 to obtain the degradation in subthreshold swing. As we will discuss, this degradation can be explained by the temperature-dependent occupation of the interface charge traps. The gate-to-bulk voltage is linked to the flatband potential, V_{FB}, through the dielectric displacement vector continuity, $V_{GB} = V_{FB} + \varepsilon_{si}\mathbf{E}_s/C_{ox} + (\psi_s - \psi_b)$, with $V_{FB} \triangleq \phi_{ms}$, where ϕ_{ms} is the metal-semiconductor work function. Including the interface charge traps, this link is modified to $V_{FB} = \phi_{ms} - Q_{it}/C_{ox}$ where $Q_{it} = -q\int_{E_v}^{E_c} D_{it} f(E_t) dE_t$ with D_{it} the density-of-interface-trap-states per unit area and energy [35]. Here, a single-trap analysis is performed close to the conduction band to show

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the impact of interface charge traps on DC characteristics at 4.2 K (i.e. drain current, SS). Therefore, Q_{it} can be rewritten as $Q_{it} = -qD_{it,i}f(E_{t,i})$ for a single trap energy level, $E_{t,i} = -q\psi_{t,i}$, and $f(E_{t,i}) = 1/\{1 + g_t \exp[(E_{t,i} - E_{F,s})/kT]\} = 1/\{1 + g_t \exp[(\psi_{t,i} - \psi_s)/U_T]\}$, and g_t is the trap degeneracy factor [43]–[45]. Therefore, in the depletion region one can write

$$n(\psi_s, T) \triangleq \frac{\partial V_{GB}}{\partial \psi_s} = 1 + \frac{\varepsilon_{si}}{C_{ox}}\sqrt{\frac{2qN_A}{\varepsilon_{si}}}\frac{1}{2\sqrt{\psi_s - \psi_A + \eta}} + \frac{qD_{it,i}}{C_{ox}}\frac{1}{U_T}\frac{g_t \exp[(\psi_{t,i} - \psi_s)/U_T]}{\{1 + g_t \exp[(\psi_{t,i} - \psi_s)/U_T]\}^2} \tag{21}$$

Here, a strong hyperbolic temperature-dependency ($1/U_T$) appears on the RHS of (21) in the additional term due to interface charge traps. The slope factor obtained from (21) is plotted versus ψ_s in Fig. 6b for different cryogenic temperatures, and $\psi_{t,i} \approx 0.58\,\mathrm{V}$, which is very close to the conduction band edge. As illustrated in this figure, for a critical value of ψ_s, the slope factor n can exceed two, for a reasonable value of $D_{it} = 10^{11}\,\mathrm{eV^{-1}\,cm^{-2}}$. Note that the peak does not appear exactly at $\psi_{t,i} = 0.58\,\mathrm{V}$ due to the trap degeneracy factor g_t. Moreover, the position and the value of this peak change with temperature. Fig. 6c shows the slope factor n with respect to ψ_s at 4.2 K for different $D_{it,i}$-values and $\psi_{t,i} = 0.58\,\mathrm{V}$.

Each interface trap will yield a subthreshold swing degradation only at a critical value of $\psi_s = \psi_{t,i}$. Even though multiple interface traps, or a continuous distribution of interface traps, may contribute to the subthreshold swing degradation, one single trap level is already sufficient to explain the DC characteristics at cryogenic temperature by the proposed model, as evidenced by Figs. 6d and 6e for nMOS $W/L = 3\,\mu\mathrm{m}/1\,\mu\mathrm{m}$ at 4.2 K. In addition, it should be noted that the deviation at high V_{GB} in Fig.6e can be modeled by the mobility reduction due to the vertical field, given by $\mu = \mu_0/[1+\theta(|V_{GB}|-V_t)]$, where μ_0 is the low-field mobility, θ the mobility-reduction factor, and V_t the charge-threshold voltage. Including the mobility reduction, Figs. 6f and 6g for pMOS $W/L = 3\,\mu\mathrm{m}/1\,\mu\mathrm{m}$ at 4.2, 77, and 300 K demonstrate the excellent agreement between the proposed model and the measurement results in the linear regime in both linear and logarithmic scales. Note that the physical model-parameters $\psi_{t,i}$ and $D_{it,i}$ are temperature dependent. With decreasing temperature, $\psi_{t,i}$ lies closer to the conduction-band edge, and $D_{it,i}$ is found to increase slightly based on this single-trap analysis. Fig. 6h shows the hyperbolic temperature-dependency of the slope factor from (21) at $\psi_s = \psi_{t,i} = 0.58\,\mathrm{V}$. This $1/T$ dependence was initially described by Tewksbury in [46] using an empirical model that could accurately fit measured data thanks to a fitting parameter. He attributed this additional $1/T$ term to the combined effects of increased D_{it}, surface potential non-uniformities and surface quantization [46]. In this work we could derive this $1/T$ behavior analytically and identify Tewksbury's fitting parameter. Plugging (21) into $SS = n(\psi_s, T)U_T \ln 10$ leads to the subthreshold swing in terms of two components: (i) $U_T \ln 10$ times the slope-factor without interface traps, n_0, and (ii) an offset, ΔSS, depending on D_{it},

$$SS = n_0 U_T \ln 10 + \Delta SS, \tag{22}$$

with $\Delta SS = (qD_{it,i}/C_{ox})[g_t/(1+g_t)^2]\ln 10$, which is about 10 mV/dec for $D_{it,i} = 3.5 \times 10^{11}\,\mathrm{eV^{-1}\,cm^{-2}}$ ($g_t = 4$ and $C_{ox} = 20\,\mathrm{mF\,m^{-2}}$). As illustrated in Fig. 6i, this model explains the measured SS-deviation from the thermal limit of $\approx$ 10 mV/dec at 77 K and 4.2 K due to interface traps only. Moreover, it should be highlighted that in (22), the D_{it}-value does not become multiplied with $U_T \ln 10$, due to $1/U_T$ in (21). This leads to a lower extracted D_{it}-value at 4.2 K (i.e. $D_{it} = 3.5 \times 10^{11}\,\mathrm{eV^{-1}\,cm^{-2}}$ in Fig. 6i) than when the temperature-dependency of interface-trap-occupation is not included ($D_{it} \approx 10^{13}\,\mathrm{eV^{-1}\,cm^{-2}}$, see e.g. [47], [48]). Furthermore, the model would predict a SS-degradation even at subkelvin temperatures in the zero-Kelvin-limit when $n_0 U_T \ln 10$ is extremely small, for a D_{it}-value which does not have to exceed $10^{13}\,\mathrm{cm^{-2}}$. Therefore, the minimum subthreshold swing is set by the temperature-independent term, $SS_{T\to 0\,\mathrm{K}} = \Delta SS$, and ultimately limits the minimum voltage swing to 8 ΔSS = 80 mV which is close to the 100 mV predicted by Tewksbury [46]. This achievable minimum will certainly impact the design and implementation of quantum computing control circuits where the power consumption and generated heat dissipation close to the qubits are crucial.

V. Conclusion

A commercial 28 nm bulk CMOS process is characterized using experimental measurements down to 4.2 K. The DC characteristics are modeled using the empirical simplified EKV model. This model is able to fit the large-signal and small-signal characteristics measured at cryogenic temperatures very well using only four parameters. However, because the simplified EKV model is empirical, it cannot predict the strong degradation of the subthreshold swing appearing at 4.2K and leading to a substantial increase of the slope factor n (typically 33 for a short-channel nMOS). This increase in n strongly mitigates the current that can be saved to achieve the same transconductance or transit frequency when reducing the temperature from RT to 4.2 K. A physics-based model is then developed to better predict this effect. The proposed model, validated by experimental results, explains the subthreshold swing degradation by including the temperature-dependent occupation of interface charge traps. Incomplete ionization does not affect the subthreshold swing due to complete field-assisted ionization. The presented physics-based model provides the core of a future cryo-compact model, enabling the design and simulation of cryo-CMOS circuits for quantum computing systems.

Appendix

Multiplying both sides of (5) with $2(\partial\psi_{\mathrm{II}}/\partial y)$, rewriting the LHS as $\partial/\partial y[(\partial\psi_{\mathrm{II}}/\partial y)^2]$, integrating from y_b to y in layer II, and using $\mathbf{E}_{\mathrm{II}} = -\partial\psi_{\mathrm{II}}/\partial y$ with $\mathbf{E}_b = 0$, leads to equation (6). Equation (7) can be obtained by rewriting (6) in the format $d\psi_{\mathrm{II}}/\sqrt{} = -\kappa dy$. Integrating both sides, the left integral gives the $\arctan$.

Using the Maxwell-Boltzmann approximation for $f(E_A)$, the charge density per unit area in the freeze-out layer is

$$Q_{\mathrm{II}}(y) = -\frac{qN_A}{g_A}\int_{y_b}^{y} e^{\frac{\psi_{\mathrm{II}}(y) - \psi_A}{U_T}} dy \tag{23}$$

Using the expression for $\psi_{\mathrm{II}}(y)$ (7) and then integrating (23), results in equation (10).

Multiplying both sides of (16) with $2(\partial\psi_{\mathrm{IV}}/\partial y)$, rewriting the LHS as $\partial/\partial y[(\partial\psi_{\mathrm{IV}}/\partial y)^2]$, integrating from 0 to y in layer IV, and applying the surface boundary condition, $\mathbf{E}_{\mathrm{IV}}(0) = \mathbf{E}_s$, leads to equation (17).

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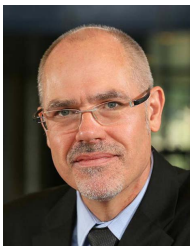

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