A 512×512 SPAD Image Sensor with Built-In Gating for Phasor Based Real-Time siFLIM

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Introduction

Fluorescence imaging is a widely adopted technique in various scientific disciplines for mapping chemical and biological characteristics or molecular interactions in cells by generating high contrast images in a non-invasive way. Recently, fluorescence lifetime imaging microscopy (FLIM) has become a practical alternative to fluorescence intensity thanks to affordable pulsed laser sources and counting electronics. FLIM has several advantages over simple intensity imaging. Specifically, fluorescence lifetime is strongly dependent on the molecular environment but very little on concentration or excitation intensity [1]. In most FLIM setups, a histogram of photon arrival times is constructed and fluorescence lifetime is extracted using various fitting algorithms (Fig. 1). This process is time consuming, especially with multiexponential decays, often a bottleneck to real-time imaging.

Phasors and siFLIM

The phasor method has recently emerged as an intuitive visual representation in FLIM, which is appealing in applications such as FRET analysis [2,3]. In phasor analysis, histogram calculation and fitting algorithms are replaced by simple algebraic calculations with the arrival time which result in a simple two-dimensional representation (Fig. 1 and Fig. 2). Time-correlated single-photon counting (TCSPC), the most common method used in FLIM, can extract fluorescence lifetime with high accuracy, as state-of-the-art time-to-digital converters (TDCs) can achieve resolutions of a few picoseconds. The use of this method in extracting phasors (Fig. 3) for wide field single-photon counters, however, is challenging due to the fill factor and frame rate restrictions imposed by in-pixel and per-column TDCs.

Sensor Architecture

We present a SPAD image sensor with in-pixel time gate to perform phasor-based FLIM measurements. This work potentially allows the execution of the phasor method in real time in hardware and, using a simplified 2-gate scheme described by Raspe et al. [4], a single-image FLIM (siFLIM) version of the technique can also be implemented, thus achieving the promised speedup at minimal loss of accuracy (Fig. 4). This sensor consists of a 512×512 pixel array, the largest time-resolved SPAD image sensor presented to date (Fig. 5). The pixel, a simplified version of the digital pixel implemented in SwissSPAD [5], comprises the SPAD, quenching and recharge, a dynamic memory, and a column readout mechanism (Fig. 6). A total of 256 output lines (128 on each 512×256 mirrored half-array) shared by a group of 4 columns, transfer the data outside the chip. Designed in 0.18 μm process technology, it achieves better than 10% fill factor, up to 50% using microlenses [6]. The sensor employs a p-i-n SPAD, shown in Fig. 7 and Fig. 8, with a PDP of 40% at 550 nm and above 20% in the 400-650 nm range [7]. The SPAD dark count rate (DCR) at 3.3 V excess bias is 0.3 Hz/μm^2.

Device Specifications

The sensor will capture a 1-bit frame in 6.4 μs, achieving a simulated frame rate of 156 kfps. The time gate is expected to have a minimum length of 5 ns and a gate edge non-uniformity better than 150 ps (Fig. 9). The pixel supports excess bias voltages up to 6.5 V, a significantly higher value than the maximum operating voltage of the CMOS process, so as to enhance the PDP by another 30% at 550 nm [7]. Power consumption is expected to be 3.52 W at 20 MHz and 600 mW at 1 MHz gate frequency. An expected performance summary of the sensor is presented in Table 1 and compared to the state-of-

the-art. The precision of the phasor extractor was verified in simulation for a variety of gating conditions (Fig. 10). In our analysis, precision is defined as

$$Precision \equiv \frac{\tau}{\sqrt{\sigma\tau^2 + \Delta\tau^2}},$$

where τ and $\sigma\tau$ are the mean and standard deviation of acquired lifetime values, respectively, and $\Delta\tau$ is the accuracy of the lifetime extraction method determined by the quantization error [8]. The suitability of our sensor for siFLIM and phasor analysis will be demonstrated in quantitative characterization of biological samples, with special attention to fast biological processes that benefit from high-speed wide field visualization.

Conclusion

We present a time gated image sensor architecture with 512×512 pixels, the largest time-resolved SPAD array presented to date. Thanks to its low-noise, high-sensitivity SPAD array and its fast readout, this sensor will be compatible with real-time FLIM applications. The adaptation of the phasor method to long time gates will significantly reduce the demanding data processing requirements of FLIM; thus allowing the combination of high spatial resolution with high frame rate.

Acknowledgements

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$$f(t)=A\exp(-t/\tau)$$

$$t_{j+1}-t_j=h$$

N_j: photon count of gate number j

GL: gate length

(a)

(b)
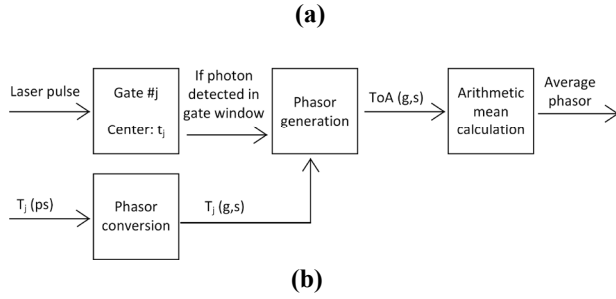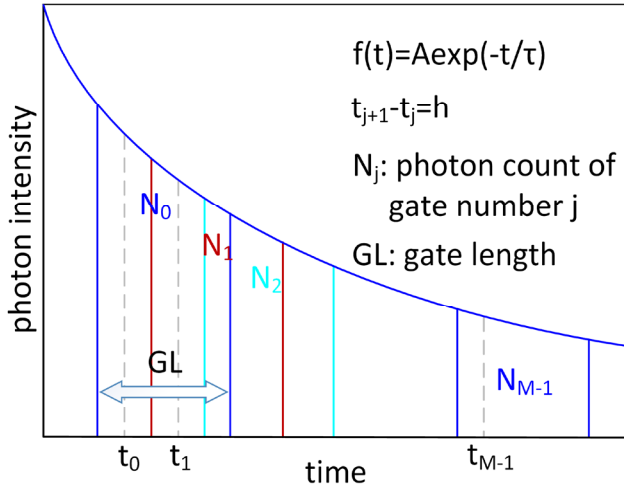
Figure 1: (a) Concept of time-gated FLIM with overlapping gates and (b) phasor analysis in time-gated FLIM

$$g = \cos(2\pi f\tau)$$
$$s = \sin(2\pi f\tau)$$
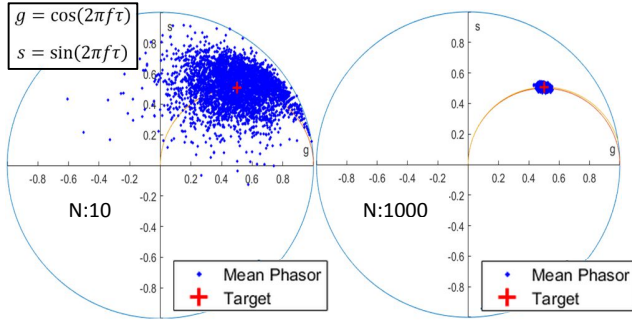
Figure 2: Conceptual diagram of the phasor-based FLIM method. Each point corresponds to the single-exponential FLIM data of one pixel in a homogeneous sample with lifetime of 950 ps (N: number of measurements, τ: photon ToA).
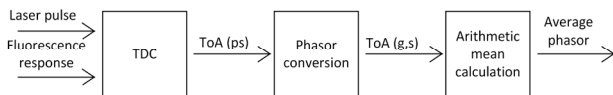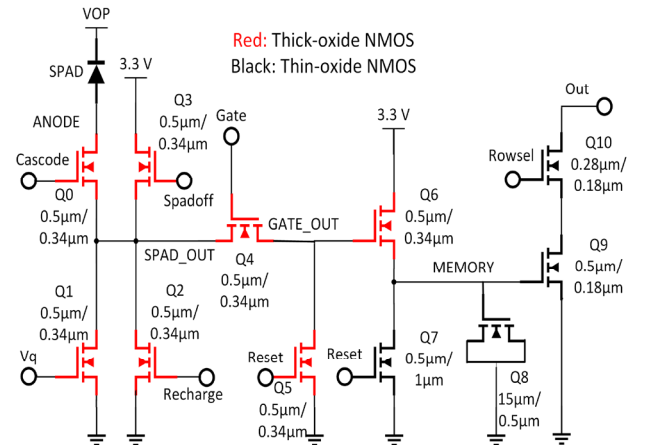

Figure 3: Phasor-based FLIM using TCSPC method
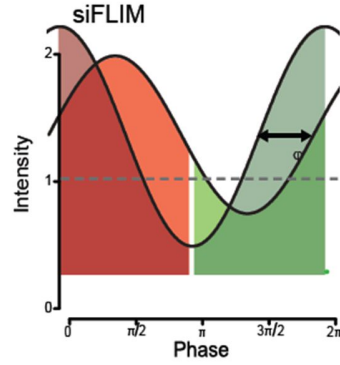
Figure 4: Principle of the single-image frequency-domain FLIM (siFLIM): Counting of photons in two gates with a phase difference of π [4]
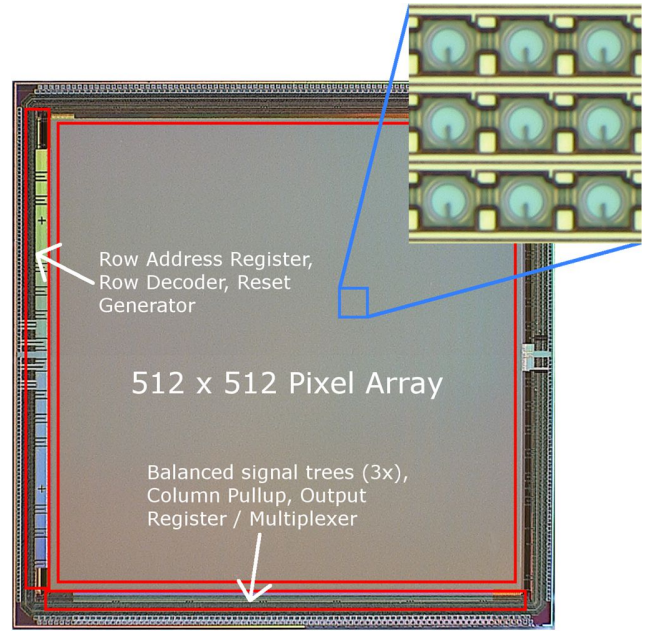


**Figure 5:** Micrograph of the 512×512 time-gated image sensor. Total size: 9.5×9.6 mm

Figure 6: Pixel schematic of the 512×512 time-gated SPAD image sensor

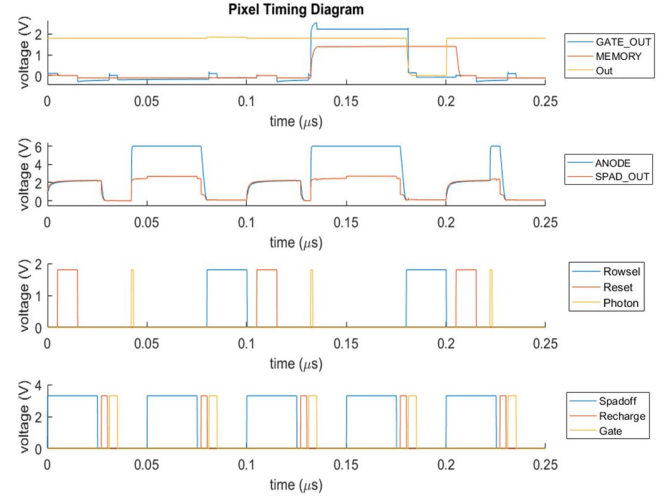|	[5]	[9]	[10]	[11]	This Work (v1)	This Work (v2)
Process	0.35 μm	0.13 μm	0.35 μm	0.35 μm	0.18 μm	0.18 μm
Array Size	512×128	320×240	100×100	160×120	512×512	512×512
Transistors Per Pixel	12	9	7 + 1 METALCAP	8	11	11
Pixel Pitch	24 μm	8 μm	25 μm	15 μm	16.38 μm	16.38 μm
Fill Factor	5%	26.8%	22%	21%	10.5%	13%

Table 1: Comparison table of state-of-the-art SPAD-based time-resolved pixels. Two versions of this work with round (v1) and square (v2) SPADs are presented.
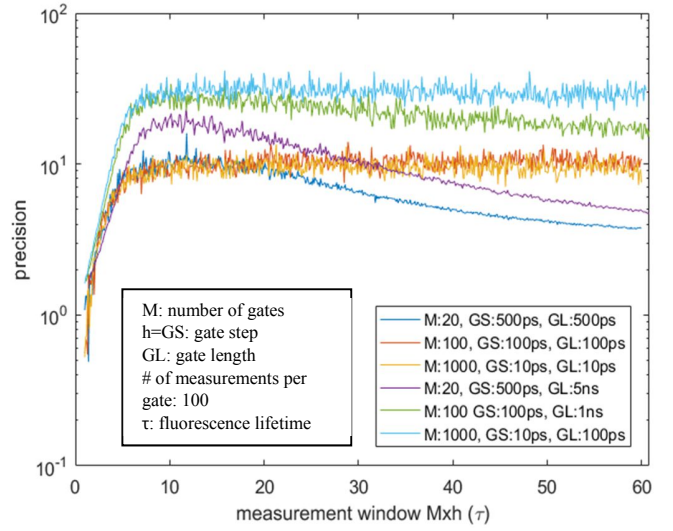

(a)   **(b)**
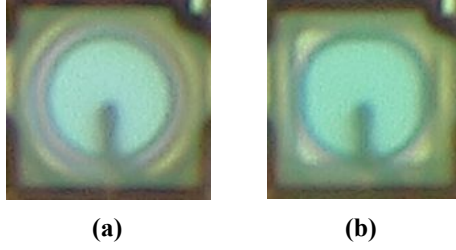
Figure 7: Micrograph of the (a) round SPAD (v1) and (b) the square SPAD with rounded corners (v2)

(a)

(b)

(c)
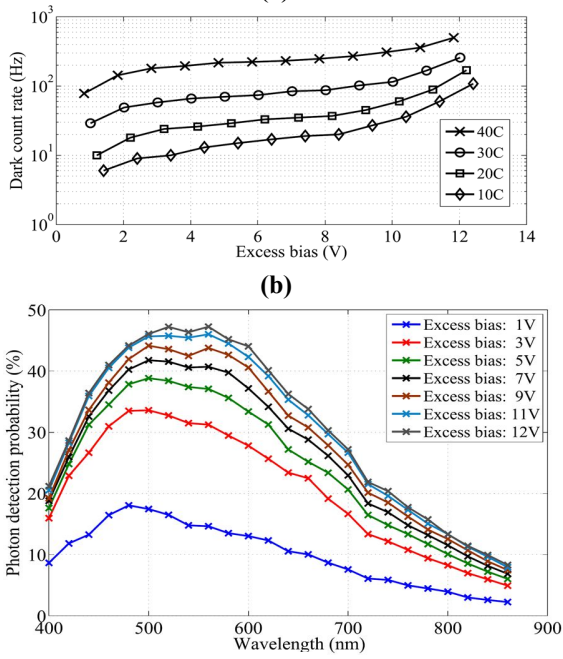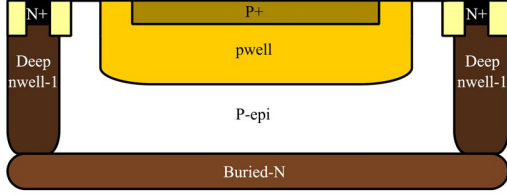
Figure 8: (a) Cross-section, (b) DCR and (c) PDP characterization of the p-i-n based SPAD used in the image sensor [7]

Figure 9: Timing diagram of the digital SPAD pixel with 1-bit dynamic memory

M: number of gates
h=GS: gate step
GL: gate length
# of measurements per gate: 100
τ: fluorescence lifetime

Figure 10: Precision of the time-gated phasor-based FLIM using non-overlapping (GL=GS) and overlapping (GL>GS) gates. For reliable results, M×h must be at least 5-10 times larger than τ. [8]