# Silicon Heterojunction Solar Cells: Recent Technological Development and Practical Aspects - from Lab to Industry

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**Abstract**

We review the recent progress of silicon heterojunction (SHJ) solar cells. Recently, a new efficiency world record for silicon solar cells of 26.7 % has been set by Kaneka Corp. using this technology. This was mainly achieved by remarkably increasing the fill-factor (*FF*) to 84.9 % - the highest *FF* published for a silicon solar cell to date. High *FF* have for long been a challenge for SHJ technology. We emphasize with the help of simulations the importance of minimised recombination, not only to reach high open-circuit voltages, but also *FF*, and discuss the most important loss mechanisms. We review the different cell-to-module loss and gain mechanisms putting focus on those that impact *FF*. With respect to industrialization of SHJ technology, we discuss the current hindrances and possible solutions, of which many are already present in industry. With the intrinsic bifacial nature of SHJ technology as well as its low temperature coefficient record high energy production per rated power is achievable in many climate regions.

*Keywords:* silicon heterojunction review, implied fill-factor, simulation

## 1. Introduction

In recent years, an increasing number of silicon solar cells were reported that feature energy conversion efficiencies greater than 25 % [1, 2, 3, 4, 5, 6]. One key element that these solar cells all have in common is that passivating contacts are used for charge carrier collection. Such contacts enable high efficiencies through the reduction of recombination by the displacement of the metal contact from the silicon surface. One possible approach is the use of silicon heterojunction (SHJ) contacts formed by the deposition of hydrogenated amorphous silicon (*a*-Si:H) layers on the surfaces of the silicon absorber. Combining intrinsic *a*-Si:H layers (*a*-Si:H(i)) that provide excellent defect passivation at the silicon surface in stacks with p- or n-doped *a*-Si:H, enables the formation of selective and passivating contacts. The achievement of fill-factors (*FF*) well above 80 % has been for long a challenge for SHJ solar cells in both academia and industry, while this was not the case for homojunction solar cells. Kinoshita *et al.* of the company Sanyo Corp. (now Panasonic Corp.) were the first to publish a *FF* above 80 % in 2011 [7]. As can be seen from Figure 1, at that time this was still 2 %$_\mathrm{abs}$ below the *FF* of the long-lasting world record obtained on a laboratory Passivated Emitter and Rear Contact[1] (PERC) solar cell (*FF* = 82.9 % [8]). It took until 2013 that Taguchi *et al.* from Panasonic Corp. published a SHJ solar cell with a *FF* of 83.2 % [9], exceeding the *FF* of the laboratory PERC cell. The efficiency of the cell reported by Taguchi *et al.*, however, was still below 25 % as a result of a relatively low short-circuit current ($J_\mathrm{SC}$). The most common approach to attain the highest possible $J_\mathrm{SC}$ of solar cells is to place both carrier collecting contacts at the rear side of the solar cell, avoiding both shadowing by the metal contact grid as well as parasitic absorption in the front contact layers. The latter is specifically limiting two-side contacted SHJ solar cells, due to the high absorption coefficient of *a*-Si:H in the visible spectrum. We discuss this issue ($J_\mathrm{SC}$ for two-side SHJ) in section 2.3.1.

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[1] Also referred to as Passivated Emitter and Rear Cell.

A challenge for back contacted SHJ solar cells is that only half of the wafer surface is available for contact formation. In combination with the general challenge to obtain low-ohmic contacts with SHJ this explains the reduction in $FF$ of the IBC-SHJ solar cell presented by Masuko *et al.* [2] compared with the previous SHJ record [9]. Still, the application of an all-back-contact architecture led to an increase in $J_{SC}$ and with an efficiency of 25.6 % set a new record for $c$-Si solar cells in 2014 [2].

In March 2017, Kaneka Corp. published their work on IBC-SHJ with the first silicon solar cell exceeding 26 % efficiency [10] with a $FF$ of 83.8 %. This high $FF$ was enabled by a series resistance of only $0.32\,\Omega\,\mathrm{cm}^2$, demonstrating that very low-resistive contacts can be achieved also with SHJ contacts. Later in 2017, further progress in efficiency was reported, culminating in 26.7 % [4]. This cell featured an even higher $FF$ of 84.9 %, enabled by its very low series resistance of only $0.2\,\Omega\,\mathrm{cm}^2$ [1]. To reach such high $FF$, not only transport losses have to be minimal but also recombination in low injection conditions, both in the silicon absorber as well as at its surfaces, needs to be sufficiently low [11]. These aspects were not covered in previous review articles [12, 13]. The impact of recombination in the silicon absorber on the $FF$ was covered by Leilaeioun & Holman, but the surface recombination was not considered in this paper [14].

Therefore, in this review, we put focus on recent progress of the $FF$ in SHJ solar cells. After introducing possible SHJ device architectures in section 2.1 we discuss the prerequisites to reach high $FF$ with the help of the simulation of implied $JV$ characteristics considering recombination both in the absorber and at its surfaces in section 2.2.2. In section 2.3 we review the loss mechanisms affecting the $J_{SC}$, $V_{OC}$, and $FF$ of SHJ devices, including resistive losses into our calculations (section 2.3.3). The impact of different interconnection technologies as well as binning of cells with slightly different JV characteristics on the $FF$ of a module is discussed in in section 3, while possible challenges for mass production are covered in section 4.
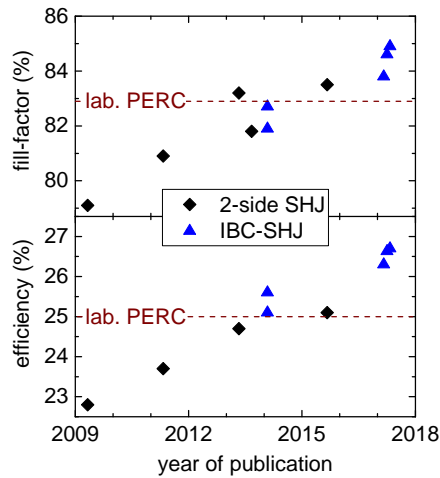
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Figure 1: Recent progress of efficiency and fill-factor for SHJ solar cells. For comparison, the long-lasting record of *c*-Si solar cells, a laboratory PERC cell [8], is included as dashed line.

## 2. SHJ solar cell devices

Silicon heterojunction solar cells consist of a crystalline silicon wafer that is passivated on both sides with stacks of intrinsic and doped hydrogenated amorphous silicon (*a*-Si:H) layers. As the conductivity of intrinsic *a*-Si:H is very low, its thickness should be as low as possible, but a minimum thickness has to be retained to provide sufficient surface passivation (cf. section 2.2.1). If at the front side[2], also the thickness of the doped *a*-Si:H layer should be as low as possible to reduce parasitic absorption (cf. section 2.3.1). To fully exploit the potential, high-quality silicon wafers featuring long charge carrier lifetimes have to be used. High efficiencies can be obtained on both doping types [15]. Nonetheless, most SHJ solar cells reported are based on n-type wafers due to its lower sensitivity towards impurities and the resulting superior charge carrier lifetimes [12].

With the very low surface recombination rates enabled by *a*-Si:H passivation, minority-charge-carrier lifetimes in the range of several milliseconds are obtained which enable open-circuit voltages well above 700 mV. At the front side, a metal grid is placed for charge carrier transport. Below the grid, usually a transparent conductive oxide (TCO) is needed to provide lateral conductivity. Other than with diffused junctions, the doped *a*-Si:H layers are laterally not conductive enough to fulfill this task. At the front side, the TCO serves also as an anti-refection coating (ARC). For stand-alone SHJ solar cells, its thickness is fixed to around 75 nm for optimal AR effect. When under glass, as in a module, this shifts to lower thickness.

### 2.1. Possible device architectures

To realize silicon heterojunction solar cells, different device architectures are possible of which the three most common are depicted in Figure 2. All have in common that they are intrinsically bifacial, which can lead to 25-30 % higher energy yield[3] [16, 17]. In the front junction configuration (Figure 2 a), the minority charge carrier collecting contact is situated at the front side of the solar cell absorber. Here, the minority-charge-carriers are generated close to their collecting contact, which enables higher short circuit current density for short-lifetime absorber material. While this is explaining why the front junction configuration is currently the most widely-used one in industry (Al-BSF are such cells), it is of less importance for SHJ solar cells. As long as minority charge carriers can reach their collecting contact, high current densities can be obtained regardless of the position of the minority-charge-carrier contact. High

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[2]The front side is the side facing the sun.

[3]Depending on site characteristics like albedo and row-to-row spacing.

charge-carrier lifetimes in the absorber and excellent surface passivation are a prerequisite to obtain this condition. Both are obtained in SHJ solar cells due to the excellent surface passivation of *a*-Si:H and the high-quality wafers used as absorber material.
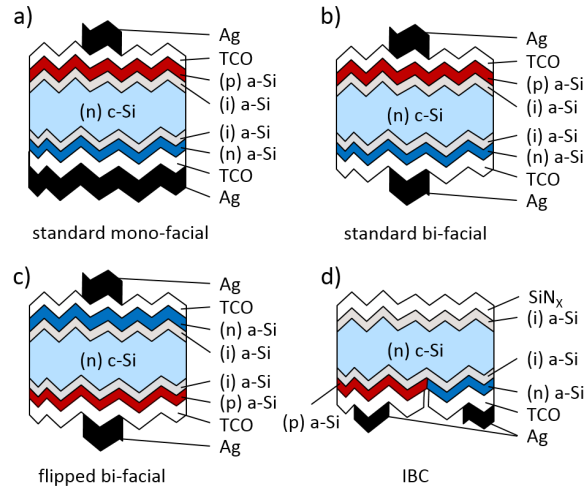


Figure 2: Device architectures for SHJ solar cells. a) Front junction mono-facial with minority-carrier-collecting contact on the front side, b) front junction bi-facial, c) rear junction bi-facial with minority-carrier-collecting contact on the rear, d) interdigitated back contacts (IBC) with charge carriers of both polarities collected on the rear side.

Therefore, SHJ solar cells enable other device architectures, including with a minority-carrier-collecting contact on the rear side (Figure 2 c). Regarding SHJ solar cells, the rear junction[4] configuration enables the use of less conductive, and therefore more transparent TCOs at the front side as lateral current transport can also take place in the wafer [19]. Furthermore, the contact formation for holes in SHJ is often considered to be more delicate compared with the electron contact [20]. Thus, placing the p-contact on the rear side enables the use of different materials i.e. thicker or more highly doped at the cost of transparency which would be a drawback in standard configuration. Despite this theoretical advantage, we would like to point out that the highest reported efficiency of a two-side contacted SHJ (which is the highest-efficiency two-side contacted large-area silicon solar cell) was obtained on an n-type wafer with the *a*-Si:H hole-contact at the front [10].

However, for both aforementioned configuration, even assuming that fully transparent materials could be engineered to form the front contact, still a front metal grid is needed, which will lead to current losses due to shadowing. In order to tap the full efficiency potential, both contacts have to be placed at the rear side of the solar cell. This, in addition, further broadens the spectrum of possible contact materials used as neither thickness nor transparency are limiting the choice. The most common approach to realise such a cell architecture is to form the contacts for both polarities in an interdigitated pattern at the rear side of the solar cell, described as interdigitated back contacts (IBC, Figure 2 c). The omission of the thickness restraint for the doped layers results also in an increased robustness towards sputter damage and can be beneficial for contact formation and band alignment [21, 22, 23, 24].

The major challenge for the industrial production of IBC devices is the cost-efficient formation of both contacts at the rear side of the wafer. Most IBC-SHJ devices reported so far rely on photolithography [25, 5, 26]. The *a*-Si:H layers are either structured by doping-selective etching in alkaline solutions [5, 26] or using additional layers as etching barriers [25]. Laser structuring in combination with sacrificial layers has also been investigated [27, 28] but so far reported efficiencies are below 20.6 % [27].

An approach that drastically reduces processing steps is the combination of in-situ shadow masking and the use of a recombination junction [29, 30, 31]. Using such recombination junction, one of the doped layers can be applied

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[4]Often referred to also as so-called "rear emitter" configuration. As "emitter" is a misnomer regarding PV [18], we use rear junction as identifier.

on the full area, reducing to two the number of patterning steps (one for one of the contact, one for the electrode) and one single alignment step [31]. In the case of this IBC configuration, only half of the area is available for charge collection, making contact resistance more problematic to reach low series resistance values. Yet, the excellent results recently obtained in several companies [32, 1, 5, 2] using an all-rear-contacted architecture indicate that this can be overcome.

### 2.2. Recombination dynamics in silicon solar cells

#### 2.2.1. Surface passivation with amorphous Silicon

The history of electronic-quality amorphous silicon can be traced back to the findings of Chittick *et al.* from 1968, when they demonstrated that intrinsic, highly resistive material could be grown from plasma-enhanced chemical vapour deposition (PECVD). The demonstration of doping by adding phosphorous and boron in the gas mixture enabled this material to be used in solar cells, initially as absorber and contact [33], later on as contact only for a silicon-wafer-based solar cell in the heterojunction architecture. Excellent passivation relies on atomically sharp interfaces between the crystalline silicon wafer and the amorphous silicon layer. A high hydrogen content has also been shown as necessary for best passivation results [34, 35, 12]. The properties of recombination-active defects at the surface of an $a$-Si:H-passivated wafer were studied in details in recent years, revealing that they are similar to bulk defects in $a$-Si:H [36, 37]. This is linked to the fact that, for thin layers, the charges photogenerated in the silicon wafer are sensitive to the defects through the whole bulk of the $a$-Si:H layer, the surface defect density ($D_{it}$) corresponding to the projected defect density of the film [36]. In recent years, the effect of light illumination on the passivation properties of $a$-Si:H layers was studied and its kinetics revealed, with clear indication that the effect of light soaking depends on the passivating structure, passivation from intrinsic layers being prone to light-induced degradation, whereas passivation from stacks of intrinsic and doped layers are prone to light-induced improvement [38, 39, 40].

#### 2.2.2. Influence of charge carrier lifetime on device performance

The device performance depends strongly on charge carrier lifetime. Knowing the injection dependent recombination of the solar cell device is important, especially for the optimization of solar cells with passivated contacts. The upper limits for fill-factor and open-circuit voltage are set by charge carrier recombination and are referred to as implied values - *iFF* and *iV*$_{OC}$. If there are no further losses, the parameters *FF* and *V*$_{OC}$ are equal to *iFF* and *iV*$_{OC}$. Ideally, recombination through defect states in the absorber and at its surfaces is so low that $iV_{OC}$ and $iFF$ are limited by intrinsic recombination i.e. Auger and radiative recombination. In Figure 3, we show the impact of recombination in the absorber (Figure 3 a) and at its surfaces (Figure 3 b) on the implied values of $V_{OC}$, $FF$, and efficiency, as obtained from the simulation of injection dependent charge carrier lifetime. Details on the simulation can be found in Appendix A.2.

Regarding the **open-circuit voltage**, the trap density in the bulk $N_{trap}^{bulk}$ needs to be sufficiently low to allow for charge carrier lifetimes $\tau_{SRH}^{bulk}$ of at least 2 ms in order that $V_{OC}$ is close to the intrinsic limit. This limit depends on the doping density in the absorber and decreases with increasing doping density. For lower lifetime absorber material ($\tau_{SRH}^{bulk}$<500 μs), a higher doping density allows for higher $V_{OC}$ as can be seen in Figure 3. This is explained by the position of the quasi-fermi level of the majority charge carriers, which is shifted closer to the band-edge, allowing for higher $V_{OC}$. This can be also beneficial for thinner absorbers, when long diffusion lengths are not mandatory [41].

Also recombination at the surfaces can limit the $V_{OC}$ and is characterised by an interface state density[5] $D_{it}$ and a fixed charge $Q_f$. For the simulations in this paper we chose identical $D_{it}$ and $Q_f$ for both surfaces. For typical values of $Q_f$ as chosen for the example shown in Figure 3, $iV_{OC}$ follows a similar trend versus $D_{it}$ as for a variation of $N_{trap}^{bulk}$.

The implied **fill-factor** *iFF* deviates earlier (for lower defect densities) from its intrinsic limit compared with the $iV_{OC}$. This can be seen from Figure 3, for both recombination in the absorber as well as at its surfaces. The

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[5]For our simulations, the term surface state density would be more concise. However, as in SHJ devices the absorber's surfaces are interfaces to the $a$-Si:H layers, we chose the term $D_{it}$. Note, that the absolute values of $D_{it}$ depend also on the chosen capture cross sections - we use here the values of ref. [42], summarised in table A.2 in the appendix.
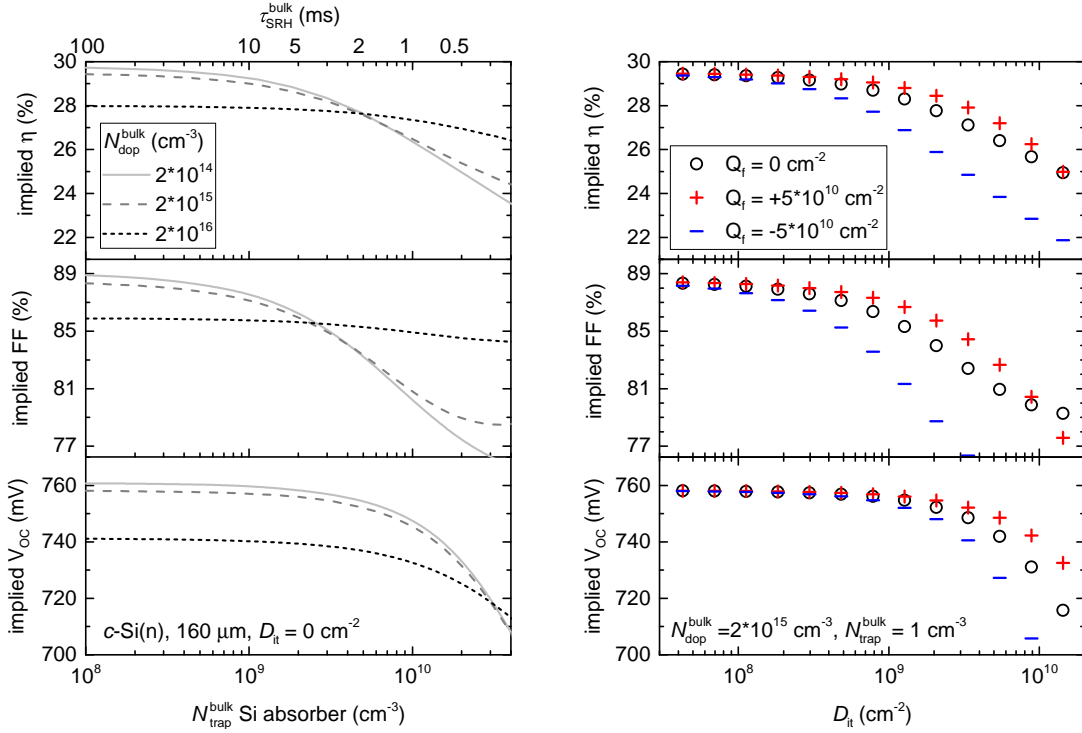
Figure 3: Efficiency, fill-factor and $V_{OC}$ of implied $JV$-curves, calculated from charge carrier lifetime. (a) For different defect concentrations and doping concentrations in an $n$-type silicon absorber. (b) For different interface state densities $D_{it}$ and surface fixed charge densities $Q_f$, assuming identical conditions for both absorber surfaces.

prerequisites to reach a high $iFF$ are therefore more demanding. While for $iV_{OC}$, a $\tau_{SRH}^{bulk}$ of >2 ms is sufficient to be limited by intrinsic recombination, for $iFF$, $\tau_{SRH}^{bulk}$ needs to be >5 ms. Similarly, $D_{it}$ needs to be kept at a minimum to ensure high $iFF$. Low defect recombination is thus primarily important to obtain a high $iFF$, as e.g. also pointed out by Adachi *et al.* [11].

## 2.3. Loss mechanisms and mitigation strategies

### 2.3.1. Short-circuit current density

Two-side contacted SHJ solar cells suffer intrinsically from short-circuit current losses due to **reflection at the front-contact grid**. These losses are eventually defined by the metalization technique used, as the ideal geometry of the grid depends on the minimum possible finger width and the resistivity of the lines. Using e.g. fine line double stencil printing, finger widths down to 36 μm [43, 44] are possible, while even narrower lines down to 15 μm can be achieved using plating techniques [45, 11]. Additionally, the sheet resistance of the TCO affects the ideal geometry as a lower sheet resistance allows for wider finger spacing. Yet, if the lower sheet resistance is achieved by increasing the carrier density, this induces higher parasitic absorption from free carriers, referred to as free-carrier absorption (FCA), specially for photons with wavelengths beyond 800 nm. At the front side, this can be mitigated using high mobility TCOs such as IO:H [46, 47] or ICO:H [48, 49] that provide a sufficiently low sheet resistance despite a low free carrier density.

Besides reflection, **parasitic absorption** is an important current loss mechanism for two-side SHJ solar cells. At the **front-side**, photons are absorbed in the $a$-Si:H and TCO layers. Holman *et al.* state a $J_{SC}$ loss of 2 mA cm$^{-2}$ in the wavelength range between 300 nm and 800 nm due to parasitic absorption at the front-side for a typical SHJ solar cell [50] with ITO as TCO. While charge carriers generated in the doped $a$-Si:H can be considered as fully lost due to the short diffusion length in the material, it is reported that at least parts of the carriers generated in the $a$-Si:H(i)

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158 layer are injected in the *c*-Si absorber and thus contribute to $J_{SC}$ [50, 51, 52] Holman *et al.* estimate that 30 % of the
159 carriers contribute to $J_{SC}$ [50], while Paduthol *et al.* report even 40 % [52].

160     The general guideline to avoid parasitic absorption losses at the front is to reduce the optical thickness $k \cdot t$,
161 i.e. either reduce the thickness $t$ or the extinction coefficient $k$ of the front contact layer. A reduction of $k$ can be
162 achieved by alloying *a*-Si:H with other elements such as carbon [53, 54] or oxygen [55, 56], to increase the band
163 gap. Unfortunately, in the case of *a*-SiO$_x$(n), the doping efficiency is reduced with increasing oxygen content [57]
164 and thus conductivity is decreased. As a result, the $J_{SC}$ gain is counterbalanced by a loss in *FF* and no efficiency gain
165 is achieved. More promising might be the application of a two-phase material such as nanocrystalline silicon oxide
166 (*nc*-SiO$_x$:H). In such a material, a columnar nanocrystalline silicon phase providing vertical conductivity is embedded
167 in an amorphous silicon oxide matrix providing enhanced transparency [58, 59]. For *nc*-SiO$_x$:H(n) at the front side
168 of a SHJ solar cell, a slightly higher efficiency compared with an oxide-free *nc*-Si:H(n) reference is reported [60, 61].
169 Also the use of nanocrystalline silicon (*nc*-Si:H) is an option [20, 62], due to the lower $k$ of *nc*-Si:H compared with
170 *a*-Si:H in the short wavelength range.

171     At the **rear side**, parasitic absorption of photons of IR wavelength can be reduced following the same approach, or
172 with an advanced rear reflector design incorporating a low-refractive index material such as MgF$_2$ as optical spacer to
173 reduce parasitic absorption of the evanescent wave in the back reflector. This apporach was proposed by Campbell *et*
174 *al.* [63] and further elucidated [64] as well as experimentally shown by Holman *et al.* [65].

175     In terms of $J_{SC}$ the ideal device architecture is the IBC-SHJ. The absence of front contact grid and TCO, as well as
176 the fact that front side layers with excellent passivation and no parasitic absorption can be realised, enables maximum
177 $J_{SC}$. A possible problem for IBC-SHJ is so called electrical shading [66, 67] which occurs when minority charge
178 carriers are generated far from their collecting contact and recombine due to insufficient effective diffusion length at
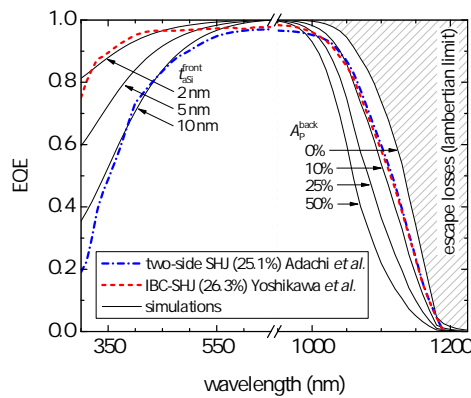179 the majority carrier contact or in the silicon absorber.



Figure 4: Experimental external quantum efficiencies (EQE) of a two-side contacted SHJ solar cell [11] and an IBC-SHJ [10]. Also shown are simulated curves assuming no reflection losses, and different levels of parasitic absorption at the front and at the rear, see Appendix A.1 for further details. Experimental EQE data with kind permission of Kaneka Corp.

180     In Figure 4 we show the external quantum efficiencies (EQE) of a two-side contacted and an IBC-SHJ solar cell.
181 The most striking difference is the absence of parasitic absorption in the range of 300 nm to 600 nm for the IBC-SHJ,
182 the absorber thickness for both cells is 160 µm. Also shown is the general impact of parasitic absorption in a front
183 *a*-Si:H layer and parasitic absorption in the IR, simulated with increasing parasitic absorption at the rear side of a
184 160 µm thick silicon absorber. Please refer to Appendix A.1 for more details.

### 2.3.2. Open-circuit voltage

186     To reach high open-circuit voltage ($V_{OC}$) in a silicon solar cell, two requirements need to be fulfilled:

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(i) defect recombination needs to be low, enabling high excess charge carrier density (that results in high implied $V_{OC}$ ($iV_{OC}$)), and

(ii) selectivity at electron- and hole-contacts needs to be sufficiently high in order to achieve charge carrier separation and as a result a potential difference between the contacts (high $V_{OC}$).

The high $V_{OC}$ is one of the key characteristics of solar cells with passivating contacts. For commonly used high quality silicon absorbers, the $V_{OC}$ is usually well above 700 mV and, for a good device, limited by intrinsic recombination (Auger & radiative) .

As generally in SHJ solar cells the $a$-Si:H layers are only several nanometers thin, the preservation of surface passivation after the $a$-Si:H deposition is a challenge. Subsequent processes as e.g. the TCO deposition can decrease the surface passivation. When sputtering is used for TCO deposition, ion bombardment and UV plasma luminescence create defects in the $a$-Si:H [68, 69, 70] which reduces the surface passivation. Depending on the process conditions during sputtering [70, 71], it can be possible to recover surface passivation with low-temperature ($\leq 200$ °C) annealing, however, in ref. [69] it was observed that the microstructure of the $a$-Si:H is irreversibly altered. Thicker $a$-Si:H can lead to a higher resistance against sputter damage [72] but is unwanted at the front side due to parasitic absorption. A protecting TCO layer applied prior to sputtering with a damage-free technique such as atomic layer deposition (ALD) can fully prevent $V_{OC}$ loss due to sputter damage when sufficiently thick [73]. Also other deposition techniques such as ion plating can be used to reduce ion bombardment during TCO deposition [48].

Only relevant for academia, where often multiple small ($< 9$ cm$^2$) solar cells are embedded in one wafer, the $V_{OC}$ of the measured cell can be reduced during the measurement of the $JV$-curve through a mask as in the perimeter region of the cell, no charge carriers are generated and charge carriers generated in the cell area diffuse in the dark perimeter region and recombine [74]. For a typical 4 cm$^2$ SHJ solar cell, when measured with a shadow mask the $V_{OC}$ is about 10 mV lower compared with a measurement with full-wafer illumination[6]. The effect is reduced with increasing area-to-perimeter ratio [75] and becomes negligible for typical SHJ cells with an area $> 9$ cm$^2$.

Regarding full-wafer solar cells as used in production or industry-oriented research, the passivation of the wafer edge becomes increasingly important the higher the $V_{OC}$ and efficiency of the solar cell. As an example, Kaneka Corp. reports on a SHJ cell on a full wafer (239 cm$^2$) with an efficiency of 25.6 % [76, page 6], while to further improve efficiency, they not only report on process improvements but reduced also the cell area to 152 cm$^2$, while still on a 6 inch wafer [11].

Besides sufficiently low recombination in the silicon absorber and at its surfaces to obtain a high excess charge carrier density, another requirement is to have contacts with sufficiently high selectivity for the respective polarity. This allows to reach high $V_{OC}$ values, matching the $iV_{OC}$. Selectivity is obtained when the contact features a high difference in conductivity for the two polarities [77]. For $a$-Si:H-based contacts, insufficient doping and/or mismatched TCO work function [22, 23, 78, 21, 24], or a combination thereof impede this conductivity asymmetry, and cause selectivity—hence $V_{OC}$—losses. A mismatched TCO workfunction will lead to a depletion of the doped layers at the interface between TCO and the doped layer (cf. band diagram in Figure 5). However, the parameter that is most affected in this case is the $FF$, as discussed in section 2.3.3.

### 2.3.3. Fill-factor

Losses in $FF$ of a silicon solar cell can be triggered by the same mechanisms as $V_{OC}$-losses:

(i) recombination, and

(ii) insufficient conductivity $\sigma_{e/h}$ of the respective contact's majority carrier.

Regarding the losses due to recombination, the same principles that impact $V_{OC}$, as e.g. sputter damage also impact the $FF$ by lowering the implied $FF$ ($iFF$) of the solar cell. As it leads to an increased $D_{it}$, sputter damage is more detrimental to the $iFF$ than to the $iV_{OC}$, as shown in section 2.2.2. Lifetime at implied open circuit is indeed limited by Auger recombination to lower values than at implied maximum power, making $iFF$ more sensitive to surface recombination than $iV_{OC}$. Regarding (ii), whereas for the $V_{OC}$ only the ratio $\sigma_e/\sigma_h$ of the conductivity of electrons

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[6]This is more pronounced if the perimeter region is electrically connected with a low resistance, as is e.g. the case for multiple rear junction cells when their rear metallization is connected via the measurement chuck during the $JV$ measurement.
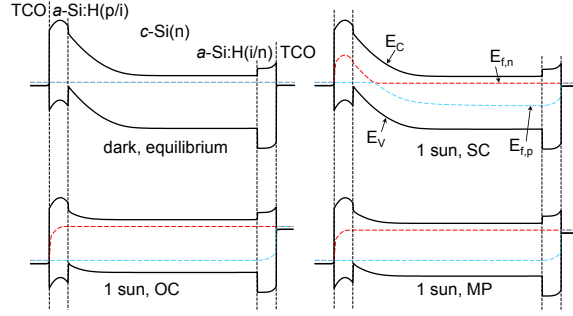
Figure 5: Energy band diagrams of a SHJ device in equilibrium, short-circuit (SC), open-circuit (OC), and maximum power (MP) conditions. With the conduction band edge $E_C$, valance band edge $E_V$ and the quasi-Fermi-levels $E_{f,n}$ and $E_{f,p}$ for electrons and holes respectively.

and holes at their respective contacts is important[7], for a high *FF*, the absolute values of $\sigma_e$ (at the electron-contact) and $\sigma_h$ (at the hole-contact) define if charge carrier transport is limited or not.

As can be seen in Figure 6, certain *FF* values can be obtained by different combinations of *iFF* and ohmic transport losses. For example, a *FF* of 83.3 % can be obtained assuming a wide range of series resistance values between $0\,\Omega\,cm^2$ and $0.9\,\Omega\,cm^2$, depending on charge carrier recombination dynamics and the resulting *iFF*. This is valid for both recombination in the absorber as well as at its surfaces. Yet, obviously, high *FF* can only be attained with a combination of low recombination and low series resistance.
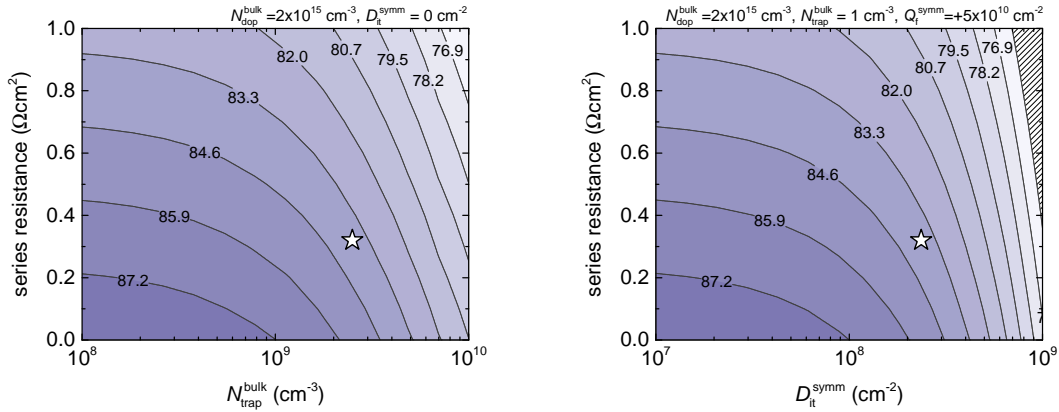


Figure 6: Contourplots of simulated FF. Left: for tau bulk limited case, right: for $D_{it}$ limited case, assuming $Q_f^{symm}=5 \times 10^{10}\,cm^{-2}$, $N_{trap}^{bulk}=1\,cm^{-3}$, both for $160\,\mu m$ n-type absorber. Star: data point of experimental IBC-SHJ device ($R_S =0.32\,\Omega\,cm^2$, *FF*=83.8 %, $\eta$=26.3 %) from ref. [10].

In experimental SHJ solar cells, transport limitations are often not fully ohmic and can also be dependent of charge carrier injection level and temperature. Their characterization and analysis of SHJ devices can thus be more challenging using classical analysis methods such as the two-diode model. These methods, however, can still be helpful when allowing e.g. for variable ideality factor *n* or recombination prefactor $J_0$.

A strong temperature dependence of transport in SHJ solar cells is caused when thermionic emission is limiting charge carrier transport. For example, when the *a*-Si:H(p) layer at the TCO/*a*-Si:H(p) interface is partly depleted (cf. Figure 5), efficient tunneling from *a*-Si:H(p) to the TCO is prevented, and a non-linear transport barrier is formed[8].

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[7]As there is no current flow in $V_{OC}$, the absolute value of the conductivity is not important. It is only important, that e.g. at the hole contact the conductivity for electrons is much lower than the one of holes, and vice versa.

[8]Such a barrier is often described also as "diode" or "counter-diode".

Tunneling has been shown to be needed when modeling the *a*-Si:H/TCO contact [24, 79] and is an important transport mechanism in SHJ solar cells. The *a*-Si:H layer depletion can occur due to a mismatched workfunction of the TCO [22, 23, 78, 79] and is enhanced by insufficient thickness [23] and/or doping of the doped *a*-Si:H layer [24, 22, 80, 81].

One way to counteract the formation of such a transport hindrance is the application of nanocrystalline[9] silicon (*nc*-Si:H) layers [62, 20, 61]. In this material, the fermi-level is closer to the valence or conduction band compared with *a*-Si:H due to its increased doping efficiency. This facilitates the contact formation with the TCO, as it reduces the width of the depletion region in the doped layer. It was reported by Nogay *et al.* that especially the hole contact (TCO/p) benefits from the increased conductivity [20], contact resistivities (for both electron and hole-contact) are reduced by a factor of three, and their temperature dependence becomes less pronounced.

## 2.4. Alternative materials for contact formation

In recent years a wide variety of novel materials have been investigated as carrier-selective contacts for silicon heterojunction solar cells. High-work-function metal-oxide lead the race for hole-selective contacts [82, 83, 84, 85] whereas low-work-function metal-fluorides or even metals are highly investigated electron-selective contacts [86, 85]. Most efficient devices use an intrinsic amorphous silicon layer for passivation [82, 85] though excellent results could also be obtained with simpler architectures, notably through the use of $TiO_2$ as electron-selective contact [86].

A strong limitation of most electron-selective contact approach is the need to use a low-work-function metal as the electrode leading to severe parasitic absorption of the IR light. This absorption is due to the absence of a dielectric spacing layer between the silicon wafer and the metal, leading to strong plasmonic absorption [87]. This effect is worsened by the fact that low-work-function metals such as aluminum typically exhibit a poor reflection contrarily to e.g. gold or silver. Yet, the need to use such a low-workfunction metal to allow an efficient carrier-selective contact stack shows that not only the contact layer but also the electrode play a strong role in the selectivity of a contact stacks.

On the hole-selective contact side, the most successful material has been slightly substoichiometric molybdenum oxide ($MoO_x$ with x close to 3) prepared by thermal evaporation. It is very notable that in this case, good solar cell results could be obtained even when this layer was capped with ITO, making it possible to exploit its transparency as a window layer. Its instability to post-deposition annealing, and to some extent to the electrode deposition make it difficult to integrate in devices, though some strategies seem promising to enhance its robustness. Also, possibly due to the narrow window of (sub)stoichiometry for which adequate conductivity, work function, and possibly defect density are obtained, no other technique than thermal evaporation was successful so far in reaching similar efficiency as with evaporated material in spite of multiple attempts [88, 89]. The stability is also a concern (and even more so) for electron contacts, with promising approaches usually incorporating $TiO_2$ [85, 86].

In addition to standard devices, IBC were also used for such contacts, with the possibility of very simple 2-evaporation-step processes, demonstrating remarkable efficiencies in spite of the absence of passivation layers [90]. Implementing a passivation layer, further improvements were made possible leading to even higher efficiencies [91].

Another approach closer to organics is the use of organic components, with PEDOT:PSS being the most successful hole-selective contact [92, 93], and dipole-inducing molecule being actively investigated as electron-selective contacts [94]. Such approaches have the advantage of typically not requiring a vacuum deposition tool, potentially enabling very inexpensive processing. Yet the use of liquid organic solutions is not straightforward on a textured surface, and the modest efficiencies shown so far do not appear sufficient to compete with traditional solar cell manufacturing solutions. The overall working principle of heterojunction solar cells using alternative materials appears still even more mysterious than silicon-based heterojunctions, with defect-assisted transport being thought as playing an important role [95].

## 2.5. Temperature dependence: theoretical limits & practical considerations

In Figure 7 we show the temperature dependence of $iV_{OC}$ and $iFF$ as obtained from our simulations. We assumed a perfectly passivated absorber in this case ($D_{it}= 0\,cm^{-2}$). $iV_{OC}$ and $iFF$ decrease both linearly with temperature, the

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[9]In literature, also the term microcrystalline is used for such materials. As grain-sizes are usually in the nanometer range in such materials, we use the term nanocrystalline.
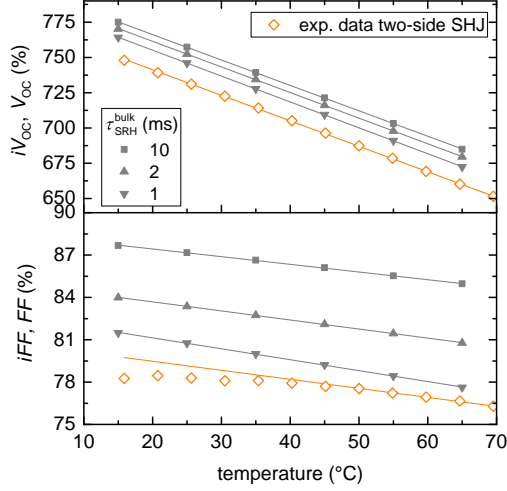
Figure 7: Filled grey symbols: Simulated $iV_{OC}$ and $iFF$ values versus temperature, assuming only recombination in the absorber. Orange open symbols: data of an experimental two-side SHJ solar cell, taken from ref. [96].

Table 1: Relative temperature coefficients of the data (simulation and experiment) shown in Figure 7, obtained from linear fitting between 15 °C and 70 °C. For the SHJ solar cell, the $TC_{FF}$ would amount to −0.08 % K$^{-1}$, when fitted only in the linear range of the curve (between 50 °C and 70 °C).

|  | $aTC_{V_{OC}}$ | $TC_{V_{OC}}$ | $TC_{FF}$ |
|---|---|---|---|
|  | mV K$^{-1}$ | % K$^{-1}$ | % K$^{-1}$ |
| sim. $\tau_{SRH}^{bulk}$ = 10 ms | -1.80 | -0.24 | -0.06 |
| sim. $\tau_{SRH}^{bulk}$ = 2 ms | -1.81 | -0.24 | -0.08 |
| sim. $\tau_{SRH}^{bulk}$ = 1 ms | -1.83 | -0.25 | -0.10 |
| exp. SHJ cell | -1.81 | -0.25 | -0.05 |

relative temperature coefficients obtained from linear fitting are given in Table 1. As well-known from literature, the $TC_{V_{OC}}$ increases with increasing $V_{OC}$ at 25 °C, the same holds true for $TC_{FF}$. The empirical models to describe $V_{OC}(T)$ and $FF_0(T)$ proposed by Green [97] describes the observed trends well as long as the ideality factor is taken into account. For the comparison with experimental data, we included also temperature-dependent $V_{OC}$ and $FF$ of a SHJ solar cell in the Figure. The experimental data has been published earlier [96]. While the $V_{OC}$ of the experimental cell follows a linear trend as the simulated data, the $FF$ versus temperature curve is only linear for temperatures above 50 °C. This can be seen from the linear fit between 50 °C and 70 °C that we extrapolated to lower temperatures. For temperatures below 50 °C, the $FF$ is lower than the extrapolated straight slope. This behaviour is typical for SHJ solar cells [98, 99, 20, 81] and due to thermally enhanced current transport. This temperature dependence leads to deviation from classical models for ohmic carrier transport, and is partly also responsible for the high[10] $TC_{FF}$. Note though that in the case of the current world-record IBC-SHJ solar cell ($FF_{25°C}$ = 84.9 %), we expect this effect to by negligible, i.e. linear behavior for temperatures above 25 °C in view of the very high $FF$ obtained at 25 °C. The remaining $R_S^{25°C}$ of probably[11] below 0.2 Ω cm$^2$ that could potentially be reduced at higher temperatures [100] is so

---

[10]The wording of high and low TC can be confusing as the TCs (except $TC_{J_{SC}}$) of silicon solar cells are usually negative. That means that a high absolute value of the TC is detrimental, but a high value (corresponding to a low absolute value) is beneficial for operation higher than 25 °C.

[11]The device with the highest efficiency (26.7 %) has so far been only reported in the efficiency tables 50 [32], where no value for $R_S$ is given. We assume that with an $R_S$ of 0.2 Ω cm$^2$ for a device with a $FF$ of 84.6 % [1], $R_S$ is probably even below 0.2 Ω cm$^2$ for the new record.

303 low, that temperature-dependent transport should play only a minor role at typical operating conditions ($\vartheta > 25\,°C$).
304 Deviation from linearity for the *FF* might still occur but at temperatures lower than 25 °C for this device [20].

## 3. SHJ solar modules

306     Several companies (e.g. Panasonic Corp., Meyer Burger) already demonstrated that the good performances of
307 SHJ solar cells can be translated into highly efficient solar modules. An important metric for module manufacturers
308 is the so-called cell-to-module (CTM) power ratio which is the module power divided by the sum of the power of its
309 constituent cells. CTM power ratios can vary greatly depending on module type and features, e.g. white backsheet
310 modules benefit from a $\approx 2\,\%$ gain in short circuit current ($I_{SC}$) because of the light recollected after reflection on the
311 backsheet between the cells [101, 102]. Advanced interconnection techniques and improvements in light management
312 at the module level are pushing CTM factors upward and they are expected to exceed 100 % by 2020 [103]. There is
313 a number of CTM loss and gain mechanisms (see e.g. [104, 105]) and it is interesting to identify those that affect the
314 $I_{SC}$ and those that affect the *FF* of modules.
315     The main optical loss phenomena is the reflection caused by the refractive index mismatch at the glass/air interface,
316 for standard solar glass this is about 4 %. Different ARC layers can be used to reduce this loss, e.g. a porous $SiO_2$
317 layer coated onto solar glass using industrial sol-gel processes increases $I_{SC}$ by about 2.7 % [106]. Another $I_{SC}$ loss is
318 caused by parasitic absorption in the encapsulant and can also take a range of values as there is a number of different
319 encapsulants on the market with various optical properties and different stabilities e.g. to UV. The encapsulant has
320 also a small positive effect on $I_{SC}$, about 0.3 %, as it acts like a dual-layer ARC. Additionally, as mentioned in Section
321 2, this implicates a lower TCO thickness to minimize reflection.[12] Another optical benefit from the encapsulation of
322 solar cells is the recollection of the fraction of light reflected on the metallization that is redirected onto the cell by
323 total internal reflection at the glass/air interface. This so-called *optical coupling* reduces the effective shading by the
324 fingers by about 50 % (depending on the finger shape) which in turn boosts $I_{SC}$ by about 1.5 %. This light recollection
325 mechanism is also important in reducing the shading by the interconnection and depends on the interconnection shape.
326 For example, the effective shading of textured ribbons is typically half that of standard ribbons (this corresponds to an
327 $I_{SC}$ gain around 1 %). In multi-wire configurations, in which the cell-interconnecting ribbons are replaced by round
328 wires, the effective optical shading is only $\approx 60\,\%$ of the wire diameter thanks to its circular shape.
329     The main mechanism that affects the module *FF* is the ohmic loss in the cell interconnections (ribbons or wires),
330 between the strings, in the junction boxes and in the cabling. The main loss stemming from the cell interconnection
331 whose design is driven by a trade-off between shading and ohmic losses as well as, for the industry, the price of metal
332 and the extra cost of features such as textured ribbons. To illustrate this, we simulate (see the details in Appendix B)
333 the losses for two multi-wires configurations with different diameters: 250 μm and 300 μm. The thicker wires cause
334 more shading than their thinner counterparts (2.1 % versus 1.7 %), but they also reduce series resistance so the ohmic
335 loss is significantly reduced (1.8 % versus 2.7 %). All in all, the 300 μm configuration enables a better CTM power
336 factor, +0.5 %, and the final choice is then driven by economic considerations. Additionally, the climate where the
337 modules are to be operated can be taken into consideration in order to maximize energy yields. For example, in very
338 sunny and hot climates, it might be beneficial to lower $R_S$ even at the expense of $I_{SC}$ while the opposite might be true
339 for a module operating at a location where the average incident irradiation is well below $1000\,W\,m^{-2}$ [96].
340     The *FF* of a module is also affected by the so-called cell-to-cell mismatch loss, which originates from the connec-
341 tion in series of cells with different IV characteristics [107]. While it has been shown that, for modern industries, the
342 cell-to-cell mismatch has a negligible effect on module power even without any cell binning [108][13], it has neverthe-
343 less an interesting two-sided effect on module *FF* and $I_{SC}$ . Figure 8 exemplifies that the $I_{SC}$ of 60 cells connected in
344 series is systematically lower than the average $I_{SC}$ of these cells (closer to the minimum $I_{SC}$ ). On the other hand, the
345 *FF* of the serially-connected cells is larger than the average *FF* of the cells. This phenomena is important to correctly
346 analyze the CTM factors of modules even when the cell-to-cell mismatch is small. This is illustrated on Figure 8

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[12]Note that the actual optimal TCO thickness remains a trade-off between anti-reflection, transparency and lateral conduction which depends upon the chosen metallization design.

[13]This study is based on IV data from 10000 cells from a production order in 2012 from a Suntech manufacturing facility in China.

347  where the distributions of the CTM factors of power, FF and $I_{SC}$ are shown of 5000 simulated modules comprised of
348  cells with $I_{SC}$ in a 4 % range. While the loss in power is low (CTM$_{P_{mpp}}$ around −0.15 %), the cell-to-cell mismatch
349  causes a strong negative CTM$_{I_{SC}}$ ($\approx$ −1 %) partially counterbalanced by a positive CTM$_{FF}$ ($\approx$ +0.85 %) [102]. This
350  effect is important for a module manufacturer to accurately separate between ohmic and optical losses (e.g. a good
351  *FF* does not necessarily mean small resistive losses if the cell-to-cell mismatch in a particular module is large).
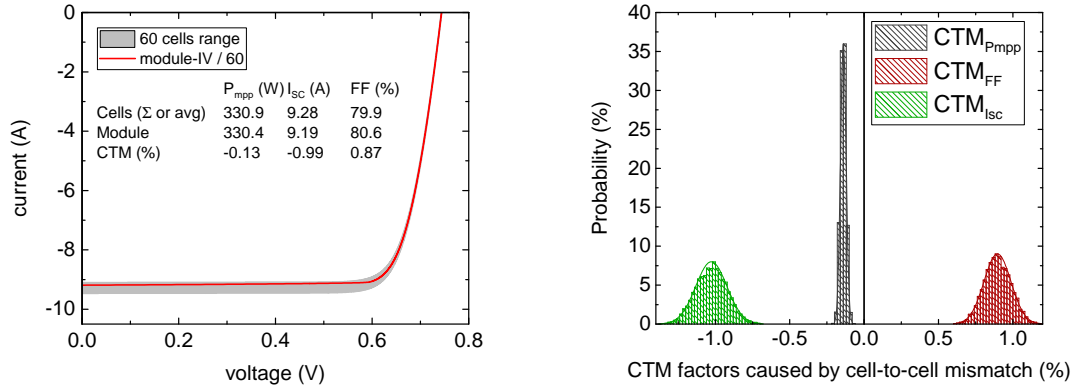


Figure 8: Left: In grey: simulated IV curves of 60 cells with identical diode characteristics but for $I_{SC}$ randomly picked in a 4 % range around 9.28 A. In red: simulated IV curve of the module constituted of these 60 cells connected in series. Right: Distributions of the CTM factors of power, *FF* and $I_{SC}$ of 5000 simulated modules comprised of cells with $I_{SC}$ in a 4 % range from ref. [102].

## 4. Industrial aspects

353  Sanyo Corp. (now Panasonic Corp.) was the first company to commercialize SHJ solar cells, and produced
354  for many years some of the most efficient *c*-Si modules with the lowest temperature coefficient [109]. In the last few
355  years, several companies have launched pilot production, or even mass production of SHJ solar cells. Some companies
356  recycled parts of the equipments designed for the production of thin film silicon solar cells for depositing some of
357  the SHJ layers. In parallel, several companies have started to design equipments specific for the manufacturing
358  of SHJ solar cells and modules. The coating technologies include hot-wire and (parallel plate) PECVD for the *a*-
359  Si:H layers and sputtering or ion plating[14] [110, 111] for the TCO deposition. For metallization, screen-printing
360  of low-temperature silver paste, or plating can be applied. The lean standard SHJ process (cf. Figure 9) ensures
361  that only few pieces of equipment are required (wet chemical preparation of the wafer, PECVD reactor for *a*-Si:H
362  layers, PVD for TCO, screen-printing for the metallization, annealing) and has a potential to come both in terms of
363  capital expenditures (CAPEX) and operational expenditures (OPEX) to a level similar to those of competing PERC
364  technologies. Considering the potential of a high bifaciality factor (>90 %) [112], record low temperature coefficient
365  and high energy yield[15] [114], thinner wafer for lower costs, SHJ bears the potential to achieve ultra-low electricity
366  costs. A mass market entrance has been delayed though by many negative perceptions with respect to the difficulty of
367  the technology, which we discuss here below:

368  • **Passivation homogeneity**: A major perceived difficulty is the achievement of homogeneous ultra-thin passiva-
369    tion layers based on *a*-Si:H in PECVD reactors, which might prevent the achievement of high production yield.

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[14]Ion plating is also referred to as high density plasma-enhanced evaporation

[15]Using $\Delta EY = \Delta TC \cdot (T_{avg} - T_{STC})$, gains in energy yield stemming from advantageous temperature coefficients can be estimated if the average operating temperature in terms of energy production expected in a given location, $T_{avg}$, is known. For example, $T_{avg}$ can reach 50 °C in desert areas in the American Southwest[113] which means that a reduction of temperature coefficient of 0.1 %/K results in an energy yield gain of 2.5 % in such locations.

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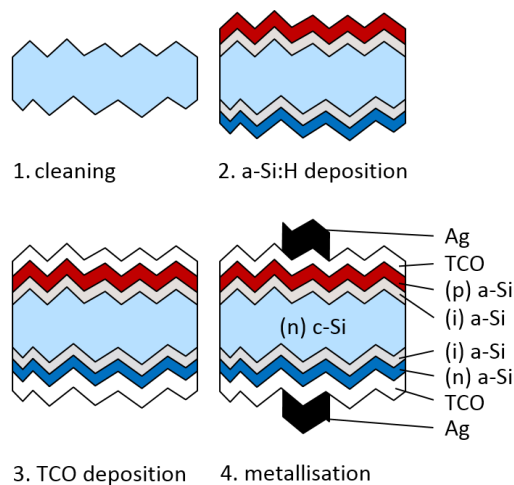
Figure 9: Manufacturing steps of a bifacial silicon heterojunction solar cell.

Indeed, such issues can be solved, e.g. by working on the PECVD reactor design [115, 116, 117, 118, 119]. The concept of closed heated plasma box [115, 118] enables for example to solve two major issues:

i) suppression of strong species diffusion near the edges of the reactor, which would occur in open reactors when the plasma is ignited and would lead to surface passivation inhomogeneity.

ii) suppression of cross-contamination linked to the cleaning of the reactor, only required after some hundred or thousands of coating cycles.

- **Availability of high-quality n-type silicon wafers at a competitive price**: A large fraction of the PV industry uses p-type wafers, raising the question of the availability of high-quality n-type material. Yet in recent years, triggered by the demand for higher p-type material quality from the PERC market, most monocrystalline silicon ingot manufacturer developed know-how enabling them to also grow high quality full n-type ingots (e.g. typically with a lifetime/resistivity above $1\,ms/\Omega\,cm$) at cost similar or only slightly superior to those of p-type materials [120]. Additionally, even in the case of multiple-charge pulls, metallic impurities and oxygen concentration can be kept at concentration sufficiently low for achieving high lifetime absorber material, without additional thermal donor treatment or gettering. A slightly higher price for n-type wafers compared to p-type wafers still come from less recharge of the quartz crucible than for p-type materials (a problem on which companies are working), and can be fully compensated by the use of thinner wafers possible for SHJ [120].

- **Risk of high metallization costs**: Because of the final annealing step at around $200\,°C$, low-curing-temperature (low-T) silver pastes are used. First generations of such low-T pastes exhibited a much lower conductivity than the pastes sintered for standard cells at over $800\,°C$ (up to a factor 10, in the late 2000's). Thanks to the continuous improvement in the paste development [112], illustrated in Figure 10, modern pastes are coming closer to bulk Ag, with resistivities in the range of $5\text{-}6\,\mu\Omega\,cm$. This is fully compatible with the current cell configurations featuring five or six busbars, and minimum amount of paste consumption [121, 122]. With the use of multi-wire configurations, in which the ribbons are replaced by round wires, the demand on finger conductance is further decreased [112]: typcially 18 wires of $\sim300\,\mu m$, embedded into a polymer foil, solder on the soft Ag paste during the lamination process. Because of the very short distance between two wires, a potential to reduce the Ag consumption down to 10-20 mg per side of 6-inch cells has been reported [121]. To entirely suppress the need for silver, copper plating has also been reported as an alternative approach, and Figure 11 shows a possible process to realize directly a bifacial Cu metalization [45, 112, 123] which then has a low cost potential upon large-scale acceptance.
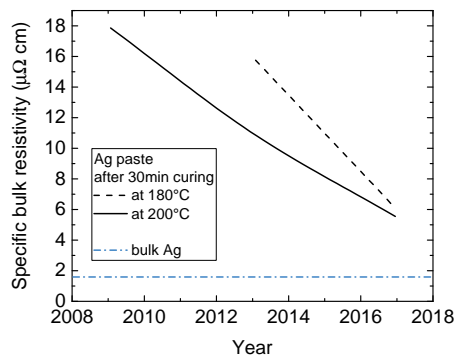
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Figure 10: Specific bulk resistivity of low-temperature Ag paste as a function of the year. Pure silver (horizontal line) is included as well for comparison. The continuous line indicates the resistivity after 30 min of curing at 200 °C, whereas the dashed line is obtained after curing 30 min at 180 °C. Data courtesy of Namics Corp.
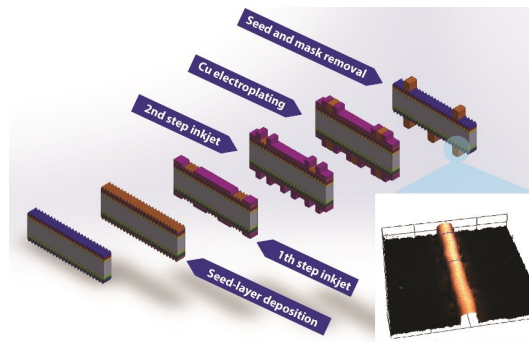


Figure 11: Process-flow of copper electroplating for a bifacial SHJ solar cell. Image courtesy of J. Geissbühler, CSEM [45, 123].

- **Risk of high costs of TCO**: typically 80 nm of TCO are deposited at the front and back of the SHJ. ITO targets are a major cost factor, corresponding typically to a usage of around 3.5 g of Indium per m$^2$ of modules for both surfaces (taking into account a 50 % usage of the sputtered materials). Without even considering the recycling of In deposited on the carriers and in the chamber, the cost of In is hence currently in the range of an acceptable 1 $/m$^2$ [124], corresponding, for a 335 W 60-cell module, to below 0.005 $/W. Alternative TCO such as Zinc oxide (ZnO) can also be used, in particular on the n-side, where the wafer-bulk conductivity plays a major role. For the configuration with p-layer on the front, a thin high-mobility TCO can be used combined with a lower-cost TCO to divide altogether the In consumption by a factor 4 (and 8 if Indium is recycled from the chamber walls). Hence this does not constitute a more fundamental problem than e.g. the use of Ag paste in standard *c*-Si cells and modules.

With the development of modern coating hardware [125, 126], highly efficient and cost-effective metallization scheme, the industry should have now many cards at hands to launch high volume manufacturing of SHJ. Indeed, six inch SHJ solar cells made in a pilot line were certified at 24 %, in the so-called busbar-less configuration (i.e. without wire shading and without resistive losses in the wires, corresponding to >23 % for full six inch devices) [127]. Modules using standard M2 SHJ cells produced in the same pilot line, multi-wire interconnection and with regular cell spacing were certified at 335 W [127], a value well above todays standard PV module performance (cf. Figure 12). The modules show a remarkable *FF* of 79.4 %. SHJ modules are free from potential induced degradation (PID), and with the right choice of module technology, a performance loss of less than 10 % after 25 years can be
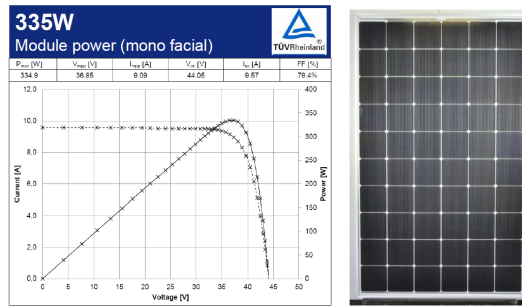
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Figure 12: Certified JV characteristic of a 60-cells (M2) module integrating SHJ solar cells and a white back-foil. The peak power of the module is 335 W. The cells were processed in the pilot-line of the Meyer Burger group in Hohenstein (DE) and the multi-wire interconnection is a new generation one, co-developed between CSEM and Meyer Burger Thun (CH). It uses wires without indium, allowing for low assembly and metallization costs. This is the highest reported performance for a module of this type.

guaranteed (e.g. on Panasonic N330). Combined with the expected high energy yield and the quasi perfect bifaciality this should lead to record high kWh production per rated $W_P$ in many environments. Finally, IBC-SHJ devices could further extend the efficiency and performance roadmap of SHJ, provided that the efficiency gain compensates for the increased process complexity. Both highest efficiency [1, 4] and lean processes have been reported [31] but not yet in the same device.

## 5. Summary

Silicon heterojunction (SHJ) solar cells are part of the family of solar cells with passivating contacts; they feature high open-circuit voltages ($V_{OC}$), generally well above 700 mV. Achieving of fill-factors ($FF$) comparable to the best high-efficiency devices based on homo-junctions has long been a challenge for SHJ solar cells. In 2017, Kaneka Corp. demonstrated a SHJ solar cell with interdigitated contacts at the rear side with a $FF$ of 84.9 %, the highest ever shown for a silicon solar cell so far. With an efficiency of 26.7 % this marked a new world record for silicon solar cells, and it underlines that SHJ technology not only enables very high $V_{OC}$, but also $FF$. In a simulation study we show the impact of recombination in the absorber as well as at its surfaces on $V_{OC}$ and $FF$ and emphasize that low recombination is especially important to reach high $FF$. We review briefly the different cell-to-module loss and gain mechanisms. For different interconnection schemes we discuss the trade-off between shading and resistive losses, and discuss $FF$ gains that can arise from cell-to-cell mismatch. Regarding industrialization, the homogeneity of the thin $a$-Si:H passivation layers as well as expensive raw materials were often seen as hindrances for the success of SHJ. With recent technological progress, these problems will likely be solved in the future. The intrinsic bifacial nature of SHJ technology as well as its low temperature coefficient should lead to record high energy production per rated power in many climate regions.

## Acknowledgements

## Appendix A. Description of simulation approach

For the simulation of (temperature-dependent) JV characteristics a python script was developed to calculate:

1. injection-dependent effective minority carrier lifetime, considering Shockley-Read-Hall, Auger and radiative recombination in the silicon absorber as well as surface recombination;

16

2. the absorbed current density $J_{abs}$ for the AM1.5g (ASTM G-173-03) spectrum at a given temperature and optical properties;

3. the implied JV characteristic from the injection-dependent effective minority carrier lifetime, assuming $J_{abs}$ as short circuit current density;

4. the JV characteristic assuming an ohmic series resistance by shifting the voltage according to the voltage drop over the resistance at the given current density following Ohm's law.

*Appendix A.1. Optical modeling*

The calculation of the absorption $A(\lambda)$ is done using analytical modeling, following an approach initially suggested by Deckman *et al.* [128] and extended by Boccard *et al.* [129]. The analytical model traces an average ray through the absorber and assumes a lambertian distribution of light. We use equation (5) in ref. [129] to calculate the absorption in the wavelength-range from 300 nm to 1300 nm. We assume no reflection when entering the absorber ($R_0 = 0$). For the simulations shown in Figure 4, we vary the parasitic absorption at the rear side as a wavelength-independent parameter ($A_P^{back}= 0, 0.1, 0.25, 0.5$). The parasitic absorption at the front side ($A_P^{front}$) we calculate with single-pass Lambert-Beer absorption

$$A_P^{front} = 1 - \exp\left(-\frac{4\pi k_{aSi}}{\lambda} \cdot t_{aSi}\right) \tag{A.1}$$

for *a*-Si:H(p) thicknesses $t_{aSi}$ 0 nm, 2 nm, 5 nm, 10 nm, and with the extinction coefficient for *a*-Si:H(p) $k_{aSi}(\lambda)$ published by Holman *et al.* [50] and taken from the refractive index library on pvlighthouse.com. Further parameters of the optical models are: $a_0 = 2$, $b_1 = 1/n^2$ (lambertian scattering), and the temperature dependent absorption coefficient of silicon $\alpha(T)$, taken from ref. [130]. Using $A(\lambda)$, the absorbed current density $J_{abs}$ is then calculated following

$$J_{abs} = \frac{q}{hc} \int_{300\,nm}^{1300\,nm} A(\lambda) \cdot \lambda E_{AM1.5}(\lambda)\, d\lambda \tag{A.2}$$

with the elementary charge $q$, the Planck constant $h$, and the speed of light $c$.

*Appendix A.2. Charge carrier lifetime & implied JV curve modeling*

Recombination in the silicon absorber is characterised by Shockley-Read-Hall lifetime $\tau_{SRH}^{bulk}$ [131, equation (5.3)] and intrinsic lifetime $\tau_{intr}$ as parametrized by Richter *et al.* [132, equation (18)]. For the temperature-dependent intrinsic carrier concentration $n_i(T)$ the parametrization by Misiakos *et al.* [133] is used.

The surface recombination rate $R_{surf}$ is modeled using the model for *a*-Si:H/*c*-Si interface recombination based on the amphoteric nature of silicon dangling bonds proposed by Olibet *et al.* [134]. The parameters used in the model are summarized in Table A.2, the same surface recombination has been assumed for both sides of the absorber.

The injection-dependent effective lifetime $\tau_{eff}$ is then calculated with $\tau_{SRH}^{bulk}$, $\tau_{intr}$, and assuming symmetrical surface recombination [135] following

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}^{bulk}} + \frac{1}{\tau_{intr}} + \frac{2R_{surf}}{\Delta n\, w} \tag{A.3}$$

with the excess charge carrier density $\Delta n$ and absorber thickness $w$.

The implied open-circuit voltage $V_{OC}$ ($iV_{OC}$) is dependent of $\Delta n$ and is calculated using

$$iV_{OC}(\Delta n) = \frac{kT}{q} \ln\left(\frac{(n_0 + \Delta n)(p_0 + \Delta p)}{n_i(T)^2}\right) \tag{A.4}$$

with the Boltzmann constant $k$, and the equilibrium concentrations of electrons ($n_0$) and holes ($p_0$), and $\Delta n = \Delta p$. The implied voltage range $iV_{OC}(\Delta n)$ represents the voltage of the implied JV characteristic.

The recombination current $J_{rec}(\Delta n)$ can be written as

$$J_{rec}(\Delta n) = q\, w\, \frac{\Delta n}{\tau_{eff}} \tag{A.5}$$

17

Table A.2: Parameter used for the simulation if not stated otherwise

| parameter (bulk) | value | parameter (surface) | value |
|---|---|---|---|
| wafer thickness $w$ | $160\,\mu\text{m}$ | model | dangling-bond |
| doping (n-type) | $2 \times 10^{15}\,\text{cm}^{-3}$ | $Q_\text{g}$ | $0\,\text{cm}^{-2}$ |
| $\sigma_\text{n}$ | $10^{-14}\,\text{cm}^2$ | $\sigma_\text{n}^0$ | $\frac{1}{20} \cdot 10^{-16}\,\text{cm}^2$ |
| $\sigma_\text{p}$ | $10^{-14}\,\text{cm}^2$ | $\sigma_\text{p}^0$ | $10^{-16}\,\text{cm}^2$ |
| $N_\text{trap}^\text{bulk}$ | $10^9\,\text{cm}^{-3}$ | $\sigma_n^+$ | $500 \cdot \sigma_\text{n}^0$ |
| trap energy level | midgap | $\sigma_p^-$ | $500 \cdot \sigma_\text{p}^0$ |

which leads to the implied JV characteristic derived for a range of $\Delta n$. For the calculation of the illuminated implied JV characteristic, the $J_\text{abs}$ as obtained from equation (A.2) is assumed as $J_\text{SC}$ and subtracted from the right side of equation (A.5) which allows for the calculation of the implied fill-factor *iFF*.

## Appendix B. Comparison of cell-to-module losses of two multi-wire configurations: $250\,\mu\text{m}$ and $300\,\mu\text{m}$

This simulation aims at illustrating the trade off between shading and ohmic losses that drives the choice of an interconnection scheme.

Because of their circular shape, the effective optical shading of wires once encapsulated in modules is about $60\,\%$ of the wire diameter ($\phi_\text{wires}$).[16] Then, the shading loss can be estimated using:

$$shading = N_\text{wires} \cdot \phi_\text{wires} \cdot 0.6 \cdot \frac{length_\text{cell}}{area_\text{cell}} \tag{B.1}$$

with e.g. for 6 inch M2 wafers, $length_\text{cell} = 156.75\,\text{mm}$ and $area_\text{cell} = 244.3\,\text{cm}^{-2}$).

The ohmic losses in the interconnection were calculated using an in-house simulation software. The parameters for the simulation were chosen to be representative of a standard bifacial multi-wire SHJ configuration: wire resistivity ($1.7\,\mu\Omega\,\text{m}$), number of fingers at the front and the rear (87 and 207), and finger line resistance at the front and the rear ($0.83$ and $0.91\,\Omega\,\text{cm}^{-1}$).

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[16]Effective optical shading can be measured on encapsulated samples using the laser beam induced current (LBIC) technique for example.

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