Multi-Tone Signaling and ADC-Based Digital Receiver for High-Speed Wireline Serial Links

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To my parents

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Abstract

The exponential growth of Internet traffic and related demands for higher communication speed pushes processor-to-processor and processor-to-memory interconnects to provide further higher data-rate. Often time, processor-to-memory interconnects' speed is limited by reflections due to their multi-drop bus (MDB) channel nature, and processor-to-processor interconnects' speed is limited by inter-symbol interference due to the slowly-decaying channel pulse response and the operating speed and/or power efficiency of the equalization circuits. For the data-rate to continue its exponential growth, more complex modulation and equalization techniques should be employed in the transmitter (TX) and receiver (RX) circuits, given the power and silicon area budget.

This thesis presents a signaling scheme designed to overcome equalization challenges related to reflection-limited interfaces such as MDB interfaces. By shaping the spectrum of the transmitted signal appropriately to the channel's frequency characteristics, the proposed signaling enables minimization of energy-loss due to reflections. While the data-rate of conventional non-return-to-zero (NRZ) signaling over MDB is limited by its first notch frequency unless power-hungry decision-feedback equalizer (DFE) is employed, the proposed signaling scheme allows overcoming such limitation by simple encoding and decoding.

Analog multi-tone (AMT) signaling with single-sideband (SSB) radio-frequency (RF)-bands for efficient bandwidth usage is proposed for lossy point-to-point interfaces. The mutually-orthogonal RF sub-bands feature self-equalization throughout the propagation through the communication medium and down-conversion at the RX, without necessitating the presence of conventional equalizers. To enable communication with higher modulation order for more efficient bandwidth utilization, an analog-to-digital converter (ADC)-based discrete multi-tone (DMT) RX is designed and implemented. Thanks to the high bandwidth efficiency of approximately 5.33 bits/Hz (including the cyclic prefix of DMT symbol) using 64-level quadrature amplitude modulation (64-QAM), the implemented RX undergoes less channel attenuation as compared to its 4-level pulse amplitude modulation (PAM-4) counterpart given target communication speed through the same channel. Moreover, the inherently parallel RX architecture of DMT signaling allows the RX digital signal processing (DSP) elements to be designed in semi-custom style without stringent timing constraints. Finally, a PAM-4 RX based on ADC with fully-digital equalization is presented. With register-transfer level (RTL) modeling of the designed digital equalizer, the results demonstrate the feasibility of frequency-domain equalization of the time-domain signal using Fourier transform and its inversion. The proposed frequency-domain equalization technique removes the necessity

of symbol-by-symbol feedback loop in DSP that is present in DFE, relaxing critical timing constraints in DSP synthesis.
The focus of this thesis is on the study of spectral characteristics of transmitted/received data and frequency-domain solution for equalization by multi-channel (carrier) and/or ADC-based digital signal processing. The spectrum shaping signaling targeting MDB interfaces is demonstrated by architectural modeling and general-purpose digital-to-analog converter (DAC)-based experiment. The SSB-AMT signaling with self-equalization characteristics is demonstrated by architectural modeling and general-purpose DAC and ADC with a high oversampling ratio for emulating analog signaling. The DMT transceiver (TRX) for ultra-high-speed wireline serial link system is demonstrated using DAC as DMT TX and fabricated RX chip in GlobalFoundries 14 nm FinFET low-power plus (LPP) process technology.

Keywords: Serial link, wireline transceiver, wireline receiver, ADC, analog-to-digital converter, ADC-based serial link, multi-drop bus, spectrum shaping, PAM-4, 4-PAM, discrete multi-tone, DMT, analog multi-tone, AMT, Fourier transform.

Résumé

La croissance exponentièlle du trafic Internet et les demandes connexes pour une vitesse de communication plus élevée poussent les interconnexions processeur-à-processeur et processeur-à-mémoire vers un débit de données plus élevé. Souvent, les interconnexions processeur-mémoire sont limitées par des réflexions dues à leur nature de canal de bus multipoint, et les interconnexions processeur-processeur sont limitées par l'interférence inter-symboles due à la réponse d'impulsion de canal à décroissance lente et la vitesse de fonctionnement et/ou l'efficacité énergétique des circuits d'égalisation. Pour que le débit de données continue sa croissance exponentielle, une modulation et une égalisation plus complexes doivent être utilisées dans les circuits émetteur et récepteur, compte tenu du budget de la puissance et de la surface de silicium.

Cette thèse présente un schéma de signalisation conçu pour surmonter les interfaces limitées par la réflexion telles que les interfaces bus multipoint. En faisant correspondre de manière appropriée le spectre du signal transmis aux caractéristiques de fréquence du canal, la signalisation proposée permet de minimiser la perte d'énergie due aux réflexions. Alors que le débit de données de la signalisation non-retour à zéro classique sur le bus multipoint est limité par sa première fréquence d'entailleur, sauf si un égaliseur à rétroaction décisionnelle gourmand en énergie est utilisé, le schéma de signalisation proposé permet de surmonter cette limitation par simples encodage et décodage.

La signalisation à plusieurs tonalités analogiques avec des bandes à fréquence radio à bande latérale unique pour une utilisation efficace de la bande passante est proposée pour les interfaces point à point avec perte. Les sous-bandes fréquence radio mutuellement orthogonales présentent une auto-égalisation tout au long de la propagation à travers le canal et une conversion vers le bas au niveau du récepteur, sans nécessiter la présence d'égaliseurs classiques. Afin de permettre une communication avec un ordre de modulation plus élevé pour une meilleure utilisation de la bande passante, un récepteur multitone discret basé sur un convertisseur analogique-numérique (CAN) est conçu et implémenté. Grâce à l'efficacité de bande passante élevée d'environ 5,33 bits/Hz (préfixe cyclique inclu) utilisant une modulation d'amplitude en quadrature de 64 niveaux, le récepteur implémenté subit moins d'atténuation du canal que sa modulation d'impulsions d'amplitude de 4 niveaux (MIA-4) contrepartie pour la même vitesse de communication par le même canal. De plus, l'architecture réceptrice intrinsèquement parallèle de la signalisation discrète multitone permet aux éléments de traitement du signal numérique du récepteur d'être conçus dans un style placé et routé automatiquement sans contraintes de synchronisation strictes. Enfin, un récepteur MIA-4 basé sur CAN avec égalisa-

tion entièrement numérique est conçu. Avec la modélisation du niveau de transfert de registre (RTL) de l'égaliseur numérique conçu, les résultats montrent la faisabilité de l'égalisation dans le domaine fréquentiel du signal dans le domaine temporel en utilisant la transformée de Fourier et son inversion. La technique d'égalisation du domaine fréquentiel proposée supprime la nécessité d'une boucle de rétroaction symbole par symbole dans le processeur de signal numérique qui est présente dans l'égaliseur à rétroaction décisionnelle, relâchant les contraintes de synchronisation dans la synthèse du processeur du signal numérique.
L'objectif de cette thèse est l'étude des caractéristiques spectrales des données transmises/-reçues et de la solution de domaine fréquentiel pour l'égalisation par traitement de signal numérique multicanal (porteuse) et/ou CAN. Le schéma de signalisation proposé ciblant les interfaces de bus multipoint est illustré par une modélisation architecturale et une expérience à base de convertisseur numérique-analogique (DAC) à usage général. La signalisation de plusieurs tonalités analogiques à bande latérale unique avec des caractéristiques d'auto-égalisation est démontrée par modélisation architecturale et l'experimentation basée sur le CDA et CAN à usage général avec suréchantillonnage pour l'émulation de la signalisation analogique. L'émetteur-récepteur multitone discret pour le système de liaison série filaire à ultra-haute vitesse est démontré en utilisant le CDA comme émetteur multitone discret et la puce RX fabriquée par la technologie de processus FinFET LPP de 14 nm de GlobalFoundries.

Mots clés : Lien série, émetteur-récepteur filaire, récepteur filaire, CAN, Convertisseur analogique-numérique, Lien série basé sur CAN, bus multi-tap, mise en forme du spectre, multi-ton discrète, multi-ton analogique, Transformée de Fourier.

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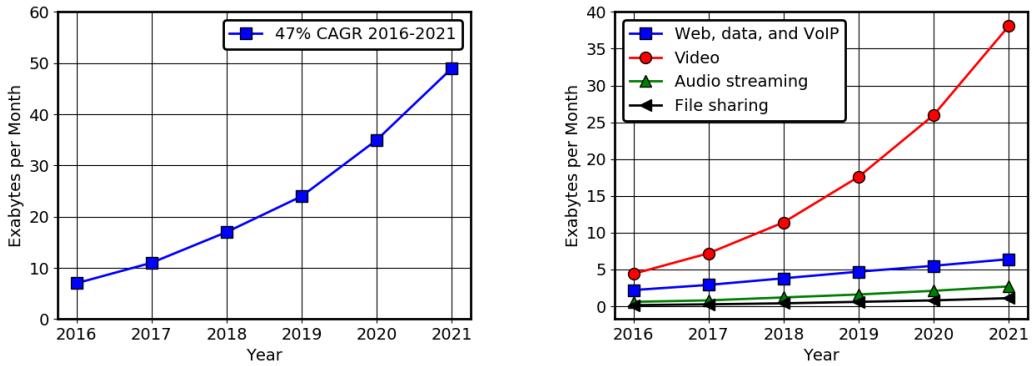
1 Introduction

A fast increase in the number of electronic devices connected each other everywhere around the world lead ever-higher global Internet protocol (IP) traffic, meeting the era of Internet-of-things (IoT) and big-data. Moreover, the volume of the multimedia contents that are transmitted/received by individual electronic devices exponentially increases throughout the years [1]. For instance, a pixel-resolution of commonly-used consumer digital displays such as monitors, or televisions has been evolving from 1024 × 768 in 2002 to 3840 × 2160 in 2018, which mutually increases the resolution of the digital videos and photos to be displayed. Also, the number of worldwide smartphone users was increased from 1.57 billion in 2014 to 1.86 billion in 2015, and it is predicted to reach 2.87 billion in 2020, while per-smartphone monthly data traffic increases by 25-40 % annually [2]. Including smartphones, home-electronics, and other IoT devices, the total number of connected consumer-electronic devices is predicted to exceed 11 billion by 2021 [1]. As a result, the global mobile data traffic is expected to reach 49 Exabyte (EB) (or 49×10^9 Gigabyte) per month by 2021 [1] where its compound annual growth rate (CAGR) is shown in Fig. 1.1(a).

Such exponential growth of data traffic necessitates enhancement of not only wireless radio frequency (RF) communication bandwidth between the cellular device and the base station or other electronic devices, but also data-rates among wired networking infrastructures. Fig. 1.1(b) highlights the growing network traffic more specifically [1]. Among various sub-segments, a significant portion of Internet traffic is due to the mobile video streaming, of which traffic is expected to grow by 54 percent every year between 2016 and 2021 on average, while the overall mobile data traffic is expected to grow by 47 percent each year. This makes the data centers to be the heart of the Internet network, where the multimedia contents and other types of files are stored. A data center includes numbers of racks of servers that are containing processors, data storage units, memories, network switches, routers, that are connected with electrical/optical cables. The server board includes various wireline transceiver (TRX) units for communication with other modules over electrical channels with different communication standards.

As the power consumption of IT/network infrastructures is becoming increasingly crucial



(a) (b)

Figure 1.1 – The expected compound data traffic growth (a) and the growth by specific data type (b) due to connected mobile devices from 2016 to 2021 [1].

while satisfying expanding bandwidth demands, pushing the limits of wireline TRXs for chip-to-chip links and chip-to-memory links in terms of data-rate, silicon area, and energy efficiency is crucial. While the aggregate input/output (I/O) data-rate can be increased by placing more I/O pins per component, the increased power consumption, additional interconnect material cost, and larger die/package area raise as an issue. Thus, higher per-pin data-rate with enhanced energy efficiency is must for keeping the aggregate power and material cost unchanged or decreased, while providing a higher total data bandwidth.

1.1 Wired Interfaces and Standards

The wired communication systems' characteristics differ from one application to another, e.g., controller-storage interconnect, controller-memory interconnect, and processor-to-processor interconnect. Data rate evolution of some widely-used wireline standards over last two decades is shown in Fig. 1.2. It can be seen that lane data-rate has been successfully following the approximately ×2 speed enhancement with every generation. The data rates of point-to-point interconnect standards such as peripheral component interconnect express (PCIe), common electrical I/O (CEI), graphics double-data-rate synchronous random-access memory (GDDR SDRAM) remain faster than those of multi-drop interconnect standards such as DDR SDRAM by as much as close to ×8.

While having relatively low per-pin data transfer rate, DDR SDRAM still exhibits as high module data-rate as 25.6 GBytes/s with a massively-parallel data bus in case of fourth generation DDR SDRAM (DDR4) dual in-line memory module (DIMM). A similar strategy has been applied in case of high-bandwidth memory (HBM) of which first- and second-generations have been adopted as joint electron device engineering council (JEDEC) standard in October 2013 and January 2016, respectively. The 2nd generation HBM (HBM2) exhibits only 2 GT/s but can

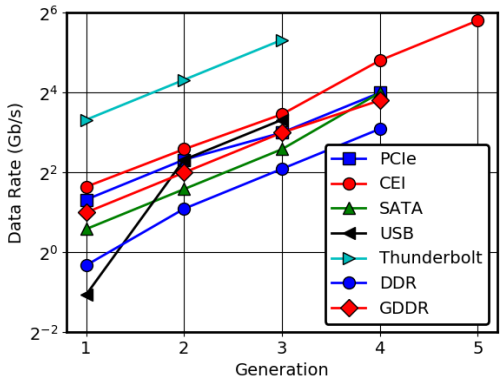


Figure 1.2 – Lane data-rate of various serial link standards.

reach as high as 256 GB/s of package bandwidth using 1024-bit-wide memory bus. Main memories such as DDR SDRAM and HBM are typical examples of serial interfaces transferring high bandwidth with relatively low per-pin data-rate using a wide parallel bus. Their massively-parallel bus characteristics requires high lane efficiency, hence single-ended signaling scheme is employed for memory I/Os.

For data center networking applications, optical internetworking forum (OIF) has defined CEI as serializer-deserializer (SerDes) interfaces for the industry since 2006, ranging its defined data-rate from 3.125 Gb/s to 56 Gb/s over multiple generations. It defines standards for various channel reaches, e.g., 10 mm ultra-short-reach (USR) traces for multi-chip modules (MCM), very-short-reach (VSR) traces for on-board module-to-module interconnects, mid-reach (MR) traces for processor-to-processor communications on server board, and long-reach (LR) backplane interconnects. While differential signaling is used for all sub-categories, modulation schemes may differ from one application to the other due to the different channel characteristics.

As a standard for high-speed computer expansion bus, PCIe standard was defined in 2003 by industries including Intel, Dell, HP, and IBM. PCIe can easily be found in most computer systems' motherboards, of which physical slots generally come with groups of lanes, e.g., ×4, ×8, ×16. Each lane supports data transfer rate from 2.5 GT/s (version 1.0) to 32 GT/s (version 5.0). After considering the redundancy introduced by line-coding such as 8b/10b code for version 1.0/2.0 and 128b/130b for version 3.0/4.0, its per-lane data-rate reaches 1969 MB/s/direction at the latest standard. While each lane is composed of two differential links for transmission/reception, multiple PCIe lanes can be aggregated to extend the bandwidth. Low-speed peripherals, .e.g, Wi-Fi card, can use a link with one PCIe lane, while bandwidth-intensive applications such as multi-graphics processing unit (GPU) cards systems can use as many as four lots of 16 PCIe lanes.

The universal serial bus (USB) is an industry standard for personal computer (PC)-peripheral devices communication and power supply. The standard was designed by industries including

Compaq, IBM, Intel, Microsoft, DEC, NEC, and Nortel in January 1996, and is maintained by the USB implementation forum. While its first standard supports data-rate of as low as 187.5 kB/s (1.5 Mb/s), it currently supports data-rate of as high as 2.5 GB/s (20 Gb/s), using differential signaling. Links employing USB standard are widely used for mass storage, extension cables, audio streaming and power supply.

The IEEE p802.3bj specifies 100 Gb/s Ethernet standard (4 × 25 Gb/s differential links) for data transmission over electrical links such as twinaxial copper cable and backplane. It allows the use of forward error-correction (FEC) to relax the raw bit error rate (BER) at the cost of coding overhead and additional latency. As FEC coding, Reed-Solomon (RS) codes are widely used in storage systems and data transmission. For example, in IEEE 802.3bj standard, RS (n=528, k=514, m=10, t=7) FEC was designed for 25 Gb/s non-return to zero (NRZ) signaling and RS (n=544, k=514, m=10, t=15) FEC was designed for 25 Gb/s 4-level pulse-amplitude modulation (PAM-4), which can also be used for links with 50 Gb/s/lane. The RS (n=544, k=514, m=10, t=15) FEC relaxes raw BER requirement to as low as 3×10^{-4} for output BER of 10^{-12} [3].

While circuit innovations and equalization techniques as well as process technology enhancement have been pushing the per-lane (or per-pin) data-rate, power/thermal density would have been increased if energy efficiency had not been improved. Moreover, faster data stream occupies larger frequency bandwidth, which makes the signal gets more attenuated and more distorted due to the frequency-dependent channel attenuation and phase distortion, especially with low-cost and/or long-reach cables. The bandwidth- and attenuation-related issues with faster data-rate for lossy channels brought multi-level modulation schemes such as PAM-4 to the stage. While multi-level signaling enables data communication with narrower bandwidth as compared to 2-level signaling (PAM-2, or NRZ) and relaxes timing constraints, it makes the equalization circuits to be more complicated, more area consuming and more power hungry.

Complementary metal oxide semiconductor (CMOS) device fabrication process technology has been aggressively scaled-down over past decades from gate length of 10 um in 1971 down to 32nm. However, the gate length shrinkage no-longer follows the number appears in the process node designation from 28nm node. Standard 2-dimensional planar CMOS technology node had been shrunk down to 20nm with Taiwan Semiconductor Manufacturing Company (TSMC), and 3-dimensional process technology such as FinFET has been rising from 22nm node down to 7nm, and even further down to 5 nm, driven by industries such as TSMC, GlobalFoundries, Samsung, and Intel. Most of today's state-of-the-art field-programmable gate arrays (FPGA), mobile systems-on-chip (SoC), GPU, central processing unit (CPU) are manufactured in FinFET technology [4, 5, 6, 7, 8, 9]. Unlike in planar CMOS, FinFET process does not allow transistor design with continuous gate length choices, but only discrete lengths based on fin-count. Combined with ever-reducing supply voltage, intrinsic metal-oxide semiconductor field-effect transistor (MOSFET) gain over node shrinkage, and a discrete gate length of FinFET, process technology becomes more and more digital-friendly but analog-unfriendly. Following the trend of die-shrinkage and speed/power enhancement of microprocessors and

SoCs, analog circuits have to be fit together with digital circuits on the same die, including analog-to-digital converters (ADC), phase-locked loops (PLL), amplifiers, radio-frequency TRXs, and SerDes. Thanks to the intrinsic speed/power enhancement occupying smaller die area with process technology advancement, analog PLL and SerDes can operate faster with enhanced power efficiency as compared to implementation with older process technologies.

A fast enhancement of low-power, high-speed and mid-resolution ADC's performance in advanced process nodes (including planar CMOS, silicon-on-insulator, FinFET) enabled ADC-based interface design [10, 11, 12, 13]. This triggered increased interests in designing digital equalizers replacing many analog equalizers traditionally implemented as analog circuits. In order to keep the serial link performance improvement in every aspect, e.g., data-rate, energy efficiency, silicon area efficiency, numbers of prior researches have been conducted and reported. In the following sub-chapter, circuits, signaling, signal processing and architectural innovations for improving point-to-point links and multi-drop links are briefly reviewed.

1.2 Background and Prior-Arts

1.2.1 Point-to-Point Interconnect

Point-to-point interconnects are widely used from short-reach electrical links such as chip-to-chip communication to long-haul optical links such as digital television and telecommunication network. Thanks to the high bandwidth and low cost, CMOS circuits are widely used for high-speed interconnect systems. Focusing more on electrical links, the transmission line (channel) exhibits low-pass filter-like behavior in its frequency response, due to the skin effect, dielectric loss, and such. Having all the effects causing a loss in channel frequency response, the resulting loss from one end of a channel to the other end is called insertion loss. As point-to-point links are mostly terminated with matched impedance, reflection is generally not pronounced. Moreover, differential signaling is typically used for high-speed links (e.g., $\geq$ 10 GHz), providing higher input dynamic range and higher signal-to-noise ratio (SNR).

The insertion loss causes frequency-selective delay/attenuation for a wideband signal that passes through the channel. The low-pass filter nature of the channel makes the pulse-response of the system slow and long, resulting in inter-symbol interference (ISI). Since signals passing through a channel can be modeled as a convolution of the incoming waveform with channel's impulse response, tail post-cursors of past pulse responses at particular time slots can accumulate and can be superimposed on top of the main cursor of current pulse response, resulting in decision error. The same mechanism can be applied with precursors. Transmitter (TX) and/or receiver (RX) circuits in wireline serial link systems in general incorporate circuits that partially cancel-out these effects of the channels' characteristics.

Equalizer on the TX side can be used to pre-distort signal to be transmitted so that the pre-distorting filter's transfer function and the channel transfer function ideally compensate for each other. As the channel is generally low-pass filter-like, high-frequency pre-emphasis or

low-frequency de-emphasis schemes are employed as TX equalizer. Implemented as digital finite impulse response (FIR) filter or analog feed-forward equalizer (FFE), such TX pre-/de-emphasis filters have an effect to shorten the channel's effective pulse response, reducing the effects of pre-cursors and/or of post-cursors, hence reduced ISI. While the frequency response of pre- and de-emphasis filters are similar given a channel to equalize, their effect on the system differs. By pre-emphasizing TX signal's high-frequency components, the overall transmitted power is increased, resulting in stronger crosstalk power and higher TX power consumption, while de-emphasis reduces the TX output power resulting in lower signal-to-noise ratio at the RX front-end. TX prototypes with 1 pre-emphasis tap are demonstrated in [14, 15, 16] and 2 pre-emphasis taps are demonstrated in [17, 18, 19, 20]. More than 2 pre-emphasis taps are employed in [21, 22, 23, 24, 25] in order to fully or partially equalize a channel with high-loss, or output driver's bandwidth loss on the TX side. Often time, implementation of TX FFE is easier than implementing it on the RX side since the symbols used for FFE taps' output values are true-digital symbols if implemented on the TX side. However, it is challenging to implement TX FFE with long memory since it will require a high-resolution digital-to-analog converter (DAC) running at symbol-rate, and also due to the limited driver's output amplitude. Hence, in many high-speed serial links for lossy channels employ RX equalizer as well.

RX equalizer is composed of a continuous-time linear equalizer (CTLE) for high-frequency peaking, a linear FFE for pre-/post-cursor cancellation, a decision-feedback equalizer (DFE) for post-cursor cancellation. A CTLE-only RX equalizer demonstrated its equalization capability in [26, 27] when the channel is very smooth without reflection, or when the channel is ultra-short-reach channel with only a small amount of loss at Nyquist. In many designs, equalizer consisting of a CTLE followed by a DFE is chosen when pre-cursors are negligible [28, 29, 30, 31, 32]. To accommodate different types of channels, [28] employs CTLE providing 4–10 dB variable high-frequency peaking followed by a 2-tap DFE with automatic threshold tracking and sign-sign least mean square (LMS) adaptation engine. An RX data-path incorporating CTLE with variable peaking from 0 to 8.8 dB followed by a 2-tap DFE for 30 dB loss compensation is shown in [29], and [30] demonstrates equalization of 20 dB loss channel with 30 Gb/s data-rate under one pJ/b energy efficiency using a CTLE followed by a 1-tap DFE. In [31], RX equalizer consisting of a CTLE and a 1-tap DFE is realized for 21 Gb/s data-rate for channel loss of 14.9 dB at Nyquist, employing low-frequency and high-frequency equalization gain balancing adaptation method. A low-power RX data-path is demonstrated in [32] with an energy efficiency of 0.23 pJ/b at 25 Gb/s data-rate for 24 dB loss channel at Nyquist. It uses a one-stage CTLE followed by half-rate/quarter-rate current-steering 2-tap DFE.

As data-rate raises ever-higher, closing DFE's feedback loop becomes problematic even with advanced process node. In order to address this, loop-unrolling (also called speculation or look-ahead) technique has been applied to ultra-high-speed DFEs, relaxing the critical-path timing [33, 34, 23, 35, 36, 37, 38, 39, 40]. Each tap-speculating requires 2^N look-ahead cases implemented by current sources and multiplexers (MUX), where N is the number of signaling levels, e.g., $N = 2$ for NRZ and $N = 4$ for PAM-4, and the number of look-ahead paths increases

exponentially with the basis N. Hence, loop-unrolling with more than two DFE taps becomes impractical due to an exponential growth of the area and resulting power consumption, especially with PAM-4 which would require 16-paths with only two-tap loop-unrolling. Some RX designs feature 2-tap speculation [34, 33, 39] with two-decision look-ahead.

As the loss at Nyquist increases with the data-rate increase when the transmission medium (channel) remains the same, equalization becomes more and more challenging. To reduce the loss at Nyquist, multi-level pulse-amplitude modulation schemes such as PAM-4 have been used for high-speed data communications. However, PAM-4 is said to be intrinsically three times more sensitive to ISI given same peak-to-peak amplitude, and the TX output driver may suffer from linearity issue [41], and the TX/RX equalizer's complexity becomes more complex than that of NRZ. Nevertheless, the fact that PAM-4 halves the bandwidth by half as compared to NRZ spectrum hence reducing insertion loss and crosstalk power lead many TRX designs supporting PAM-4. For the cases where using PAM-4 can give at least 9.5 dB less insertion loss when compared to the cases using NRZ signaling, prototypes employing PAM-4 signaling effectively demonstrated its feasibility for ≥ 25 Gb/s [42, 43, 35], for ≥ 56 Gb/s [33, 44, 45, 46, 35, 47], and for 112 Gb/s [24, 25].

Taking advantage of recent advancement of ADC performance, ADC-based receivers are highly featured. In [48], ADC-based quarter-rate digital 8-tap FFE followed by 8-tap DFE based on 4-tap loop-unrolling and a look-up table (LUT)-based architecture, without analog equalizer has been demonstrated for NRZ RX. Based on a 5-bit 16 GS/s quarter-rate flash ADC, it demonstrated 3.5 pJ/b of energy efficiency at 16 Gb/s data-rate for equalizing 20 dB attenuation at Nyquist. Similar work in [49] including clock and data recovery (CDR) circuit and with added digital gain control function to the FFE shown in [48] demonstrated 25 Gb/s data-rate to equalize 40 dB loss at Nyquist with 8-tap FFE and 8-tap DFE. An NRZ RX with 6-bit 10.3125 GS/s 2-way time-interleaved flash ADC followed by digital 5-tap DFE together with 4-tap TX FFE is presented in [50]. This design incorporates a three-stage peaking amplifier to partially compensate for high-frequency channel attenuation before ADC. In [51], a 10 Gb/s NRZ RX based on 6-bit asynchronous successive approximation register (SAR) ADC embedding 3-tap analog FFE, followed by 3-tap DFE is present. By separating the RX input voltage range into reliable-'0' and reliable-'1' regions, the RX disables part of its equalizer to save power whenever the decisions are in the reliable region resulting in power saving. With the help of two-stage CTLE at the analog front-end (AFE), [52] demonstrated 8-bit 28 GS/s 32-way TI-SAR ADC-based RX for 56 Gb/s data-rate with 31 dB attenuation at Nyquist achieving BER of 10^{-8} dissipating 370 mW, where power consumption of digital signal processor (DSP) is not included in the reported number. Another ultra-high-speed ADC-based RX can be found in [53], based on reconfigurable ADC. Having three-stage CTLE followed by a VGA as AFE, the ADC can be configured as either 7-bit mode or 3-bit mode depending on the required equalization effort. It demonstrated that for channels that are easy to equalize, CTLE could practically perform all the required equalization letting the DSP to be bypassed, resulting in significant power saving. [54] presents a 64 Gb/s PAM-4 TRX with both TX/RX equalization, where RX employs a reconfigurable 4-way TI 6-bit flash ADC. For an easy channel, the ADC

can be configured as a 2-bit sampler if CTLE can equalize that channel, while for channels that require RX equalization in addition to TX FFE, ADC can be configured to a 6-bit mode for DSP equalization. However, the DSP is not implemented in [54], but the RX DSP equalization is performed in PC with recorded ADC output data.

1.2.2 Multi-Drop Link

Unlike the smoothly-decaying frequency response shape in point-to-point interconnects, multi-drop interconnects exhibits considerable notches in their frequency response [55]. This is because there are multiple possible electrical paths when modules or chips are connected to a bus for communicating between a TX and one of the RXs, which is known as multi-path distortion in wireless communications. In time-domain, signals that are arriving at the selected RX after traveling around different paths can cause destructive superposition at certain frequencies depending on the physical feature of the multi-electrical-paths. Due to the destructive superposition, the energy of the received signal has been significantly reduced as compared to the transmitted energy, that is translated into spectrum notches in frequency-domain. A typical example of multi-drop bus (MDB) is dynamic random access memory (DRAM) interface as main system memory, where multiple DIMMs are connected to a controller without matched impedance. Also, the interface between NAND-flash memory controller and stacked NAND dies is MDB. Often time, such reflections exhibit long-tail post-cursors in the pulse response, necessitating DFE to effectively cancel them out if the first reflective frequency comes below the Nyquist frequency of the transmitted signal. However, even without speaking about being power hungry, implementing such equalization is challenging since CMOS memory process technologies for DRAM manufacturing only offers low-cost and slow devices.

To overcome the technology-limited DRAM interface performance, various efforts have been investigated. In [56], analog multi-tone (AMT) signaling is employed to allocate the transmit power avoiding channel notches efficiently. By transmitting 2.5 Gb/s NRZ at baseband with 5 Gb/s quadrature phase-shift keying (QPSK)-modulated RF band, the prototype in [56] demonstrated 7.5 Gb/s data transmission over MDB that exhibits the first notch at 2.5 GHz with 40 dB loss. With the same signaling scheme, the prototype shown in [57] demonstrated 9 Gb/s per lane data-rate for the same type of channel with four parallel data bus with source synchronous clocking. Measurement results in [57] proved the far-end crosstalk reduction capability of the AMT signaling for dense MDB interconnects. [58] proposed baseband + RF-bands signaling similar to [56, 57] with higher RF-bands' constellation order. While the proposed TX in [58] can efficiently transmit energy in terms of power, the proposed signaling scheme requires a 4-bit DAC and ADC per sub-band, respectively for TX and RX. Moreover, if the first notch in channel frequency response is located at a lower frequency, AMT becomes impractical with an increased number of sub-channels that are required for communicating at a fixed aggregated data-rate. Above-mentioned works all use differential signaling, which is not preferred in DRAM interfaces due to its pin-inefficiency. Phase-difference modulation

scheme that modulates each clock edge by data information is proposed in [59]. While being able to be configured as a single-ended mode for 7.8 Gb/s/pin data-rate, the prototype in [59] demonstrated 2 pJ/b energy efficiency for data transmission over 2-drop MDB.

1.3 Contributions and Thesis Organization

In high-speed wireline TRX systems, among different equalization circuits, time-domain equalizers such as FFE and DFE analyze wireline TRX response in time-domain and apply equalization in time-domain. Frequency-domain equalizer such as CTLE views channel response in frequency-domain and applies equalization in the same domain. Moreover, most of the widely-researched signaling schemes are time-domain signaling such as NRZ/PAM-4. Particularly in MDB interfaces, communicating with time-domain signaling (NRZ/PAM-N at baseband) combined with frequency-domain signaling (QPSK/16-level quadrature-amplitude modulation (16-QAM) or 256-QAM at RF-bands) were explored by analyzing channel in frequency-domain point of view. This thesis contributes to two wireline TRX sub-domains with different approaches: point-to-point link and MDB interfaces.

- For MDB interfaces, instead of analyzing the system and applying signal processing in the same domain (either in time-domain or frequency-domain), this thesis analyzes the MDB TRX system in frequency-domain and propose a time-domain signaling scheme. By doing so, the proposed signaling scheme demonstrates greater bandwidth improvement compared to conventional time-domain equalization-based systems, with greater architectural simplicity as compared to systems employing frequency-domain signaling. A TX employing the proposed signaling scheme is demonstrated by measurement using programmable DAC with MDB board.

- For point-to-point interconnect with a highly lossy channel, this thesis proposes AMT signaling of which each frequency-domain sub-channel spectrum is single-sideband (SSB). The proposed scheme uses the channel's frequency response inversion property by up/down-conversion by analog mixers in TX/RX respectively. By doing so, the RX does not require any of FFE/CTLE/DFE for receiving at data-rate that is much greater than it would be possible without the presence of equalizers with time-domain signaling. Moreover, since the proposed signaling divides aggregate data-rate into using multiple frequency-domain sub-bands, the TRX's data-path can operate at sub-band-rate with relaxed timing. The proposed TRX is demonstrated by system-level measurement using oversampling DAC and ADC as TX and RX respectively, where up/down-conversions and filtering are performed in PC with oversampling to mimic analog behavior.

- For ultra-high-speed point-to-point link, e.g., 56 Gb/s, discrete multi-tone (DMT) (or called orthogonal frequency division multiplexing (OFDM) in wireless communications fields) modulation is employed. The RX is implemented in fully-digital circuits

following ADC without any analog equalizer in AFE. Unlike time-domain signaling that necessitates symbol-by-symbol feedback using DFE, OFDM enables parallel circuit implementation allowing the RX circuit to benefit from nanosecond-order critical path delay. A prototype RX chip including ADC and fully-synthesized digital RX is implemented in 14 nm FinFET process technology and demonstrated less than 3 pJ/b RX energy consumption at 56 Gb/s data-rate with BER $\leq 10^{-6}$ for channel exhibiting 18 dB loss at 14 GHz. This is the fastest reported DMT RX implemented in FinFET process with lowest energy-per-bit for electrical links.

- Another ADC-based RX for PAM-4 is proposed. Instead of time-domain symbol-by-symbol equalization, the proposed RX transforms a collection of consecutive time-domain received symbols into frequency-domain by Fourier transform and apply frequency-domain equalization. The frequency-domain-equalized symbols are then transformed-back into time-domain to reconstruct original time-domain PAM-4 data. Since time-domain circular convolution is equivalent to frequency-domain symbol-by-symbol multiplication in frequency-domain, the proposed method relaxes feedback equalizer's critical path with the help of domain-transformations and technique to make circular convolution equivalent to linear convolution. The proposed RX has demonstrated its feasibility to lossy wireline interfaces with 25 dB loss at 14 GHz channel by architectural modeling with register-transfer-level (RTL)-modeled RX.

The remaining parts of the thesis are organized as follows.

Chapter 2: Digital Spectrum Shaping Signaling In this chapter, a simple digital encoding scheme that shapes the transmitted signal's spectrum to mitigate energy loss caused by MDB frequency-domain notches is presented. The limitations of using NRZ signaling for MDB interfaces are analyzed, then the concept of digital spectrum shaping signaling is proposed. While the signaling scheme is proposed based on frequency-domain analysis, its time-domain behavior in reducing ISI/crosstalk is then analyzed. Then, a potential circuit implementation example is shown, followed by simulation results with measured MDB channel S-parameter. Measurement results using programmable DAC as TX for the proposed scheme are presented, and an enhanced modulation scheme is then introduced with pulse-response analysis, TX/RX design example, and simulation results, followed by a conclusion.

Chapter 3: Single-Sideband Analog Multi-Tone Signaling This chapter presents AMT signaling TRX architecture with SSB sub-channels for communication through lossy channels. Lossy-channel's self-equalization mechanism with RF up/down-conversion of upper-sideband-suppressed RF signal is analyzed. The proposed AMT/SSB TRX architecture is then shown with inter-channel-interference (ICI) analysis for RF sub-channels. Practical design considerations are discussed, then simulation results with measured S-parameter of example channel are shown. To demonstrate the feasibility of the proposed system, measurement results with oversampling DAC/ADC-based example system with digital pre-/post-processing in PC are presented followed by a conclusion.

Chapter 4: ADC-Based Wireline Receiver With Discrete Multi-Tone Signaling This chapter presents fully-digital ADC-based wireline RX with DMT modulation. While an 8-bit DAC is used as DMT TX with programmable data memory block, a TX architecture considered for generating equivalent DMT test sequence is presented. Then, the RX implementation details and measurement results under various conditions are shown. The full TRX system performance is compared with previous works followed by a conclusion.

Chapter 5: ADC-Based Fully-Digital PAM-4 Receiver This chapter presents a fully-digital ADC-based PAM-4 RX without the presence of analog front-end. It starts by reviewing basic high-speed wireline TRX architecture. Then, a frequency-domain equalization technique of the time-domain signal is presented. Simulation results and DSP implementation results are then shown, followed by a conclusion.

2 Digital Spectrum Shaping Signaling

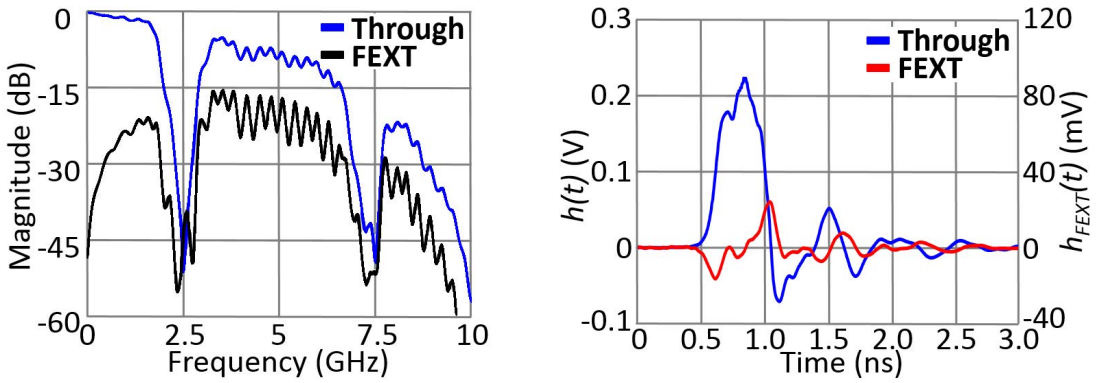
[1] This chapter presents a spectrum shaping signaling scheme and the corresponding transceiver architecture. The proposed signaling scheme can considerably reduce ISI and far-end crosstalk (FEXT) in MDB interfaces. The proposed TRX architecture features digital-style implementation rather than analog-based approach, which can provide a versatile and power-efficient silicon implementation. Moreover, the noise induced by FEXT can be greatly reduced by employing the proposed digital spectrum shaping signaling, and the TRX can customize to the communication channel by simple configuration while the aggregate data-rate is unchanged.

2.1 NRZ Signaling for Multi-Drop Interfaces

A multi-drop channel has its frequency notches at all odd multiples of f_{notch} where f_{notch} is the first notch frequency of a given multi-drop channel [62]. Fig. 2.1(a) shows measured through and FEXT frequency responses of an example 12-inch FR-4 MDB, with $f_{\text{notch}} = 2.5$ GHz [56]. The multi-path reflections cause long post-cursors on the pulse response as shown in Fig. 2.1(b), resulting in significant ISI. This example channel exhibits 45 dB attenuation at f_{notch} due to the disruptive superposition of the main and reflected signals at RX front-end, making the RX difficult to equalize the channel.

The nulls of the power spectrum of a random NRZ stream are located at n/T_{b} where n is an integer number and T_{b} is one-bit pulse duration [63]. Transmitting NRZ data stream over a channel that bears a notch around the Nyquist frequency necessitates complex equalizer including DFE with many number of taps to cancel out the reflected signals [56]. Although the MDB shown in Fig. 2.1(a) exhibits only 4 dB insertion loss at Nyquist for 5 Gb/s data-rate, the received eye diagram is closed due to the reflections.

[1] The contents of this chapter is based on: G. Kim, K. Gharibdoust, A. Tajalli, and Y. Leblebici, "A digital spectrum shaping signaling serial-data transceiver with crosstalk and ISI reduction property in multi-drop interfaces,", *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 63, no. 12, pp. 1126–1130, Dec. 2016 (©IEEE) [60] and G. Kim, C. Cao, K. Gharibdoust, A. Tajalli, and Y. Leblebici, "A time-division multiplexing signaling scheme for inter-symbol/channel interference reduction in low-power multi-drop memory links,", *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 64, no. 12, pp. 1387–1391, Dec. 2017 (©IEEE) [61].



(a) (b)

Figure 2.1 – Measured example multi-drop bus: (a) through and FEXT frequency responses, (b) pulse response with 200-ps pulse-width.

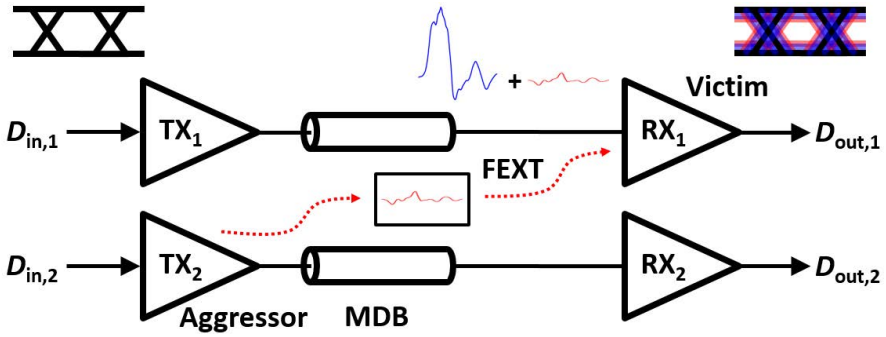
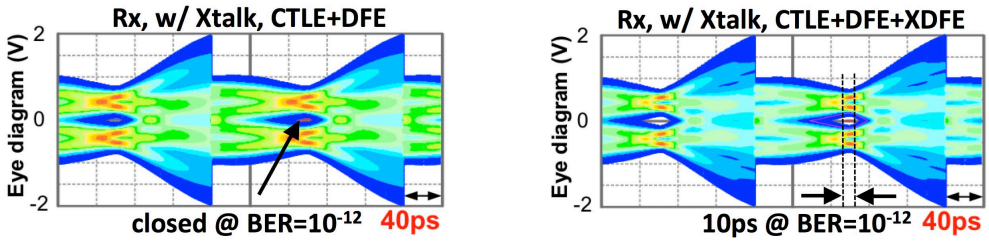


Figure 2.2 – Crosstalk from an aggressor lane to a victim lane.



(a) (b)

Figure 2.3 – Eye diagram of received 5 Gb/s single-ended NRZ signal with a CTLE followed by a 10-tap DFE, (a) without FEXT cancellation and (b) with 1-tap XFFE+1-tap XDFE.

The effect of crosstalk should be addressed when multiple closely-spaced lanes transmit data simultaneously, as depicted in Fig. 2.2. Measurements on the example MDB traces indicate that the dominant crosstalk source is inductive coupling. The transfer function of the inductive FEXT, $H_{\text{FEXT}}(w)$, can be modeled as the derivative of the through-response of the channel [56]. The measured FEXT pulse response is shown in Fig. 2.1(a). Transmitting NRZ data stream on the adjacent lanes creates long-tail FEXT as shown in Fig. 2.1(b) (red line), hence degrades the

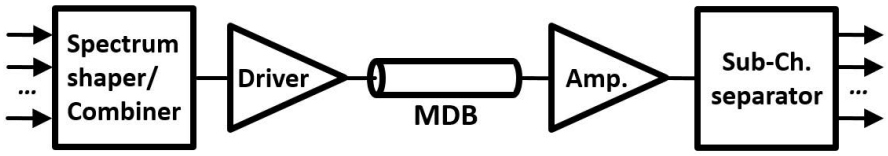


Figure 2.4 – Overall system architecture of the proposed TRX.

signal integrity on the victim channel. However, FEXT cannot be canceled out by conventional DFE unless more complicated equalizer architecture such as cross-equalizer is employed [64], which makes the equalizer even more power-hungry. Fig. 2.3(a) shows that although an RX equalizer consisting of a CTLE followed by a 10-tap DFE reduces ISI, the received eye is closed at BER = 10^{-12} due to the FEXT. In this simulation, a 5 Gb/s NRZ stream is transmitted over MDB shown in Fig. 2.1 with TRX non-idealities including 2 ps rms random jitter (Rj), 10 mV_{rms} additive white Gaussian noise (AWGN) on TX output, 8 mV_{pp} RX sampler offset and 40 ps output driver rise/fall time. Fig. 2.3(b) shows the received eye with additional 1-tap RX cross-feed-forward equalizer (XFFE) and 1-tap RX cross-DFE (XDFE) for FEXT reduction, so as to meet at least 5% horizontal eye opening at BER = 10^{-12}.

2.2 Digital Spectrum Shaping Signaling for ISI and Crosstalk Reduction

2.2.1 ISI/Crosstalk Reduction Scheme

One way to minimize energy waste of a transmitted NRZ signal is to reduce the data-rate so that the first null of its power spectrum matches the first channel notch, given a multi-drop channel. However, adjusting the data-rate of an NRZ data stream changes the communication speed if the total number of parallel NRZ stream is fixed, which is not preferable. The signaling scheme that will be shown in this section provides a solution to overcome this issue, by transmitting multiple parallel NRZ data stream over a single multi-drop channel applying a multiplexing-based spectrum shaping technique, and by de-multiplexing the received signal into each parallel stream at the receiver side. This can be realized by a TRX of which simplified architecture is depicted in Fig. 2.4.

Transmitting data with ($m \times f_{\mathrm{notch}}$) b/s data-rate over a multi-drop channel exhibiting characteristics such as frequency domain and time domain responses shown in Fig. 2.1 can be considered, where m is an integer number. In order to minimize energy waste around channel notches, we deserialize a single ($m \times f_{\mathrm{notch}}$) b/s NRZ data stream into m sub-channels with (f_{notch}) b/s each, thus, having matching nulls to the multi-drop notches. The sub-channels are then multiplexed by non-overlapping clocks before being summed so that the received stream can be re-separated into the m original sub-channels on the receiver side. The time domain waveform of the spectrum shaping signaling transmitter is illustrated in Fig. 2.5. The non-overlapping clocks CK_{i} and CK_{j} where $i, j \in \{1, 2, \cdots, m\}, i \neq j$, are mutually orthogonal.

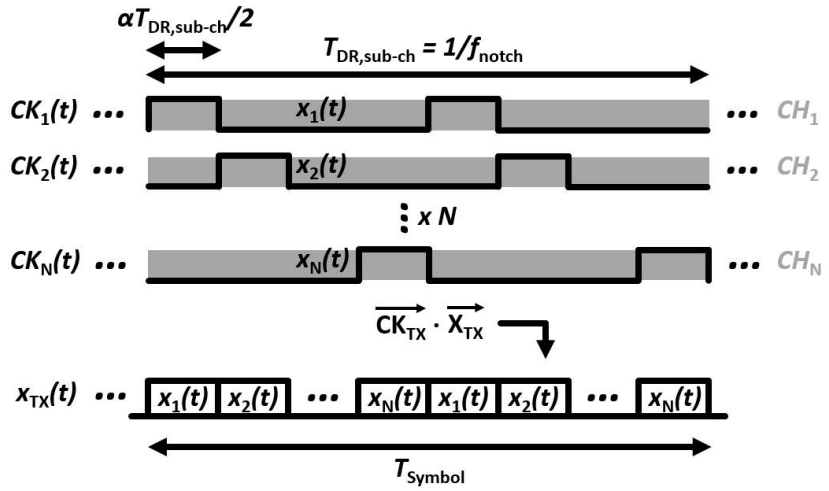


Figure 2.5 – The time domain flow of the spectrum shaping signaling transmitter.

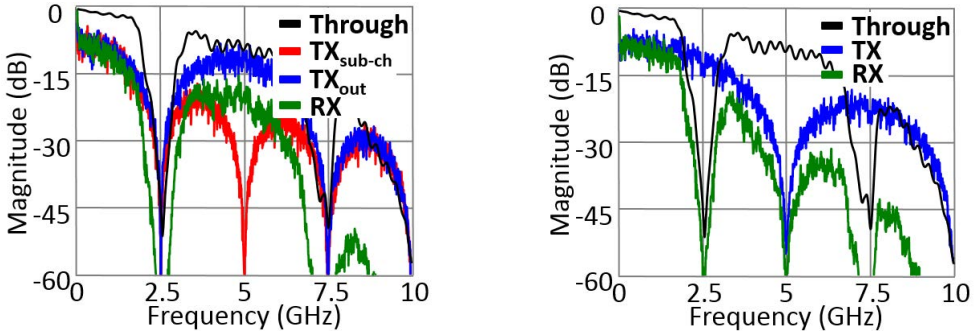


Figure 2.6 – Power spectrums of signals (a) for the proposed TRX and (b) for the conventional NRZ TRX, shown with the reference multi-drop channel frequency response.

The transmitter output signal in time domain ($x_{\mathrm{TX}}(t)$ in Fig. 2.5) can be expressed as

$$x_{\mathrm{TX}}(t) = \overrightarrow{\mathbf{X}_{\mathrm{TX}}(t)} \cdot \overrightarrow{\mathbf{CK}_{\mathrm{TX}}(t)}$$

where $\overrightarrow{\mathbf{X}(t)} = \{x_1(t), x_2(t), \cdots, x_{\mathrm{m}}(t)\}$, $\overrightarrow{\mathbf{CK}_{\mathrm{TX}}(t)} = \{CK_1(t), CK_2(t), \cdots, CK_{\mathrm{m}}(t)\}$, and the operator $(\cdot)$ is dot product. The resulting power spectrum of the transmitted signal, $x_{\mathrm{TX}}(t)$, is shown in Fig. 2.6(a) as a blue line, given that there are two sub-channels (x_1 and x_2) and $f_{\mathrm{notch}} = 2.5$ GHz. Fig. 2.6 shows how the notch in a multi-drop channel affects the spectrum of a serial data stream with two different signaling schemes, i.e., NRZ and spectrum shaping signaling. From Fig. 2.6(b), it can be seen that the power spectrum of the received 5 Gb/s NRZ stream has been severely harmed by the first channel notch around Nyquist frequency, which results in closed eye diagram unless DFE properly cancels out the reflective post-cursors. On the other hand, the power spectrum profile of the received spectrum shaped signal in Fig. 2.6(a) shows that the spectrum shaping signaling can make the signal's spectrum avoid the notch to

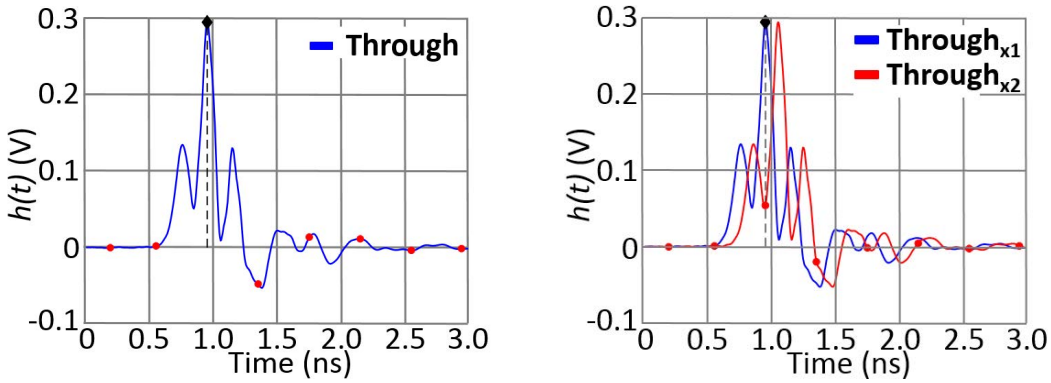


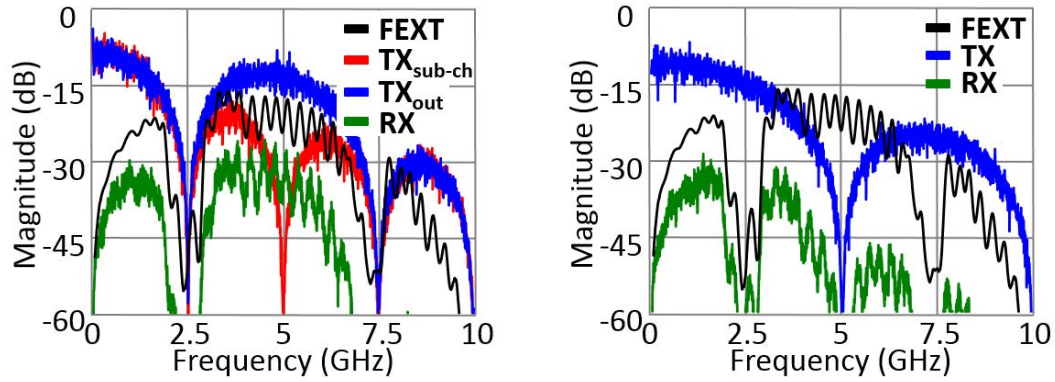
Figure 2.7 – (a) Effective pulse response and its pre/post-cursors of a modulated 2.5 Gb/s each and (b) the ICI pre/post-cursors.

minimize the signal integrity corruption by multi-drop notches.

As the transmitter multiplexing clocks ($\overrightarrow{\mathbf{CK}_{\mathrm{TX}}(t)}$) are mutually orthogonal, the transmitted signal $x_{\mathrm{TX}}(t)$ carries information over a limited frequency bandwidth and can be separated on the receiver side, resulting in higher spectral efficiency. The phase misalignment between sub-clocks may change the orthogonality among the sub-channels, increasing ICI. Given a target total data-rate and a sub-channel data-rate, by selecting a proper number of sub-channels m that accommodates multi-drop channel, the power spectrum of the transmitted signal can minimize the effect of multi-drop notches. The resulting pulse response for the frequency-shaped 2×2.5 Gb/s data transmission is shown in Fig. 2.7(a). The effectively transmitted pulse is a sequence of $\cdots 0010100 \cdots$ with 100 ps bit-width, not a sequence of $\cdots 00100 \cdots$ with 400 ps bit-width. Fig. 2.7(b) shows the pre/post-cursors (red dots) of a sub-channel causing ICI on a victim sub-channel in this example case. The amount of contribution of ISI and ICI to the main pulse response as jitter sources will be shown in the following sub-section.

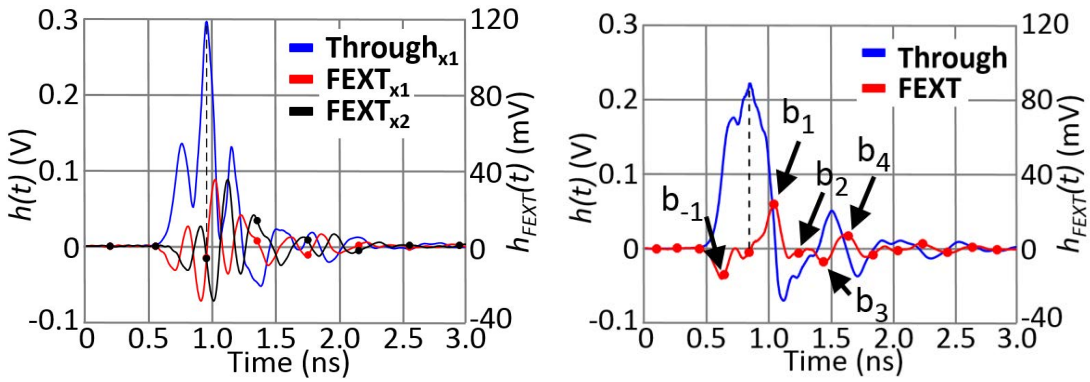
In a similar way, the spectrum shaping signaling affects FEXT reduction as well, which is the dominant crosstalk noise source in communicating over an MDB. Fig. 2.8(a) shows the spectrum of the transmitted aggressor signal (blue), the sub-channel spectrum (red), the FEXT spectrum on the victim lane (green), and the FEXT frequency response of the considered MDB (black line), when the spectrum shaping signaling scheme is applied. From Fig. 2.8(a), it can be observed that by applying the proposed spectrum shaping technique, the FEXT can avoid MDB notches in the same manner as through response. On the other hand, as shown in Fig. 2.8(b), the FEXT spectrum on the receiver side of the victim lane has experienced the MDB notches severely, and it would result in a long-tail of pulse response due to reflections.

Fig. 2.9 visualizes the crosstalk reduction scheme in time domain, for the case where $m = 2$ and $f_{\mathrm{notch}} = 2.5$ GHz. The zeros or amplitudes close to zero (black and red dots) of crosstalk pulse response fall on top of the victim cursor as shown in Fig. 2.9(a), thereby not adding



(a) (b)

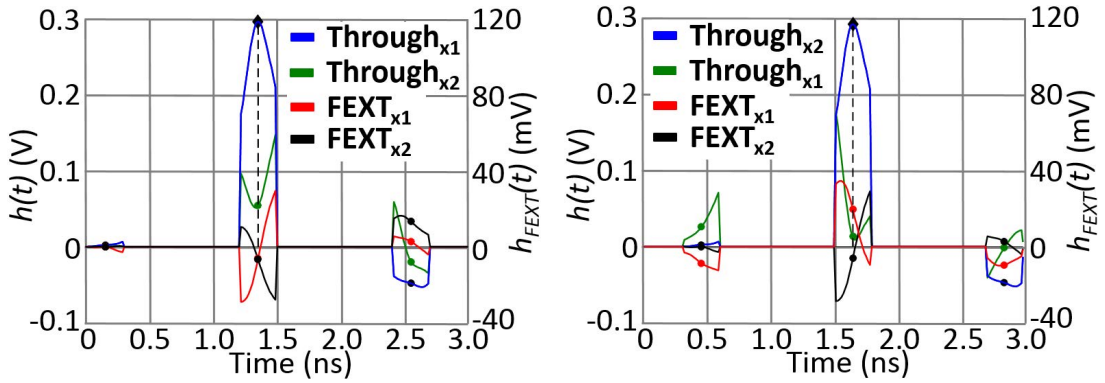
Figure 2.8 – MDB FEXT frequency response and power spectrum envelopes for (a) 2 × 2.5 Gb/s modulated signals and (b) 5 Gb/s NRZ.



(a) (b)

Figure 2.9 – FEXT and through response for, (a) 2-sub-channel 2.5 Gb/s each modulated stream and (b) 5 Gb/s NRZ stream.

considerable FEXT-induced jitter to the main cursor of the victim pulse response. However, there exist m-aggressor FEXT sources for one victim lane, as m bits over m different sub-channels are transmitted during one symbol UI. Therefore, m FEXT pulse responses that are mutually phase-shifted have to be considered for FEXT analysis. In Fig. 2.10, the effective pulse responses of Fig. 2.9(a) seen from the receiver samplers are shown, focusing on some important cursors around the main cursor. Despite the presence of multiple ripples in the through, ICI and FEXT pulse responses, the effective cursors that will overlap onto the main-cursor of the victim lane at the optimum receiver sampling point remain reasonably small. In case of transmission of high data-rate NRZ stream of which Nyquist frequency is higher than f_{notch} over a dense interconnect, peaks of pre/post-cursors of FEXT response fall to the main peak of the through response, resulting in a significant contribution to the deterministic jitter. Fig. 2.9(b) shows an example with 5 Gb/s NRZ stream per lane over the example MDB.



(a) (b)

Figure 2.10 – Effective pulse responses of sub-channels with ISI, ICI and FEXT for valid time-division sampling windows on the receiver side for (a) x_1 and (b) x_2.

Table 2.1 – Worst-case contributions of each deterministic jitter sources in percentage to the main pulse response.

Channel	ISI	ICI	FEXT$_{total}$	DJ$_{total}$
5 Gb/s NRZ [%]	119.8	-	29.2	149.0
2.5 Gb/s - x_1 [%]	30.7	28.6	17.5	76.8
2.5 Gb/s - x_2 [%]	30.7	21.5	26.4	78.6

The worst-case contributions in terms of percentage of each of the deterministic jitter sources to the main pulse response are listed in Table 2.3, for both of 5 Gb/s NRZ signal and 2 × 2.5 Gb/s frequency-shaped signal, and without equalization. It can be seen that the total jitter percentage for 5 Gb/s NRZ stream is above 100%, resulting in a closed received eye. On the other hand, the percentage of the total jitter of the 2-sub-channel frequency shaped signal to the main response is 78.6%, guaranteeing ideally 21.4% vertical eye opening at the best sampling point without taking any Rj sources into account.

2.2.2 Hardware Architecture Example

Fig. 2.11(a) and Fig. 2.11(b) show the example transmitter and receiver architectures, respectively, to realize the proposed signaling scheme. On the transmitter side, a serial ($m \times f_{\text{notch}}$) b/s binary data stream is deserialized into m-parallel streams with data-rate of (f_{notch}) b/s each. The number of sub-channels, m, can vary from 1 to N according to the desired total data-rate and MDB characteristics, where N is the maximum supported number of sub-channels. The m sets of data streams are then encoded by an encoder, which is basically a MUX of which select signal is clock vector, $\overrightarrow{\mathbf{CK}_{\text{TX}}(t)}$. The encoder streams out a sub-channel of which corresponding select signal (a corresponding component of $\overrightarrow{\mathbf{CK}_{\text{TX}}(t)}$) is high while the other select signals are all low. The encoded serial stream is transmitted to the channel by a single-ended

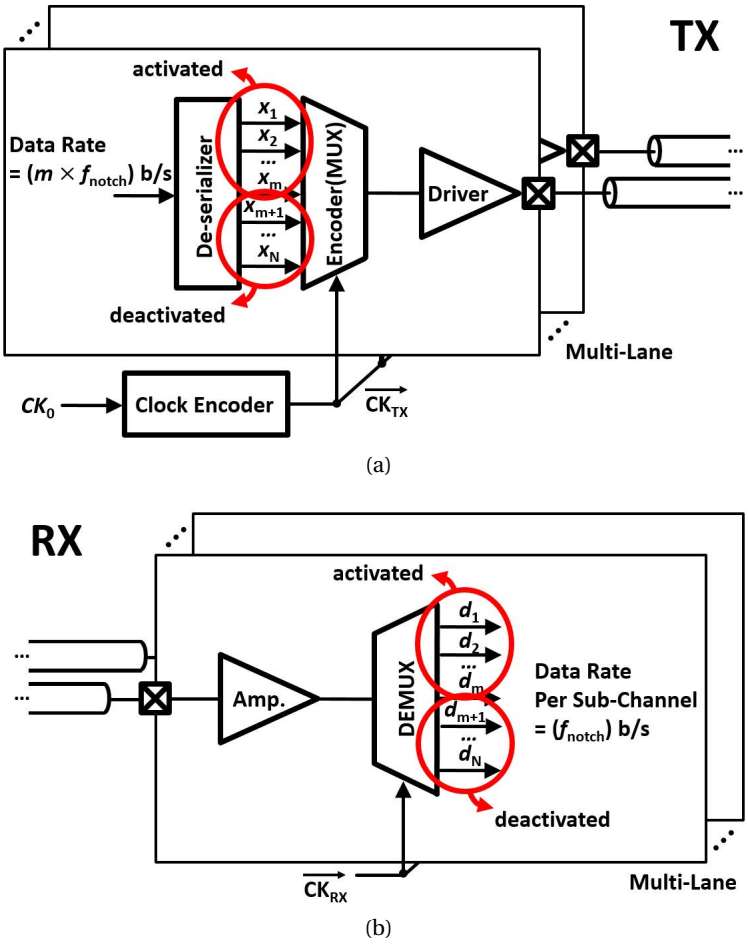


Figure 2.11 – Proposed (a) transmitter architecture and (b) receiver architecture.

output driver. On the receiver side, an amplifier restores the logic level of the incoming signal, and the following demultiplexer (DEMUX) recovers the original m parallel data stream.

Since the proposed spectrum shaping signaling scheme is realized by a *cyclic* multiplexing/demultiplexing of multiple sub-channels as illustrated in Fig. 2.5, clock vector generator is the core block that differentiates the proposed TRX from PAM-N TRXs. The block diagram of a fully-digital-style clock vector generator is shown in Fig. 2.12. A $(m \times f_{\text{notch}})$ GHz reference clock (CK_0) generates N sub-clocks $(CK_{1:N})$ with digital sequential circuits. Double-edge-triggered DFFs should be employed as sequential elements in clock vector generator so as to relax the reference clock frequency. Although the clock vector generator can be realized in fully-digital, its layout has to be drawn carefully to provide fair matching among different clock phases. The sub-clocks then turn on/off the switches of the encoder (N-to-1 MUX) for corresponding sub-channel data streams, as shown in Fig. 2.13. The clocks $CK_j, m < j \leq N$ are deactivated always having logic level 0 since the *count* signal does not become higher than $m-1$ due to the counter, and in so doing, the encoder outputs the modulated signal for only the first m sub-channels. For the receiver clocking, a source-synchronous interface with a

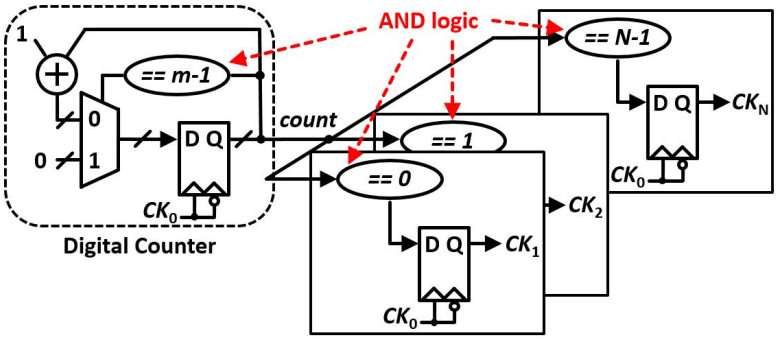


Figure 2.12 – Block diagram of clock vector generator.

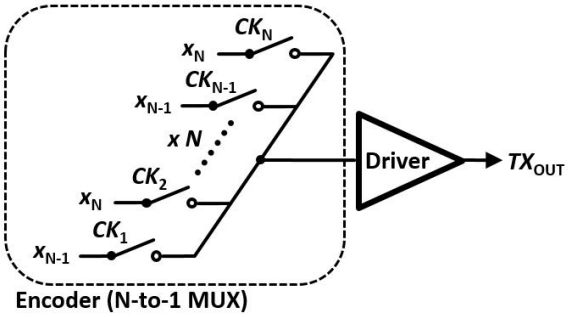
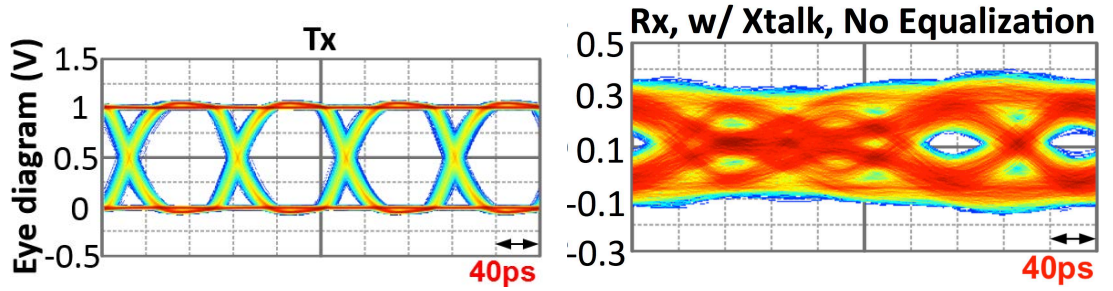


Figure 2.13 – Encoding MUX and its data-path and control signals.

delay-locked loop (DLL)-based CDR circuitry can be employed, since it does not accumulate jitter and consumes less power as compared with a PLL-based CDR [65].

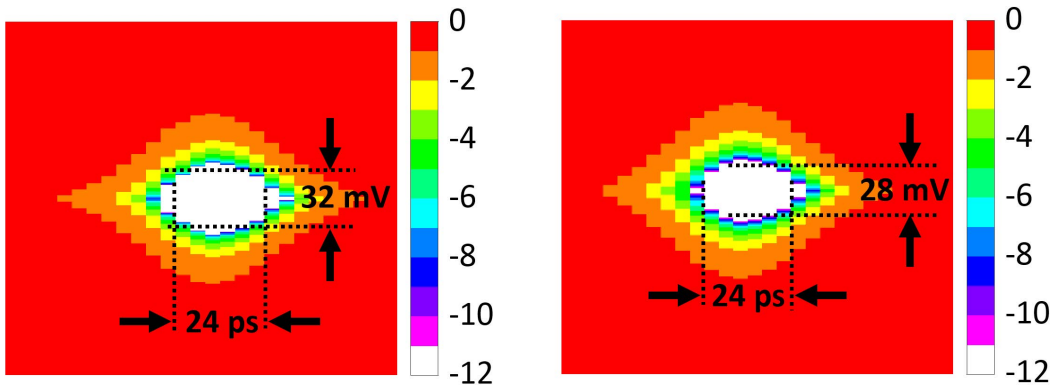
2.2.3 Simulation Results

The proposed TRX architecture and spectrum shaping signaling have been validated through system-level modeling for two-channel 2 × 2.5 Gb/s data-rate. A two-lane 12-inch FR-4 MDB exhibiting characteristics shown in Fig. 2.1 is used as data transmission medium. On each sub-channel of the transmitter, Rj of 2 ps rms and 5 ps peak-to-peak (pp) phase mismatch for sub-clocks have been assumed, and 10 mV_{rms} AWGN has been added to the TX driver output. Inter-channel skew is considered to be 1 ps, and 8 mV_{pp} sampler offset non-ideality is assumed. The eye diagram on the TX output is shown in Fig. 2.14(a), and the received eye is shown in Fig. 2.14(b). From Fig. 2.14(b), it can be observed that two eyes are in one data transmission period of one sub-channel (one symbol UI) with 100 ps time shift each other, as two multiplexing clocks on the transmitter side have 100 ps time shift (π radian phase shift) between each other. The BER eye diagrams for both sub-channels are shown in Fig. 2.15. After having considered the effects coming from aforementioned deterministic jitter sources and non-idealities, the BER eye diagrams show 24 ps horizontal opening and at least 28 mV vertical opening at BER = 10^{-12} without employing CTLE or DFE. The Rj, the clock phase



(a) (b)

Figure 2.14 – Eye diagrams (a) on the TX output and (b) on the receiver front-end with the FEXT, for a 2 × 2.5 Gb/s proposed TRX.



(a) (b)

Figure 2.15 – BER eye diagram for (a) x_1 sub-channel and (b) x_2 sub-channel, taking the effect of some important deterministic jitter sources into account.

mismatch, the inter-channel skew and the sampler offset resulted in 29 ps more eye closure as compared to the case without the presence of the aforementioned non-idealities. The clock phase mismatch can potentially be reduced by applying a timing mismatch correction technique [66], which may improve the eye quality.

As discussed in Section II, simulation results show that FEXT noise of the neighboring aggressor closes the victim channel RX eye, even with an aggressive equalization setting. Hence, to have similar horizontal eye opening in NRZ and the proposed signaling scheme (5 Gb/s at BER = 10^{-12}), one should employ cross-wire equalization scheme [64] to cancel out the crosstalk-induced noise at sampling points. System-level simulation results show that by removing 5 Xtalk samples ([b_{-1}, b_1, b_2, b_3, b_4] in Fig. 2.9(b)) with 1-tap XFFE, 4-tap XDFE, and with 5 additional DFE taps (thus 15-tap DFE), the horizontal opening of NRZ signaling for 5 Gb/s at BER = 10^{-12} becomes similar to the proposed approach (24 ps, 12% UI of 5 Gb/s NRZ), which does not require any additional equalization circuit. Indeed, in addition to power overhead of such complicated cross-equalization technique, the CDR circuit for these techniques become

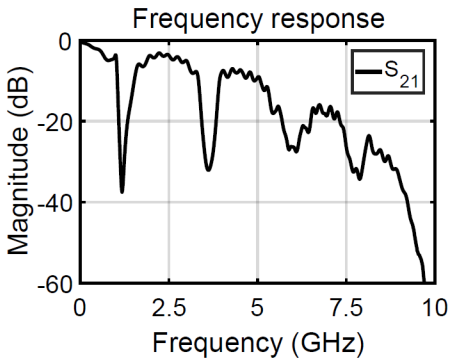


Figure 2.16 – MDB channel frequency response used for the measurement.

critical and imposes a sophisticated calibration circuit[2], which increases power consumption and circuit complexity.

2.2.4 Supplementary Experimental Results

To validate the proposed signaling scheme with experiment, measurement using a general-purpose DAC are performed. The system are measured for two different N-sub-channel modes, i.e., $N \in \{2,3\}$ for channel of which frequency response is shown in Fig. 2.16. Fig. 2.17(b) shows the 1.2 Gb/s NRZ spectrum's main lobe is almost not harmed by the notch in MDB frequency response since the first notch frequency is much higher than 1.2 Gb/s NRZ signal's Nyquist frequency. Hence, eye diagram shown in Fig. 2.17(a) is clearly open with large vertical/horizontal margins. On the other hand, it can be seen in Fig. 2.17(c) that the eye diagram is closing with 2.2 Gb/s NRZ signaling while it is still open, due to the fact that the near-Nyquist frequency components around 1.1 GHz are getting harmed by the notch as can be seen in Fig. 2.17(d). With 2.6 Gb/s NRZ, the eye shown in Fig. 2.17(e) is completely closed as the frequency components around 1.2 GHz (notch frequency) are severely harmed by the MDB notch as can be seen in Fig. 2.17(f).

Eye diagrams and spectrums with the proposed spectrum shaping signaling are shown in Fig. 2.18. Since the first notch is located at 1.2 GHz, sub-channel data-rate is 1.2 GHz except for the case using two sub-channels. Fig. 2.18(a) shows that the eye diagram is open with 2×1.3 GHz data-rate, even if the sub-channel data-rate does not perfectly match the first notch frequency. Its corresponding spectrum shown in Fig. 2.18(b) demonstrates that most of the energy contained in baseband and RF-band is not severely harmed by the notch. To increase the total data-rate from 2.4 Gb/s to 3.6 Gb/s, three sub-channels are used while each of them has a data-rate of 1.2 Gb/s. Since the sub-channels share the same frequency bands, the received spectrum practically does not differ from the case with two-sub-channels, as can be seen in Fig. 2.18(d). The eyes are open as shown in Fig. 2.18(c) while they are more closed as compared to those with two-sub-channels due to the increased ICI. It demonstrates that

[2] To align the XDFE sampling clock with the through pulse response.

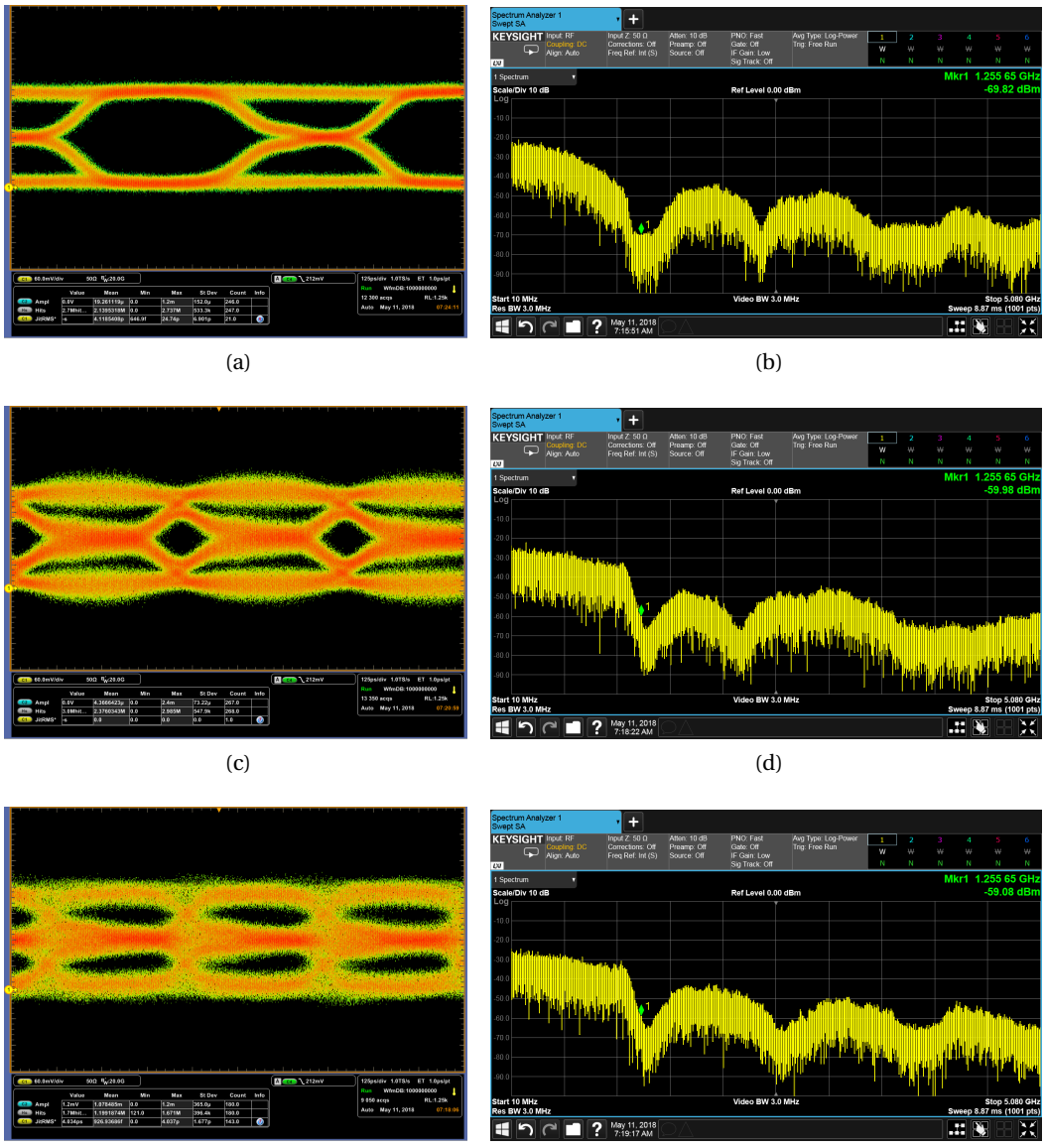
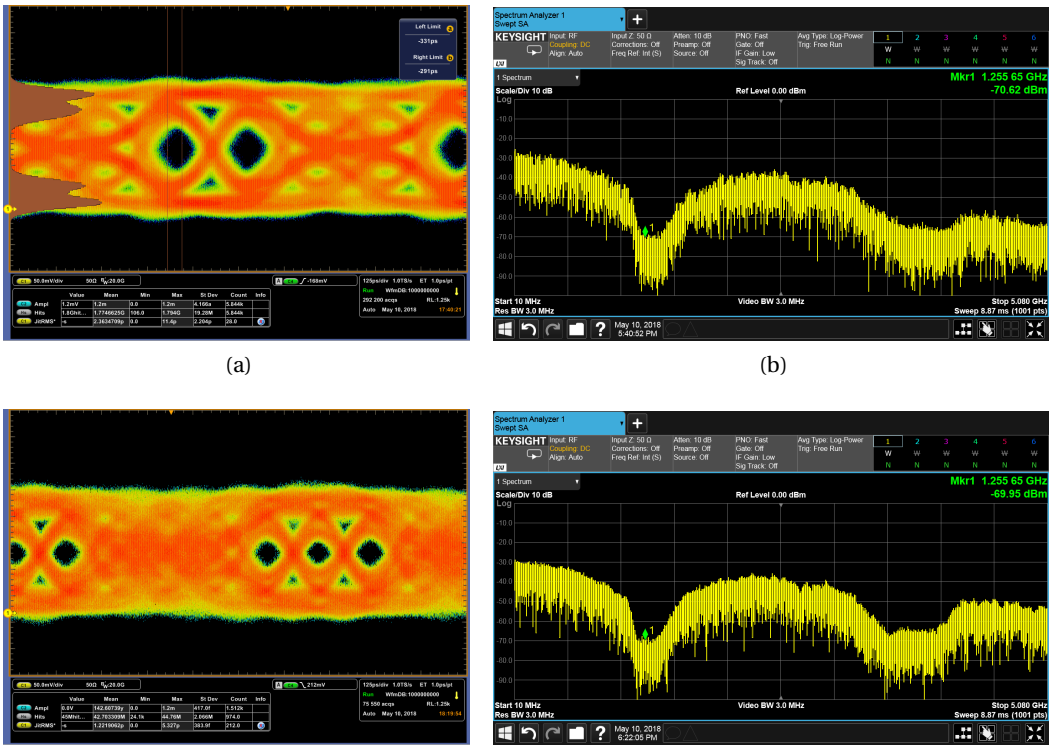


Figure 2.17 – Eye diagrams of NRZ data at the end of MDB shown in Fig. 2.16 with 1.2 Gb/s (a), 2.2 Gb/s (c), 2.6 Gb/s (e) and their corresponding spectrum (b), (d), and (f), respectively.

the proposed signaling scheme can make the RX eye open at 3.6 Gb/s for the reference MDB while NRZ signaling provides a completely closed eye at 2.6 Gb/s for the same channel. Table 3.2 compares this work with other relevant works.



(a) (b)

(c) (d)

Figure 2.18 – Eye diagrams of signal at the end of MDB shown in Fig. 2.16 using spectrum shaping signaling with 2×1.3 Gb/s (a), 3×1.2 Gb/s (c) and their corresponding spectrum (b) and (d), respectively.

Table 2.2 – Performance Comparison With Other Relevant Works.

Ref.	**[67]**	**[68]**	**[69]**	**This work**
Channel	4.7″ MDB	7.5″ MDB	4.7″ MDB	**12″ MDB**
Drops	2	4	6	**2**
Data rate (Gb/s)	3.8	3.4	5.8	**Notch @2.5 GHz: 5.0 (simulated) Notch @1.2 GHz: 3.6 (measured)**
Signaling	NRZ	NRZ	Duobinary	**Spectrum shaping**
I/O type	Single-ended	Single-ended	Differential	**Single-ended**
EQ	2-tap DFE	2-tap DFE	7-tap DFE	-
BER	10^{-12}	10^{-12} / 60 ps	10^{-10} / 62 ps	**10^{-12} / 24 ps**

2.3 ICI Reduction for Digital Spectrum Shaping Signaling

While communicating with digital spectrum shaping signaling can effectively avoid MDB notches, it is shown that a particular sub-channel's pre-cursors and post-cursors can affect

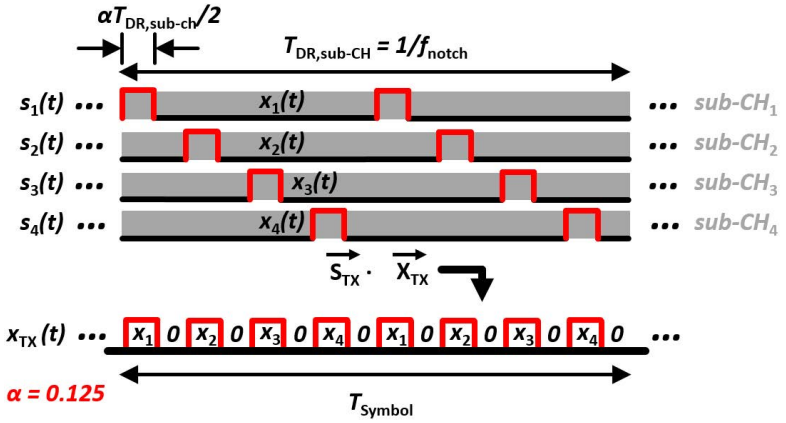


Figure 2.19 – Time-domain signal flow of the proposed signaling scheme by introducing guard interval.

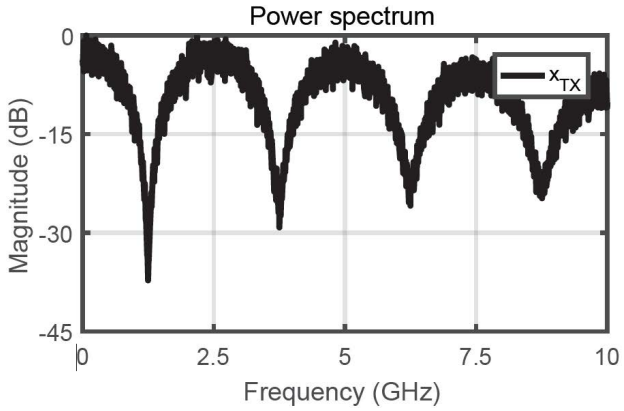


Figure 2.20 – Magnitude of the power spectrum of $x_{\mathrm{TX}}(t)$.

its neighboring sub-channels, worsening their signal integrity. Although the exact numbers can vary depending on the communication configuration such as data-rate and transmission medium, it is noticeable from Table 2.3 that the contribution of ICI can rise as high as 37% to the total deterministic jitter (Dj_{total}), while ISI contributes 40% in the considered simulation environment, when the number of sub-channels is configured to 2. With the increased number of sub-channels, the ICI contribution to Dj_{total} can be raised and becomes more critical than ISI and/or crosstalk jitter.

2.3.1 ICI Reduction Mechanism

Fig. 2.19 shows the time-domain signal flow of the improved signaling scheme, where a guard-interval is inserted between adjacent sub-channel data samples, resulting in reduced ICI. While the number of sub-channels is set to 4 in Fig. 2.19, it can be configured depending on the MDB channel profile and the target DR, and the sub-channel select signals' ($s_{1:4}(t)$) pulse-width changes accordingly. Noting that the first notch of the MDB channel is located

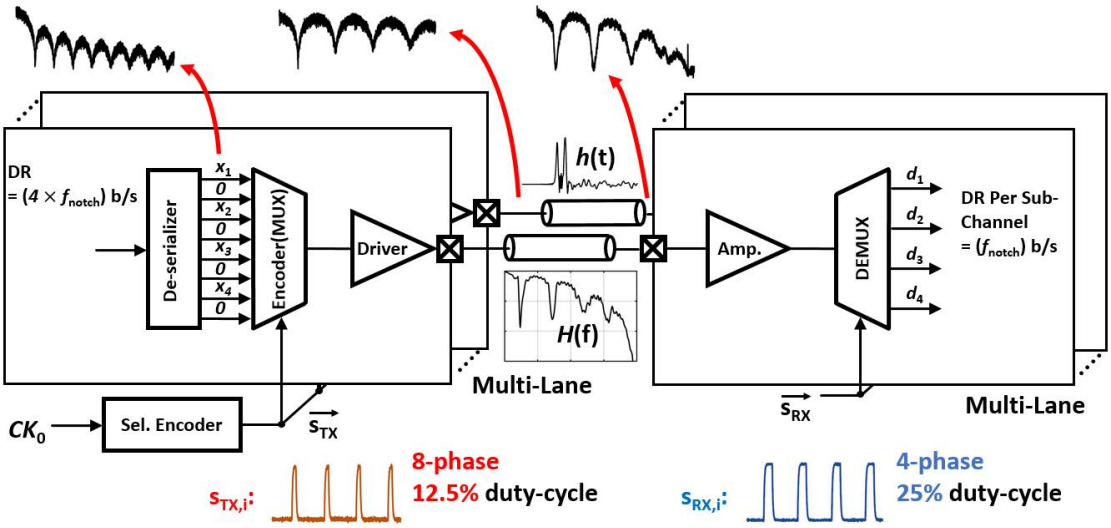


Figure 2.21 – TDM-based serial data TRX architecture employing the proposed signaling scheme, with the maximum number of sub-channel being 4.

at f_{notch}, a serial data stream at $N \times f_{\text{notch}}$b/s is de-serialized to N low-DR NRZ streams, with $DR_{\text{sub}} = f_{\text{notch}}$b/s. Then, the power spectrum $X_{\text{i}}(f)$ (in magnitude) of each sub-stream $x_{\text{i}}(t)$, where i is sub-channel index, can be expressed as

$$X_{\text{i}}(f) = \frac{T_{\text{b}}}{2\pi}\left[\frac{\sin(\pi f T_{\text{b}})}{(\pi f T_{\text{b}})}\right]^2 \tag{2.1}$$

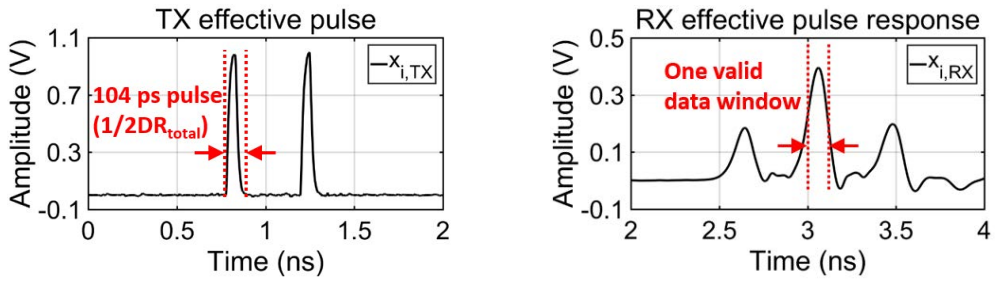
where T_{b} is the period of each sub-channel bit, i.e., $1/f_{\text{notch}}$ [63]. At the TX output, $x_{\text{TX}}(t)$ can be viewed as the sum of $x_{\text{i}}(t)$ that have been multiplied (AND-ed in digital) by the multiplexing signals $s_{\text{i}}(t)$, where the power spectrum of $s_{\text{i}}(t)$ (in magnitude) can be expressed as

$$S_{\text{i}}(f) = \alpha A\left[1 + 2\sum_{k=1}^{\infty}\frac{\sin(\alpha k\pi)}{k\pi}\cos(2k\pi f_{\text{sel}}t)\right] \tag{2.2}$$

where α is the duty cycle of $s_{\text{i}}(t)$ which can be expressed as $\alpha = \frac{1}{2N}$, A is the amplitude of $s_{\text{i}}(t)$, f_{sel} is the frequency of $s_{\text{i}}(t)$. Noting that multiplication in time-domain is equivalent to convolving in frequency-domain, each time-division multiplexed sub-channel component of the resulting TX output stream can be expressed as

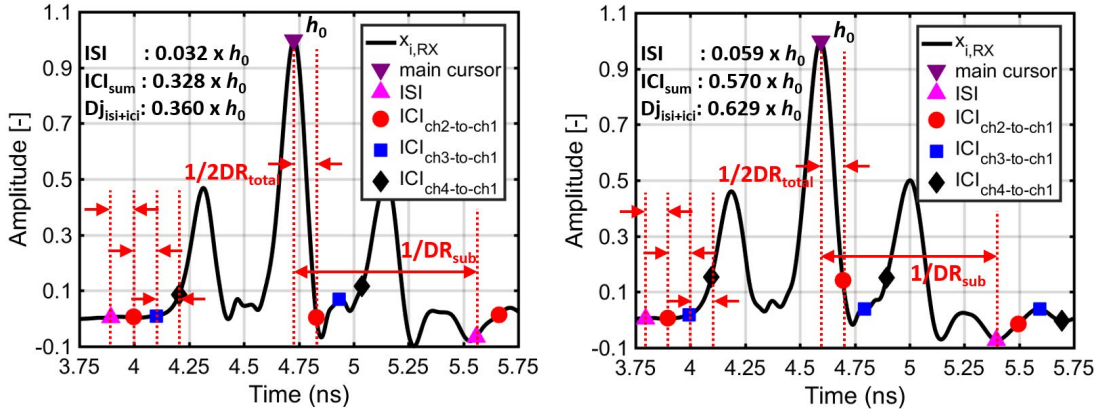
$$X_{\text{i}}(f) * S_{\text{i}}(f) = \alpha A\left[X_{\text{i}}(f) + 2\sum_{k=1}^{\infty}\frac{\sin(\alpha k\pi)}{k\pi}\left\{X_{\text{i}}(f - kf_{\text{sel}}) + X_{\text{i}}(f + kf_{\text{sel}})\right\}\right] \tag{2.3}$$

where $X_{\text{i}}(f)$ is Fourier transform of a single sub-channel data stream and $S_{\text{i}}(f)$ is Fourier transform of the corresponding multiplexing signal. The resulting power spectrum $X_{\text{TX}}(f)$ (in magnitude) of $x_{\text{TX}}(t)$ is shown in Fig. 2.20, where $X_{\text{TX}}(f) = \sum_{i=1}^{N}(X_{\text{i}}(f) * S_{\text{i}}(f))$. As the first spectral null location corresponds to the first notch frequency, the ISI due to the disruptive superposition of the reflected waves to the forward wave can be minimized. The TX output



(a) (b)

Figure 2.22 – Effective transmitted pulse (a) and the effective pulse response (b) with 4 sub-channels and DR_{total} = 4.8 Gb/s.



(a) (b)

Figure 2.23 – Effective pulse responses and their main cursor, ISI, and ICI cursors (a) for the proposed signaling scheme and (b) for the signaling proposed in Chapter 2.2.1.

spectral shape of the proposed signaling TRX is quite similar to the one proposed in [60] and exhibits the same ISI and FEXT reduction property.

Fig. 2.21 depicts the overall TRX architecture for the realization of the enhanced signaling scheme, with the maximum number of sub-channel being 4. Frequency-domain and time-domain characteristics of the reference MDB used in this work are shown in the inset of Fig. 2.21 (H(f), h(t), respectively). The first channel notch in the frequency response is located at 1.2GHz followed by multiple notches at odd-integer multiples of 1.2GHz, resulting in significant reflection post-cursors in MDB impulse response (h(t)). For the proposed signaling, f_{sel} has to be twice as fast as the DR_{sub}. As a result, two pulses represent a transmitted bit '1' as shown in Fig. 2.22(a), and consequently, a response shown in Fig. 2.22(b) has to be considered as the effective pulse response. The ISI and ICI noise amplitude can be obtained from the effective pulse response. Fig. 2.23(a) shows the effective pulse response of the proposed signaling and its main, ISI, and ICI cursors for 4-sub-channels configuration at total DR (DR_{total}) = 4.8 Gb/s with DR_{sub} = 1.2 Gb/s, where the amplitude of the pulse response

Table 2.3 – Contribution of each deterministic jitter sources in percentage to the main cursor.

Noise [% to h_0]	ISI	ICI_2	ICI_3	ICI_4	$Dj_{isi+ici}$
NRZ	367.7	-	-	-	367.7
w/o guard interval	5.9	16.6	9.7	30.8	62.9
w/ guard interval	3.2	2.6	9.0	21.2	36.0

is normalized to 1. As can be seen in Fig. 2.23(a), there are three ($N-1$, with $N=4$) ICI aggressors and each of them contributes to signal-to-noise ratio (SNR) degradation of the victim sub-channel at the main cursor (h_0) sampling point. Therefore, the total noise coming from the aggressor sub-channels, ICI_{sum}, is the sum of the magnitude of all ICI cursors, and the total ISI-induced noise can be obtained in the same manner. Fig. 2.23(b) shows the effective pulse response and the main, ISI, and ICI cursors with the signaling scheme proposed in [60], in the same communication condition. By introducing a time-domain guard-interval between neighboring sub-channels, the width of the pulse-response around the main cursor becomes narrower. Consequently, the $ICI_{ch2-to-ch1}$ cursor following h_0 is significantly reduced and $ICI_{ch4-to-ch1}$ cursors are considerably decreased as well. As a result, the total deterministic noise induced by ISI and ICI has been decreased by 43%. Table 2.3 summarizes the noise amplitude from various sources to the main cursor of the pulse response. It is worth noting that the NRZ pulse response is obtained by transmitting a single-pulse with its pulse-width being $T_{pulse} = \frac{1}{DR_{total}}$.

2.3.2 TRX Architecture Example

TX Data-Path

While the overall TRX architecture for realizing the proposed signaling scheme is shown in Fig. 2.21, a more detailed TX block diagram is shown in Fig. 2.24. The internal signals are indicated as black italic texts, and the operating speeds at the corresponding nodes are indicated as red italic texts. In the example circuit, the number of sub-channels N is designed to be configurable from 2 to 4. However, for the sake of simplicity, N is fixed to 4 in the rest of the description in this section. The clock signal CK_{TX} of which frequency is twice the value of DR_{total} is applied to the select signal encoder circuit to generate N select signals, s_A, s_B, s_C, and s_D. The select signals have a frequency of $2 \times f_{notch}$ and a duty cycle of $\frac{1}{N}$, with 25% of phase-shifted between neighboring sub-channel select signals. While multiplexing the N sub-channels, $s_{A:D}$ operate as input clocks of the deserializing clock encoder circuit. The deserializing clocks exhibit half the frequency of the select signals, i.e., f_{notch}, and they deserialize the input data stream into N sub-channels. When one of the select signals is high, the data of the corresponding sub-channel passes through the MUX. The rising-edge of CK_D should be aligned to the rising-edge of s_D so that the pattern of the multiplexed data stream (D_{MUXed}) is A-B-C-D-A-B-C-D, as illustrated in Fig. 2.25. In order to insure this alignment,

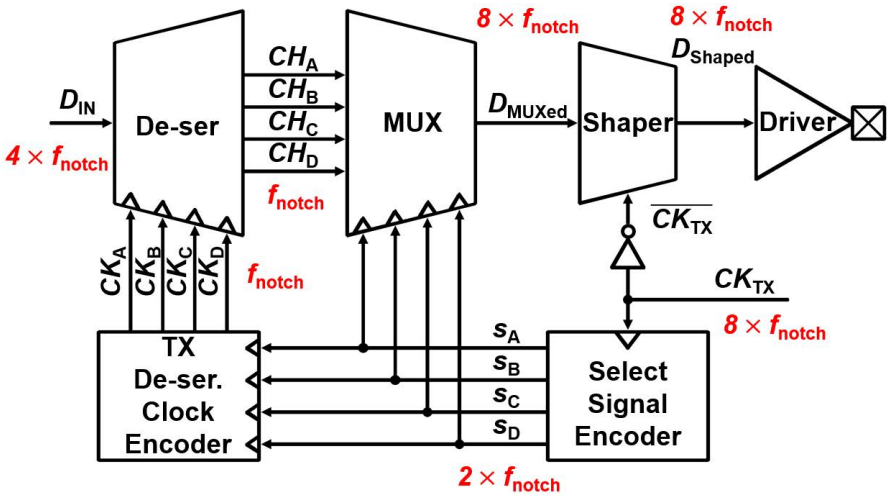


Figure 2.24 – TX block diagram for the proposed signaling scheme.

s_D and CK_D always have to be present when N changes, e.g., when $N = 3$, s_A is disabled; when $N = 2$, s_A and s_b are disabled. In order to avoid the risk from timing uncertainty, all the abovementioned signals and data are synchronized to CK_{TX}. Then, D_{MUXed} is further shaped by $\overline{CK_{TX}}$ for generating the A-0-B-0-C-0-D-0-A-0-B-0-C-0-D-0 pattern: when $\overline{CK_{TX}} = 1$, $D_{Shaped} = D_{MUXed}$ and when $\overline{CK_{TX}} = 0$, $D_{Shaped} = 0$. The inversed clock $\overline{CK_{TX}}$ is used instead of CK_{TX} to ensure that the one-level of the shaping signal ($\overline{CK_{TX}}$ in Fig. 2.25) is entirely inside a valid data window of D_{MUXed}.

RX Data-Path

The RX block diagram for the proposed signaling scheme is shown in Fig. 2.26. In order to reduce the design complexity of the comparator that is sensitive to offset, a limiting amplifier is employed for widening the vertical eye of the incoming data. Due to the characteristics of the proposed signaling scheme, only half of the received bits are valid, in other words, can have open eyes, as depicted in Fig. 2.27. Using a single comparator running at the rate of $8 \times f_{notch}$, half of the energy will be wasted due to the above-mentioned eye diagram characteristic. Therefore, one comparator per sub-channel is used, running at the rate of f_{notch}. This not only improves the comparator's power efficiency but also makes the design complexity more relaxed thanks to the lower operating speed. The sampling clocks for the comparators are generated by an RX deserializing clock encoder circuit, which can generate configurable sampling clocks for 2 to 4 sub-channel modes.

2.3.3 Simulation Results

By transmitting a time-division multiplexing (TDM)-based spectrum shaped data with 4×1.2 Gb/s streams over the reference MDB shown in Fig. 2.16, the eye diagrams shown in Fig. 2.28

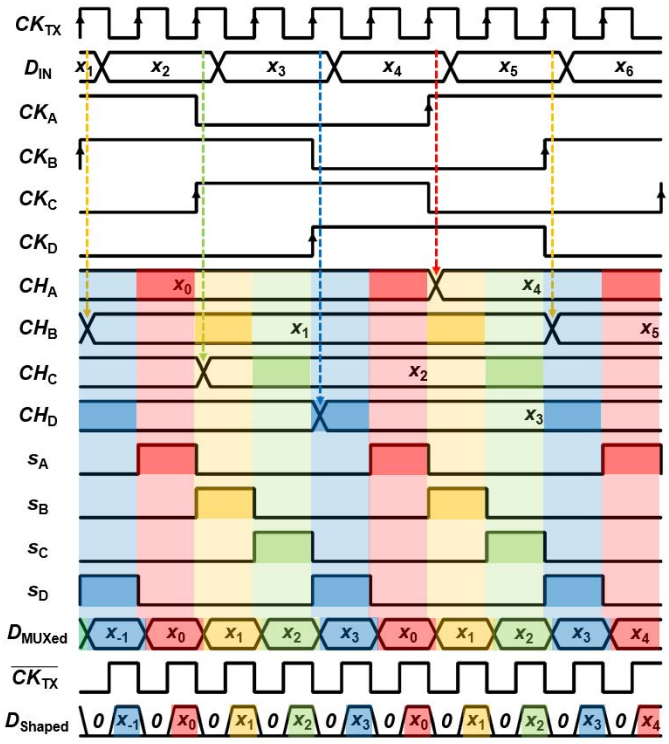


Figure 2.25 – Data flow at the TX internal nodes.

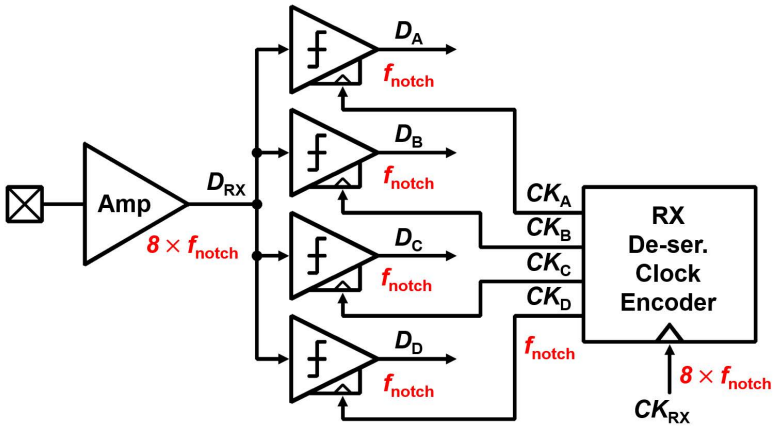


Figure 2.26 – RX block diagram for the proposed signaling scheme.

are obtained: (a) with 25% duty cycle of the multiplexing signals as proposed in [1], and (2) with 12.5% duty cycle for guard-interval insertion. The TX sequence generators' random jitter on each sub-channel is assumed to be 2 ps root-mean-square (rms) and sub-channel select signal's random jitter is assumed to be 2 ps as well. And 10 mV_{rms} random voltage noise is added on the TX output for addressing other noise sources such as power supply noise and thermal noise. Inter-channel skew is considered to be 1 ps, and 5 mV_{pp} RX sampler offset non-ideality is assumed. The higher the inter-channel skew is, the more the eye-shape imbalance

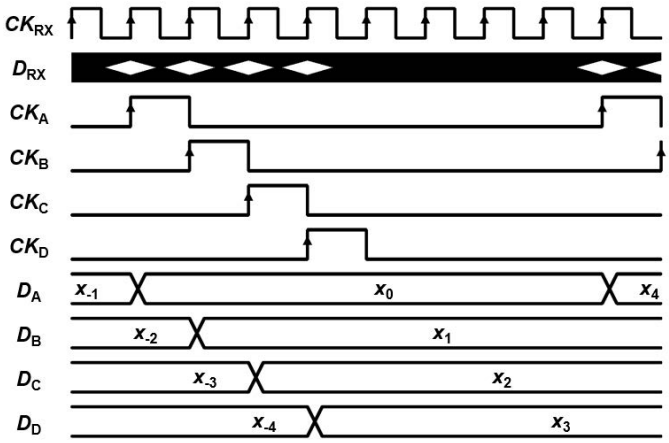
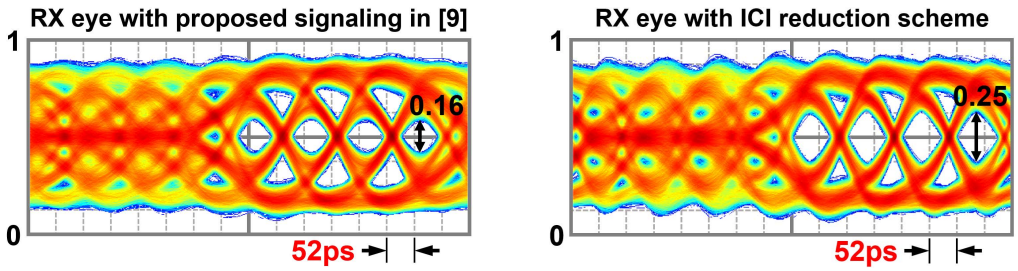


Figure 2.27 – Waveform of RX nodes.



(a) (b)

Figure 2.28 – Received eye diagrams of 4-channel 4.8Gb/s data stream with the system in [60] and (b) that with the proposed scheme.

among different sub-channels is due to imbalanced ICI, and the worse the worst-case eye closure is. Considering offset-calibrated RX comparators and the amplified received signal by RX front-end amplifier, comparator design is not of particular concern to the proposed system. The resulting normalized eye diagram with ICI reducing scheme exhibits more than 50% larger vertical opening while the horizontal opening is practically unchanged, at $DR_{\text{total}} = 4.8$ Gb/s. It is worth noting that the DR_{sub} can be configured by up to ±10%, ±15%, and ±20% from $DR_{\text{sub}} = f_{\text{notch}}$b/s, for $N = 4$, 3, and 2, respectively, with the cost of degraded eye opening. The fact that the tunable DR_{sub} range does not cover a continuous range to make the DR_{total} continuous from low-rate to high-rate, e.g., 1Gb/s - 5Gb/s, can be the main limitation of the proposed signaling scheme. By employing ICI reduction scheme as shown in this work, the RX will be more robust against far-end crosstalk having larger voltage margin. Without taking crosstalk into account, the horizontal eye opening at BER of 10^{-12} is 42 ps, which is equivalent to 40.4% UI. The TX and the RX power consumptions are estimated to be 3.2 mW (logic+driver) and 1.9mW (front-end amplifier+comparators+clock encoder), respectively. Table 3.2 compares this work with other relevant works.

Table 2.4 – Comparison with other relevant works.

Ref.	**[60]**	**[68]**	**[70]**	**[71]**	**This work**
Channel	12″ MDB	7.5″ MDB	4.7″ MDB	2″ P-to-P	**12″ MDB**
# of sub-bands	2	1	1	5	**4**
1^{st} notch frequency	2.5 GHz	NA	NA	NA	**1.2 GHz**
Drops	2	4	6	0	**2**
Experiment	sim.	meas.	meas.	meas.	**sim.**
DR (Gb/s)	5.0	3.4	5.8	4.0	**4.8**
Signaling	TDM	NRZ	Duo-binary	5-Band QPSK	**TDM with guard-interval**
I/O type	Single-ended	Single-ended	Diffe-rential	Diffe-rential	**Single-ended**
EQ	-	2-tap DFE	7-tap DFE	LPF	**-**
BER/eye opening	10^{-12} / 24 ps	10^{-12} / 60 ps	10^{-10} / 62 ps	NA / 1.8 ns	**10^{-12} / 42 ps**
Power (mW/Gb/s)	NA	0.89 (RX)	2.45 (RX)	1.35 (TRX)	–

2.4 Conclusion

A TRX employing digital spectrum shaping signaling for multi-drop interfaces has been proposed. By applying the spectrum shaping signaling scheme, a transmitter can transmit data minimizing the effect of multi-drop channel notches in the frequency domain, thereby resulting in reduced ISI and crosstalk-induced jitter thanks to the reduced reflections in the time domain. Given a fixed target data-rate, a spectrum shaping signaling TRX can transmit data that are coming from multiple sub-channels over a single-lane, customizing its per-sub-channel data-rate and number of sub-channels depending on the multi-drop channel characteristics. The proposed TRX without ICI reduction scheme has been examined through system-level modeling and measurement using discrete DAC, and the proposed TRX with ICI reduction scheme has been examined through system-level modeling, demonstrating the feasibility and advantages of the spectrum-shaping signaling over the NRZ signaling for two reference 12-inch FR-4 MDBs.

3 Single-Sideband Analog Multi-Tone Signaling

[1] This chapter presents the design and analysis of a serial link TRX architecture employing AMT signaling for chip-to-chip communication. Multi-tone SSB signaling scheme is proposed in TRX architecture in order to optimize bandwidth requirements for each sub-channel and to improve SNR by reducing ICI between neighboring sub-channels. System-level modeling results show that the proposed TRX architecture enables equalizer-free communication at 16 Gb/s over a lossy backplane channel that exhibits 22 dB attenuation at 8 GHz, while conventional NRZ signaling TRX necessitates a two-stage continuous-time linear equalizer CTLE. A channel frequency-response inversion scheme, the up/down-conversion mechanism of the TX/RX data stream and the RX design considerations have been analyzed and investigated by architectural modeling.

3.1 Single-Sideband RF

Since multiplying in time-domain is equivalent to convolving in frequency-domain, the upconverted double-sideband (DSB)-RF signal can be expressed in frequency-domain as

$$X(f) * CK(f) = \alpha A\left[\sum_{k=1}^{\infty} \frac{\sin(\alpha k\pi)}{k\pi/2}\left\{X(f-kf_{\mathrm{CK}}) + X(f+kf_{\mathrm{CK}})\right\}\right] \tag{3.1}$$

where $X(f)$ is Fourier transform of the baseband signal, $CK(f)$ is Fourier transform of the differential square-clock used for local oscillator (LO), α is the duty cycle of the clock, and f_{CK} is the LO clock frequency. As can be seen in (3.1), the upconversion of a baseband (BB) signal transforms the BB spectrum to two RF spectrums, centered at $\pm f_{\mathrm{CK}}$, ignoring the terms with $k > 1$. After the signal being upconverted, the resulting signals in each of positive and negative frequency ranges occupy twice the bandwidth than the BB signal occupied, since each of $X(f + kf_{\mathrm{CK}})$ and $X(f - kf_{\mathrm{CK}})$ contains both lower sideband (LSB) and upper sideband(USB).

[1] The contents of this chapter is based on: G. Kim, T. Barailler, C. Cao, K. Gharibdoust, and Y. Leblebici, "Design and modeling of serial data transceiver architecture by employing multi-tone single-sideband signaling scheme,", *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 12, pp. 3192–3201, Aug. 2017 (©IEEE) [72].

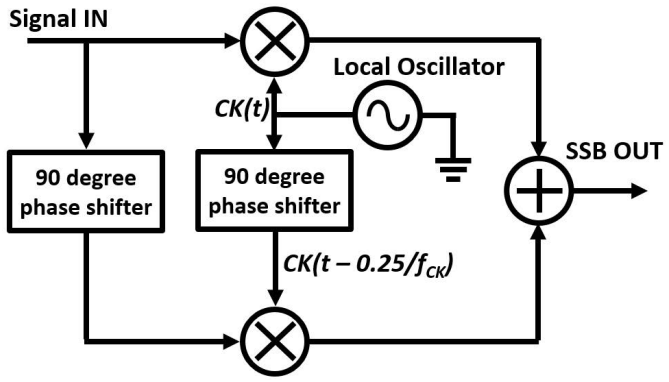


Figure 3.1 – Block diagram of a phase-discrimination circuit.

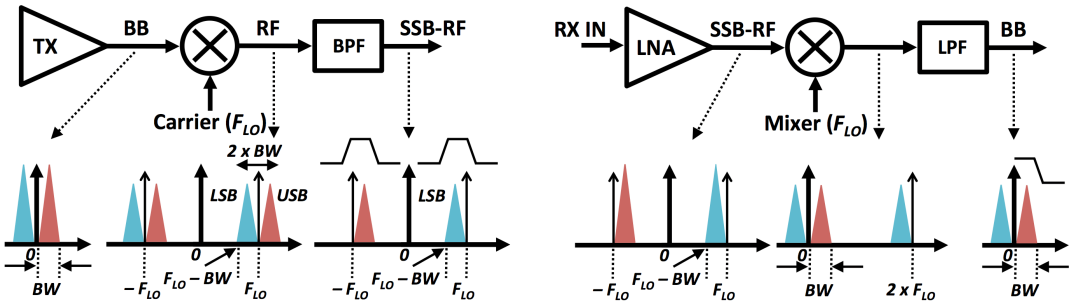


Figure 3.2 – A basic SSB TX (a) and RX (b) architecture with analog filter and corresponding power spectrums of signal.

Generally, when a signal is upconverted by amplitude-shift keying (ASK) modulation, the spectrum of the resulting RF signal occupies twice the frequency bandwidth as compared to its original baseband signal. Since both of LSB and USB contain the same information, only one sideband is needed in order to restore the original BB signal on the RX side.

The elimination of one sideband to generate an SSB-RF signal from a DSB-RF signal can be done either by using phase-discrimination method (PDM) or by using an analog sideband suppression filter. Shown its block diagram in Fig. 3.1, the phase discrimination circuit delays the modulating signal by 90 degree, upconverts the signal and its delayed version by $CK(t)$ and $CK(t-\frac{1}{4f_{CK}})$ respectively, then sums up the mixed signals. The mixing of the modulating signal with the carriers are performed by balanced mixers. However, considering the design complexity of integrating balanced mixers, phase shifters, and analog summer for each sub-channel, the PDM is not suitable for multi-carrier wireline TRXs.

Fig.3.2(a) illustrates a TX architecture for one sideband suppression using an analog filter, and power spectrums at the corresponding sub-block nodes. The suppression of one sideband can be realized by using a bandpass filter (BPF) having its passband (PB) either on the LSB or USB (LSB in Fig. 3.2(a)). The RX demodulates the incoming SSB-RF signal with a downconverting

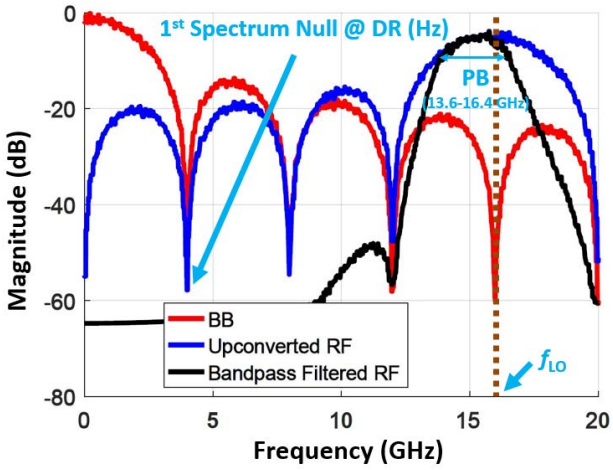


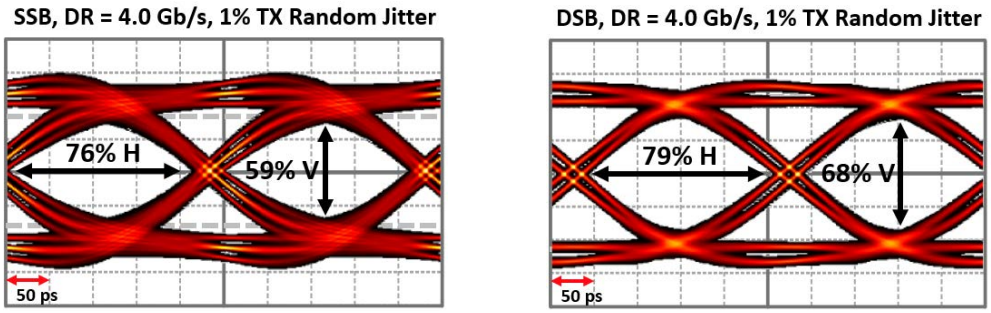
Figure 3.3 – Power spectrums of the 4 Gb/s data stream along the transmitter building blocks.

mixer, then applies a low-pass filter retaining only the BB spectrum, as illustrated in Fig. 3.2(b).

In wireline TRX systems, although it is not possible to completely remove one sideband of DSB-RF signal without the presence of an ideal filter due to the spectral property of the BB NRZ signal, one sideband can be properly attenuated so that the resulting signal practically become an SSB signal. Fig. 3.3 shows spectrums of BB, upconverted RF, and bandpass filtered RF signals. For USB suppression shown in Fig. 3.3, a 3rd order Butterworth bandpass filter has been chosen, and its passband is from 13.6 GHz to 16.4 GHz, while the bandwidth of the upconverted RF signal is 12 GHz - 20 GHz. Conserving frequency components from 14 GHz to 16 GHz is enough for original signal reconstruction since the frequency components from DC to f_{NYQ} of the original BB signal are located between 14 GHz to 18 GHz where the information stored in 14 GHz - 16 GHz (LSB) and 16 GHz - 18 GHz (USB) are identical. It can be observed that the USB of the DSB-RF spectrum can be considerably attenuated by a bandpass filter of which PB is over the useful frequency range of the LSB, i.e., 14 GHz - 16 GHz $\mp$ 0.4 GHz of margin, resulting in the RF spectrum practically SSB. Fig. 3.4(a) shows that the eye diagram of the received signal after demodulation is open even though one sideband is absent. Note that the channel is not included in this simulation since this simulation has been designed to observe the effects of the absence of a sideband. The asymmetrically remaining USB after USB rejection deteriorates the signal integrity of the received signal (Fig. 3.4(a)) by 3% of timing margin and 9% of voltage margin as compared to the eye quality without any sideband rejection (Fig. 3.4(b)), but the level of deterioration due to one sideband rejection is not significant.

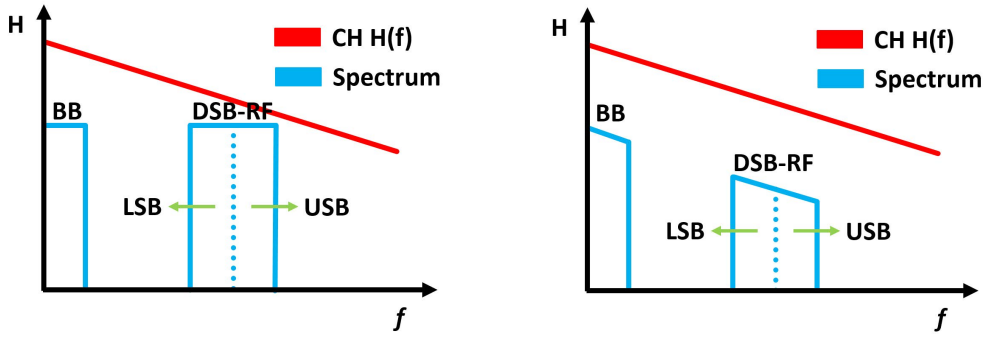
3.2 Single-Sideband Selection

As LSB and USB contain the same information, rejecting either LSB or USB should results in the similar eye shape, assuming that there are no other noise sources. However, when the



(a) (b)

Figure 3.4 – Eye diagrams on the RX output after demodulation, for the (a) SSB and the (b) DSB signals.



(a) (b)

Figure 3.5 – Spectrum illustrations of BB and DSB-RF signals (a) before channel attenuation and (b) after channel attenuation.

channel is considered, rejecting either LSB or USB starts to matter. As illustrated in Fig. 3.5(b), USB experiences more attenuation than LSB. For example, if an NRZ stream is upconverted and transmitted through a channel, then the USB frequency components corresponding to the Nyquist frequency of the BB NRZ signal (f_{Nyq}) will experience more attenuation than that of LSB. Fig. 3.6 shows how the resulting BB spectrum will look like after RX downconversion. Note that only the main spectrums are shown in Fig. 3.6, ignoring the images for the sake of simplicity. Fig. 3.6(a) and Fig. 3.6(b) show that the remaining power of LSB after sideband rejection is bigger than that of USB, which means that the interference caused by one sub-band to its neighboring sub-band is more significant in the case of Fig. 3.6(b) than in Fig. 3.6(a). In Fig. 3.6(c), it can be seen that the high-frequency components of the original BB signal are amplified relatively to its low-frequency components, with some overall signal level attenuation over the whole bandwidth span. The gain coming from the relative high-frequency amplification is as much as the channel attenuation (in absolute value) at the corresponding frequencies, which can be seen as *channel inversion*. Therefore, the spectrum of the BB signal in Fig. 3.6(c) can easily be shaped to match the transmitted signal's spectrum by passing

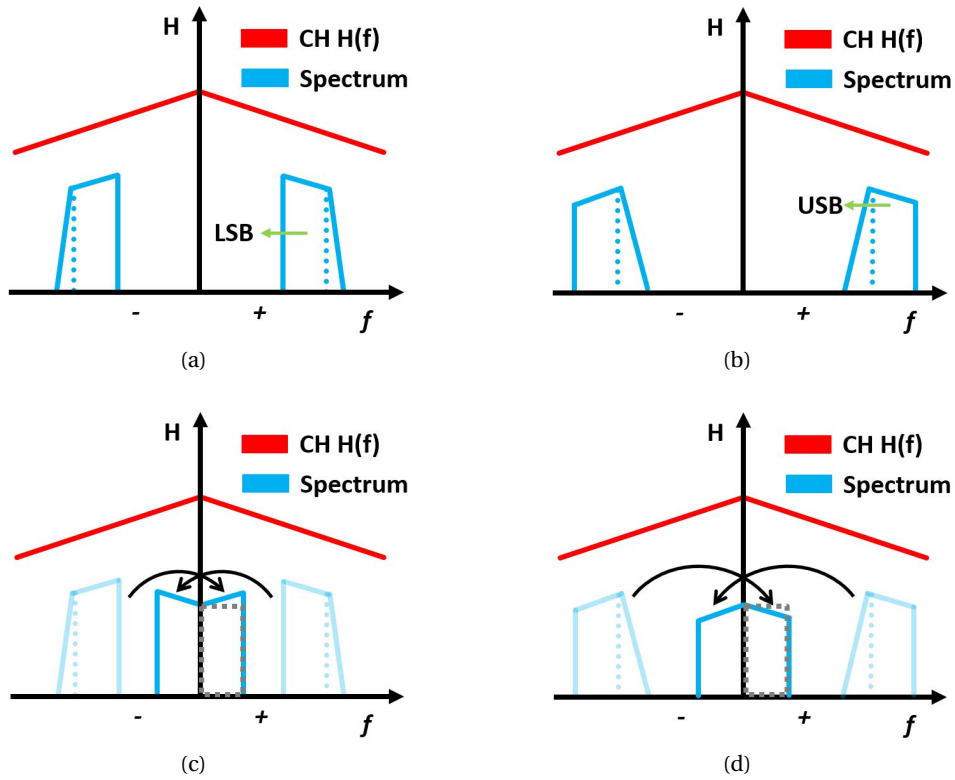


Figure 3.6 – Spectrum of signals (a), (b) before downconversion, and (c), (d) after downconversion. (a), (c) are for LSB-RF downconversion and (b), (d) are for USB-RF downconversion.

it through a low-pass filter (LPF) stage (chopping stage), targetting the recovered signal to be close to the dotted-gray rectangle, which has the shape of the transmitted spectrum. On the other hand, the BB spectrum in Fig. 3.6(d) needs high-frequency amplification which is typically done by a CTLE. Thus, keeping the LSB for data transmission, CTLE peaking and bandwidth specifications can be simplified and be replaced by an LPF. This leads to a reasonable die area and power consumption imprisonment.

As an illustration, a SSB-RF TRX with 4 Gb/s data-rate and $f_{LO} = 8$ GHz is modeled and the related frequency spectrum is shown in Fig. 3.7. Fig. 3.7(a) shows the spectrums of transmitted and received signals when the USB is suppressed, and Fig. 3.7(b) when the LSB is suppressed, where yellow lines represent the channel insertion loss, blue lines are the original BB 4 Gb/s NRZ signals' spectrum, red lines are the spectrums of the transmitted SSB-RF signals, green lines are the received (attenuated) SSB-RF signals' spectrums, and black lines are the spectrum of the downconverted BB signal. Note that the black line in Fig. 3.7(a) shows the spectrum of a downconverted-low-pass filtered signal with LPF cutoff frequency around 2.4 GHz, and that in Fig. 3.7(b) shows the spectrum of a downconverted signal with LPF cutoff frequency around 4 GHz only for image rejection purpose. Fig. 3.7(c) and Fig. 3.7(d) show the eye diagrams of the recovered BB signals corresponding to the Fig. 3.7(a) and Fig. 3.7(b), respectively. The eye

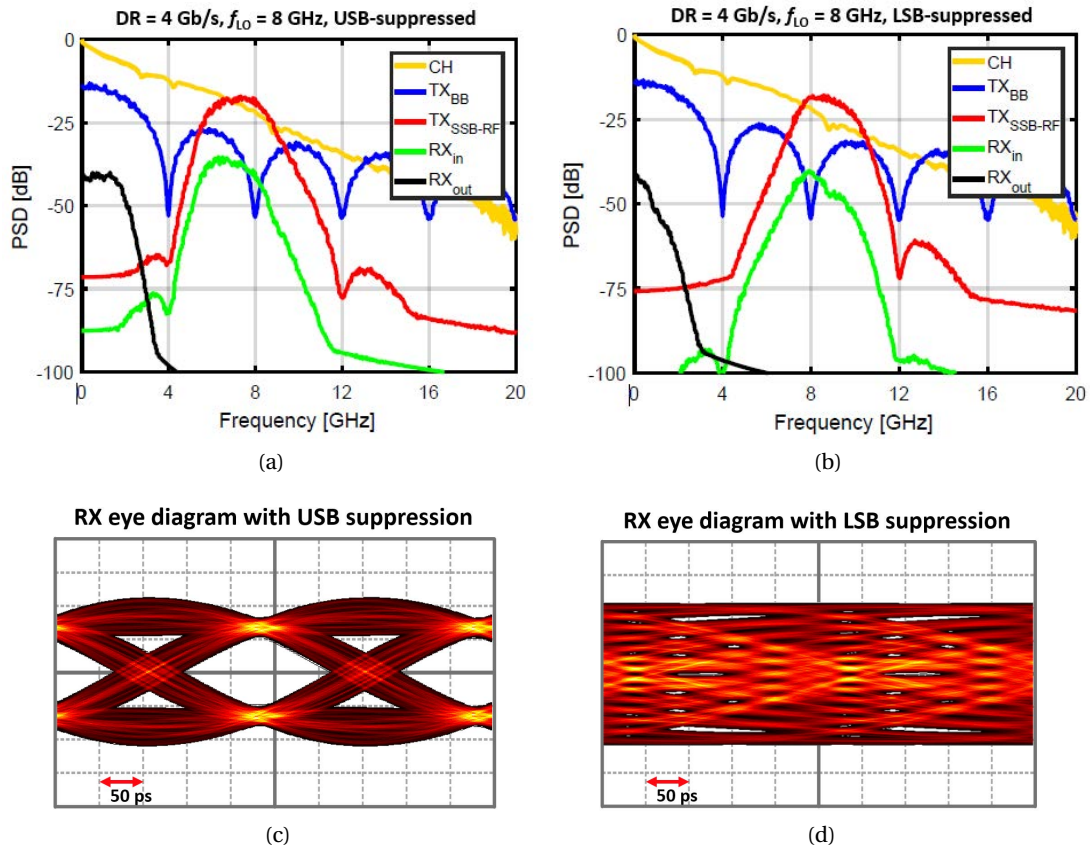


Figure 3.7 – SSB-RF spectrums with (a) USB-suppressed, (b) LSB-suppressed, and (c), (d) the eye diagrams of their demodulated signals, respectively.

diagram shown in Fig. 3.7(c) is clearly open while that shown in Fig. 3.7(d) is closed due to the significant attenuation near f_{Nyq}, as explained in previous paragraph.

3.3 Proposed TRX Architecture

The TX and RX proposed in this paper communicate by transmitting/receiving multiple closely-spaced sub-channels. In AMT serial link systems, it is important to limit the number of sub-channels in order not to burn too much power in clock generators/networks. Nevertheless, in this Section, the number of sub-channels is expressed with a letter N for generalization purpose.

3.3.1 Transmitter

The proposed TX architecture is shown in Fig. 3.8. It is composed of N sub-TXs, where each of them consists of an NRZ data source, a low-pass prefilter, an upconverting mixer, and a

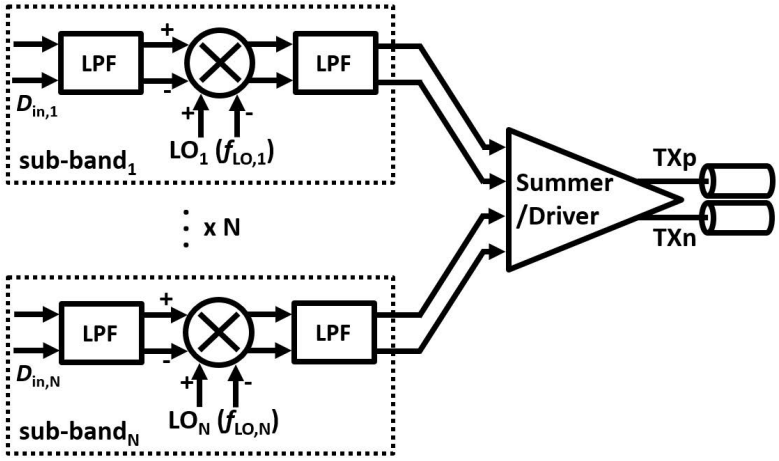


Figure 3.8 – AMT/SSB TX architecture.

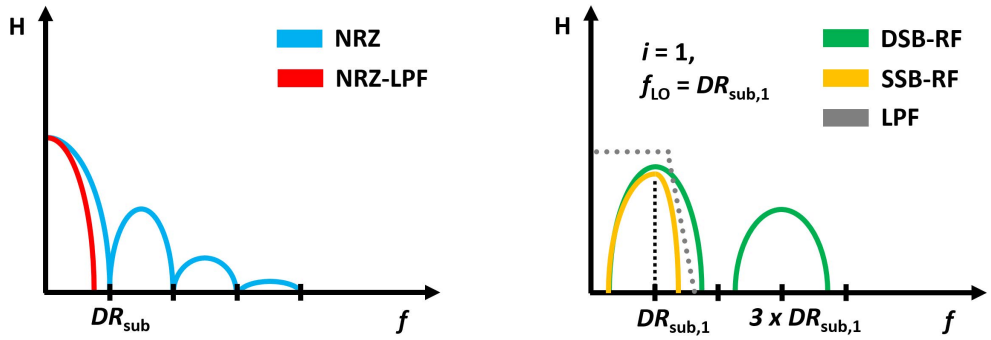


Figure 3.9 – Illustration of spectrums of signals along TX data-path: (a) BB NRZ and its low-pass filtered signal are shown in blue and red lines respectively, (b) the upconverted signal, SSB-RF signal after low-pass postfilter, and the low-pass filter frequency characteristics are shown in green, yellow and gray lines, respectively.

low-pass postfilter. The NRZ data source has N times lower data-rate as compared to the total data-rate, thus $DR_{\text{sub}} = DR_{\text{total}}/N$. Each NRZ stream is low-pass filtered before being upconverted, for the purpose of side-lobe suppression for minimizing ICI. The i^{th} low-pass-filtered NRZ stream is upconverted by a mixer which has a LO operating at $i \times DR_{\text{sub}}$ Hz, where i is $1, 2, \cdots, N$. The upconverted signal is then again low-pass filtered, for USB suppression. For the sideband suppression LPFs, different cutoff frequencies are required for different sub-bands, with step frequency of DR_{sub} Hz from $i = 1$ to $i = N$. Then an analog summer will merge all sub-bands forming an AMT/SSB signal, and the AMT/SSB signal is driven toward the channel.

As can be seen in Fig. 3.9(a), the low-pass prefilter suppresses side-lobes of the original NRZ spectrum (blue line), making the bandwidth occupancy of the output signal lower than the original one (red line) by placing the LPF cutoff frequency slightly above the f_{Nyq}. The images

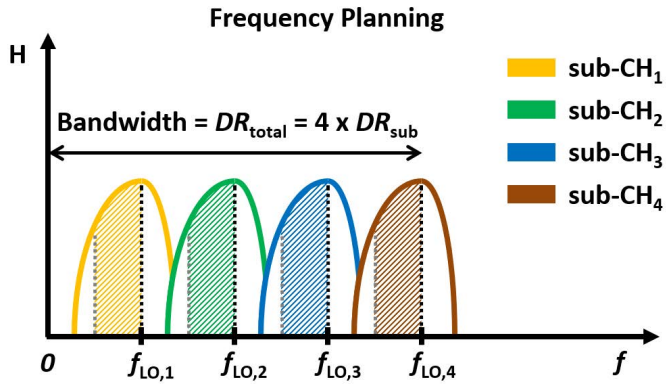


Figure 3.10 – Frequency planning with four sub-channels.

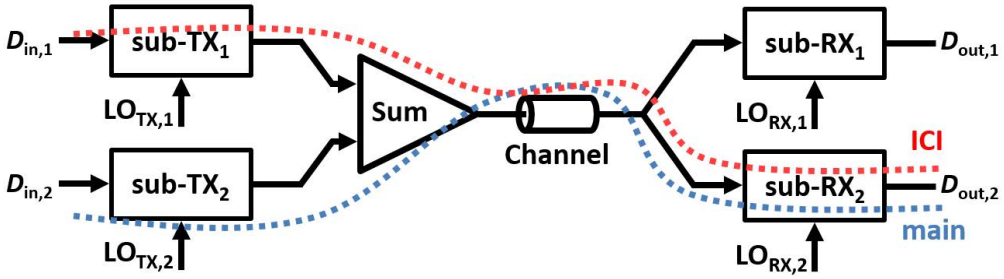


Figure 3.11 – ICI mechanism of sub-channel 1 to sub-channel 2.

of DSB-RF signal created by the LO harmonics (green line) in Fig. 3.9(b) are suppressed together with the USB by a low-pass postfilter (dotted gray line), resulting in the RF signal SSB (yellow line). The spectrum shown in Fig. 3.9(b) is for the sub-channel $i = 1^{st}$, where $f_{LO,1} = 1 \times DR_{sub}$ Hz. For other sub-channels, the SSB-RF spectrums will be located at corresponding $f_{LO,i} = i \times DR_{sub}$ Hz, thereby filling a total of DR_{total} Hz of bandwidth for the merged AMT/SSB signal.

Fig. 3.10 illustrates the frequency planning of the proposed TX with 4 sub-channels, where $f_i = i \times DR_{sub}, i \in \{1,2,3,4\}$, the dotted gray lines indicate the f_{Nyq} of the sub-channel NRZ data stream, the dotted black lines indicate the upconverting mixers' LO frequency for each sub-channel. The shaded area inside each spectrum envelope is the spectral contents that need to be received properly at the RX front-end. Assuming that the LSB power is dominating over the quasi-rejected USB for each sub-channel spectrum, the interference of USB of a particular sub-channel to the LSB of its neighboring sub-channel is limited. An example of such interference, ICI, of sub-channel 1 to sub-channel 2 is shown in Fig. 3.11. Therefore, the sub-channels can be rather orthogonal to each other, enabling correct recovery of original sub-streams on the RX.

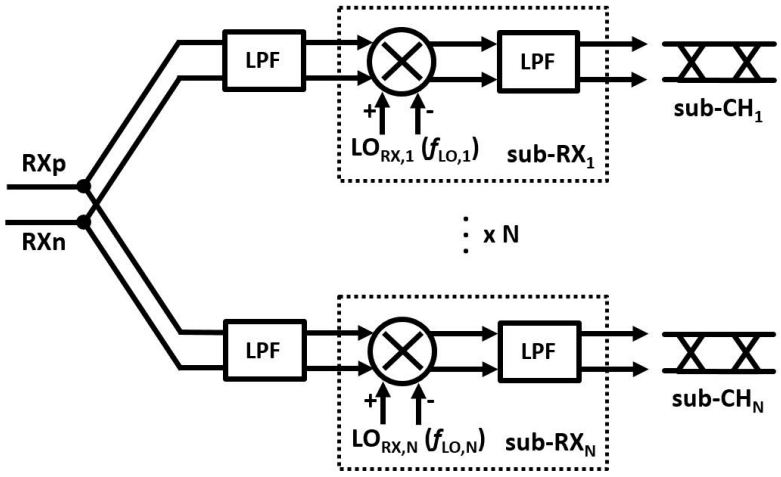


Figure 3.12 – AMT/SSB RX architecture.

3.3.2 Receiver

The proposed RX architecture, shown in Fig. 3.12 contains N sub-RXs, where each sub-RX being responsible for demodulation of one sub-channel. Each sub-RX consists of a low-pass prefilter, a downconverting mixer, and a low-pass postfilter. The sub-RXs separate their corresponding sub-channel from the received multi-tone signal by proper filtering and downconversion, where the requirement of the prefilter and its specifications vary depending on the channel characteristics. Some non-trivial design considerations have to be taken into account due to the SSB property of the received signal and the effect of the channel attenuation that is uniformly increasing (in dB) over the frequency span. Detailed explanations with the support of figures are given in the following paragraphs.

An example downconversion case with $N = 4$ and $i = 2$ is depicted in Fig. 3.13, without taking the low-pass prefilter into account. The upper plot depicts the BB spectrum reconstruction mechanism by a downconverting mixer, where $f_{\mathrm{LO,i}} = i \times DR_{\mathrm{sub}}$, $i \in \{1,2,3,4\}$, and highlighting downconversion of sub-band $i = 2$. If the channel insertion loss is negligible, e.g., ultra-short-reach/short-reach channel cases, the received spectrum of all sub-bands have similar power assuming that same power is allocated for all sub-bands in TX. Since each sub-band spectrum has USB-suppressed SSB characteristics, the frequency bands $-f_{\mathrm{LO},2} \leq f < -f_{\mathrm{LO},1}$, $f_{\mathrm{LO},2} \leq f < f_{\mathrm{LO},3}$ contain spectral contents as highlighted by red rectangles. Note that correct demodulation for $i = 2$ requires a well-preserved green shaded area at BB with limited interferences from other sub-band spectrums. After downconversion, the spectrum in $-f_{\mathrm{LO},2} \leq f < -f_{\mathrm{LO},1}$ will be moved to $-f_{\mathrm{LO},4} \leq f < -f_{\mathrm{LO},3}$ and $0 \leq f < f_{\mathrm{LO},1}$, with reduced power. Similarly, the spectrum in $f_{\mathrm{LO},2} \leq f < f_{\mathrm{LO},3}$ will be moved to $0 \leq f < f_{\mathrm{LO},1}$ and $f_{\mathrm{LO},4} \leq f < f_{\mathrm{LO},1} + f_{\mathrm{LO},4}$. The band-of-interest after downconversion is the band $0 \leq f < f_{\mathrm{LO},1}$, which is highlighted by a dotted red circle.

The bottom inset of Fig. 3.13 depicts how the BB spectrum (dotted red circle) will look like,

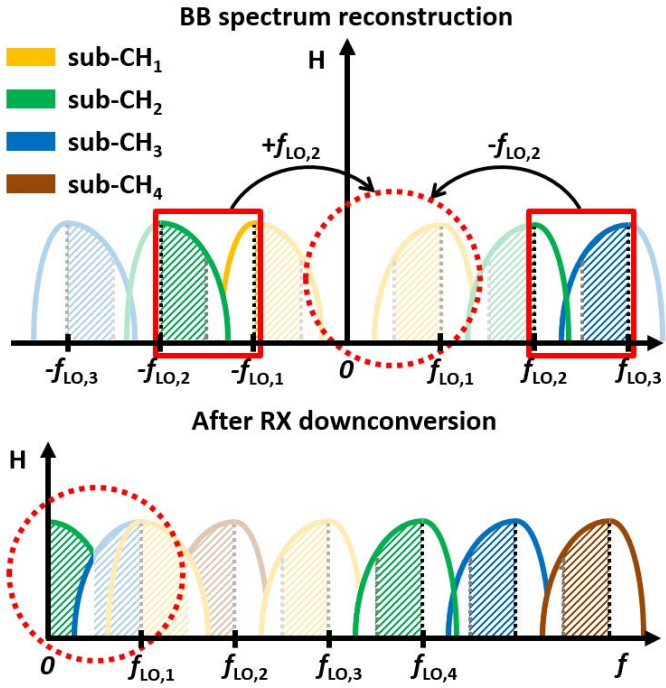


Figure 3.13 – BB spectrum reconstruction mechanism when downconverted, for sub-channel $i = 2$.

which is a superposition of the two red rectangles of the upper plot. It can be observed that the spectral component at f_{Nyq} of the $i = 2$ NRZ sub-stream (victim) is interfered by the LSB of sub-channel $i = 3$ (aggressor) with equal power, resulting in the correct demodulation impossible. Generally speaking, the aggressor of i^{th} sub-channel is the LSB of $(i+1)^{\text{th}}$ sub-channel, the BB spectrum-of-interest comes from the negative frequency, and the aggressor comes from the positive frequency.

Noting that the low-pass postfilter is required to suppress the high-frequency images created by downconversion, two sub-cases can be considered to analyze the necessity of the low-pass prefilter: RX for 1) low-attenuative channel (ultra-short-reach, short reach), and 2) lossy channel (long-reach).

RX for Low-Attenuative Channel

The extreme case of a low-attenuative channel is the example shown in Fig. 3.13, where the SNR at f_{Nyq} of the NRZ sub-stream being 0 dB. In such cases, a low-pass prefilter is necessary in order to cut the aggressor spectrum off, by placing the pole of the filter around f_{LO} for sub-channel to be downconverted. Fig. 3.14 depicts the BB spectrum reconstruction mechanism taking the low-pass prefilter into account. As depicted in the upper inset, the 3$^{\text{rd}}$ sub-channel spectrum is filtered-out. This provides larger SNR at f_{Nyq} for downconverted 2$^{\text{nd}}$ sub-channel as depicted in the bottom-right inset, as compared to the downconversion

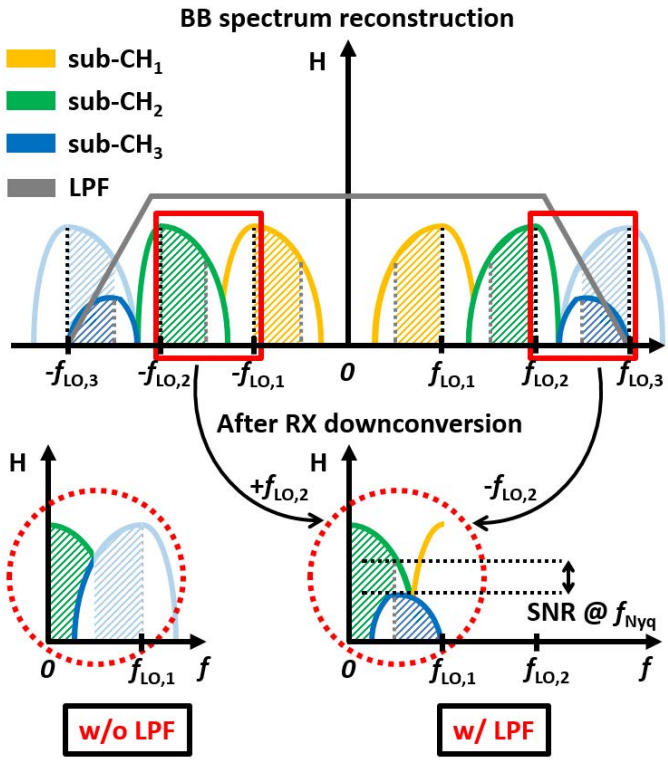


Figure 3.14 – Effect of low-pass prefilter on downconversion, for sub-channel $i = 2$.

case without low-pass prefilter shown in the bottom-left inset. Thus, a low-pass prefilter is must-have in AMT/SSB RX when the channel attenuation is low to prevent aggressor sub-band deteriorating the victim sub-band SNR. To do so, the PB of the i^{th} low-pass prefilter has to cover up to $f_{\text{LO,i}}$ in order to preserve i^{th} sub-channel spectrum and to properly suppress $(i+1)^{\text{th}}$ sub-channel spectrum. The following RX postfilter attenuates $f > f_{\text{Nyq}}$ components for BB recovery. The orders of the RX pre/postfilters depend on the channel profile. For the RX prefilter, the higher the channel attenuation is, the less the RX prefilter's order can be, as the channel's low-pass filter nature contributes filtering out the sub-channel aggressors located at higher frequencies. On the contrary, the higher the channel attenuation is, the higher the RX postfilter's order should be, as the absolute attenuation level difference between the less attenuated sub-channel and the most attenuated sub-channel becomes larger when the channel is lossy. And that absolute attenuation level difference determines the minimum order of the RX low-pass postfilter that is required to open the eye diagram of the demodulated signal. The influence of the channel profile to the minimum RX pre/post filters' order for the resulting eye opening is shown in Section IV.

RX for Highly-Attenuative Channel

The downconversion and BB spectrum reconstruction mechanism when channel insertion loss is high is depicted in Fig. 3.15. The aggressor sub-band experiences higher attenuation

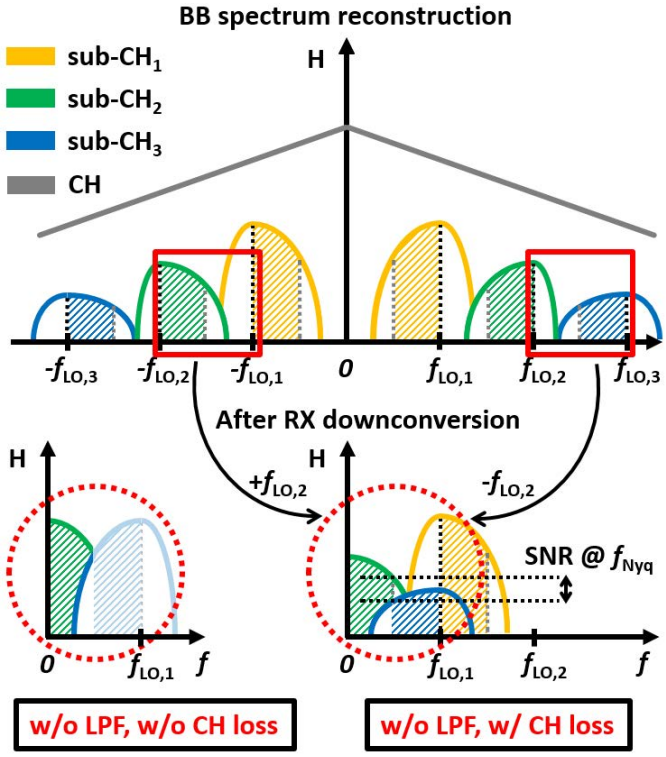
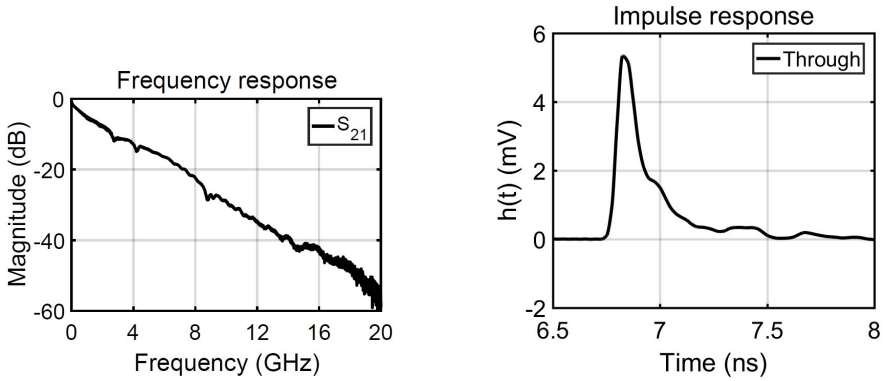


Figure 3.15 – Effect of channel insertion loss on downconversion, for sub-channel $i = 2$.

than the victim sub-band does, therefore SNR improves. However, the i^{th} sub-channel spectrum to be downconverted (the victim channel, e.g., $i = 2$) experiences more attenuation than the sub-channels with lower i indices (e.g., $i = 1$), thus it requires steeper low-pass postfilter in order to properly suppress $f > f_{\text{Nyq}}$ frequency bands after downconversion. The larger the channel attenuation is, the less the necessity of the existence of the low-pass prefilter is, but the steeper the low-pass postfilter should be. In addition, after being downconverted, the frequency components around f_{Nyq} are less attenuated as compared to the BB frequency components as depicted in Fig. 3.6(c), another 1^{st}-2^{nd} order low-pass filter stage (chopping filter) may be required to restore the downconverted BB spectral shape to be close to the original NRZ sub-stream spectral shape. However, this additional chopping filter stage is not essential as long as the high-frequency boosting effect due to the channel frequency-response inversion is not considerable. It is worth noting that the demodulated signal quality mostly depends on the RX prefilter under the condition that the RX postfilter is steep enough to properly suppress the $f > f_{\text{Nyq}}$ components. However, the higher the channel attenuation is, and the higher the sub-channel index is (e.g., $i = 4$ out of four sub-channels), the higher the impact of RX postfilter specification on the demodulated signal's quality is.



(a) (b)

Figure 3.16 – Measured channel profiles. (a) Through frequency response and (b) impulse response.

3.3.3 Design Considerations and Main Limitations

The TX driver should exhibit enough bandwidth since the bandwidth should support the DR_{total}, and its linearity specification has to be carefully met since AMT system with N consecutive sub-bands can have 2^N signal amplitude levels. The attenuation due to channel insertion loss at $f_{\text{LO,N}}$ can be significant if the channel is lossy, e.g., 30 dB loss at 10 GHz, such as in backplane links. This can be compensated for by proper power allocation for each tone on the TX side with the cost of additional linearity of the driver, otherwise, the total data-rate should be limited. In addition to this, unlike discrete multi-tone system such as OFDM, in AMT system the more the number of sub-channels is, the larger the number of required clock signals is, as local oscillators with $f_{\text{LO,i}} = i \times DR_{\text{sub}}$ are required on both TX and RX sides.

In wireline TRX, power consumption in clocking units can take nearly 20% or even higher over the entire TRX system power budget [56, 32]. Considering the difficulty of generating clocks for each local oscillator, where their frequencies are multiplied or divided by 3, 5, 7, $\cdots$ from a reference clock for $N \geq 8$ at multi-gigahertz or tens of gigahertz, it can be concluded to be impractical to consider more than four sub-channels.

Thus, the DR_{total} of the proposed TRX is mainly limited by the bandwidth and the linearity of the TX driver, the channel loss at the highest local oscillator frequency, i.e., $f_{\text{LO,N}}$, and the number of sub-channels due to clocking overhead.

3.4 Simulation Results

This Section provides simulation results for AMT/SSB TRX on the overall achievable data-rate and timing margin of demodulated signals for a measured channel, which exhibits 22 dB attenuation at 8 GHz (reference channel) of which frequency response and impulse response are shown in Fig. 3.16(a) and in Fig. 3.16(b), respectively. The number of sub-channels is fixed

Table 3.1 – Lowpass filters' specifications.

LPF	**TX prefilter$_i$**	**TX postfilter$_i$**	**RX postfilter$_i$**
Type	Butterworth	Butterworth	Butterworth
Order	2	3	1, 2, 3, 4
f_{cutoff}	$0.6 \times DR_{\text{sub}}$	$(0.1+\text{i}) \times DR_{\text{sub}}$	$0.7 \times DR_{\text{sub}}$

to four where each sub-channel data-rate is 4 Gb/s, resulting in 16 Gb/s aggregate data-rate. The measured S-parameters are used as channel models. The TX transmits USB-suppressed AMT/SSB signal. The RX prefilter has different configurations for different channels, and four different RX postfilter orders (1, 2, 3, 4) are considered to leverage the impact of RX postfilter's order, while other LPFs have fixed specifications for all channel models as listed in Table 3.1, where $\text{i} \in \{1,2,3,4\}$. The Rj of TX NRZ generators is assumed to be 4 ps, the TX/RX clock Rj are estimated to be 2 ps regardless of sub-band index, and the bandwidth of TX driver is estimated to be 17 GHz. The number of received bits that are overlapped for constructing one eye diagram is 10^4. The reported vertical/horizontal sampling margins of demodulated signals are at BER of 10^{-9} that is calculated based on the extrapolated histogram.

3.4.1 With High-order RX Lowpass Postfilter (4^{th} order)

Given that a high-order low-pass postfilter is present, the demodulated signal's quality mainly depends on the RX prefilter order. Fig. 3.17(a)-(d) show the demodulated eye diagrams when the channel between TX and RX is lossless, for RX low-pass prefilter order from 0 (no filter) to 3, respectively. Note that the eye height is normalized for the sake of easy comparison of the eye shapes. In Fig. 3.17(a), it can be observed that the eye is closed due to the fact that the interferer could not be filtered out because of the absence of the RX low-pass prefilter, as depicted in the bottom-left inset of Fig. 3.14. In Fig. 3.17(b), the eye starts to open with the help of 1^{st} order RX low-pass prefilter as depicted in the bottom-right inset in Fig. 3.14, while it is still deficient to eliminate the interferer properly. Fig. 3.17(c)-(d) show roughly the same eye diagrams where their horizontal and vertical margins are much wider than those in Fig. 3.17(a)-(b), meaning that filter order of ≥ 2 is enough for proper interferer rejection for this system configuration. On the other hand, the eye diagrams of 4^{th} sub-channel shown in Fig. 3.18(a)-(d) exhibit widely open eyes regardless of the order of the RX low-pass prefilter, due to the fact that there is no interferer at the higher-frequency side of 4^{th} sub-channel spectrum. Fig. 3.19(a)-(d) show the eye diagrams of the demodulated four sub-channels' signals for the communication through a reference channel without the presence of the RX prefilter. Fig. 3.20(a) and Fig. 3.20(b) show the horizontal and vertical sampling margins of the demodulated sub-channels' signals versus RX prefilter order, respectively, for the same transmission medium. It can be seen that for high-loss channels such as backplane links, the

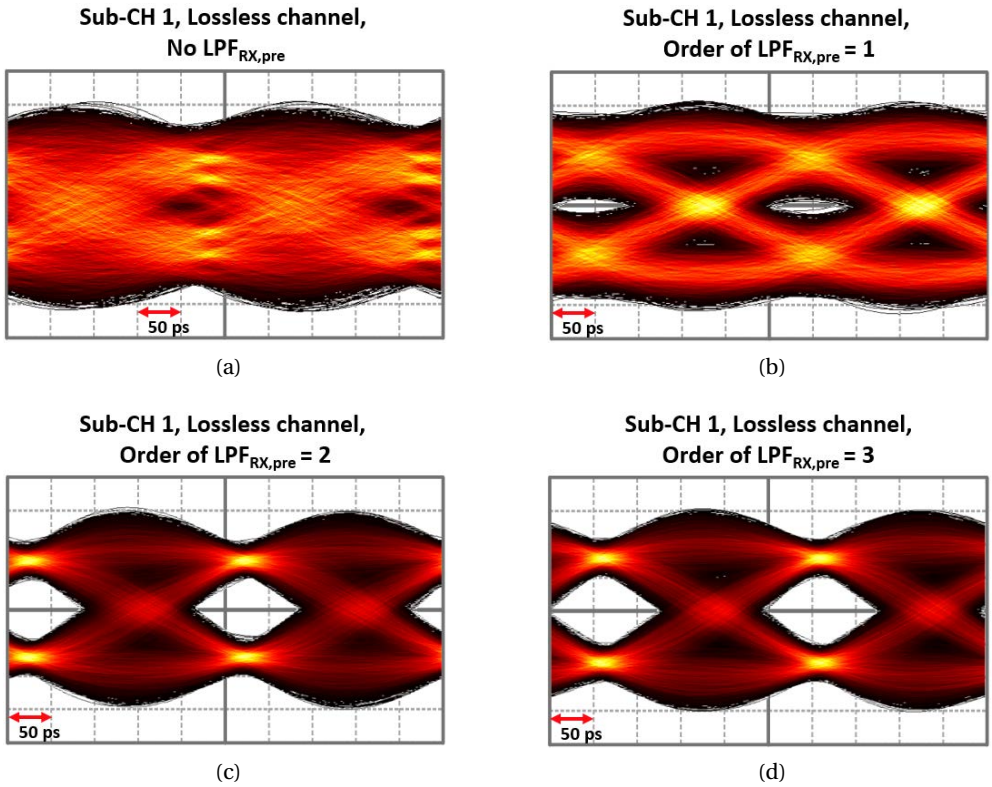


Figure 3.17 – Eye diagrams for demodulated sub-channel 1 when the transmission medium is lossless, with the order of RX low-pass prefilter is (a) 0 (no filter), (b) 1, (c) 2, and (d) 3.

demodulated signal integrity practically does not depend on the RX prefilter order and even its existence is not essential, as discussed in Section III.

3.4.2 With Low-order RX Lowpass Postfilter (2nd order)

In order to leverage the importance of the RX postfilter steepness for highly-attenuative channels, a set of simulations with four different RX postfilter orders have been performed. It is worth noting that the higher the sub-channel index is, the larger the power gap between the i^{th} sub-channel and the 1st sub-channel is, due to a large absolute attenuation level difference between these two frequency bands. As shown in Fig. 3.19, all sub-channels' eyes are open with enough SNR margin when the RX postfilter order is 4, since its capability to reject $f > f_{\text{Nyq}}$ components is high enough. However when RX postfilter is a 3rd order low-pass filter, the 4th sub-channel eye is closed, and the 3rd sub-channel eye is barely open while the 1st and 2nd sub-channels show widely open eye diagrams. For RX postfilter order 2, only 1st sub-channel eye is open, and for the 1st order LPF, all the sub-channels show closed eyes. A summary of horizontal/vertical eye opening versus RX postfilter order is shown in Fig. 3.21, showing that at least 4th order LPF is essential for the last filter stage for opening all sub-channels' eyes.

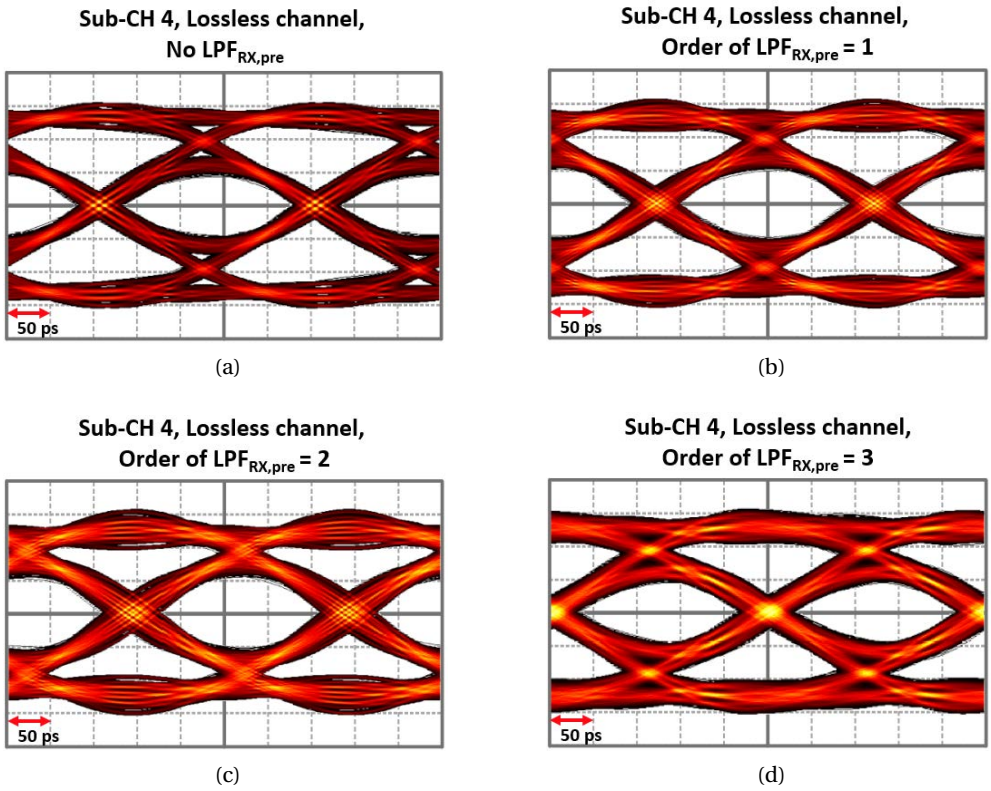


Figure 3.18 – Eye diagrams for demodulated sub-channel 4 when the transmission medium is lossless, with the order of RX low-pass prefilter is (a) 0 (no filter), (b) 1, (c) 2, and (d) 3.

While a total of 16 Gb/s-rate data can be transmitted and received with the proposed AMT/SSB TRX by upconversion/downconversion and proper low-pass filtering, an NRZ TRX necessitates a CTLE to make the pulse response of the channel short to minimize post-cursor ISI. If the pulse response is not shortened enough, DFE should follow CTLE to cancel the remaining post-cursors, which is not the case in this work. Fig. 3.22(a) shows the equalized eye diagram of a 16 Gb/s NRZ stream with a two-stage CTLE for providing about 16 dB peaking at the Nyquist frequency, and Fig. 3.22(b) shows the closed eye diagram of an 8 Gb/s NRZ stream when the CTLE is absent. The channel used for NRZ simulation is the same as what used for AMT/SSB TRX. It can be seen that a power hungry two-stage CTLE is essential to open the 16 Gb/s NRZ eye in conventional wireline TRX architecture; otherwise, the eye will be completely closed since it is already closed at 8 Gb/s data-rate as shown in Fig. 3.22(b). Table 3.2 compares this work with some relevant works.

3.5 Supplementary Experimental Results

To prove the conceptual feasibility, experiment with the setup shown Fig. 3.23 is performed. In order to have high attenuation level below sufficiently low frequency, e.g., 4 GHz, multiple

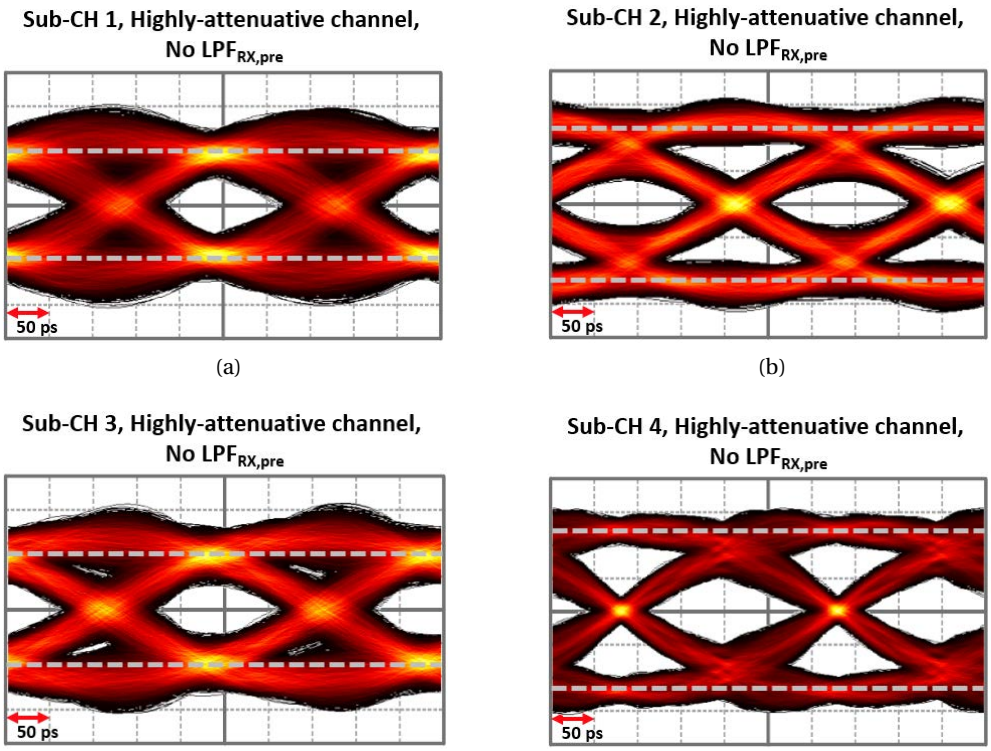


Figure 3.19 – Eye diagrams for demodulated four sub-channels when the transmission medium is highly-attenuative, without the presence of RX low-pass prefilter. (a) $i = 1$, (b) $i = 2$, (c) $i = 3$, and (d) $i = 4$ where i is sub-channel index. Dotted-lines indicate rail-to-rail.

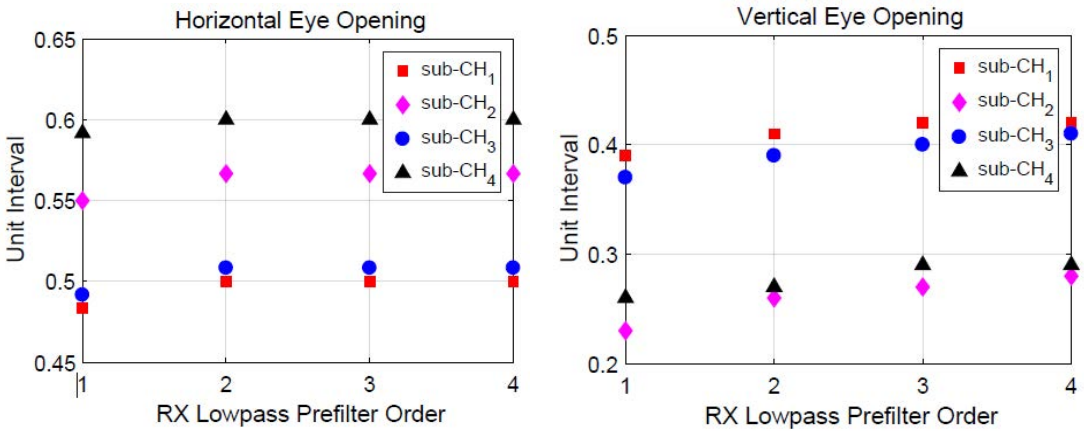
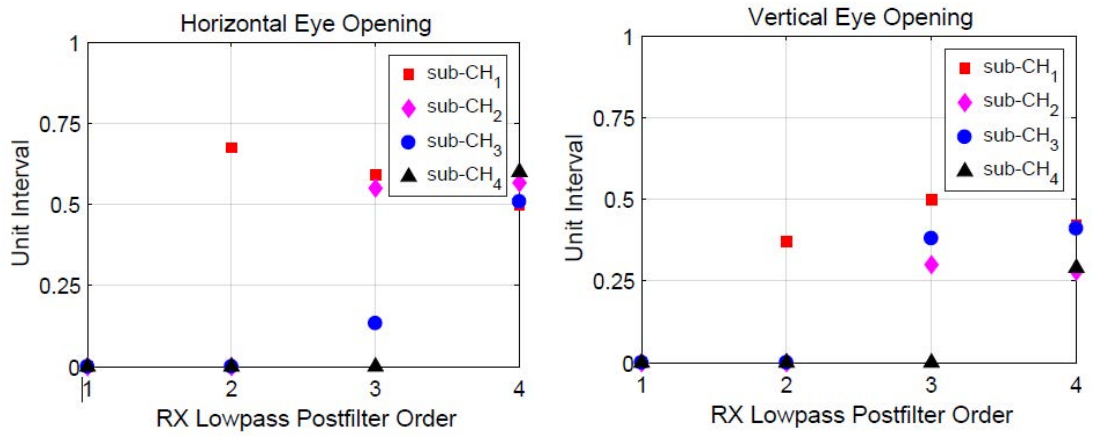
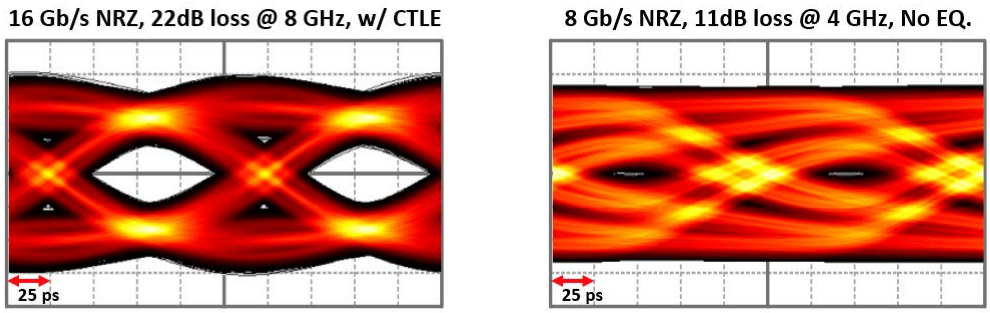


Figure 3.20 – Horizontal and vertical eye openings versus RX prefilter order for communicating over a reference channel.



(a) (b)

Figure 3.21 – Horizontal and vertical eye openings versus RX postfilter order for communicating over a reference channel. RX prefilter is fixed to a 4^{th} order LPF.



(a) (b)

Figure 3.22 – Eye diagrams for (a) 16 Gb/s NRZ with a two-stage CTLE, (b) 8 Gb/s NRZ without equalization.

striplines are series-connected, enabling digital-to-analog and analog-to-digital conversions with sufficient oversampling ratio. The 110.7" stripline composed of 49.5", 22.5" and 38.7" striplines exhibits 13 dB loss at 1 GHz, 23 dB loss at 2 GHz, and 30 dB loss at 3 GHz. The 8-bit DAC transmits SSB-AMT signal consisting of baseband 0.5 Gb/s NRZ (sub-Ch 0), 2 Gb/s PAM-4 upconverted to 1 GHz (sub-Ch 1), 1 Gb/s NRZ upconverted to 2 GHz (sub-Ch 2), and 1 Gb/s NRZ upconverted to 3 GHz (sub-Ch 3), where all RF-bands are single-sideband. All sub-channel data are created based on PRBS-7 sequence, then baseband data is oversampled by 48, RF1, RF2, RF3 bands' data are oversampled by 24, and DAC conversion rate is 24 GS/s.

The spectrum of the emulated AMT signal by DAC at RX front-end is shown in Fig. 3.24 (blue line) together with channel through response (black line), where CK_1, CK_2, and CK_3 represent upconverting clocks. The gain of each sub-channel is provided in such a way that the modulation SNR penalty and channel attenuation with respect to the carrier frequency are

Table 3.2 – Comparison With Other Relevant Works.

Ref.	**[73]**	**[56]**	**[74]**	**[71]**	**This work**
Channel	4″ FR4	7.5″ FR4	40″ Megtron	2″ FR4	**17″ FR4**
Channel Type	P-to-P	4-Drop MDB	P-to-P	P-to-P	**P-to-P**
Signaling	BB+RF	BB+RF	NRZ	RF	**RF**
# of sub-bands	2	2	1	5	**4**
Data rate (Gb/s)	10	7.5	28	4.0	**16**
I/O type	Differential	Differential	Differential	Differential	**Differential**
EQ	-	LPF	5-tap TX FFE, 14-tap RX DFE	LPF	**LPF**
Experiment	measured	measured	measured	measured	**simulated**

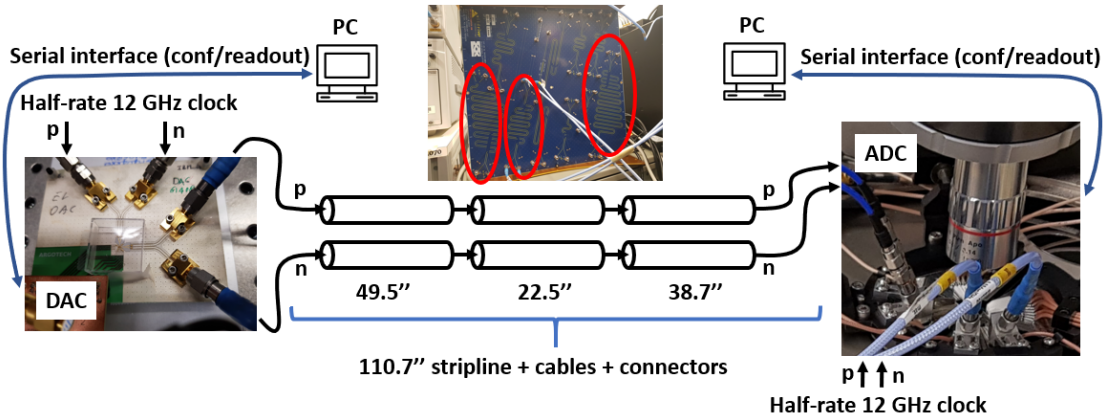


Figure 3.23 – Experiment setup with oversampling DAC and ADC, and series-connected striplines to maximize attenuation for DAC/ADC-based experiment.

partially compensated for, which can easily be integrated in analog summer if implemented in silicon [56]. From the spectrum in Fig. 3.24, it can be observed that the frequency components corresponding to the originally-Nyquist frequency of each sub-band sidelobe are minimally-affected by the neighboring sub-channel spectrum. Fig. 3.26 show the recovered eye diagram from the waveform of which portion is shown in Fig. 3.25, by proper downconverting and filtering. It can be seen that the eyes in each eye diagram are open at 4.5 Gb/s aggregate data-rate without conventional equalizers such as CTLE, FFE/DFE. The measured eye diagrams with NRZ signaling for 1 Gb/s, 1.5 Gb/s and 2.0 Gb/s are shown in Fig. 3.27(a), Fig. 3.27(b) and Fig. 3.27(c) respectively. Without equalization, the eye is closed already from 1.5 Gb/s

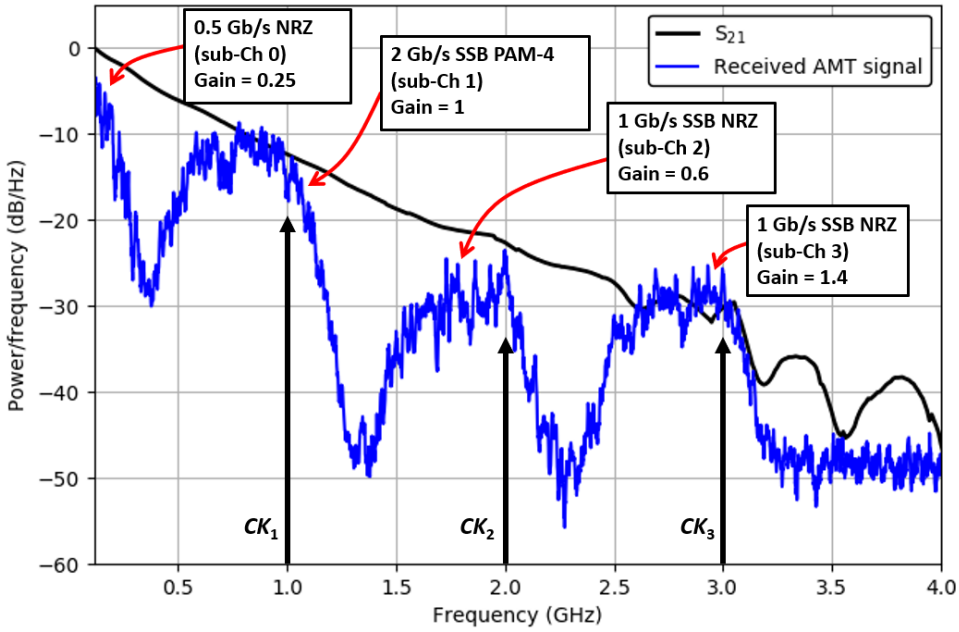


Figure 3.24 – Channel S_{21} frequency response and the measured spectrum of the received 4.5 Gb/s 4-channel digitally-emulated AMT signal.

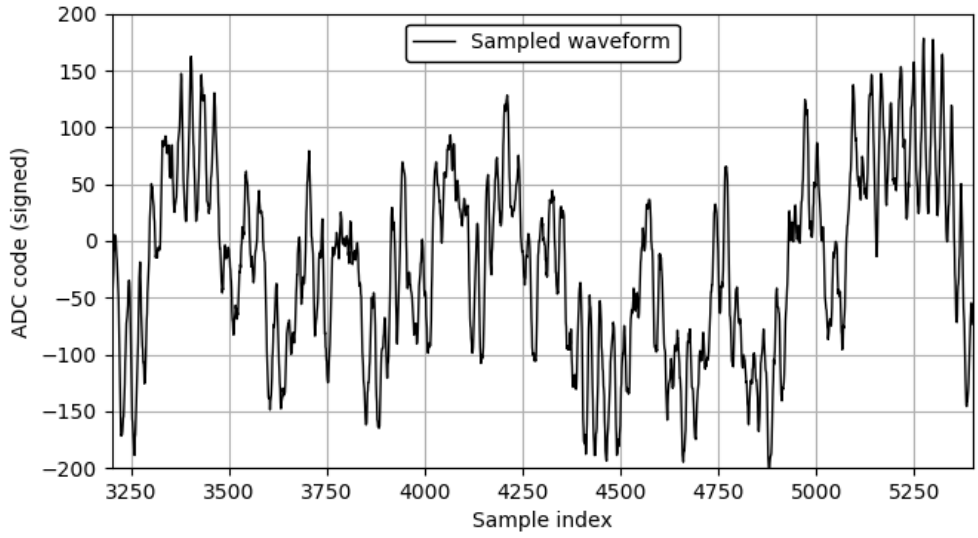


Figure 3.25 – Portion of waveform of AMT signal at the RX front-end sampled by 24-times oversampling 10-bit ADC.

data-rate, and it would require FFE/DFE followed by CTLE to equalize 25 dB loss at 4.5 Gb/s. The proposed SSB-AMT signaling scheme would help in removing the necessity of FFE/DFE in RX at the cost of analog mixing and filtering.

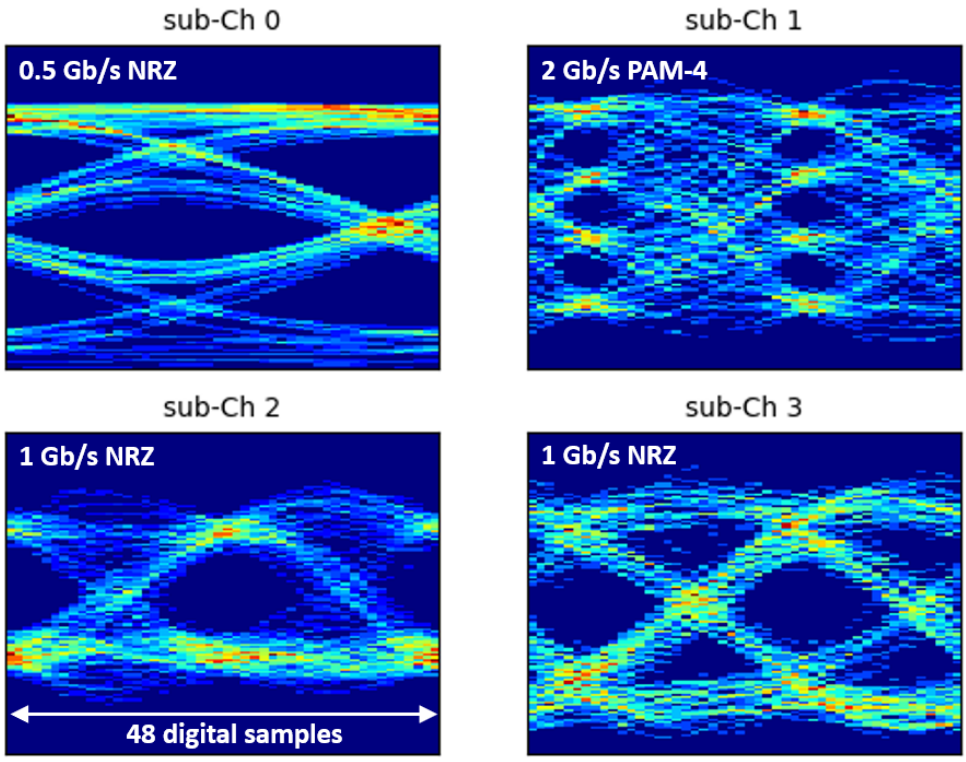
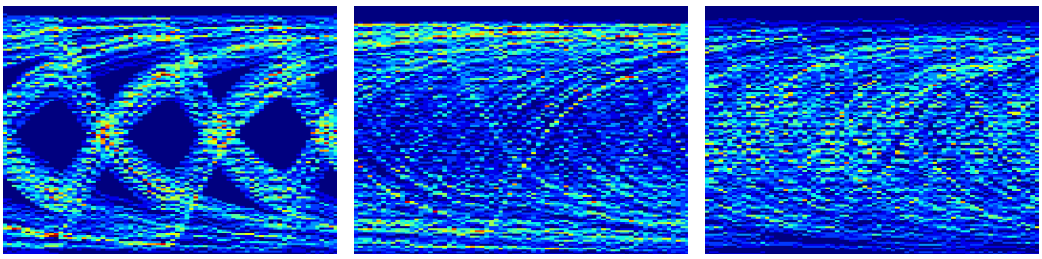


Figure 3.26 – Reconstructed eye diagrams from oversampled RX AMT signal of which spectrum is shown in Fig. 3.24.



(a) (b) (c)

Figure 3.27 – Measured RX front-end eye diagrams of 1 Gb/s NRZ (a), 1.5 Gb/s NRZ and 2 Gb/s NRZ (c) with channel of which frequency response is shown in Fig. 3.24.

3.6 Conclusion

This chapter proposes an AMT/SSB TRX architecture for high-speed chip-to-chip serial link TRX with reduced equalization complexity. The proposed architecture is analyzed including the RF sideband selection mechanism, the channel inversion property, and the downconversion mechanism that is present uniquely in SSB-RF system. Design consideration of filters in the RX data-path for ICI reduction between neighboring AMT sub-channels have been investigated by modeling the proposed TRX for data communication through a measured

channel model. System-level modeling results show that the proposed TRX can communicate over chip-to-chip links exhibiting up to 22 dB attenuation at 8 GHz, at aggregate data-rate of 16 Gb/s with four orthogonal sub-channels without necessitating FFE, CTLE, nor DFE. Supplementary experiments using oversampling D-to-A and A-to-D converters with 110.7” stripline are conducted to demonstrate the proposed concept.

4 ADC-Based Wireline Receiver With Discrete Multi-Tone Signaling

This chapter presents the design and implementation of a high-speed wireline RX for DMT signaling, also known as OFDM. The data-path of DMT RX is designed in a synthesized fully-digital circuit, operating at 1/36-rate of the sampling rate. The prototype chip is implemented in 14nm FinFET process, which achieved 56 Gb/s data-rate consuming 161.46 mW. The DMT RX data-path and test circuitry area is $180 \times 400\ \mu m^2$, excluding input network (ESD and T-coil), ADC and clock-path area.

4.1 Introduction

DMT modulation, which is widely known as OFDM in the wireless communications field, is a digital modulation scheme that separates a wideband frequency bandwidth into multiple narrow frequency sub-channels centered at the carrier frequency of each of those, and all carriers are mutually orthogonal. DMT (OFDM) has been employed in wideband digital wired/wireless communications applications such as audio broadcasting, digital television, digital subscriber line (DSL) internet access, fourth-generation broadband cellular network mobile communications. Some examples of DMT-based standards in wired communications are asymmetric DSL (ADSL) and very-high-bit-rate DSL (VDSL) for data communications over the copper telephone line, G.hn for home local area networking with existing legacy wires, digital video broadcasting-cable (DVB-C) for cable digital television broadcasting. In wireless communications, there are wireless LAN (WLAN) such as IEEE 802.11a/g/n/ac, DVB-terrestrial (DVB-T) for digital terrestrial television broadcasting, long-term evolution (LTE) for high-speed wireless networking for mobile devices, as standards. Leaving the detailed theoretical background about DMT modulation to be referenced to [75, 76, 77], some key background knowledge is re-stated below.

Considering each frequency sub-band independent of each other thanks to the orthogonality, each sub-channel experiences relatively constant channel response in terms of attenuation and phase, over the sub-channel bandwidth. However, the delay spread of the channel still adds the tail of a DMT symbol on top of the head of the following DMT symbol as shown in

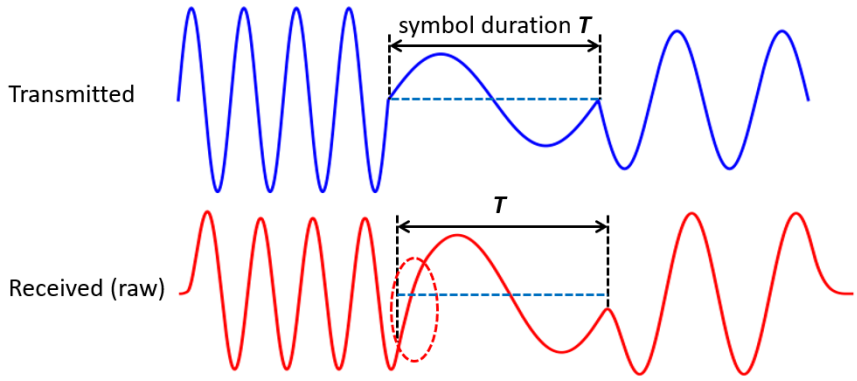


Figure 4.1 – Transmitted 3 consecutive DMT symbols (a) and the received symbols with ISI (red circle).

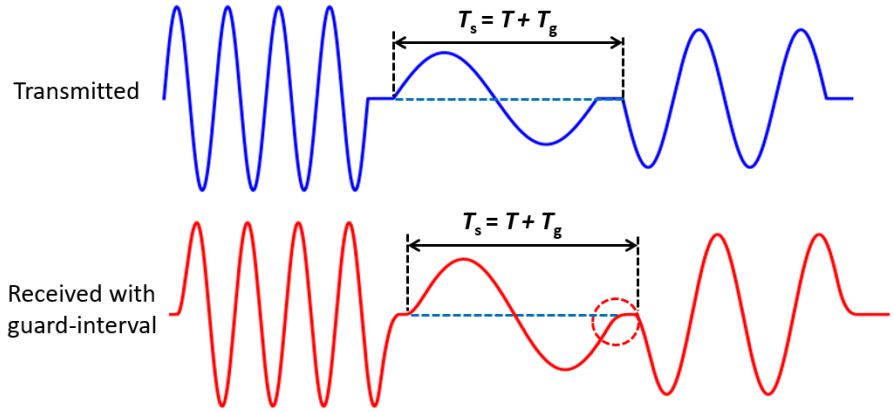


Figure 4.2 – Transmitted 3 consecutive DMT symbols (a) and the received symbols with guard-interval.

Fig. 4.1, introducing ISI (highlighted as red circle in Fig. 4.1). It results in signal distortion and also the loss of orthogonality among sub-carriers. By inserting a guard interval at the end of each symbol at the cost of bandwidth expansion, the DMT symbols can effectively avoid ISI. However, this results in the loss of orthogonality since the effect of delay spread remains within the guard interval, as highlighted by the red circle in Fig. 4.2. Instead of guard-interval insertion, a tail of a DMT symbol can be copied and inserted into the head of the same DMT symbol as a cyclic prefix. This cyclic prefix guarantees the continuity of the frequency components within the guard interval plus symbol period ($T_s + T_g$) as long as the length of cyclic prefix can cover the channel's delay spread. Fig. 4.3 illustrates how the cyclic prefix protects the symbol from ISI. It can be seen that the received waveform shown in Fig. 4.3 maintains an entire period of a sine wave of the second symbol after the reception, while it is not the case with a raw transmission or with guard-interval shown in Fig. 4.1 and Fig. 4.2, respectively. Hence, even if the channel impulse response exhibits long delay spread, the ISI induced by the delayed past symbol can be covered by the cyclic prefix if the length of the cyclic prefix is sufficiently long, and the DMT symbol is not affected by ISI, at the cost of bandwidth

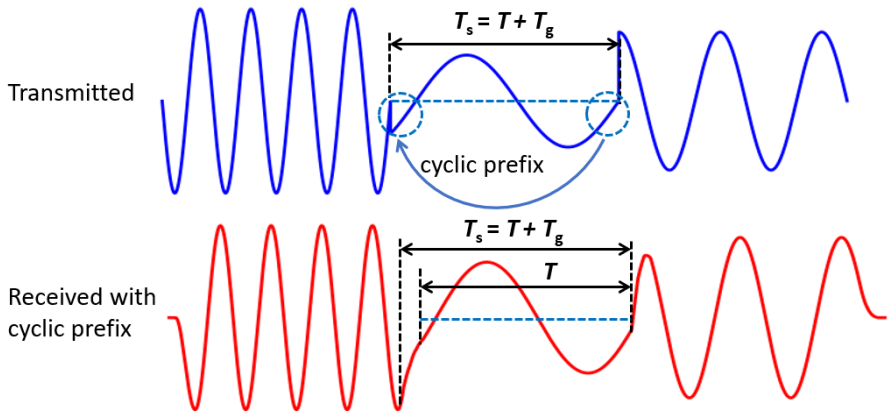


Figure 4.3 – Transmitted 3 consecutive DMT symbols (a) and the received symbols with cyclic prefix.

expansion due to the redundant samples. Although ISI can be handled by sufficiently long cyclic prefix, its length has to be traded-off with data-rate in a bandwidth-limited system.

In order to increase the bandwidth efficiency of the DMT system, higher-order constellation size can be constructed by assigning more bits to each of sub-channels. For example, 64-QAM exhibiting 6 bits/Hz of bandwidth efficiency is adopted in LTE, while LTE-A Pro uses 256-QAM (8 bits/Hz) having 33% higher data transmission rate than that of LTE, given the bandwidth constraint. However, moving toward higher-order modulation requires higher SNR for achieving the same BER. In PAM-4 systems (time-domain signaling), the bandwidth efficiency is 4 bits/Hz, which corresponds to 16-QAM DMT equivalent without considering cyclic prefix. Hence, in order for the DMT solution to be potentially more interesting than PAM-4 in terms of bandwidth efficiency, at least 32-QAM with cyclic prefix length not longer than 25% of symbol length should be considered.

Since DMT is digital modulation, data conversions for transmission and reception are essential. High-speed CMOS data converters for wireline communications that operate at tens of GS/s have limited signal-to-noise and distortion ratio (SNDR) (< 40dB at Nyquist) [10, 11, 12, 13, 78] as compared with sub-GS/s converters targeted for wireless communications [79, 80, 81] with SNDR> 60 dB at Nyquist. Such limitations in quantization noise in ultra-high-speed digital wireline serial link limit the adoptable maximum modulation order. Addressing this together with the bandwidth limitation given the target data-rate, a cyclic prefix length equivalent to 12.5 % of symbol length is chosen in this work, and the maximum modulation order is set to 64-QAM. When the bits are maximally loaded, the implemented system communicates at 56 Gb/s data-rate occupying 11.2 GHz of bandwidth, which is 25 % more bandwidth-efficient than a PAM-4 equivalent system.

One of the main advantages of DMT modulation over time-domain modulations such as NRZ or PAM-4 is its immunity to ISI thanks to the cyclic prefix (as long as the cyclic prefix's length is sufficiently long). Moreover, although the cyclic prefix cannot cover the entire post-cursor tail,

the effect of ISI is spread out over the entire bandwidth, resulting in minor SNR degradation per sub-channel as long as all the channels have enough SNR margin given target BER. Hence, there is no need for symbol-by-symbol feedback to cancel ISI out in a DMT system. Such symbol-by-symbol-feedback-free nature allows the data-path to be fully-parallel, enabling the physical design flow to be in semi-custom style without stringent timing constraints. This reduces the design effort and improves the design portability to different process technologies, and the implemented circuit can be low-power architecture with relaxed timing constraints. Moreover, DMT signaling features high bandwidth efficiency and high flexibility to allocate a different number of bits and power to accommodate the communication medium's (channel) characteristics. On the other hand, the inherent parallel data-path due to the property of DMT signaling and arithmetic-intensive DSP architecture requiring multiple pipeline stages cause high latency. Thus, DMT signaling is more suitable to applications that exhibit inherently high latency due to the use of FEC, such as IEEE p802.3bj or p802.3bs standards.

A DMT TRX using a maximum of 15 frequency-domain sub-channels (excluding DC) is described in this chapter. An 8-bit DAC available from [25] is used as DMT TX where the symbols to be transmitted are constructed from PC. The implemented RX consists of a 10-bit 48-way time-interleaved ADC (only 8 LSBs are used out of 10 bits), a 32-point Fourier transform processor, frequency-domain equalizer, on-chip test circuitry for BER measurement and constellation scanner. Implemented in 14nm FinFET process, the data-rate is measured at 56 Gb/s for communicating over a channel exhibiting 18 dB attenuation at 14 GHz, while the occupied bandwidth is 11.2 GHz. The total power consumption is 161.46 mW, where 93.24 mW is consumed in ADC (including the clock path and the interleaver) and 68.22 mW is consumed in RX data-path.

4.2 Transmitter Architecture

The DMT transmitter's conceptual block diagram is shown in Fig. 4.4. While the RX is fully-implemented on silicon, a general-purpose DAC with 32-kByte memory is used as DMT TX. The building blocks shown in Fig. 4.4 are implemented as Python model that outputs the DMT symbols to be transmitted by DAC.

Three independent parallel 32-output pseudo-random binary sequence (PRBS) generators distribute pseudo-random bits to I/Q phases of 16 sub-channels. Constellation mapper maps a set of time-domain pseudo-random bits to frequency-domain complex constellations with minimum modulation order of PAM-2 and maximum modulation order of 64-QAM for each sub-channel, and it can disable each sub-channel independently from one to others. Before the inverse discrete Fourier transform (IDFT) stage, the frequency-domain symbol corresponding to DC sub-channel is ignored and replaced by zero, in order not to have any baseband components in the data spectrum. Since the IDFT output should be a purely real number to be able to be transmitted without up/down-conversion with analog mixers, the 15 non-zero-forced sub-channel symbols corresponding to the first-half IDFT bin inputs are

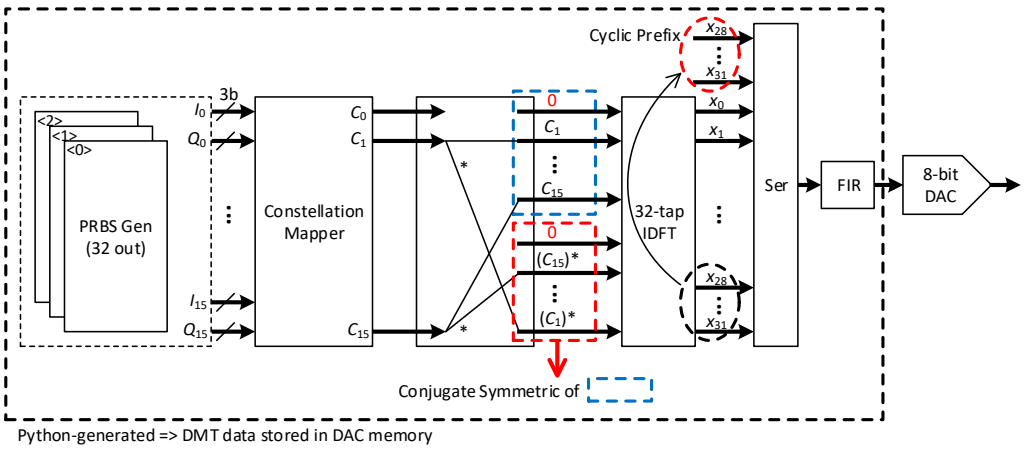
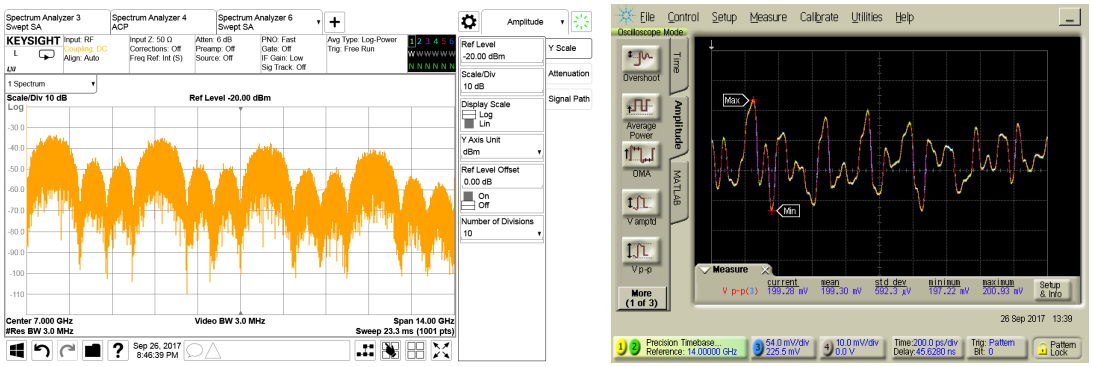
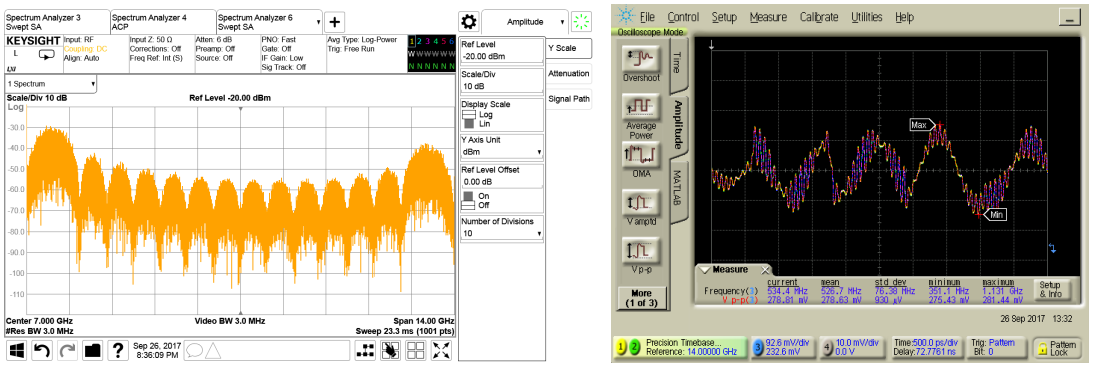


Figure 4.4 – DMT TX block diagram.



(a) (b)



(c) (d)

Figure 4.5 – Measured spectrum (a) and waveform (b) of the transmitted data (without TX FIR) at 28 GS/s conversion rate for DMT symbols with 1/5/9/13th activated sub-channels, and spectrum (c) and waveform (d) with 1st and 15th activated sub-channels.

complex-conjugated and copied symmetrically to the second half IDFT bin inputs. Then, the 4-sample tail of the time-domain IDFT output, i.e., DMT symbol, is replicated to the head of the DMT symbol as cyclic prefix.

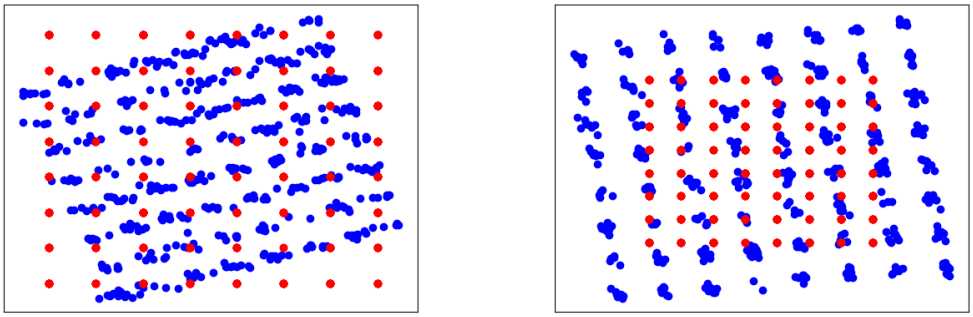
Fig. 4.5(a)-(b) show an example of DMT transmission with 28 GS/s digital-to-analog conversion speed when 1^{st}, 5^{th}, 9^{th} and 13^{th} sub-channels are enabled. The spectrum of the measured transmitted DMT signal is shown in Fig. 4.5(a), clearly showing the power at the enabled sub-channels, and its time-domain waveform is shown in Fig. 4.5(b). It is difficult to extract bit information from Fig. 4.5(b) unlike time-domain signaling, and individual frequency components are not noticeable from the time-domain waveform. Fig. 4.5(c)-(d) show the measured transmitted spectrum and time-domain waveform when the first (1^{st}) and the last (15^{th}) sub-channels contain data while the others are disabled. Fig. 4.5(c) shows the activated sub-channels where the high-frequency sub-channel's amplitude is attenuated by cable's insertion loss. Fig. 4.5(d) gives clear indication about the frequency components' information contained in the transmitted signal, where the amplitude attenuation is also noticeable.

The TX FIR filter can pre-distort the signal to be transmitted for effective channel shortening. As an example, Fig. 4.6(a) and Fig. 4.6(b) shows the first (sub-channel 1) and second-last (sub-channel 14) sub-channels' 64-QAM constellation diagrams, respectively, where red dots represent symbol values before FIR-filtered and blue dots represent FIR-filtered symbols. From these FIR-filtered constellations, phase rotation, relative high-frequency amplitude expansion compared with low-frequency amplitude, and the effect of ISI (pre-distortion) are noticeable. Since the cyclic prefix of length 12.5%×symbol length in the implemented system can cover only a limited number of post-cursor taps, the FIR filter should be designed in such a way that it minimizes pre-cursors and the uncovered post-cursors in the converter's sampling-rate-pulse response. This is implemented based on the iteration loop in Python searching for the optimal tap coefficients that minimize the sum of the uncovered cursor taps with respect to the main cursor's amplitude. The resulting Python-generated floating-point symbols (with or without FIR filter) are converted to 8-bit-wide words, then a string of these 8-bit words is stored in the 8-bit Nyquist-rate DAC memory.

4.3 Receiver Architecture

The key building blocks of DMT RX are a medium-to-high-resolution high-speed ADC, a high-throughput low-power discrete Fourier transform (DFT) processor, and a low-power frequency-domain equalizer (FDE). Each of these building blocks should provide high SNR on its output, under high-speed operation with limited power budget. Therefore, given the ADC's SNDR, the DFT processor and the FDE should be designed in such a way that their area is not wasted by redundant bits on their data-path.

Fig. 4.7 shows the block diagram of the implemented DMT receiver. The on-die terminations (ODT) at ADC inputs ($V_{IN,N}$, $V_{IN,P}$) and half-rate clock inputs ($C2_N$, $C2_P$) include differential 100 Ohm resistor and T-coil for bandwidth extension, compensating for the parasitic capaci-



(a) (b)

Figure 4.6 – Constellation diagrams of the 1st (a) and the 14th (b) sub-channels, with red dots representing pre-FIR constellation and blue-dots representing post-FIR constellation.

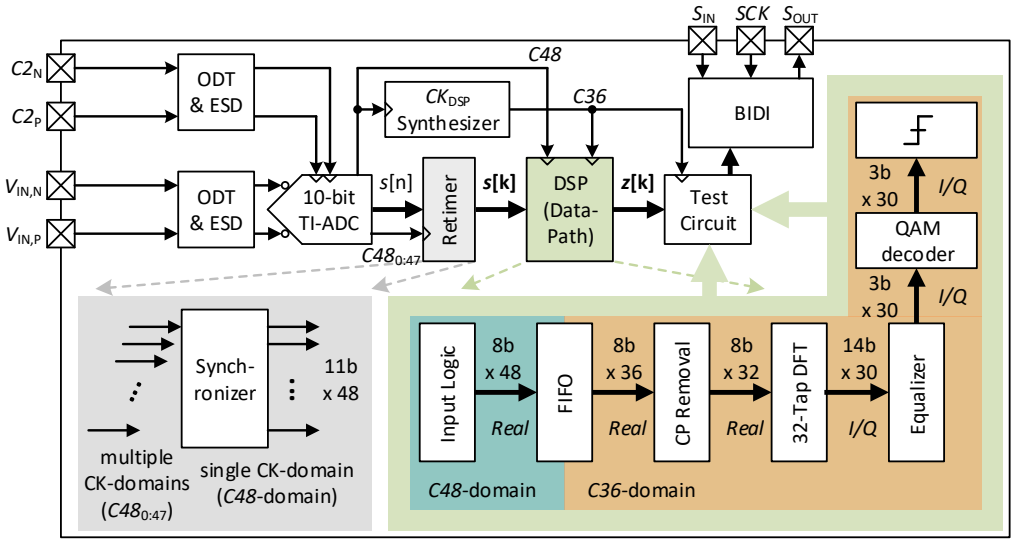


Figure 4.7 – Implemented DMT RX block diagram.

tances coming from the input pad and ESD protection circuit. The analog input differential signal is discretized by a 10-bit 48-way time-interleaved pipelined successive approximation register (PL-TI-SAR) ADC, which outputs 11-bit raw binary code per sub-ADC including one bit of redundancy. The retimer synchronizes the time-interleaved 48 output words (or samples) in 48 different phases of 1/48-rate clocks (C48) into a single C48-domain so that the DSP receives an aligned packet of 48 × 11 bits.

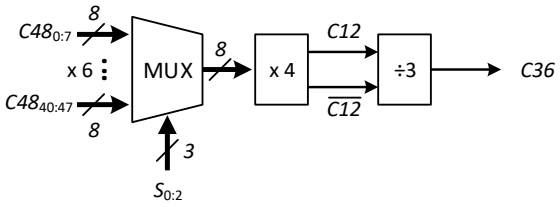
As described in sub-chapter 4.1, the number of cyclic prefix for a DMT (or OFDM) symbol

with 32-tap DFT is chosen to be 4. Since the DFT performs one conversion of 32 time-domain samples into 32 frequency-domain samples per DSP clock cycle, 36 samples have to be processed in each DSP clock cycle, taking the cyclic prefix into account. Given that the ADC architecture is fixed to the 48-way interleaved architecture, a FIFO that receives 48 words and outputs 36 words is required to bridge the ADC and the DSP core. Thus, the DSP clock operating at 1/36-rate is synthesized by a clock synthesizer which multiplies C48 by 4/3. The DSP clock synthesizer consists of a phase selector, a ×4 multiplier, and a divide-by-3 circuit, as shown in Fig. 4.8(a). The phase selector selects eight C48 phases that are used to the synthesized C36 clock out of 48 phases, determining the phase of the synthesized C36 clock for configurability. The selected 8× C48 clocks are multiplied by a factor of 4 with XOR-based clock multiplier to make a differential 1/12-rate clock (Fig. 4.8(b)), then the differential C12 clocks are divided by factor of 3 to synthesize a single C36 clock (Fig. 4.8(c)). All data-path and test circuitries coming after FIFO are clocked by C36 clock, while bidirectional serial interface circuit (BIDI) for chip configuration and data readout is clocked by a separately provided slow-clock (SCK).

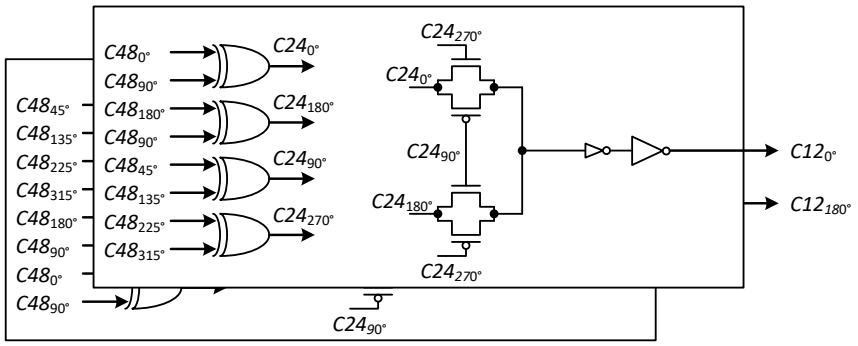
The 11-bit raw ADC output words are translated into 10-bit words and offset-calibrated with off-chip offset calibration code estimation. As the ADC has limited ENOB, not the entire 10 bits are required to go through the data-path. Considering that the ADC provides about 6.5-ENOB over the bandwidth-of-interest, e.g., $f \leq 11.2$GHz for 56 Gb/s data-rate, only the first 8 MSBs form a data-path input word. The switchbox is used to delay the most recent 48×8-bit packets in order to align 2×48 consecutive words, and to take 48 words of which the first word corresponds to the head of a DMT symbol, i.e., the first element of the cyclic prefix, as shown in Fig. 4.9. A FIFO interfaces the C48/C36-domain crossing, and the 4 cyclic prefix elements are removed by simply disregarding these 4 elements out of 36 incoming words.

The DMT symbol synchronization by searching for the cyclic prefix location is performed off-chip together with the best ADC sampling phase search, based on training sequences. Having information of a portion of the transmitted sequence, the phase search engine sweeps the signal generator's phase with a fine-step. For each phase, a cross-correlation of the transmitted training sequence with the received sequence without knowing phase and cyclic prefix's location is computed, by sweeping the potential location of the first cyclic prefix sample. Thus, the search engine features two loops in which the best phase and cyclic prefix location that results in the highest similarity of the received and transmitted signals are updated. Since the DMT TRX system is considered to use synchronized reference clocks in both TX and RX chips, a single set of phase and cyclic prefix starting point can be found only once at the beginning of the measurement. However, when TX and RX do not receive synchronous reference clocks, the ADC sampling phase and clock frequency would have to be found with on-chip CDR circuit. Alg. 1 presents the pseudo-code of the phase and cyclic prefix search algorithm.

The time-domain received signal is then converted to frequency-domain by a 32-tap DFT processor. Since the DFT is arithmetic-intensive and should operate at > 620 MHz for 56 Gb/s data-rate, the implemented DFT processor features a fully-parallel data-path to maximize the



(a)



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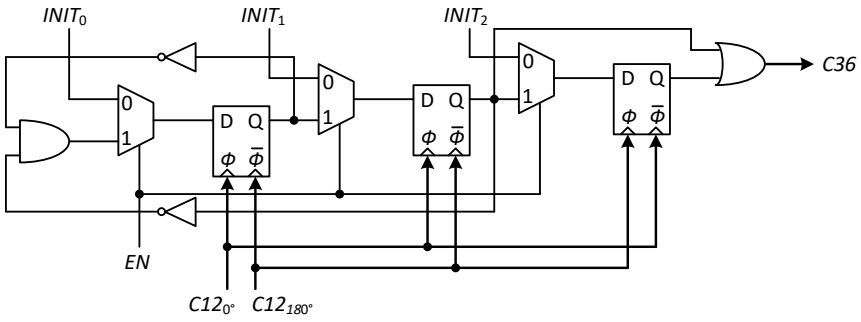


(c)

Figure 4.8 – A DSP clock synthesizer block diagram (a), multiply-by-4 circuit detail (b), and divide-by-3 circuit detail (c).

throughput, and Winograd small DFT-based architecture is chosen for high area-efficiency. While Winograd small DFT algorithm exhibits non-regularity making its full-custom style digital implementation difficult and unfriendly architecture for implementation on general-purpose DSP, it does not have particular disadvantage coming from non-regular architecture

Algorithm 1 Search for the optimum sampling phase and beginning of the cyclic prefix

procedure PHASEANDCYCLICPREFIXSEARCH
    transmit training sequence of length $L_{\text{training}} \times 2$
    $A_{max} \leftarrow 0$
    for $\theta_{\text{RX}} \in [0, 360[$ **do**
        Sample training sequence of length L_{training}
        for $ii_{\text{RX}} \in [0, L_{\text{training}}[$ **do**
            $x_{\text{TX,REF}} = x_{\text{TX}}[ii_{\text{RX}} : ii_{\text{RX}} + L_{\text{training}}]$
            $A \leftarrow max(xcorr(x_{\text{RX}}, x_{\text{TX,REF}}))$
            if $A > A_{max}$ **then**
                $A_{max} \leftarrow A$
                $\theta_{\text{RX,opt}} \leftarrow \theta_{\text{RX}}$
                $ii_{\text{RX,opt}} \leftarrow ii_{\text{RX}}$
            end if
        end for
    end for
end procedure

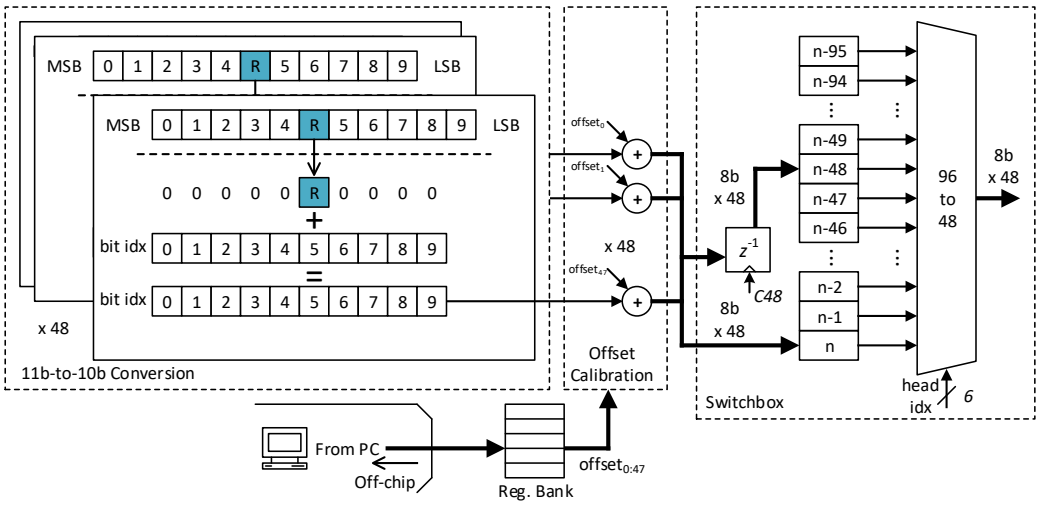


Figure 4.9 – Input layer details.

when implemented in semi-custom style digital application-specific integrated circuit (ASIC) based on hardware description language (HDL), as compared with Cooley-Tukey fast Fourier

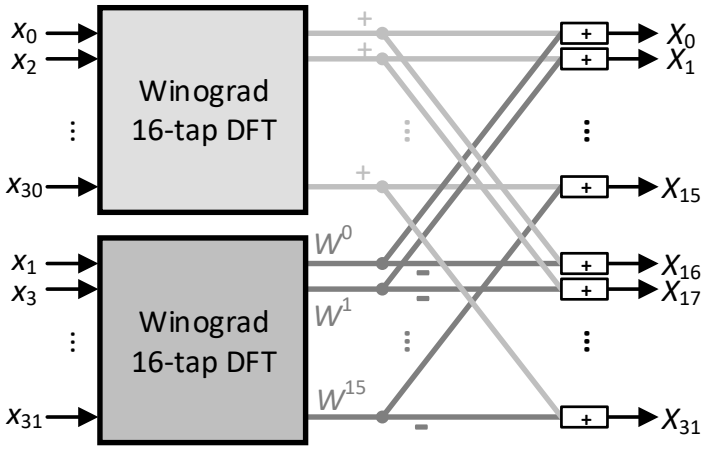


Figure 4.10 – A 32-tap DFT architecture based on two Winograd 16-tap DFTs.

transform (FFT) algorithm. As

$$\begin{aligned} X_{k,[0:N-1],N-tap} &= \sum_{n=0}^{N-1} x_n \cdot e^{-\frac{2k\pi j}{N} n} \\ &= \left(\sum_{r=0}^{\frac{N}{2}-1} x_{2r} \cdot e^{-\frac{2k\pi j}{N} 2r} \right) + \left(\sum_{r=0}^{\frac{N}{2}-1} x_{2r+1} \cdot e^{-\frac{2k\pi j}{N}(2r+1)} \right) \\ &= \left(\sum_{r=0}^{\frac{N}{2}-1} x_{2r} \cdot e^{-\frac{2k\pi j}{\frac{N}{2}} r} \right) + \left(e^{-\frac{2k\pi j}{N}} \cdot \sum_{r=0}^{\frac{N}{2}-1} x_{2r+1} \cdot e^{-\frac{2k\pi j}{\frac{N}{2}} r} \right) \\ &= X_{k,even,N/2-tap} + e^{-\frac{2k\pi j}{N}} \cdot X_{k,odd,N/2-tap} \end{aligned} \tag{4.1}$$

, where $X_{k,[0:N-1]}$ denotes the value of the k^{th} bin of N-tap DFT with $x_{0:N-1}$ complex numbers, a 32-point DFT ($N = 32$ from 4.1) can be decomposed into two 16-tap DFTs with a twiddling network. As the DFT input signal is known to be purely real without any imaginary term, the DFT complexity can be further reduced (to almost half the size of the full DFT), which has not been taken into account in this test chip implementation. Fig. 4.10 shows the designed 32-tap DFT architecture based on two 16-tap Winograd DFTs, where $W = e^{-\frac{2\pi j}{N}}$. As a twiddling factor multiplier, a complex multiplier of the 3-multiplier/5-adder structure is employed instead of the 4-multiplier/3-adder structure to save area, where the two corresponding equations can be expressed as

$$(a+bj)\cdot(c+dj) = ac - bd + j\big((a+b)\cdot(c+d) - ac - bd\big) \tag{4.2}$$

$$= (ac - bd) + j(ad + bd) \tag{4.3}$$

, respectively (4.2 and 4.3).

Table 4.1 – Number of real multipliers and adders in some Winograd small DFTs for complex data with length of power-of-2.

Length	Trivial Mult.	Non-Trivial Mult.	Adds	# W for DFT32	Total Eq. Adds
2	4	0	4	49	1485
4	8	0	16	41	1317
8	12	4	52	29	1177
16	16	20	148	15	1051

Unless area saving coming from the use of smaller Winograd DFT blocks is larger than the area overhead coming from additionally required twiddling factor multipliers, choosing relatively larger unit Winograd DFT blocks is beneficial in both for RTL design complexity and area perspectives. Table 4.1 shows the number of required arithmetic operators in some Winograd short DFT with lengths of power-of-two, and the number of required twiddling factors, i.e., complex multipliers, to form a 32-tap DFT based on each Winograd DFT block, and the equivalent number of adders estimated from the required arithmetic resources. Although the number of equivalent adders is obtained with limited rigorousness by assuming that one real multiplier is equivalent to eight real adders, it gives enough guidance which architecture is most area-efficient. The Winograd 16-tap DFT is implemented based on the algorithm described in [82].

As the output of 32-tap DFT is conjugate symmetric, only 16 out of 32 output bin complex values are needed for further processing toward FDE which rotates the tilted frequency-domain symbols back to the original constellations with amplitude adjustment. Assuming that each sub-channel experiences a flat channel frequency response within sub-channel bandwidth, the above-mentioned procedure can be analytically expressed as

$$\begin{aligned} \hat{X}_{\mathrm{k}} &= X_{\mathrm{RX,k}} \cdot H_{\mathrm{FDE,k}} \\ &= X_{\mathrm{TX,k}} \cdot H_{\mathrm{FIR,k}} \cdot H_{\mathrm{CH,k}} \cdot H_{\mathrm{FDE,k}} \end{aligned} \tag{4.4}$$

, where $\hat{X}_{\mathrm{k}}$ is the equalized symbol, $X_{\mathrm{RX,k}}$ is the received symbol after Fourier transform, $X_{\mathrm{TX,k}}$ is the original symbol to be recovered, $H_{\mathrm{FDE,k}}$ is the FDE's complex coefficient, $H_{\mathrm{FIR,k}}$ is the TX FIR filter's frequency response, and $H_{\mathrm{CH,k}}$ is the channel frequency response, all in k^{th} frequency bin and without taking the quantization effect and other noise into account for $k \in \{1, 2, \cdots, 15\}$ ignoring DC bin ($k = 0$).

Fig. 4.11 illustrates a frequency-domain equalization example. Due to the low-pass filter nature of the transmission line, received signal at higher-frequency sub-bands tends to be more attenuated than low-frequency sub-bands. Equalization at FDE should invert the channel attenuation, by applying an amplification factor. Moreover, frequency-dependent phase delay that translates into constellation rotation should properly be equalized in the FDE. Hence, equalization coefficients should be in the complex domain, and their norm is the inverse of

the corresponding sub-channel attenuation, and their angle is the negation of the frequency-dependent rotation due to the channel. However, the norm of equalization coefficients for each sub-channel can vary significantly from one sub-channel to another, since the channel attenuation increases exponentially as frequency (or sub-channel index) increases linearly. For example, the coefficient values in red-circles in Fig. 4.11 are much smaller than those in blue-circles in Fig. 4.11. This can translate into an inaccurate rotation and/or amplitude expansion of the constellation diagram of the sub-channels corresponding to the small equalization coefficient norms.

Fig. 4.12 shows the FDE architectures, where Fig. 4.12(a) shows the simplest form of FDE only using a complex multiplier array, and Fig. 4.12 shows the FDE architecture implemented in this work addressing the above-mentioned issue. The data-path corresponding to DC-band is not shown in both sub-figures and the first bit of equalization coefficient is sign-bit and the rests are weights ranging from 2^{-1} to 2^{-8} (8-bit weights), with normalization to ± 1 for each of real/imaginary parts. In Fig. 4.12(a), the sub-channel 1 is 8× less attenuated than the sub-channel 15 if the effective channel loss difference is around 18 dB. The off-chip-computed equalization coefficients' decimal values are converted to 9-bit signed binary with equal bit-weights. The sub-channel 1 coefficient cannot use the full fixed-point length due to the too small norm, wasting the first 4 MSB weights as continuing sign-bits. For sub-channel 15, there can be wasting weight bits if the normalized coefficient norms are less than 0.5 although the number of wasted weight bits is less than that of sub-channel 1. In Fig. 4.12(b), the number of wasted weight bits is minimized by pre-multiplying small weight values by powers of 2, before converting the computed coefficients' decimal values to binary. By doing so, the weight bits of at least for one of real or imaginary parts are always used for every sub-channel. Then, each complex multiplier's output is divided by an appropriate factor by shifting to the right. This guarantees the maximum usage of existing weight bits of equalization coefficients' registers providing more accurate angular rotation and magnitude adjustment of the sub-channel constellation diagram.

4.4 Measurement Results

Fig. 4.13(a) illustrates the measurement system setup. The packaged 8-bit DAC [25] transmits DMT symbols and the RX is tested without packaging but directly on the probe station as shown in Fig. 4.13(b). The ADC's input differential clock buffer supply, ADC's interleaver supply, the ADC analog power domain supply and the DSP supply are 0.8 V, 0.7 V, 0.7 V, and 0.75 V respectively, provided by Agilent N6705B, for 56 Gb/s data-rate. The 8-bit DAC operates under 1 V for the digital parts and for the output driver, and 0.95 V for the clock driver, which are provided by Agilent E3642A (also used for the input and the clock common-mode of the ADC). The RX DMT prototype chip is fabricated in GlobalFoundries 14nm FinFET LPP process with the DSP core area of $180 \times 400 \mu m^2$, of which die photo and layout organization are shown in Fig. 4.14. The ADC from [83] occupies $300 \times 400 \mu m^2$ of area and the DSP height is chosen accordingly despite of its high aspect ratio. About 32% of the DSP area is used for sequential

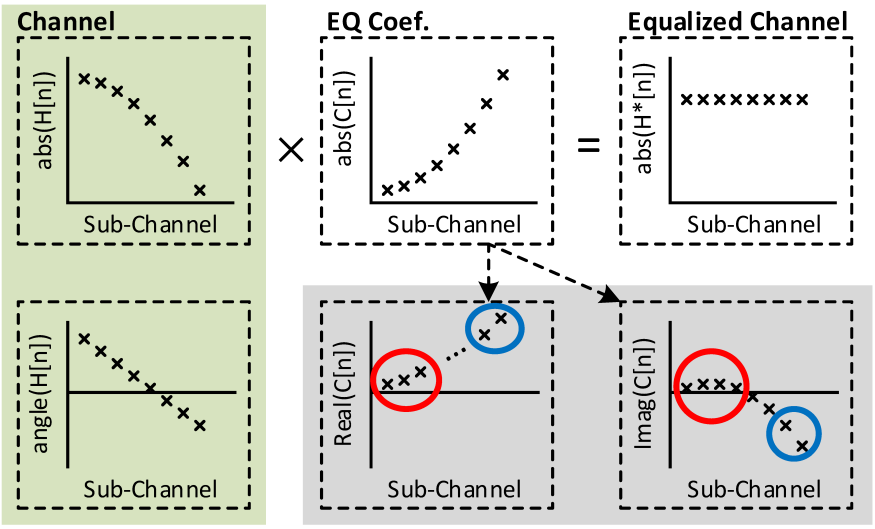
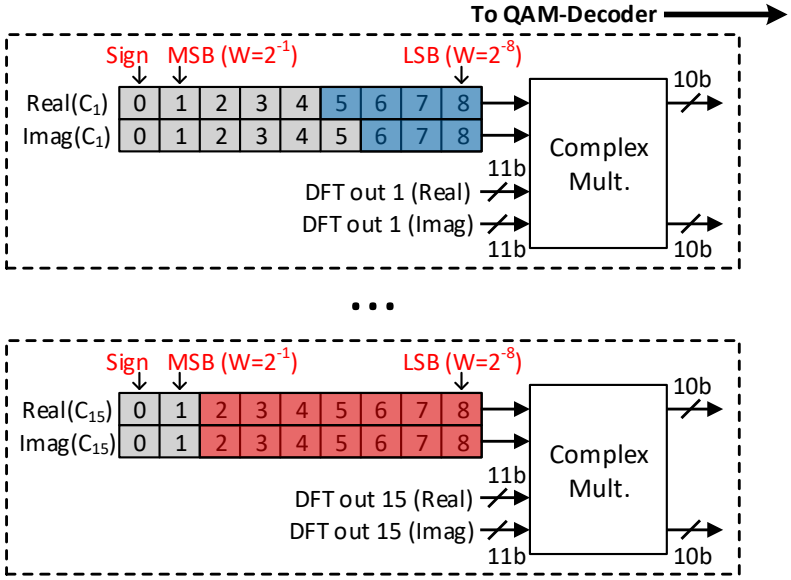


Figure 4.11 – Illustration of frequency-domain equalization.

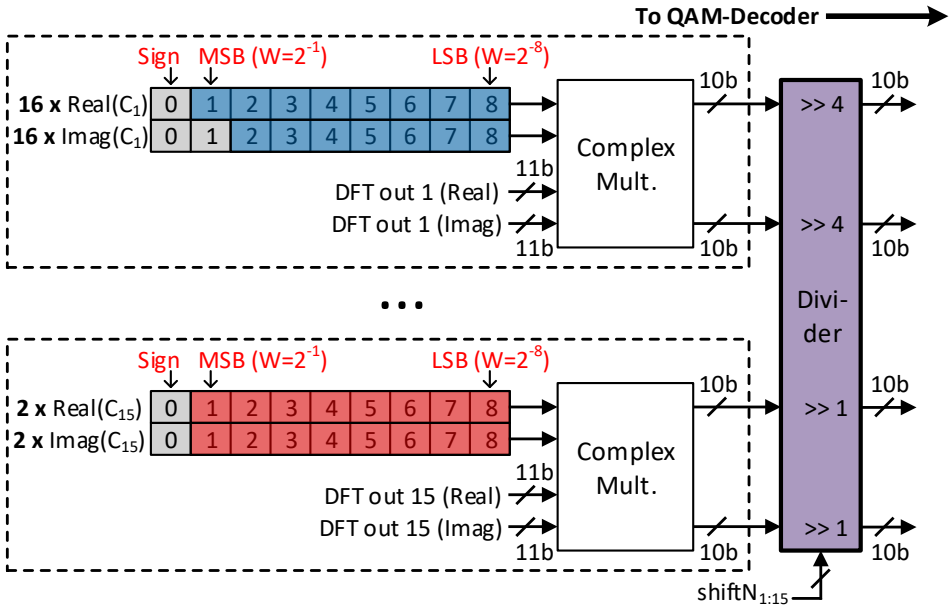
cells and 68% is used for combinational logic.

The performance has been measured for three different channels of which time-domain and frequency-domain characteristics are shown in Fig. 4.15(a)-(f). Unlike time-domain signaling where widely-used test sequence such as PRBS with length 7/11/15/23/31 is well-defined, the implemented DMT link uses a custom-defined test sequence due to the limited memory size (32 kBytes) of the DAC used as DMT TX. The three independent PRBS generators stream out PRBS sequences with independent seeds so that the mapped DMT symbols are mostly uncorrelated. As DMT mapping with three PRBS-7 is too short to guarantee pseudo-random DMT symbols over the entire DAC memory cycle, portions of three PRBS-15 are used to map DMT symbols with sufficient randomness to test the implemented system.

The DMT test sequence based on three PRBS-15 is generated in PC and stored in DAC memory and is repeatedly transmitted. Due to the frequency-selective attenuation of the channel, the SNR of the higher frequency sub-channels are more degraded as compared with the lower frequency sub-channels. This results in higher symbol-error rate (SER) and thus higher BER at higher frequency sub-bands as compared with that of lower frequency sub-bands, if the same number of bits and power are assigned to all sub-channels equally. On top of this, the uncompensated long-tail post-cursors of the pulse response that are not covered by the cyclic prefix with limited length result in non-orthogonality among sub-channels, worsening the overall BER with ISI. Hence, a TX digital FIR filter is considered in order to shorten the effective channel and is pre-applied before storing the data to be transmitted in DAC memory. Water-filling algorithm for optimum bit-loading can be applied to address the frequency-dependent channel attenuation. However, with a fixed target data-rate, the overall DMT bandwidth

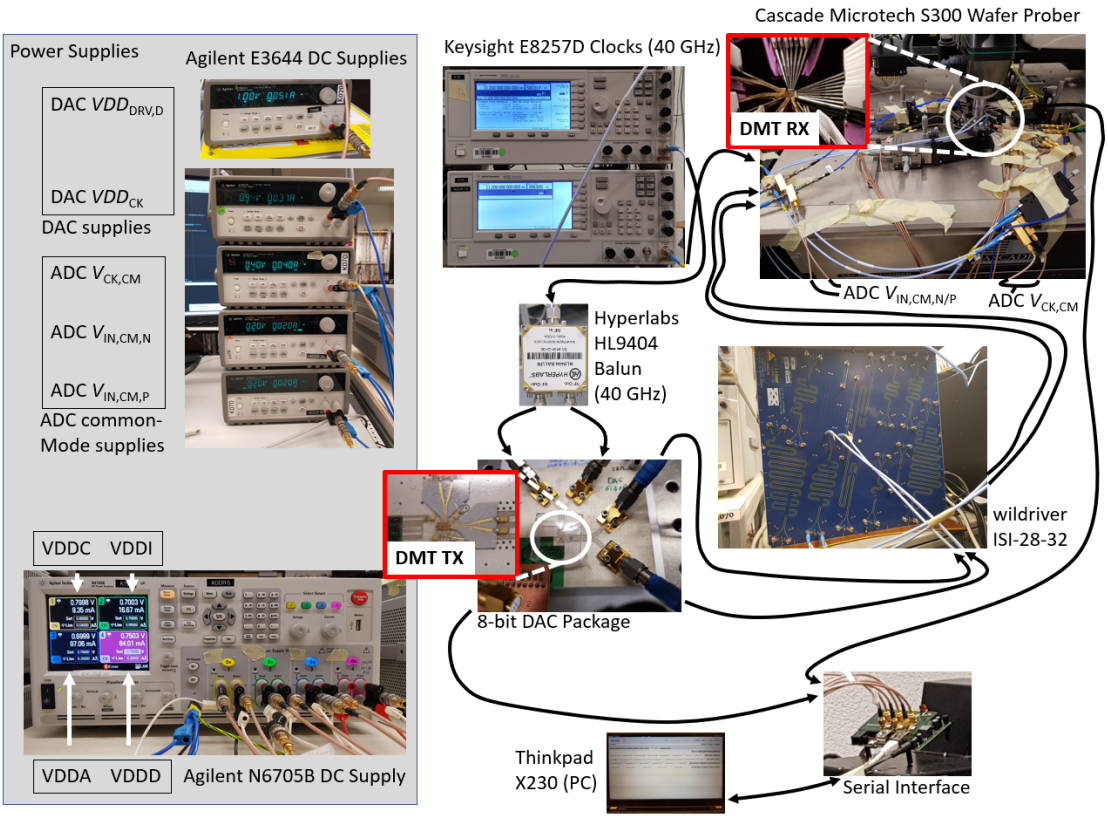


(a)

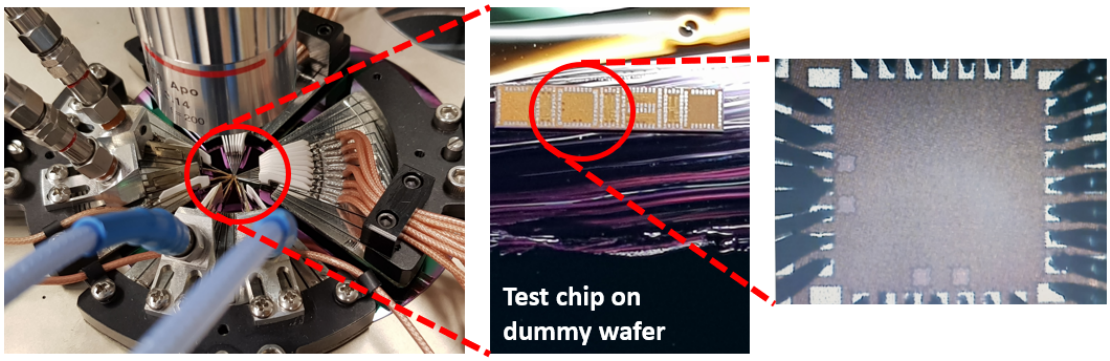


(b)

Figure 4.12 – The FDE architecture without per-sub-channel coefficient gain adjustment (a) and with per-sub-channel coefficient gain adjustment (b).



(a)



(b)

Figure 4.13 – Measurement setup (a) and DMT RX die with direct probing (b).

should be increased if less number of bits is assigned to higher SNR frequency slots, which results in more ADC/DSP power consumption and longer pulse response requiring longer cyclic prefix taps. Different types of experiments are performed to identify the effects of each factor: bit-loading given the data converters' sampling rate and equal power for all sub-channels; power-loading given the data converters' sampling rate with an equal number of bits for all sub-channels; the presence of channel-shortening FIR filter. For all measurements, the overall time-domain DMT symbols' amplitude and ADC's input dynamic range are scaled in

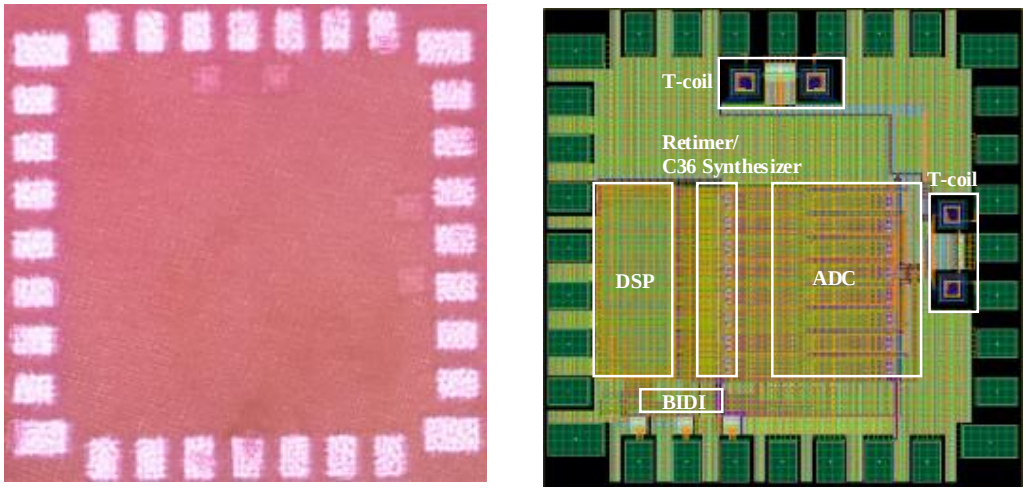


Figure 4.14 – Die photo of the DMT RX chip (left) and the top-level layout view (right).

such a way that no clipping on both TX/RX sides occurs, with DAC output differential dynamic range being $1V$ ($0.5V$ single-ended dynamic range centered at $V_{CM} = 0.5V$).

Although the ADC's designed number of bits is 10b, DSP discards the last two LSBs. Since ADC effective number of bits (ENOB) is not expected to exceed 8 bits at such high sampling rate and input frequency up to around 10 GHz, this does not bring significant practical SNDR degradation but reduces DSP area and power consumption. The pipeline inter-stage gain in each sub-ADC, gain mismatch among sub-ADCs and their offset are calibrated off-chip while leaving other mismatches such as bandwidth mismatch and interleaving skew mismatch are left uncalibrated. In Fig. 4.16(a) and Fig. 4.16(b), measured spectra of 10-bit ADC output with near-DC input frequency and highest DMT carrier input frequency with $f_s = 24$ GS/s are presented, respectively, with 18432-point DFT.

It can be seen that the limited calibration capability of the fabricated DSP limits the ADC performance. Measured SNDR/SFDR plot of 10-bit output from near-DC to near-Nyquist frequency is shown in Fig. 4.16(c). The same measurement is performed to characterize the 8-bit output spectra through DSP scope-mode. Since the ENOB of 10-bit output is below 7, it can be observed from Fig. 4.17(a)-Fig. 4.17(c) that the SNDR and SFDR do not differ noticeably from those of 10-bit output.

Fig. 4.18(a) shows the measured full constellation diagram with 15 sub-channels where 6 bits are allocated to each sub-channel (64-QAM), and Fig. 4.18(b) shows the scan of local constellation points, for CH-C shown in Fig. 4.15(e)-(f) with 56 Gb/s data-rate. The loss at the highest sub-channel carrier frequency is -20 dB at 10.5 GHz that corresponds to the highest sub-channel carrier frequency, and the loss of CH-C at 14 GHz (Nyquist frequency of the equivalent PAM-4 system) is measured to be -28 dB. In order to balance the DAC/ADC quantization

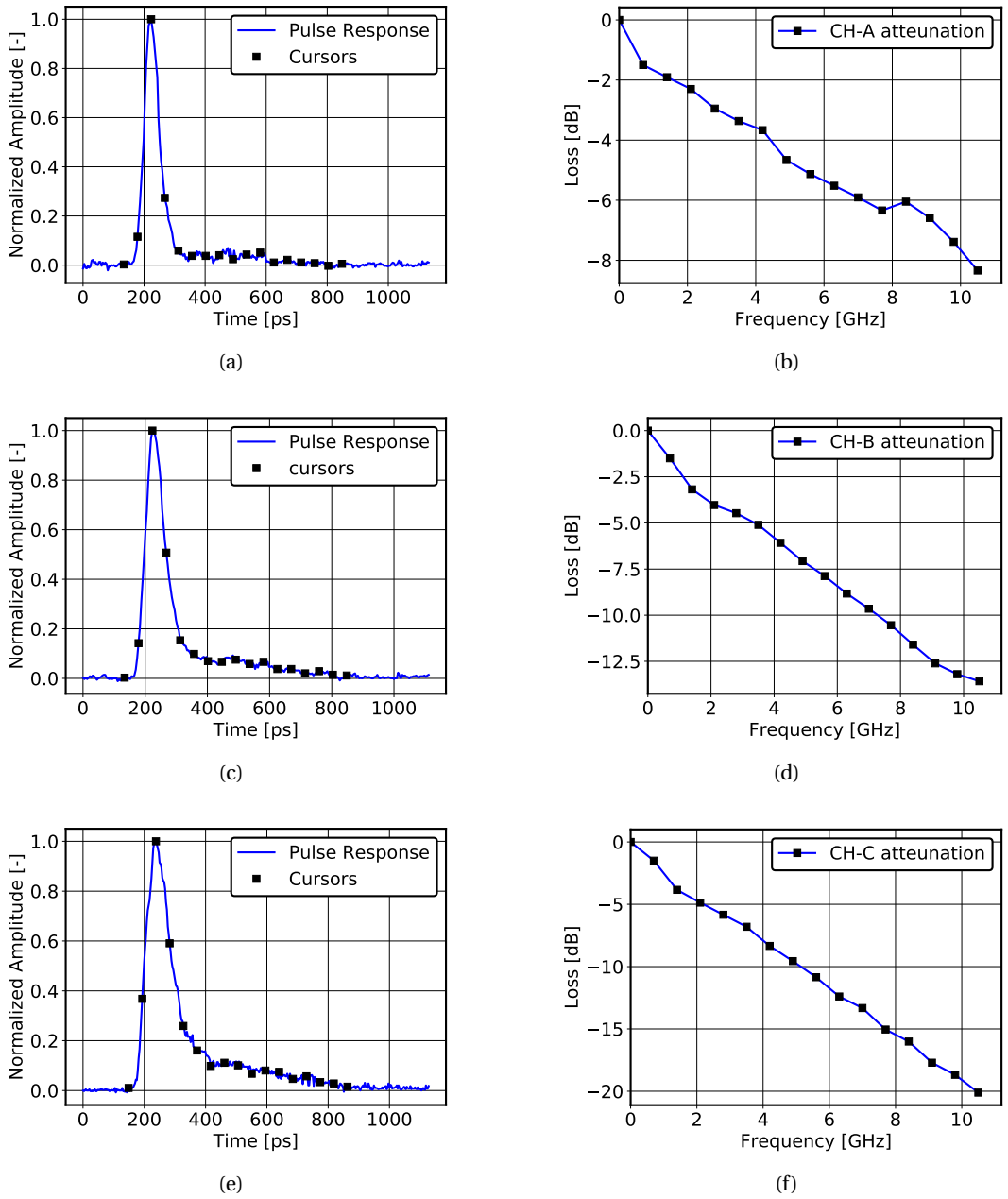
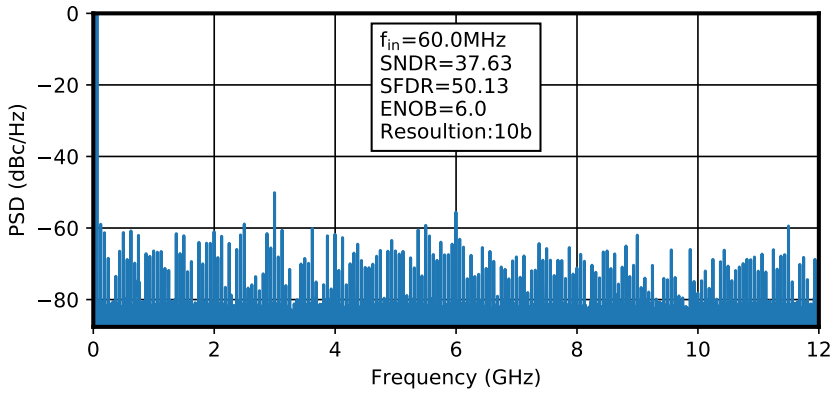
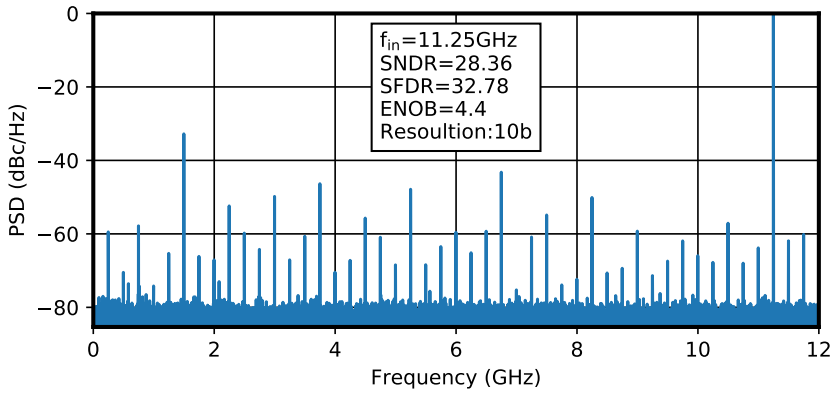


Figure 4.15 – Channel characteristics: (a), (c), (e): pulse responses of channel-A,-B,-C, respectively, and (b), (d), (f): attenuation level at discrete frequencies of channel-A,-B,-C, respectively.

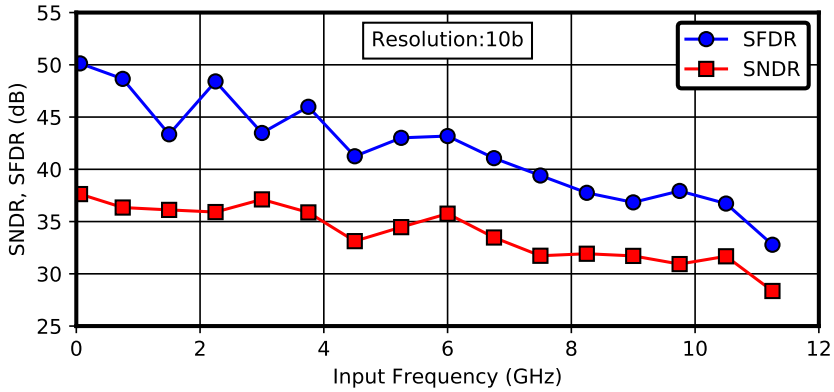
noise over the entire frequency range, exponentially-decreasing power allocation has been considered from the first to the last sub-channels on top of the Python-emulated TX digital FIR filter which shortens the channel pulse response with high-frequency peaking characteristics. If lower-frequency sub-channels' power is not boosted with respect to the FIR-filtered higher-frequency sub-channels, the information contained in weak lower-frequency sub-channels



(a)

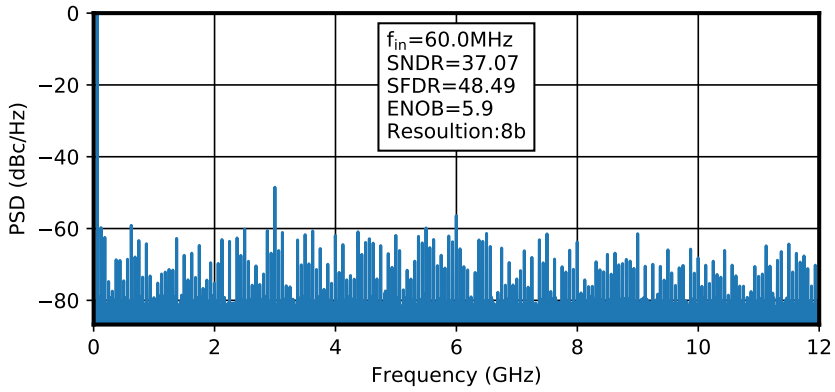


(b)

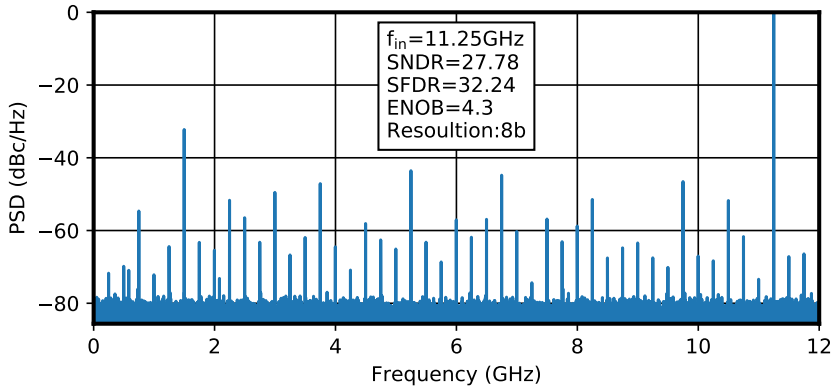


(c)

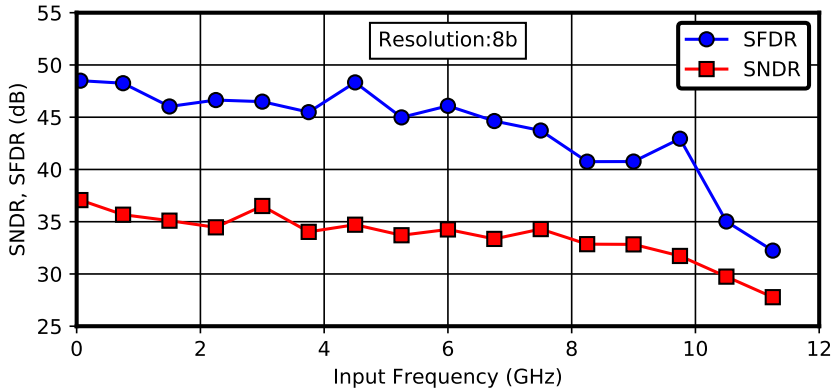
Figure 4.16 – Measured spectra of 10-bit output with 0.06 GHz input frequency (a) and 11.25 GHz input frequency (b), and SNDR/spurious-free dynamic range (SFDR) from near-DC to near-Nyquist frequency.



(a)

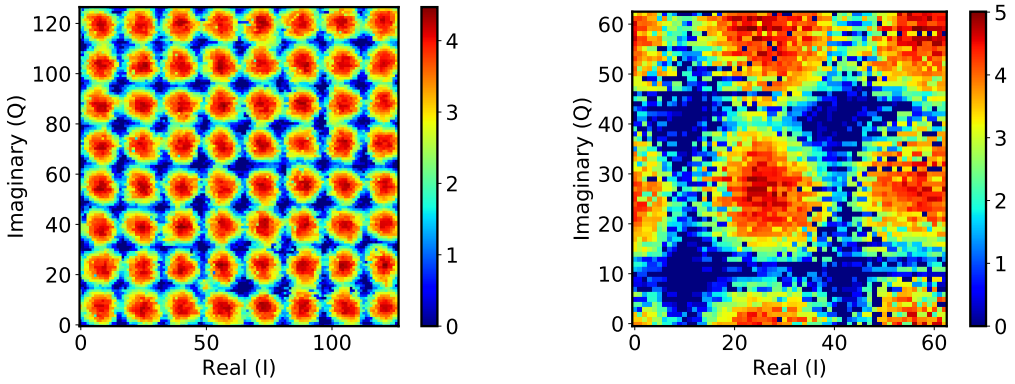


(b)



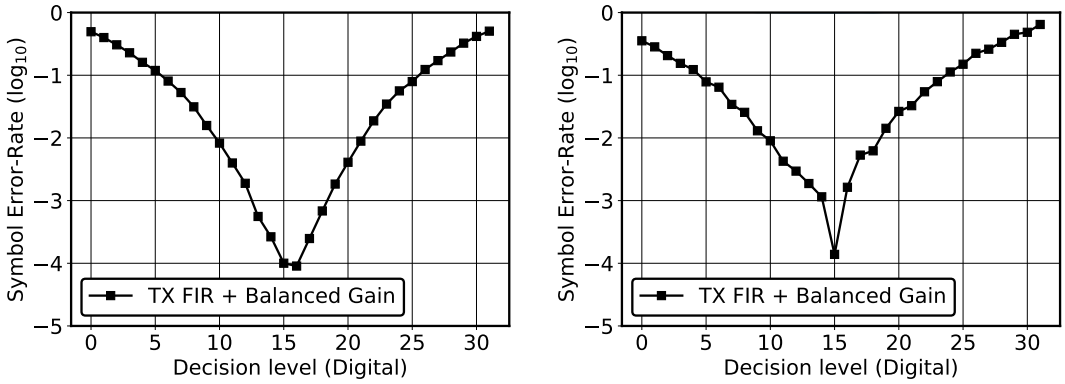
(c)

Figure 4.17 – Measured spectra of 8-bit output with 2-LSB rejection with 0.06 GHz input frequency (a) and 11.25 GHz input frequency (b), and SNDR/SFDR from near-DC to Nyquist frequency.



(a) (b)

Figure 4.18 – Constellation diagram of all-64-QAM 15-sub-channels 56 Gbps data-rate over CH-C with full-scan (a) and locally focused scan (b).

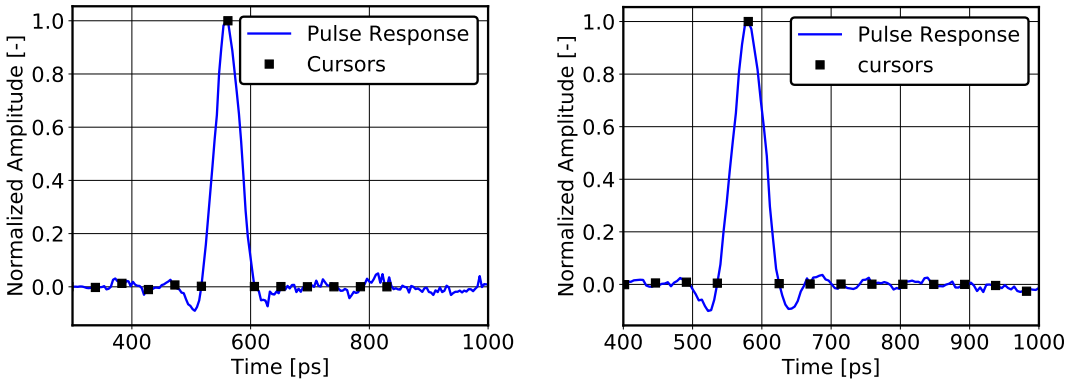


(a) (b)

Figure 4.19 – Bathtub curves of all-64-QAM 15-sub-channels, 56 Gbps data-rate over CH-C with horizontal cross-section (a) and vertical cross-section (b).

are hidden by strong high-frequency components as the digital-domain resolution is limited, introducing severe quantization noise during digital-to-analog conversion. Fig. 4.19(a) and Fig. 4.19(b) show the bathtub curves of the scanned local constellation across I-axis and Q-axis, respectively, with respect to the digital-domain decision threshold. Considering Reed-Solomon FEC coding with 514 data bits and 30 parity bits (KP4-RS10), the measured BER performance with the best decision level satisfies the raw-BER requirement of 3×10^{-4} of FEC-adopted IEEE P802.3bj and P802.3bs standards.

Measurements with CH-A and CH-B with relaxed loss are performed targeting better BER performance for applications with better material quality and/or shorter cables as compared with CH-C. Fig. 4.20(a) and Fig. 4.20(b) show the effective pulse responses of 44.64 ps pulse width with TX channel-inverting FIR filter for CH-A and CH-B, respectively. While TX FIR



(a) (b)

Figure 4.20 – Effective 22.4 GBaud/s pulse response with TX FIR filter, for channel-A (a) and for channel-B (b).

filter helps in channel's phase delay and amplitude loss correction, it does not guarantee clean channel-equalization due to the fact that the lower frequency components experience relative quantization SNR degradation compared with the higher frequency components. Constellation diagrams shown in Fig. 4.21(a) and Fig. 4.21(b) demonstrate the relative SNR penalty of lower frequency components to the overall signal integrity, given the same bit-loading and channel-inversion filter for 56 Gb/s data-rate. When an exponentially-increasing gain of 0.34 dB/sub-channel is applied in order to partially compensate for each sub-channel's amplitude attenuation, the constellations (Fig. 4.21(a) and Fig. 4.21(b)) are sharper than the case without gain balancing (Fig. 4.21(c) and Fig. 4.21(d)). The corresponding TX/RX spectrum with and without gain balancing are shown in Fig. 4.22(a) and Fig. 4.22(b), respectively. The equivalent DAC/ADC-induced relative quantization noise difference between first- and last-sub-channels provides balanced quantization SNR over the entire bandwidth in the case of Fig. 4.22(a) unlike in Fig. 4.22(b), under the condition that the maximum number of bits should be applied in all sub-channels for best bandwidth and power efficiency. The BER versus decision level bathtub curves in both cases are shown in Fig. 4.23. Fig. 4.23(a) and Fig. 4.23(b) demonstrate that the implemented DMT RX can operate at 56 Gb/s with BER $< 10^{-6}$ occupying 11.2 GHz of bandwidth for communicating over a channel exhibiting 13 dB of loss at the highest sub-channel frequency slot (18 dB loss at 14 GHz for PAM-4 equivalent system). A comparison of Fig. 4.23(a)-(b) with Fig. 4.23(c)-(d) concludes that applying the gain balancing results in a better BER performance in quantization noise-limited system.

The constellation diagram of the 64-QAM RX-equalized signal with full-scan and local-scan for 56 Gb/s data-rate over CH-A are shown in Fig. 4.24 with TX FIR filter and gain balancing. The corresponding bathtub curves shown in Fig. 4.25(a) and Fig. 4.25(b) demonstrate DMT RX operation at 56 Gb/s with BER $< 10^{-6}$ for communicating over CH-A exhibiting > 8 dB attenuation at the highest frequency sub-channel (11 dB loss at 14 GHz for PAM-4 equivalent system), while the 56 Gb/s DMT signal occupying only 11.2 GHz of bandwidth.

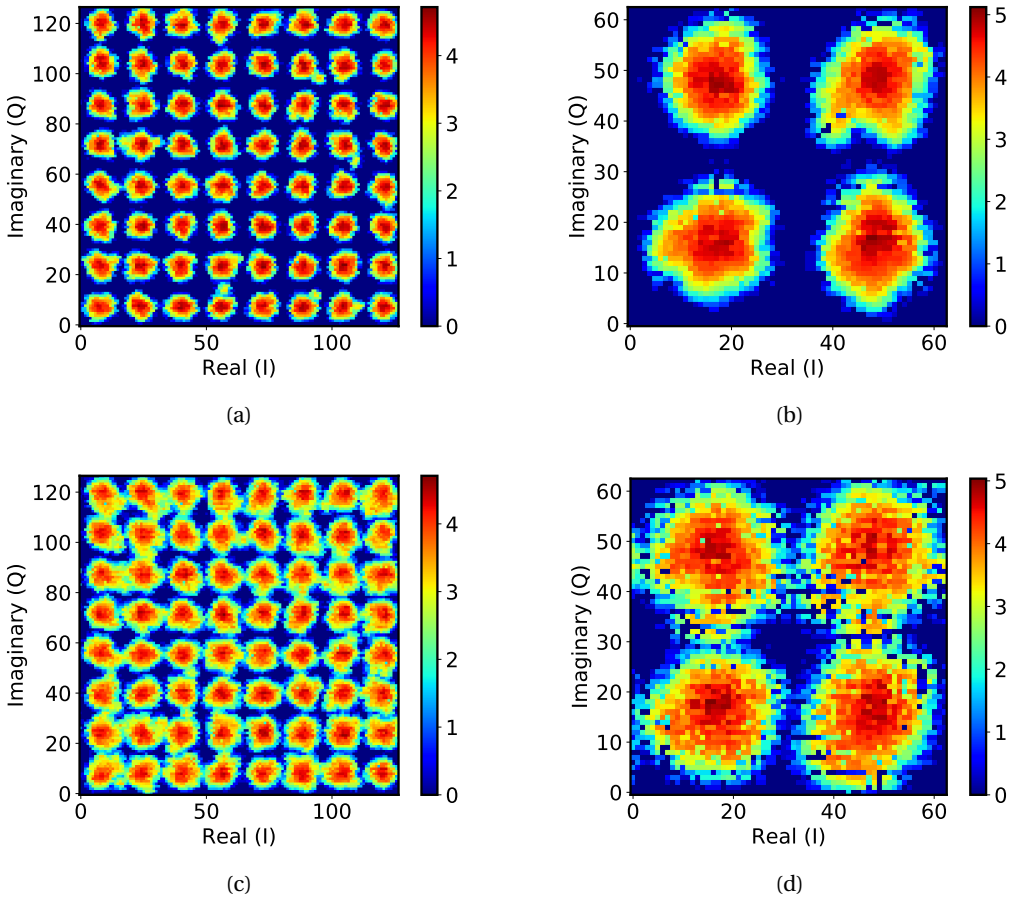


Figure 4.21 – Constellation diagrams of all-64-QAM 15-sub-channels 56 Gbps data-rate over CH-B with full-scan (a) and locally focused scan (b) with exponentially-increasing gain of 0.34 dB/sub-channel from the 1^{st} sub-channel to the 15^{th} sub-channel. The full-scan and locally focused scan without frequency-dependent gain are shown in (c) and (d) respectively. The same FIR filter and channel (CH-B) are applied in both cases.

The system's sensitivity to the sampling phase skew is characterized by measuring BER versus ADC sampling phase. As a first measurement, the BER versus ADC sampling phase curve is obtained with fixed FDE's coefficients. The RX sampling phase (relative to the TX clock phase) is locked to a phase θ_0 in such a way that the ISI of the sampling-rate pulse response is minimized, and the channel is estimated only once for setting FDE coefficients. As expressed in 4.5 where $x[n-D]$ is time-domain sample delayed by D and $X[k]$ is the corresponding N-tap discrete Fourier transform value at k^{th} tap, time-domain delay results in rotation in frequency-domain complex plane.

$$x[n-D] \iff e^{\frac{-j2\pi kD}{N}} X[k] \tag{4.5}$$

Thus, this measurement indicates how much the system can tolerate TX-RX phase skew

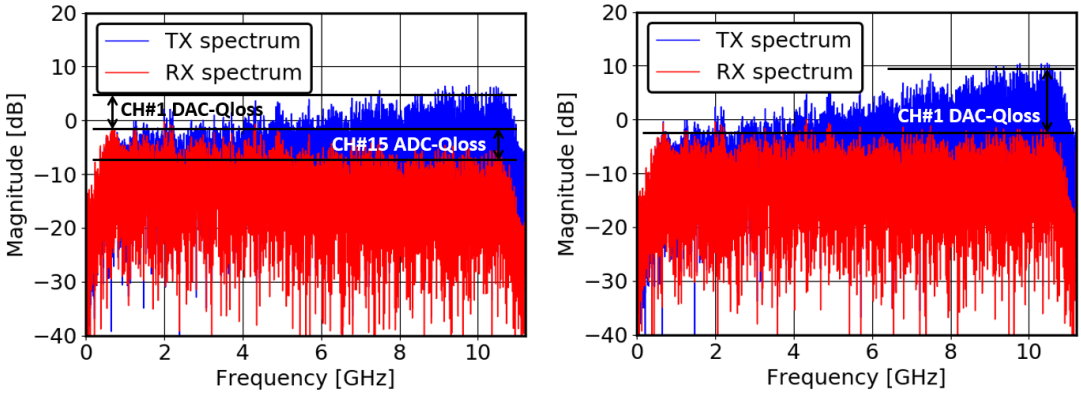


Figure 4.22 – TX (blue) and RX (red) spectrum with (a) and without (b) exponentially-increasing gain of 0.34 dB/sub-channel, where the TX 1^{st} sub-channel power is normalized to RX 1^{st} sub-channel power. Qloss: SNR loss induced by data conversion.

without re-estimating the channel once the channel is estimated at θ_0. Fig. 4.26 shows two BER versus sampling phase curves for two different channels: black markers for CH-A and red markers for CH-B. A data-rate of 58.67 Gb/s (14×64-QAM + 1×16-QAM) could be achieved with BER < 10^{-6} for CH-A with the best ADC sampling phase ($\theta_{0,\mathrm{A}}$) thanks to the relatively relaxed attenuation level providing high SNR as compared with the case with CH-B. For CH-B, 57.33 Gb/s (13×64-QAM + 2×16-QAM) data-rate could be achieved with BER of 10^{-4} at the corresponding phase $\theta_{0,\mathrm{B}}$. In order to satisfy BER < 3×10^{-4} requirement of IEEE P802.3bj and P802.3bs standards with CH-B, the system can tolerate only ±1%-UI of phase skew due to the widely-spread constellations that can cause decision error even with a small rotation angle. By having more concentrated constellations with CH-A, the system can tolerate ±3%-UI of phase skew without channel re-estimation.

On top of the constellation rotation-induced decision errors, drifting away from $\theta_{0,\mathrm{A/B}}$ may increase ISI of which the effect to the constellation integrity has to be identified. In order to address this, another set of measurements is conducted by re-estimating channel coefficients in PC after sampler's phase drift. This test indicates the tolerance of the system against the sampler's phase position assuming continuous channel estimation. The BER curves shown in Fig. 4.27 represent the sensitivity of the system to ISI caused by the sampler phase skew from $\theta_{0,\mathrm{A/B}}$. It can be observed that the BER curves became rather flat over a wide range of sampling phases, as decision errors caused by the constellation rotation has been eliminated thanks to the updated equalization coefficients after phase shift. While BER performance is noticeably worse at some sampling phases as compared with the one at $\theta_{0,\mathrm{A/B}}$, it is sometimes even better than one at $\theta_{0,\mathrm{A/B}}$. This indicates that sampling at phase giving the peak of pulse response does not guarantee the best BER. Hence, potential inclusion of on-chip real-time channel estimation circuitry and the adaptive engine will help to make the DMT RX tolerate better the TX-RX samplers' phase skew and to find the best locking phase.

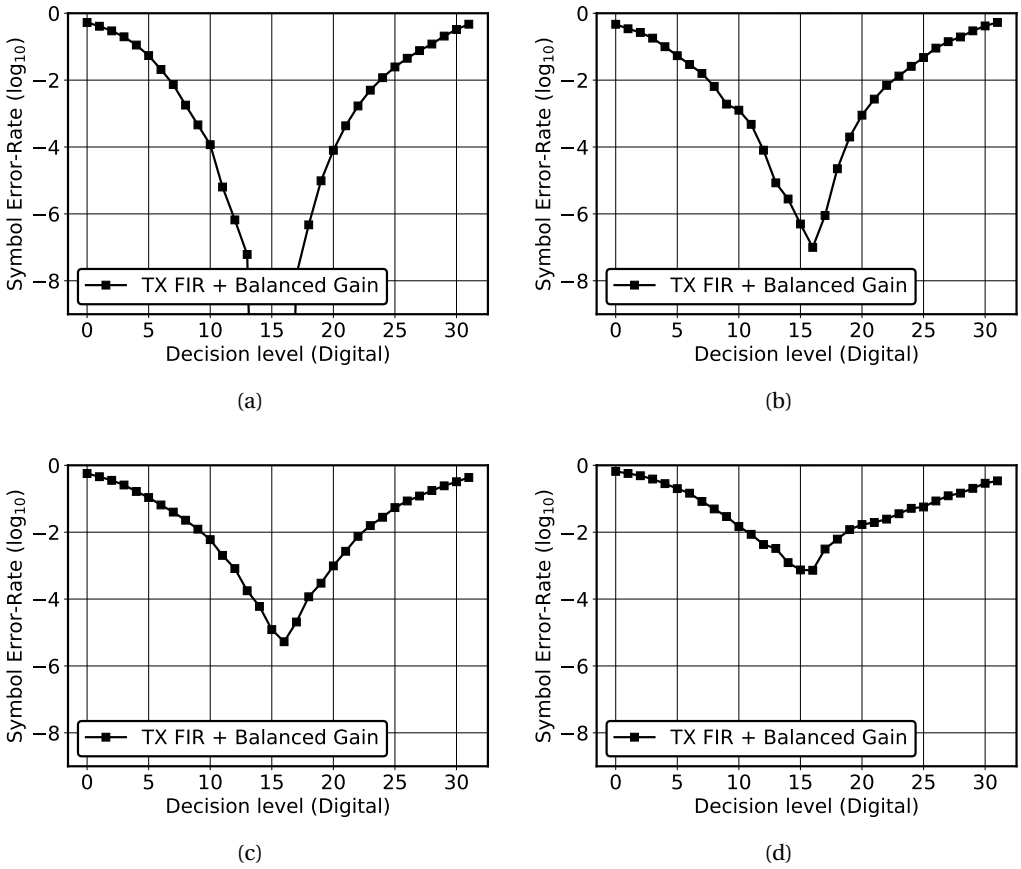
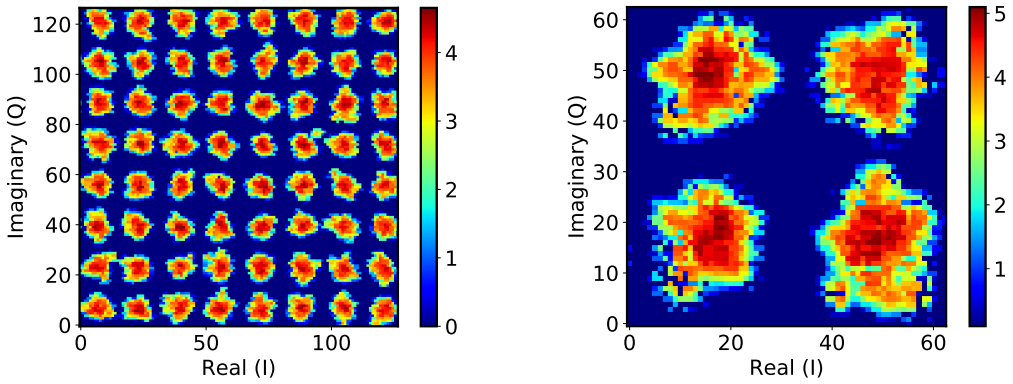


Figure 4.23 – Bathtub curves of all-64-QAM 15-sub-channels 56 Gbps data-rate over CH-B. Horizontal cross-section and vertical cross-section with gain balancing ((a) and (b), respectively) and without gain balancing ((c) and (d), respectively).

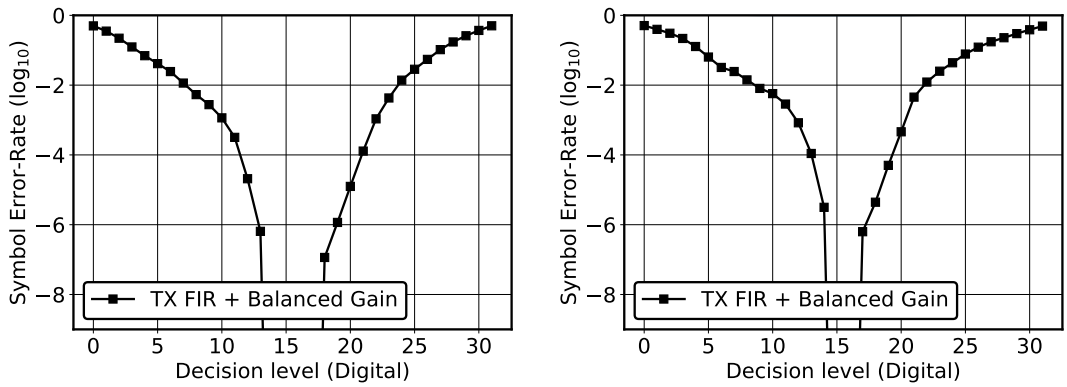
While the lowest measured digital supply is $0.72V$ at 622 MHz DSP core frequency (for 56 Gb/s data-rate) with chip-to-chip variation, nominal $0.75V$ provides reliable operation at 622 MHz core frequency for all 8 measured chips. Under $0.75V$ digital supply, the measured current is 90.96 mA, hence 1.22 pJ/b of energy efficiency in DSP is achieved. Power supplies for clock buffer, TI-ADC interleaver, and ADC are $0.8V$, $0.7V$, and $0.7V$, respectively, drawing 9.31 mA, 16.69 mA and 105.87 mA, respectively. The total RX power consumption is thus 161.46 mW, i.e., 2.88 pJ/b of energy efficiency.

For 57.33 Gb/s and 58.67 Gb/s data-rate, the DSP operates at 667 MHz and all 8 chips operated reliably under $0.8V$ digital supply drawing 108.7 mA of current, which translates into 1.48 pJ/b DSP energy efficiency. The DSP operation under $0.75V$ digital supply at 667 MHz frequency failed with some of the measured chips. All the other supplies for the clock buffer, the interleaver, and the ADC are set to $0.8V$, drawing 9.92 mA, 22.61 mA, and 126.92 mA, respectively. The total RX energy efficiency is 3.74 pJ/b and 3.66 pJ/b for 57.33 Gb/s and 58.67 Gb/s, respectively. Table 4.2 compares this work with other high-speed wireline RXs.



(a) (b)

Figure 4.24 – Constellation diagrams of all-64-QAM 15-sub-channels 56 Gbps data-rate over CH-A with full-scan (a) and locally focused scan (b) with exponentially-increasing gain of 1.03/sub-channel from the 1^{st} sub-channel to the 15^{th} sub-channel.



(a) (b)

Figure 4.25 – Bathtub curves of all-64-QAM 15-sub-channels 56 Gbps data-rate over CH-A: horizontal cross-section (a) and vertical cross-section (b).

4.5 Conclusion

This chapter described wireline TRX communicating with DMT modulation using 8-bit DAC shown in [25] and implemented RX in this work. The DMT TRX achieves 56 Gb/s data-rate over channel with 13 dB loss at 10.5 GHz (18 dB loss at 14 GHz considering PAM-4 equivalent systems), and the RX consumes only 161.46 mW (2.88 pJ/b) at BER <1e-6, which is significantly lower than 3e-4 raw BER requirement of IEEE p802.3bj/bs standards. With a more aggressive channel exhibiting 28 dB loss at 14 GHz, 2e-4 raw BER was achieved at 56 Gb/s data-rate, satisfying IEEE p802.3bj/bs BER requirements. While the DMT RX is implemented with 10-bit ADC, similar data-rate/BER/area performance can be achieved with 7-bit ADC with better power consumption both in ADC and DSP sides since 6 ENOB at DC and 5 ENOB at Nyquist

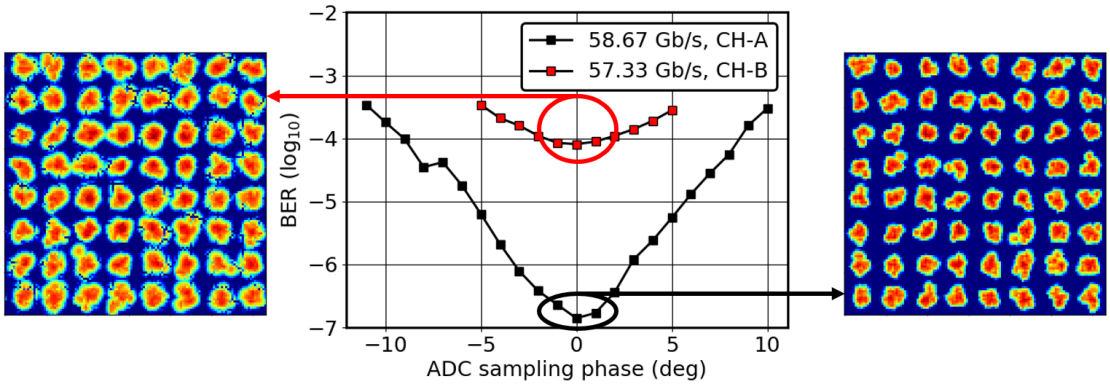


Figure 4.26 – Bathtub curve of 14×64-QAM and 1×16-QAM sub-channels 58.77 Gb/s data-rate over CH-A (black markers. and that of 13×64-QAM and 2×16-QAM sub-channels 57.33 Gb/s data-rate over CH-B (red markers), both with 24 GS/s data conversion rate.

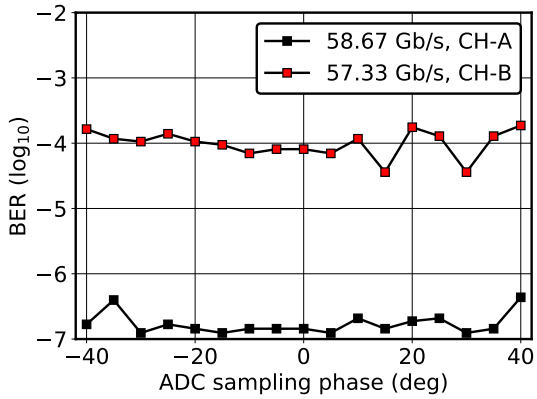


Figure 4.27 – Bathtub curve of 14×64-QAM and 1×16-QAM sub-channels 58.77 Gb/s data-rate over CH-A (black markers. and that of 13×64-QAM and 2×16-QAM sub-channels 57.33 Gb/s data-rate over CH-B (red markers), both with 24 GS/s data conversion rate, with continuous equalization coefficient update.

have been demonstrated to be sufficient for the achieved results. Moreover, the DFT processor can be implemented in more power- and area-efficient thanks to the fact that the input is purely real without any imaginary component. Among the state-of-the-art ADC-based RX with similar communication speed, this work achieves the highest energy efficiency.

Table 4.2 – Comparison with state-of-the-art ADC-based RXs.

	ISSCC18[54]	JSSC2017[52]	ISSCC18[53]	**This work**
Data Rate (Gb/s)	64.375	56	56	**56**
Modulation	PAM-4	PAM-4	PAM-4	**DMT**
Analog EQ	CTLE/VGA	CTLE/VGA	CTLE/VGA	**–**
ADC Res. (bits)	6	8	7	**10/8***
ADC ENOB @ DC	4.9	6.5	N.A.	**5.9**
ADC ENOB at f_{High}**	4.31	4.9	N.A.	**4.3**
f_s (GS/s)	32.1875	28	28	**22.4**
DSP Power (mW)	N.A.	N.A.	220	**68.22**
RX Tot. Power (mW)	283.9***	280***	545	**161.46**
Energy (pJ/b)	4.41***	5***	9.7	**2.88**
Supplies (V)	0.9/1.2	0.9/1.2/1.8	0.85/0.9/1.2/1.8	**0.8/0.7/0.7/0.75**
RX Area (mm^2)	0.1625***	N.A.***	1.76****	**0.26**
Ch. Loss (dB)	29.5	31	32	**CH-A: 11***** **CH-B: 18***** **CH-C: 28*****
Pre-FEC BER	<1e-4	<1e-8	<1e-12	**CH-A: <1e-6** **CH-B: <1e-6** **CH-C: <2e-4**
Technology	16nm FinFET	16nm FinFET	16nm FinFET	**14nm FinFET**

*DSP receives 8 LSBs for equalization out of 10 bits.
** f_{High}=16 GHz in [54], 14 GHz in [52, 53], and 11.25 GHz in this work.
***DSP is not implemented in silicon, hence DSP area and power are not included.
****Estimated from die photo reported in [53].
*****Loss at f_{NYQ} of PAM-4 equivalent system for comparison purpose. Actual losses in DMT system are 8 dB (CH-A), 13 dB (CH-B) and 20 dB (CH-C).

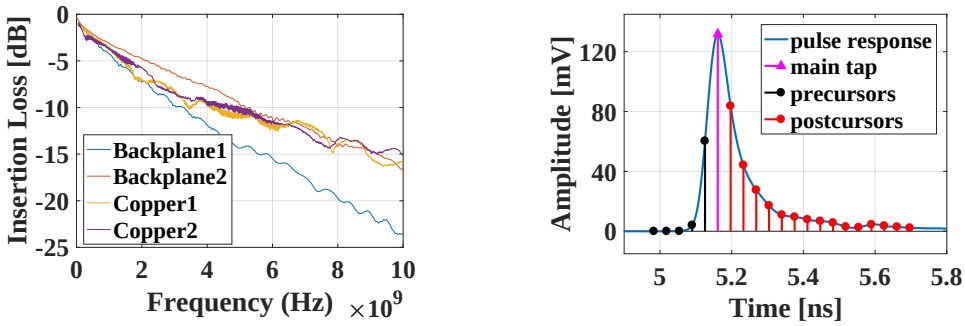
5 ADC-Based Fully-Digital PAM-4 Receiver

[1] A parallel implementation technique of digital equalizer for high-speed wireline serial link RX is presented. In wireline RX, ISI is mitigated by a continuous-time linear equalizer, and the remaining ISI is canceled out by DFE. However, due to the existence of feedback loop in DFE, there is no trivial way to parallelize it, making it difficult to be realized in digital circuits for wireline RX based on ADC with ≥ 56 Gb/s data-rate. In this work, convolution theorem is applied for achieving parallel digital equalizer implementation. The digital equalizer datapath consists of DFT core, IDFT core, complex multipliers between DFT and IDFT cores, and overlap-add circuit. Instead of zero-forcing the ISI postcursors by DFE, a 17-tap FIR filter has been realized in frequency-domain, in order to eliminate the sample-by-sample feedback loop. Taking the purely-real valued nature of the input signal into account, the DSP is designed to be area-efficient. Design considerations for low-area VLSI implementation of such architecture is discussed.

5.1 High-Speed Wireline Receiver Basics (Revisited)

The globally-low-pass nature of the channels (Fig. 5.1(a)) causes a few precursors and long postcursor tail on the pulse response, resulting in strong ISI as shown in Fig. 5.1(b) for 28-Gb/s 500mV amplitude pulse transmitted over Backplane2 example channel. In order to mitigate ISI, wireline RX consists of a set of equalizers. Fig. 5.2 shows a typical point-to-point high-speed wireline RX architecture. The RX mainly consists of a continuous-time linear equalizer (CTLE), DFE and clock recovery (CR) circuits. The CTLE amplifies the received signal and provides a high-frequency peaking, to match the channel characteristics. Thus, the received signal is globally amplified providing more amplitude margin for DFE slicer, and its high-frequency components' power loss is compensated, resulting in reduced pre- and postcursors taps. For some high-loss channels exhibiting strong precursors, linear feed-forward equalizer (LFFE)

[1] The contents of this chapter is based on: G. Kim, L. Kull, D. Luu, M. Braendli, C. Menolfi, P. A. Francese, C. Aprile, T. Morf, M. Kossel, A. Cevrero, I. Ozkaya, T. Toifl, and Y. Leblebici, "Parallel implementation technique of digital equalizer for ultra-high-speed wireline receiver,", *2018 IEEE International Symposium on Circuits and Systems,* pp. 1–5, May 2018 (©IEEE) [84].



(a) (b)

Figure 5.1 – (a) Frequency responses of some real channel examples and (b) a 28-Gb/s 500mV amplitude pulse response of Backplane2 example and its precursor, main and postcursor taps at ideal sampling point.

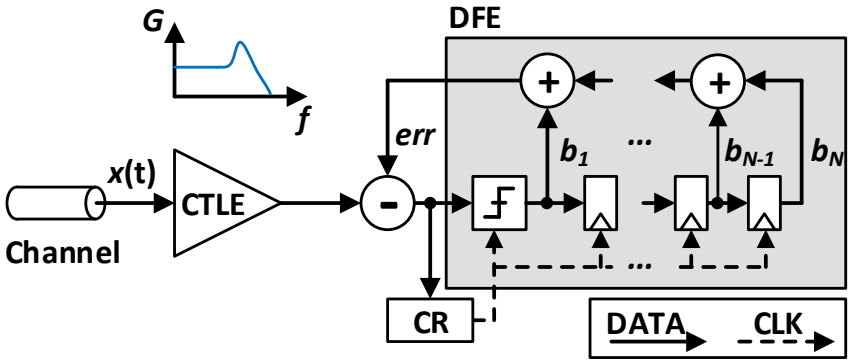


Figure 5.2 – Simplified receiver equalizer architecture consisting of CTLE, DFE and CR.

which is not shown in Fig. 5.2 is adopted for precursor cancellation. When LFFE is used, it follows variable-gain amplifier if CTLE is not present, and its tap weights are optimized to cancel out precursors of the pulse response. The DFE cancels out the remaining postcursors. In order to relax its critical path for closing the feedback loop at high-speed signaling rate, e.g., ≥ 14GBaud/s, loop-unrolling (also called speculation) technique has been adopted. The DFE slicer and delay elements are clocked either by recovered clock from the data or by a forwarded clock. As forwarded-clocking scheme (also called source-synchronous scheme) requires two additional pins for a differential clock, recovering a clock from data is preferred in pad-limited designs.

5.2 Parallel Implementation of Digital Receiver

An ADC-based RX architecture overview is shown in Fig. 5.3. The analog received signal is firstly amplified with channel compensation by CTLE, then discretized by time-interleaved ADC. For high-speed high-resolution sampling, i.e., ≥ 28GS/s with ≥ 8-bit resolution, time-

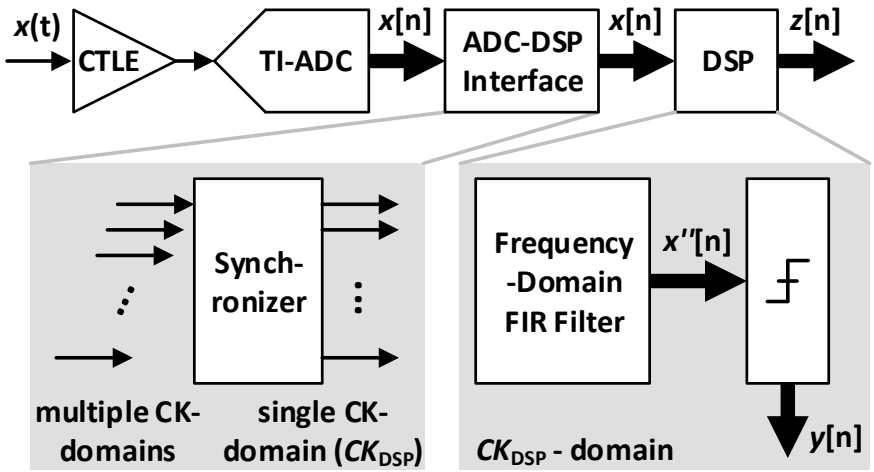


Figure 5.3 – The parallel digital receiver's architecture overview.

interleaved architecture is typically employed in ADC (TI-ADC). Hence, the interleaved output of TI-ADC has to be aligned by a synchronizer so that parallel stream can be processed by DSP operating in a single clock domain, CK_{DSP}. This synchronizing ADC-DSP interface circuit should generally be custom-designed.

5.2.1 Signal Processing for Digital Equalization

The error that is ideally to be subtracted from the current data at ADC sampling instant can be expressed as

$$err[n] = \sum_{i=1}^{N_{PRE}} s_{\mathrm{TX}}[n+i]c_i + \sum_{j=1}^{N_{POST}} s_{\mathrm{TX}}[n-j]b_j$$

where N_{PRE} and N_{POST} are the number of precursors and postcursors to be cancelled out respectively, $s_{\mathrm{TX}}[n+i]$ is the $(n+i)^{\mathrm{th}}$ transmitted symbol (future symbols), $s_{\mathrm{TX}}[n-j]$ is the $(n-j)^{\mathrm{th}}$ transmitted symbol (past symbols), c_i and b_j are the i^{th} precursor and j^{th} postcursor values of the pulse response, respectively. The precursors cannot be eliminated by DFE as there is no decisions from the future symbols. Thus, precursors are typically reduced by channel shortening using TX/RX FFE and/or RX CTLE, and the residual postcursors are eliminated by DFE. However, due to the existence of a sample-by-sample feedback, a direct implementation of decision feedback in a parallel digital circuit is not trivial.

According to signal processing theory, the discrete convolution of an infinite-length sequence $x[n]$ with a FIR filter $g[n]$ of length $L+1$ with finite support in $\{0,1,\cdots,L\}$ where L is non-zero even number, can be evaluated using *overlap-add* method. The sequence $x[n]$ can be broken

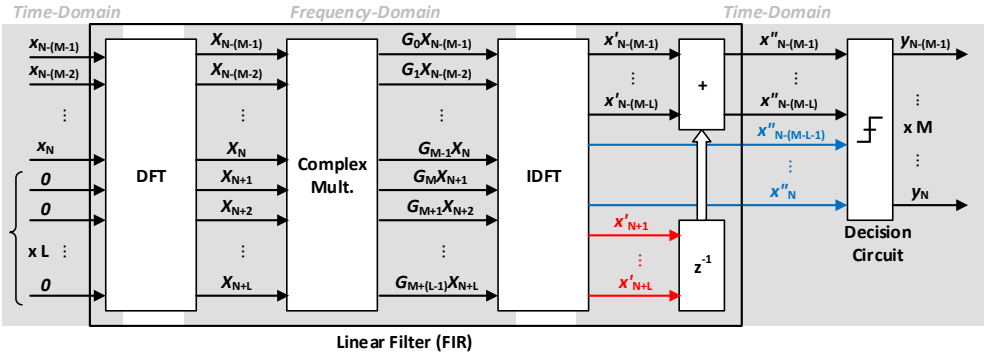


Figure 5.4 – Receiver DSP system overview and data flow.

into smaller blocks of $x_k[n]$ as

$$x_k[n] = x[n - kM] \text{ when } n \in [1, M], \text{ else } 0 \tag{5.1}$$

for any integer k, where M is an arbitrary block-length. Thus, $x[n]$ can be expressed as a sum of $x_k[n]$ as

$$x[n] = \sum_{k=-\infty}^{\infty} x_k[n - kM], \tag{5.2}$$

and the convolution $y[n]$ of $x[n]$ with $g[n]$ can be expressed as

$$x[n] * g[n] = \left(\sum_{k=-\infty}^{\infty} x_k[n - kM] \right) * g[n] \tag{5.3}$$

$$= \sum_{k=-\infty}^{\infty} (x_k[n - kM] * g[n]) \tag{5.4}$$

$$= \sum_{k=-\infty}^{\infty} y_k[n - kM], \tag{5.5}$$

where $y_k[n]$ is the $N = (M + L)$-point circular convolution of $x_k[n]$ with $g[n]$. Since the last L samples of $y_k[n]$ overlaps with the first L samples of $y_{k+1}[n]$, they have to be added, hence *overlap-add*.

5.2.2 DSP Implementation

The DSP architecture is depicted in Fig. 5.4. Noting that N-point circular convolution can be efficiently implemented in frequency-domain by convolution theorem, the DSP consists of a DFT core, a column of complex multipliers for sample-by-sample multiplication, an IDFT core to bring the signal back to time-domain, delay/adder blocks for overlap-add operation, and a decision circuit.

The input of DFT core is a parallel array of M-consecutive received samples concatenated

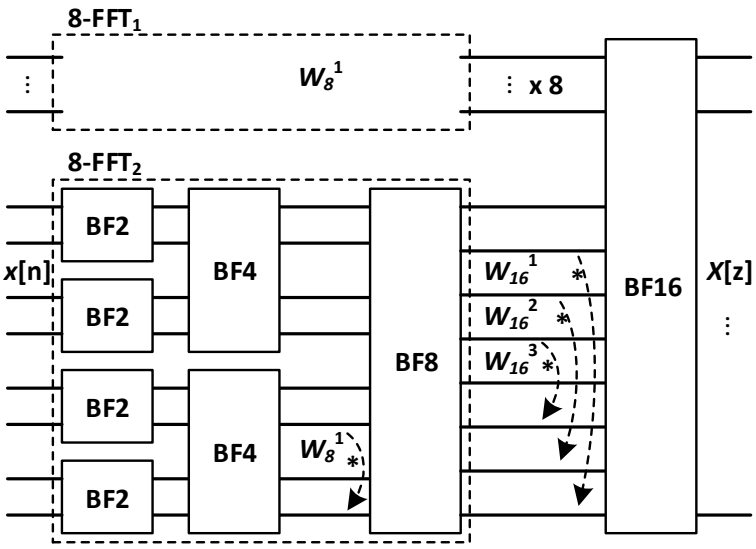


Figure 5.5 – A 16-tap real-input DFT core's outline. The BF2,4,8,16 are butterfly units and $W_8 = e^{-i2\pi/8}$, $W_{16} = e^{-i2\pi/16}$.

with zeros of length-L, forming an input window. This concatenation is called zero-padding, which is needed to translate a cyclic convolution into linear convolution. As the input of DFT is purely real, its DFT is conjugate symmetric, i.e., $X_{\mathrm{k}} = X^*_{\mathrm{N-k}}$ where $k \in \{1, 2, \cdots, N/2-1\}$. Thus, only the first half of DFT output has to be computed, and the other half can be simply rewired and negated from the first half results, saving hardware resources. This applies to sub-DFT entities as well if the top-DFT core is recursively based on multiple smaller DFT cores followed by twiddling factors. An example of 16-tap DFT core realized with FFT algorithm realized in radix-2 butterfly architecture is shown in Fig. 5.5. While not shown in Fig. 5.5, its input has to be ordered as $x[n] = \{0, 8, 4, 12, 2, 10, 6, 14, 1, 9, 5, 13, 3, 11, 7, 15\}$ to keep the output order regular, i.e., $X[z] = \{0, 1, \cdots, 15\}$, and the same ordering manner applies to larger FFTs. In real-input FFT, the number of non-trivial complex multiplications has been reduced by half as compared to that of the complex-input FFT, and the adders/subtractors in the butterfly units related to those complex conjugate paths can be removed as well. For instance, 16-tap real FFT can be implemented with only 5 complex constant multipliers, and 64-tap real FFT with only 49 complex constant multipliers.

The DFT of an input window is then element-wise multiplied by an array of complex numbers. These complex numbers, H_m with $m \in \{N-(M-1), N-(M-2), \cdots, N+L\}$, are a portion of the DFT output of the inverted-channel's pulse response of the transmission line. The H_m can be calculated as follows. Firstly, obtain a P-point discrete-time pulse response $h[n]$, i.e., pulse-response, sampled by Baud-rate ADC at ideal sampling moment, of the channel, where P can be an arbitrarily large positive integer, e.g., ≥ 100 to cover long enough pre-/post cursors. Then, compute the P-point DFT of that response, $H[z]$. Set the target pulse-response of length-P, e.g., an ideal pulse response $h_{ideal}[n] = 0, 0, \cdots, 0, 1, 0, 0, \cdots, 0$ with $\#(h_{ideal}[n]) = P$. Then, the inverted discrete-time pulse response $h_{\mathrm{inv}}[n]$ is IDFT of $H_{ideal}[z]/H[z]$, where $H_{ideal}[z]$ is

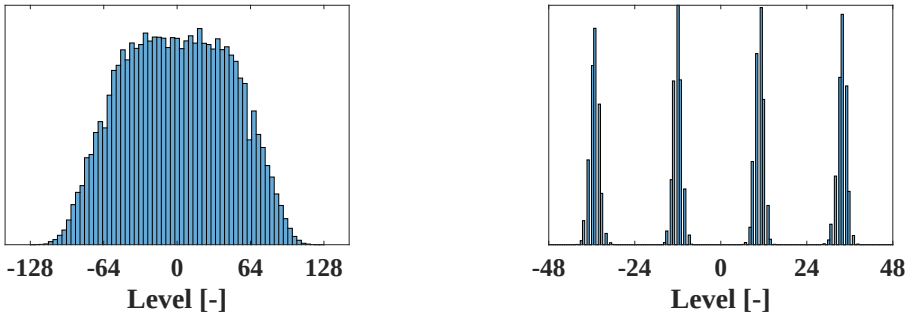


Figure 5.6 – Level histogram of the sampled signal (a) and after equalization (b). The FFT/IFFT twiddling factors are 10-bit-wide and same for the complex multipliers array.

DFT of $h_{ideal}(n)$. The time-domain coefficients $g[n]$ of length-N can be obtained by taking N samples around the amplitude-pick of $h_{\text{inv}}[n]$, and $G[z]$ is DFT of $g[n]$.

It is worth noting that $G[z]$ has same property of complex conjugate like $X[z]$, since $G[z]$ is element-wise division of $H_{ideal}[z]$ by $H[z]$ of which IDFT are purely real. And as $(z^*)(w^*) = (zw)^*$ is true for any two complex numbers z and w, $N/2+1$ complex multipliers are required instead of N complex multipliers. Hence, only the $N/2+1$ outputs are needed at the last butterfly layer in DFT core for being element-wise multiplied by $G[z]$, then IDFT core converts the frequency-domain signals back into time-domain. The IDFT core can be implemented in a similar way as DFT core, taking advantage of the fact that the IDFT output, x' is purely real, which is inverse of the case of DFT. The resulting implementation complexity, i.e., resource usage of IDFT is equivalent to that of DFT. Then, the last L elements of x' are delayed by one clock cycle and are added to the first L elements of the x' of the following clock cycle, finalizing the filtering. The resulting signals are then compared with references by decision circuit for symbol decision.

5.3 Simulation and Implementation

To examine the feasibility of the proposed digital equalizer, a simulation has been performed with emulated TX and ADC in MATLAB, and with RX hardware model implemented in VHDL. The channel used in this experiment exhibits 25dB loss at 14GHz with smooth lowpass nature, and the data-rate is set to 56-Gb/s with PAM-4 encoding. As non-idealities, the transmit driver has 16GHz -3dB bandwidth, the 28GS/s ADC has 38dB SNDR (6 ENOB) over the entire bandwidth. The TX is assumed to include a 4-tap FIR filter for high-frequency amplification to partially compensate for the channel loss. The CTLE with high-frequency peaking on the RX front-end has not been considered, but variable gain amplifier (VGA) with constant gain over the entire bandwidth has been taken into account to restore the peak-to-peak differential voltage level ($V_{\text{pp,diff}}$) of the received signal to ADC full-scale. A 48-way time-

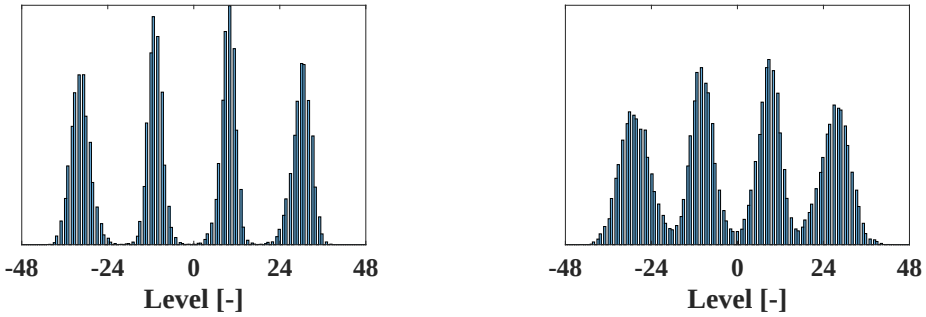


Figure 5.7 – Level histogram of the equalized signals with different DSP multipliers' width. (a) is with 6-bit-wide multipliers and (b) is with 5-bit-wide multipliers. Symbol error-rate order is 10^{-4} and 10^{-2} respectively.

interleaved architecture ($M = 48$) is considered for the ADC which allows the RX to include a filter of length 17 ($L = 16$), using 64-tap architectures for DFT and IDFT for efficient hardware implementation. The DSP clock rate is set to 583MHz (28GS/s sampling rate divided by 48-interleaved) in behavioral simulation, and it is assumed that the ADC-DSP interface circuit exists. The DSP input bit-width is 8-bit (with 38dB SNDR) and the bit-width grows by one every radix-2 stage in the DFT core, thus DFT core output is 14-bit-wide. The IDFT core has the inverse bit-width grows, i.e., decreases by one every radix-2 stage from its input to the output.

Fig. 5.6(a) shows the signal level distribution histogram at the ADC output, and Fig. 5.6(b) shows that of the equalized signal, when all the multipliers in DSP have 10-bit-wide coefficient (both for complex multiplier column and FFT/IFFT twiddling factors). No symbol error occurred for a simulation of 10^6 symbol stream, with a large margin between ideal symbol levels. In Fig. 5.7, equalized histograms with two different multipliers' bit-widths are shown: Fig. 5.7(a) with 6-bit-wide multipliers and Fig. 5.7(b) with 5-bit-wide multipliers. As the multipliers' bit-width affect the DSP's computation round-off errors, the equalized symbols' error-rate strongly depends on the resolution of DSP computation units.

The DSP for digital RX datapath is implemented in 28nm FDSOI process technology libraries. The architectural design is described in VHDL, synthesized by Synopsis Design Compiler, and the physical design is done with Cadence Encounter. Fig. 5.8 shows the resulting layout, where I/O pins' locations are arbitrarily chosen. The cell density is near 81% while the total area is 0.112 mm^2. The target operation speed was set to 667MHz with nearly 15% of margin from 583MHz actual target clocking rate. The post-layout RC-extracted power estimation under ss-corner, $V_{\mathrm{DD}} = 0.81$V, $T = 125$C with primary input activity of 0.5 reports 424.5 mW of total power consumption. This indicates that the energy efficiency of the implemented design is 6.63 pJ/b for 56-Gb/s data-rate.

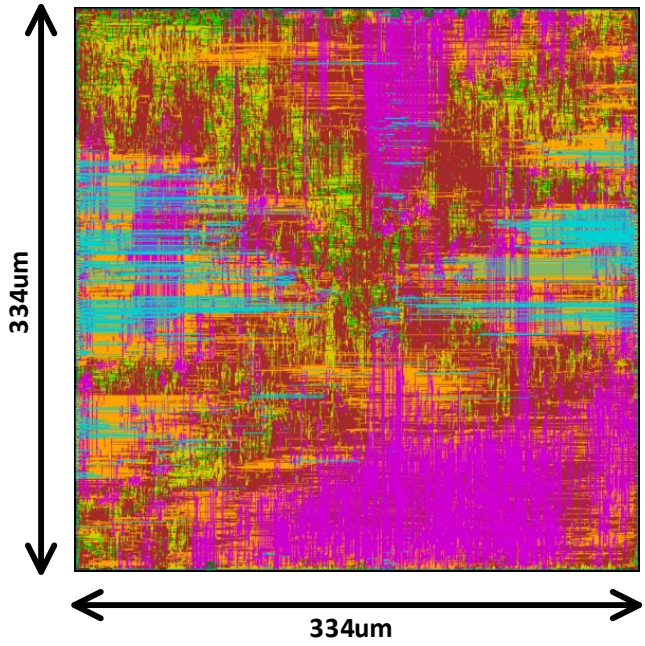


Figure 5.8 – The layout of the DSP. The I/O pins are placed arbitrarily.

5.4 Conclusion

A synthesizable digital implementation of high-speed wireline RX datapath is presented. The RX datapath realizes equalization of time-domain signal in frequency-domain using dedicated DFT/IDFT processor cores, a set of complex multipliers, and an overlap-add circuit. While the implemented circuit shows its capability of error-free equalization of 25 dB insertion loss at Nyquist for PAM-4 signal based on 6-ENOB Baud-rate ADC, it is shown that the equalization capability strongly depends on the fixed-point width of the arithmetic operators. The DSP layout is implemented using 28nm FDSOI process technology libraries, and the post-layout simulation results indicate that the DSP consumes 6.63 pJ/b for 56-Gb/s data-rate while occupying 0.112 mm^2 with 81% cell density.

6 Conclusion

6.1 Achievements

This thesis investigated simple signaling scheme for efficient communication over highly-reflective electrical interfaces, analog and discrete multi-carrier signaling for lossy electrical interfaces, and architectural study and its implementation of a fully-digital ADC-based receiver.

More specifically, digital-style spectrum shaping signaling scheme based on time-division multiplexing targeting multi-drop interfaces was proposed in Chapter 2. The proposed signaling technique achieved 5 Gb/s and 4.8 Gb/s data-rates in simulation for two different example MDBs respectively without any particular equalization, where conventional NRZ signaling exhibited completely closed eye diagram without equalization, or could barely open the eye with extensive equalization at the same data-rate. On top of simulations, supplementary measurement results showed that the proposed scheme could achieve 3.6 Gb/s data-rate while 2.4 Gb/s data-rate was maximum achievable speed without extensive equalization with NRZ signaling.

Targeting lossy point-to-point link, AMT signaling scheme with single-sideband RF sub-bands was proposed in Chapter 3. The SSB-AMT signal exhibits per-sub-channel self-equalization during up/down-conversions and filtering, thereby eliminating the necessity of power-hungry equalizers such as FFE/DFE. A theoretical study has been conducted focusing on the self-equalization mechanism, and the proposed signaling scheme was examined through architectural modeling. Using general-purpose oversampling DAC/ADC, the proposed signaling scheme was tested by measurements using baseband, one RF PAM-4 sub-channel, and two RF NRZ sub-channels with SSB RF sub-bands. Measurement results showed that the proposed scheme could self-equalize up to 25 dB loss at the highest sub-channel carrier frequency demonstrating open eye diagrams for all sub-channels.

Chapter 4 presented DMT RX implementation in 14 nm FinFET process targeting point-to-point mid-to-long-reach electrical links. Measurement of full TRX system using 8-bit DAC

and the implemented RX demonstrated 56 Gb/s data-rate for channels with up to 28 dB attenuation at 14 GHz for less than 3 pJ/b RX energy consumption without the presence of any analog equalizer, satisfying IEEE p802.3bj/bs raw-BER requirements with 0.26 mm^2 of area-occupancy including ADC and DSP. The implemented RX is the fastest DMT RX implemented in FinFET process with digital-only equalization for lossy electrical links. Moreover, the implemented DMT RX exhibits the best energy-efficiency among state-of-the-art ADC-based serial links with similar data-rate.

A fully-digital ADC-based PAM-4 RX with frequency-domain equalization was proposed in Chapter 5. By moving time-domain convolution and symbol-by-symbol equalization into frequency-domain sample-wise parallel multiplication with sub-ADC clock-rate feedback, it enables synthesizable fully-digital RX design without stringent timing constraints. To the best of the author's knowledge, the proposed RX is the first effort to move time-domain digital equalization into frequency-domain for relaxing feedback timing constraint in high-speed wireline serial link. The data-path is designed and laid-out in 28 nm FDSOI process, occupying 0.112 mm^2 with a cell density of 81% and target core frequency of 667 MHz with 15% of margin for 56 Gb/s data-rate at 583 MHz DSP clock rate. The post-layout estimated power consumption is 424.5 mW that corresponds to 6.63 pJ/b energy-efficiency.

6.2 Future Works

Since the scope of this thesis focuses on signaling scheme and data-path architectures, CDR algorithm and its architecture were not considered. To meet potential real-world applications with various proposed signaling schemes and implemented ADC-based RX circuits, proposing appropriate CDR architecture would be essential. For ADC-based RX investigated in this thesis, i.e., DMT RX and PAM-4 RX with frequency-domain equalization, studies about more customized ADC architectures would be valuable. The implemented DMT RX features some lack of optimization in its data-path arithmetic circuits although the measured results show excellent energy efficiency. Addressing such optimization for next-version tape-out would result in more power- and area-efficient RX architecture. Except for DMT RX, other proposed TXs/RXs are either simulated or measured using general-purpose DAC and/or ADC. Thus, silicon implementations and their measurements would be interesting for a better understanding of the benefits of the proposed schemes and their limitations. Also, ADC-based RX implementation with CTLE/VGA front-end targeting 112/224 Gb/s/lane system would be valuable. Multi-lane implementation of ADC-based links with crosstalk cancellation scheme as done in wireless MIMO systems including PLL/CDR would feature full-RX system implementation.

Bibliography

[1] V. N. I. Cisco, "Global mobile data traffic forecast update, 2016–2021 white paper," *Document ID*, vol. 1454457600805266, 2016.

[2] A. Ericsson, "Ericsson mobility report: on the pulse of the networked society," *Ericsson, Sweden, Tech. Rep. EAB-14*, vol. 61078, 2015.

[3] H. Zhang, B. Jiao, Y. Liao, and G. Zhang, "PAM4 signaling for 56G serial link applications—A tutorial," *DesignConn*, 2016.

[4] Qualcomm, "Qualcomm snapdragon 845," *https://www.notebookcheck.net/Qualcomm-Snapdragon-845-SoC-Benchmarks-and-Specs.299446.0.html*.

[5] Intel, "Intel stratix family," *https://www.altera.com/products/fpga/stratix-series.html*.

[6] Xilinx, "Xilinx ultrascale+ family," *https://www.xilinx.com/about/generation-ahead-16nm.html*.

[7] Intel, "Intel 22nm FinFET technology," *https://www.intel.com/content/www/us/en/silicon-innovations/intel-22nm-technology.html*.

[8] ——, "Intel 14nm FinFET technology," *https://www.intel.com/content/www/us/en/silicon-innovations/intel-14nm-technology.html*.

[9] Nvidia, "Nvidia pascal architecture," *https://www.nvidia.com/en-us/data-center/pascal-gpu-architecture/*.

[10] L. Kull, J. Pliva, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Brändli, M. Kossel, T. Morf, T. M. Andersen *et al.*, "Implementation of low-power 6–8 b 30–90 GS/s time-interleaved ADCs with optimized input bandwidth in 32 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 636–648, 2016.

[11] L. Kull, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, "A 90GS/s 8b 667mW 64× interleaved SAR ADC in 32nm digital SOI CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*. IEEE, 2014, pp. 378–379.

[12] L. Kull, D. Luu, C. Menolfi, M. Braendli, P. A. Francese, T. Morf, M. Kossel, A. Cevrero, I. Ozkaya, and T. Toifl, "A 24-to-72GS/s 8b time-interleaved SAR ADC with 2.0-to-3.3 pJ/conversion and> 30dB SNDR at Nyquist in 14nm CMOS FinFET," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 358–360.

[13] B. Xu, Y. Zhou, and Y. Chiu, "A 23-mW 24-GS/s 6-bit voltage-time hybrid time-interleaved ADC in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1091–1100, 2017.

[14] W. Bae, G.-S. Jeong, and D.-K. Jeong, "A fully integrated 1-pJ/bit 10-Gb/s/Ch forwarded-clock transmitter with a resistive feedback inverter based driver in 65-nm CMOS," in *Circuits and Systems (ISCAS), 2016 IEEE International Symposium on*. IEEE, 2016, pp. 2906–2906.

[15] T. Yazaki, N. Chujo, H. Yamashita, T. Takemoto, Y. Lee, and Y. Matsuoka, "25-Gbps x 4 optical transmitter with adjustable asymmetric pre-emphasis in 65-nm CMOS," in *Circuits and Systems (ISCAS), 2014 IEEE International Symposium on*. IEEE, 2014, pp. 2692–2695.

[16] S. Saeedi and A. Emami, "A 10Gb/s, 342fJ/bit micro-ring modulator transmitter with switched-capacitor pre-emphasis and monolithic temperature sensor in 65nm CMOS," in *VLSI Circuits (VLSI-Circuits), 2016 IEEE Symposium on*. IEEE, 2016, pp. 1–2.

[17] S.-G. Kim, T. Kim, D.-H. Kwon, and W.-Y. Choi, "A 5–8 Gb/s low-power transmitter with 2-tap pre-emphasis based on toggling serialization," in *Solid-State Circuits Conference (A-SSCC), 2016 IEEE Asian*. IEEE, 2016, pp. 249–252.

[18] B. Hu, Y. Du, R. Huang, J. Lee, Y.-K. Chen, and M.-C. F. Chang, "A capacitor-DAC-based technique for pre-emphasis-enabled multilevel transmitters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 9, pp. 1012–1016, 2017.

[19] W. Bae, H. Ju, K. Park, and D.-K. Jeong, "A 6-to-32 Gb/s voltage-mode transmitter with scalable supply, voltage swing, and pre-emphasis in 65-nm CMOS," in *Solid-State Circuits Conference (A-SSCC), 2016 IEEE Asian*. IEEE, 2016, pp. 241–244.

[20] K. Huang, Z. Wang, X. Zheng, C. Zhang, and Z. Wang, "A 80 mW 40 Gb/s transmitter with automatic serializing time window search and 2-tap pre-emphasis in 65 nm CMOS technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1441–1450, 2015.

[21] C. Menolfi, T. Toifl, R. Reutemann, M. Ruegg, P. Buchmann, M. Kossel, T. Morf, and M. Schmatz, "A 25Gb/s PAM4 transmitter in 90nm CMOS SOI," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*. IEEE, 2005, pp. 72–73.

[22] M.-S. Chen, Y.-N. Shih, C.-L. Lin, H.-W. Hung, and J. Lee, "A fully-integrated 40-Gb/s transceiver in 65-nm CMOS technology," *IEEE Journal of solid-state circuits*, vol. 47, no. 3, pp. 627–640, 2012.

[23] H. Kimura, P. M. Aziz, T. Jing, A. Sinha, S. P. Kotagiri, R. Narayan, H. Gao, P. Jing, G. Hom, A. Liang *et al.*, "A 28 Gb/s 560 mW multi-standard serdes with single-stage analog front-end and 14-tap decision feedback equalizer in 28 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3091–3103, 2014.

[24] J. Kim, A. Balankutty, R. Dokania, A. Elshazly, H. S. Kim, S. Kundu, S. Weaver, K. Yu, and F. O'Mahony, "A 112Gb/s PAM-4 transmitter with 3-tap FFE in 10nm CMOS," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 102–104.

[25] C. Menoifi, M. Braendli, P. A. Francese, T. Morf, A. Cevrero, M. Kossel, L. Kull, D. Luu, I. Ozkaya, and T. Toifl, "A 112Gb/s 2.6 pJ/b 8-tap FFE PAM-4 "SST TX in 14nm CMOS," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 104–106.

[26] Y.-F. Lin, C.-C. Huang, J.-Y. M. Lee, C.-T. Chang, and S.-I. Liu, "A 5–20 Gb/s power scalable adaptive linear equalizer using edge counting," in *Solid-State Circuits Conference (A-SSCC), 2014 IEEE Asian*. IEEE, 2014, pp. 273–276.

[27] T. O. Dickson, Y. Liu, A. Agrawal, J. F. Bulzacchelli, H. A. Ainspan, Z. Toprak-Deniz, B. D. Parker, M. P. Beakes, M. Meghelli, and D. J. Friedman, "A 1.8 pJ/bit 16x16 Gb/s source-synchronous parallel interface in 32 nm SOI CMOS with receiver redundancy for link recalibration," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1744–1755, 2016.

[28] Z.-H. Hong, Y.-C. Liu, and W.-Z. Chen, "A 3.12 pJ/bit, 19–27 Gbps receiver with 2-tap DFE embedded clock and data recovery," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 11, pp. 2625–2634, 2015.

[29] P. A. Francese, T. Toifl, M. Braendli, C. Menolfi, M. Kossel, T. Morf, L. Kull, T. M. Andersen, H. Yueksel, A. Cevrero *et al.*, "10.6 continuous-time linear equalization with programmable active-peaking transistor arrays in a 14nm FinFET 2mW/Gb/s 16Gb/s 2-tap speculative DFE receiver," in *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*. IEEE, 2015, pp. 1–3.

[30] P. A. Francese, M. Brändli, C. Menolfi, M. Kossel, T. Morf, L. Kull, A. Cevrero, H. Yueksel, I. Oezkaya, D. Luu *et al.*, "23.6 a 30Gb/s 0.8 pJ/b 14nm FinFET receiver data-path," in *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*. IEEE, 2016, pp. 408–409.

[31] Y.-H. Kim, Y.-J. Kim, T. Lee, and L.-S. Kim, "A 21-gbit/s 1.63-pJ/bit adaptive CTLE and one-tap DFE with single loop spectrum balancing method," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 2, pp. 789–793, 2016.

[32] J. W. Jung and B. Razavi, "A 25 Gb/s 5.8 mW CMOS equalizer," *IEEE Journal of solid-state circuits*, vol. 50, no. 2, pp. 515–526, 2015.

[33] H. Yueksel, L. Kull, A. Burg, M. Braendli, P. Buchmann, P. A. Francese, C. Menolfi, M. Kossel, T. Morf, T. M. Andersen *et al.*, "A 3.6 pJ/b 56Gb/s 4-PAM receiver with 6-bit TI-SAR ADC and quarter-rate speculative 2-tap DFE in 32 nm CMOS," in *European Solid-State Circuits Conference (ESSCIRC), ESSCIRC 2015-41st*. IEEE, 2015, pp. 148–151.

[34] J. F. Bulzacchelli, C. Menolfi, T. J. Beukema, D. W. Storaska, J. Hertle, D. R. Hanson, P.-H. Hsieh, S. V. Rylov, D. Furrer, D. Gardellini *et al.*, "A 28-Gb/s 4-tap FFE/15-tap DFE serial link transceiver in 32-nm SOI CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3232–3248, 2012.

[35] H.-W. Yang, A. Roshan-Zamir, Y.-H. Song, and S. Palermo, "A low-power dual-mode 20-Gb/s NRZ and 28-Gb/s PAM-4 voltage-mode transmitter," in *Solid-State Circuits Conference (A-SSCC), 2017 IEEE Asian*. IEEE, 2017, pp. 261–264.

[36] M. S. Jalali, M. H. Taghavi, A. Melaren, J. Pham, K. Farzan, D. Diclemente, M. van Ierssel, W. Song, S. Asgaran, C. Holdenried *et al.*, "A 4-lane 1.25-to-28.05 Gb/s multi-standard 6pJ/b 40dB transceiver in 14nm FinFET with independent TX/RX rate support," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 106–108.

[37] R. Navid, E.-H. Chen, M. Hossain, B. Leibowitz, J. Ren, C.-h. A. Chou, B. Daly, M. Aleksić, B. Su, S. Li *et al.*, "A 40 Gb/s serial link transceiver in 28 nm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 814–827, 2015.

[38] H. Miyaoka, F. Terasawa, M. Kudo, H. Kano, A. Matsuda, N. Shirai, S. Kawai, T. Arai, Y. Ide, K. Terashima *et al.*, "A 28-Gb/s 4.5-pJ/bit transceiver with 1-tap decision feedback equalizer in 28-nm CMOS," in *Solid-State Circuits Conference (A-SSCC), 2015 IEEE Asian*. IEEE, 2015, pp. 1–4.

[39] H. Miyaoka, F. Terasawa, M. Kudo, H. Kano, A. Matsuda, N. Shirai, S. Kawai, T. Shibasaki, T. Danjo, Y. Ogata *et al.*, "A 28.3 Gb/s 7.3 pJ/bit 35 dB backplane transceiver with eye sampling phase adaptation in 28 nm CMOS," in *VLSI Circuits (VLSI-Circuits), 2016 IEEE Symposium on*. IEEE, 2016, pp. 1–2.

[40] I. Ozkaya, A. Cevrero, P. A. Francese, C. Menolfi, T. Morf, M. Brändli, D. M. Kuchta, L. Kull, C. W. Baks, J. E. Proesel *et al.*, "A 64-Gb/s 1.4-pJ/b NRZ optical receiver data-path in 14-nm CMOS FinFET," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3458–3473, 2017.

[41] A. Healey and C. Morgan, "A comparison of 25 Gbps NRZ & PAM-4 modulation used in legacy & premium backplane channels." DesignCon, 2012.

[42] L. Tang, W. Gai, L. Shi, X. Xiang, K. Sheng, and A. He, "A 32Gb/s 133mW PAM-4 transceiver with DFE based on adaptive clock phase and threshold voltage in 65nm CMOS," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 114–116.

[43] H. Ju, M.-C. Choi, G.-S. Jeong, W. Bae, and D.-K. Jeong, "A 28 Gb/s 1.6 pJ/b PAM-4 transmitter using fractionally spaced 3-tap FFE and Gm-regulated resistive-feedback

driver," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 12, pp. 1377–1381, 2017.

[44] P.-J. Peng, J.-F. Li, L.-Y. Chen, and J. Lee, "6.1 a 56Gb/s PAM-4/NRZ transceiver in 40nm CMOS," in *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*. IEEE, 2017, pp. 110–111.

[45] T. O. Dickson, H. A. Ainspan, and M. Meghelli, "A 1.8 pJ/b 56Gb/s PAM-4 transmitter with fractionally spaced FFE in 14nm CMOS," in *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*. IEEE, 2017, pp. 118–119.

[46] E. Depaoli, E. Monaco, G. Steffan, M. Mazzini, H. Zhang, W. Audoglio, O. Belotti, A. A. Rossi, G. Albasini, M. Pozzoni *et al.*, "A 4.9 pJ/b 16-to-64Gb/s PAM-4 VSR transceiver in 28nm FDSOI CMOS," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 112–114.

[47] J. Im, D. Freitas, A. B. Roldan, R. Casey, S. Chen, C.-H. A. Chou, T. Cronin, K. Geary, S. McLeod, L. Zhou *et al.*, "A 40-to-56 Gb/s PAM-4 receiver with ten-tap direct decision-feedback equalization in 16-nm FinFET," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3486–3502, 2017.

[48] T. Toifl, P. Buchmann, T. Beukema, M. Beakes, M. Brändli, P. A. Francese, C. Menolfi, M. Kossel, L. Kull, and T. Morf, "A 3.5 pJ/bit 8-tap-feed-forward 8-tap-decision feedback digital equalizer for 16Gb/s I/Os," in *European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014-40th*. IEEE, 2014, pp. 455–458.

[49] S. Rylov, T. Beukema, Z. Toprak-Deniz, T. Toifl, Y. Liu, A. Agrawal, P. Buchmann, A. Rylyakov, M. Beakes, B. Parker *et al.*, "3.1 a 25Gb/s ADC-based serial line receiver in 32nm CMOS SOI," in *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*. IEEE, 2016, pp. 56–57.

[50] B. Raghavan, A. Varzaghani, L. Rao, H. Park, X. Yang, Z. Huang, Y. Chen, R. Kattamuri, C. Wu, B. Zhang *et al.*, "A 125 mW 8.5–11.5 Gb/s serial link transceiver with a dual path 6-bit ADC/5-tap DFE receiver and a 4-tap FFE transmitter in 28 nm CMOS," in *VLSI Circuits (VLSI-Circuits), 2016 IEEE Symposium on*. IEEE, 2016, pp. 1–2.

[51] A. Shafik, E. Z. Tabasy, S. Cai, K. Lee, S. Hoyos, and S. Palermo, "A 10 Gb/s hybrid ADC-based receiver with embedded analog and per-symbol dynamically enabled digital equalization," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 671–685, 2016.

[52] Y. Frans, J. Shin, L. Zhou, P. Upadhyaya, J. Im, V. Kireev, M. Elzeftawi, H. Hedayati, T. Pham, S. Asuncion *et al.*, "A 56-Gb/s PAM4 wireline transceiver using a 32-way time-interleaved SAR ADC in 16-nm FinFET," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1101–1110, 2017.

[53] P. Upadhyaya, C. F. Poon, S. W. Lim, J. Cho, A. Roldan, W. Zhang, J. Namkoong, T. Pham, B. Xu, W. Lin *et al.*, "A fully adaptive 19-to-56Gb/s PAM-4 wireline transceiver with a

configurable ADC in 16nm FinFET," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 108–110.

[54] L. Wang, Y. Fu, M. LaCroix, E. Chong, and A. C. Carusone, "A 64Gb/s PAM-4 transceiver utilizing an adaptive threshold ADC in 16nm FinFET," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 110–112.

[55] B. Jacob, S. Ng, and D. Wang, *Memory systems: cache, DRAM, disk*. Morgan Kaufmann, 2010.

[56] K. Gharibdoust, A. Tajalli, and Y. Leblebici, "Hybrid NRZ/multi-tone serial data transceiver for multi-drop memory interfaces," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3133–3144, 2015.

[57] ——, "A 4x9 Gb/s hybrid NRZ/multi-tone I/O with crosstalk and ISI reduction for dense interconnects," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 4, pp. 992–1002, 2016.

[58] Y. Du, W.-H. Cho, P.-T. Huang, Y. Li, C.-H. Wong, J. Du, Y. Kim, B. Hu, L. Du, C. Liu *et al.*, "A 16-Gb/s 14.7-mW tri-band cognitive serial link transmitter with forwarded clock to enable PAM-16/256-QAM and channel response detection," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1111–1122, 2017.

[59] S. Lee, J. Seo, K. Lim, J. Ko, J.-Y. Sim, H.-J. Park, and B. Kim, "A 7.8 Gb/s/pin 1.96 pJ/b compact single-ended TRX and CDR with phase-difference modulation for highly reflective memory interfaces," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*. IEEE, 2018, pp. 272–274.

[60] G. Kim, K. Gharibdoust, A. Tajalli *et al.*, "A digital spectrum shaping signaling serial-data transceiver with crosstalk and ISI reduction property in multidrop interfaces," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 12, pp. 1126–1130, 2016.

[61] G. Kim, C. Cao, K. Gharibdoust, A. Tajalli, and Y. Leblebici, "A time-division multiplexing signaling scheme for inter-symbol/channel interference reduction in low-power multi-drop memory links," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 12, pp. 1387–1391, 2017.

[62] F. Aryanfar and A. Amirkhany, "A low-cost resonance mitigation technique for multidrop memory interfaces," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 5, pp. 339–342, 2010.

[63] B. Razavi, *Design of integrated circuits for optical communications*. John Wiley & Sons, 2012.

[64] A. Cevrero, C. Aprile, P. A. Francese, U. Bapst, C. Menolfi, M. Braendli, M. Kossel, T. Morf, L. Kull, H. Yueksel *et al.*, "A 5.9 mW/Gb/s 7Gb/s/pin 8-lane single-ended RX with crosstalk cancellation scheme using a XCTLE and 56-tap XDFE in 32nm SOI CMOS," in *VLSI Circuits (VLSI Circuits), 2015 Symposium on*. IEEE, 2015, pp. C228–C229.

[65] M.-t. Hsieh and G. E. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery," *IEEE Circuits and systems magazine*, vol. 8, no. 4, 2008.

[66] C. Li, M. Li, M. Verhelst, A. Bourdoux, M. Ingels, L. Van der Perre, and S. Pollin, "Efficient timing mismatch correction for low-cost digital-mixing transmitter," *IEEE Transactions on Signal Processing*, vol. 63, no. 24, pp. 6553–6564, 2015.

[67] H.-J. Chi, J.-S. Lee, S.-H. Jeon, S.-J. Bae, Y.-S. Sohn, J.-Y. Sim, and H.-J. Park, "A single-loop SS-LMS algorithm with single-ended integrating DFE receiver for multi-drop DRAM interface," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2053–2063, 2011.

[68] W.-H. Shin, Y.-H. Jun, and B.-S. Kong, "A DFE receiver with equalized VREF for multidrop single-ended signaling," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 7, pp. 412–416, 2013.

[69] H.-W. Lim, S.-W. Choi, J.-K. Ahn, W.-K. Min, S.-K. Lee, C.-H. Baek, J.-Y. Lee, G.-C. Hwang, Y.-H. Jun, and B.-S. Kong, "A 5.8-Gb/s adaptive integrating duobinary DFE receiver for multi-drop memory interface," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 6, pp. 1563–1575, 2017.

[70] H.-W. Lim, S.-W. Choi, S.-K. Lee, C.-H. Baek, J.-Y. Lee, G.-C. Hwang, B.-S. Kong, and Y.-H. Jun, "A 5.8 Gb/s adaptive integrating duobinary-based DFE receiver for multi-drop memory interface," in *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*. IEEE, 2015, pp. 1–3.

[71] W.-H. Cho, Y. Li, Y. Kim, P.-T. Huang, Y. Du, S. J. Lee, and M.-C. F. Chang, "A 5.4-mW 4-Gb/s 5-band QPSK transceiver for frequency-division multiplexing memory interface," in *Custom Integrated Circuits Conference (CICC), 2015 IEEE*. IEEE, 2015, pp. 1–4.

[72] G. Kim, T. Barailler, C. Cao, K. Gharibdoust, and Y. Leblebici, "Design and modeling of serial data transceiver architecture by employing multi-tone single-sideband signaling scheme," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 12, pp. 3192–3201, 2017.

[73] G.-S. Byun, Y. Kim, J. Kim, S.-W. Tam, and M.-C. F. Chang, "An energy-efficient and high-speed mobile memory I/O interface using simultaneous bi-directional dual (base+ RF)-band signaling," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 117–130, 2012.

[74] B. Zhang, K. Khanoyan, H. Hatamkhani, H. Tong, K. Hu, S. Fallahi, M. Abdul-Latif, K. Vakilian, I. Fujimori, and A. Brewster, "A 28 Gb/s multistandard serial link transceiver for backplane applications in 28 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3089–3100, 2015.

[75] R. v. Nee and R. Prasad, *OFDM for wireless multimedia communications*. Artech House, Inc., 2000.

[76] J. Heiskala and J. Terry Ph D, *OFDM wireless LANs: A theoretical and practical guide*. Sams, 2001.

[77] J. Armstrong, "OFDM for optical communications," *Journal of lightwave technology*, vol. 27, no. 3, pp. 189–204, 2009.

[78] S. Cai, E. Z. Tabasy, A. Shafik, S. Kiran, S. Hoyos, and S. Palermo, "A 25 GS/s 6b TI two-stage multi-bit search ADC with soft-decision selection algorithm in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2168–2179, 2017.

[79] T.-K. Kao, P. Chen, J.-Y. Tsai, and P.-C. Chiu, "A 16nm FinFet 19/39MHz 78/72dB DR noise-injected aggregated CTSDM ADC for configurable LTE advanced CCA/NCCA application," in *VLSI Circuits (VLSI Circuits), 2015 Symposium on*. IEEE, 2015, pp. C260–C261.

[80] H. Nakane, R. Ujiie, T. Oshima, T. Yamamoto, K. Kimura, Y. Okuda, K. Tsuiji, and T. Matsuura, "A fully integrated SAR ADC using digital correction technique for triple-mode mobile transceiver," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2503–2514, 2014.

[81] Y. Dong, J. Zhao, W. Yang, T. Caldwell, H. Shibata, R. Schreier, Q. Meng, J. Silva, D. Paterson, and J. Gealow, "A 930mW 69dB-DR 465MHz-BW CT 1-2 mash ADC in 28nm CMOS," in *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*. IEEE, 2016, pp. 278–279.

[82] R. E. Blahut, *A collection of Winograd small FFT algorithms*. Cambridge University Press, 2010, p. 435–441.

[83] L. Kull, D. Luu, C. Menolfi, P.-A. Francese, M. Braendli, M. Kossel, A. Cevrero, I. Ozkaya, and T. Toifl, "A 10-bit 20-40 GS/s ADC with 37 dB SNDR at 40 GHz input using first order sampling bandwidth calibration," in *VLSI Circuits (VLSI Circuits), 2018 Symposium on*. IEEE, 2018, pp. C260–C261.

[84] G. Kim, L. Kull, D. Luu, M. Braendli, C. Menolfi, P. A. Francese, C. Aprile, T. Morf, M. Kossel, A. Cevrero *et al.*, "Parallel implementation technique of digital equalizer for ultra-high-speed wireline receiver," in *Circuits and Systems (ISCAS), 2018 IEEE International Symposium on*. IEEE, 2018, pp. 1–5.

List of Acronyms

ADC	Analog-to-Digital Converter
AFE	Analog Front-End
AMT	Analog Multi-Tone
ASIC	Application-Specific Integrated Circuit
ASK	Amplitude-Shift Keying
AWGN	Additive White Gaussian Noise
BB	Baseband
BER	Bit Error Rate
BPF	Band-Pass Filter
CAGR	Compound Annual Growth Rate
CDR	Clock and Data Recovery
CEI	Common Electrical Input/Output
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CTLE	Continuous-Time Linear Equalizer
DAC	Digital-to-Analog Converter
DEMUX	Demultiplexer
DDR SDRAM	Double Data Rate Synchronous Random-Access Memory
DDR4	Fourth Generation DDR SDRAM
DFE	Decision Feedback Equalizer
DFT	Discrete Fourier Transform
DIMM	Dual In-line Memory Module
Dj	Deterministic Jitter
DLL	Delay-Locked Loop
DMT	Discrete Multi-Tone
DR	Data-Rate
DRAM	Dynamic Random Access Memory
DSB	Double-Sideband
DSL	Digital Subscriber Line
DSP	Digital Signal Processing/Processor
EB	Exabyte

ENOB	Effective Number of Bits
ESD	Electrostatic Discharge
FDE	Frequency-Domain Equalizer
FEC	Forward Error-Correction
FEXT	Far-End Crosstalk
FFE	Feed-Forward Equalizer
FFT	Fast Fourier Transform
FinFET	Fin Field-Effect Transistor
FIR	Finite Impulse Response
FPGA	Field-Programmable Gate Arrays
Gb/s	Giga-bit-per-Second
GDDR SDRAM	Graphics Double Data Rate Synchronous Random-Access Memory
GPU	Graphics Processing Unit
GS/s	Giga-Sample-per-Second
HBM	High-Bandwidth Memory
HBM2	2^{nd} Generation HBM
HDL	Hardware Description Language
I/O	Input/Output
I/Q	In-Phase and Quadrature
ICI	Inter-Channel-Interference
IDFT	Inverse Discrete Fourier Transform
IIR	Infinite Impulse Response
IoT	Internet-of-Things
IP	Internet Protocol
ISI	Inter-Symbol Interference
JEDEC	Joint Electron Device Engineering Council
LFFE	Linear Feed-Forward Equalizer
LMS	Least Mean Square
LO	Local Oscillator
LPF	Low-Pass Filter
LSB	Lower-Sideband or Least-Significant Bit
LUT	Look-Up Table
MCM	Multi-Chip Modules
MDB	Multi-Drop Bus
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MR	Mid-Reach
MSB	Most-Significant Bit
MUX	Multiplexer
NRZ	Non-Return to Zero
ODT	On-Die Termination
OFDM	Orthogonal Frequency Division Multiplexing
OIF	Optical Internetworking Forum

PAM	Pulse-Amplitude Modulation
PB	Passband
PC	Personal Computer
PCIe	Peripheral Component Interconnect Express
PDM	Phase-Discrimination Method
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Binary Sequence
QAM	Quadrature-Amplitude Modulation
QPSK	Quadrature Phase-Shift Keing
RF	Radio Frequency
RS	Reed-Solomon
RTL	Register-Transfer-Level
RX	Receiver
SAR	Successive Approximation Register
SER	Symbol-Error Rate
SerDes	Serializer-Deserializer
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	Systems-on-Chip
SSB	Single-Sideband
TDM	Time-Division Multiplexing
TRX	Transceiver
TX	Transmitter
USB	Universal Serial Bus or Upper-Sideband
USR	Ultra-Short-Reach
VSR	Very-Short-Reach
XDFE	Cross Decision-Feedback Equalizer
XFFE	Cross Feed-Forward Equalizer

Gain Kim

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SUMMARY

I have been working on the design of high-speed (e.g., DR > 56 Gb/s) Analog-to-Digital Converter (ADC)-based serial link for wireline transceivers in data center and/or cloud servers, analysis and development of new modulation schemes such as analog multi-tone signaling and spectrum shaping signaling for multi-drop memory interfaces (e.g., DRAM interfaces), behavioural modeling of serial link systems for the sake of quick verification of new modulation and signaling techniques, starting from July 2015. Beside main projects in serial link modeling/design field, I have been working on signal processing for sampled signal reconstruction algorithm as a side project. All in all, my research interests include but are not limited to high-speed interface circuit modeling/design and signal processing.

Main Projects

- "Ultra-High Bandwidth, Low-Power Data Link Circuits in 14nm FinFET"

In collaboration with *IBM Research Zurich Laboratory*.
Directors: Prof. Yusuf Leblebici (*EPFL*), Dr. Thomas Toifl (*IBM Research Zurich Laboratory*)

- "Multi-Carrier Signaling for Multi-Drop Interfaces"

Directors: Prof. Yusuf Leblebici (*EPFL*), Dr. Kiarash Gharibdoust (*Kandou Bus SA*)

- "Behavioural Modeling Framework Development for High-Speed I/O Links"

Director: Prof. Yusuf Leblebici (*EPFL*)

EDUCATION

PhD Candidate (February 2015 – July 2018)
EPFL, Microelectronic Systems Laboratory - Ecublens, Vaud, Switzerland
(Expected) Dissertation: "Multi-Tone Signaling and ADC-Based Digital Receiver for High-Speed Wireline Serial Links"
Director: Prof. Yusuf Leblebici

Master's in Electrical Engineering (September 2013 – January 2015)
EPFL, Integrated Systems Laboratory - Ecublens, Vaud, Switzerland
Research Project: Design of a Novel High Performance and Low Power Multi-Input/Multi-Output Basic Logic Element in FPGA
Directors: Prof. Giovanni De Micheli, Dr. Pierre-Emmanuel Gaillardon
Grade: 5.43/6

Bachelor's in Electrical Engineering (September 2010 – July 2013)
EPFL, Microelectronic Systems Laboratory - Ecublens, Vaud, Switzerland
Grade: 4.86/6

WORK AND RESEARCH EXPERIENCES

Contractor (September 2016 – July 2018)
IBM Research Zurich Laboratory, High-Speed Interconnect Technology Group - Ruschlikon, Switzerland
1. Discrete Multi-Tone (DMT) wireline transceiver (TRX) development in Global Foundries (GF) 14 nm FinFET (LPP) for the data rate > 56 Gb/s.
2. Digital receiver circuit design for PAM-N signaling for data center wireline TRX applications.

Graduate Research Intern (September 2015 – October 2015)
Samsung Electronics, Memory Division, Flash Design Team, I/O Group - Hwasung, Gyeonggi, South Korea Worked on SerDes modeling for stacked NAND FLASH interfaces.

Research Assistant (Master Student) (November 2013 – January 2015)
EPFL, Integrated Systems Laboratory - Ecublens, Vaud, Switzerland
Worked on the Field-Programmable Gate Array (FPGA) architecture, focusing on the enhancement of the basic logic element (BLE) for high-speed and low-power.

Internship (July 2013 – August 2013)
The European Organization for Nuclear Research (*CERN*), PH-SFT Group - Meyrin, Geneva, Switzerland Worked on the next-generation software development project (GeantV) for a particle accelerator and collider simulation.

LIST OF PUBLICATIONS

Journal Articles

- **G. Kim**, C. Cao, K. Gharibdoust, A. Tajalli and Y. Leblebici, **"A Time-Division Multiplexing Signaling Scheme for Inter-Symbol/Channel Interference Reduction in Low-Power Multi-Drop Memory Links,"** *IEEE Transactions on Circuits and Systems - II: Express Briefs (TCAS-II),* vol. 64, no. 12, pp. 1387-1391, December 2017.
- **G. Kim**, T. Barailler, C. Cao, K. Gharibdoust and Y. Leblebici, **"Design and Modeling of Serial Data Transceiver Architecture by Employing Multi-Tone Single-Sideband Signaling Scheme,"** *IEEE Transactions on Circuits and Systems - I: Regular Papers (TCAS-I),* vol. 64, no. 12, pp. 3192-3201, December 2017.
- **G. Kim**, K. Gharibdoust, A. Tajalli and Y. Leblebici, **"A Digital Spectrum Shaping Signaling Serial-Data Transceiver with Crosstalk and ISI Reduction Property in Multi-Drop Interfaces,"** *IEEE Transactions on Circuits and Systems - II: Express Briefs (TCAS-II),* vol. 63, no. 12, pp. 1126-1130, December 2016.
- X. Tang, **G. Kim**, P.-E. Gaillardon and G. De Micheli, **"A Study on the Programming Structures for RRAM-based FPGA Architectures,"** *IEEE Transactions on Circuits and Systems - I: Regular papers (TCAS-I)*, vol. 63, no. 10, pp. 503-516, April 2016.
- P.-E. Gaillardon, X. Tang, **G. Kim** and G. De Micheli, **"A Novel FPGA Architecture based on Ultra-Fine Grain Reconfigurable Logic Cells,"** *IEEE Transactions on Very Large Scale Integration (TVLSI)*, vol. 23, no. 10, pp. 2187-2197, October 2015.

Selected Conference Proceedings

- **G. Kim,** T. Barailler, C. Cao, K. Gharibdoust and Y. Leblebici, **"Design and Modeling of Serial Data Transceiver Architecture by Employing Multi-Tone Single-Sideband Signaling Scheme,"** *IEEE International Symposium on Circuits and Systems (**ISCAS 2018**),* Florence, Italy, May 27-30, 2018. (T-CAS presentation)
- **G. Kim,** L. Kull, D. Luu, M. Braendli, C. Menolfi, P.-A. Francese, C. Aprile, T. Mork, M. Kossel, A. Cevrero, I. Ozkaya, T. Toifl and Y. Leblebici, **"Parallel Implementation Technique of Digital Equalizer for Ultra-High-Speed Wireline Receiver,"** *IEEE International Symposium on Circuits and Systems (**ISCAS 2018**),* Florence, Italy, May 27-30, 2018.
- **G. Kim,** C. Cao, K. Gharibdoust and Y. Leblebici, **"A Time-Domain Multiplexing Signaling Scheme for Low-Power Multi-Drop Memory Links,"** *IEEE International Symposium on Circuits and Systems (**ISCAS 2017**),* Baltimore, MD, USA, 2017. (Late Breaking News)
- **G. Kim** and Y. Leblebici, **"Architectural Modeling of a Multi-Tone/Single-Sideband Serial Link Transceiver for Lossy Wireline Data Links,"** *IEEE 13th Asia Pacific Conference on Circuits and Systems (**APCCAS 2016**),* Jeju Island, Korea, 2016.
- K. Gharibdoust, **G. Kim**, A. Tajalli and Y. Leblebici, **"A Fully-Digital Spectrum Shaping Signaling for Serial-Data Transceiver with Crosstalk and ISI Reduction Property in Multi-Drop Memory Interfaces,"** *IEEE International Symposium on Circuits and Systems (**ISCAS 2016**),* Montreal, Canada, 2016.

AWARDS AND SCHOLARSHIPS

- **2018 Pre-Doctoral Scholarship** by the IEEE Circuits and Systems Society (CASS).
- **Student travel grant** by the IEEE Circuits and Systems Society (CASS) for attending the *13th Conference on PhD Research in Microelectronics and Electronics* (PRIME 2017).

ACADEMIC SERVICES

- Reviewer for conferences: ISCAS (2017, 2018), MWSCAS (2017), GLSVLSI (2017), ICECS (2016), APCCAS (2016)
- Reviewer for journals: TCAS-II, TCAS-I

PROFESSIONAL SKILLS

Tools/languages in daily-basis use are highlighted in bold font.

- **SW/HW Programming Languages**: C, C++, **Matlab**, **Python**, **VHDL**, Verilog
- **CAD tools**: **Modelsim**, **Design Compiler**, **Virtuoso**, **Encounter**
- **Languages**: Korean (native), English (full professional proficiency), French (full professional proficiency)