

# Design Considerations of Ferroelectric Properties for Negative Capacitance MOSFETs

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**Abstract**—Impact of physical parameters of ferroelectric layer on the performance of Negative Capacitance (NC) MOSFETs is experimentally studied in this paper. Electrical behaviors of PZT-based and Si:HfO<sub>2</sub>-based NC-FETs are investigated and discussed. In a PZT-based p-type NC-FET, a sub-thermal swing down to 20mV/dec is achieved due to the remarkable voltage gain of NC, reaching a maximum value of 10V/V. Nevertheless, the performance improvements with Si:HfO<sub>2</sub> NC booster are significantly lower than PZT due to the coexistence of different phases and also high leakage current which can enormously reduce the enhancement by NC.

## I. INTRODUCTION

An average Subthreshold Swing (SS) smaller than thermal limit of MOSFET swing would enable the scaling of supply voltage,  $V_{dd}$ , which results in a reduced power consumption. A sub-thermal swing ( $< \ln(10) \times k_B T/q$ , which is 60mV/dec at room temperature) can be obtained by decreasing the device body factor,  $m=1+C_s/C_{ins}$ , to a value smaller than 1 (where  $C_s$  and  $C_{ins}$  are semiconductor and gate oxide capacitance respectively). This can be achieved by using the recently proposed NC effect of ferroelectric materials to the gate stack of conventional MOSFETs [1]. It has been suggested that a Metal-Ferroelectric-Semiconductor (MFS) can provide a feasible solution to step-up the semiconductor surface potential ( $\psi_s$ ) above the gate voltage ( $V_g$ ) which leads to a reduction of SS [2]. The basic idea is to benefit of NC region of ferroelectric materials. The practical implementation of the NC involves the series combination of a ferroelectric capacitor, operating in the NC region, with a positive capacitor capable of stabilizing the NC [3]. A negative capacitor in the gate stack can make the total capacitance larger than its classical value, decreasing the required  $\Delta V_g$  to provide the same  $\Delta \psi_s$  [4]. One of the main integration constraints of NC with conventional transistors is about the CMOS incompatibility of classical ferroelectrics commonly used in experimental demonstrations of NC.

In this study, first, we have experimentally investigated the impact of a PZT capacitor as a commonly used ferroelectric on DC electrical behavior of commercial MOSFETs, fabricated in 28nm CMOS technology node. The matching condition between the ferroelectric NC and MOS capacitance of the baseline FET is mostly fulfilled, leading to a small hysteresis. A sub-thermal swing down to 20mV/dec is realized as a result of the internal voltage gain of NC, reaching a factor of 10V/V. Additionally, results are compared with the performance of

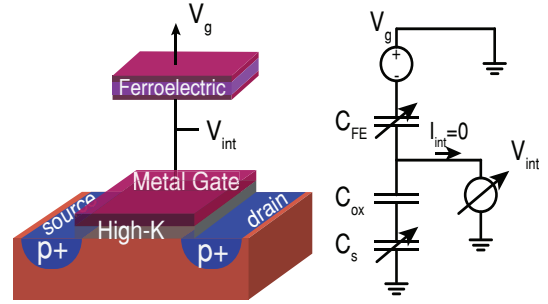


Fig. 1. Experimental configuration of a p-type NC-FET where the gate of a conventional MOSFET is loaded with a ferroelectric capacitor (left) and the measurement setup considering the capacitance model of the structure (right).

an NC-FET using the CMOS compatible ferroelectric, silicon doped HfO<sub>2</sub> [5]. A limited boosting is observed in comparison to the PZT-based NC-FET due to the formation of non-ferroelectric phases in Si:HfO<sub>2</sub> and also its high leakage.

## II. THEORY OF PERFORMANCE BOOSTING IN NC-FETs

The SS of a MOSFET is given by the inverse of change in the current which can be obtained for a unit change in gate voltage,  $V_g$ :

$$SS = \frac{\partial V_g}{\partial (\log I_d)} = \frac{\partial V_g}{\partial \psi_s} \frac{\partial \psi_s}{\partial (\log I_d)}. \quad (1)$$

In a conventional MOSFET, the second term, relating the change of current to the change of surface potential in the channel cannot be any lower than 60mV/dec at room temperature. Nevertheless, the first term which is known as the body factor ( $m$ ), can be reduced with the internal voltage amplification ( $\beta$ ) caused by a negative capacitor in-series with the gate (Fig. 1) [4]:

$$\beta = \frac{\partial V_{int}}{\partial V_g} = \frac{C_{FE}}{C_{FE} + C_{int}}, \quad (2)$$

where  $C_{int}$  is the equivalent capacitance of the base transistor looking into the gate. Accordingly, an NC booster can provide an internal amplification ( $\beta > 1$ ) that lowers the body factor,  $m$ :

$$m = \frac{1}{\beta} \times \frac{\partial V_{int}}{\partial \psi_s} = \frac{1}{\beta} \times \left( 1 + \frac{C_s}{C_{int}} \right) < 1, \quad (3)$$

and leading to a sub-60mV/dec swing [4]. In order for the NC to occur, the negative slope region of the polarization

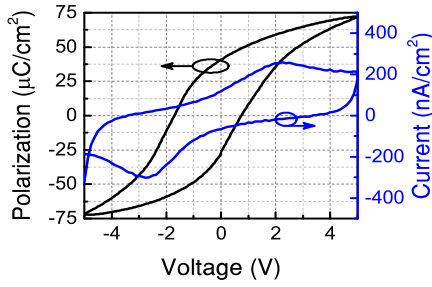


Fig. 2. Polarization and current characteristics of a 50nm thick PZT capacitor. A coercive field of +80kV/cm; -260kV/cm and a remanent polarization of  $\pm 30\mu\text{C}/\text{cm}^2$  is measured. The capacitor shows a very low leakage current in the order of nA/cm<sup>2</sup>.

should have an intersection with the transistor charge line [6]. Moreover, to have a non-hysteretic behavior, the total capacitance of the structure should remain positive in the whole range of  $V_g$  while a negative value of the total capacitance leads to instability and hysteretic jumps in the polarization characteristic of ferroelectric [7].

### III. PZT-BASED NC-FET

In this section, we report an experimental NC-FET demonstrated by connecting an external PZT capacitor to the gate of a p-type MOSFET ( $L=1\mu\text{m}$ ,  $W=3\mu\text{m}$ ). This external connection offers an advantage of testing many capacitors and MOSFETs until the best possible matching is obtained [7]. A 50nm polycrystalline PZT layer has been deposited via chemical-solution-deposition root on a Pt-coated silicon wafer. The polarization and current characteristics of PZT are illustrated in Fig. 2, showing a low switching current in the order of nA/cm<sup>2</sup>. It should be remarked that the leakage current of a ferroelectric capacitor is comparable to its switching current. High-quality epitaxial ferroelectrics are commonly considered suitable for NC devices due to their ability to form a monodomain state characterized by a simple coercive field. This is in contrast with the typical behavior of polycrystalline films, which tends to form complicated poly-domain patterns with a broad distribution of nucleation energies and coercive fields. However, this behavior can be changed dramatically by a repetitive bipolar voltage stress, known as the training procedure of ferroelectric. Here, well-trained ferroelectric capacitors are employed to demonstrate NC effect.

Fig. 3 reports and compares the electrical performance of the PZT-based NC-FET with its reference transistor. Here,  $|V_{ds}|$  is 900mV. The output transfer characteristic of the NC-FET shows a relatively small hysteresis of about 250mV as the matching condition between the ferroelectric NC and MOS capacitance is mostly fulfilled [4]. A subthreshold swing well below the thermal limit of MOSFETs, down to 20mV/dec, is evidenced (Fig. 3-b) as a result of the internal voltage gain of NC, which reaches values greater than one up to 10V/V (Fig. 3-c). The P-V curve of the PZT capacitor is obtained by imposing the displacement vector continuity, showing an effective negative capacitance in both forward and reverse

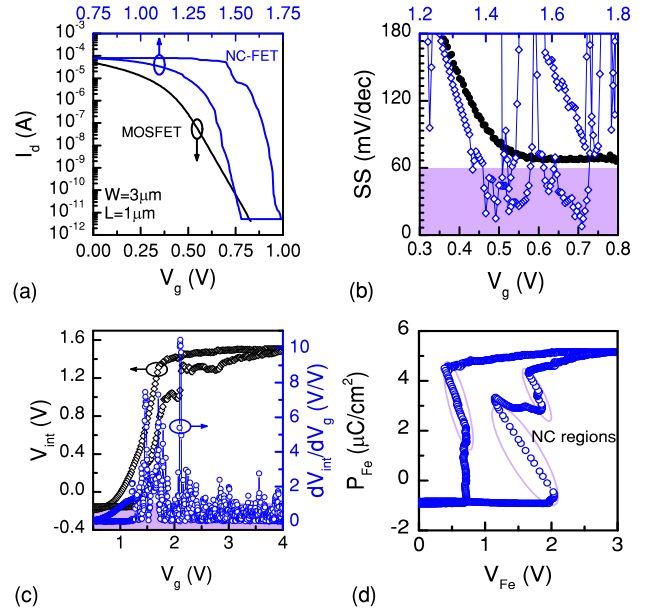


Fig. 3. Transfer characteristic of a p-type NC-FET with a low hysteresis of 250mV (a) when a PZT capacitor (thickness of 50nm and an area of  $30\mu\text{m}\times 30\mu\text{m}$ ) is externally connected to the gate of a commercial MOSFET ( $L=1\mu\text{m}$ ,  $W=3\mu\text{m}$ , and  $|V_{ds}| = 900\text{mV}$ ). The SS is effectively reduced, reaching values smaller than 20mV/dec (b). Internal voltage measurement shows an amplification factor greater than one up to 10V/V (c). Extracted polarization characteristic of the PZT capacitor demonstrates an effective NC in both forward and reverse sweeps of the gate voltage (d).

sweeps of the gate voltage (Fig. 3-d). The ferroelectric shows two separated NC regions despite the training procedure which is limiting the performance boosting of NC effect.

### IV. Si:HfO<sub>2</sub>-BASED NC-FET

Another NC-FET configuration, using the same baseline transistor and silicon-doped HfO<sub>2</sub> as the NC booster is demonstrated. A 15nm layer of Si:HfO<sub>2</sub> (4.3% Si) is deposited with ALD on a TiN coated silicon wafer. A 10nm TiN capping layer is then sputtered to provide the mechanical stress during annealing ( 800°C for 20sec). Top Pt electrodes are sputtered and patterned using shadow masking technique. The TiN layer is removed in a wet etching process. P-V and I-V plots of Si:HfO<sub>2</sub> MIM structure is depicted in Fig. 4. A remanent polarization of about  $15\mu\text{C}/\text{cm}^2$  and a coercive field of 1MV/cm are measured together with a relatively large switching current (leakage) in the range of mA/cm<sup>2</sup>.

In this last case, a limited boosting of performance is observed when a Si:HfO<sub>2</sub> ferroelectric capacitor is connected to the gate of a conventional MOSFET (Fig. 5-a). A small yet clear improvement of SS, down to 50mV/dec, is obtained (Fig. 5-b). The internal voltage measurement shows discrete regions of amplification where  $\beta$  is greater than 1, never exceeding 2V/V (Fig. 5-c). This is due to the fact that Si:HfO<sub>2</sub> is not well stabilized and performed discrete regions of NC (Fig. 5-d). A stark difference between vigorous NC effect observed on the device with PZT capacitor and a relatively weak effect measured on the device connected to the Si:HfO<sub>2</sub> capacitor

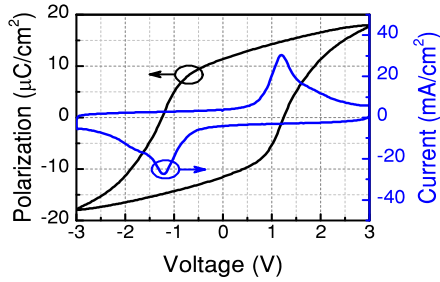


Fig. 4. P-V and I-V characteristics of a silicon-doped  $\text{HfO}_2$  ferroelectric capacitor with a thickness of 15nm and a Si concentration of 4.3%. The coercive field of  $\pm 1\text{MV/cm}$  and a remanent polarization of about  $\pm 15\mu\text{C/cm}^2$  are extracted together with a relatively high switching current.

implies that the two ferroelectrics operates differently. Unlike PZT consisting of a single tetragonal perovskite ferroelectric phase, doped  $\text{HfO}_2$  has several phases coexisting in different portions depending on processing and mechanical, thermal, and electrical conditions [5]. The ferroelectric orthorhombic phase can be promoted by choosing the right dopant and processing conditions. However, other non-ferroelectric phases (mostly monoclinic and tetragonal) cannot be eliminated completely even in the state of the art materials. The presence of the secondary phase, even in small quantity, may severely impede the formation of a stable mono-domain state, and consequently, deteriorate the NC gate performance [8]. Previous studies indicate a possibility to promote a single phase state by voltage cycling [5]. However, this technique provokes an increase of the leakage, which also undermines the NC effect [9]. Besides that, the high leakage of ferroelectric results in instability of NC in an MFMS structure [10]. This analysis highlights the importance of further improvements of  $\text{HfO}_2$  based ferroelectrics for devices with NC-enhanced gates. Specifically, ferroelectric materials composed of a single ferroelectric phase with low leakage are required for a strong and stable NC effect. Recent progress in the use of different dopants stabilizing the orthorhombic ferroelectric phase suggests that devices with CMOS compatible ferroelectric NC gates are feasible.

## V. CONCLUSIONS

The performance of NC p-type MOSFETs using PZT and  $\text{Si:HfO}_2$  is experimentally investigated in this study. A sub-thermal swing of 20mV/dec is achieved by a significant internal gain of NC up to 10V/V when PZT is employed as the NC booster. The operation of an NC-FET with CMOS compatible ferroelectric,  $\text{Si:HfO}_2$ , is also reported and discussed. A limited improvement is observed in this latter case due to the coexistence of different phases and also the high leakage current of silicon doped  $\text{HfO}_2$ .

## ACKNOWLEDGMENT

The authors acknowledge ERC advanced grant Militech (695459) for providing the financial support of this research.

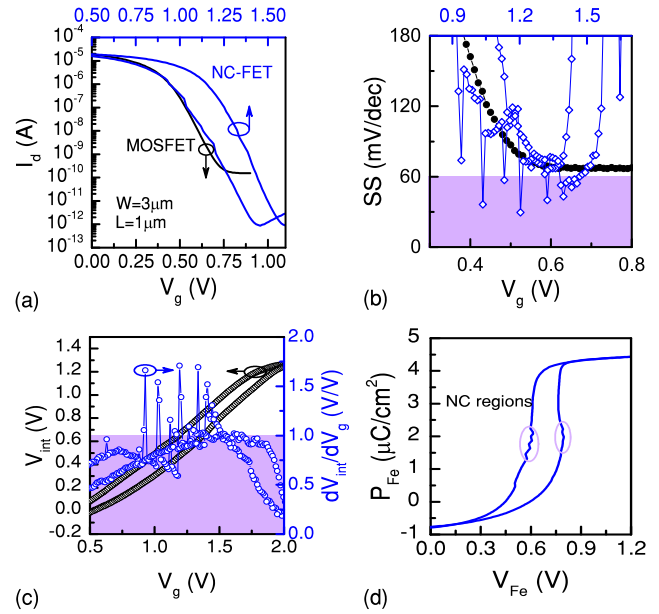


Fig. 5. Transfer characteristic of a p-type NC-FET ( $L=1\mu\text{m}$ ,  $W=3\mu\text{m}$ ) using  $\text{Si:HfO}_2$  ( $30\mu\text{m}\times 30\mu\text{m}$ ). A limited improvement is observed in the device performance due to the NC effect ( $|V_{ds}|=900\text{mV}$ ) (a). SS is slightly improved (50mV/dec) (b). Internal voltage measurements show discrete points of amplification with values below 2V/V (c). P-V plot of the ferroelectric shows multiple small regions of negative capacitance (d).

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