Effect of Negative Capacitance on Tunnel FETs DC Performance

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Abstract. This work experimentally demonstrates that the negative capacitance effect can be used to significantly improve the key figures of merit of tunnel FET switches. In the proposed approach, a matching condition is achieved between a trained-polycrystalline PZT capacitor and the TFET gate capacitance fabricated on a strained silicon-nanowire technology. We report a non-hysteretic switch configuration by combining a homojunction TFET and a negative capacitance effect booster, suitable for logic applications, for which the *on*-current is increased by a factor of 100x, the transconductance by 2 orders of magnitude, and the region of low values of the subthreshold slope is extended. The operation of a hysteretic negative capacitance TFET, when the matching condition for the negative capacitance is fulfilled only in a limited region of operation, is also reported and discussed. In this late case, a limited improvement in the device performance is observed. Overall, the paper demonstrates the main beneficial effects of negative capacitance on TFETs are the overdrive and transconductance amplification, which address exactly the most limiting performances of the current TFETs.

1. Introduction

As CMOS technology is continuing its relentless downscaling, new challenges are encountered to sustain the performance of integrated circuits; among these, the reduction of the threshold voltage and voltage multiply are high priorities of the research community. Among alternative structures, Tunnel FETs (TFETs) are the most promising steep-slope switch candidates making use of quantum-mechanical Band-To-Band Tunneling (BTBT).[1, 2, 3] The most critical challenge in TFETs is to realize high *on*-current without compromising the subthreshold swing. The *on*-current of the TFET is the integral of the transmission probability, T_{WKB}, of the interband tunneling barrier over the source-channel junction[4, 5]. This barrier can be approximated by a

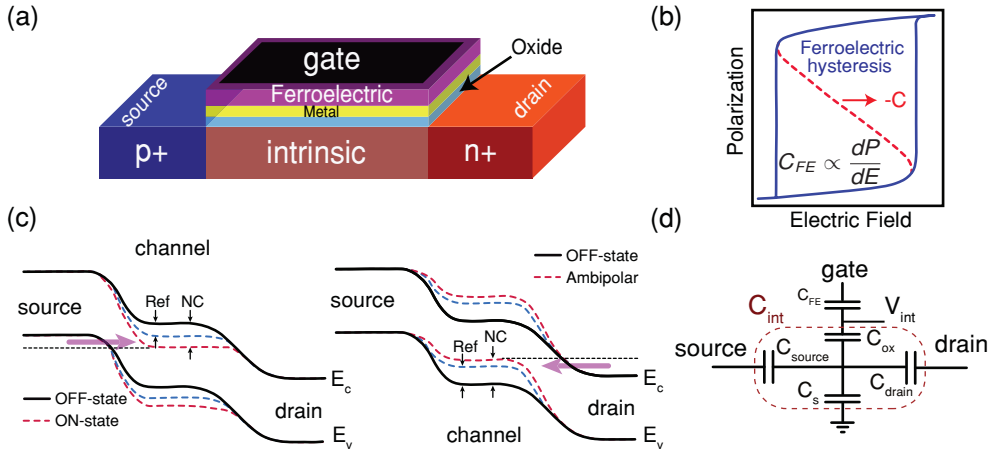

Figure 1. NC-TFET structure and operation principle. (a) Cross-section schematic of an n-type NC-TFET. (b) The P-E characteristic of ferroelectric materials that can be stabilized and provide an effective NC if it placed in-series with a positive capacitor. (c) The NC-TFET band diagram is presented for $V_g > 0$ (left) and $V_g < 0$ (right) corresponding to the normal operation and ambipolar behavior of an n-type NC-TFET. The amplified gate voltage reduces the energetic difference between the conduction band in the source and valence band of the channel that results in an enhanced tunneling current. (d) The simplified capacitance model of the NC-TFET where C_{source} and C_{drain} represent the gate overlapping capacitance with source and drain, respectively. The ferroelectric, oxide, and semiconductor capacitances are expressed as C_{FE}, C_{ox}, and C_s.

triangular potential[2], so T_{WKB} can be calculated using the Wentzel-Kramer-Brillouin (WKB) approximation[6]:

$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^\star}\sqrt{E_g^3}}{3q\hbar\left(E_g + \Delta\Phi\right)}\right), \tag{1}$$

where $m^\star$ is the effective mass and E_g is the bandgap. Here, λ is the screening tunneling length that describes the spatial extent of the transition region at the source-channel interface[4]. In a TFET, at a constant drain voltage (V_d), the increase of the gate voltage (V_g) modulates the device surface potential, which reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel ($\Delta\Phi$). This means that in the first approximation, the drain current is a super-exponential function of V_g (a high *on*-current requires a high transparency of the tunneling barrier, thus maximizing T_{WKB})[7].

Recently, it has been suggested that the integration of a ferroelectric material to the gate stack of conventional field effect transistors (FETs) can provide a feasible solution to step up the gate voltage. The underlying idea consists of exploiting the Negative Capacitance (NC) region of the ferroelectric materials, which is defined as $C_{FE} = dQ/dV_{FE}$, where Q and V_{FE} refer to the charge density per unit area and the voltage drop over the ferroelectric, respectively[8, 9, 10]. It is well established that ferroelectric materials can provide an effective NC in a certain range of the polarization[11, 12].

Theoretically, the use of a ferroelectric negative capacitor in-series with the gate of a field effect transistor could offer an internal voltage amplification[13, 14], which is expected to increase the tunneling probability in TFETs[10, 15].

The NC-TFET structure and its operation principle are schematically depicted in Figure 1. The gate stack of a conventional TFET is replaced by a series combination of a ferroelectric and linear dielectric[16]. The use of an intermediate metallic film has the advantage to avoid any non-uniform potential profile along the source-drain direction[10]. The NC region of ferroelectric materials is unstable and exhibits hysteretic jumps in polarization. However, it can be stabilized if a series capacitance, such the one formed by a conventional oxide and a semiconductor in an MOS structure, is placed in-series with the ferroelectric negative capacitor (Figure 1b). The challenges of using BTBT together with the NC in a single device are related to the matched design of the capacitances (ferroelectric and in-series stabilizing MOS capacitance) in a regime of operation, where a significant boosting of TFET electrical performance can be achieved[5, 17, 14]. In order to have a non-hysteretic NC switch, the total capacitance of the gate needs to be positive in the whole range of the operation[16]. Accordingly, the matching condition of the NC-TFET to have a sufficient amplification in the non-hysteretic operation of the device can express as it follows[14, 18, 5, 17, 19]:

$$C_{total} = \left(C_{FE}^{-1} + C_{int}^{-1}\right)^{-1} > 0, \tag{2}$$

$$\beta = \frac{\partial V_{gint}}{\partial V_g} = \frac{C_{FE}}{C_{FE} + C_{int}} \gg 1, \tag{3}$$

where β is the amplification factor due to the differential amplification of NC, C_{int} and C_{total} represent the equivalent capacitance of the base TFET and NC-TFET, respectively (Figure 1d). The amplification factor, β, is introduced as the derivative of the internal voltage with respect to the gate voltage and its rather a differential voltage gain [19, 14]. The absolute value of the ferroelectric negative capacitance ($|C_{FE}|$) and C_{int} needs to be relatively close, while the total capacitance of the gate should remain positive in the whole range of the operation[14]. Using the amplification factor of NC, β, the subthreshold swing (SS) and transconductance (g_m) of a NC switch can be indicated as

$$SS_{NC} = \left(\frac{\partial log I_d}{\partial V_g}\right)^{-1} = \frac{\partial V_{int}}{\partial log I_d} \times \frac{\partial V_g}{\partial V_{int}} = \frac{SS_{ref}}{\beta}, \tag{4}$$

$$g_{m-NC} = \frac{\partial I_d}{\partial V_g} = \frac{\partial I_d}{\partial V_{int}} \times \frac{\partial V_{int}}{\partial V_g} = g_{m-ref} \times \beta. \tag{5}$$

In the region where the ferroelectric provides an effective negative capacitance, $\beta > 1$ and the *on*-current will be boosted as a result of the subthreshold slope and transconductance enhancement. A direct analytical expression that quantitatively links β to the total drain current of the NC-TFET cannot be provided as the tunneling current depends on the surface potential near the tunneling junction in a complex way. Previous works [8, 9, 10] have essentially concentrated on the role of the internal gain,

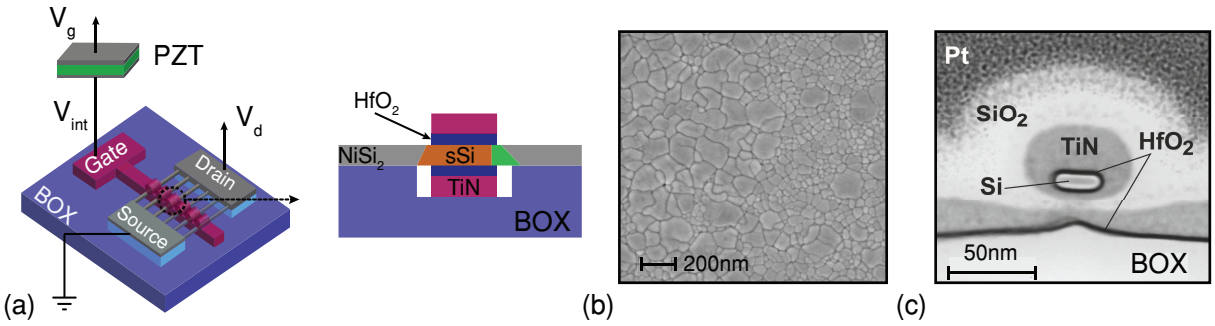

Figure 2. (a) The investigated experimental configuration of the NC-TFET, where the gate of a Si-NW array TFET is loaded by a PZT capacitor. (b) The SEM analysis of the PZT indicating the polycrystalline nature of the film. (c) The transmission electron microscopy image of the silicon-nanowire TFET. The nanowire array TFETs have a cross section of $30\times5\text{nm}^2$ with a gate length of $350\mu m$.

β, to reduce the subthreshold slope of FETs, while here we explore the double beneficial role of β on both subthreshold and overdrive regions of TFETs in a non-hysteretic configuration. The non-hysteretic operation of a negative capacitor can be observed by performing specific time domain measurement conditions [20]. However, this is different with our proposed approach that guarantees the non-hysteretic operation of a negative capacitance field effect transistor regardless of measurement conditions.

2. Experiments

The employed experimental configuration of the NC-TFET in this work is depicted in Figure 2a where a PZT capacitor is externally connected to the gate of a strained Silicon-Nanowire (Si-NW) array TFET. Such external electrical connection offers the flexibility of testing tens to hundreds of PZT capacitor values until the best matching, according to equations (2) and (3), is obtained. The employed configuration is actually a Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) structure that is commonly used for the experimental configuration of NC field effect transistors [10]. For this study, 46 ± 3nm of $Pb(Zr_{43},Ti_{57})O_3$ (PZT) ferroelectric film has been grown via the chemical solution deposition root on a Pt-coated silicon wafer. The polycrystalline PZT film has a dense columnar grain structure with the grain size of 200 ± 100nm (Figure 2b). The fabrication process and the electrical characterization of the employed PZT thin film are extensively discussed in the supplementary materials. The nanowire array TFETs have a cross section of $30\times5\text{nm}^2$ with a gate length of $350\mu m$ (Figure 2c). The structural data and the fabrication procedure of reference TFETs are also explained in detail in supplementary materials.

Generally, high-quality epitaxial ferroelectric layers are considered suitable for NC devices as they are more likely to form a mono-domain state characterized by a simple coercive field[21]. This is in contrast with the typical behavior of polycrystalline films, which tend to form complicated poly-domain patterns with a broad distribution of

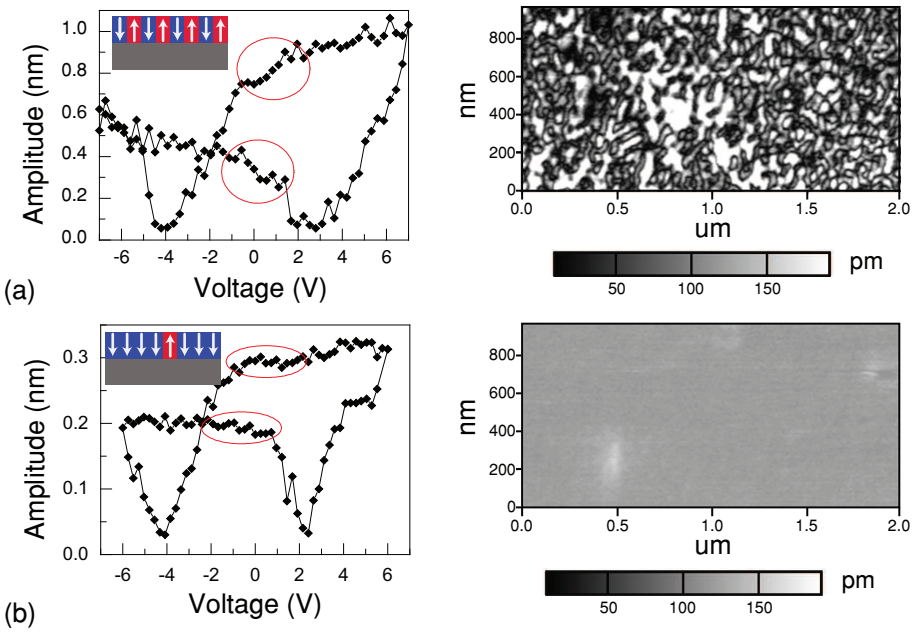

Figure 3. The piezoelectric response of the PZT thin film. Results are measured before (a) and after (b) the training procedure of ferroelectric. (a) illustrates the broad distribution of nucleation energies and coercive fields while (b) represents the mono-domain like behavior of the poled PZT after 20 cycles at ±7V.

nucleation energies and coercive fields[22, 23, 24]. Here, we show that this behavior can be changed dramatically by repetitive bipolar voltage stress, known as the training procedure of the ferroelectric. It should be noted that the training procedure of ferroelectric is different from the well-known wake-up phenomena. The wake-up effect corresponds to the increase of existing remanent polarization after a large number of switching cycles ($> 10^3$)[25, 26]. Here, we are raising the point that by applying a limited number of bipolar voltage stress, dipoles can be aligned in the same direction which leads to a mono-domain-like behavior of the ferroelectric film. Figure 3 depicts the piezoelectric response measured on the PZT capacitor before (Figure 3a) and after (Figure 3b) the training. Piezoelectric loops measured through the top electrode of the PZT capacitor after 20 cycles at ±7V represent sharp switching and nearly constant piezoelectric response within the voltage range from -2V to 1V (or from 2V to -1V). This behavior suggests that the poled polycrystalline ferroelectric layer approaches the mono-domain behavior and does not switch at least at low DC voltages up to 2V[21]. Note that the piezoelectric loops collected on the as-fabricated capacitors without any training reveal different behavior typical for region-by-region poly-domain switching expected from a polycrystalline film. Consequently, the demonstration of the NC effect using a polycrystalline ferroelectric layer constitutes a significant step towards the integration of NC gates in CMOS technology[21]. In fact, fabrication of epitaxial perovskite layers on silicon is an extremely challenging task, whereas polycrystalline ferroelectrics such as PZT can be integrated, as shown in previous reports[27, 28].

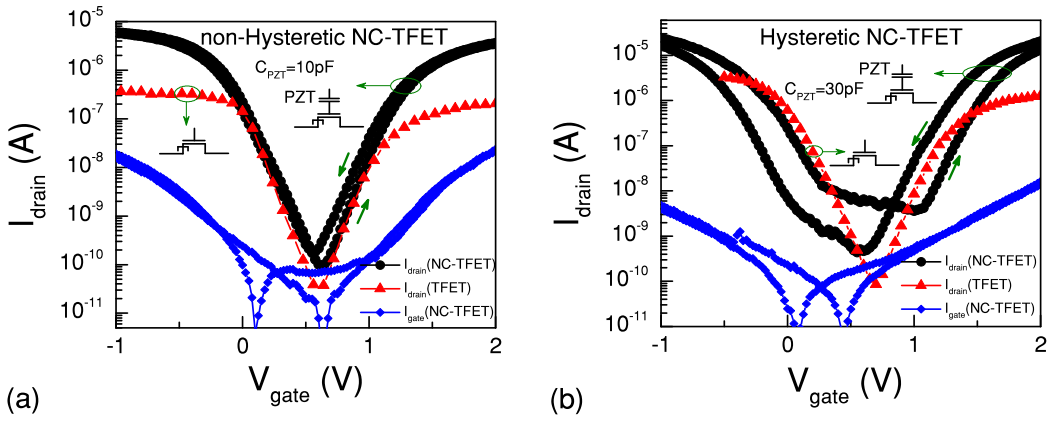

Figure 4. Transfer characteristics of a non-hysteretic and a hysteretic NC-TFET where the negative capacitance matching condition is fulfilled in the entire range of the operation (a) and in a limited range of the gate voltage (b). The reference devices correspond to Si-NW array n-type TFETs with the drain voltage of 0.5V.

3. Results and Discussions

Figure 4 reports experimental transfer characteristics data measured on n-type Si-NW array TFETs with and without connecting a PZT capacitor. The reference homojunction TFETs have I_{on} $\sim$0.1μA at V_g=2V and V_d=0.5V with a swing in the order of 100-150mV/dec and show ambipolar behavior. The presented characteristics in Figure 4 are indeed for two different tunnel FETs that are not identical due to the process variation. The gate current of TFETs is very low and negligible compared to the drain current over the whole operation range. A significant double improvement in subthreshold slope and overdrive of the TFET is shown in Figure 4a when the ferroelectric and the gate capacitances are matched so that a non-hysteretic NC operation can be achieved over the whole gate voltage range. The I_{on} is boosted over the whole range of the operation, enhanced up to 100 times of its original value at the maximum gate voltage. This is explained by the fact that the NC behaves as an efficient electrical booster of the surface potential (ψ_s) and the body factor (m) of the TFET in the region following the barrier narrowing. This is fundamentally reflected into a body factor reduction less than 1, acting as a performance booster where the *on*-current of the TFETs would otherwise start to have a sloppy dependence on the gate voltage[2, 4]. It should be remarked that the surface potential boosting of NC effect not only increases the tunneling probability but also improves the region over which the tunneling current is integrated. In addition to, considering Landau-Khalatnikov equation, high order terms of the ferroelectric charge cannot be neglected at high gate voltages that result in an enhanced negative capacitance effect [29]. The NC effect acts as the TFET performance booster near subthreshold ($V_g < V_{th}$) and for the overdrive region ($V_g > V_{th}$). Therefore, the gate voltage can be reduced by 65% maintaining the same level of the output current. Another device architecture with a different PZT capacitor and TFET, matching the condition of NC only in a limited region (at high V_g) is reported in Figure 4b. In this

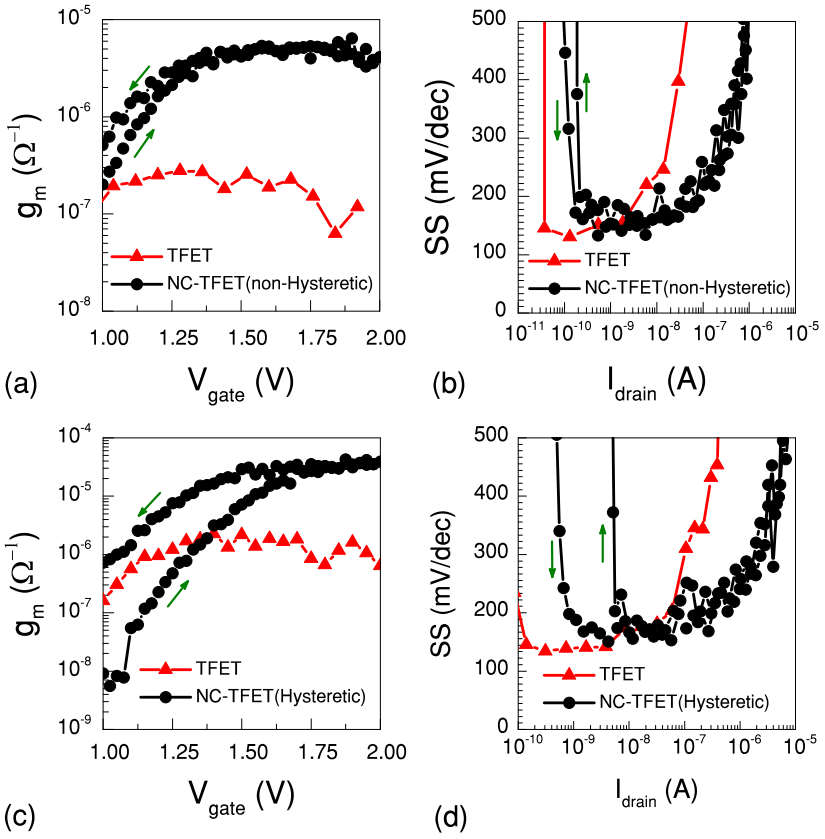

Figure 5. Experimental performance improvement of non-hysteretic and hysteretic NC-TFETs corresponding to the presented devices in Figures 4a and 4b. The transconductance is boosted up to 100 times of its original value (a) and the low slope region is extended over 2 decades of current (b) in the case of the non-hysteretic NC-TFET. A more limited enhancement is obtained in the transconductance of the hysteretic NC-TFET (c) without any boosting in the subthreshold slope (d).

late case, the NC-TFET operation is fully hysteretic and the performance boosting is narrowed down to a reduced region. All measurements have been carried out at the low drain voltage of 0.5V due to the fact that high values of the drain voltage provide a non-uniform potential profile that will change the negative capacitance condition [19]. Both Figures 4a and 4b report the recorded gate leakage current in all range of experiments, proving that its level is systematically lower than the I_{on} and, then, that leakage and charge trapping mechanisms can be neglected in the reported effects. Moreover, this hysteretic leakage presents the typical signature of the ferroelectricity of PZT capacitors. The obtained enhancement in the TFET performance should not be mistaken with the effect of the ferroelectric polarization switching that always causes a huge hysteresis. The reported non-hysteretic improvement in the current and conductance can be only achieved in a well-designed negative capacitance transistor.

In Figure 5, we report the improvement induced by the use of the negative capacitance on TFET transconductance and subthreshold slope, in non-hysteretic and hysteretic matching conditions. Double sweep measurements with a negligible hysteresis

for a device that fulfills the analytical condition of the non-hysteretic NC (corresponds to the presented device in Figure 4a) are reported in Figures 5a and 5b. In this case, the ferroelectric is stabilized and provides an effective NC in the whole range of the gate voltage which results in an amplification factor above unity ($\beta > 1$) in both subthreshold and overdrive regions. Figure 5a represents the transconductance boosting by a factor of 10 to 100 compared to the base TFET. The largest improvement (higher β value) occurs in the overdrive region ($V_g > V_{th}$) due to the surface potential amplification, caused by the NC effect where g_m is increased by up to two orders of magnitude. This evidences that the negative capacitance provides a very strong performance boosting effect in TFETs. Figure 5b illustrates a smaller, yet clear improvement of the subthreshold swing by the NC effect, in agreement with the recently reported theoretical results[30, 31]. As a consequence of the SS and overdrive enhancement, the *on*-current is boosted over the whole operation range.

Figures 5c and 5d summarize the effect of the PZT capacitor on DC electrical performance of the hysteretic NC-TEFT (Figure 4b) fulfilling the NC matching condition in a limited region. The transconductance is boosted for high V_g, reaching a factor of 10x at the maximum gate voltage (Figure 5c). The subthreshold slope shows no considerable enhancement (Figure 5d) as the NC matching condition is not fulfilled for low gate voltages. It is remarkable that from variously tested devices, only for the ones that closely verifying the NC stability condition, such a performance boosting is observed. Otherwise, a ferroelectric capacitor out of the range of the stability condition in-series with the gate of a TFET would provide a hysteresis without performance boosting. This type of device could be a proper candidate for hysteretic low power logic or for one transistor (1T) Fe-TFET memory applications[31].

Conclusion

In short, it has been reported that the NC can be efficiently utilized to significantly improve the most limiting factors of TFETs: *on*-current, transconductance, and overdrive. It was demonstrated that by designing properly the ferroelectric gate stack, fulfilling the condition for the non-hysteretic NC-TFET, the conduction performance can be improved by many orders of magnitude for $V_g > V_{th}$ and a significant overdrive can be obtained. This strong effect is explained by the voltage amplification that is caused due to the ferroelectrics negative capacitance. The NC has been reached using a chemical-solution-deposited polycrystalline PZT thin film and employing the training procedure of ferroelectrics. By its insights and reported experiments, this paper proposes a new path to the adoption of both homojunction and heterojunction TFETs with an improved performance, while a NC effect booster is properly designed and additively integrated into their gate stack.

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