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# An Approach for the Emulation of DC Grid Admittances: Implementation on a Buck Converter

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**Abstract**—This work proposes a method to actively emulate dc grids, including their equivalent admittance, by means of a modified current control structure of a dc/dc converter. The stability of power converter units (PCUs), interconnected with electrical grids is frequently assessed by the characteristics of the equivalent admittance/impedance of the grid, at the point of connection, and the PCU. Several approaches have been proposed to shape the PCU equivalent admittance, by means of the control structure, in order to fulfil the requirements about stability, robustness and dynamic response. On top of this, the integration of dc distribution systems is steadily growing, due to its simpler implementation and the potential cost and losses reduction. The presence of PCUs, in dc grids, is inherently higher, which complicates the overall stability assessment. In order to verify an impedance/admittance stability analysis in a laboratory scaled system, the characteristics of the impedance/admittance needs to be emulated. A suitable control structure, implemented on a buck converter, to actively emulate dc grid admittance has been proposed and tested. The analytical expressions of the emulator converter admittance, with the modified control structure, are presented. The admittances of a MVDC collection network for offshore wind farms, and a MVDC drive, working with a vector control scheme, have been calculated to be used for the emulation. The experimental validation has shown the overall feasibility of the proposed emulation approach.

## I. INTRODUCTION AND MOTIVATION

The integration of dc distribution systems has grown significantly in recent years due to the potential efficiency improvement, cost reduction and simplicity. The specific benefits of implementing a dc distribution system varies significantly with the application [e.g. ac grid availability, high presence of energy storage systems (ESS) or electronics loads, etc.], however, for isolated electrical power systems, the use of dc voltage is, in general, the most convenient option [1], and in the telecommunication and automotive industries, dc distribution system are a mature solution [2], [3].

Lately, this trend can be observed in higher power electric systems, as the ones used for maritime and aircraft applications [4]–[7], but also in grid connected systems with a high presence of dc loads, as datacenters [8].

Furthermore, a high penetration of renewable energy sources (RES) and ESS at consumption level, allows for a significant efficiency improvement, by avoiding unnecessary conversion stages, since distribution between mostly dc-based devices [e.g. photovoltaic (PV) panels, batteries, and electronic loads] is performed more efficiently if dc voltage is employed [1], [9]. For higher power distribution, through longer distances, the

absence of reactive power, makes dc voltage a more suitable candidate for distribution in low-voltage (LV) [10], medium-voltage (MV) [11], [12], and high-voltage (HV) [13].

Nevertheless, the use of dc, always relies on power converter units (PCUs) to adapt the voltage levels, making the presence of PCUs inherently higher in dc distribution systems, which can compromise the overall stability of the system [14]–[18].

Impedance-based methods are frequently used to assess the stability of the electrical system, and to design the control structures of the power converters [6], [7], [16]–[22]. The electrical power system can be systematically analysed by studying the interaction of the output impedance of the source converter (e.g. a MVDC collector converter of an offshore wind farm [12], or a front-end rectifier for supplying a datacenter [23], etc. ), and the equivalent admittance of the rest of the system, aggregated in the total grid admittance.

The grid admittance depends on several factors (i.e. distribution architecture, individual admittance of the connected power converters, cables...) and replicating the specific grid conditions for testing the source converter can be challenging.

In this work, an approach to actively emulate a given dc grid admittance, is shown. The emulation is performed by means of a modified current control structure that sets a relation between the input voltage and current of the PCU. The concept of the active admittance emulator is shown in Fig. 1. In many applications, the output impedance of the source converter  $Z_s(s)$  is shaped, so a set of design requirements are fulfilled when interacting with the equivalent admittance of the rest of the dc grid,  $Y_g(s)$ , as seen from the point of connection of the source converter. Therefore, in order to perform the experimental validations, the approach shown in Fig. 1, can be followed, where the dc grid admittance is emulated by a second PCU connected at the terminal of the source converter.

The same reasoning has been applied for emulating the behaviour of devices, where a dc/dc converter is used to replicate different components such as PV panels and batteries [24], [25], for a given emulated conditions (e.g. solar irradiation, temperature, state of charge, etc.).

## II. MODELLING AND CONTROL OF BUCK CONVERTER FOR ADMITTANCE EMULATION

The proposed approach, for emulation of an equivalent dc grid admittance, is based on a modified current control structure, that shapes the equivalent input admittance of the

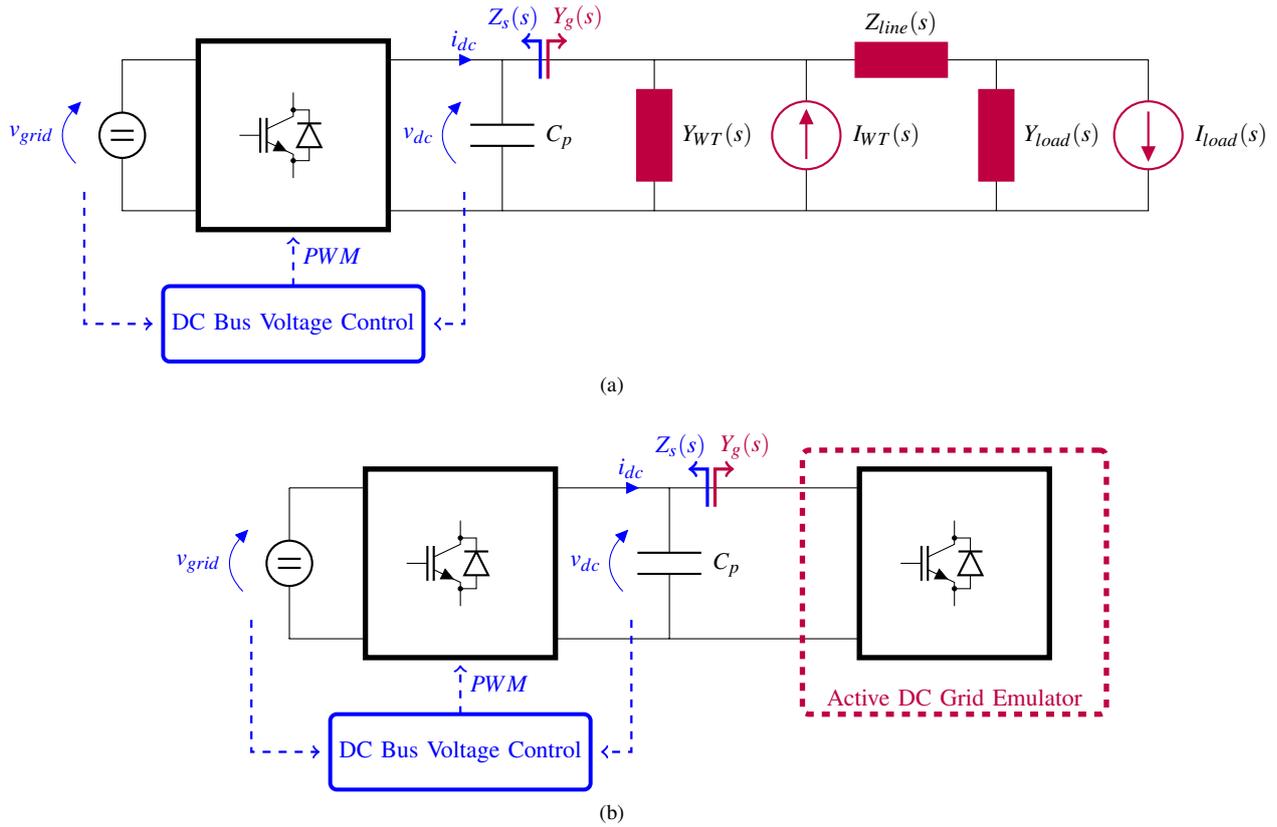


Fig. 1: Concept of dc grid admittance emulator.

emulator converter ( $Y_{em}$  in the rest of the paper), in order to match the objective dc grid admittance ( $Y_g$  in the rest of the paper).

In the scenario shown in Fig. 1, the dc grid admittance defines the grid current responses against voltage variations at the terminal of the source converter, therefore, it can be seen that the converter needs to regulate the input current as function of the input voltage, in order to emulate the dc grid behaviour.

In this work, a buck converter is modelled for the application. The current control is performed on the inductor of the converter, as shown in Fig. 2. The current references are obtained from the input voltage ( $v_s$ ) measurements and the objective grid admittance (e.g.  $i_s^*(s) = Y_g(s)v_s(s)$ ), therefore it is expected that, within the current controller bandwidth,  $Y_{em}(s) \approx Y_g(s)$ . The use of the buck topology, allows for a lower converter output voltage (i.e.  $V_o < V_s$ ), nevertheless, the inductor is placed at the output, and therefore,  $i_s$  is not directly controlled (i.e. the control is performed on  $i_o$ , and  $i_o^*$  needs to be estimated from  $i_s^*$ ).

Alternatively, using a boost converter, would allow to directly control  $i_s$ , however, it requires a higher voltage on the output side, ideally twice as big, which can compromise the implementation of this topology due to hardware limitations, especially for MVDC or HVDC applications. Therefore, for this work, the buck topology has been analysed.

For the admittance calculation of the emulator, the current and voltage waveforms have been averaged during one switch-

ing period, therefore the equations that described the system, are as follows:

$$L \frac{di_o(t)}{dt} = [v_s(t) - v_o(t)]d(t) - v_o(t)[1 - d(t)] \quad (1)$$

$$i_s(t) = i_o(t)d(t) \quad (2)$$

where  $v_s(t)$ ,  $v_o(t)$ ,  $i_s(t)$  and  $i_o(t)$  are the voltages and currents on the high voltage and low voltage sides, respectively,  $L$  is the inductance value of the inductor in the buck converter, and  $d(t)$  is the duty cycle.

It can be seen that equation (1) and (2) are non-linear, therefore linearizing the equations around a given operating point, and assuming that  $V_o$  is tightly regulated ( $\hat{v}_o(t) \approx 0$ ), results in the following linear expressions in the s-domain:

$$Ls i_o(s) = d(s)V_s + v_s(s)D \quad (3)$$

$$i_s(s) = i_o(s)D + d(s)I_o \quad (4)$$

From the control structure shown in Fig. 2, the expression of  $d(s)$  can be obtained.

$$d(s) = \frac{e^{-sT} H_{zoh}(s)}{V_s} K(s) \left[ \frac{v_s(s) Y_g(s)}{D} - i_o(s) \right] \quad (5)$$

where  $Y_g(s)$  is the equivalent admittance of grid that is being emulated,  $K(s)$  is the main current controller,  $D$  and  $V_s$  are the dc quantities of the duty cycle and the input voltage respectively, and  $e^{-sT}$  and  $H_{zoh}(s)$  are the system delays due

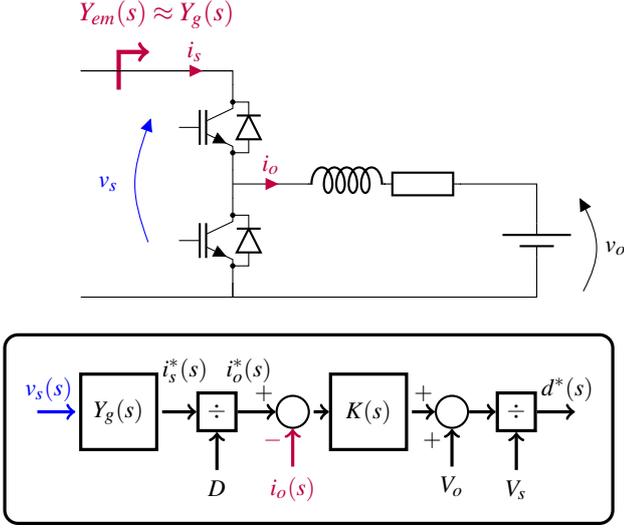


Fig. 2: Control structure of the active dc grid admittance emulator based on a buck converter.

to the sampling and PWM action.

The model of the system is shown in Fig. 2. From equations (1), (2), and (5), the emulator admittance can be derived, and the expression is the following:

$$Y_{em}(s) = \frac{i_s(s)}{v_s(s)} = B_0(s) + Y_g(s)B_1(s) \quad (6)$$

where,

$$B_0(s) = \frac{Y_o/Y_s - Y_s C}{Ls + C} \quad (7)$$

$$B_1(s) = \frac{C + Y_o C(Ls + C) - Y_o C^2}{Ls + C} \quad (8)$$

where,  $Y_o = I_o/V_o$ ,  $Y_s = I_s/V_s$ , and  $C = K(s)e^{-sT}H_{zoh}(s)$ .

Equation (6) shows that  $Y_{em}(s)$  is formed by two terms, a term  $B_0(s)$  independent of the objective admittance, and a second term,  $B_1(s)Y_g(s)$ , dependent on the objective admittance. It is easily appreciated that an ideal admittance emulator (i.e.  $Y_{em}(s) = Y_g(s)$ ) is achieved when  $B_0(s) = 0$ , and  $B_1(s) = 1$  for the whole frequency range. This is not achievable in practise due to finite controller gains and time delays.

As it can be seen from (7), and (8), the tuning of the current regulator,  $K(s)$ , and the converter parameters ( $L$ ,  $V_s$ ,  $V_o$ , etc.) allows to shape the frequency response of  $B_0(s)$ , and  $B_1(s)$ . It has been found that, tuning the current controller to cancel the pole of the converter inductor ( $K_i = R/L$ ) and a close loop bandwidth ( $K_p = 2\pi Lbw$ ) slightly below  $\omega_s/10$ , gives the best match of both magnitude and phase of the objective admittance,  $Y_g(s)$ .

Fig. 3 show the frequency responses of  $B_0(s)$ , and  $B_1(s)$ , where the  $e^{-sT}$  and  $H_{zoh}(s)$  have been approximated by their first order expressions [20]. It can be seen that, first,  $B_0(s)$  has a magnitude below -40 dB, and second,  $B_1(s)$  has a magnitude of 0 dB up to  $\omega_s/10$  approximately, while introducing some phase delay after  $\omega_s/100$ .

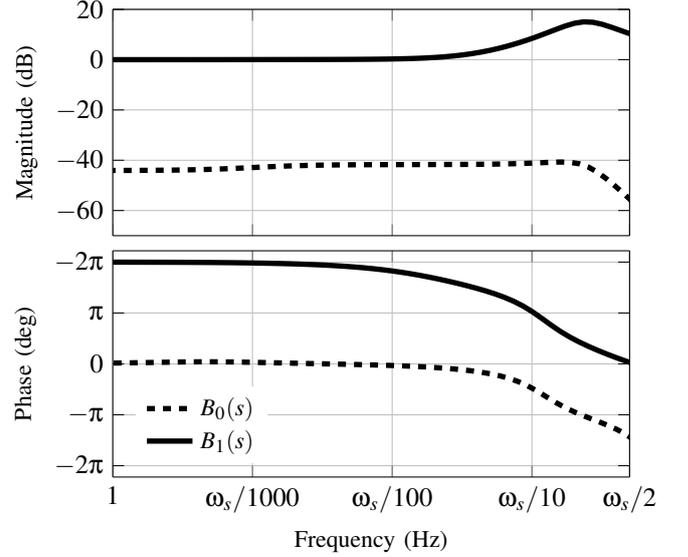


Fig. 3: Frequency responses of  $B_0(s)$  and  $B_1(s)$ .

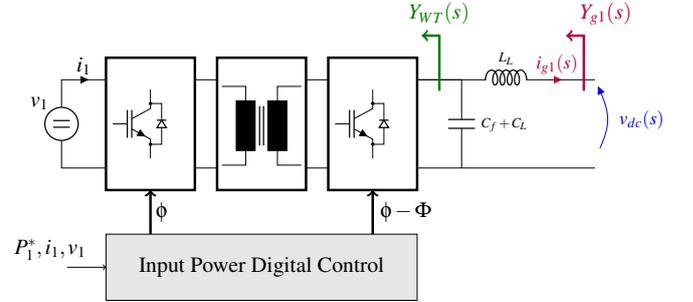


Fig. 4: Studied System of a DC Collection Network for Offshore Wind Farms.

### III. EQUIVALENT ADMITTANCES OF DC GRIDS

In order to assess the feasibility of the proposed emulation approach, two representatives cases of dc distribution systems have been selected and modelled, in order to use the calculated dc grid admittances [ $Y_{g1}(s)$  and  $Y_{g2}(s)$ ] in the emulator. The dc grid admittances, calculate in this Section, include the effect of constant power sources (CPSs), constant power loads (CPLs), and resonances introduced by the distribution line parameters. The presence of this elements y a dc distribution grid can compromise the stability of the system, therefore they are of most interest to test the emulation approach. Also, both dc grid admittances have been calculated in p.u. values.

#### A. MVDC collection Network for Offshore Wind Farms

The first case consist on a dc distribution line that connects the output of a WT, interfaced by a dc-dc converter, with a collector converter, that it is connected to the HVAC or HVDC grid. This configuration, shown in Fig. 4, has been widely proposed in the literature for WT farms collectors [11], [12], [26]–[29].

In this particular case, a WT interfaced by a dual-active-bridge (DAB) converter, working under power control oper-

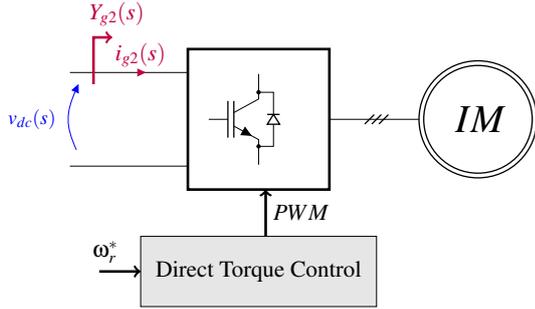


Fig. 5: Analysed system of a MV drive supplied from a DC source.

Table I: Physical parameters used for the study cases.

Parameter	Value
<b>DAB</b>	
Nominal Power ( $P_1$ )	1 MW
Nominal Input Voltage ( $V_1$ )	1000 V
Nominal Output Voltage ( $V_2$ )	10 kV
Controller Bandwidth ( $\alpha$ )	$2\pi 10$ rad/s
<b>Line</b>	
Line inductance ( $L_L$ )	0.347 mH/km
Line resistance ( $R_L$ )	0.089 $\Omega$ /km
Line Capacitance ( $C_L$ )	0.307 $\mu$ F/mk
Filter capacitance ( $C_f$ )	6.5 mF
Length	1 km
<b>Drive</b>	
Nominal Power	3 MW
Nominal DC bus Voltage	10 kV
Switching Frequency	250 Hz
Control Bandwidth	$2\pi 15$ rad/s

ation, has been modelled. The low voltage (LV) side of the DAB converter receives the output power of the rectifier ( $P_1$ ), connected to the WT generator. Therefore the DAB acts a physical actuator of a higher level mechanical controller, that regulates the power that is extracted from the turbine.

In WT applications, the requirements, for the controller design, are the specified maximum allowable time constant, and no overshoot in the power tracking response. The parameters used for this study case are shown in table I. Linearizing the system at a given operating point, the output admittance of the WT is seen as a CPS, up to the bandwidth of the power controller. The analytical derivation of the WT equivalent admittance is as follows:

$$Y_{WT}(s) = \frac{I_2}{V_2} \frac{\alpha}{s + \alpha} \quad (9)$$

where,  $I_2$  and  $V_2$  are the output current and voltage of the DAB converter, and  $\alpha$  is the close loop bandwidth of the power controller.

From Fig. 4, the equivalent admittance of the grid ( $Y_{g1}$ ), as

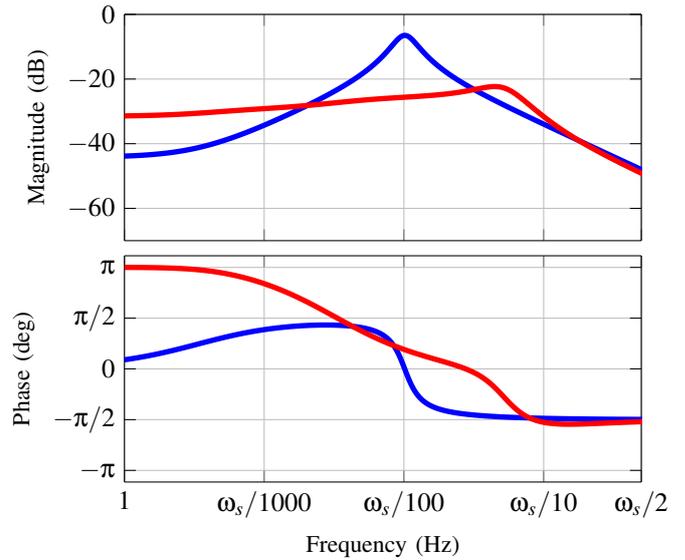


Fig. 6: Calculated equivalent dc grid admittances. DC collection network for offshore wind farms,  $Y_{g1}(s)$  (blue), and for a drive working with DTC,  $Y_{g2}(s)$  (red).

seen from the collector, can be calculated as follows:

$$Z_{g1}(s) = \frac{1}{Y_{WT}(s) + Y_C(s)} + Z_L(s) \quad (10)$$

$$Y_{g1}(s) = \frac{i_{g1}(s)}{v_{dc}(s)} = \frac{1}{Z_{g1}(s)} \quad (11)$$

where,  $Y_C(s)$  is the admittance of the combination of the DAB filter capacitance ( $C_f$ ) and parasitic line capacitance ( $C_L$ ), and  $Z_L(s)$  is the impedance of the parasitic line inductance.

The frequency response of  $Y_{g1}(s)$  is shown in Fig. 6. As expected, at low frequencies, the admittance is dominated by the power control of the WT [ $Y_{WT}(s)$ ], while the filter capacitance, together with the parasitic line parameters, create a resonance. The dc value of  $Y_{g1}(s)$  is given the operating point of the WT (i.e.  $P_2 = V_2 I_2$  in steady state operation), while for higher frequencies, beyond the controller bandwidth, the line parameters dominate the shape of  $Y_{g1}(s)$ .

## B. MVDC Drive

The second case is based on a drive connected to a MVDC electrical distribution system for maritime applications. In this application, the stability of the electrical system can be compromise by high presence of high-power motor drives (propulsion motors can make up to 80% of the electrical load of the ship [6]), which generally show a CPL behaviour [18].

Vector controls of motors are used as the control of the propulsion drives [e.g. field-oriented control (FOC) and DTC]. The specific parameters used to derived the equivalent admittance of the propulsion drive,  $Y_{g2}(s)$ , are shown in Table I, however an analytical expression for the equivalent input admittance has not been obtained. The system has been simulated using PLECS, and  $Y_{g2}(s)$  has been measured.

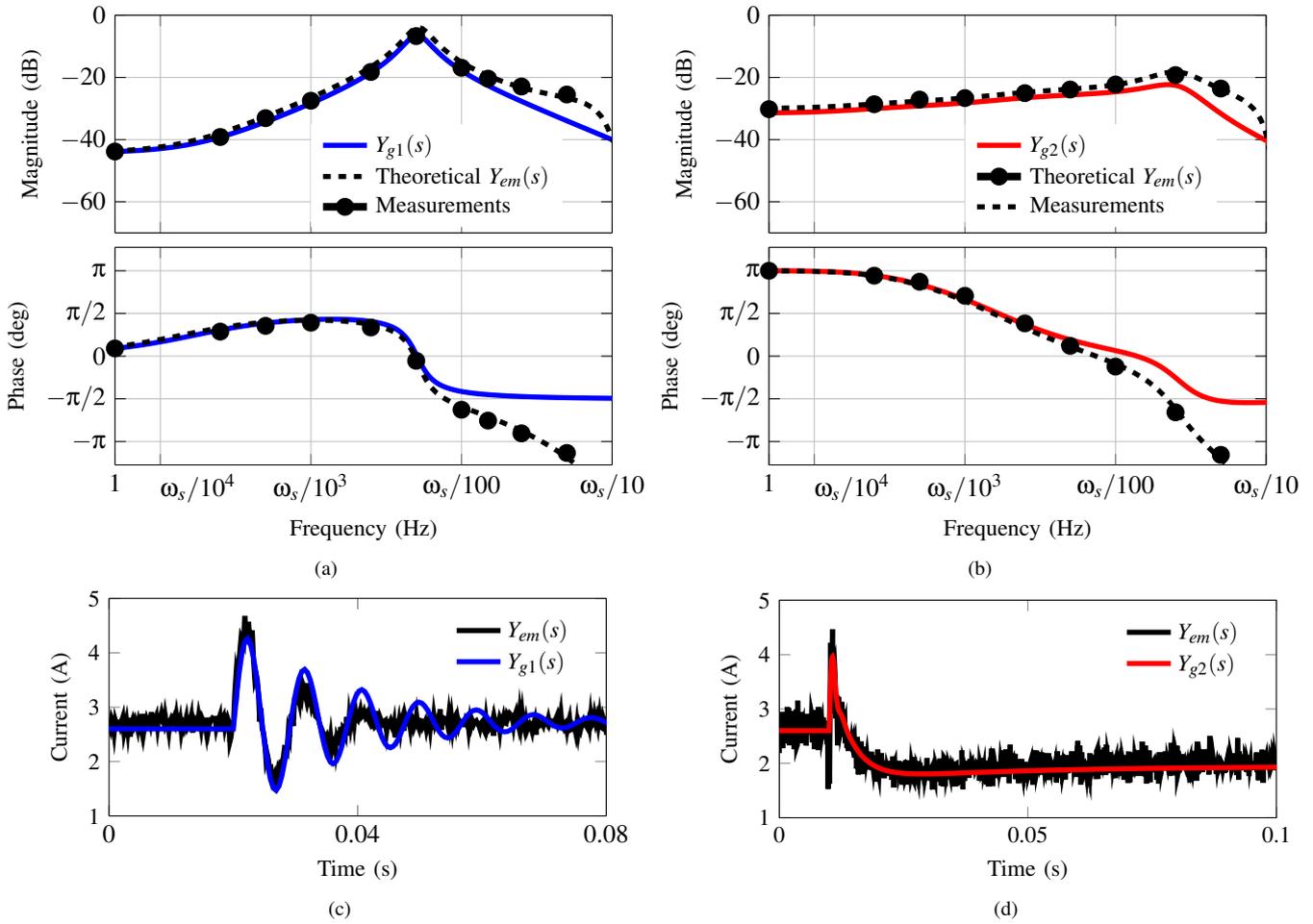


Fig. 7: Emulator admittance measurement tests. (a)-(b) Admittances measured in a specific set of frequencies. (c)-(d) Input voltage steps.

The frequency response of  $Y_{g2}(s)$  is shown in Fig. 6. It can be seen that at low frequencies, inside the controller bandwidth, the admittance effectively shows a CPL behaviour.

#### IV. EXPERIMENTAL VERIFICATION

A prototype, with the configuration shown in Fig. 2, has been build for the experimental verification of the proposed active dc grid admittance emulator. The physical parameters of the experimental setup are shown in Table II.

The dc grid is created by a REGATRON TopCon TC.ACS, used as controllable dc source, that has also been employed to introduce a perturbation in the dc voltage, in order to measure the emulator admittance in a pre-defined set of frequencies. The dc grid admittances, shown in Fig. 6, have been implemented as the objective admittances  $[Y_g(s)]$  in the control structure, shown in Fig. 2. The results from the experimental verification are shown in Fig. 7, as it can be seen, the results are in a good agreement with the theoretical analysis and modelling.

As expected from Fig. 3, there is a magnitude amplification of the objective admittances for frequencies above  $\omega_s/10$ . For the emulation of most grid admittances this is not an issue,

since in practise, the magnitude of grid admittance naturally tends to decrease as the frequency increases. This magnitude amplification is created by the current reference estimation used in this work  $[i_o^*(s) \approx i_s^*(s)/D]$ , see Fig. 2], since at high frequencies the term  $[d(s)I_o/D]$  start to be non-negligible.

The admittance of the emulator has been measured for an specific set of frequencies [see Figs 7(a) and 7(b)]. Since there is a maximum frequency at which the admittances can

Table II: Physical parameters used for the experimental validation.

Parameter	Value
Nominal Power ( $P_1$ )	1 kW
Nominal DC Grid Voltage ( $V_s$ )	400 V
Nominal Output Voltage ( $V_o$ )	200 V
Converter Inductor	$L = 14$ mH, $R = 1$ $\Omega$
PI regulator	$132(1 + 71.5/s)$
Switching frequency	20 kHz
Theoretical closed loop bandwidth	$2\pi 1500$ rad/s

be measure with the available hardware, a second set of experiment have been performed. Figs 7(c) and 7(d) show the response of the emulator for a dc voltage step ( $v_s$ ). It can be seen that the measured current responses well matches the theoretical ones.

## V. CONCLUSION

In this work a novel method for the active emulation of dc grid admittances has been proposed. A modified current control structure, that effectively establishes a relation between the input voltage and current responses, defined by a given grid admittance, is shown. The buck-based emulator is able to effectively emulate the objective grid admittances, nevertheless it has been seen that the emulation performance is inherently limited by the switching frequency.

As the results have shown, the analytical expressions derived, for the emulator admittance's, accurately matches the measurements. Also, both admittances' phases and magnitudes are well emulated within the bandwidth of the current controller. The delays introduced by the inner current control loop limit the emulation capability to one tenth of the switching frequency approximately, where the phase and magnitude errors start to be significant.

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