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Six-Step MMC-Based High-Power DC-DC Converter

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***Abstract*—Both DC collection and transmission grids have enjoyed a lot of popularity lately. In order to successfully take advantage of the benefits offered by DC systems, reliable connection between two networks of different voltage levels has to be obtained. This paper presents high step-down ratio, isolated DC-DC converter intended to connect high/medium voltage grid with a low voltage DC grid. Proposed converter combines two Modular Multilevel Converters in series at high/medium voltage side with conventional Six-Step Converter at low voltage side, interfaced by means of Three Winding Three-Phase transformer. Basic operating principles, along with design and sizing rules, are presented and supported by simulation results.**

***Index Terms*—HVDC, MVDC, Modular Multilevel Converter (MMC), High Power DC-DC Conversion**

I. Introduction

Steadily increasing electrical energy consumption demands have led to the need for the modern power systems to expand. However, limited ampacity of existing power lines is said to represent one of the most significant bottlenecks towards expanding power transfer capabilities of the existing systems [1]–[4]. High Voltage Direct Current (HVDC) systems have shown certain advantages over their High Voltage Alternating Current (HVAC) counterparts, some of which are reduced transmission losses, alleviated stability problems, no limitations in terms of distance at which the energy can be transferred through a line, etc. On the other hand, stringent ecological requirements have led to renewable energy resources proliferation. Consequently, HVDC transmission and Medium Voltage Direct Current (MVDC) distribution grids are expected to expand since they represent promising solutions for integration of renewable energy sources into the existing grid. Additionally, success of HVDC technology is expected to be replicated within Medium Voltage (MV) domain. Further, large off-shore wind power plants usually require MVDC connection with existing distribution grids due to higher transmission efficiency and lower overall system cost compared to AC systems [5], [6]. Additional advantage provided by the DC systems is the fact that bulky Low Frequency Transformer (LFT) can be replaced by smaller Medium Frequency Transformer (MFT), leading to high power densities and decreased system volume and weight.

Ideas of increasing power transfer capacity of existing AC power lines by converting them into DC, appeared during 1970s [1]. It was stated in [1] that conversion of an AC line into DC shows potential of power increase by the factor of almost 3.5. Having an AC line converted into DC might result in different line configurations [3], [4], however this paper focuses on converters operating within bipolar networks with neutral conductor.

Within the aforementioned systems, DC-DC power converter can be labeled as a key component providing the means for interfacing two DC networks of different voltage levels. However, certain requirements have to be met in order to provide reliable connection between two networks, some of which are high step-up/down voltage ratio, high efficiency, isolation due to safety reasons, redundancy, modularity, etc. Galvanic isolated power converters are quite often referred to as Solid State Transformers (SSTs). SST concept has been envisioned within AC grids a long time ago, however research interests including SST have only increased over time. So far, majority of SST configurations have involved multiple conversion stages connected by means of multiple MFTs, whereas this paper focuses on bulk power processing concept implying the existence of one single MFT in the isolation stage. Due to the fact that High Voltage (HV)/MV has to be handled at either side of the converter, Modular Multilevel Converter (MMC) is used.

MMC-based high power DC-DC converters have been subject to various research projects. In [6] MMC-based Single-Phase (1PH) Dual-Active Bridge (DAB) was proposed, with aim of obtaining electronic tap changer. However, problems with high voltage stress imposed on isolation stage, originating from instantaneous MMC cells insertion, had not been addressed. To overcome the aforementioned problems, Quasi Two-Level (Q2L) operation was proposed [7], [8]. Such an operation implies sequential insertion of MMC-alike cells in equidistant time steps within a fraction of fundamental converter operating period. On the other hand, topologies operating with sinusoidal currents within the isolation stage were also reported [9]. However, keeping HV/MV semiconductor devices switching frequency equal to MFT operating frequency tends to be quite challenging in these cases. Therefore, topologies operating similarly to conventional DAB were preferred by the authors. None of the aforementioned references has analyzed the employment of MMC-based DAB within bipolar DC grids with neutral conductor, where redundancy principle can be utilized providing suitable converter structure is chosen.

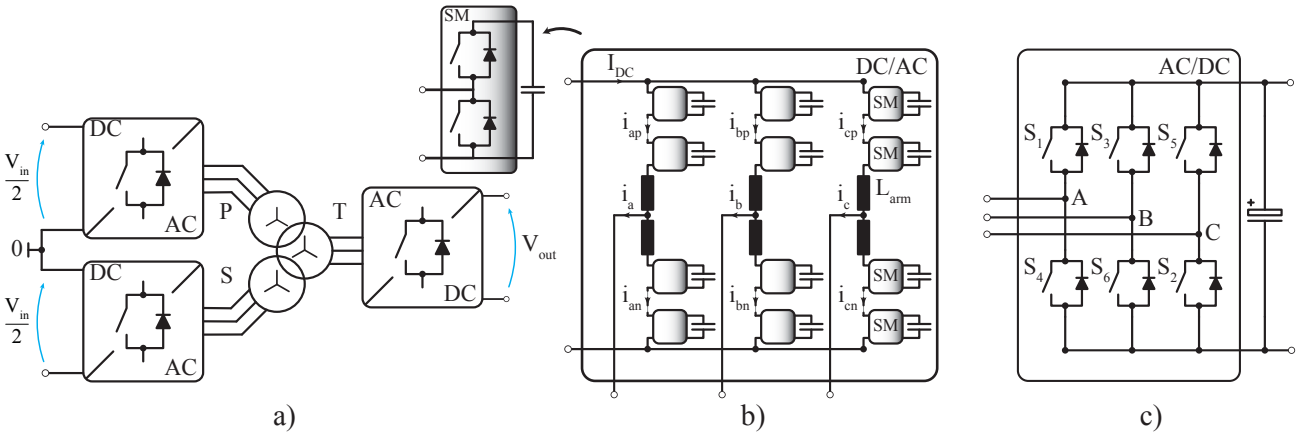

Figure 1: a) Proposed topology b) MV MMC stage c) LV Six-Step Converter

II. Converter structure

Fig. 1 presents the proposed topology consisting of series connection of two MMCs at HV/MV side and Six-Step Converter (SSC) at Low Voltage (LV) side. With aim of interfacing HV/MV grid, both MMCs employ Half-Bridge (HB) cells whose number depends on available HV/MV along with voltage class of semiconductors to be used. HV/MV and LV stages are interconnected by means of three winding Three-Phase (3PH) transformer. According to Fig. 1a, HV/MV side windings are referred to as primary (P) and secondary (S) windings, whereas LV side winding is referred to as tertiary (T) winding. Analyzed system ratings are presented in Tab. I. In order to maintain switching frequency within reasonable limits, both MMCs as well as SSC, operate in six-step mode. Therefore, in terms of operation principles, the proposed topology corresponds to 3PH DAB presented in [10]. LV side semiconductor devices switch at MFT operating frequency, thus creating the possibility for employing low conduction losses switching devices such as Insulated Gate-Commutated Thyristor (IGCT). In addition, Zero-Voltage Switching (ZVS), a property inherent to DAB within a restricted operating range, leads to reduction of converter switching losses. Another advantage offered by the proposed topology is its redundancy in case of failure of either MMC. On these terms, faulty MMC gets isolated from the rest of the circuit, whereas converter can continue to operate with half the rated power, without the need for system reconfiguration. The same applies if any of the voltage poles were to be lost.

SSC operates with square-wave voltages, therefore creating four level voltage waveform at transformer T-winding. However, driving HV/MV converter stage with square-wave voltages would have detrimental effect on transformer's insulation. Consequently, with aim of alleviating problems related to high dV/dt stress, MMC cells were inserted sequentially during the fundamental period fraction labeled with θ_d, as suggested by Fig. 2. Hence, voltage waveforms generated by MMC arms correspond to the ones introduced with Q2L converter [7], [8]. Another convenient feature offered by the sequential cells insertion is the ability to balance the MMC capacitor voltages since every cell receives different amount of charge depending on the time instant at which it receives the switching signal [11].

Table I: Analyzed system ratings

Input Voltage	V_{in}	± 20kV
Output Voltage	V_{out}	1.5kV
Rated Power	P	10MW
Operating frequency	f	400Hz

Primary and secondary MMCs are connected in series, nonetheless due to galvanic isolation, existence of transformer leakage inductance as well as MMCs' arm inductances, they are independent from each other. Hence, only one MMC can be analyzed, bearing in mind that obtained results apply for the other one providing converter operates with no faults.

Power flow analysis can be conducted using the circuit presented in Fig. 3a. In order to derive relevant equations, voltages V_{an}, V_{bn} and V_{cn} are the ones of interest. Voltages V_{si} generated at a MMC AC pole are defined by (1), where V_n and V_p denote MMC lower and upper arm voltages, respectively.

$$V_s = \frac{V_n - V_p}{2} \tag{1}$$

According to Fig. 1, maximum AC voltage generated by a single MMC branch equals $V_s^{max} = V_{in}/4$. Analyzing the circuit from Fig. 3a, along with Fig. 3b, voltage V_{an} can be calculated as (2), according to which its maximum equals

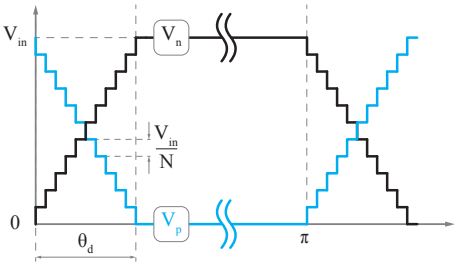

Figure 2: Sequential MMC cell insertion

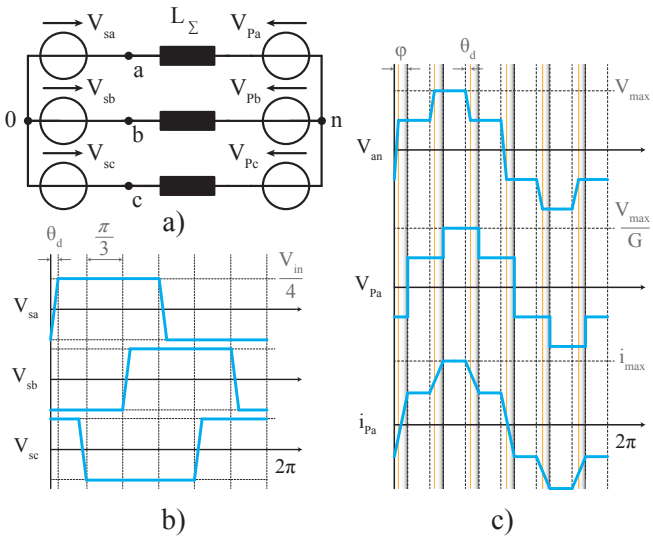

Figure 3: a) Equivalent circuit of one MMC connected to the MFT b) Voltages generated at MMC AC poles c) Idealized waveforms relevant for power flow analysis (G=1)

$V_{max} = V_{in}/3$. Even though MMC cells insertion occurs in discrete time instants, AC pole voltage waveform was linearized with aim of alleviating converter sizing procedure as well as relevant equations derivation. Normally, number of cells employed within a MMC-based system is quite high, therefore linearization should not significantly hinder precision of the obtained results. Further, transformer EMF seen from P/S side depends on its turns ratio m_t. Ratio $G = V_{in}/2m_tV_{out}$ can be referred to as converter voltage gain. It can be shown that this parameter plays a major role in defining converter current shape, as well as that it does not necessarily have to be equal to one. Fig. 4 presents the influence of converter voltage gain G on MMC arm currents. Phase A of both MMCs will be observed. At time instant $t = 0$ upper arm of the observed phase ramps its voltage down. In order to achieve ZVS, prior to switching an IGBT on, its free-wheeling diode needs to conduct. Therefore, MMC upper arm current needs to remain negative in order to achieve ZVS for all the cells within an arm. It can be seen Fig. 4 that the higher the converter voltage gain, the more negative the MMC arm current at time instant $t = 0$.

Relevant per-phase voltage and current waveforms are presented in Fig. 3c. Similarly to conventional DAB, adjustment of the phase angle φ between voltage V_{an} and transformer EMF denoted by V_{Pa}, enables the control of power at which the energy is transferred through the converter. Observing given waveforms, power equation for either MMC can be derived (3), whereas full power of the system can be obtained by multiplying derived expression by two. In (3) MFT operating frequency was denoted by f, whereas L_Σ accounts for the sum of transformer leakage inductance, half the MMC arm inductance and, eventually added, external inductance.

$$V_{an} = \frac{2V_{sa} - V_{sb} - V_{sc}}{3} \tag{2}$$

$$P_{mmc} = \frac{V_{in}^2}{3\omega L_\Sigma G}\left\{\varphi\left(\frac{1}{2} - \frac{3\varphi}{8\pi}\right) - \frac{\theta_d^2 + (2\pi - 3\varphi)\theta_d}{8\pi}\right\} \tag{3}$$

It is noteworthy that MMCs' phase-shifts can be controlled separately due to the fact that they operate independently.

III. System Sizing

In order to ensure proper converter operation, passive components such as MMC cell capacitances, arm inductances, output capacitor as well as transformer turns ratio have to be correctly determined. However, sizing procedure depends on converter nominal operating points such as phase angle φ, voltage gain G, arm voltage ramp-up time described by angle θ_d, etc.

Firstly, reasonable range of the angles φ and θ_d should be discussed. Converter operation was simulated employing 3.3kV rated IGBTs. Considering that MMC cell rated voltage should be around 55% of employed semiconductors voltage class, one might calculate that number of cells per MMC arm equals $N = 20kV/(0.55 \cdot 3.3kV) \approx 11$, according to Tab. I. Considering standard dead times of devices falling into this

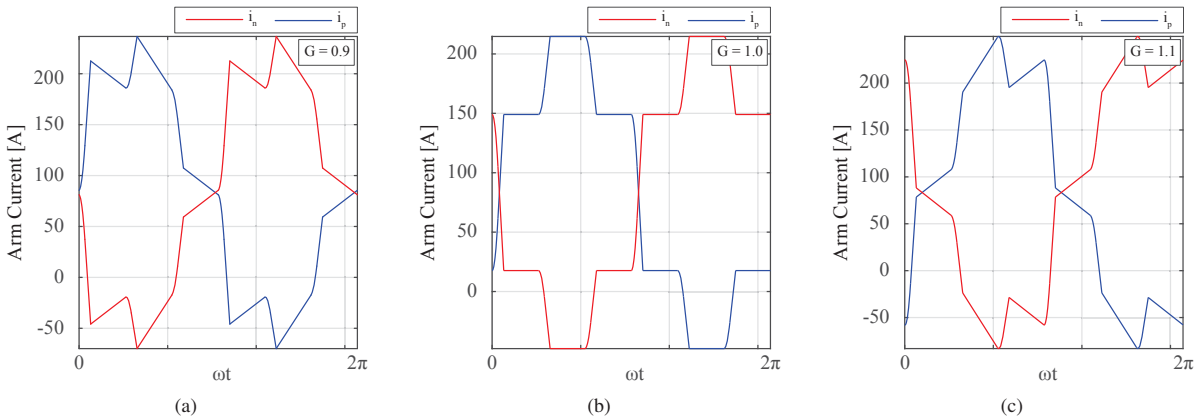

Figure 4: Influence of converter voltage gain G on MMC arm currents. It can be seen that the higher the gain G the lower the upper arm current at time instant t=0. Therefore, ZVS conditions might be provided for the HV/MV side devices.

voltage class being around 5μs, it can be assumed that ramp-up time of an arm voltage equals 50μs at least. If converter operating frequency was set too high, possibility that arm voltage ramp-up time would be higher than nominal phase angle would exist. With aim of avoiding such a phenomenon so that converter operation resembles conventional DAB as much as possible, operating frequency was set as 400Hz. Therefore, angle θ_d equals approximately 7.2°. This leaves the possibility to set nominal phase angle φ as 15°, which is expected to provide solid output voltage regulation flexibility while keeping AC stage reactive power moderate. With aim of achieving ZVS at HV/MV side, converter voltage gain was set as G=1.1. Tab. II summarizes the design of passive components used for system simulations.

A. Arm inductor design

MMC arm inductors were sized so that power transfer can be controlled without the need for adding any external inductances in series with the MFT, while providing the possibility to limit converter common-mode currents ripple. It was assumed that MFT leakage inductance can be considered negligible compared to the MMC arm inductance. Once the nominal power, nominal phase angle, voltage gain, and arm voltage ramp-up time are known, arm inductance can be determined using (3).

B. Output capacitor design

Output capacitance was determined so to improve converter dynamic response during abrupt load changes, as well as to alleviate output voltage oscillations originating from the SSC output current nature. It was reported in [12], [13] that phase angle abrupt changes should be treated properly in order to avoid SSC current offset and oscillations. However, methods proposed in [12], [13] rely on the prevention of phase angle change during a fraction of fundamental converter operating period. Hence, if abrupt load change occurred during the period at which the phase angle change is forbidden, output voltage drop has to be prevented by determining output filter capacitance properly.

The most critical case can be perceived as the abrupt full load connection to the converter LV bus in the time instant at which output voltage sampling occurred slightly prior to the load connection. It will be assumed that phase-angle changes will be forbidden until the next sampling instant, leaving the system operating as if no load was connected (namely, no power is transferred through the converter). Therefore, until the next sampling instant, energy demanded by the load must be supplied by the output capacitor. Allowed voltage drop, system sampling time and reference output voltage were denoted as ΔV, T_{samp} and V_{ref}, respectively. Unless converter starts providing the load with current, system can be modeled as a simple RC circuit, at which capacitor initial voltage equals V_{ref}. Hence (4), can easily be derived.

$$C_{out} \geq -\frac{T_{samp}P_{nom}}{V_{ref}^2 ln\left(1-\frac{\Delta V}{V_{ref}}\right)} \tag{4}$$

C. MMC cell capacitance design

MMC cells voltage balancing method presented in [11] was used. Consequently, every cell was inserted/bypassed with duty cycle matching 0.5, however instants at which switching signals were passed to the cells differed by $\beta_d = \theta_d/(N-1)$. In order to perform MMC capacitor sizing, converter current waveforms need to be known. Suitable current waveform integration leads to amount of charge which causes MMC cell voltage ripple. Cell capacitance can be chosen according to desired voltage ripple caused by arm current flowing through it providing the cell is inserted into the circuit.

D. Transformer turns ratio determination

As already mentioned, converter voltage gain G can be chosen different to unity in order to provide conditions for ZVS at HV/MV side. It can be shown that, on these terms, converter voltage gain should be greater or equal to some value G^* (however, this analysis falls out of this paper scope). Having this constraint as well as voltage gain definition in mind, transformer turns ratio can be determined as (5).

$$m_t = floor\left[\frac{V_{in}}{2V_{out}G^*}\right] \tag{5}$$

Table II: Passive components design

MMC arm inductance	L_{arm}	7.2mH
Submodule capacitance	C_{sm}	1mF
Output capacitance	C_{out}	12mF
Number of MMC cells per arm	N	11
Transformer turns ratio	m_t	12

IV. Overall converter control

Observing the topology depicted in Fig. 1, it can be concluded that output voltage can be controlled by means of SSC output current, whose mean value can be derived from (3) if system losses were neglected. However, power equation is nonlinear, therefore linearization might be performed with aim of relieving system computational burden. Taking system ratings from Tab. I into account, power equation (3) can be linearized around nominal phase shift. However, it can be shown that linearization around $\pi/6$ does not significantly hinder power calculation precision, leading to (6).

$$\varphi = \frac{1}{A}\left(\frac{V_{out}\overline{i_R}^*}{2} + B\right) \tag{6}$$

where

$$A = \frac{V_{in}^2}{48\omega LG\pi}\left(6\theta_d + 7\pi\right)$$
$$B = \frac{V_{in}^2}{24\omega LG\pi}\left(\theta_d^2 + 2\pi\theta_d\right)$$

As presented in Fig. 5, output voltage is sensed and fed through the Low-Pass Filter (LPF) in order to diminish the influence of higher order harmonics on the regulation loop. Error signal is forwarded to PI regulator, whereas directly measurable output current is used as a feed-forward in order to

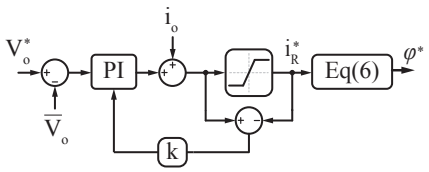

Figure 5: Output voltage control structure

keep regulator actions moderate and therefore improve system dynamic response. SSC mean current reference $\overline{i_R}^*$ is passed to the block which extracts reference phase shift according to (6). Thereafter, phase shift information is being used by modulator which generates switching signals for both MMCs, as well as SSC.

V. Simulation Results

Previously discussed system was simulated in PLECS and steady state results are presented in Fig. 6. System was controlled so that output voltage remains equal to the reference value defined in Tab. I. To avoid abrupt output power changes, which might lead to either instabilities or require oversizing the output capacitor, full load (10MW) was applied sequentially in time steps of 0.75s. Firstly, half the rated load was connected to the LV bus at time instant denoted by t_1, whereas the other half was connected 0.75s after, at time instant denoted by t_2. It can be seen from Fig. 6 that control system manages to maintain the output voltage V_o at desired reference. At time instant denoted by t_3, ideal current source with current ramping-up from zero to twice the nominal output current over the period of 0.25s was connected to the LV bus in order to inspect converter behavior in case the energy needs to be routed in the opposite direction. It can be seen from Fig. 6 that converter output current i_o changes according to the ramp-up time of the ideal current source connected to the LV bus.

Fig. 7 presents converter operating waveforms under full load during four fundamental periods. It can be seen that output voltage V_o consists of mean value being equal to the reference defined by Tab. I along with ripple occurring at six times converter operating frequency. As expected, SSC output current i_{SSC} proves to behave the same. Transformer P, S and T winding currents (i_{Pi}, i_{Si} and i_{Ti}, respectively) are of the same shape, which is logical considering that both MMCs were controlled so that powers delivered to the LV side match. Steady state MMCs' input currents i_{in1} and i_{in2} consist of mean value with small ripple originating from the ripple over MMC cell capacitors superimposed. Neutral conductor current i_n can be neglected, however during faults it is actually the neutral conductor which is going to overtake the current of the faulty voltage pole (MMC). However, one might also notice that, even thought they are symmetrical, transformer currents shape slightly differs compared to the ideal 3PH DAB due to the fact that voltage gain G was selected different than unity with aim of achieving ZVS at the HV/MV side.

Fig. 8 presents MMC arm currents, which consist of a DC component along with half the transformer current. Owing to the fact that transformer's currents sum up to zero, as well to the existence of a DC component in MMC arm currents, one might conclude that, in steady state, MMC input current should be flat ideally. Therefore, filtering capacitors in the HV/MV stage can be omitted.

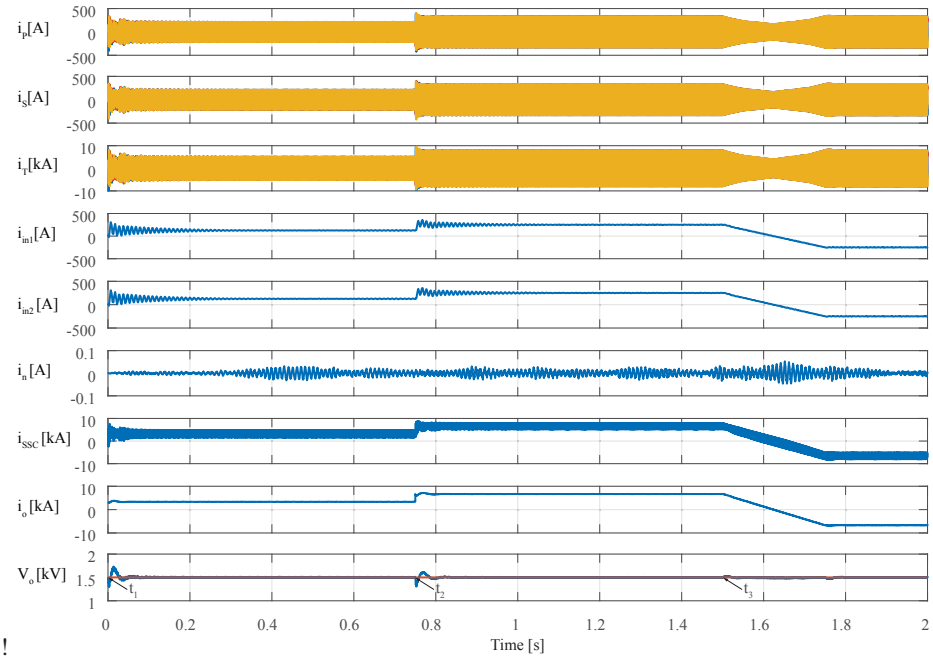

Figure 6: Converter operating waveforms after stepwise load changes ($t = t_1$) and ($t = t_2$) as well as power reversal ($t \geq t_3$)

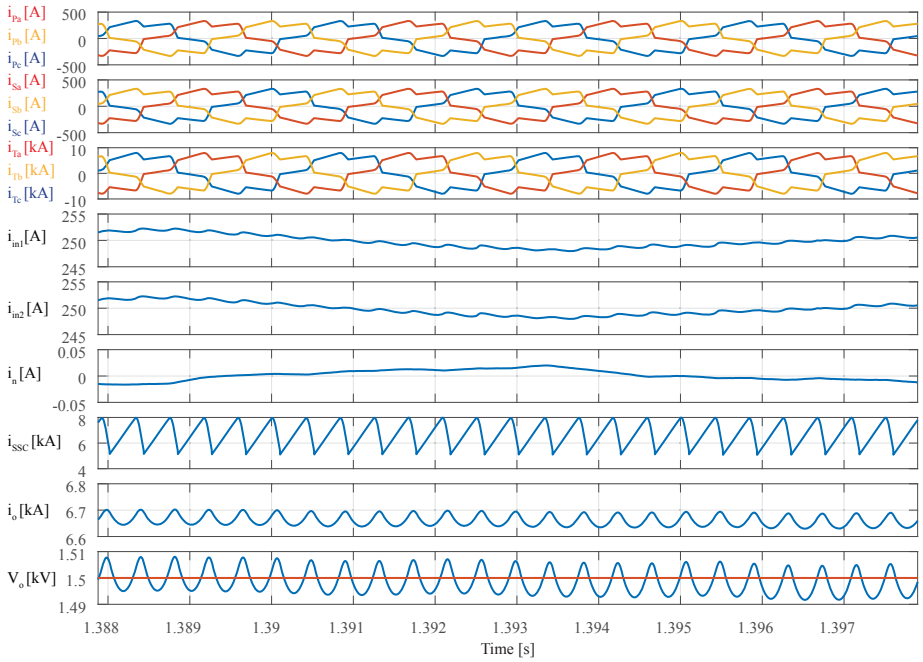

Figure 7: Converter operating waveforms under full load during four fundamental periods

Fig. 9 presents voltages across a MMC arm over several fundamental periods. It can be seen that voltage ripple equals around 3% of a cell nominal voltage. Moreover, zoomed part of the graph indicates that switching pulses were indeed delayed with respect to each other by $\beta_d = \theta_d/(N-1)$.

In order to verify that HV/MV side devices experience ZVS, Fig. 10 depicts currents of upper (i_H) and lower (i_L) switches within an upper arm of either MMC. If converter voltage gain G was correctly determined, all the switches within an arm should experience ZVS, meaning that during the arm voltage transition period, determined by the angle θ_d, observed arm current should remain negative. A cell being inserted into the circuit first was labeled as "Cell 1", whereas the one being inserted the last was labeled as "Cell 11" (please notice that gate signal was multiplied by 100 for the sake of presenting the analyzed situation on a single graph). When MMC upper arm cells receive inserting signal, current should divert from lower switches to the upper ones. In order to achieve ZVS, free-wheeling diode of the upper switch should start conducting during the dead-time interval, which means that upper switch current should be negative, which is easy to verify from Fig. 10. On the other hand, when an upper arm gate signal equals zero, lower arm cells get inserted into the circuit. Once again, observed arm current has to be negative in order to achieve ZVS. It can be seen from Fig. 10 that for both the first and the last cell inserted into the lower arm, its current is still negative, meaning that ZVS is obtained for both MMC arms.

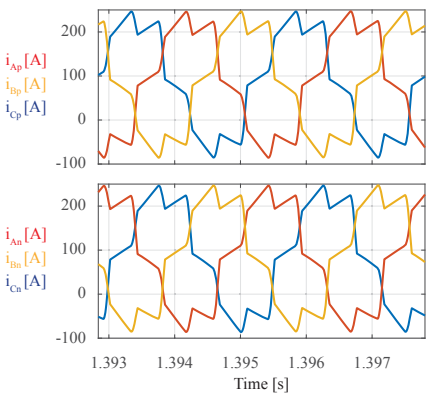

Figure 8: MMC arm currents

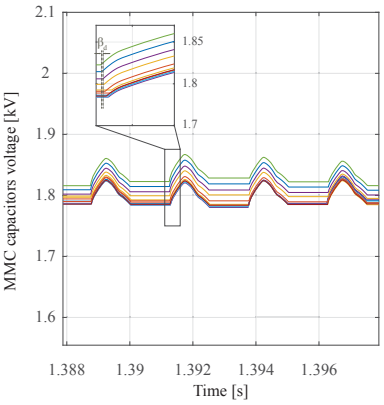

Figure 9: MMC arm capacitors' voltage

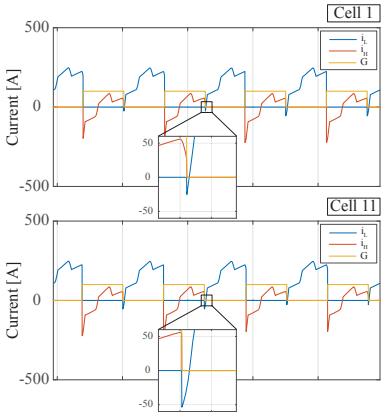

Figure 10: MMC arm current

VI. Conclusion

This paper proposed six-step MMC-based high power DC-DC converter intended for connection of HV/MV bipolar grid with LV DC grid. In order to provide the possibility to successfully utilize redundancy principle inherently offered within bipolar grids with neutral conductor, proposed converter employs Three Winding 3PH transformer. Both converter stages operate at MFT operating frequency, therefore reducing switching losses and providing the means for system operating frequency increase with respect to conventional AC systems. Operating principles resemble the ones introduced with the appearance of the DAB. Additionally, correct determination of transformer turns ratio can provide soft switching at both converter stages.

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