2kV slanted tri-gate GaN-on-Si Schottky barrier diodes with ultra-low leakage current

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Citation: Appl. Phys. Lett. 112, 052101 (2018); doi: 10.1063/1.5012866
View online: https://doi.org/10.1063/1.5012866
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Published by the American Institute of Physics

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High-voltage rectifiers are crucial in nearly every topology of power converters, and GaN-on-Si Schottky barrier diodes (SBDs) are highly promising for such applications due to their superior performance and competitive cost.\(^{1-8}\) Moreover, they are lateral devices and can be monolithically integrated with GaN-on-Si transistors and circuits, which is highly desirable for future compact and efficient power converters.\(^{9,10}\)

Despite these advantages, a major obstacle for GaN-on-Si SBDs is their limited voltage-blocking performance. Efficient power devices must present high \(V_{\text{BR}}\) and small \(I_R\), which are however very challenging in GaN SBDs. First, the \(I_R\) in GaN SBDs is typically large, being dominated by many non-ideal effects that are very difficult to eliminate, such as tunneling.\(^{11}\) Second, although a small Schottky barrier (\(Q_B\)) leads to a small \(V_{\text{ON}}\), it also increases the \(I_R\), and thus, there is a natural trade-off between good ON- and OFF-state performances. Finally, the lateral current conduction in GaN SBDs results in an inhomogeneous distribution of the electric field, which severely limits their \(V_{\text{BR}}\),\(^{12,13}\) despite the resistivity of their buffer layers. Consequently, the poor voltage-blocking capability in GaN-on-Si SBDs is usually limited by the device architecture, rather than their buffer layers. As an example, the voltage-blocking performance of GaN-on-Si SBDs is still much inferior than that of GaN-on-Si transistors, even though they share the same material platform. While GaN-on-Si power transistors have been commercialized for applications up to 650 V, GaN-on-Si SBDs for such ratings are still missing.

In this work, we demonstrate that high-performance GaN-on-Si power SBDs with superior voltage-blocking capabilities (2 kV at 1 \(\mu\)A/mm) can be achieved with a judicious device design, by integrating hybrid tri-anode (TA) and slanted tri-gate (TG) architectures. The hybrid tri-anode reduced the \(I_R\) by controlling the \(V_{\text{SCH}}\) with the width of its nanostructures (w), resulting in an ultra-low \(I_R\) of 51 \(\pm\) 5.9 nA/mm at −1000 V and in a small \(V_{\text{ON}}\) of 0.61 \(\pm\) 0.03 V. The slanted tri-gate provided a continuous gradient of pinch-off voltage (\(V_p\)) from the anode towards the cathode, spreading effectively the electric field in OFF state, leading to a record \(V_{\text{BR}}\) of 2 kV at 1 \(\mu\)A/mm. These results establish a milestone for GaN power devices and could lead to enormous opportunities for future monolithic GaN power circuits.

The \(\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}\) heterostructure in this work was grown on a silicon substrate with 5 \(\mu\)m-thick buffer layers. The fabrication of the slanted tri-gate SBDs (Fig. 1) started with e-beam lithography to define the nanostructures in the anode, which were etched by inductively coupled plasma with a depth of \(\sim\)180 nm. The width (w) and spacing of the nanostructures in the tri-gate and tri-anode regions were 200 nm and 400 nm, respectively, while the \(w\) in the slanted tri-gate region increased continuously from 200 nm to 600 nm.
towards the cathode. The devices were isolated by mesa etching, and the cathode ohmic contact was formed by alloying Ti/Al/Ti/Ni/Au at 830 °C. Then, 10 nm SiO2 and 10 nm Al2O3 were deposited by atomic layer deposition and selectively removed in the tri-anode region. Finally, the anode contact was formed with Ni/Au. The oxide in the access and ohmic regions was removed by wet etching, which did not affect the Ir in this work. The length of the planar (LFP), slanted tri-gate (LsTG), tri-gate (LTG), and tri-anode (LTA) regions was 1.3 μm, 0.7 μm, 0.5 μm, and 4 μm, respectively (Fig. 1). All current values in this work were normalized by the width of the device footprint (60 μm).

The schematic and equivalent circuit of the nanostructured anode are shown in Figs. 2(a) and 2(b), respectively. It consists of a tri-anode SBD connected in series with a tri-gate, a slanted tri-gate, and a planar-gate transistor. The main idea is to design the distribution of potential along the gate, a slanted tri-gate, and a planar-gate transistor. The value of the pinch-off voltage (Vpinch) of the each type fabricated on a control sample with 20 nm Al2O3 as the oxide.

1. The tri-anode (TA) was designed for small VON, and low IR. In ON state, the metal contacts the 2DEG channel in the SBD under a large reverse bias. (c) Averaged absolute value of the pinch-off voltage (Vp,p) as a function of the width (w) of the nanowires in tri-gated AlGaN/GaN structures, determined from about eight devices of the each type fabricated on a control sample with 20 nm Al2O3 as the oxide.

2. The tri-gate region (TG) was inserted to shield the tri-anode, since the TA is vulnerable to high electric fields, which are concentrated at its cathode-side edge, and can lead to large IR and even early breakdown of the device. By connecting the TG in series with the TA, the voltage drop at the cathode-edge of the TA (VTA) is pinned at [Vp,TG - Vp,TA] [Fig. 2(c)], which can be also reduced with a smaller w [Fig. 2(d)], when w is below 1 μm, shielding the TA from large reverse biases. More details about the impact of the w on device characteristics can be found elsewhere.

3. The slanted tri-gate (sTG) was included to enhance the VBR. It was patterned with a slanted w, increasing towards the cathode. Since the [Vg] in a tri-gate MOS structure reduces with smaller w [Fig. 2(d)], the sTG works as many incrementally stepped field plates (FPs) with a continuous gradient of [Vp,sTG] increasing towards the cathode. As a result, the electric field is spread along the entire sTG, which significantly improves the VBR [Fig. 2(c)], similarly to conventional slanted FP, but with the advantage of a much easier and more controllable fabrication by simply tuning the w lithographically in a single step.

4. The long planar region (P) works as a planar FP to further improve the VBR, since the Vp of the planar region (Vp,P)
is more negative with respect to the most negative value of the $V_{p+SG}$.6,17

The slanted tri-gate SBDs presented very good ON-state performance as shown in Fig. 3(a), despite the partial removal of the 2DEG in the anode. The ON-resistance ($R_{ON}$) was 13.9 ± 1.3 Ω mm and 22 ± 2.9 Ω mm at room temperature for devices with $L_{AC}$ of 15 µm and 25 µm, respectively, and increased to 27.6 ± 2.9 Ω mm and 37 ± 1.8 Ω mm at 150°C. The $V_{ON}$ was as small as 0.61 ± 0.03 V [Fig. 3(b)], determined at 1 mA/mm. The ideality factor ($n$) was 1.40 ± 0.02 at room-temperature (RT) and reduced to 1.27 ± 0.01 at 150°C [inset in Fig. 3(b)], indicating the high quality of the sidewall Schottky contacts despite the etching.

In OFF state, the $I_R$ of the slanted tri-gate SBDs was saturated after the pinch-off of the tri-anode at about −1.7 V [the inset in Fig. 3(c)] due to the fixed $V_{SCH}$, which was not affected by $L_{AC}$, and thus, the $I_R$ was nearly constant at 5.5 ± 1.8 nA/mm until −650 V and did not reach 10 nA/mm until −830 V [Fig. 3(c)]. Extremely low $I_R$ of 51 ± 5.9 nA/mm was observed at −1000 V, which is significantly smaller than in any other reports of GaN-on-Si SBDs. For voltages below −900 V, there was no significant difference in $I_R$ measured with floating and grounded substrates. From RT to 150°C, the $I_R$ increased by only ~50 nA/mm [inset of Fig. 3(d)], and at 150°C, the $I_R$ at −200 V was as small as 57 ± 13 nA/mm [Fig. 3(d)]. This is the smallest $I_R$ among reported lateral GaN SBDs at such high temperature.

In addition to their small $V_{ON}$ and ultra-low $I_R$, the slanted tri-gate SBDs also presented high $V_{BR}$ [Fig. 4(a)]. With floating substrate, the $V_{BR}$ at 1 µA/mm was −1450 V and −2000 V, and the hard breakdown was −1500 V and −2500 V for devices with $L_{AC}$ of 15 µm and 25 µm, respectively, corresponding to a critical breakdown field of 1 MV/cm (extracted from the hard breakdown voltage versus $L_{AC}$). With grounded substrate, the $V_{BR}$ at 1 µA/mm for both $L_{AC}$ was about −1060 V, while the hard breakdown was up to −1200 V, which is comparable to current 650 V-rated GaN-on-Si power transistors18–21 and is limited by the vertical breakdown of the buffer layers.22 These results indicate that the 15 µm-$L_{AC}$ SBDs can fulfill the voltage-blocking requirements of 600/650 V applications, even for those requiring grounded substrate connection, and the 25 µm-$L_{AC}$ SBDs can be used for 1200 V applications (with floating substrate connection)25 both providing a safety margin in breakdown of about 100% (from the rated voltage to the hard breakdown).

Figure 4(b) shows the C-V measurement characteristics of the slanted tri-gate SBDs plotted along with the $I_R$. The slanted tri-gate SBDs presented ultra-low $I_R$, because their $V_{SCH}$ was pinned and the $I_R$ saturated at the pinch-off of the tri-anode, at about −1.7 V [Fig. 4(b)], instead of increasing exponentially with the voltage. This decouples the $I_R$ from the $V_{ON}$, allowing an independent design of the forward and reverse performance of the SBD, which is a major feature of this architecture. The high $V_{BR}$ of the slanted tri-gate SBDs was due to the better-distributed electric field along the device. The discontinuity of the $C$ in the slanted tri-gate region [sTG + TG region in Fig. 4(b)] indicates a gradual depletion of the channel with increasing reverse bias, due to the gradient of $V_p$, which spread effectively the electric field and greatly improved the $V_{BR}$. Such an effect is similar to conventional slant FPs23 but observed here with a more precise and controllable way of tuning the $w$ lithographically, instead of the complex sloped etch of the FP oxide.

The slanted tri-gate SBDs are also promising for fast switching, due to their small capacitive charge ($Q_C$) of 0.263 ± 0.13 nC/A [inset of Fig. 4(b)], which is comparable to or below reported values for fast-switching GaN power SBDs on Si (0.415 nC/A)24 and SiC (0.213 nC/A)25 substrates. The switching time estimated from $Q_C^2$ was ~263 ps, which is about 25% shorter than that of conventional high-voltage GaN SBDs with double FPs.4

The high performance of the slanted tri-gate SBDs makes them excellent power rectifiers (Fig. 5), presenting...
the highest \( V_{BR} \), the lowest \( I_R \) of 5.5 \( \pm \) 1.8 nA/mm at \(-650 \text{ V}\) (or \(\sim 0.1 \mu\text{A at }-1200 \text{ V}\)), a small \( V_{ON} \) of 0.61 \( \pm \) 0.03 V, and an excellent high-power figure-of-merit up to 1.16 GW/cm\(^2\), as compared with existing GaN-on-Si power diodes with conventional technologies, rendering a breakthrough for the family of GaN-on-Si power devices.

In conclusion, in this letter, we presented 2 kV GaN-on-Si power SBDs by 3-dimensional integration of slanted tri-gate and hybrid tri-anode architectures. The hybrid tri-anode allows an independent design of the forward and reverse performances of the SBD, resulting in an ultra-low \( I_R \) and a small \( V_{ON} \). Together with the slanted tri-gate, a high \( V_{BR} \) of \( \sim 2000 \text{ V at }1 \mu\text{A/mm} \) was achieved, yielding a significant breakthrough from existing technologies. The approach presented in this work demonstrates a pathway to achieve high-voltage power SBDs and opens enormous opportunities for future monolithic GaN power converters.

This work was supported in part by the European Research Council under the European Union’s H2020 program/ERC Grant Agreement No. 679425 and in part by the Swiss National Science Foundation under Assistant Professor Energy Grant No. PYAPP2_166901.