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N. Hildebrandt, M. Petkovic, and D. Dujic

POWER ELECTRONICS LABORATORY
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

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Nicolai Hildebrandt, Marko Petković and Dražen Dujić
Power Electronics Laboratory - PEL
École Polytechnique Fédérale de Lausanne - EPFL
Station 11, CH-1015 Lausanne, Switzerland
nicolai.hildebrandt@epfl.ch, marko.petkovic@epfl.ch, drazen.dujic@epfl.ch

***Abstract*—High fidelity AC grid emulators allow early testing and qualification of various equipment under conditions close to those expected in reality. Realizing this at medium voltage high power level is associated with certain challenges, some of which are discussed in this paper. Medium voltage grid emulator based on the well-known four-quadrant Robicon topology is considered as platform for realization of the AC grid emulator. To achieve high resolution AC waveform with sufficiently high control bandwidth, SiC based cell design is compared with pure Si and Hybrid (Si+SiC) designs. Using SiC devices for the output H-bridge stage allows significantly higher switching frequencies, improving achievable control bandwidth and improving fidelity of emulator output voltage.**

***Index Terms*—Grid Emulator, CHB, SiC**

I. Introduction

Over the last two decades the use of distributed energy power generation increased rapidly. This led to growing concerns regarding grid stability and therefore tightened requirements found their way into standards and into codes issued by the grid operators. At the same time, advancements in power semiconductor technology and digital signal processing enabled researchers to build novel high-power electronic systems, like solid-state transformers, which bring additional capabilities to directly improve the medium-voltage grid stability and power quality.

Testing of grid-connected inverters from early stages of research and development to final qualification for compliance with standards requires test benches that can emulate normal and abnormal grid conditions. These are typically deviations in voltage amplitude, symmetry, frequency, phase angles, content of harmonics and sudden faults of the grid. The complexity of such a test bench can range from shunt inductors and tapped autotransformers to emulate voltage sags over series injection of voltage harmonics and programmable voltage sources [1] to power-hardware in-the-loop (PHiL) systems [2]. In PHiL systems the programmable voltage source is controlled by a real-time grid model simulation which reacts to the behavior of the equipment under test (EUT). In general, power electronics based solutions are most flexible regarding test scenarios and waveforms.

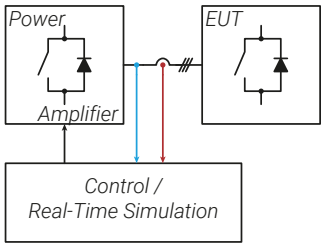

Fig. 1: Grid Emulator Setup

Depending on the testing purpose and depth, a programmable voltage source or a PHiL system can be used as a grid emulator. Both have in common a power amplifier (PA) unit which generates the emulated grid voltage and sinks or sources the currents delivered or consumed by the EUT as illustrated in Fig. 1.

While at low-voltage level linear voltage sources can be used as PA to create high precision, high dynamics and low noise waveforms, their losses are not permissible for test benches at high-power medium-voltage level. Switch-mode power converters, however, introduce harmonics around their switching frequency which can influence the EUT. The typical second order output filters used to mitigate this harmonic distortion for their part can limit the output dynamics of the PA if their cut-off frequency is low. Moreover, in order to be able to impose the desired grid voltage on the PA to EUT interface, the grid emulator needs a higher bandwidth than the EUT. These requirements can be addressed by a sufficiently increased switching frequency, which is a challenging endeavor if the PA is rated for high power.

Main approaches to reach higher switching frequency and dynamics in this case are series voltage injection by a second inverter [3][4], interleaved parallel operation of inverters or phases [5][6] and multilevel inverters. The latter offer a higher apparent output switching frequency than their two- or three-level counterparts with the same output voltage and power rating. A high number of levels can be achieved with modular cell based inverters. While the use of modular multilevel converter (MMC) has been demonstrated in [7], this work

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considers the use of the Cascaded H-Bridge (CHB) converter [8][9] with four-quadrant (4Q) cell design. Advantages offered by Silicon Carbide (SiC) devices are compared with more common Silicon (Si) based solutions.

II. CHB Based Grid Emulator

The grid emulator shall generate a precisely controllable voltage from zero to full line voltage of $6\,\mathrm{kV}$ ac with various types of grid voltage disturbances: symmetrical and unbalanced voltage sags, swells, harmonic disturbances, frequency and phase angle variations with up to $1\,\mathrm{MVA}$ output power at $50\,\mathrm{Hz}$ nominal fundamental frequency.

Emerging conversion structures such as solid state transformers or even established MMCs, push the required switching frequencies to higher values. Typical switching frequencies of state-of-the-art drives below $1\,\mathrm{MVA}$ stay below $5\,\mathrm{kHz}$, thus having a 5 times higher bandwidth and switching frequency should provide sufficient flexibility for tests.

In case of voltage harmonics injection up to 25^{th} harmonic, which is the highest harmonic explicitly defined in EN 50160 [10], the calculation can be as following in closed-loop control case: If an LC output filter is used, an order of magnitude frequency distance should be kept between the resonance frequency and the desired harmonic frequency to limit the effects of the phase-shift introduced by the filter. The switching frequency then should be at least 4 times higher than the resonance frequency, depending on the control method used, which is at least $50\,\mathrm{Hz} \cdot 25 \cdot 10 \cdot 4 = 50\,\mathrm{kHz}$ or even $100\,\mathrm{kHz}$ to damp the switching ripple to less than $1\,\%$. As such a high switching frequency is hard to be reached with Si devices, SiC devices are naturally considered as a feasible approach, despite their higher cost.

Finally, the impact on the grid that supplies the grid emulator shall be kept low in terms of input current power factor and distortion both in stationary operation and during transients at the grid emulator output.

The CHB topology shown in Fig. 2 is well-established in medium-voltage applications. Most of the produced high-power CHB converters are non-regenerative, i.e. their cells have a diode front-end, and operate in drive applications with low demand on dynamics like fans or pumps. This makes the design and control of the cells simple and cost-effective.

The output terminals of N low-voltage cells are connected in series to give a multilevel medium-voltage phase voltage which can directly be applied to a machine. Typically, phase-shifted carrier PWM (PSC-PWM) [11] with carrier frequency between 400 and $1000\,\mathrm{Hz}$ is used as it evenly distributes the switching and conduction losses among all the silicon IGBT (Si IGBT) switches of the inverter H-Bridge (HB) stages. This increases the apparent switching frequency seen at the output as $N \cdot f_{\mathrm{sw,cell}}$.

In applications where regenerative breaking is economically sensible, the diode front-ends are replaced or extended by silicon IGBT based Active Front-Ends (AFEs) with switching frequencies from $1.25\,\mathrm{kHz}$ [12] to $10\,\mathrm{kHz}$ [13]. Transformer secondary windings are shifted by multiples of $60°/N$ to

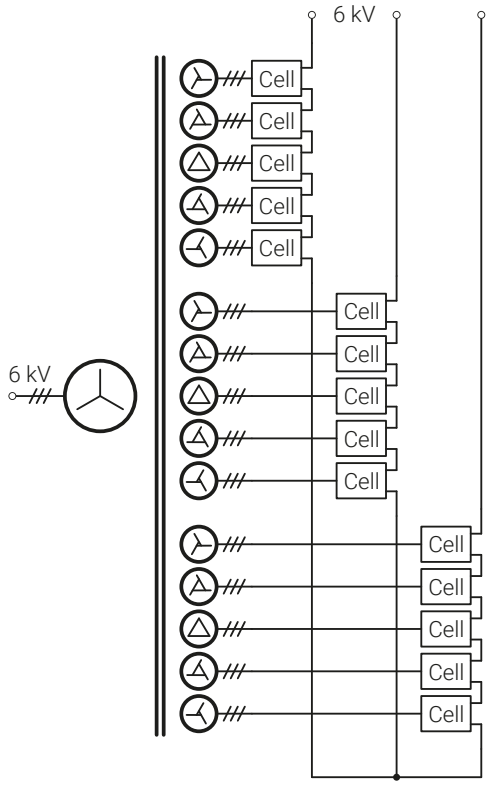

Fig. 2: Cascaded H-bridge topology

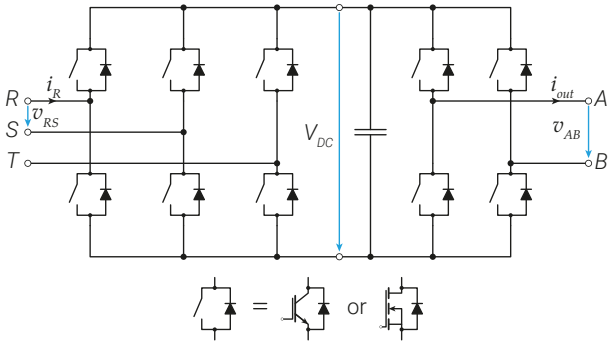

Fig. 3: Regenerative cell with an AFE stage (left) and inverter HB stage (right). Input filter is not shown.

cancel grid frequency current harmonics below harmonic order $6 \cdot N - 1$. Therefore, the AFE current control bandwidth requirements is rather low. However, a higher switching frequency could reduce the filtering effort of the AFE switching harmonics and increase the bandwidth of the dc link voltage control for the emulated transients. As EUT can be both sink and source, the grid emulator has to be designed to be fully regenerative.

Having access to a multi-winding transformer with parameters provided in Table I, presence of only five secondary windings per phase implies relatively low multiplication factor ($N = 5$) for the apparent switching frequency, thus to increase the apparent switching frequency SiC devices are considered for HB stage. Yet, to provide fair and complete comparison,

TABLE I: Multi-Winding Transformer Parameters

Parameter	Value
Apparent Power Rating	1 MVA
Primary Side Line Voltage	6 kV
Secondary Side Line Voltage	710 V
Frequency	50 Hz
Star Primary Windings	1
Extended Delta Secondary Windings	15
Phase Shifts of the Secondaries	0°, 12°, 24°, 36°, 48°

TABLE II: Regenerative Cell Parameters

Parameter	Value
Apparent Power Rating	66.7 kVA
AFE Nominal Current	54 A
Inverter HB Nominal Current	96 A
Maximum dc link voltage	1200 V
Semiconductor blocking voltage	1700 V
AFE zero-sequence voltage injection	min/max
Inverter HB zero-sequence voltage injection	none
AFE Modulation	triangle carrier PWM
Inverter HB Modulation	PSC-PWM

full Si, full SiC as well as hybrid module and hybrid cell designs are evaluated. Cell ratings are summarized in Table II.

In our application, high dynamics has a higher weight than efficiency, thus a generous loss budget of 4 % at nominal power is allocated for semiconductors alone.

III. Power Semiconductor Modules

Fully qualified and commercially available power modules of the 1.7 kV voltage class were evaluated, and as shown in Fig. 3 for simplicity reasons two-level switching cells are considered for both AFE and HB.

A. Half-Bridge SiC Modules

Currently, the choice of commercially available 1.7 kV SiC MOSFET halfbridge modules is very limited and the only considered modules are the Wolfspeed module [14] in an M6 screw terminals package and the Microsemi module [15] in a through-hole mounting package.

B. Half-Bridge Si IGBT Modules

In contrast to SiC MOSFET modules and Si IGBT / SiC SBD hybrid modules, there is a big choice of Si IGBT modules, so only several recent generation IGBTs like Infineon IGBT4 and similar of current classes up to 150 A were considered. Available half-bridges start at 75 A and six-packs at 100 A. Various packages are used but 62 mm and EconoPACK™ 3 and 4 mounting dimensions are most common for several manufacturers. One of the compared modules, a 150 A SEMIKRON module [16], was picked to represent this group.

C. Half-Bridge Hybrid Modules

Hybrid modules with Si IGBTs and SiC SBD could be a viable solution for reaching higher switching frequency or lower losses at moderate cost. The smallest module available at the moment is rated at 400 A [17], so potential benefits of this technology can only be extrapolated for lower-rated modules.

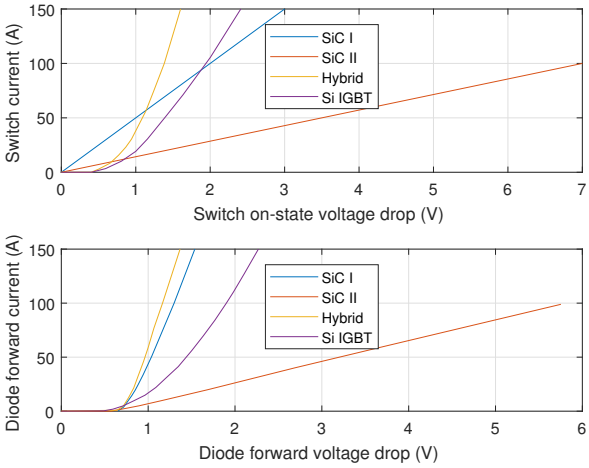

Fig. 4: Static characteristics. Junction temperature details are provided in Table III

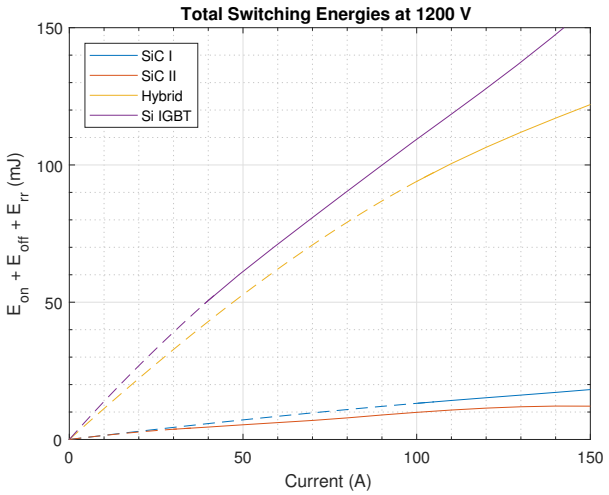

Fig. 5: Switching energies at 1200 V. Datasheet based values: solid lines, cubic interpolation: dashed lines. Junction temperatures and external gate resistor values are provided in Table III.

The modules whose results are presented are listed in Table III. Short designators were assigned to simplify the descriptions throughout the paper.

Fig. 4 shows the hot conduction curves of the switches and co-packed diodes. One can already see that SiC II might be undersized for the full power rating in our application. Fig. 5 shows that the Hybrid module has about 15 % lower switching losses than the Si IGBT despite more than two times higher dc current rating. The losses of both SiC devices are almost one order of magnitude below those of the Si IGBT and more similar than one would expect from their current ratings.

TABLE III: Parameters of the Compared Power Semiconductor Modules

Halfbridge Module	Short Designator	Package	Datasheet Parameters				Ref.
			$T_{\mathrm{j,SW}}$	$T_{\mathrm{j,D}}$	$R_{\mathrm{g,on}}$	$R_{\mathrm{g,off}}$	
CAS300M17BM2	SiC I	62 mm	150 °C	150 °C	2.5 Ω	2.5 Ω	[14]
APTMC170AM30CT1AG	SiC II	SP1	150 °C	175 °C	10 Ω	10 Ω	[15]
2MSI400VE-170-53	Hybrid	M277	150 °C	150 °C	1 Ω	0.5 Ω	[17]
SKM150GB17E4	Si IGBT	34 mm	150 °C	150 °C	2 Ω	2 Ω	[16]

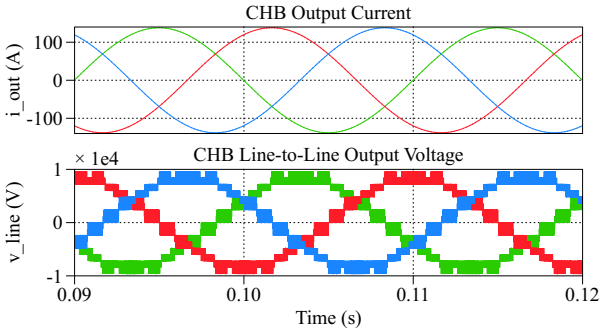

Fig. 6: Simulated CHB output waveforms for 1 MW, $PF = -1$ and $f_{\mathrm{sw,cell}} = 5\,\mathrm{kHz}$

IV. Simulation Results

A. Semiconductor Loss Benchmark

The input and output stages of the cell were modeled separately in Matlab / Simulink with PLECS blockset: the AFE of a single cell up to the constant voltage source as dc link, the cascaded HB output stages as 15 cells with constant voltage source at dc link.

Both stages were controlled with open loop PWM, the correct phase amplitude and phase angle were established by an accordingly parametrized interface impedance and ac voltage source. The modulation and zero-sequence voltage injection methods listed in Table II ensure a better dc link voltage utilization by the AFE and even distribution of switching and conduction losses among all switches. This way, additionally, only one transistor and diode per stage had to be observed. Fig. 6 shows waveforms of one of the benchmark operating points of the inverter HB cells.

The switching instants, voltage and current waveforms were recorded and used as identical dataset for the loss calculation of all semiconductors. The semiconductor loss models contain a linearization of the conduction curves and piece-wise cubic interpolations of multiple samples from the switching loss diagrams, both at high junction temperature; loss energies given at 900 V were linearly extrapolated to 1200 V dc link voltage which is our worst case. Besides equal benchmark conditions, this method is faster than simulation of each semiconductor separately if a high number of semiconductor models and/or high switching frequencies are involved.

In contrast to the calculation methods proposed in [18] the losses are simulated for the maximum operating junction temperature and do not assume partial reverse conduction through the intrinsic SiC MOSFET diode, whose current share depends on the junction temperatures and the actual conduction characteristics of the two diodes. Our results may therefore give some design margin in the real application.

B. AFE — Power Losses

Simulation results for losses per switch of the AFE for switching frequencies from 1.2 to 20 kHz are shown in Fig. 7. All modules showed similar results for both power flow directions: only conduction loss share of diode and switch are reversed for the opposite power factor. For power factor zero almost equal conduction losses in diode and switch were observed. In this paper, for both stages, power factor $PF = +1$ corresponds to power flow from dc to ac.

As expected Si IGBT modules with similar switching energies but different current ratings performed similarly as their switching losses dominate. Reverse recovery losses account for about 30 % of the switching losses. The Hybrid module performed slightly better due to the negligible reverse recovery losses and reduced turn-on losses, despite the larger chip size. In contrast to the Si IGBT and the Hybrid switch, conduction losses dominate for SiC I module in general and for SiC II below 10 kHz which is favorable when the AFE is operated at lower loading conditions.

The Hybrid module features lower losses than the Si IGBT module for switching frequencies above approximately 2 kHz, however, as the dissipated power increases rapidly to several hundreds of Watts per switch in both cases, the cooling effort, thermal cycling stress and switching transient duration may limit the maximum switching frequency below 10 kHz which is sufficient in our case.

In contrast to that, a low cooling effort could be necessary for the SiC I device which additionally, as SiC device, has a superior thermal conductivity than the Si IGBT. Compared to SiC I, SiC II has higher losses in our AFE application and higher thermal resistances, however, it would still require a smaller heatsink at 20 kHz than the Si IGBT module would do at 5 kHz if thermal resistances of both were exactly equal.

C. HB — Power Losses

The difference between the modules is even more significant in the output stage due to higher currents: While the Si IGBT module can hardly be operated over 5 kHz due to thermal limitations, Fig. 8a suggests that the SiC I module could be operated even significantly higher than 20 kHz with a proper cooling.

Although most of the losses in the Hybrid module are still located in the Si transistor, see Fig. 8c, its chip area is much higher in the Hybrid module than in the Si IGBT module. Therefore the switching frequency could be increased

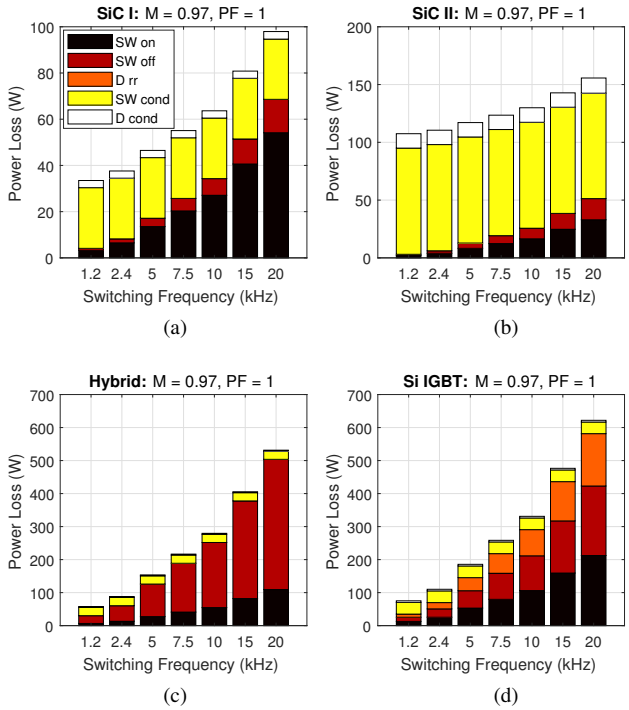

Fig. 7: AFE losses per switch, $P = 1\,\mathrm{MW}$. Note the adapted vertical loss scales.

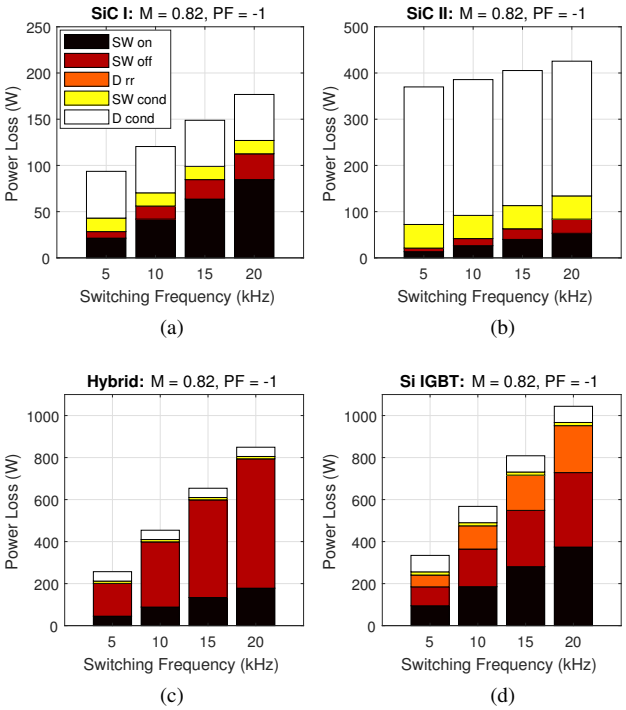

Fig. 8: Inverter losses per switch, $P = 1\,\mathrm{MW}$. Note the adapted vertical loss scales.

compared to the full-Si module. The distribution of losses between conduction and switching is unfavorable for the whole output power range. A Hybrid module with a lower current rating would be preferred.

The losses in Fig. 8b and their distribution show that SiC II is not suitable for the fully rated HB stage.

D. 4Q Cell — Total Power Losses

As both stages have different requirements on the switching frequency, we can use the operation at different switching frequencies in the two stages as a degree of freedom for optimization.

The above results are therefor scaled by the number of switches per stage (six and four) and combined in two-dimensional plots as Figs. 9 and 10. AFE stage losses are arranged along the abscissa, the inverter HB stage losses along the ordinate. The cell losses are the sum of the two stages. Lines connect the losses of the combined operating points and span a grid for interpolation. The plot assumes that the junction temperature can be kept below maximum up to $20\,\mathrm{kHz}$ in any device.

Fig. 9 clearly shows that the full-SiC cells with SiC II modules are within our loss budget at any frequency and with SiC I modules even at its half. Total losses in a Si IGBT cell are 3 to 6 times higher than in a SiC I cell but lower than in a SiC II cell if only the lowest plotted frequencies are required.

Possible switching frequency combinations for the Si IGBT cell and Hybrid switch cell are limited by the dotted $4\,\%$ line. Disregarding the cooling effort, the highest inverter HB stage switching frequency that is affordable when the AFE is operated at $1.2\,\mathrm{kHz}$ is approximately $10\,\mathrm{kHz}$ for the Si IGBT solution and $13\,\mathrm{kHz}$ for the Hybrid switch solution. Taking thermal restrictions into account and driving both stages below $5\,\mathrm{kHz}$, the Hybrid module reduces the losses by ca. $25\,\%$ compared to Si IGBT. This switching frequency could be enough to convey tests related to the fundamental grid frequency for state-of-the-art sub-megawatt inverters.

Also, different type of modules could be used in the two stages, to optimize the semiconductor costs and performance within the loss budget. Fig. 10 shows a combination of Si IGBT modules in the AFE stage and SiC I modules in the output stage. The latter reduces the semiconductor losses in the output stage by 5 to 6 times at $1\,\mathrm{MVA}$, compared to a full-Si IGBT solution. Moreover, both $20\,\mathrm{kHz}$ in the output stage and up to $10\,\mathrm{kHz}$ in the AFE stage are within our loss budget. Finally, Fig. 11 shows the 4Q cell efficiencies for a reduced set of switching frequencies in the AFE.

V. Conclusion

This paper demonstrates effects of using $1.7\,\mathrm{kV}$ SiC MOSFET switches on the performances of the high power medium voltage grid emulator, based on the CHB output stage. Compared to Si devices, higher switching frequencies allow significantly better output performances, which are of high importance for voltage quality for analyzed application. While full-SiC solution would improve system efficiency even further, this is judged unnecessary for the AFE stage, where $10\,\mathrm{kHz}$ Si operated modules provide sufficiently good performances.

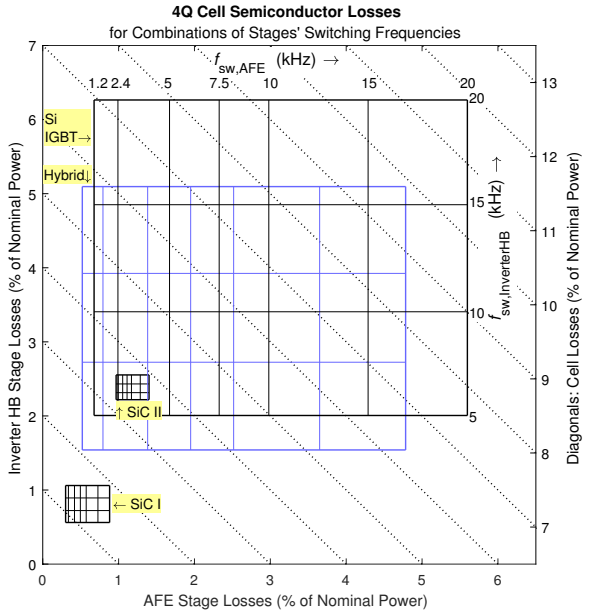

Fig. 9: 4Q cell losses for different switching frequencies in the two stages with same modules in both stages

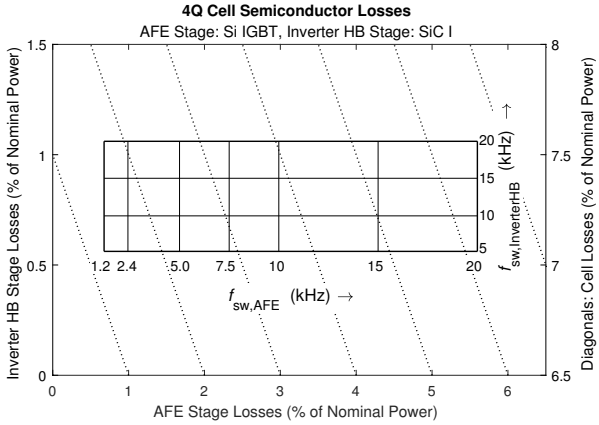

Fig. 10: 4Q cell losses for Si IGBT AFE and SiC I HB at different switching frequencies

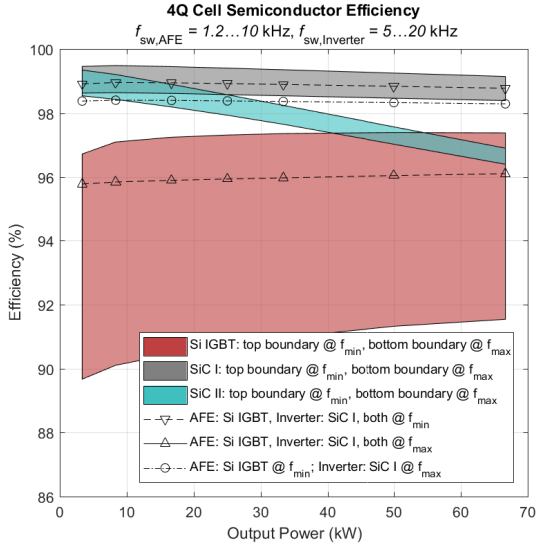

Fig. 11: 4Q cell semiconductor efficiency for switching frequency ranges

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