The 19th International Conference on Industrial Electronics - ICIT2018

Comparative Study of Two-Quadrant DC/DC Stage in Power Supply for Superconducting Magnets

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***Abstract*—To improve the performances of the present European Organization for Nuclear Research (CERN) Large Hadron Collider (LHC), a new family of power supplies for Superconducting Magnets (SCM) is being designed to enhance the operating cycle and recover magnetic-stored energy. Those specific magnets require low-voltage high-current high-precision isolated power supplies. This paper compares different modes of operation for 4-quadrant full-bridge DC/DC converter and its reduced 2-quadrant variant, with emphasis placed on semiconductor losses and overall electrical performances. From the presented comparative study, it can be seen that 2-quadrant topology combined with synchronous rectification offers the most interesting characteristics for considered application.**

I. Introduction

In order to proceed to the future upgrade of the Large Hadron Collider (LHC) [1], [2] into High Luminosity-LHC (HL-LHC) [3], [4] with a reduced beam size to increase particles collision rate, several systems of the facility have to be upgraded. Inner-Triplet [5], [6] circuit is one of them, where the goal is to reach a magnetic field of 12 T [7] by circulating a precise 18 kA current into the newly developed Superconducting Magnets (SCM) [8]. To achieve a proper magnetic field for the physics experiments, a very stable current with precisely defined rise/fall rates must be applied to the magnets: the dynamics is constrained by the system operation whose limit is $\pm 16\,\mathrm{A\,s^{-1}}$, which leads to a ramp-up/down in around 20 min, the flat-top time can be up to 15 h, during which experiments are conducted. Regarding lifetime expectancy, 200 days of physics operation a year, with two cycles per day are foreseen; the system must be designed to achieve at least 20 years of lifetime.

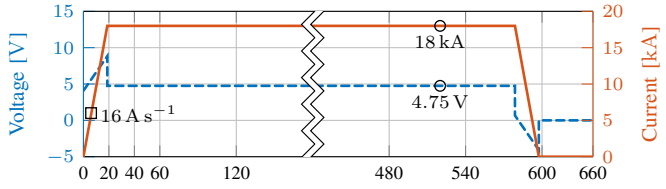

Figure 1: Typical load profile and ratings for Inner-Tripets magnets cycle. Magnet voltage (left axis, dashed) and magnet current (right axis, solid).

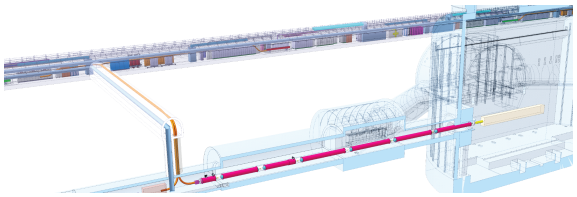

Figure 2: Integration layout in the underground galleries.

Figure 1 shows three typical stages: (i) ramp-up, where the current goes from a minimum to the nominal value (magnet is energized) (ii) flat-top, where the current must be precisely regulated at parts-per-million (ppm) level (only resistive losses are supplied) (iii) ramp-down, where the magnet current decreases from nominal to minimum value (magnet gives energy back). Table I shows the parameters for the Inner-Triplet magnets load. In contrast to existing LHC installations, HL-LHC magnets feeding supplies will be located close to the SCM, directly in the underground galleries as depicted in Figure 2. Only a reduced length of copper cable between supply and superconducting feedbox will determine the resistive part of the load, resulting in very large discharge time if done through dissipation in water-cooled cables, as currently performed by 1-quadrant supplies. For that reason 2-quadrant supplies with specifications in Table II are needed, providing unidirectional current and voltage of both polarities.

Table I: Load specifications.

Inductance	Resistance	Peak power	Accuracy class
L_{LOAD}	R_{LOAD}	$P_{LOAD[peak]}$	I_{acc}
255 mH	0.264 mΩ	159 kW	18 mA (10 ppm)

Table II: Power supply specifications.

Rated current	Rated voltage
I_{RATED}	V_{RATED}
18 kA	±10 V

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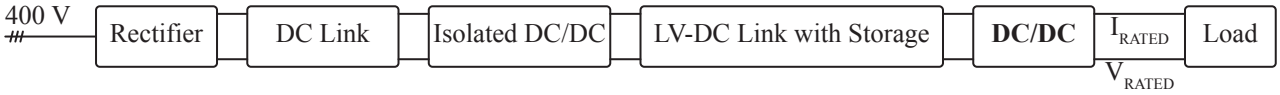


Figure 3: Complete magnet supply structure, output converter stage (DC/DC) is discussed in this paper.

II. Superconducting Magnets Power Supply System

The simplified layout of SCM power supply is shown in Figure 3. Focus of this paper is on the output DC/DC converter stage, directly interfaced to the SCM, and supplied on the grid side through a rectifier followed by an isolated step-down DC/DC converter. Low-voltage DC link includes an energy buffer (or storage) in order to locally manage recovered energy from the load (superconducting magnet).

III. Output DC/DC Stage

Taking into account Table II ratings, paralleling of several power converter stages is mandatory to reach the rated output current. The DC/DC converter stage is then considered to be divided into *N sub-converters* themselves composed of *m* parallel *branches*, the structure is depicted in Figure 4a. This brings modularity and redundancy to the converter architecture, as these are two criteria highly valued for CERN designs. In addition, the complete supply adopts the *N+1* redundancy principle in order to guarantee availability of the system in case of individual fault. This work focus is on one $2\,\mathrm{kA}$ *sub-converter* (cf. Figure 4c) by considering $N = 9$, with still $10\,\mathrm{V}$ (rated) output voltage.

Overall system and naming convention are depicted in Figure 4, where S (Switch) is the generic name (Figure 4b) as in the proposed topologies it can either be a diode (D) or a MOSFET (T). The switching stage is followed by a single stage LC filter, and parallelization of the *m branches* is done after the aforementioned filter to compose one *sub-converter* in an Input Parallel Output Parallel (IPOP) configuration.

Due to the required 2-quadrant operation, topology from Figure 5a is considered (2Q). It features two switching cells composed of one MOSFET and one diode connected in full-bridge alike configuration. For the positive output voltage it operates as buck-converter where T_4 is always on and the pair (T_1; D_2) is operated in Pulse Width Modulation (PWM). For the negative output voltage, the mode of operation changes to switching the other leg (D_3; T_4), while T_1 is always off. The duty-cycle d is different for each mode of operation. Because of the MOSFET ability to carry current in both directions [9], the Synchronous Rectification (SR) operation can be introduced (2QSR), resulting in four active switches, as depicted in Figure 5b. The modes of operation, for positive and negative output voltage, are the same as previously described, respectively. As the 2QSR topology features four active switches, it can be operated as a classical 4-quadrant full-bridge topology (4Q) either with bipolar (4QBI) or unipolar (4QUNI) modulation scheme as depicted

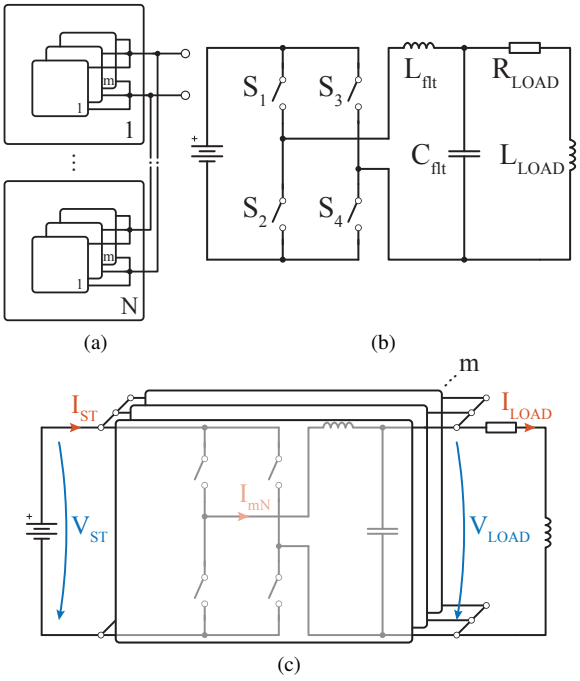
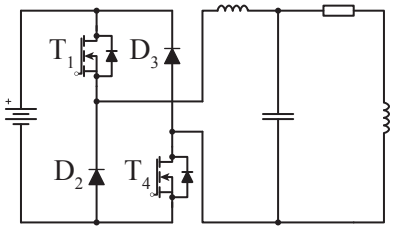


Figure 4: (a) Paralleling of *N sub-converters*, (b) naming convention and (c) electrical circuit for *m* parallel *branches*.

in Figure 5c. Even though full 4-quadrant is not needed, performances are interesting to be compared between bipolar, unipolar modulation and the considered SR. Those mode of operation could be considered for controllability reasons. The characteristic of each switch together with the adopted modulation strategy leads to four different solutions whose losses and electrical performances are compared hereafter. The goal is to correctly evaluate the modes of operation before reaching prototyping as any voltage drop is directly affecting output dynamics as well as electrical losses, thus should be taken into account in the simulation. These issues are inherent to the very low output voltage, high-current power supplies.

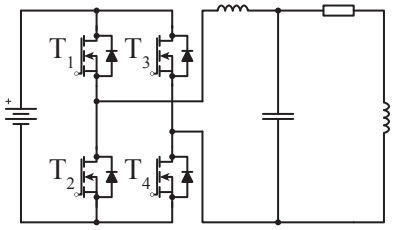
For the comparison, a $100\,\mathrm{V}$ MOSFET from *IXYS* is selected [10], rated $500\,\mathrm{A}@25\,^{\circ}\mathrm{C}$, $R_{DS_{on}} = 1.6\,\mathrm{m}\Omega$ and used at $150\,\mathrm{A}$ for the simulation of one $2\,\mathrm{kA}$ *sub-converter*: operating current is deduced from $@120\,^{\circ}\mathrm{C}$ junction temperature, derating of the component takes into account worst case scenario. The *sub-converter* is considered to have $m = 14$ devices in parallel. Results are given for $50\,\mathrm{kHz}$ switching frequency, interleaving is considered to increase the apparent switching frequency needed to reach precision requirements and reduce the size of the passive elements of the filter.

Mode	T_1	D_2	D_3	T_4
$V_{LOAD} \geq 0$	d_1	$1-d$	blk	on
$V_{LOAD} \leq 0$	off	cond	$1-d$	d



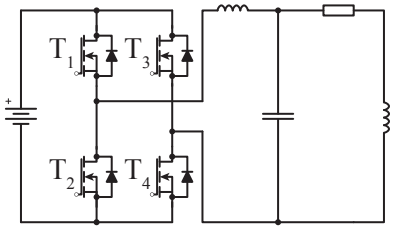
(a)

Mode	T_1	T_2	T_3	T_4
$V_{LOAD} \geq 0$	d	$1-d$	off	on
$V_{LOAD} \leq 0$	off	on	$1-d$	d



(b)

Mode	T_1	T_2	T_3	T_4
bipolar	d	$1-d$	$1-d$	d
unipolar	d	$1-d$	d	$1-d$



(c)

Figure 5: Configurations under study (a) 2-quadrant operation with diodes (2Q), (b) 2-quadrant operation with MOSFET operated in synchronous rectification (2Q) and (c) 4-quadrant operation with classic bipolar (4QBI) or unipolar modulation (4QUNI).

A. 2-Quadrant Bipolar Buck Supply

1) 2-Quadrant: This is the case presented in Figure 5a where diodes can either be MOSFETs body diode or external discrete one. The switching strategy determines two modes of operation: one for positive output voltage (to feed the load) and another one for negative output voltage (to recover the energy from the magnet), leading to a buck supply with bipolar output voltage operated in Continuous Conduction Mode (CCM), presented in Figure 6. In the following $\pm 10\,\mathrm{V}$ are considered for positive an negative output voltage, respectively.

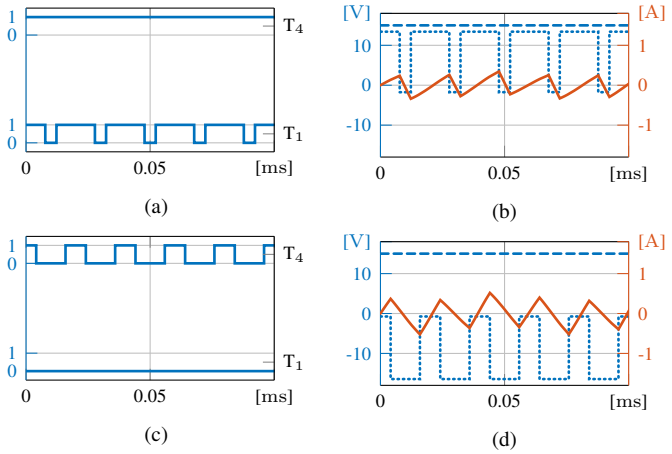


Figure 6: (2Q) 2-quadrant. Positive output voltage: (a) gate signals, (b) output waveforms. Negative output voltage: (c) gate signals, (d) output waveforms. In (b), (d) output waveforms. In (b), (d) dashed is V_{ST}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis).

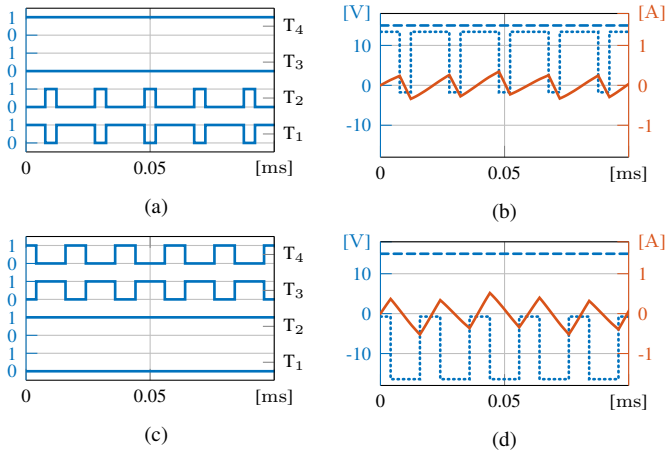


Figure 7: (2QSR) 2-quadrant with SR. Positive output voltage: (a) gate signals, (b) output waveforms. Negative output voltage: (c) gate signals, (d) output waveforms. In (b), (d) dashed is V_{ST}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis).

2) 2-Quadrant with Synchronous Rectification: A variation of the previous topology, considering the use of four driven switches (S_2 and S_3 are MOSFETs), and the well know synchronous rectification widely used in buck applications [11], is implemented while keeping the same modulation strategy. The firing on the same leg is still complementary, with adequate dead-times to avoid shoot-through because the internal diode of corresponding MOSFET starts conducting before, which leads to a sort of Zero Voltage Switching (ZVS) operating mode [12] as presented in Figure 7. In such configuration, output waveforms remains almost identical to previous ones.

B. 4-Quadrant Full-Bridge

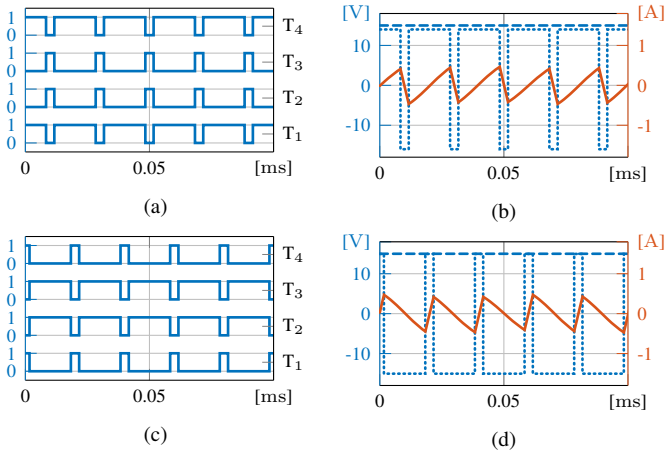


Figure 8: (4QBI) Full-bridge bipolar modulation. Positive output voltage (a) gate signals, (b) waveforms. Negative output voltage (c) gate signals, (d) waveforms. In (b), (d) dashed is V_{ST}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis).

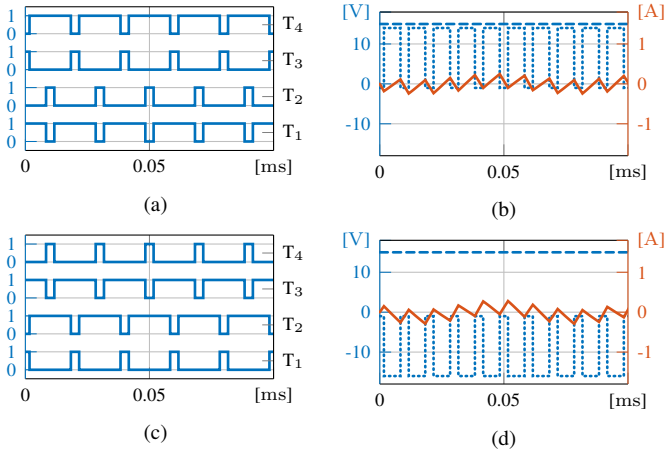


Figure 9: (4QUNI) Full-bridge unipolar modulation. Positive output voltage (a) gate signals, (b) waveforms. Negative output voltage (c) gate signals, (d) waveforms. In (b), (d) dashed is V_{ST}, dotted is output voltage (left axis) and solid is output filter current ripple (right axis).

The synchronous rectification leads to the same power part count as a conventional full-bridge converter, 2-quadrant can be compared with traditional 4-quadrant modulations, bipolar: (S_1, S_4) and (S_2, S_3) are treated as two switch pair, as depicted in Figure 8; and unipolar with the frequency doubling effect depicted in Figure 9. Then, there is only one mode of operation (i.e., only one duty-cycle definition) where positive output voltage is simply defined by $d > 0.5$. For the same output as before, duty cycles need to be adapted accordingly.

IV. Losses and Performances Comparison

Comparative results obtained from PLECS® simulations are shown in Figures 10 and 11. For all considered power supply topologies, DC/DC converter is supplied from 15 V (V_{ST}) and at first, operates at the flat-top operating point: 4.75 V with 2 kA load current. This is the nominal operating point of the converter, which is reached after the ramp-up transition phase.

For the 2-quadrant operation (2Q), from the loss split, it can be seen that the dominant losses are the conduction ones, particularly because of the poor performances of the diode (cf. Figure 10a). Even if in this case, an external Schottky diode is selected and is taken into account for the simulations: losses in the component D_2 represents 10 % of the total output power of the stage (9.5 kW), which is not acceptable. However it can be seen that D_3, as it is constantly blocking, does not account for any losses, there is then a strong unbalance of the losses among the semiconductor devices of the converter.

Introduction of SR (2QSR) improves the performances, as it can be seen in Figure 10b, in particular for S_2, because of the better conducting performances of the MOSFET than the selected Schottky diode: even if there is some switching losses in the component, the reduction of conducting losses account for a global improvement of the performances. The specific modulation allows to reduce switching losses, as only the minimal number of devices is switched.

Finally, results for a classical 4-quadrant (4Q) operation are provided in Figure 10c. First noticeable fact is the equal split of the losses among diagonal devices (T_1;T_4 and T_2;T_3) . Analysis of the losses at the component level can lead to some improvement (i.e. for T_2), but as all devices are constantly switching, there is an unavoidable share of switching losses in all the devices. Additionally, the overall sum of losses is closer to $2Q$ topology. That result is also highlighted in Figure 11.

As the operating cycle of the converter is well predictable, only several operating points can be considered to establish the performances of the converter during operation (cf. Figure 1). Such operating points are the following: (i) OP1 is 2 min into ramp-up, (ii) OP2 is middle of ramp-up, (iii) OP3 is end of ramp-up, (iv) OP4 is flat-top, (v) OP5 is middle of ramp-down. The average values of the output voltage and current are given in Table III and efficiencies are plotted in Figure 11. Out of those five points, only one (OP5) requires the negative mode of operation ($V_{LOAD} \leq 0$), in all of the other (OP1,...,OP4) the converter operates in positive mode ($V_{LOAD} \geq 0$). Even though OP2 and OP5 are in the middle of transition phase, their output power is different because of the reduced negative voltage during recovery.

Table III: Operating points.

Unit	OP1	OP2	OP3	OP4	OP5
[V]	4.59	6.46	8.83	4.75	−1.70
[A]	210	1000	2000	2000	1000
[kW]	963.9	6.46	17.7	9.5	−1.7

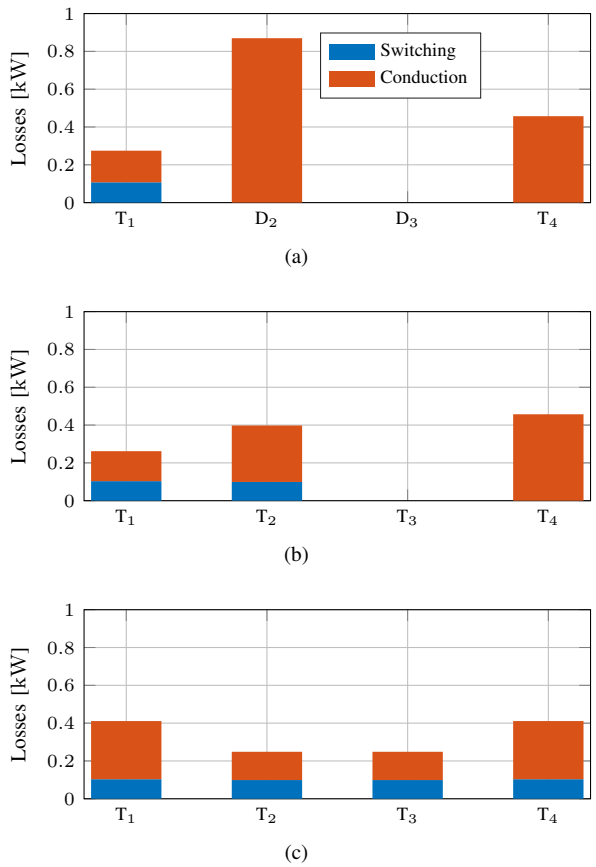


Figure 10: Comparison of *sub-converter* (addition of 14 switching devices) losses for different topologies at 50 kHz and flat-top operating point (4.75 V; 2 kA; 9.5 kW). (a) 2-quadrant (2Q), (b) 2-quadrant with SR (2QSR) and (c) 4-quadrant bipolar (4QBI) and unipolar (4QUNI).

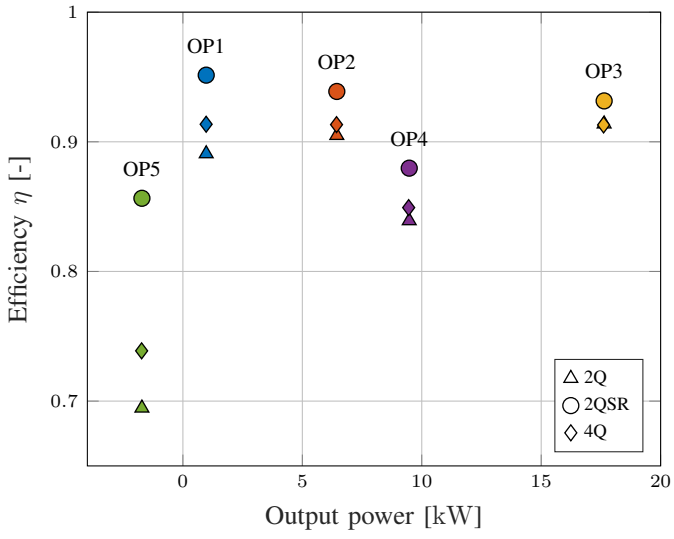


Figure 11: Efficiency vs output power of the converter for all topologies and operating points.

Table III presents the efficiency of all topologies at the defined operating points. Out of these simulations, highlighted by the figures, some conclusions can be drawn:

- The analysis of the graph allows to establish a clear hierarchy in efficiency within the topologies, where 2QSR is the best performing one, 2Q the worst and 4Q intermediate one, rather close to 2Q.
  - The optimized switching pattern of the 2QSR topologies allows to reach higher efficiency because of overall reduced losses (cf. Figure 10).
- The highest efficiency is reached for low-current operating point (OP1), especially because of the importance of conduction losses.
- At the peak power of the operating cycle (OP3), all topologies reach similar efficiency around 92 %, output voltage is at its peak value thus, the voltage drop on the component becomes less critical.
- The operating point in the recovery mode of operation (OP5) is the least efficient one across all topologies (series of points at the most left hand side of Figure 11).
  - As the operating condition (mainly the output voltage) change between the positive output and negative output mode of operation, the efficiency is not symmetrical during ramp-up/down of the current (cf. OP2 vs OP5).
  - The loss sharing among devices is reversed compared to Figure 10: T_1 is OFF leading to no losses, whereas T_3/T_4 are switching accordingly to the imposed duty-cycle imposed on T_4.
  - Efficiency in this phase should be maximized in order recover most of the load magnetic energy.
- For 4Q unipolar or bipolar modulation, there is no difference on losses, but an impact on the output waveforms of the converter.
- As the switching losses account for a limited percentage of the overall losses, reducing the switching frequency can impact the efficiency of the converter. In the proposed case, lowering it from 50 kHz to 20 kHz increase the efficiency by 2 % (cf. Figure 12).

High currents impact significantly achievable operational efficiency of the converter, and reaching higher efficiencies can be done by paralleling more devices as it can be seen in Figure 12. The price to pay is to greatly oversize the system in order to reduce the current that each device has to handle. Some saturation effect can be noticed, and the optimal number of component will be defined according to mechanical integration and output filter design.

There is still room for further optimization: as in the 2QSR topology there is an uneven split of losses among devices, the one that are mainly used in conduction can take advantage of a lower $R_{DS_{on}}$ whereas the others T_1, T_2 should keep good performances in switching, selection of the device depending on those constraints could improve further the efficiency of the converter.

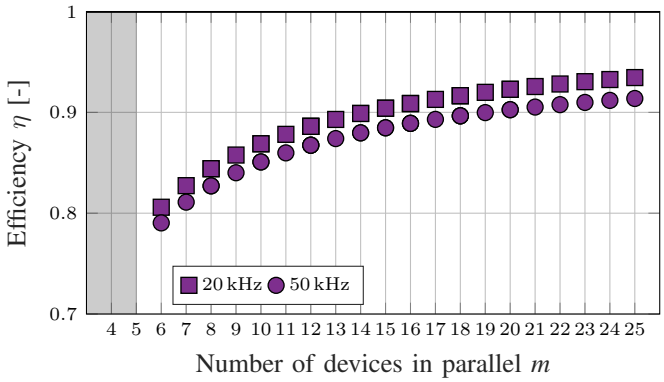


Figure 12: Efficiency vs number of devices in parallel. Grey area defines thermally not viable configurations.

V. Conclusions

In this paper, the specific requirements for a magnet power supply as well as effectiveness of various topologies under different operating modes is presented. The description as well as complete simulation and comparison of the models including losses analysis and electrical performances, taking into account temperature and operating conditions highlights the predominant role of conduction losses. The 2-quadrant topology operating with synchronous rectification has been identified as the most efficient topology at any operating point of the cycle, with a possible optimization on the number of devices parallelized and the switching frequency.

References

[1] O. Brüning, P. Collier, P. Lebrun, S. Myers, R. Ostojic, J. Poole, and P. Proudlock, *LHC Design Report*. CERN, Jun. 2004.

[2] ——, *LHC Design Report V2*. CERN, Nov. 2004.

[3] "HL-LHC Preliminary Design Report: Deliverable: D1.5", CERN, Tech. Rep., Nov. 2014.

[4] G. Apollinari, I. Béjar Alonso, O. Brüning, M. Lamont, and L. Rossi, *High-Luminosity Large Hadron Collider (HL-LHC): Preliminary Design Report*. CERN, Dec. 2015.

[5] P. Pfund, "Inner Triplet Systems at IR1, 2, 5 and 8", TD/FNAL, USA, Tech. Rep. EDMS 108981, May 2005.

[6] S. Yammine and H. Thiesen, "HL-LHC inner triplet powering and control strategy", in *Proc. of International Particle Accelerator Conference (IPAC'17), Copenhagen, Denmark, 14-19 May, 2017*, May 2017, pp. 3544–3546.

[7] L. Bottura, G. de Rijk, L. Rossi, and E. Todesco, "Advanced accelerator magnets for upgrading the lhc", *IEEE Transactions on Applied Superconductivity*, vol. 22, no. 3, pp. 4 002 008–4 002 008, Jun. 2012.

[8] F. Savary, M. Bajko, B. Bordini, L. Bottura, L. Fiscarelli, J. Fleiter, A. Foussat, S. I. Bermudez, M. Karppinen, F. Lackner, C. H. Löffler, E. Nilsson, J. C. Perez, H. Prin, R. Principe, D. Ramos, G. de Rijk, L. Rossi, D. Smekens, S. S. Tavares, G. Willering, and A. V. Zlobin, "Progress on the development of the nb3sn 11t dipole for the high luminosity upgrade of lhc", *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 4, pp. 1–5, Jun. 2017.

[9] S. Jaunay and J. Brown, *DC-to-DC Design Guide*, V 1, Vishay Siliconix, Oct. 2002.

[10] IXYS_CORPORATION, *IXYS MMIX1F520N075T2*, Dec. 15.

[11] T. Instruments, *Synchronous rectification in high–performance power converter design*, V 0.3, Texas Instruments, Sep. 2016.

[12] R. Semiconductor, *Calculation of Power Loss (Synchronous)*, V 0.3, ROHM Semiconductor, Oct. 2016.