A Design-oriented Charge-based Simplified Model for FDSOI MOSFETs

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***Abstract*—In this paper a design-oriented model for asymmetrical double-gate (ADG) MOSFETs is proposed. Including the back-gate effect into the original simplified EKV bulk model requires only one additional parameter to the existing four, and extends the simplified EKV model to FDSOI processes. This will help the designer to find the right trade-off in terms of design parameters, including the back-gate biasing. A comparison with measurement results from a 28-nm FDSOI CMOS process is provided, assessing the excellent accuracy of the proposed.**

***Index Terms*—simplified EKV, modeling, FDSOI, back-gate**

I. Introduction

In most of the applications that nowadays are dealing with integrated circuits, low-power operation is a key aspect. Due to this fact, conventional design methodologies have been revised in order to exploit at best all the features of advanced technologies [1]. In that sense, the simplified EKV model (sEKV) [2], [3], based on the inversion coefficient (IC), has demonstrated its effectiveness in describing the performance of MOSFETs in all inversion conditions while using only a few parameters. The key of this capability, together with the charge-related basis, is the normalization, that strips off the dependence to a specific technology which is then captured by only a few parameters. This makes the simplified EKV model suitable also as a benchmark for technologies, in addition to helping the designer to explore the design space and find the right trade-off in terms of design parameters [2].

However, the technologies portfolio has been growing rapidly as the scaling-down process gets close to reach physical limits achievable with a standard bulk planar technology. In the latest years, two main alternatives to bulk process has emerged, i.e. finFET and FDSOI processes [4], [5]. If in the case of finFET, the sEKV bulk model is still suitable [2], for FDSOI back-gate effects have to be considered. Therefore, this further degree of freedom has been addressed through a re-adaptation of the sEKV model, so that the design flow can directly focus on the performance trade-offs linked also to the back-gate biasing.

The paper is organized as follows. In Section II, the sEKV model is briefly recalled and its extension for ADG processes is detailed, followed by the parameter extraction flow described in Section III. Its validation with respect to measurement results from a 28-nm FDSOI CMOS process is shown in Section IV, while the practical implications of the proposed approach are highlighted in Section V. At the end, conclusions are drawn.

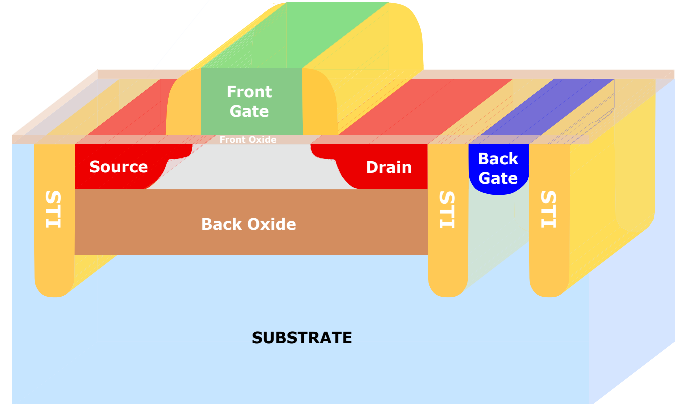

Fig. 1: Sketch of a typical FDSOI MOSFET.

II. Model description

As a starting point, the simplified EKV model is considered [2]. In order to recall it, its derivation basics are cited below. The net normalized drain current that flows into the device can be expressed as a function of the normalized source and drain charges, q_s and q_d respectively, as $i_d = q_s + q_s^2 - q_d - q_d^2$.

The first simplification introduced assumes that the device is operating in saturation region, that is actually the case in most of its practical uses in analog design. In this conditions, q_d can be reasonably neglected, yielding:

$$IC = \frac{I_D|_{\text{saturation}}}{I_{\text{spec}}} = i_{\text{dsat}} = q_s + q_s^2, \tag{1}$$

where the Inversion Coefficient IC is defined as the drain current in saturation normalized with respect to the specific current I_{spec}.

Nevertheless, in ultra-scaled technologies, Short-Channel Effects (SCEs) play a crucial role when the channel length L approaches the minimum feature size. When this occurs, the simple relation in (1) is not effective. In order to take into account SCEs, and in particular Velocity Saturation (VS), the following relation is considered instead [6]:

$$IC = \frac{4(q_s + q_s^2)}{2 + \lambda_c + \sqrt{4\,(1+\lambda_c) + \lambda_c^2\,(1+2q_s)^2}}, \tag{2}$$

where $\lambda_c = L_{\text{sat}}/L$ is the VS parameter, corresponding to the relative portion of channel in full velocity saturation.

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In order to make a link between the drain current and the gate voltage, and hence have an analytical expression for the MOSFET's transfer characteristic, the EKV model is again exploited. The latter provides a charge-to-voltage relation expressed as

$$2\,q_{\mathrm{s}} + \ln q_{\mathrm{s}} = v_{\mathrm{p}} - v_{\mathrm{s}}, \tag{3}$$

where v_{p} and v_{s} are the normalized pinch-off and source voltage respectively. Notice that all voltages are normalized to the thermal voltage $U_{\mathrm{T}} = kT/q$, where k is the Boltzmann constant, T is the temperature and q is the electron charge.

The crucial statement that enables the inclusion of back-gate effect is the re-definition of the channel pinch-off voltage v_{p}. The sEKV model for bulk processes defines it as $(v_{\mathrm{g}} - v_{\mathrm{t0}})/n$, that is the difference between the gate voltage and the threshold voltage, rescaled with respect to the slope factor n. Targeting ADG processes, this definition has to be modified accounting for the two independent gates, namely the front-gate voltage v_{fg} and the back-gate voltage v_{bg}.

In the range of voltage useful for the designer, the impact of the back-gate voltage can simply be modeled as a threshold voltage with a linear dependence to v_{bg} (this claim will be confirmed in Section IV), so the pinch-off voltage v_{p} can be defined as

$$v_{\mathrm{p}} = \frac{v_{\mathrm{fg}} - v_{\mathrm{t}}}{n} = \frac{v_{\mathrm{fg}} - (v_{\mathrm{t0}} - k_{\mathrm{ox}} v_{\mathrm{bg}})}{n}, \tag{4}$$

where v_{t0} is considered as the threshold voltage when v_{bg} is set to 0, and k_{ox} is a constant parameter directly linked to the device structure, namely to the the two gate oxide capacitances ratio:

$$k_{\mathrm{ox}} = \frac{C_{\mathrm{ox_b}}}{C_{\mathrm{ox_f}}} = \frac{EOT_{\mathrm{f}}}{EOT_{\mathrm{b}}}. \tag{5}$$

Hence, inserting Eqs. (2) and (4) into (3), the voltage-current expression related to the front- and back-gate voltages can be derived:

$$\frac{v_{\mathrm{fg}} - (v_{\mathrm{t0}} - k_{\mathrm{ox}} v_{\mathrm{bg}})}{n} - v_{\mathrm{s}} = \sqrt{(1+\lambda_{\mathrm{c}} IC)^2 + 4IC} + \ln\left[\sqrt{(1+\lambda_{\mathrm{c}} IC)^2 + 4IC} - 1\right] - (1 + \ln 2). \tag{6}$$

It is worth to make some remarks. First of all, notice that (6) expresses the front-gate voltage as a function of IC, and it is not invertible. Secondly, for the drain current normalization, the I_{spec} is given by $I_{\mathrm{spec}_\square} \frac{W}{L}$, where $I_{\mathrm{spec}_\square} = 2n\mu_0 C_{\mathrm{ox}} U_{\mathrm{T}}^2$. Since for these structures the analytical individual definition of the low-field mobility μ_0 and C_{ox} is not trivial, and the actual goal of this model is to provide an instrument for early-stage design procedures rather than a physics-based compact model, the proposed approach is to replace their product with a generic parameter β, extracted through data fitting and only related to the specific process.

III. Parameter Extraction Flow

As a whole, the parameters included into sEKV are now five. Together with the four already included into the sEKV for bulk, namely n, $I_{\mathrm{spec}_\square}$, L_{sat} and v_{t0}, k_{ox} is considering the back-gate impact on the threshold voltage.

The first necessary step for extracting these parameters regards the standard extraction flow for n, $I_{\mathrm{spec}_\square}$, L_{sat} and v_{t0}, to be performed as described in [2] and synthesized in the flow diagram in Fig. 2, starting from long-channel towards short-channel devices. All this has to be performed initially at $V_{\mathrm{bg}} = 0\,\mathrm{V}$, then also for several back-gate bias points, positive and negative.

Notice that the parameter database consistency among all the lengths has to be constantly checked. Namely, $I_{\mathrm{spec}_\square}$ variation versus L can be justified only in case of a corresponding variation in n, while L_{sat} should remain constant. Thus, once verified that the parameter set is consistent, and eventually performed a general fine-tuning, the k_{ox} parameter can be extracted.

Initially, the threshold voltage at $V_{\mathrm{bg}} = 0\,\mathrm{V}$, normalized with respect to U_{T}, will assume the value of v_{t0}. Then, considering all the threshold voltage values extracted from

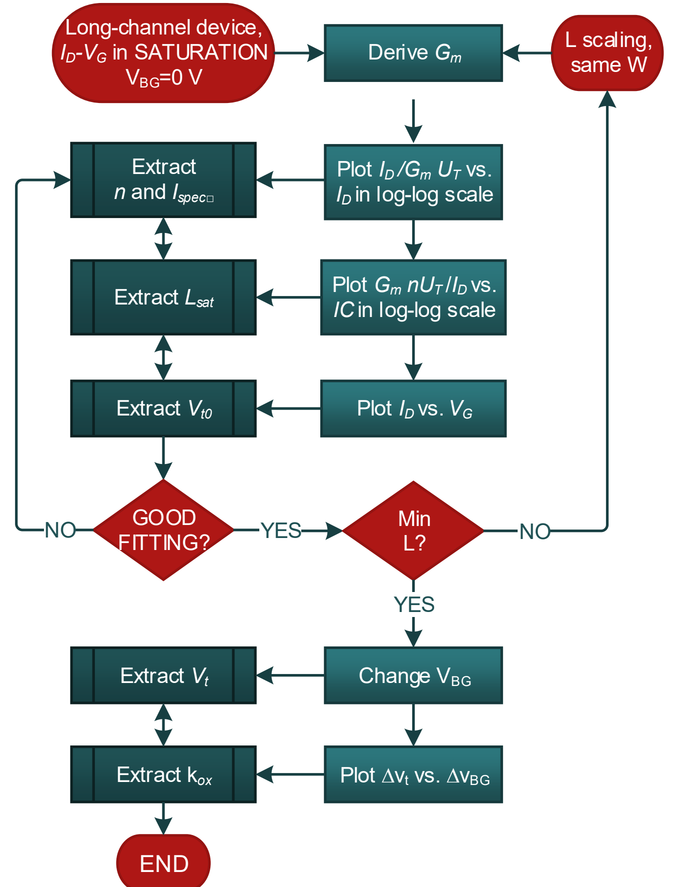

Fig. 2: Simplified EKV parameters extraction flow.

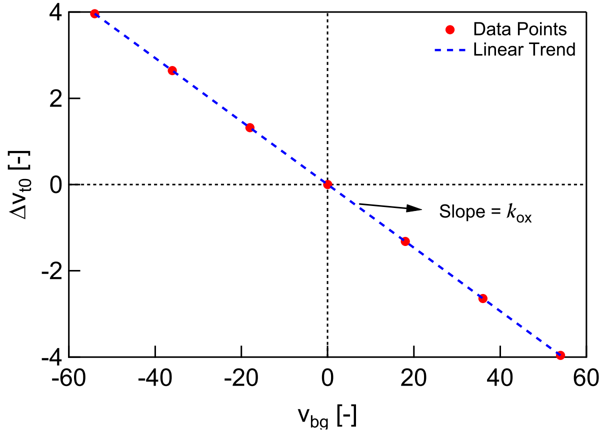

Fig. 3: Δv_{t0} vs. v_{bg} plot used for k_{ox} extraction.

others back-gate bias points and for a specific channel length, it is possible to plot the relative variation of the threshold voltage, i.e. Δv_{t0}, with respect to v_{bg}, as shown in Fig. 3. Specifically, the collection of obtained points should follow a linear trend with zero intercept, whose slope is k_{ox} indeed. Notice that the value of k_{ox} should not depend on L, meaning that for each channel length analyzed, the extracted k_{ox} should be identical.

IV. Model validation

In order to confirm the validity of the previously described sEKV model, a set of measurement data from a 28-nm FDSOI technology is considered (Figs. 4 to 6). In detail, two process options with different front gate oxide thicknesses have been analyzed, whose reference is set to "GO1" and "GO2".

Since the two families of devices differ only by their equivalent front-gate oxide thickness EOT_{f}, by means of the obtained values for k_{ox} in the two cases the equivalent back-oxide thickness EOT_{b} can be extracted. If the theory is valid, the EOT_{b} values extracted from both families should match. The dataset details are listed in Table I.

TABLE I: 28-nm FDSOI dataset specifications.

	GO1		GO2	
Type	NMOS	PMOS	NMOS	PMOS
TOXE	1.55 nm	1.7 nm	3.7 nm	
W	1 µm		2 µm	
L	1 µm 28 nm		2 µm	

Following the flow described in Section III and considering the case of GO1 Thin-Oxide nMOSFETs (Figs. 4a to 4c), the extracted k_{ox} value is 66.7 mV/V. Since the EOT_{f} for this family is equal to 1.55 nm, from (5) the value obtained for EOT_{b} is 23.24 nm.

As a remark, the specific FDSOI process considered is fabricated using the same back-oxide thickness both for GO1 and GO2 devices. Thus, in order to have the model assessed, from the obtained EOT_{b} value and the k_{ox} extracted as in Fig. 6c for GO2 Thick-Oxide nMOSFET (158 mV/V), the EOT_{f} indicated in Table I should be obtained. Indeed, using again (5), a value of 3.67 nm for EOT_{f} is derived, with less than 1% discrepancy.

Proceeding the same way for Thin-Oxide pMOSFETs (Figs. 5a to 5c, $EOT_{\mathrm{f}} = 1.7$ nm), the extracted k_{ox} results in 73.3 mV/V, that gives an EOT_{b} of 23.28 nm. Consequently, for the Thick-Oxide family an EOT_{f} of 3.68 nm is obtained, close to the expected value of 3.7 nm.

Notice that for the same device type and family, a consistent set of sEKV parameters has been extracted. This may lead to a non-ideal fit in some of the curves shown in Figs. 4 to 6 (ex.: moderate inversion region of Fig. 5b). However, as already reminded, the goal of the approach is to provide an instrument for early-stage design procedures rather than a physics-based compact model.

V. Practical consequences

Parameter k_{ox} changes the effective threshold voltage with respect to the back-gate voltage and hence shifts the I-V curves to the left of the $v_{bg} = 0$ curve when v_{bg} is positive or to the right when v_{bg} is negative. The larger k_{ox}, e.g. the larger the ratio of oxide thicknesses, the larger the spread of the curve for an equal v_{bg} step.

Considering the process, it is evident from (5) that the back-gate effect is weaker when the back-oxide is considerably thicker than the front-oxide, as in GO1 process family. However, this effect can be boosted as far as the two oxides thicknesses get similar, which is the case of GO2 process family.

From a design perspective, the parameter k_{ox} can be exploited as a new degree-of-freedom. Indeed, it represents the direct measure of the possible shift in the range of IC values available for a specific geometry and front-gate bias point. This can eventually be employed into a quantitative design of dynamic non-idealities compensation circuits, which can actively counteract on offset/mismatch phenomena that affect a specific structure [7].

VI. Conclusions

A charge-based simplified model for ADG processes is proposed, that is able to include the effect of back-gate biasing on the threshold voltage by means of only one additional parameter, k_{ox}, with respect to the four used in the bulk model. Through measurement data analysis on two device families from a 28-nm FDSOI process, the approach has demonstrated to be effective, by checking the correspondence between extracted physical parameters, i.e. the equivalent front- and back-oxide thicknesses, and their expected value.

The straightforward consequence of this approach, is that even for FDSOI processes, the IC-based design methodology [8] remains valid including the additional back-gate voltage. On top of that, the new parameter k_{ox} can act as a range shifter for the charge-to-voltage relationship, meaning that for the same front-gate bias point and geometry, the device can operate in a range of ICs, directly linked to the value of k_{ox}. This has been already shown practically [5], but now it can be assessed quantitatively and, above all, simply.

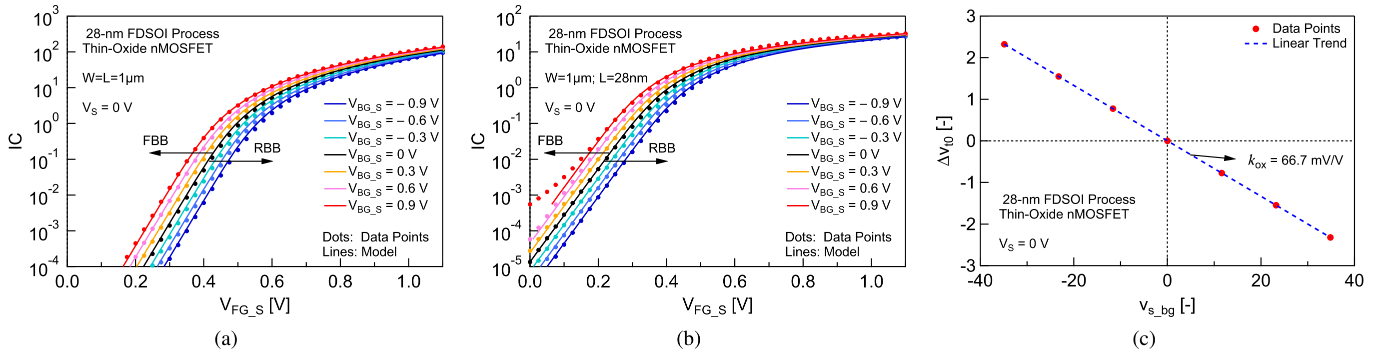

Fig. 4: a) IC vs front-gate voltage for Long-Channel Thin-Oxide nMOSFET (GO1) at different back-gate bias points. b) IC vs front-gate voltage for Short-Channel Thin-Oxide nMOSFET (GO1) at different back-gate bias points. c) k_{ox} extraction from Δv_{t0} vs v_{bg} plot for Thin-Oxide nMOSFET (GO1).

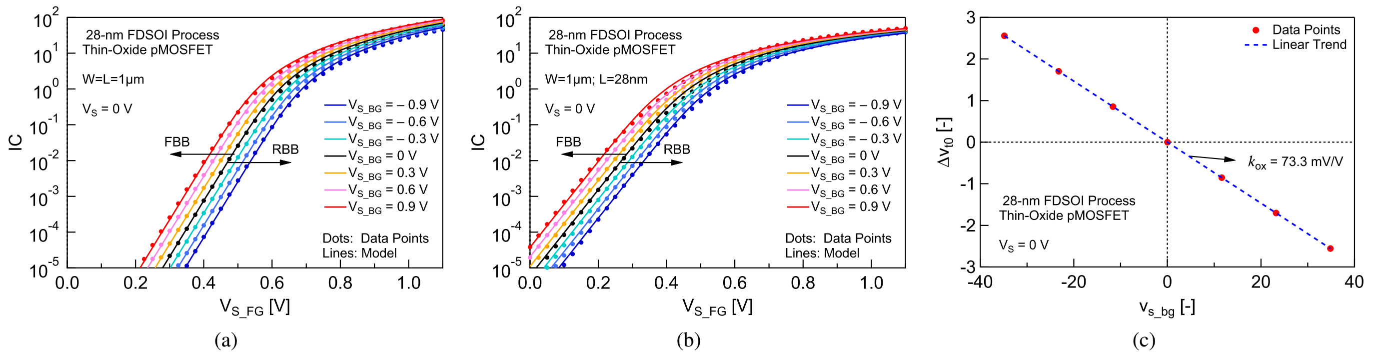

Fig. 5: a) IC vs front-gate voltage for Long-Channel Thin-Oxide pMOSFET (GO1) at different back-gate bias points. b) IC vs front-gate voltage for Short-Channel Thin-Oxide pMOSFET (GO1) at different back-gate bias points. c) k_{ox} extraction from Δv_{t0} vs v_{bg} plot for Thin-Oxide pMOSFET (GO1).

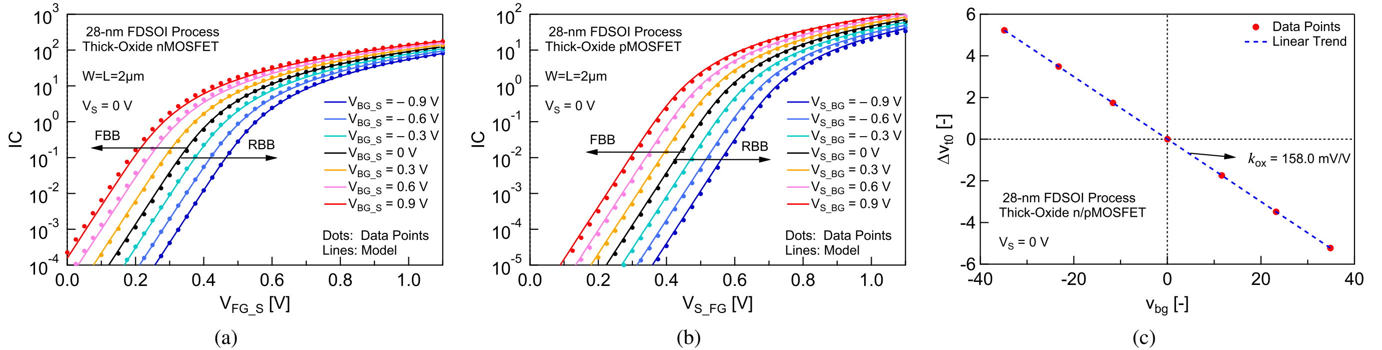

Fig. 6: a) IC vs front-gate voltage for Long-Channel Thick-Oxide nMOSFET (GO2) at different back-gate bias points. b) IC vs front-gate voltage for Long-Channel Thick-Oxide pMOSFET (GO1) at different back-gate bias points. c) k_{ox} extraction from Δv_{t0} vs v_{bg} plot for Thick-Oxide n/pMOSFET (GO2).

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