Analysis of CMS Noise Reduction for 65 nm CIS

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***Abstract*—This work explores the combination of a downscaled technology with in-pixel source-follower (SF) optimization, a high column-level gain and an analog implementation of Correlated-Multiple-Sampling (CMS) for noise reduction of CIS readout chains. Transient noise simulations show that in the optimal condition of a pMOS SF, a column-level gain equal to 64 and a CMS of order 8, the noise can be reduced to the extremely low value of 0.20 e^-_{rms}, with a readout time of 43 μs, demonstrating the possibility of true photoelectron counting for this standard 65 nm process.**

***Index Terms*—CMOS, image sensors, 1/f noise, thermal noise, shot noise, CMS, deep sub-electron noise, photoelectron counting**

I. Introduction

Low-noise performance of CMOS image sensors (CIS) became an active point of research since the development of pinned photodiodes (PPDs). After reducing the readout noise below 1 e^-_{rms} [1, 2], the next step was to approach the near photoelectron counting limit of 0.3 e^-_{rms}. Recently it has been demonstrated that sub 0.5 e^-_{rms} noise performance can be reached through process level optimization and also in standard CMOS process. Process refinements at the pixel level increasing the conversion gain have been combined with column-level amplification and correlated multiple sampling (CMS), in order to achieve the required 0.3 e^-_{rms} level, at the cost of a low full well capacity (200 e^-) [3], the use of a reset signal voltage of 25 V and a large pixel readout time [4]. In [5], it has been shown that 0.48 e^-_{rms} can be reached in a full VGA imager using a standard CIS process and optimal design including the choice of an in-pixel thin oxide source follower (SF), bandwidth control with column-level amplification and a simple correlated double sampling (CDS). It has been expected in [6] that technology downscaling can be used to further reduce the noise. In this work, we explore the combination of design optimization, technology downscaling and a new implementation of CMS based on a passive switched capacitor network, in order to reach deep sub-electron noise.

II. Noise Reduction Techniques

Fig. 1 shows the schematic of a conventional CIS readout chain featuring three different in-pixel SFs, a column-level amplifier and a CMS stage. The readout chain thermal noise can be reduced through bandwidth control and column-level amplification (A_{col}), which also mitigates the noise contribution of the next stages (multiple sampling and analog-to-digital converter (ADC)) [7]. With an optimized thermal noise, flicker noise becames the dominant noise source, despite of the CDS effect. In a standard process, the 1/f noise contribution of the readout chain transistors located outside the pixel can be made negligible with respect to the in-pixel SF if the formers are designed to have much larger gate areas [7]. On the other hand, the in-pixel SF 1/f noise can be reduced by using a SF transistor having a low oxide trap density (N_{t}), a large oxide capacitance C_{ox}, a minimum width and an optimal length [8]. To achieve this reduction, the parasitic capacitance of the sense node C_{p} must also be minimized. This noise reduction techniques are compliant with technology downscaling, if the $\mathrm{N_t}$ does not increase sharply [6]. CMS consists in combining the CDS with averaging. Indeed, *M* samples of the reset level voltage are averaged and then subtracted from the average of other *M* samples taken after the charge transfer from the PPD to the sense node. Compared to a simple CDS, CMS can further reduce the thermal noise variance proportionally to the number of samples *M*. The 1/f noise can also be further reduced thanks to the CMS, but this reduction reaches a plateau for order of *M* higher than 4 [9].

III. Low-Noise CIS Readout Circuit Design

Fig. 1 shows three low-noise CIS readout chains with different pixel-level designs using a 65 nm technology. The different pixels are based on the SF transistors shown in Table I. Transistors PMOS2.5 and PMOS1.2 are expected to have the best 1/f noise performance due to their lower $N_{\mathrm{t}}/C_{\mathrm{ox}}^2$ ratio [5].

TABLE I
Relevant Transistors Parameters

	nMOS2.5	**pMOS2.5**	**pMOS1.2**
V_{dd} [V]	2.5	2.5	1.2
$N_{\mathrm{t}}\,[(\mathrm{eV})^{-1}\,\mathrm{cm}^{-3}]$	8×10^{16}	2.4×10^{16}	9.5×10^{16}
$C_{\mathrm{ox}}\,[\mathrm{fF}/\mu\mathrm{m}^2]$	6.2	5.9	12.0
$t_{\mathrm{ox}}\,[\mathrm{nm}]$	5.6	5.9	2.8
$N_{\mathrm{t}}/C_{\mathrm{ox}}^2\,[(\mathrm{eV})^{-1}\,\mu\mathrm{m}\,(\mathrm{fF})^{-2}]$	2081	689	660

The three readout chains share the same column-level amplifier and CMS circuit. The gain of the column-level amplifier can be set to 16, 32 and 64. Consequently, the bandwidth corresponds to 512 kHz for a gain of 16 and 256 kHz for a gain of 64. The CMS is implemented with a passive switched capacitor network. The schematic shown in Fig. 1 allows performing a CMS of order 8 with the minimum number of capacitors [9]. Fig. 2 shows the timing diagram of the full readout chain operation. The averaging is performed using the mechanism of charge sharing between two identical capacitors. Iterating this mechanism allows averaging a number of samples, corresponding to powers of 2. In this

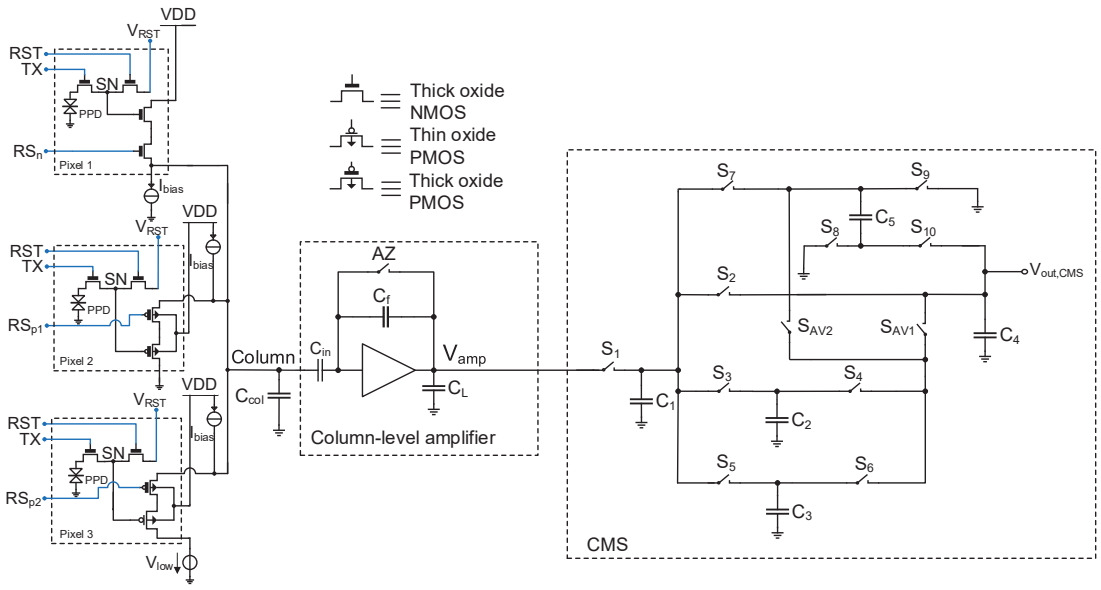

Fig. 1. Schematic of the simulated low-noise CIS readout chains.

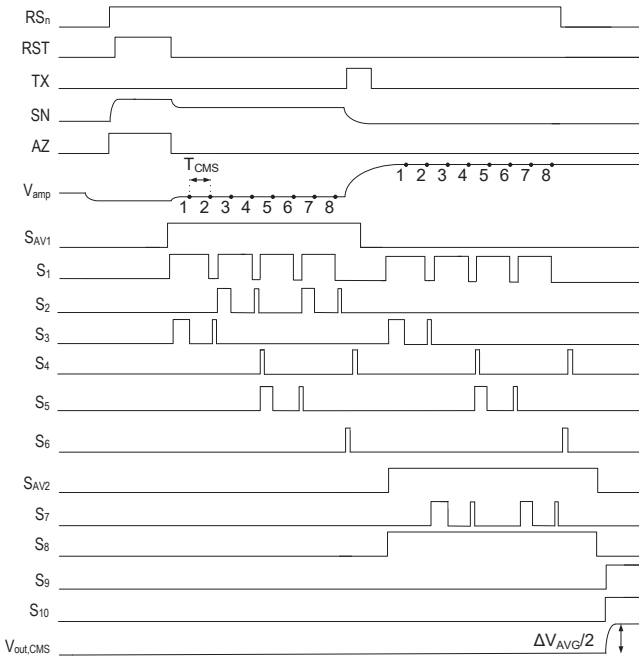

Fig. 2. Timing diagram of the simulated CIS readout chain.

example, first switches S_1 and S_3 are closed. S_3 is opened to hold a sample in C_2. Then S_1 is opened after T_{CMS} in order to hold the next sample in C_1. S_3 is then closed with a short pulse, as shown in Fig. 2, to compute the average of the two samples, held in capacitor C_2, after S_3 is opened. The same operation is iterated with capacitors C_1-C_4 to compute the average of the third and fourth samples that will be held in C_4. The average of the first four samples is then computed by connecting C_2 and C_4 through a short pulse of the signal controlling S_4 and held in C_2. As shown in Fig. 2, these operations are repeated in the same way to compute the average of the next four samples that will be held in C_4. Then S_4 is closed in order to calculate the average of the first 8 samples. After the charge transfer from the PPD to the sense node, the same operation is repeated by substituting the capacitor C_4 by capacitor C_5. This is done by opening the switch S_{AV1} and closing the switch S_{AV2} and S_8. This operation results in averaging 8 consecutive samples of voltage levels after the charge transfer held in capacitor C_5. The final result is obtained by subtracting the two averages (reset and transfer levels) by opening S_8 and closing S_9 and S_{10}. In this way the difference of the two averages is calculated in an analog and passive way without any impact on the dynamic range. In addition, computing the averages by connecting the different capacitors of the network is much faster than performing multiple analog to digital conversion that would allow performing CMS in the digital domain [1]. Indeed, the line readout times corresponding to each CMS order, shown in Table II, range between 22 and 43 μs.

TABLE II
FULL LINE READOUT TIME

CMS order M	**2**	**4**	**8**
Readout time [μs]	22	31	43

IV. Simulations Results

In order to validate the impact of the combination of an advanced technology (65 nm) together with an optimal design of the SF, column-level amplification and analog CMS, transient noise simulations are performed for the readout chains based on the three different in-pixel SFs, using ELDO transient simulator. Transient noise simulations have shown good matching with experimental results in [5] for both

thermal and flicker noise. A parametric simulation is first performed in order to evaluate the overall conversion gain of each readout chain. Then the noise voltage, evaluated at the output, is referred at the input as an equivalent noise charge. The simulated pixel conversion gain are $145\,\mu V/e^-$ for the *n*MOS2.5, $140\,\mu V/e^-$ for the *p*MOS2.5 and $162\,\mu V/e^-$ for the *p*MOS1.2. Thermal, flicker and leakage current shot noise are now analyzed separetely.

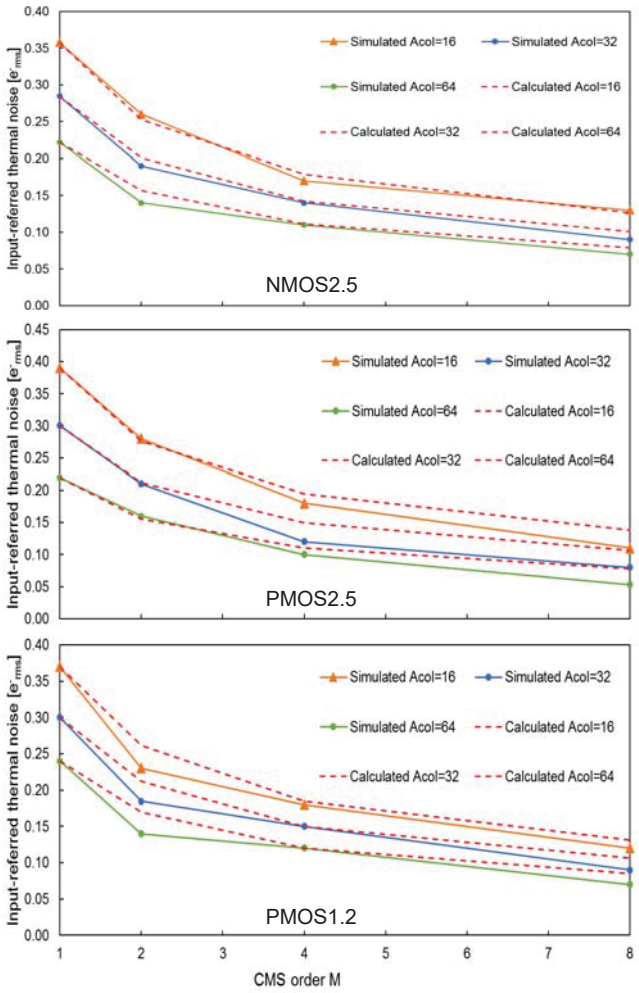

Fig. 3. Input-referred thermal noise of the CIS readout chain with nMOS2.5, pMOS2.5 and pMOS1.2 SF, respectively, as function of the column-level gain and the CMS order M.

1) Thermal noise: The input-referred thermal noise, obtained from transient noise simulations, is shown in Fig. 3, as a function of the CMS order *M* and the column-level gain A_{col}, for each of the three pixel configurations. The curves show that both the column-level gain and an increased CMS order reduce the thermal noise. The decrease in the input-referred thermal noise due to the CMS is proportional to $\sqrt{\mathrm{M}}$, as expected by [9]. The mismatch between simulated and expected values can be explained by the additional bandwidth limitation that the switched capacitors introduce at the output of the column amplifier, further reducing the thermal noise contribution. For a column-level gain of 64, a C_{L} of 200 fF and a CMS order equal to 8, the input-referred thermal noise of each configuration is well below $0.1\,\mathrm{e^-_{rms}}$. In fact, both the readout chain based on *n*MOS2.5 and *p*MOS1.2 feature an input-referred thermal noise of $0.07\,\mathrm{e^-_{rms}}$, while the *p*MOS2.5 features a noise level of $0.05\,\mathrm{e^-_{rms}}$. This confirms that the 1/f noise, analyzed in the next section, under this condition is dominant.

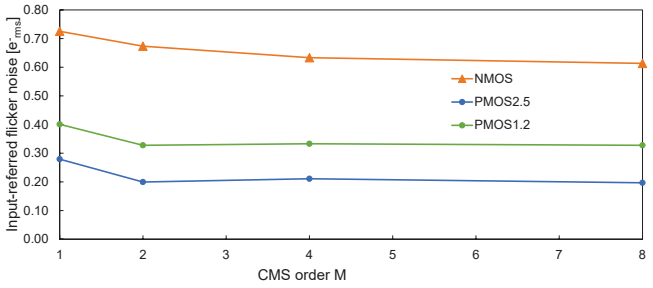

Fig. 4. Input-referred flicker noise of the CIS readout chain with different type of in-pixel SFs, as function of the CMS order M.

2) 1/f Noise: Fig. 4 shows the results of 1/f noise simulations for each of the three readout chains shown in Fig. 1. As expected in the previous section, the pMOS1.2 and the pMOS2.5 exhibit the lowest input-referred flicker noise. The impact of CMS can be appreciated from Fig. 4 for the three readout chains. The 1/f noise reduction, as a function of CMS order, reaches a plateau after CMS of order 4, as expected theoretically in [9]. The step between CMS of orders 2 or 4 and simple CDS ($M = 1$) is interesting. This step is due to the fact that for a simple CDS the input-referred flicker noise depends on the ratio between the sampling interval (T_{CDS}) and the signal settling time (τ), which cannot be controlled precisely. On the other hand, for a CMS of order 2 or more, the input-referred flicker noise is approximately independent of the T_{CMS}/τ. Fig. 4 shows that combining the pMOS2.5 as SF and using CMS of order 2 or higher, an input-referred flicker noise as low as $0.20\,\mathrm{e^-_{rms}}$ is reached, in contrast to $0.32\,\mathrm{e^-_{rms}}$, obtained when a simple CDS is used with a $\mathrm{T_{CDS}}$ of 7 μs.

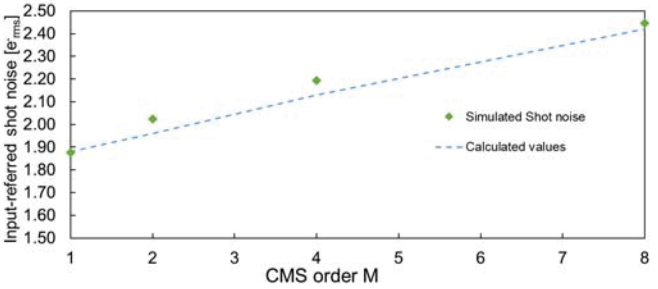

Fig. 5. Input-referred shot noise of the CIS readout chain with pMOS1.2 SF.

3) Shot Noise: It is known that the gate tunneling current depends exponentially on the oxide thickness. For state of the art CIS processes (larger than 100 nm technology node), the gate leakage current has been negligible, but in a 65 nm process the latter increases by several orders of magnitude. The

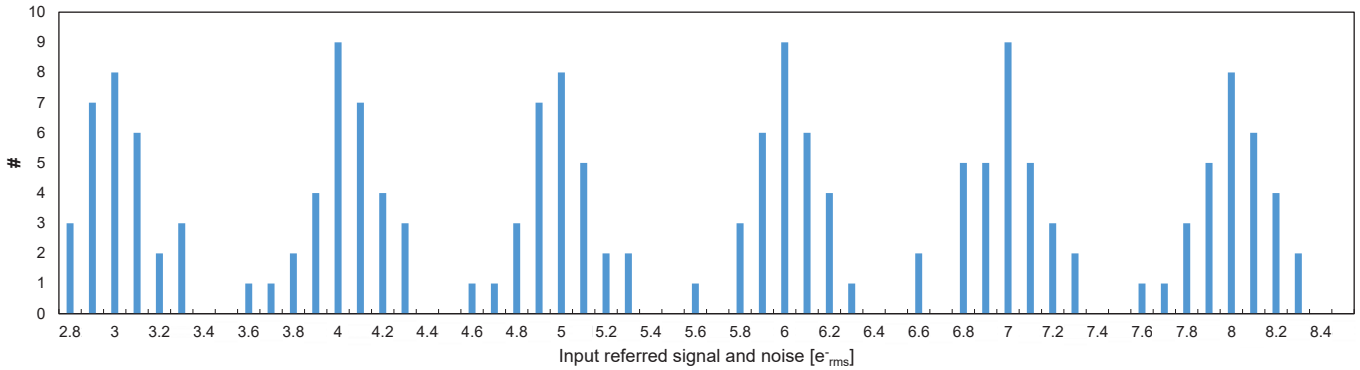

Fig. 6. Histogram of the output signal voltage for 6 different inputs.

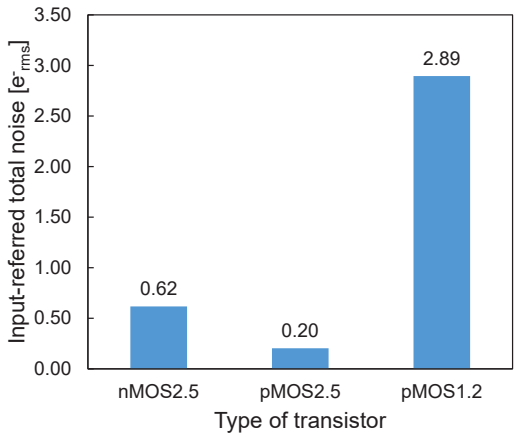

Fig. 7. Input-referred total noise of the CIS readout chain with the NMOS2.5, PMOS2.5 and PMOS1.2 SF, respectively.

gate leakage tunneling current is associated with a shot noise. In the 65 nm process simulated in this work, the pMOS1.2 transistor is the only one considerably concerned by this phenomena, due to its low oxide thickness, below 3 nm. In [6], it has been shown that the variance of the leakage current shot noise at the level of the SF increases linearly with the CMS order, starting from $M = 2$. Hence, the input-referred shot noise is expected to increase with $\sqrt{M}$. Fig.5 shows the simulated input-referred gate leakage shot noise together with the theoretical values based on [6]. The input-referred shot noise appears to dominate the other noise sources for this thin oxide transistor.

4) Photoelectron counting possibility: Based on the previous results, the input-referred total noise has been calculated and shown in Fig. 7, for a A_{col} of 64 and a CMS of order 8. The pMOS2.5 transistor appears to be the best choice as in-pixel SF. Thanks to the combination of an advanced process, an optimized pixel, a high column-level gain and CMS, the total noise of the readout chain based on the pMOS2.5 SF has been reduced to the extremely low value of $0.20\,\text{e}^-_{\text{rms}}$. The noise performance of the readout chain based on PMOS2.5 SF gives the possibility of a true photoelectron counting. Fig. 6 is the histogram of the input-referred signal when injecting in the sense node a number of electrons ranging from 3 to 8. The histogram shows that the number of electrons can be easily quantified, thanks to the values of the valeys going down to zero.

V. Conclusion

In this work the combination of using an advanced process, pixel SF optimization, column-level gain and CMS is investigated by transient noise simulation. the simulations show that an input-referred noise as low as $0.20\,\text{e}^-_{\text{rms}}$ can be reached with pMOS2.5 SF, $M = 8$ and $A_{\text{col}} = 64$. The simulated noise histogram shows that in such conditions, photoelectron counting can be envisaged with a standard CIS process. This paper also shows that CMS increases the gate leakage shot noise, which might be a concern with SF transistors presenting considerable leakage current, higher than 10 fA.

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