820 V GaN-on-Si Quasi-Vertical P-i-N Diodes with BFOM of 2.0 GW/cm^2

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***Abstract*— In this work we demonstrate GaN-on-Si p-i-n diodes with high breakdown voltage (BV) and state-of-the-art Baliga's Figure of Merit (BFOM) among GaN-on-Si vertical devices. The growth and doping of the GaN drift layer were optimized, leading to a remarkable electron mobility of 720 cm^2/Vs for a Si doping level of 2×10^{16} cm^{-3}. With a 4 µm-thick drift layer, we achieved an excellent breakdown voltage of 820 V and ultra low specific on resistance ($R_{on,sp}$) of 0.33 mΩcm^2. This results in a BFOM of 2.0 GW/cm^2, the highest value reported for GaN-on-Si vertical diodes. These results reveal the excellent prospect of GaN-on-Si for cost-effective vertical power devices.**

***Index Terms* – GaN vertical power devices, GaN-on-Si, high breakdown, quasi-vertical, p-i-n diodes.**

I. Introduction

GaN-based devices have the capability to work at higher voltages, temperatures and switching frequencies with higher efficiencies as compared to existing Si devices [1]. This emanates from the superior properties of GaN such as higher bandgap, saturation velocity, electron mobility and critical electric field as compared to Si [2]. Lateral GaN electronic devices such as HEMTs [3]–[7] have been extensively researched upon and are already commercially available for the 200-600 V power applications. However, these devices suffer from poor scalability, limited breakdown voltage compared to the GaN capability, and reliability issues [8], [9].

A vertical structure is more suitable for high power applications as it offers better scalability, higher current density, larger breakdown voltages, and lower sensitivity to traps and surface states [10]. Recently reported vertical devices on low defect density epitaxial layers grown on high-quality bulk GaN substrates have reached nearly ideal performance, thus reaffirming the choice of GaN vertical devices for future power applications [11]–[17]. However, these substrates are available only in small diameters and are prohibitively expensive. Hence, for the future adoption and commercialization of GaN vertical power devices, it would be desirable to develop such devices in low-cost substrates, such as Silicon. Recent demonstrations of GaN-on-Si p-i-n diodes [18]–[23], as well as vertical GaN-on-Si power MOSFETs, reaching a BV of 645 V [24],

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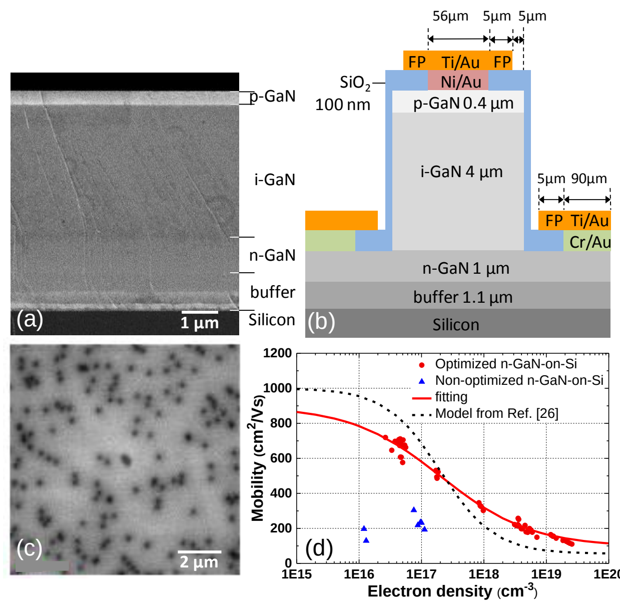

Fig. 1. (a) Cross sectional scanning electron microscope (SEM) image of the GaN-on-Si wafer revealing clearly the different layers. (b) Simplified schematic of the fabricated p-i-n diode on GaN-on-Si. (c) Cathodoluminescence (CL) image of the as-grown GaN layer on Si. (d) Electron mobility versus electron density of the optimized and non-optimized n-GaN layers compared against the model from Ref. [26].

reveal the great promise of such substrates. Fully vertical p-i-n diodes have also been demonstrated by substrate removal reaching a *BV* up to 500 V [19]. However, these values are much below the performances demonstrated in bulk GaN and for their use in practical applications, both the *BV* and the $R_{on,sp}$ need to be significantly improved.

In this letter, we report quasi-vertical GaN-on-Si p-i-n diodes with *BV* of 820 V, achieved using a 4 µm-thick GaN drift layer while earlier reports on p-i-n diodes fabricated on GaN-on-Si used drift layer thicknesses of about 2-2.7 µm [18]–[22]. The doping of the GaN drift layer was optimized, leading to a remarkable electron mobility of 720 cm^2/Vs with a Si doping level of 2×10^{16} cm^{-3}. In the forward conduction, these diodes demonstrated a very low $R_{on,sp}$ of 0.33 mΩcm^2 at 6.4 V and current density over 10 kA/cm^2 at 10 V with excellent stability at higher temperatures. In reverse bias, the devices presented low leakage current of 4×10^{-2} A/cm^2 at -500 V. These results yield a BFOM of 2.0 GW/cm^2 which is more than 6x-larger than the best value reported to date in GaN-on-Si p-i-n diodes [19].

II. Device Structure and Fabrication

The p-i-n epitaxial structure consisted of 0.4 µm-thick p-GaN (N_A ~ 3×10^{17} cm^{-3}), 4 µm-thick GaN drift layer (N_D ~ 2×10^{16} cm^{-3}), 1 µm-thick n-GaN (N_D ~ 10^{19} cm^{-3}) and 1.1 µm-thick buffer layer grown on p-type Si, as shown in Fig. 1(a) and (b). All the GaN layers were grown by metal-organic chemical vapor deposition (MOCVD) on 6-inch Si (111) substrates.

High quality buffer layers with low defect densities are important to grow thick GaN-on-Si with low threading dislocation densities, especially the AlN nucleation layer. AlN on Si with high crystalline quality with (002) X-ray rocking curve (XRC) of less than 1000 arc sec and smooth surface was obtained by optimizing the AlN growth. With high-quality buffer layer, thick GaN on Si was grown without relaxation of the compressive stress during growth. High-resolution x-ray diffraction (HRXRD) was used to characterize the crystalline quality of the as-grown p-i-n structure on Si. The full width at half maximum (FWHM) of the X-ray omega rocking curves for (002) and (102) orientations were 235 arcsec and 307 arcsec, respectively. From the FWHM values we estimated a threading dislocation density (TDD) of 2.95×10^{8} cm^{-2} through empirical equations from Refs. [25]. A similar TDD of about 2.0×10^{8} cm^{-2} was obtained from cathodoluminescence (CL) microscopy of the GaN grown on Si as shown in Fig. 1(c). In addition to TDD, impurity control such as carbon, silicon and oxygen is also critical. To achieve high breakdown voltage and low leakage current in GaN diodes, the background impurities, including both Si and O, have to be controlled to less than 1×10^{16} cm^{-3}. Large O or Si background concentrations, for example, in the range of 1×10^{17} cm^{-3}, require intentional carbon doping to compensate the shallow donors of Si or O in order to achieve high breakdown voltage. However, the presence of C may significantly degrade the electron mobility of Si-doped n-GaN. As it is shown in Fig.1(d), the non-optimized n-type GaN sample, which has a relatively high C concentration of ~ 8×10^{16} cm^{-3}, presented an electron mobility of ~ 200 cm^2/Vs at a doping level of 1×10^{17} cm^{-3}. By tuning the growth parameters, the C concentration was reduced to less than 1×10^{16} cm^{-3}, leading to a much larger mobility of 720 cm^2/Vs at a Si doping level of 2×10^{16} cm^{-3}. Furthermore, from SIMS measurements of our un-intentionally doped GaN samples, the Si or O background level was below 1×10^{16} cm^{-3}, and thus not requiring extra C doping. Fig. 1(d) shows the mobility of n-GaN/i-GaN/buffer/Si samples as a function of electron density obtained using an Accent HL5500 Hall system [26].

The fabrication process of the quasi-vertical diodes (Fig. 1(b)) started with the activation of p-GaN by thermal annealing in N_2 ambient at 750 ºC for 15 min. The p-electrode layer was formed by Ni (20 nm)/Au (50 nm) subsequently annealed at 480 ºC in N_2/O_2 ambient for 10 min for ohmic contact formation. This was followed by mesa isolation through a deep etching of GaN using inductively coupled plasma-reactive ion etching (ICP-RIE) to access the bottom n-GaN layer. The sample was then treated with 25% Tetra Methyl Ammonium Hydroxide (TMAH) at 85 ºC for 1 hour to smoothen the sidewalls and heal the damages occurred during the deep-etching step. Cr (50 nm)/Au (250 nm) bi-layer was deposited for ohmic contact to n-GaN. The etched sidewalls were passivated with 100nm-thick SiO_2, deposited by atomic layer deposition (ALD), and the field plates (FP) were formed with Ti (50 nm)/Au (300 nm) bi-layer (Fig. 1(b)).

III. Results And Discussion

Fig. 2(a) shows the forward current density versus voltage (*J-V*) characteristics and the specific on-resistance ($R_{on,sp}$) of p-i-n diodes with passivation and FP. We observed no difference in the forward characteristics between the passivated and the un-passivated devices. The diode anode diameter was 56 µm. The turn-on voltage (V_{on}), extracted at a current density of 20 A/cm^2 was 3.3 V which is close to the bandgap of GaN. The $R_{on,sp}$ extracted from the forward *J-V* plot at 6.4 V was 0.33 mΩcm^2, while the equivalent on-resistance calculated by voltage over current at 6.4 V was 1.56 mΩcm^2. For quasi-vertical diodes, the on-resistance is mainly determined by the current crowding in the n-GaN layer towards the n-GaN contact [27], which was significantly alleviated in these devices due to the highly doped 1 µm-thick n-GaN layer presenting a low sheet resistance of 26 Ωcm. For larger anode contacts, we

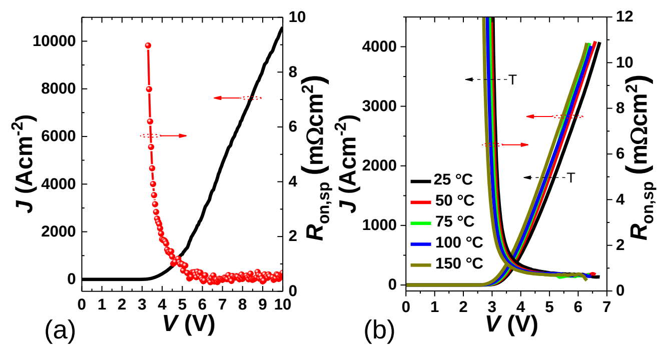

Fig. 2. (a) Forward *J-V* and specific on-resistance measurement. (b) Forward *J-V* and specific on-resistance measurement at various temperatures.

observed an increase in $R_{on,sp}$ since the higher current leads to a much more severe current crowding at the n-GaN layer. Current crowding can be further reduced by modifying the device structure from a quasi- to a fully-vertical structure, by substrate removal for instance [20]. Another main contribution to the $R_{on,sp}$ comes from the thick drift layer, which was minimized in our devices by optimizing the electron mobility and doping of the GaN drift layer. This resulted in a much smaller $R_{on,sp}$ than in previous reports of GaN-on-Si p-i-n diodes, even compared to fully vertical structures [18] and to devices with larger doping in n-GaN layers [19].

Our diodes presented a very high current density (normalized by the anode surface), larger than 10 kA/cm^2 at 10 V, which to our knowledge is the highest value reported for GaN diodes grown on foreign substrates [18]–[23], [28]–[30]. Despite the thick GaN layers grown on Si, a small ideality factor of 2.56 was extracted at a forward voltage of 2.4 V, reflecting the excellent quality of the epitaxial layers.

Fig. 2(b) shows the temperature dependence of the forward *J-V* characteristics. As expected, the turn-on voltage decreased at higher temperatures due to bandgap narrowing and thermally-enhanced carrier diffusion. We observed very little change in $R_{on,sp}$ and drift in the current density with temperature, as opposed to degradation or inconsistencies observed in

previously reported papers [19], [20]. These excellent results are comparable to fully vertical diodes fabricated on GaN substrates [14], [36].
Fig. 3(a) shows the reverse current density versus voltage (*J-V*) curve of the diode in logarithmic scale, performed on an insulating chuck. The *BV* of the diode without FP was 700 V, which was significantly improved to 820 V by the 5 µm-long FP (Fig. 1(b)), corresponding to an average electric field in the

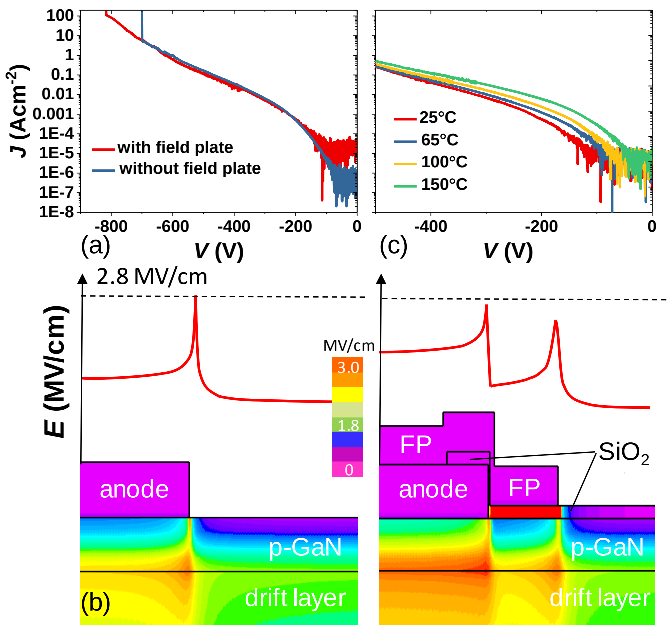

Fig. 3. (a) Reverse *J-V* measurement (b) Simulated electric field in a non-terminated (at 690 V) and terminated diode (at 823 V). (c) Reverse *J-V* measurement at various temperatures.

drift layer of 2.1 MV/cm. To the best of our knowledge, this is the highest *BV* among all previously reported quasi/fully-vertical GaN-on-Si p-i-n diodes. This enhancement was confirmed by 2D-TCAD simulations as shown in Fig 3(b). For a non-terminated anode, the electric field at a reverse bias of 690 V peaks at the edge of the electrode at about 2.8 MV/cm. The field plate spreads the electric field in two peaks at the edge of the anode and of the FP, resulting in an electric field peak of ~ 2.7 MV/cm at a much higher voltage of 823 V.

The measured leakage current density was ~ 5×10^{-3} A/cm^2 and ~ 4×10^{-2} A/cm^2 at -300 V and -500 V, respectively. Such low reverse leakage current can be attributed to the high crystalline quality of the GaN epi layers grown on Si substrate, since it is dominated by space charge limited current (SCLC), mainly due to traps in the thick epi-layers [21], [32]. According to the model from Ref. [32], the epitaxial GaN grown on Si contains both acceptor- as well as donor- type traps. At low reverse voltages, the acceptor traps start getting filled with electrons. As the reverse voltage increases, the Fermi level moves up towards the conduction band and the ionized donor traps start getting filled. At the point where all the trap states get filled, denoting the onset of the trap filled voltage, the current increases sharply as the Fermi level reaches the conduction band. The leakage current in log-scale, prior to the trap filled voltage, is proportional to V^n. A value of n ~ 6.39 was obtained by fitting the Fig. 3(a), which is comparable to previous reports of p-i-n diodes on GaN-on-Si [20], [21]. We have not observed a significant difference in leakage current with and without passivation, which we believe is due to the effective healing of the etching damages on the sidewalls by the TMAH treatment [33]. Fig. 3(c) shows the reverse *J-V* characteristics of the diodes at different temperatures, revealing a slight increase in leakage current with temperature due to thermal carrier generation.

The performance of our diodes was benchmarked against other GaN vertical diodes reported in the literature in a $R_{on,sp}$ *vs BV* plot as shown in Fig. 4 [13,14,18-21,23,28,30,31,33–38] . The excellent *BV* of 700 V (without field plate) and 820 V of our diodes, with a small $R_{on,sp}$ of 0.33 mΩcm^2, leads to a BFOM value of 2.0 GW/cm^2, which is more than 6x-larger than the best value reported for p-i-n diodes fabricated on GaN-on-Si [19].

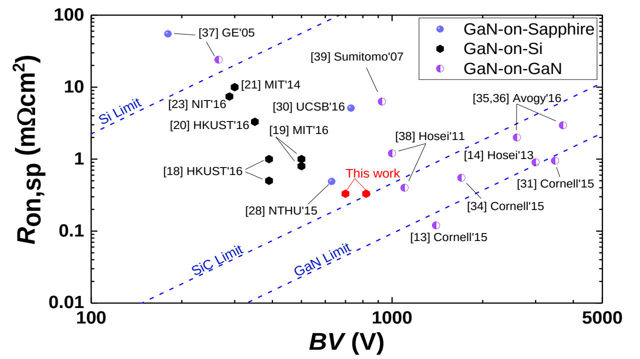

Fig. 4. Benchmarking of our GaN-on-Si diodes against those reported in literature using $R_{on,sp}$ and *BV* as parameters.

IV. Conclusions

In this work we demonstrated a high performance quasi-vertical GaN-on-Si p-i-n diode with record performance, achieved with a drift layer with 4 µm-thick drift layer. The growth and doping of the GaN drift layer were optimized, leading to a remarkable electron mobility of 720 cm^2/Vs for a doping level of 2×10^{16} cm^{-3}. A low $R_{on,sp}$ of 0.33 mΩcm^2, high forward current density of 10 kA/cm^2 at 10 V, and a record breakdown voltage of 820 V were achieved. As a result, our diodes presented a BFOM of 2.0 GW/cm^2, which is the best achieved on GaN-on–Si diodes. These results demonstrate the enormous potential of GaN-on-Si diodes for low-cost high-voltage power devices.

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VI. References

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