Nanoionics Phenomena and Devices with Oxide Thin Films

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Abstract

The number of studies on solid state ionic thin films (Nanoionics) has increased dramatically over last decades due to their high potential in micro and nano scale technologies. Micro solid oxide fuel cells (µSOFC), and resistive switching memories (ReRAMs) are the most promising topics in this field, having impacts on portable energy sources, and future non-volatile memories. One can also add the new discovery of giant electrostriction (GES) in Gd doped ceria (CGO), proposing ion conducting thin films as a new electromechanical family. While very astonishing results have been obtained, there are still some remaining challenges that are needed to be addressed: a) Mechanical stability in µSOFC, b) performance study of classically known fast ion conducting -i.e. yttrium stabilized zirconia (YSZ) and CGO- in ReRAMs, and c) Investigating and understanding of the acting mechanism leading to novel properties in CGO thin films.

In µSOFC we have proposed a ring-shaped corrugated structure that can result in more stable membranes up to millimeters wide openings. Stable liberation borders, low mechanical buckling, increased area density in given volume, and high surface utilization are the main characteristics of such membranes. The electrochemical performance of a 500 µm wide µSOFC cell has been measured at 350°C and a power density of 12.5 mW/cm^2 has been obtained. This value is close to the reported performance in the literature at the same temperature. An open circuit voltage of 0.7 V was achieved. It is not clear whether the expected value of 1.1 V was missed due to gas or electron leakage. The optimal membrane diameter in a single PEN cell (Positive electrode-Electrolyte-Negative electrode) was identified as 0.5 mm. For upscaling to several Watts of electrical output, it is proposed to fabricate a planar array of such cells.

Furthermore, we have studied the potential of CGO and YSZ thin films to be used as switching layer in ReRAMs. Both films have shown outstanding electrical characteristics comparable to high-performance switching materials with high stability and endurance. CGO thin films are able to operate at V_{set} = 1 V and V_{reset}= -0.6 V over multiple cycles. YSZ thin films switch between V_{set} = 1.1 V and V_{reset}= -0.6 V. Both cells have shown stable response over 10^4 cycles with ON/OFF ratio of 100 and 5 for CGO and YSZ, respectively. It turned out that the switching mechanism in CGO films is rather of multi-filamentary mechanism as the low resistance state (LRS) and forming voltage decreases with increasing the device size. In contrast, in the YSZ-based memories, less filaments are expected to be formed since the scaling effect was not clearly observed.

Finally, we have investigated the GES in CGO thin films and we succeeded to reproduce the giant response, which was found to take place only at low frequency (<1kHz). We have shown that the giant electrostriction is related to the defects which are produced during rather specific deposition parameters such as low deposition temperature, an optimal ion bombardment, and high deposition rate. It has been found that a higher oxygen vacancy concentration than introduced by Gd doping is needed. Additional oxygen vacancies are most likely compensated by the reduction of Ce^{4+} to Ce^{3+}. Furthermore, we have seen that the giant electrostriction is dependent on the material of the bottom electrode. Al leads to better results than Cr or Pt. A large dielectric constant of over 1000 was observed at low frequency reminding at the phenomenon of the colossal dielectric constant. Moreover, the films are characterized by a strong nonlinear I-V behaviour with a threshold voltage of about 10V, very much like a varistor.

Key words: Yttrium stabilized zirconium oxide, YSZ, Gadolinium doped cerium oxide, CGO, Microfabrication, Corrugated membrane, free-standing membrane, Solid Oxide Fuel Cell, SOFC, Resistive switching, Random Access Memory, RRAM, ReRAM, Memristor, Electrostriction, Dielectric constant, Varistor, non-linear I-V, Nanoionics, Oxide thin films.

Résumé

Le nombre d'études en ionique de l'état solide des couches minces (nano-ionique) a beaucoup augmenté au cours des dernières décennies, en raison du potentiel qu'elles offrent en microtechnologie et nanotechnologie. Les micro-piles à combustible à oxyde solide (uSOFC, selon l'acronyme anglais) et les mémoires vives à commutation résistive (ReRAMs, selon l'acronyme anglais) sont les objets les plus prometteurs de cette discipline, de par leur impact sur la technologie des sources d'énergie portables et sur le futur de la technologie des mémoires non-volatiles, respectivement. A cela s'ajoute la découverte récente d'un phénomène d'électrostriction géante (GES, selon l'acronyme anglais) dans les films d'oxyde de cérium dopés au gadolinium (CGO), élargissant la famille des matériaux offrant un couplage électromécanique aux conducteurs ioniques en couche mince. Même si des résultats stupéfiants ont déjà été obtenus, de nombreux défis restent à relever : a) la stabilité mécanique des uSOFC ; b) l'étude des performances dans les ReRAMs des conducteurs ioniques rapides classiques tels que l'oxyde de zirconium stabilisé à l'yttrium (YSZ) et le CGO ; c) l'étude et la compréhension des mécanismes à l'œuvre dans les nouvelles propriétés découvertes dans les couches minces de CGO.

Concernant les uSOFC, nous avons proposé une structure annulaire ondulée qui permet aux membranes de conserver leur stabilité mécanique pour des ouvertures allant jusqu'à plusieurs millimètres. Ces membranes ont pour principales caractéristiques des jointures stables entre le corps fixe et la membrane libérée, un faible flambage, une plus grande surface pour un volume donné, et une grande surface utile. Les performances électrochimiques d'une uSOFC de 500um de large ont été mesurées à 350°C, et une densité de puissance de 12.5mW/cm^2 a été obtenue. Cette valeur est proche des performances à la même température publiées dans la littérature. Une OCV de 0.7V a été obtenue. Il n'est pas encore clair si la valeur attendue de 1.1V n'a pas été atteinte à cause d'une fuite de gaz ou bien d'une fuite d'électrons. Le diamètre optimal de la membrane d'une cellule PEN a été déterminé et se monte à 0.5 mm. Pour atteindre plusieurs Watt de puissance de sortie, il est proposé de fabriquer un réseau planaire de ces cellules.

De plus, nous avons étudié le potentiel des couches minces de CGO et de YSZ pour les applications de ReRAMs. Les deux types de films montrent d'excellentes caractéristiques électriques, comparables aux matériaux à commutation résistive de haute performance, avec une stabilité et une endurance élevées. Les couches minces de CGO sont capables de fonctionner avec un Vset de 1V et un Vreset de -0.6V durant de multiples cycles.

Les couches minces de YSZ changent de résistance entre Vset = 1.1V et Vreset = -0.6V. Les deux types de cellule conservent une réponse stable sur 10^4 cycles avec un ratio ON/OFF de 100 pour le CGO et de 5 pour le YSZ. Le mécanisme de commutation résistive des films de CGO est du type multi-filamentaire, puisque la résistance de l'état de basse résistance ainsi que le voltage de formation diminuent tous deux lorsque la taille du dispositif augmente. Au contraire, ce phénomène d'échelle n'est pas clairement observé pour les mémoires basées sur les couches minces de YSZ, ce qui suggère la formation d'un nombre limité de filaments.
Enfin, nous avons étudié la GES dans les couches minces de CGO et nous avons réussi à reproduire la réponse géante, qui n'a été observée qu'à faible fréquence (moins de 1kHz). Nous avons montré que l'électrostriction géante est liée à la présence de défauts dans la couche, qui ne sont produits que pour des paramètres de dépôts bien spécifiques, tels qu'une faible température de dépôt, un bombardement ionique optimal, et une vitesse de dépôt élevée. Nous avons découvert qu'il est nécessaire que le film contienne une densité de lacunes d'oxygène plus élevée que celle introduite par le dopage au Gd. Les lacunes supplémentaires sont le plus probablement compensées par la réduction des ions Ce^{4+} en ions Ce^{3+}. En outre, nous avons observé que la magnitude de l'électrostriction géante dépend du matériau employé pour l'électrode inférieure. L'aluminium fournit de meilleurs résultats que le chrome ou le platine. Une constante diélectrique élevée, supérieure à 1000, a été observée à basse fréquence, ce qui rappelle le phénomène de constante diélectrique colossale. De plus, les films ont un comportement courant-tension fortement non linéaire, avec un voltage seuil d'environ 10V ; ce comportement est très semblable à celui d'un varistor.

Mots clefs : oxyde de zirconium stabilisé à l'yttrium, YSZ, oxyde de cérium dopé au gadolinium, CGO, microfabrication, membrane ondulée, membrane libre, pile à combustible à oxyde solide, SOFC, changement de résistance, mémoire vive, RRAM, ReRAM, memristor, électrostriction, constante diélectrique, varistor, caractéristique courant-tension non linéaire, nano-ionique, couches minces d'oxyde.

Contents

Acknowledgements **i**

Abstract (English/Français) **iii**

List of Figures **xi**

List of Tables **xv**

List of Acronyms **xvii**

1 Introduction **1**
1.1 Towards Nanoionics 1
1.2 Nanoionics: Applications and Challenges 2
1.3 Objective of This Thesis 3

I Portable Solid Oxide Fuel Cell (SOFC) **5**

2 Micro Solid Oxide Fuel Cells **7**
2.1 Introduction 7
2.2 Solid Oxide Fuel Cells Principle 9
2.3 PEN Elements 11
2.4 Thermal-Mechanical Stability 14
2.5 State of The Art 20
2.6 Complete µSOFC Device 21

3 Thin films study: Deposition and Characterization **23**
3.1 Thin Films Deposition 23
3.1.1 Sputtering Technique 23
3.1.2 Atomic Layer Deposition (ALD) 24
3.2 Characterization Methods 25
3.2.1 Microstructure Characterization 25
3.2.2 DC Conductivity 25

3.3 Electrolyte Layer . . . 26
3.3.1 Yttrium Stabilized Zirconia (YSZ) . . . 26
3.3.2 Hafnium Oxide (HfO_2) . . . 30
3.4 Porous Electrodes: Platinum . . . 33

4 μSOFC Device Fabrication and Characterization 37
4.1 Corrugated Structure . . . 37
4.1.1 Substrate Patterning . . . 37
4.1.2 Corrugation Design . . . 40
4.2 μSOFC Device Fabrication Process Flow . . . 41
4.3 Membrane Mechanical Buckling . . . 43
4.4 Electrochemical Performance of μSOFC Devices . . . 44
4.5 Summary . . . 47

II Resistive Random Access Memories (ReRAMs) 49

5 Physical Principle and Status 51
5.1 Towards Resistive Switching Memories . . . 51
5.2 ReRAM Characteristics and Switching Mechanisms . . . 53
5.3 General Requirements . . . 57
5.4 Thin Films in Use . . . 58
5.4.1 CeO_2 based ReRAMs . . . 59
5.4.2 ZrO_2 based ReRAMs . . . 61

6 ReRAM Device Fabrication and Characterization 63
6.1 Device Fabrication . . . 63
6.2 Characterization Methods . . . 66
6.2.1 DC I-V Characterization . . . 66
6.2.2 AC Pulse Measurement . . . 66
6.3 CGO-Based ReRAMs . . . 67
6.4 YSZ-Based ReRAMs . . . 71
6.5 Electrical Forming Process . . . 73
6.6 Summary . . . 75

III Novel Properties in Gadolinium Doped Ceria (CGO) 77

7 Giant Electrostriction (GES) in CGO: Principle and Status 79
7.1 Electrostriction . . . 79
7.2 Proposed Mechanism . . . 80
7.3 Effect of Frequency and Temperature . . . 83

8 Electrochemical and Dielectric Properties in CGO Thin Films **85**
8.1 Electrostriction Coefficients in Thin Films 85
8.2 Experimental Methods 87
8.2.1 Thin Film Synthesis and Sample Fabrication 87
8.2.2 Structural Characterization 87
8.2.3 Electromechanical Measurement Setup 88
8.2.4 Nanoindentation 88
8.2.5 Dielectric Spectroscopy 89
8.2.6 Electrical Characterization 89
8.2.7 Raman Spectroscopy 90
8.3 Results and Discussion 90
8.3.1 Microstructure Effect 90
8.3.2 Ion Bombardment Effect 95
8.3.3 The Effect of Excitation Frequency 96
8.3.4 Dielectric Spectroscopy 97
8.3.5 Dielectric Properties at High Temperature 103
8.3.6 Non-linear Electrical Properties 105
8.3.7 The effect of Joule heating 106
8.3.8 Raman Spectroscopy 110
8.4 Summary 111

IV Summary and Outlook **113**

Thesis Summary **115**

Thesis Outlook **119**

Bibliography **121**

Curriculum Vitae **137**

List of Figures

2.1 Energy need and power source capacitance of cell phones versus time . . 7
2.2 Specific energy and energy density of available portable energy sources . 9
2.3 Schematic of SOFC working principle 10
2.4 Three main polarization mechanisms of fuel cells 11
2.5 Optical images of free standing membrane 15
2.6 The cross-section of corrugated membrane. 16
2.7 Corrugated membrane proposed by Prinz group [55, 14] 18
2.8 µSOFC mebrane supported with metallic grid proposed by Muralt group[25] 19
2.9 µSOFC membrane supported with metallic grid proposed by Ramanthan group[37] 19
2.10 Supported µSOFC mebrane, anodic aluminum oxide substrate [59] 20
2.11 Layout of ONEBAT µSOFC systems, adopted from [68] 22

3.1 Nordiko, RF magnetron sputtering system, configuration. 24
3.2 The schematic view of test structures, Pt/electrolyte/pPt. 25
3.3 YSZ thin films XRD pattern and surface morphology 28
3.4 Arrhenius plot of YSZ thin films with different microstructure 29
3.5 XRD pattern and morphology of HfO_2 thin films 31
3.6 Ion conductivity of HfO_2 thin films 31
3.7 YHfO XRD pattern and surface morphology 32
3.8 Ion conductivity of 30% yttrium doped HfO_2 thin film 33
3.9 SEM micrographs of porous platinum deposited at high pressure 34
3.10 SEM micrographs of porous platinum deposited with substrate rotation . 35

4.1 LOCOS process schematic and SiN stress trenches 38
4.2 Silicon topology as function of etchant composition [95] 39
4.3 AFM analysis for surface roughness measurement after wet etching of silicon with two different diluent a) H_2O (PolySi) b) CH_3COOH (HNA) . 39
4.4 Etch profile of 50 µm wide cavity using HNA solution 40
4.5 Fabrication process flow of ring-shaped corrugated SOFC membrane. . . . 42
4.6 Etching profile with HNA solution and concave sidewalls 43
4.7 Mechanical buckling of 750 µm liberated membrane 43

4.8 Membrane displacement after substrate liberation as function of device opening . . . 44
4.9 Electrochemical performance measurement setup . . . 45
4.10 I-V characteristics of 500 µm wide µSOFC . . . 45
4.11 Comparison of Ohmic and activation polarization at 350°C operation temperature for 500 µm wide µSOFC . . . 47

5.1 The memory storage hierarchy . . . 52
5.2 a) Unipolar Switching mode, b) Bipolar Switching mode [106] . . . 53
5.3 Schematic view of filamentary switching in ECM memories . . . 54
5.4 Illustration of switching process in metal-oxide-metal ReRAM [108] . . . 55
5.5 Resistance scaling in interface-type switching with the device size[109]. . . 56
5.6 Interface-type switching schematic in Resistive switching . . . 57
5.7 Materials in use for resisteve random access memories (ReRAMs) . . . 58
5.8 Gd:CeO resistive switching under UV light . . . 61

6.1 ReRAM fabrication using the shadow mask technique . . . 64
6.2 Process flow of ReRAM fabrication using the shadow mask technique . . 65
6.3 Schematic of electrical measurements setup in a) DC mode. b) Pulse mode operation . . . 66
6.4 I-V characteristics of 14 nm CGO thin films for ReRAMs . . . 67
6.5 Device size dependence of resistive switching in CGO thin films . . . 69
6.6 Schematic view of possible mechanism for resistive switching in CGO thin films . . . 69
6.7 CGO resistive switching endurance over multiple cycles . . . 70
6.8 I-V DC electrical characteristics of YSZ thin films . . . 72
6.9 AC pulse electrical measurement for YSZ endurance characterization . . . 73
6.10 Forming voltage scaling model . . . 74
6.11 Forming voltage versus via diameter for CGO (14nm), HfO_2 (5nm) and YSZ (20 nm) ReRAM. . . . 74

7.1 Electrostrictive strain coefficient (M) (m^2/V^2) versus dielectric constant . . 80
7.2 Lattice view of Gd-Doped Ceria crystal structure [163] . . . 81
7.3 Amplitude of the in-plane stress as a function AC voltage at 10 mHz when DC voltage was switched off [19] . . . 81
7.4 Scheme of the electric field induced reorganization of a distorted Ce near neighbor coordination shell containing an oxygen vacancy [165] . . . 83
7.5 Frequency and voltage dependency of electromechanical of CGO at 2nd harmonic . . . 83
7.6 Effect of electric pulse, temperature and frequency on ES response of CGO 84

8.1 Test structre for electromechanical characterizaiton, CGO thin films . . . 87

8.2 Electromechanical characterization steup schem 88
8.3 Effect of deposition temperature on ES response of CGO thin films 91
8.4 STEM-EDAX line scan of CGO thin films deposited on different elecrodes 92
8.5 TEM dark field images of CGO thin films deposited on different electrodes 93
8.6 In-plane stress change of CGO deposited on different BE 94
8.7 HAADF TEM image of full CGO film thickness 95
8.8 In-plane stress change as funciton of frequency 97
8.9 Dielectric properties of CGO thin films deposited on a) Pt and b) Al bottom electrode 100
8.10 HR-TEM images of bottom electrode interface for CGO/Al and CGO/Pt samples 100
8.11 Schematic of equivalent circuit considering MW and UDR relaxation as the main mechanism governing the dielectric response when a CDC is observed in CGO thin films 101
8.12 Contribution of MW and UDR relaxation in the total dielectric behaviour of CGO thin films with GES 102
8.13 The contribution of Maxwell-Wagner and Jonsher's universal relaxation in overall conductivity for CGO/Pt sample 103
8.14 Temperature dependence of dielectric properties of CGO thin films deposited on Al and Pt bottom electrode at Room temperature 104
8.15 Hopping conduction activation energy for Al sample using $\ln(1/\tau)$ and Pt sample using $\epsilon''(T)$ directly (at 20 Hz and 1kHz). 105
8.16 C-V and I-V characteristics of CGO thin films deposited on Pt and Al electrodes 106
8.17 Dielectric properties and electrostrictive strain coefficient of CGO/Al film 107
8.18 Schematic view of electrostriction measurement setup with IR camera on top for tracking the temperature change. 107
8.19 Tip displacement recorded by proximity sensor, as well as the sample temperature change, as function of applied electric field. 108
8.20 Temperature profile of CGO/Al cantilever under application of an electric field 109
8.21 AC modulation of temperature under applied electric field 109
8.22 The Raman spectra of CGO thin films deposited on Al and Pt electrodes . 110

List of Tables

2.1 The comparison of energy density of different liquid fuels [23] 8
2.2 Overview of different μSOFCs 21

3.1 YSZ deposition parameters using Nordiko sputtering system 27
3.2 HfO_2 thin film deposition condition using ALD technique 30
3.3 YHfO deposition conditions 32

4.1 PolySilicon and HNA wet echting solutions 38
4.2 Studied corrugated designs 41

5.1 Studies on CeO_2 resistive switching 60
5.2 Studies on ZrO_2 based structures resistive switching 62

6.1 Pt/Ti bottom electrode deposition conditions (Spider 600) 63
6.2 CGO and YSZ switching layer deposition conditions (Nordiko Sys.) 64

7.1 Electrostriction performance of $Ce_{1-x}Gd_xO_{2-x}$ and $CeO_{2-\delta}$ thin films . . . 82

8.1 Sputter process conditions for CGO thin film deposition 87
8.2 CGO thin film composition studies by SEM-EDAX 91
8.3 CGO electromechanical and material properties 94
8.4 ES response of CGO as funciton of dep. pressure and T-S distance 96

List of Acronyms

ALD	Atomic Layer Deposition
AFM	Atomic Force Microscopy
AFC	Alkaline Fuel Cell
ASR	Area Specific Resistance
AAO	Anodic Aluminium Oxide
BHF	Buffered Hydrofluoric Acid
BE	Bottom Electrode
CGO	Gadolinium Doped Cerium oxide
CDC	Colossal Dielectric Constant
CVD	Chemical Vapor Deposition
CMP	Chemical Mechanical Polishing
CPU	Central Processing Unit
CMOS	Complementary Metal–Oxide–Semiconductor
CF	Conductive Filament
CMi	Center of MicroNanotechnology of EPFL
CC	Compliance current
CCTO	Calcium Copper Titanium Oxide
DMFC	Direct Methanol Fuel cell
DRIE	Deep Reactive Ion Etching
DRAM	Dynamic Random Access Memory
ES	Electrostriction
EDX	Energy Dispersive X-Ray Analysis
ECM	Electrochemical Metallization Cell
EXAFS	Extended X-ray Absorption Fine structure Spectroscopy
FEM	Finite Element Simulation
GES	Giant Electrostriction
HRS	High Resistance State
HNA	Nitric acid + Hydrofluoric acid + Acetic acid
HR	High Resolution
HAADF	High Angle Annular Dark Field
ISO	Isotropic Etching

IBE	Ion Beam Etching
LRS	Low Resistance State
LOCOS	Local Oxidation Of Silicon
LSC	Lanthanum Strontium Cobalt oxide
LPCVD	Low Pressure Chemical Vapor Deposition
LTO	Low Temperature Silicon Oxide
LSI	Large Scale Integration
MW	Maxwell-Wagner
MEMS	Micro-Electro-Mechanical-Systems
MIM	Metal-Insulator-Metal
MCFC	Molten Carbonate Fuel Cells
OCV	Open Circuit Voltage
PEN	Positive electrode-Electrolyte-Negative electrode
PolySi	Nitric acid + Hydrofluoric acid + water
PAFC	Phosphoric Acid Fuel Cell
PEMFC	Proton Exchange Membrane Fuel Cell
PLD	Pulsed Laser Deposition
pPt	Porous Platinum
PCRAM	Phase Change Random Access Memory
PVDF	Polyvinylindene Flouride
ReRAM	Resistive Random Access Memory
RF	Radio Frequency
RTA	Rapid Thermal Annealing
RIE	Reactive Ion Etching
SOFC	Solid Oxide Fuel Cell
SEM	Scanning Electron Microscopy
SSI	Solid State Ionic
S-T	Substrate-Target
SRAM	Static Random Access Memory
SM	Shadow Mask
SMU	Source Measure Unit
SPGU	Semiconductor Pulse Generated Unit
SAED	Selected Area Electron Diffraction
STEM	Scanning Transmission Electron Microscopy
TPB	Triple Phase Boundary
TEM	Transmission Electron Microscopy
TE	Top Electrode
UV	Ultra Violet
UDR	Universal Dielectric Response
VSI	Vertical Shift Interference

VCM	Valance Change Memory
XRD	X-ray Diffraction
YHfO	Yttrium doped hafnium oxide
YSZ	Yttrium Stabilized Zirconium oxide

1 Introduction

1.1 Towards Nanoionics

The concept of "Nanoionics" has grown dramatically in last decades due to its high potential in different application especially for energy conversion and memory devices. Nanoionics is known as a scientific and technical direction to fabricate micro and nano sized devices based on fast solid state ion conductors [1]. The physical basis is, in fact, the same as Solid State Ionics (SSI), however, at miniaturized scale, particularly with much thinner membranes. Thus, one can define Nanoionics more precisely as the synthesis, characterization, theory, and application of fast ion conducting solids at micro and nano scale.

The ionic transport phenomenon was known since 1833 when Faraday reported experiments on ionic motions in inorganic solids [2]. The effect was quickly confirmed by different studies and led to many interesting findings including *fuel cell* by Schönbein and Groove, *galvanic solid electrolyte gas cells* by Gaugain, and *electric lighting devices* by Nernst. Towards the end of 19th century, the term "solid electrolyte" was in use and many facts were known about the characteristics of these materials [3]. Albeit, the complete picture was presented by Frenkel in 1926 when he realized that an atomic species in crystalline solid cannot move before becoming a defect, a temporary deviation from the perfect crystal [4]. Meaning that ionic and electronic conductivity, as well as diffusion, are all dependent on the presence of local deviation from perfect crystalline order. This was the beginning of *defect chemistry* explaining the ion migration in solid state materials and its relation to material synthesis.

Even though the understanding of ion conduction was quite mature in the early 20s, ion conductivity in solids did not find enough interest for applications. This had been changed in the 1970s after the discovery of high ionic conductivity in solid electrolytes such as $RbAg_4I_5$ which allowed for the realization of high-power-density batteries [5, 6,

7]. The search for optimized structures and enhanced ion conductivity was also directed towards composite structures, in which the presence of an interface layer was improving the ion conductivity. The conductivity enhancement in composite structures was first discovered by Liang in 1973, who reported a 50 times ion conductivity enhancement in LiI by adding small Al_2O_3 particles [8]. The effect of interfaces has been developed mostly by Maier with introducing the concept of space-charge regions in 1995 [9]. The space charge region effect was expected to be more significant in systems with a high density of inter-phases and grain boundaries, i.e. nanostructured materials [10]. Thus, one can consider late the 20s as the initiation of Nanoionics. Moreover, the reduced thickness in thin films structures was leading to a lower ohmic loss. This was giving the possibility to miniaturized the conventional electrochemical devices such as fuel cells and gas sensor to achieve reduced operation temperature, besides miniaturization. This field found a large interest in the emerging industry of Micro Electrical and Mechanical Systems (MEMS).

1.2 Nanoionics: Applications and Challenges

The first attempt of Nanoionics was the enhancement of ion conductivity using thin film structures in order to lower Solid Oxide Fuel Cell (SOFC) operation temperature for portable applications. The idea was to embed miniaturized SOFC with Micro-Electro-Mechanical-Systems (MEMS) components and other active electronics into the same silicon wafer for portable power generation [11]. The first description of miniaturized SOFC was made in 1990 by Barnett [12] who had predicted an operation temperature of $< 750°C$ and power density of 500 mW/cm^2 for 0.5 to 10 μm yttrium stabilized zirconia electrolyte layer. The first demonstration was made by Jonkowski in 2002 working at $600°C$ with power density of 145 mW/cm^2 [13]. Nowadays, the power density has exceeded even 1 W/cm^2 [14] at only $450°C$. However, the delicate mechanical stability, and complex packaging and gas handling issues, no successful implementation by industry has been achieved yet.

Another interesting application for Nanoionics was found for non-volatile memory applications: resistive switching in thin, oxygen conducting thin films. The building block is a simple metal-insulator-metal (MIM) structure. The resistance switching is explained by either cation or anion migration into the insulating layer. While the cation migration is limited to specific materials, the anion migration is possible in almost all transition metal oxides with a high concentration of oxygen vacancies (defects). Many binary oxides, including HfO_x [15] and TaO_x [16], were studied extensively and very promising results have been obtained. However, surprisingly, YSZ and gadolinium doped ceria (CGO) as well-known fast ion conductors in SOFCs have not been investigated. Some limited works have been done on pure or slightly doped CeO_{2-x} [17, 18] but reasonably

doped structures remained untouched.

Finally, the most resent discovery in Nanoionics was giant electrostriction response in CGO thin films by Korobko et al [19], introducing ion conducting thins films as a new family of electromechanical materials. The size, and also the fact that a compressive stress is generated – in contrast to the piezoelectric effect in thin films that produces a tensile stress at equal geometry – makes this finding extremely interesting for actuators in MEMS. Since in addition, it is a lead-free material, there are excellent prospects for such applications. Electrostriction (ES) was explained by the lability of cerium and oxygen vacancy pairs leading to the possibility to reorient them with an electric field. Korobko et al [19] could also make plausible that bond reorientation and length change in an electric field would lead to a compressive stress. Verifying this hypothesis is somehow challenging and one has to study the defect density and more particularly the content of oxygen vacancies on the final response.

1.3 Objective of This Thesis

It can be seen that Nanoionics-based devices have great potential in different applications which are in high demand in today's technology. Many promising results have been obtained and many big steps have been taken towards implementing such devices in real applications, however, there are still some remaining challenges that are needed to be addressed more carefully.

- Micro Solid Oxide Fuel cells (µSOFC): mechanical stability and reliable performance are still insufficient.
- Resistive switching memories: the potential of classically known fast ion conductors, i.e. YSZ and CGO is completely unexplored even though one can expect superior characteristics with respect to more frequently studied metal oxides.
- Electromechanical response of CGO thin films: while the observed behavior is very astonishing there is no clear understanding about the acting mechanism.

This thesis is divided into three main parts, corresponding to the three above topical areas. Firstly, we have studied the mechanical stability of free-standing SOFC membranes. A new concept has been developed and implemented (Part I). Secondly, we have investigated the potential of CGO and YSZ thin films for memory applications. The preliminary results are very promising and with small improvement, one can classify them between best switching layers (Part II). Finally, we have extensively studied the origin of the giant electrostriction in CGO thin films. We identified the acting mechanism and basic requirements for achieving the giant electromechanical response. It also turned

out that CGO thin films with the GES effect exhibit as well a property called "Colossal dielectric constant". As a side result, we also discovered that such films are showing interesting non-linear I-V characteristics for varistor type applications (Part III).

Part I

Portable Solid Oxide Fuel Cell (SOFC)

2 Micro Solid Oxide Fuel Cells

2.1 Introduction

In almost last two decades, the demand, as well as opportunities for portable electronic devices, have grown for improving different aspects of human life including information and communication, autonomy, health support and etc. The market value of all portable devices is estimated as >300 billion dollars [20]. However, they suffer from a painful Achilles of inadequate batteries. It is somehow accepted that the upper limit performance of batteries for use in portable devices is being approached. As an example Fig. 2.1 shows the required energy for cell-phones over last 15 years and also the energy capacity of their power sources. It can be clearly seen that even though the power demand has increased about 20 times, the battery capacity is hardly doubled. This indeed leaves a huge gap in between. Thus, developing new types of portable power sources are becoming very crucial.

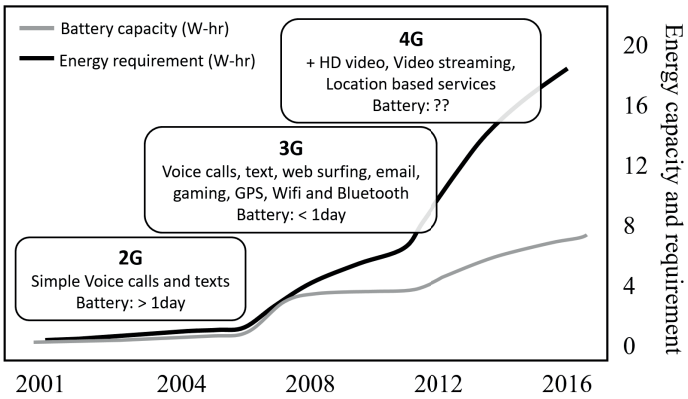


Figure 2.1 – Energy need and power source capacitance of cell phones versus time, adopted from [21]

Fuel cells, electrochemical devices that convert directly chemical energy to electricity, are often proposed as a possible solution for satisfying the energy requirement of portable devices. Fuel cells consist of an electrolyte, i.e. an ion conducting layer, that is sandwiched between two electrodes, thus forming Positive electrode-Electrolyte-Negative electrode (PEN) structures. Depending on the material in use fuel cells are classified into different types such as SOFC (Solid Oxide Fuel cell), MCFC (Molten Carbonate Fuel Cell), PAFC (Phosphoric acid fuel cell), PEMFC (Proton Exchange Fuel Cell) and AFC (Alkaline Fuel Cell) [22].

The performance of fuel cells is highly dependent on the using fuel. As it can be seen from Table 2.1 published by Evans et al [23], propane is the most favored liquid fuel. However, it is limited to high-temperature fuel cells such as SOFCs, except if a gas reformer for syngas production is applied [24].

Table 2.1 – The comparison of energy density of different liquid fuels [23].* LPG: Liquid Pressurized Gas

Fuel	Energy density by mass (MJ/kg)	Energy density by volume (MJ/L)
LPG* propane	49.60	25.3
Ethanol	30.0	24.0
Methanol	19.7	15.6
Liquid Hydrogen	6.1	10.1
Hydrogen in Metal Hybrid	1.2	3.2

The combination of fuel cells with fuel containers puts µSOFC with propane fuel on top of all other available power sources, including micro Proton Exchange Membrane Fuel Cells (µPEMFCs) and micro Direct Methanol Fuel Cells (µDMFCs), according to the energy density per volume and weight. One can estimate that a laptop can operate five times longer with µSOFC as compared to Li-ions batteries. µPEMFCs and µDMFCs can operate two to three times longer than Li-batteries. The disadvantages of fuel cells are complications due: to the need to ramp up the temperature, to include a gas handling system, to care about exhaust gases, and thermal insulation. A hybrid system might be the ideal, i.e. a battery that is backed-up with a fuel cell.

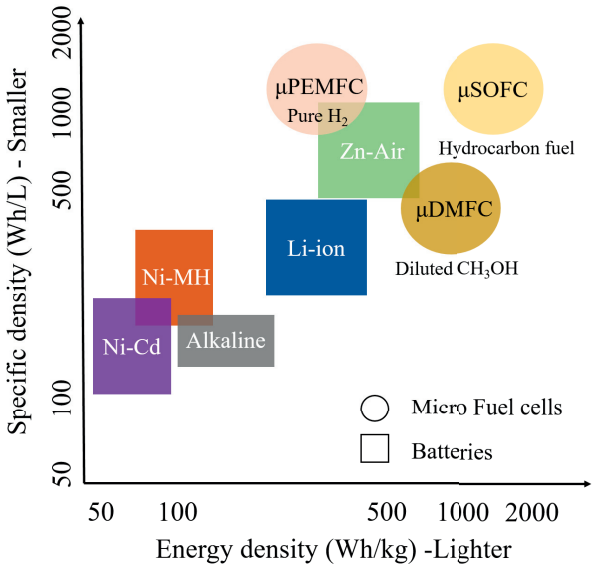


Figure 2.2 – Specific energy and energy density of available portable energy sources and estimated values for micro scale fuel cells (adopted from [25]).

2.2 Solid Oxide Fuel Cells Principle

All types of fuel cells split combustion reactions into two electrochemical half reactions. The reaction causes a voltage difference between the two sides of the electrolyte, based on the electrochemical potentials involved in the reactions. It is required that the electrolyte does not permit electronic conduction and that only ionic conduction driven by concentration gradient is carrying the charges across the electrolyte. In this way, the fuel cell potential difference can be exploited like with a battery, i.e. an electronic current can be fed into an external electrical element (consumer). In order to maintain the voltage, fuel and oxidant gas must be supplied, and are balanced with the electrons passing through the external consumer. The schematic of SOFC working principle is presented in Fig. 2.3. The fuel (hydrogen gas) is continuously fed to the anode side and the oxidant (oxygen from the air) is supplied to the cathode side. There, the electrons dissociate and reduce absorbed oxygen and consequently forms oxygen ions ($O_2 + 4e \longleftrightarrow 2O^{2-}$). The ions diffuse through the electrolyte and oxidize the fuel at the anode side, where the oxygen vacancies are formed in consequence. The product of the reaction is thus electrons plus water steam ($H_2 + O^{2-} \longleftrightarrow H_2O + 2e$).

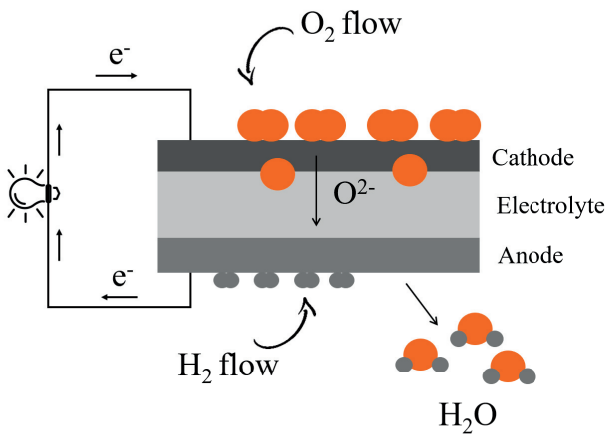


Figure 2.3 – Schematic of SOFC working principle

The voltage difference can be written according to the Nernst equation, which for the water reaction[26]:

$$E_{OCV} = E_0 - \frac{RT}{nF} ln \frac{p_{H_2O}}{p_{H_2} p_{O_2}^{1/2}} \tag{2.1}$$

where (R) is the universal gas constant, (T) is temperature, (n) is the number of charges transferred, (F) is Faraday constant, 96485 C, (p) is the partial pressure and (E_0) is the standard potential (temperature dependent) that can be derived from thermodynamics according to Eq. 2.2. Using the standard Gibbs free energy of water in the gas state, -228.61 (kJ/mol), one calculates [27]:

$$E_0 = \frac{\Delta G}{-nF} = 1.184V \tag{2.2}$$

As soon as a current drawn from the cell the SOFC output voltage starts to drop due to different losses -known as polarization- at the electrodes, and inside the electrolyte. There are three major losses, a) Activation polarization, b) Ohmic polarization and c) Concentration polarization.

The **activation polarization** is the first loss encountered when a current is driven from the fuel cell. It is related to the energy barrier of electrochemical reactions taking place at the electrodes surfaces. The activation loss occurs at low driving voltages and it highly depends on the reactant/catalyst interface, the number of triple phase boundaries (TPB),

and the operation temperature. TPBs are reaction sites where the reactants, the electrode, and the electrolyte meet.

The **ohmic polarization** is due to ion transfer in the bulk of electrolyte and simply follows the ohmic law. In general, it may also include the electrical resistance in the electrodes, current collectors, and contact resistance. The ionic resistance is much larger than the other components and makes the major influence on the overall response. Reducing the electrolyte thickness has been introduced as best solution so far, in order to be able to obtain reasonable ion conductance at low temperatures, $\approx 500°C$.

Finally, at high current densities, the **concentration polarization** is the strongest loss which is due to mass balance at reaction points. The gas diffusion through electrodes is the main feature that can reduce the concentration polarization. Thus, the electrode microstructure and fuel flow rates are the controlling factors. Fig. 2.4, shows how different polarizations can affect the operation efficiency.

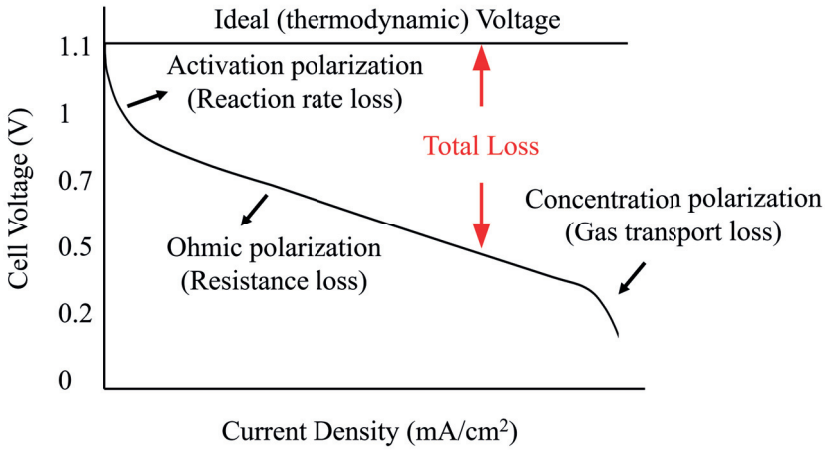


Figure 2.4 – Three main polarization mechanisms of fuel cells which lowers the operation efficiency from ideal case

2.3 PEN Elements

As has been discussed so far, the architecture of a SOFC membrane consists of two electrodes (anode and cathode) and oxygen ion conducting electrolyte forming a PEN structure. The two electrochemical half reactions are practically taking place at the interface of electrode and electrolyte that are having access to the gas, TPB. Therefore, the electrodes have to be porous for enabling gas access to the electrolyte surface, while keeping its electronic conductivity. On the other hand, the electrolyte has to be dense

and gas tight to prevent the gas leak and a voltage drop. Below we have discussed different materials that have been studied in thin films scale for µSOFC membranes.

Electrolyte

Most of the good ion conductors exhibit fluorite related structures as it is an open structure and has exceptional tolerance for a high concentration of atomic disorder introduced by doing and non-stoichiometry due to oxidation or reduction [28]. By doing with di- or trivalent cations on the cation sub-lattice results in the formation of oxygen vacancies to preserve the electrical neutrality. The created oxygen vacancies give rise to the ion conductivity. Doped CeO_2 and doped ZrO_2 are the most well-known examples of oxide with fluorite structure with high ion conductivity that are also investigated at thin film scale [29]. While Gd doped ceria (CGO) is considered as a very good ion conductor at low temperatures [30], the electronic leakage due to the reduction of Ce ions makes CGO very difficult to be used in form of thin films [25]. Thus yttrium stabilized zirconia (YSZ) looks as best solid oxide conductor that can exhibit exclusively ionic conduction at very small thicknesses. It is worth to mention that scandium doped zirconia also exhibit superior ion conductivity characteristics but due to the high costs yttrium is more favorable [31]. Different deposition techniques e.g. Atomic Layer Deposition (ALD), Pulsed Laser Deposition (PLD), and sputtering have been used so far to fabricate YSZ thin films from 50 nm to 10 μm.

Prinz group in Stanford used ALD to fabricate YSZ thin-film electrolytes with a thickness of 60 nm onto a corrugated silicon nitride structure obtained with nano-structuration, combined with platinum (Pt) thin film electrodes. The maximum power output achieved for a 43×43 μm^2 was 1.3 W/cm^2 at 450°C, using hydrogen fuel [32]. A free-standing YSZ electrolyte membrane prepared with PLD technique has been also investigated. It had been found that a nanocrystalline microstructured YSZ thin-film electrolyte with a thickness of 200 nm can show an area-specific resistance (ASR) of 0.15 $\Omega.cm^2$ at temperatures as low as 450°C [33] which is very interesting for lowering the operation temperature. However, PLD is prone to pinhole formation and it is mostly available for small size depositions. The other deposition technique is sputtering that is expected to yield films of good quality at a sufficiently high deposition temperature. Although, there seem to be more problems with stress issues. Ramanathan group in MIT used sputtering to fabricate 160×160 μm^2 membranes on free-standing silicon nitride and reported 1 W/cm^2 [34]. As was expected, a mechanical post-buckling problem was observed due to thermal strain.

Cathode

At the cathode, oxygen molecules dissociate and atomic oxygen takes up two electrons and eliminates oxygen vacancies. Hence, the electrode should have high electro-catalytic activity towards oxygen reduction and high chemical stability in an oxidizing environment. One type of cathode electrodes is mixed ionic-electronic conducting perovskites (ABO_3). Both A (rare earth element, e.g. Lanthanum) and B (a transition metal) sites can be substituted to tailor material properties. The composition of lanthanum partially substituted with strontium ($La_xSr_{1-x}BO_{3\pm\delta}$) is a well-known option. Sr^{+2} cation site on the La^{+3} sites because of similar ionic radii. The substitution of La^{+3} by Sr^{+2} creates a fully ionized acceptor level (Sr'_{La}) whose charge is compensated by holes ($\dot{B}_B$) in the valance band as well as oxygen vacancies ($V_{\ddot{O}}$) [35]. Recently, Ramanthan's group demonstrated good µSOFC properties with $(La_{0.6}Sr_{0.4})(Co_{0.8}Fe_{0.2})O_3$ [36, 37]. $(Ba_{0.5}Sr_{0.5})(Co_{0.8}Fe_{0.2})O_3$ (BSCF) thin film cathodes were also developed for µSOFC applications [38]. RF-sputtered BSCF thin films with a thickness in the sub-100 nm range were grown on the YSZ electrolyte and Pt anode. Pure electronic conductor metals are the other type. And finally, one can also consider a composite structure of metal and ion conducting material, e.g. Pt-YSZ [39, 40].

The performance of cathodes is based on the ASR, which besides material properties depends on microstructure and processing. As the ionic conductivity of mixed conducting perovskites decreases strongly with temperature, metal cathodes become more interesting at modest temperatures. Moreover, they can maintain their catalytic behaviour at low temperatures. Therefore, porous metals are more suitable for µSOFC operating at intermediate temperature <500°C.

Anode

At the anode, H_2 and CO molecules react with oxygen ions that diffuse through the electrolyte, and the excess electrons are given to electron collector. The electrode has to be conductive, porous, and chemically stable. Moreover, the anode has to provide catalytic activity since the oxidation of hydrogen and hydrocarbons begins with a chemisorption and dissociation at the surface of the anode [41]. Platinum thin films are commonly used because of their good catalytic activity [42]. Nevertheless, above 400°C in hydrogen (reducing environment) after long period of operation the porosity of Pt decreases significantly, as dewetting and recrystallization increases with Pt surface mobility. Metal ceramic composites can be used as an alternative. It has been shown that the performance of Ni- based anodes can be substantially increased by impregnating nano-sized YSZ or CGO [43, 44]. Usually, they can be fabricated for instance from NiO-YSZ composites and then reduced to form porous Ni-YSZ cermet. Different deposition

techniques have been used to fabricate such Ni-based anodes, like RF-sputtering [45], PLD and spray pyrolysis [46].

In addition, Jung et al [47] have shown superior performance of columnar porous samarium doped ceria for hydrogen electro-oxidation. They propose columnar doped ceria as an excellent ceramic anode in an intermediate temperature regime with no need of an extra metallic component. Recently, porous vanadium oxide has been studied by Van Overmeere and co-authors [48]. They have shown that the endurance of the cells increases while the performance was similar to porous Pt. More interestingly the material can be reversibly reduced and oxidized or store hydrogen in fuel cell operation conditions. This allows the delivery of stored energy when the fuel supply is depleted.

2.4 Thermal-Mechanical Stability

The reliability and performance of µSOFC are highly size dependent, meaning that one has to deal with two conflicting features at the same time; enlarging the active while keeping it as thin as possible. The main issue is the thermal loading which can cause several failure modes including, buckling, fracture, and delamination [49]. Moreover, the intrinsic stress has to be added as well.

Depositing thin films at high temperature will induce thermal stress depending on the thin film structure. Thin films are part of a composite structure where the film is free to move out of the plane but it is clamped in the plane to the substrate. Thus, under temperature change, the film (ϵ_s) and substrate strains (ϵ_f), can be written as Eq. 2.3 and Eq. 2.4 [50].

$$\epsilon_s = \alpha_s \Delta T + \frac{F_f(1-\nu_s)}{Y_s t_s W} \tag{2.3}$$

$$\epsilon_f = \alpha_f \Delta T - \frac{F_f(1-\nu_f)}{Y_f t_f W} \tag{2.4}$$

where α_s and α_f are the thermal expansion coefficient of substrate and film, respectively. F_f is the mismatch force and W is the substrate width. Strain compatibility requires that

$\epsilon_s = \epsilon_f$ thus the F_f can be written as Eq. 2.5.

$$F_f = \frac{W(\alpha_s - \alpha_f)\Delta T}{((1-\nu_f)/Y_f t_f) + ((1-\nu_s)/Y_s t_s)} \tag{2.5}$$

The in-plane thermal stress (σ_f) can be derived by dividing F_f by the surface ($t_f W$), which with considering $(Y_s t_s/(1-\nu_s)) \gg (Y_f t_f/(1-\nu_f))$ can be presented as Eq. 2.6.

$$\sigma_f = \frac{(\alpha_s - \alpha_f)\Delta T Y_f}{(1-\nu_f)} \tag{2.6}$$

Let us consider YSZ deposited at high temperature (350°C) on a silicon wafer. The thermal expansion difference between Si and YSZ is about 7 ppm/K, the Poisson ratio is 0.28 and the YSZ elastic modulus is 192 GPa [25], thus the in-plane thermal stress can be estimated as -560 MPa. The negative value means a compressive stress. This indicates that after membrane liberation the membrane would have mechanical buckling, see Fig. 2.5 [51]. It can be calculated from Eq. 2.6, the thermal stress, and mechanical buckling do not depend on any geometrical parameter like the thickness of the film and size of the opening.

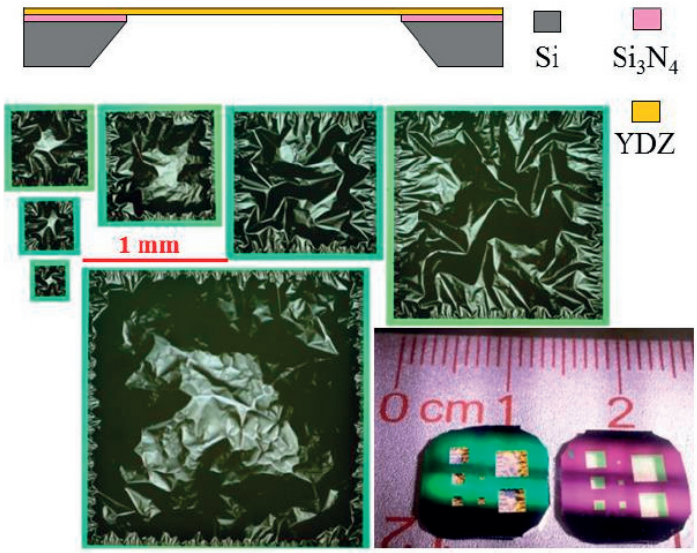


Figure 2.5 – Optical images of free standing membrane published by Kerman in his PhD thesis at Harvard university [51].

One approach for reducing the membrane stress is to make corrugated structures (Fig. 2.6), often used in micromachined sensors, that can reduce the structure stress by allowing the membrane to change dimensions to some degree [49]. The essential feature in corrugated membranes is profile parameter (q) which is the ratio of the rigidity of the corrugation.

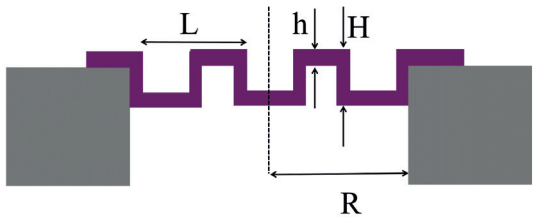


Figure 2.6 – The cross-section of corrugated membrane.

Depending on the level of corrugation which is defined as the depth of corrugation (H) over the wavelength (L) the (q) factor is changing. For $H/L < 0.4$ the (q) can be considered as Eq. 2.7 [52].

$$q^2 = 1 + 1.5\frac{H^2}{h^2} \tag{2.7}$$

where (h) is the film thickness. According to the profile parameter, Di Giovanni had derived the thermal stress as Eq. 2.8 which is dependent on the radial position from the membrane center (r) [52].

$$\sigma_{corr} = \frac{(\alpha_s - \alpha_f)\Delta T Y_f}{q}(\frac{r}{R})^{q-1} \tag{2.8}$$

If we consider 500 nm YSZ film deposited at 350°C for an opening of 500 µm with corrugation depth of 5 µm the stress would be neglectable at the center of the membrane and it reached to -40 MPa at the border. Unlike the flat membrane, the in-plane thermal stress is highly dependent on the geometrical parameters, and it is not uniform over the whole area. The edges are facing higher stress but still much less than the flat membranes.

Moreover, the high operation temperature of µSOFC can also lead to thermal-mechanical failure as the clamped membrane tends to expand due to temperature change. The

membrane expansion leads to compressive stress and consequently post-buckling in flat membranes and buckling in corrugated structures. The critical stress has been given by Young [53] and Harings [54] for flat (Eq. 2.9) and corrugated (Eq. 2.10) membranes.

$$\sigma_{fc} = -1.22 \frac{E}{(1-\nu^2)} \left(\frac{h}{R}\right)^2 \tag{2.9}$$

$$\sigma_{cc} = -\frac{E(q+1)^2}{48} \beta^2 \left(\frac{h}{R}\right)^2 \tag{2.10}$$

where (β) is the buckling number which is dependent on (q). For q>10, β changes from 4.8 to 5.14 [52]. If one combines the thermal stresses with critical stresses, the temperature difference at which the films buckle are Eq. 2.11 and Eq. 2.12 for flat and corrugated films, respectively [49].

$$\Delta T_{flat} = -\frac{1.22}{(1+\upsilon)(\alpha_s - \alpha_f)} \left(\frac{h}{R}\right)^2 \tag{2.11}$$

$$\Delta T_{corr.} = -\frac{q(q+1)^2}{48(\alpha_s - \alpha_f)} \beta^2 \left(\frac{h}{R}\right)^2 \tag{2.12}$$

This means for 500 nm thick membrane which supposed to work at 500°C the maximum opening for flat membrane has to be less than 20 µm for not facing any post-buckling. However, in case of corrugated structure, (5 µm deep corrugation) the minimum dimension reaches about 500 µm, 25 times more than the flat membrane.

Very promising results have been reported by Prinz group using corrugated substrates, even though they have proposed corrugated structures for increasing the surface density in given volume. They have used silicon deep etching for making 20 μm holes through silicon substrate [55], Fig. 2.7 (a). With this method, the surface roughness is relatively high and it can induce pinholes in the membrane. However, they have used ALD for thin film deposition, hence, they have faced any issue due to the good film coverage. The corrugation sharp edges are also an issue. They are so-called stress concentration points. Moreover, with the hole structure, one cannot solve the issue of liberation border where the membrane remains in contact with a silicon substrate. Furthermore, when

the corrugation is made with 20 μm deep structures, one needs to use KOH wet etching for membrane liberation which is very violent for thin films and the final opening is square-shaped which is also not favorable [56]. Moreover, KOH etch has very poor surface utilization, especially for small openings. Finally, the straight sidewalls of the holes are definitely not practical for conventional thin film deposition techniques.

They have also studied the corrugated substrates by the nano-sphere lithography method, Fig. 2.7 (b-e), where they have somehow solved the straight sidewalls. However, the peak-shaped profile is still not ideal. Moreover, the scalability and ease of fabrication are still questionable. Nevertheless, they obtained the highest reported power density, 1.34 W/cm^2 at 500°C, so far [14].

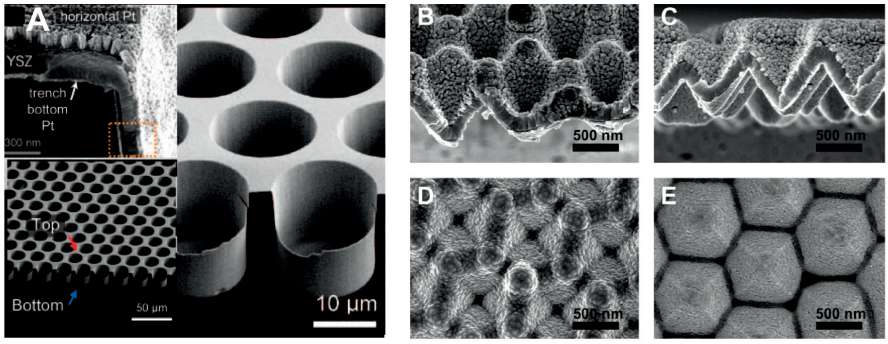


Figure 2.7 – A) Corrugated structure using 20 μm holes. SEM image shows the good coverage of the angles which is achievable by atomic layer deposition [55] B) corrugated structure using nano-sphere lithography with porous electrode C) side view of nano structures D,E) top and bottom view (cathode and anode side) [14]

Another concept to increase the mechanical stability is to use a metallic grid on top of the membrane i.e. a nickel grid on the anode side. This was initially proposed by our group in 2008. Using a mechanical support gives the possibility of increasing the active area to some square millimeters. The idea was to partitioning the membrane area for reducing the mechanical buckling and increasing the critical stress (Eq. 2.9) [57]. The grid also has the function of anode current collector [58]. The cell diameter varied between 0.5 to 5 mm, and very good mechanical stability have been obtained at 600°C, Fig. 2.8. Unfortunately, a high cathode contact resistance reduced the current very much, therefore, the achieved power density was only 19 μW/cm^2 [25].

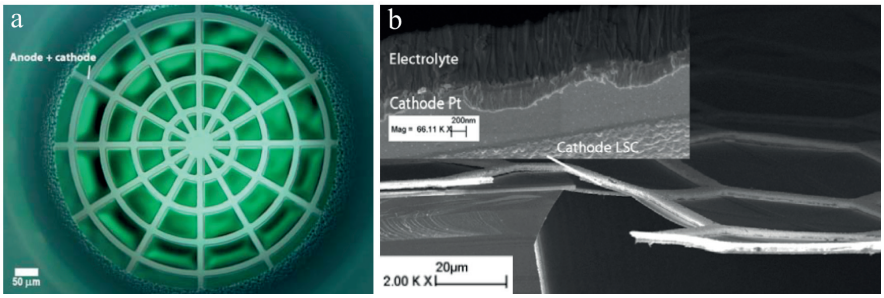


Figure 2.8 – a) Optical image of supported cell with spider web b) SEM cross section of nickel supported electrolyte (Pt current collector and LSC cathode) [25]

Recently, Tsuchiya et al achieved a good success using grid strategy at MIT [37]. They have managed to fabricate µSOFC in the range of 4 cm^2. However, their power density was not as high as expected, 150 mW/cm^2 (active area of 13 mm^2). The highest output power that they obtained was about 20 mW, Fig. 2.9. The idea of using a metallic grid seems very practical, however, the problem of mechanical buckling is still unsolved (Fig. 2.9 (b-d)) and a weak liberation border is remaining.

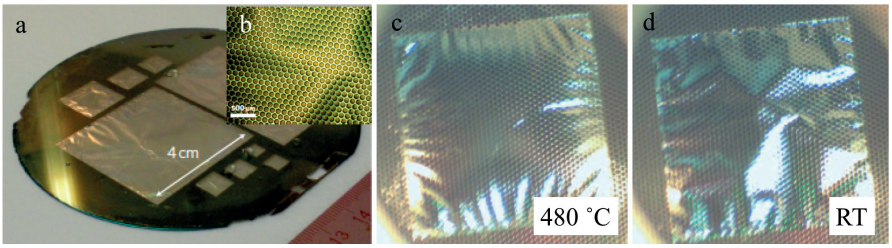


Figure 2.9 – a) Various sizes active μSOFCs fabricated on 4 inch wafer, b) optical micrograph of membranes with metallic grid, Optical micrograph of cathode side at c) 480°C, d) close to room temperature [37]

Another interesting result was published by Chang and co-workers [59] using supported µSOFC. They reached 44 mW output at 319°C. This is the lowest operation temperature that has been published and the power output is meeting the minimum requirements of device implementation. The weak point is the low power density, 6.7 mW/cm^2, meaning that for delivering such power one has to have about 2.56 cm wide cells. They grew PEN structures over porous substrates. In their PEN structure, they used YSZ with an interlayer of gadolinium doped ceria (CGO) as the electrolyte, Fig.2.10.

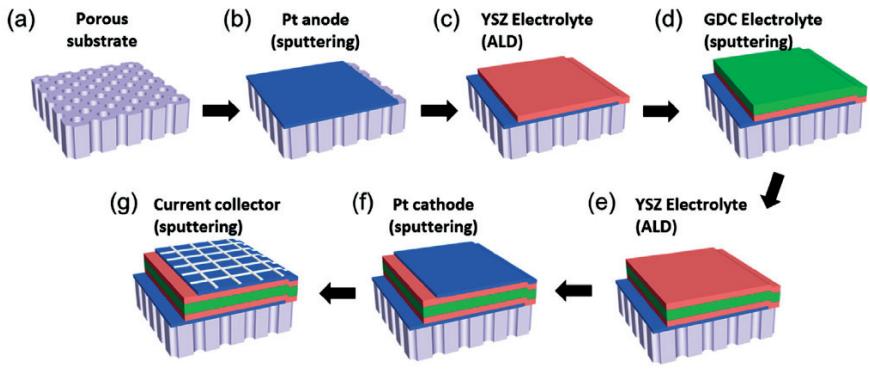


Figure 2.10 – Diagrams for fabrication of the thin-film SOFC composed of (a) AAO (anodic aluminum oxide) substrate, (b) Pt anode, (c)-(e) multilayer electrolyte (Y-G-Y), (f) Pt cathode, and (g) current collector [59]

2.5 State of The Art

Table 2.2 gives an overview of studies that have been published so far. The reported energy densities are very promising especially the 1.3 W/cm^2 that is published by Prinz group [32]. However, due to the small active area, the output power cannot exceed 20 μW, which is not yet practically interesting. Unfortunately, the high power density is not achievable at large scales. As mentioned before, the group of Ramanathan in MIT has enlarged the active area in the range of 5 cm but the energy density dropped to 150 mW/cm^2, or even lower, thus the power output was only 20 mW [37]. This indeed meets the minimum requirement of application implementation but one should do significantly better. Perhaps the ideal case would be reaching 1 W/cm^2 for 500 µm wide membranes and with an array of these cells obtain 1-2 Watts power output at chip size of 2×2 cm^2.

Table 2.2 – Overview of different μSOFCs

Group	Year	Ref.	Structure P-E-N	Thickness (μm)	Operating T (°)	Power density (mW/cm^2)	OCV (V)	Opening
Livemore National lab.	2002	[13]	Ag-YSZ-Ni	0.5-1.2-0.8	600	145	0.35	
Standford	2006	[60]	Pt-YSZ-Pt	0.050-0.185-	350	0.04	0.83	
	2006	[61]	Pt-YSZ-Ni	20-0.200-	400	7	0.6	
	2007	[62]	Pt-YSZ-Pt	0.080-0.050-0.080	400	400	1.10	
	2007	[63]	Pt-YSZ-Pt	0.080-0.060-0.080	350	270	1.05	
					300	66	1.10	
	2008	[55]	Pt-YSZ-Pt	0.080-0.070-0.080	450	861	1.10	
					400	677	1.05	
	2012	[64]	Pt-YSZ-YDC-Pt	0.080-0.070-0.020-0.080	500	1040	1.15	
	2011	[14]	Pt-YSZ-Pt	0.060-0.080-0.060	500	1340	1.10	
					450	820	1.14	
	2013	[32]	Pt-YSZ-YDC-Pt	0.080-0.060-0.020-0.080	450	1300	1.08	
	2012	[65]	Pt-YSZ-Pt	0.120-0.070-0.120	450	198	1.10	
Harvard	2009	[36]	LSCF-YSZ-Pt	0.040-0.075-0.015	500	60	1.03	
	2011	[37]	LSCF-YSZ-Pt	0.047-0.054-	510	150	1.00	
	2011	[34]	Pt-YSZ-Pt	0.1-0.07-0.10	525	1037	1.00	
	2012	[66]	Pt-YSZ/CGO-Pt	0.085-0.085-0.085	520	1175	1.01	
	2012	[48]	Pt-YSZ-Pt/VO	0.028-0.090-0.028	360	6.6	1.00	
ETH	2004	[67]	LSCF-YSZ/CYO-NiO/YSZ	50-0.600-300	720	750	1.01	
	2008	[68, 69]	LSCF-YSZ-Pt	0.05-0.550-0.200	550	150	1.06	
	2012	[70]	Pt-YSZ-Pt	-0.150-0.200-	550	209	0.57	
	2013	[70]	LSCF-CGO-YSZ-Pt	-0.150-0.200-	650	850	1.15	
	2015	[71]	LSC-3YSZ-Pt	200-300-80	425	262	1.1	
EPFL	2008	[25]	Pt-YSZ-Pt	0.1-0.5-0.1	500	0.02	0.85	
	2012	[40]	Pt/YSZ-CGO/YSZ-Pt	0.05-0.550-0.200	450	7	0.68	
SNU (S.Korea)	2015	[72]	Pt-YSZ-Pt	150-70-320	500	170	1.17	
	2016	[59]	Pt-YSZ-CGO-YSZ-Pt	350-100-300-100-?	319	6	3	
Hanyang Uni.	2016	[73]	Pt-YSZ-Pt	100-230-100	450	158	1.07	
NTU (Singapore)	2016	[74]	Pt-YSZ-Pt	100-80-100	400	317	1.04	
	2017	[75]	BSCF-YSZ-Pt	248-200-100(?)	450	55	0.9	
IREC(Barcelona)	2014	[76]	LSC-YSZ-CGO	200-300-250	750	100	1.10	

2.6 Complete µSOFC Device

A complete µSOFC device is rather a complex structure. It consists of an electrochemical active fuel cell membrane, a gas processing unit, and a thermal system. The fuel tank can be considered as external unit like the µSOFC devices that have been proposed by Lilliputian Systems (Nectar) in the USA [77, 78] and OneBAT project in Switzerland [23]. In the gas unit, if one uses the butane or propane as fuel, there will be a gas reformer to crack the hydrocarbon gas into hydrogen and carbon monoxide. Afterwards, a post-combustor must be added to burn the non-used fuel. All the gas units are needed to heat up in order to work properly. The gas reformer temperature is expected to be around 500°C [79]. Therefore, a thermal insulating system should be added to the device. Ideally, the fuel cell should also work at the same temperature range, which rises the

need of having SOFC in micro-scale. Fig. 2.11 presents a schematic view of complete µSOFC that was presented in the scope of ONEBAT project [68].

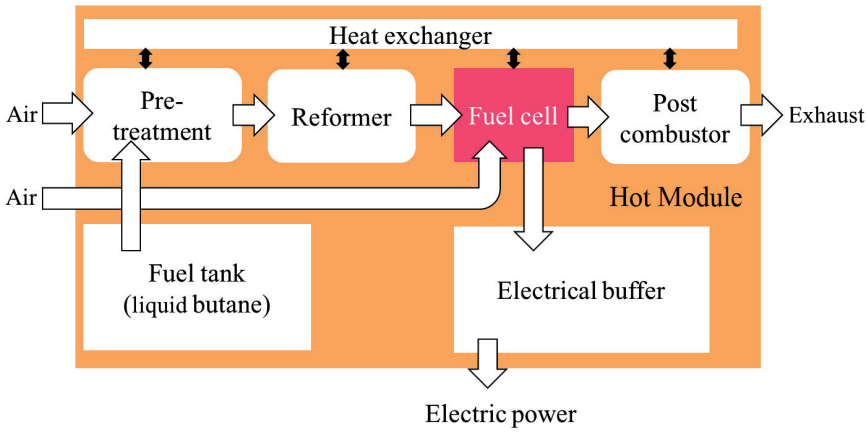


Figure 2.11 – Layout of ONEBAT µSOFC systems, adopted from [68]

Recently, Pla et al [80] have studied the feasibility of 1-W µSOFC power generator with ethanol fuel using finite element modeling. They have proposed a vertical stack of a vaporizer, double reformer, µSOFC and post combustor. The insulating configuration, as well as the start-up time, has been studied. The starting time was estimated fairly below 1 min using electrical-chemical start-up with 500 J energy. The study confirms the potential of using µSOFC based systems to be used as the power generator in portable devices. The operation conditions were chosen based on the experimental results that were obtained in the same group. Thus, the operation temperature was 750°C and the power density of µSOFC has been considered as 100 mW/cm^2 for the cell size of 1.8×1.8 to 3.5×3.5 mm^2. The high operation temperature was justified based on the efficient reforming system above 600°C [76].

3 Thin films study: Deposition and Characterization

3.1 Thin Films Deposition

3.1.1 Sputtering Technique

During sputtering, a solid material target is bombarded by energetic ions emitted by a gas plasma. To create a plasma a high electrical field needs to be applied between the two electrodes serving as anode and cathode. The substrate and the chamber are close to anode potential and the target is mounted on the cathode. Depending on the type of target material a DC or RF (13.56 MHz) power is applied to the electrodes. In order to obtain higher deposition rate and sputtering efficiency, a magnetron source can be added. It possesses a magnetic field to confine the secondary electrons ejected from the target and increases their collision probability with neutral atoms that lead to higher plasma density. The key parameters in sputtering process are the applied power, substrate temperature, the target-substrate distance, the nature of the plasma (types of gases) and finally the applied bias on the substrate. Sputtering is a well-known method for the study of PEN elements. The sputter deposited films are normally dense with a columnar microstructure that is indeed favorable for electrolyte deposition [25].

Here, we have used single chamber Nordiko sputtering system with rotating substrate holder. Having a RF generator, as well as a DC generator, makes the tool capable of depositing a variety of materials. Running both generators at the same time and also the rotating substrate holder gives the possibility of depositing composite structures benefiting from co-sputtering. The Substrate-Target (S-T) distance can be also changed from 10 to 4 cm which can affect the ion bombardment and deposition rate. For the heating system, an indirect heating with lamps has been installed behind the substrate carrier that can reach a nominal temperature of 600°C. The pressure in the chamber can be monitored using a Baratron gauge and the control of pressure was done with the aperture of gate-valve. We have refurbished the tool because of the lack of technical

support and now one can make a completely manual operation which makes the tool more reliable. Fig. 3.1 present a schematic of the Nordiko configuration.

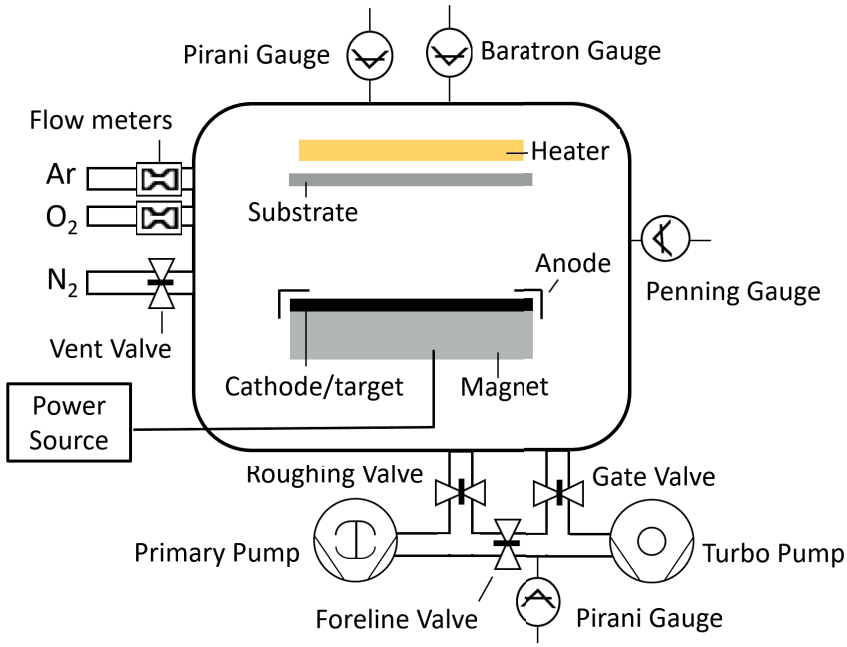


Figure 3.1 – Nordiko, RF magnetron sputtering system, configuration.

3.1.2 Atomic Layer Deposition (ALD)

Atomic Layer Deposition (ALD) as a subclass of chemical vapor deposition (CVD) can result in uniform and isotropic thin films with conformal coverage over three-dimensional substrates without pinholes [63]. The substrate surface is exposed to various vaporized precursors. During film deposition, different precursors are completely separated from each other and they have self-limiting chemistry, meaning that the reaction terminates as soon as all the reactive sites on the surface are utilized. Ideally, one reaction cycle produces one atomic layer. In case of doped oxide thin films, the composition can be modified by cycles ratio.

In this project, we have used BENEQ TFS200 ALD tool for preparing HfO_x thin film to study its potential as an electrolyte in PEN membranes. It is expected to show similar properties to ZrO_2 and a thin layer of hafnia prepared by ALD can protect the PEN membrane from gas and electronic leakage.

3.2 Characterization Methods

3.2.1 Microstructure Characterization

The thin films crystallographic orientation was investigated using X-ray diffraction in 2θ-θ mode using Bruker D8 systems with Cu-Kα radiation. The morphology and the microstructure of the films were studied by Scanning Electron Microscopy SEM (Zeiss-Merlin and LEO 1550) and Transmission electron microscopy TEM (FEI Tecnai Osiris).

3.2.2 Electrical Characterization:DC Conductivity

In order to measure DC conductivity across the electrolyte layers, the dielectric properties of test structures were measured using frequency response analyzer (Hewlett Packard 4282). The experimental setup was also composed of a hot plate capable of ramping up to 500 °C. The top and bottom electrode were accessed using homemade manipulators made out of Pt wires, Fig. 3.2. For test structures, YSZ thin films were deposited on a Pt/Ti (100/10 nm) bottom electrodes. The Pt/Ti electrodes were made using DC magnetron sputtering Spider 600 at 350°C using Ar pressure of 15 mTorr. Finally, porous Pt has been deposited through a shadow mask to from 600 µm-2 mm wide round-shaped devices. The details of sputtering conditions for each film deposition is presented in the corresponding section.

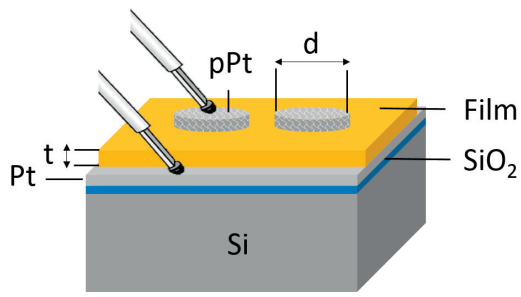


Figure 3.2 – The schematic view of test structures, Pt/electrolyte/pPt.

The film conductivity can be calculated using the admittance as:

$$Y = \frac{1}{R_{ll}} + j\omega C = j\omega C(1 - j\frac{1}{R_{ll}\omega C}) \tag{3.1}$$

Where "R_{ll}" is the parallel resistance of capacitance, "ω" is the angular frequency, "C"

is the capacitance of the film. The total R_{ll} can be derived using the imaginary part of capacitance, Eq. 3.2.

$$R_{ll} = j\frac{1}{\omega C \tan\delta} \tag{3.2}$$

The film conductivity σ is the inverse of R_{ll} multiplied by film thickness divided by active area, Eq. 3.3.

$$\sigma = \frac{4t}{R_{ll}\pi d^2} = \frac{4t\omega C \tan\delta}{\pi d^2} = \omega\epsilon_0\epsilon'' \tag{3.3}$$

where "t" is the film thickness, "d" is the active area diameter, "ϵ_0" is the vacuum permittivity, and "ϵ''" is the dielectric loss.

3.3 Electrolyte Layer

3.3.1 Yttrium Stabilized Zirconia (YSZ)

YSZ seems to be the most reliable material at thin film scale that can maintain a dense structure with exclusively ionic conduction. We have deposited YSZ thin films via Nordiko sputtering tool using 99.9% pure zirconia doped with 8% yttrium oxide from Kurt J. Lesker company. For test structures, the YSZ thin films were grown on passivated Si wafer with Pt/Ti (100/10 nm) coating prepared by Pfeiffer Spider 600 DC magnetron sputtering at 15 mTorr argon pressure with DC power of 1000 W at 350°C. Table 3.1 summarizes the processing conditions that have been used for YSZ deposition. The effect of sputtering pressures, substrate temperature as well as Ar flow have been studied.

Table 3.1 – YSZ deposition parameters using Nordiko sputtering system

Pressure (mTorr)	Ar Flow (sccm)	RF power (W)	Temperature (°C)	S-T distance (mm)
5	10	200	500	100
5	30	200	500	100
5	30	200	550	100
10	30	200	550	100
15	10	200	500	100
15	30	200	500	100
15	30	200	550	100

It turned out that YSZ texture is mostly dependent on the Ar flow as it changes from nicely (111) texture to almost polycrystalline with increasing Ar from 10 to 30 sccm (see Fig. 3.3 (a,c)). This can be explained based on the purity of plasma, which means that with increasing the Ar flow one has to increase the pumping speed to maintain the same pressure which can results in less number of impurities in the chamber. In addition to argon flow, by increasing the chamber pressure a mix structure with (111) and (002) orientation can be obtained. In this case, the film uniformity was also enhanced that can be attributed to the increased collisional scattering that results in more homogeneous flux and decreased ion bombardment. The enhanced film uniformity is, in practice, more favorable of microfabrication. Fig. 3.3 (a-f) shows the XRD pattern and surface morphology of YSZ films deposited at different conditions, representing (111)-textured (a,b), polycrystalline (c,d) and (111)-(002) mix oriented films (e,f). The sharp peak at about 34° (Fig. 3.3 (a,c)) is the forbidden peak of silicon which is appearing due to residual compressive stress. In order to reduce the residual stress, films were annealed at 600°C in an oxygen atmosphere for 1 min using Rapid Thermal Annealing (RTA).

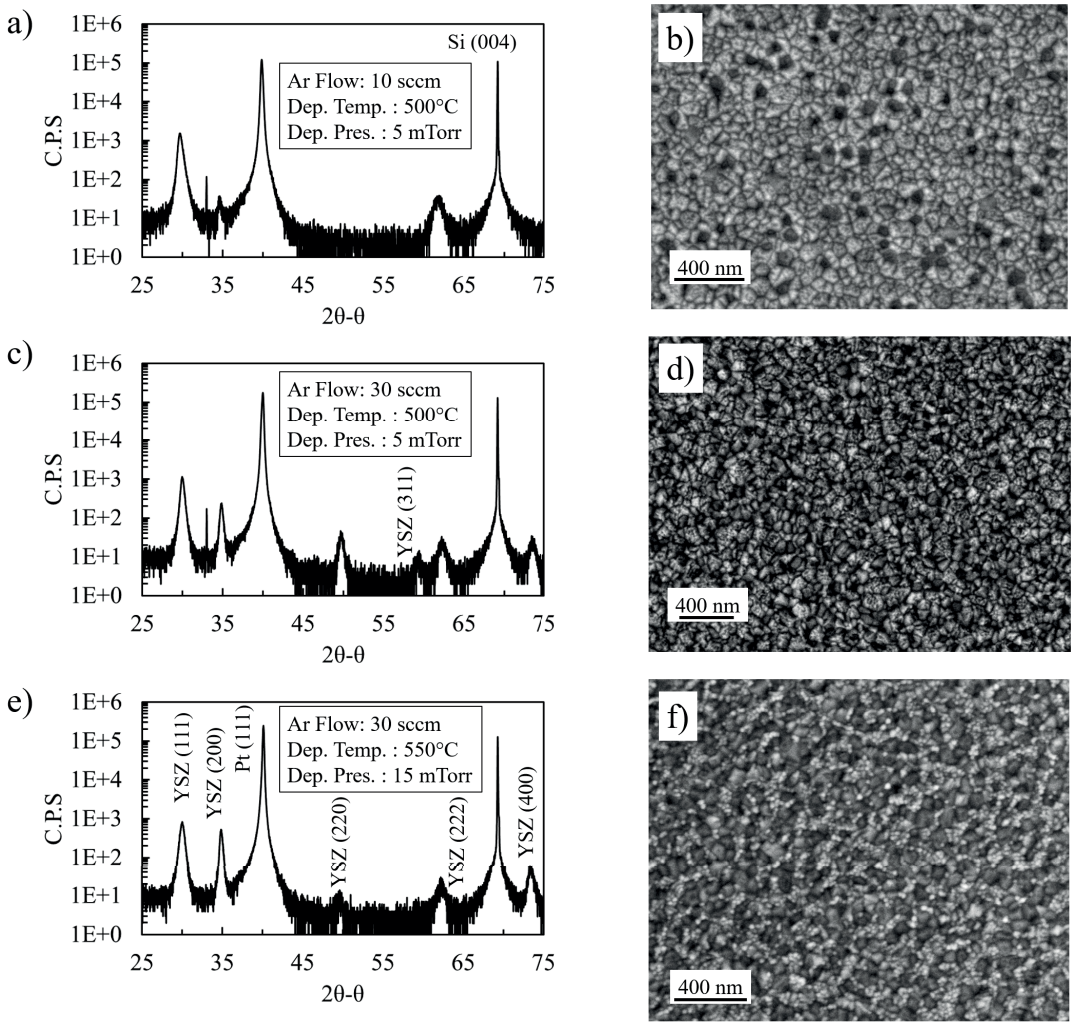


Figure 3.3 – a,c,e) XRD pattern of YSZ thin films deposited under different processing conditions indicated in each graph. b,d,f) SEM surface morphology of YSZ thin films for the corresponding XRD pattern on the left side.

Many studies are showing that the ionic transport in polycrystalline YSZ (bulk) is highly dependent on the texture and level of crystallization due to the contribution of grain boundaries [81, 82, 83]. The reduced ion conductivity of grain boundaries in highly pure YSZ has been related to electrical distortion as result of a large number of displaced atoms. This is explained based on the space charge layer concept stating that oxygen vacancies are enriched at grain boundaries and result in a positively charged region. This region is compensated by acceptor accumulation and oxygen vacancy depletion in two adjacent space-charge layers. Space charge layers are electrically resistive and therefore hinders the oxygen ion transport from grain to grain [82]. The size of the

space-charge region is estimated as 1 nm in micron sized grains that can reach 7 nm by reducing the grain to 17 nm. This means that by decreasing the grain size from micron to nanometers the oxygen vacancy depletion increases over large volume fraction of grains and consequently decreases the ion conductivity [81]. However, the story is expected to be different in case of thin films as the ratio of surface/volume is very large and also dealing with substrate and film interface is also complicated [84]. The reports on thin film structures are showing that the ion conductivity is lower and the activation energy is higher in comparison to the YSZ bulk. The activation energy in YSZ bulk is calculated as 0.9 eV whereas in thin films it is mostly reported as 1.1 eV [85, 84]. The reduced conductivity in thin films is also explained based on grain boundaries and space charge layers. As presented in Fig. 3.3 depending on the deposition parameter the texture of YSZ thin films can be varied that enables us to study the effect of microstructure on the ion conductivity of YSZ thin films. The DC conductivity was measured as presented in section 3.2.2. Fig. 3.4 demonstrates the ion conductivity of YSZ thin films with different microstructure as a function of temperature.

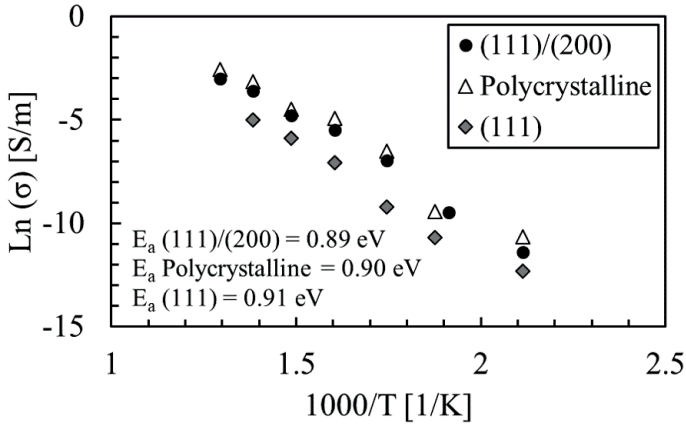


Figure 3.4 – Arrhenius plot of YSZ thin films with different microstructure

It can be seen that the activation energy is very well corresponding to the bulk values, the same as the conductivity [84]. The same measurement was also done for different film thickness and as was expected no dramatic change was observed. Hence, one can conclude that the space-charge layers are not contributing significantly to the ion conductivity. Moreover, in earlier work by Rey-Mermet it has been reported that grain boundaries in (111) textured films are very likely crossing the film [25]. This can lead to electronic leakage as well as H_2 permeability. Thus, we have used (111)/(200) recipe for making electrolyte layer in µSOFC devices as beside good film uniformity, it is expected to have low activation energy, high conductivity, and low leakage.

3.3.2 Hafnium Oxide (HfO_2)

An interesting material that can be considered to be used as an electrolyte in µSOFC devices is HfO_2 due to its similarities to ZrO_2 in physical and chemical properties [86, 87]. The main advantage of HfO_2 in our case is its availability on ALD systems which is very favorable for corrugated design. Thus, even with lower ion conductivity, a thin layer of hafnia can protect the membrane.

In order to study the potential of HfO_2 based thin films, we have prepared HfO_2 thin films on 100 nm (111)-textured sputtered platinum layer (the same bottom electrode as YSZ) using Beneq TFS200 ALD system at 200°C. Like YSZ, the films have been annealed in an oxygen atmosphere at 600°C using rapid thermal annealing (RTA). A porous Pt thin film has been sputter deposited through a shadow mask to form the top electrode and complete the test structure. Details of HfO_2 deposition is given in Table 3.2.

Table 3.2 – HfO_2 thin film deposition condition using ALD technique.*TEMAH (Tetrakis(ethylmethylamino)hafnium)

Precursor 1	*TEMAH
Temperature	80°C
Precursor 2	H_2O
Temperature	RT
Chamber temperature	200°C
Deposition rate (A/cy)	1.0

Fig. 3.5 shows the XRD pattern and surface morphology of 100 nm HfO_2 thin film. HfO_2 can have either Orthorhombic or Monoclinic crystal system at room temperature which in our case due to the appearing peak at 17 ° it is more likely Monoclinic, which was locally confirmed by the high resolution transition electron microscopy (HR-TEM). According to TEM studies, the lateral size of the grains was estimated about 100 nm which is also evident form the surface morphology Fig. 3.5 (b).

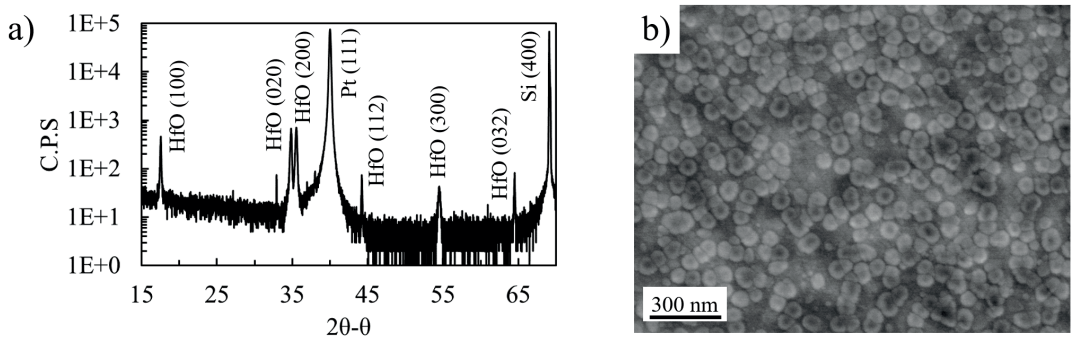


Figure 3.5 – a) XRD patten and b) surface morphology of 100 nm HfO_2 thin film deposited (ALD) on Pt bottom electrode after annealing

Fig. 3.6 shows the ion conductivity of HfO_2 in comparison to YSZ thin film. Up to 300 °C as was theoretically predicted by Wei et al [88], HfO_2 is showing the same response as YSZ thin films, however, it seems that the film is going into a phase transition after 300 °C and the conductivity drops dramatically. In studies regarding the ferroelectricity in hafnium oxide, it has been reported that in Y doped hafnia, the Curie temperature is about 450 °C meaning that the crystal structure changes from ferroelectric orthorhombic to paraelectric tetragonal [89]. The same case might take place in hafnia thin films, albeit at a lower temperature due to the absence of a phase stabilizer, i.e. yttrium.

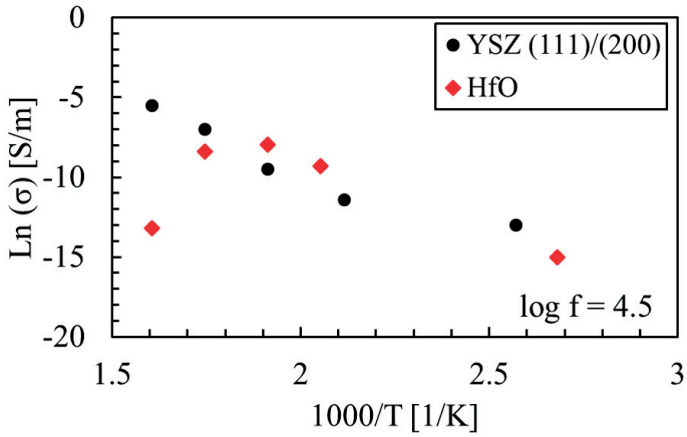


Figure 3.6 – Ion conductivity of HfO_2 thin films as function of temperature in comparison to YSZ thin films

In order to study the effect of Y dopant on the ion conductivity and microstructure of HfO_2 thin films, we have prepared doped structures using RF magnetron sputtering. The films were deposited using a 5 cm wide and 3 mm thick Hf disks with purity of 97% sitting on 10 cm wide yttrium target. The deposition conditions are presented in Table 3.3. Based on the SEM-EDAX analysis the film composition was estimated as $Y_{0.3}Hf_{0.7}O_{2-x}$.

Table 3.3 – Y doped hafnia thin film deposition parameters using Nordiko sputtering system

Pressure (mTorr)	Ar Flow (sccm)	O_2 Flow (sccm)	RF power (W)	Temperature (°C)	S-T distance (mm)
15	30	10	200	500	100

As usual, the films were annealed for 1 min at 600°C. The comparison of XRD analysis (Fig. 3.7 (a)) to the reported studies on yttria stabilized hafnia (YHfO) [90, 91] suggests that crystal structure is rather cubic, similar to YSZ thin films, with (111) texture. Studies show that more than 10% Y doping stabilizes the cubic structure in hafnium oxide [92]. According to surface morphology, Fig. 3.7 (b), the grain size seems to be reduced in compare to pure hafnia.

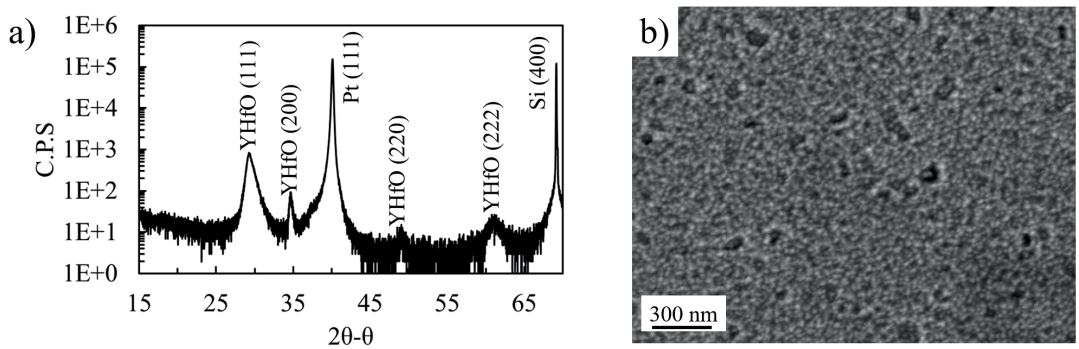


Figure 3.7 – a) X-ray diffraction of Y doped hafnia thin films prepared by magnetron sputtering, b) surface morphology of the YHfO film.

The ion conductivity was lower than pure hafnia till 300°C, however, a steep increase is observed at higher temperatures (Fig. 3.8). Like hafnia, some instabilities was recorded close to 400°C suggesting that a phase transition might also take place in YHfO as well. This indeed needs to be confirmed by high-temperature XRD characterization. Nevertheless, the enhanced ion conductivity at high temperature can be comparable to YSZ thin films, although with higher activation energy 1.21 eV. The activation energy is very well corresponding to the reported values for YSZ thin films in which the grain

boundaries are dominating the ion conductivity [82]. It has been reported that for the thin films with a grain size of < 10 nm due to high contribution of grain boundaries the activation energy rises from 0.95 to 1.21 eV. Based on surface morphology which shows a packed structure with small grain size, one can consider the same explanation for high activation energy in YHfO. According to the theoretical prediction by Wei et al 8% YHfO is expected to have the same ion conductivity as YSZ with activation energy close to 1.1 eV [88].

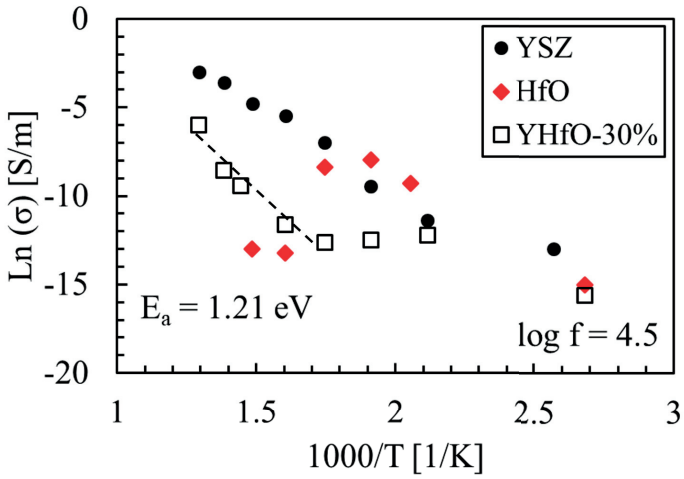


Figure 3.8 – Ion conductivity of 30% yttrium doped HfO_2 thin film as function of temperature in comparison to pure hafnia and YSZ thin films

Defect clustering can be also considered as the responsible for high activation energy and lower ion conductivity in YHfO in comparison to YSZ thin films. By increasing the number of charge carriers above certain concentration they start to interact with each other and reduce their ability to move [93]. Thus, it can be expected that the ion conductivity will be enhanced by lowering the dopant concentration.

3.4 Porous Electrodes: Platinum

Porous platinum as the most commonly used electrode in µSOFC devices has been used for both electrodes. The porous structure can be either obtained by high-pressure deposition or rotating substrate. A Pt foil with 99.9% purity was used for film preparation. In case of high-pressure deposition which was carried out at 75 mTorr Ar pressure, the DC power was set to 100 W, and the target-substrate distance was 100 mm. The deposition was performed without substrate heating. The working pressure and applied power were taken from previous reports by Prinz and Ramanathan groups [65, 34]. The deposition rate was estimated about 100 nm/min.

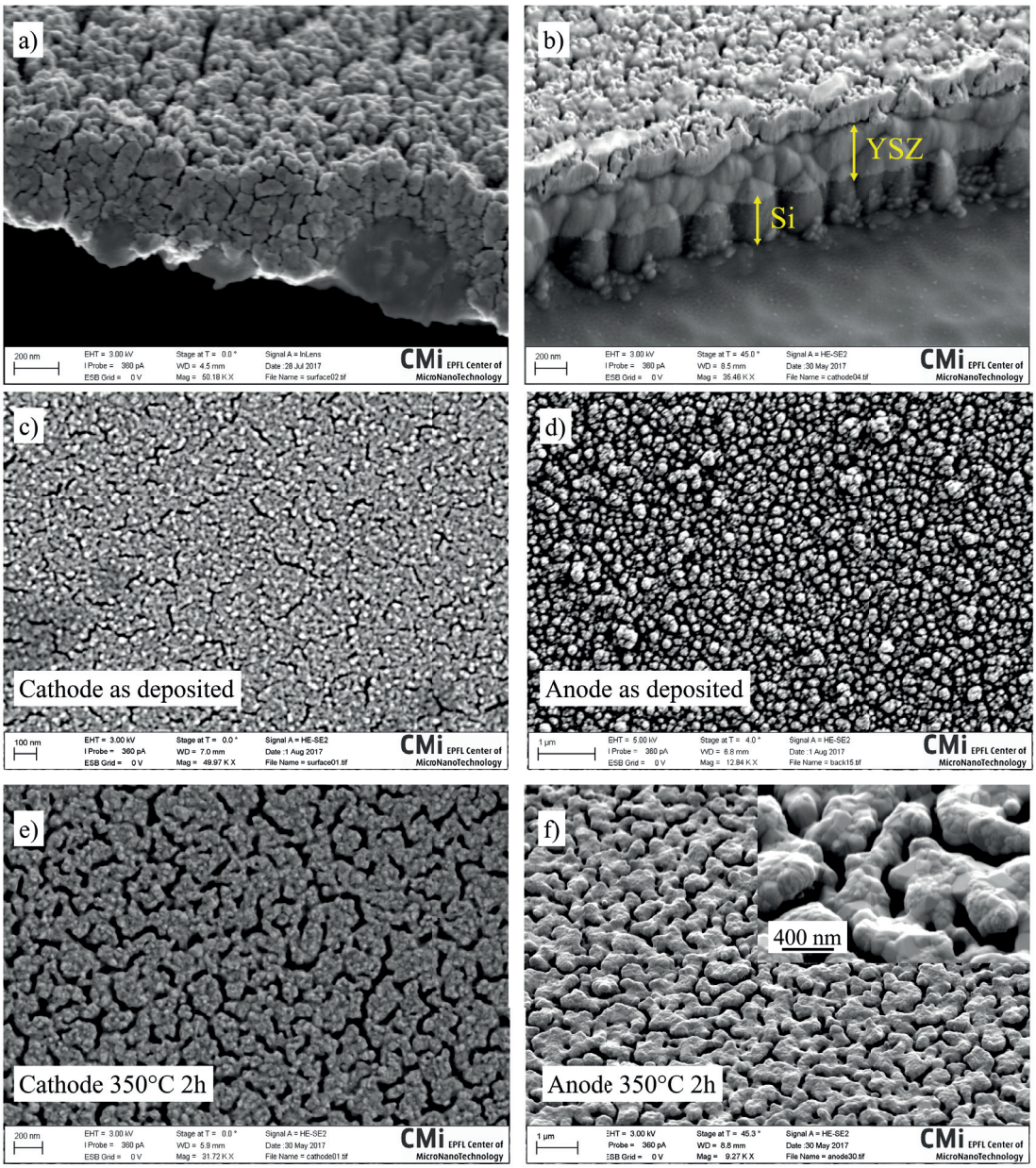


Figure 3.9 – SEM micrographs of porous platinum deposited at high pressure to be served as both electrodes in PEN membrane. a) on a liberate membrane b)cross-section of a patterned device, c) cathode as-deposited, d) anode as-deposited, e) cathode after operation, f) anode after operation.

Fig. 3.9 presents the SEM micrographs of pPt for both anode and cathode side before and after cell operation. The shape of porosity has been recorded on a broken part of a liberated membrane (Fig. 3.9 (a)) which somehow demonstrate the gas paths through the cathode towards the YSZ surface. The porosity shape might not be ideal, as a Pt

horizontal growth can facilitate the gas access. This can result in reduced number of TPB and lower power density. Nevertheless, the surface morphology is similar to earlier reports [34].

The columnar growth can be obtained by substrate rotation, see Fig. 3.10. However, it would be challenging to use rotating substrate for through-silicon-deposition that is needed for anode deposition after membrane liberation. The processing conditions are 50 W power, 5 mTorr pressure, and 10 sccm Ar flow. After stabilizing the plasma, the substrate holder starts to rotate with speed of 6 rpm. The deposition has been done without substrate heating and the rate was estimated as 6 nm/min. Ideally, one can use the rotating substrate technique for cathode deposition and high-pressure deposition for the anode side.

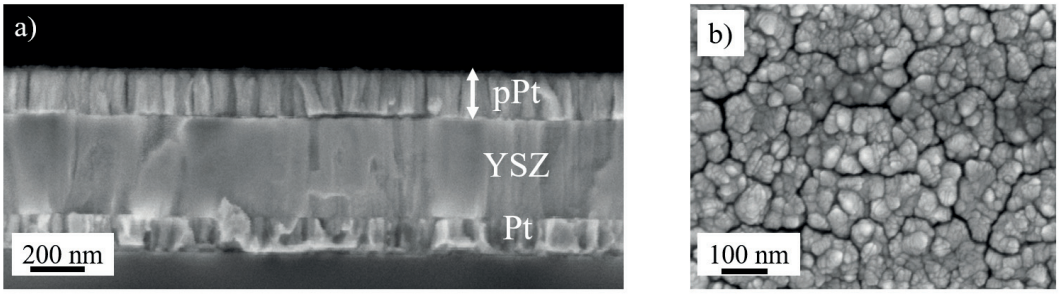


Figure 3.10 – SEM micrographs of porous platinum deposited with substrate rotation at low pressure a) cross-section and b) plain view

4 µSOFC Device Fabrication and Characterization

As it has been mentioned in the previous chapter, corrugated based structures have superior characteristics over the other concepts for making stable µSOFC *membranes. However, there are still some critical issues that have not been addressed. First is the optimal way of making corrugation that results in a smooth surface, avoids the stress concentration points and straight sidewalls. Second is the corrugation design that can result in stable liberation borders and increase the surface area density in liberated volume. In this chapter we propose a new concept so-called ring shaped corrugated membrane that can address the mentioned challenges. The electrochemical performance of the membranes at low operation temperature (350°C) has been also studied.*

4.1 Corrugated Structure

4.1.1 Substrate Patterning

The first approach was implementing Local Silicon Thermal Oxidation (LOCOS) as an established method in semiconductor industry [94]. LOCOS with well-known bird pick oxidation pattern generates blunt edges and also avoids straight walls. In this method, one has to cover the silicon wafer (w/o oxide layer) with a silicon nitride (SiN) layer as the sacrificing mask and perform a thermal oxidation after SiN patterning. Finally, the concave structure can be obtained by etching away both SiN and SiO_2 layers, Fig. 4.1.

The challenge of LOCOS process is making deep structures in the range of microns due to oxidation of SiN sacrificing layer. In fact, 500 nm low-stress SiN resistant toward oxidation can last for only hundreds of nm or hardly 1 μm of oxidation. Of course the thickness of SiN can be increased for deeper structures but in this case, high SiN tensile stresses would make deep stress trenches into the silicon substrate, see Fig. 4.1.

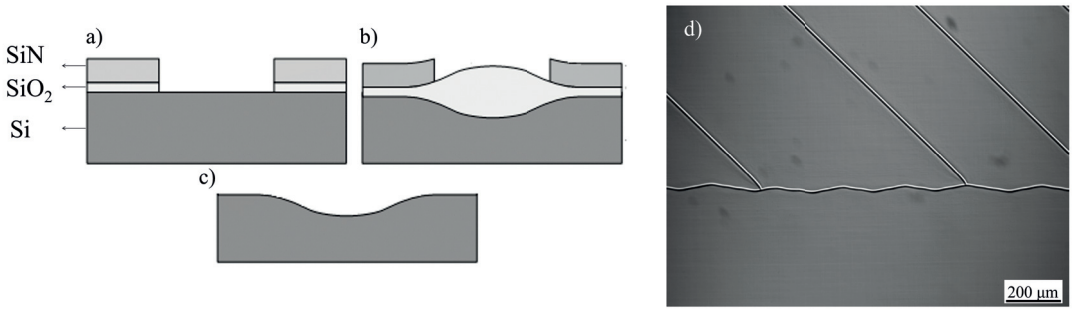


Figure 4.1 – Si substrate patterning using LOCOS method. a) SiN/SiO patterning, b) Wet oxidation, c) SiN/SiO etching, and d) trenches induced in silicon substrate as result of high SiN tensile stress

Isotropic etching (ISO) of silicon can be an alternative. However, the final surface roughness needs to be treated carefully. A diluted solution of hydrofluoric acid and nitric acid are generally used for Si-ISO. The diluent can be either water known as Polysilicon wet etching or acetic acid, HNA. The overall etching reaction is:

$$Si + HNO_3 + 6\,HF \longleftrightarrow H_2SiF_6 + HNO_2 + H_2O + H_2 \tag{4.1}$$

The etching occurs via a redox reaction followed by dissolution of the oxide by an acid (HF) that acts as a complexing agent. Fig. 4.2 summarizes how the topology of the Si surfaces depends strongly on the composition of the etch solution. Around the maximum etch rates the surface appears quite flat with rounded edges, and quit slow etching solutions lead to rough surfaces, a detailed discussion can be found in ref [95].

Both Polysilicon and HNA solution have been examined, Table 4.1 summarizes the final parameters that were used.

Table 4.1 – Different solutions of isotropic etching of silicon. The base parameters of HNA solution have been taken from ref [95].

Solution	HNO_3 (70%)	HF (50%)	H_2O	CH_3COOH
PolySi	50	3	20	-
HNA	7	2	-	1.5

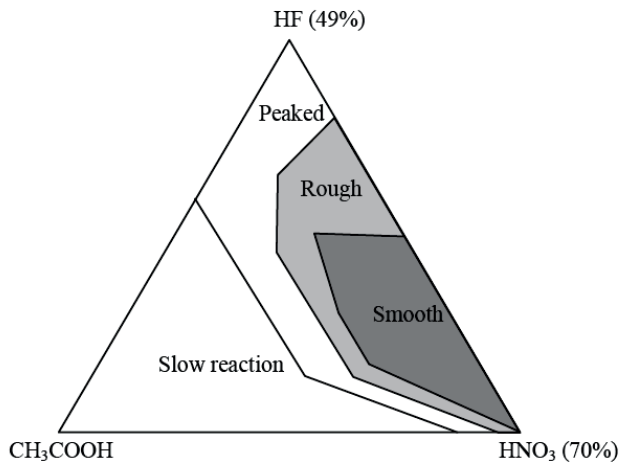


Figure 4.2 – Silicon topology as function of etchant composition [95]

The FastScan AFM scanner with standard ScanAsyst scanning mode was used to measure the surface roughness after etching for both solutions, Fig. 4.3. It can be seen that HNA gives smoother surface than PolySi since acetic acid better prevents the dissociation of nitric acid and preserves the oxidizing power of HNO_3, which depends on the non-dissociated nitric acid species [95]. The roughness (R_{rms}) was 12.4 and 1.2 nm for PolySi and HNA, respectively. In this method, like LOCOS a SiN layer has to be used as the mask layer. Fig. 4.6, shows the etching profile of 50 µm wide cavity using HNA solution.

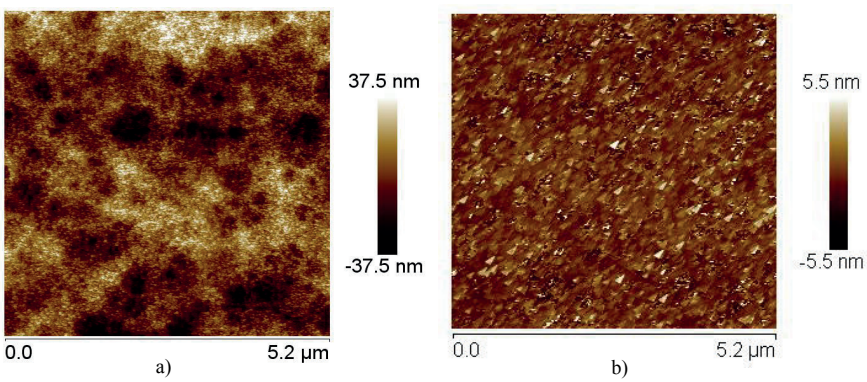


Figure 4.3 – AFM analysis for surface roughness measurement after wet etching of silicon with two different diluent a) H_2O (PolySi) b) CH_3COOH (HNA)

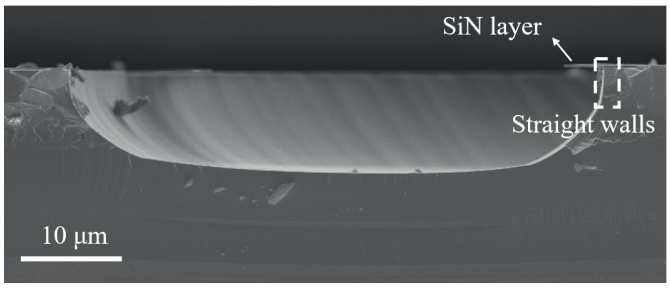
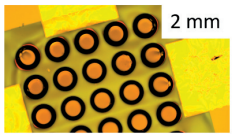
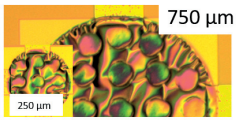
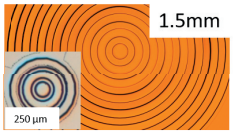


Figure 4.4 – Etch profile of 50 µm wide cavity using HNA solution

4.1.2 Corrugation Design

The basic design for corrugated membranes is hole-based. In this method, deep holes are etched through silicon substrate using Deep Reactive Ion Etching (DIRE). A problem of this method is the straight sidewalls and sharp corrugations angles that are very challenging for film coverage. This can be solved by Si isotropic etching as proposed in previous section. In continuation of the works published in the literature, we started with hole-based structures to fabricate our membranes. However, with this technique the problem of liberation borders are remained unsolved. In order to address this issue, we have proposed the ring-shaped structures in which the membrane is pre-bent at liberation border and becomes more stress-tolerant. The structure consists of ring-shaped cavities with a flat gap in between. The biggest cavity defines the membrane liberation border. The liberation border has to be positioned on the outer sidewall of the biggest cavity. The width of the cavities can be varied between ten to several hundreds of microns. The gap between the cavities has to be twice the etching depth. Since the isotropic etching of silicon is supposed to be the same in all directions, the gap has to be big enough to avoid the overlap of etch profiles of two neighboring cavities. The overlap can result in sharp peaks which are indeed not favorable. Table 4.2, summarizes different designs that have been used in this project.

Table 4.2 – Different corrugated designs that has been used in order to obtain buckle-free membrane with stable liberation borders.

Design	Structure parameters			Backside opening method	After liberation	Remarks
	Hole width (µm)	Hole depth (µm)	Active area width (mm)			
	300	20-30	2	Dry + KOH		- Very deep holes; problem with dry etching - Too big openings; high percentage of failure after back opening
	50	1-2	0.25-1.5	Dry		- Holes are not deep enough; the membranes do not follow in large scale - The borders have high potential of failure
	50	5	0.25-1.5	Dry		+ No buckling + The borders seem stable + High Surface utilization

4.2 µSOFC **Device Fabrication Process Flow**

The membrane fabrication was carried out using sequences of MEMS processing steps presented in Fig. 4.5. Here, we have used a 100 mm wide double side polished silicon wafer with a thickness of about 380 µm covered with 200 nm Low-stress silicon nitride (SiN). The process starts with SiN etching, Fig. 4.5 (b), that is served as the etching mask for Si substrate wet etching. After preparation of etching solution, HNO_3:HF:CH_3COOH (7:2:1), the Si substrate was etched for 20 seconds. The etch depth was about 11-15 µm. In order to avoid the sharp edges and also for eliminating the SiN layer, Chemical Mechanical Polishing (CMP) has been used. The polishing height is highly dependent on the shape of the etching profile but experimentally, it should be at least 30% of the etch depth. The polishing step can be replaced with the combination of grinding and polishing in which the sacrificing layer has to be etched or polished first and the silicon wafer will be grinned afterwards. For obtaining a smooth final surface, the wafer needs to be polished after grinding. Finally, the wafer was cleaned using BHF acid to get rid of any remaining silica particles that agglomerate into the cavities. To further reduce the angle of the etched profile, high angle etching has been done using Ion Beam Etcher (IBE). The wafer was tilted about 55° towards the ion beam that makes the beam to pass mostly over the surface hitting the corrugated angles, see Fig. 4.5 (c).

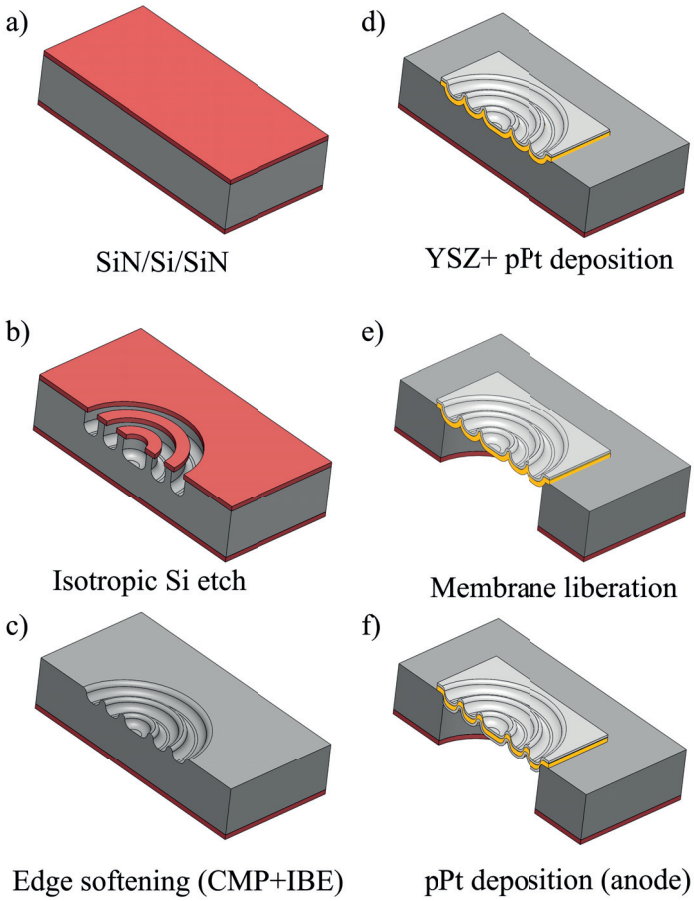


Figure 4.5 – Fabrication process flow of ring-shaped corrugated SOFC membrane.

After substrate preparation, YSZ electrolyte films were grown by RF sputtering at a power of 200 W from a stoichiometric target in 15 mTorr Ar pressure as discussed in the previous chapter. The substrate temperature was nominally 500°C. Porous Pt films were deposited from Pt foil target at 75 mTorr Ar pressure with a DC power to 100 W without substrate heating. After Pt/YSZ deposition, the films were patterned using conventional photolithography and IBE (Fig. 4.5 (d)). The YSZ etching rate was estimated as 60 nm/min. The membrane liberation was done using conventional Bosch process in which a sequential gas flows -SF_6/CF_4- results in directional etching (Fig. 4.5 (e)). The advantage of Bosch process over the commonly used KOH solution is high surface utilization and round-shaped opening. Due to the preferential etching of KOH the surface utilization of this method is rather poor, especially for small openings. Finally, porous Pt, with the same conditions for cathode deposition, was deposited through the silicon wafer to complete the PEN material stack.

The film coverage over the corrugated structures was studied using scanning electron microscopy (SEM). As it can be seen from Fig. 4.6(a) a good film coverage have been obtained over the edges. With this method, we are able to fabricate 1.5 mm wide membranes without any noticeable mechanical buckling and stable liberation borders, see Fig. 4.6(b).

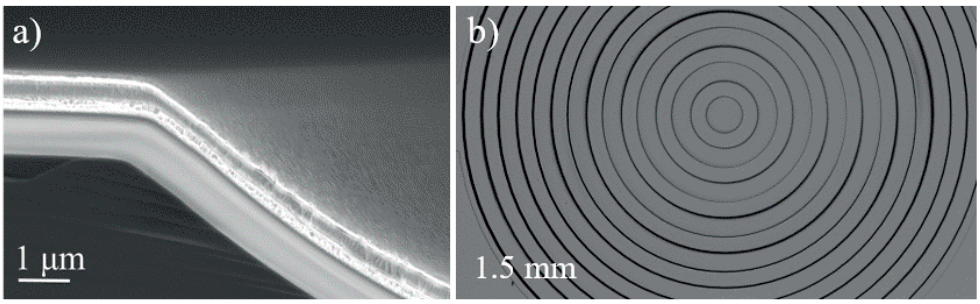


Figure 4.6 – a) Thin film coverage over corrugated structure (Pt/YSZ/Pt), b) 1.5 mm wide free standing membrane by ring-shaped corrugation

4.3 Membrane Mechanical Buckling

In order to study the mechanical buckling of the structure after substrate liberation, an optical profilometry analysis has been carried out using Veeco Wyko NT1100. The measurement was done in Vertical Shift Interference (VSI) mode which is based on white light vertical scanning interferometry [96]. Fig. 4.7 shows the three-dimensional surface profile of 750 µm wide membrane, as well as the membrane displacement line-scan through the center of the membrane. It can be seen that the maximum displacement is about 2.5 µm at the second ring.

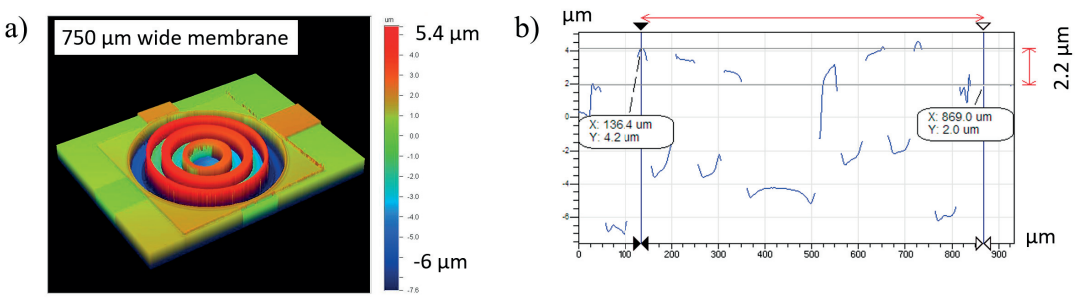


Figure 4.7 – a) 3D displacement of the membrane after the back-side liberation, b) membrane profile after back-side liberation, line-scan through center of the membrane

The same analysis has been done for different cell openings (200 µm to 1.5 mm), see Fig. 4.8. Up to 750 µm, the mechanical buckling is almost neglectable. In millimeters range, membrane displacement starts to grow and reaches 15 µm. While in mm range the buckling is still in the safe range, one can conclude that the optimal opening diameter is between 500 to 750 µm. This was predicted by numerical calculation presented in section 2.4. Therefore, in order to increase the power output, we shall go towards multi-array devices.

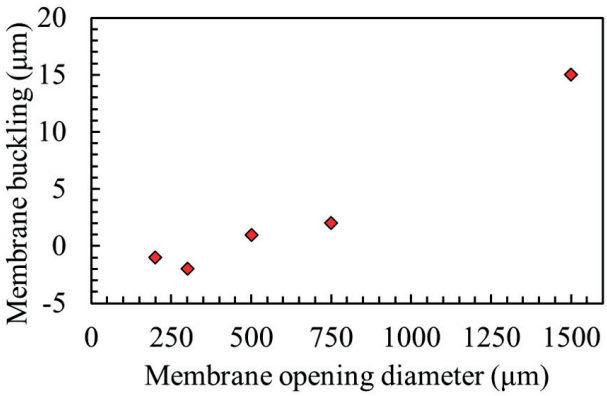


Figure 4.8 – Membrane displacement after substrate liberation as function of device opening

4.4 Electrochemical Performance of µSOFC Devices

The µSOFC performance was measured using a homemade setup with supplying a mixture of hydrogen and argon gases (50%) to the anode side, while the cathode was exposed to the air. A sample chip of 1.8×1.8 cm^2 was mounted on an alumina holder using Zircar cemet. The electrodes were accessed by home-made Pt-wire manipulators. The hotplate was surrounded by aluminum wall to preserve the heat radiation. The gas flow was controlled by MKS 647B. The setup was placed on a hotplate, capable of heating up to 350°C with the heating rate of 2°C/min. The cell was kept at 350°C for 2 hours. A digital multimeter (HP 34401) installed in parallel controlled the cell voltage. A variable resistance was used as a load and placed in parallel to µSOFC. The cell voltage was recorded by decreasing the resistance of the load. Fig. 4.9 shows the schematic view as well as the actual image of the presented setup.

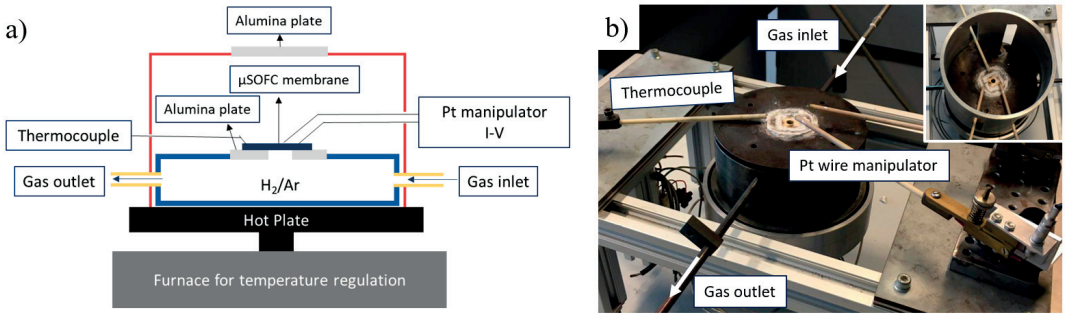


Figure 4.9 – Electrochemical performance measurement setup, a) the schematic view of the setup, the sample carrier with a gas chamber sitting on a hotplate capable of heating to 350°C, b) The actual view of the setup

Fig. 4.10 presents the I-V characteristics of 500 µm wide µSOFC with 500 nm YSZ electrolyte and 250 nm porous Pt electrodes. The OCV voltage, as well as the power density, are lower than expected values. Up to 200 mV reduction in OCV has normally reported as results of a slight gas leak between anode and cathode due to minor microstructural defects or testing apparatus sealing variation [34]. Moreover, an imperfect open circuit can also result in voltage drop. The fast voltage drop by decreasing the circuit resistance is most likely due to the activation polarization because of low operation temperature and a limited number of TPBs.

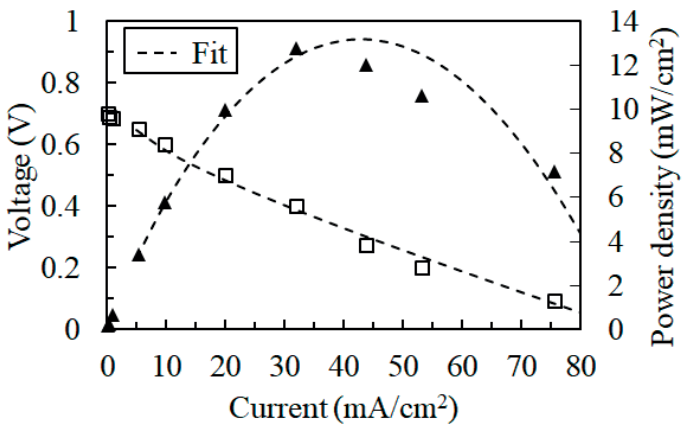


Figure 4.10 – I-V characteristics of 500 µm wide µSOFC with 500 nm YSZ electrolyte and 250 nm porous Pt electrodes at 350°C.

In order to quantitatively analysis the cell characteristics, we have used an analytical model that has been presented earlier by Sirkar et al [97] and Chan et al [98]. The model considers activation and ohmic polarizations as the main responsible for the voltage

drop and assumes that concentration polarization is neglectable. Thus, the cell potential was given as Eq. 4.2 [97]:

$$E = E_{OCV} - \eta_{Ohmic} - \eta_{Activation} \tag{4.2}$$

where

$$\eta_{Ohmic} = i\frac{t_f}{\sigma_f} \tag{4.3}$$

and

$$\eta_{Activation} = \frac{RT}{nF}\left(\frac{i}{i_1}\right) + \frac{2RT}{nF} ln\left(\frac{i}{i_2}\right) \tag{4.4}$$

(i) stands of current density, (t_f) is film thickness, (σ_f) is film conductivity, (R) is universal gas constant, (T) is operation temperature, (n) is the number of charges transferred, (F) is Faraday constant, (i_1) and (i_2) are the free parameters that are obtained from data fitting. The ohmic polarization is simply dependent on film thickness and conductivity. The film conductivity has been measured by DC conductivity measurement at 350°C, 0.004 (S/m).The activation polarization is following Butler-Volmer equation where each term corresponds to limiting cases for more general Butler-Volmer analysis [98]. By fitting the Eq. 4.2 to experimental data the the exchange current densities (i_1) and (i_2) are calculated as 45 A/m^2 and 13 A/m^2, respectively. In order to distinguish between Ohmic and activation polarization, one can plot Eq. 4.3 and 4.4 based on calculated current densities, see Fig. 4.11

As was expected, the activation polarization is dominating loss mechanism. This means that increasing the electrolyte thickness by a factor of 10 would not change the performance dramatically and one still needs to deal with the activation polarization. Hence, the electrolyte thickness has to be chosen based on the mechanical stability issues and further decreasing its thickness to sub 100 nm is not necessarily. The first task to lower the activation polarization is to increase the operation temperature to more than 500°C. Furthermore, Kerman et al [34] have reported that increasing the electrode thickness by few nanometers will change the number of TPBs and the optimal thickness is about 100 nm. Thus, the second task is to decrease the electrode thickness. Nevertheless, the

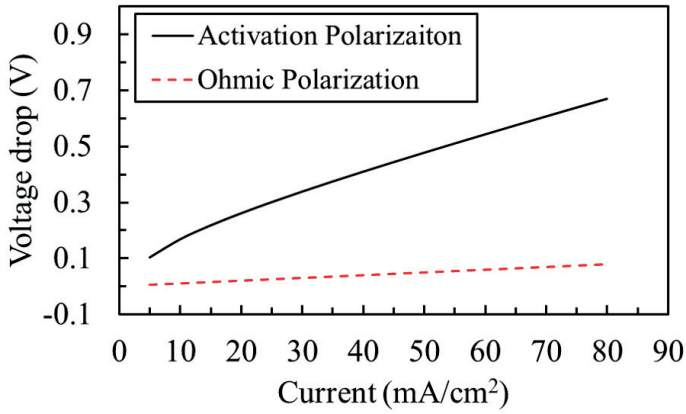


Figure 4.11 – Comparison of Ohmic and activation polarization at 350°C operation temperature for 500 µm wide µSOFC with 500 nm YSZ electrolyte and 250 nm porous Pt electrodes

measured power density, 12.5 mW/cm^2, for µSOFC with 500 nm thick electrolyte at 350°C is comparable to the reported results at same operation temperature. For instance, Kerman et al reported 20 mW/cm^2 for 100 nm thick YSZ [34], and Huang et al published 5 mW/cm^2 with YSZ/CGO/YSZ (100/300/100 nm) electrolyte for a supported membrane [59]. In the same reports by increasing the operation temperature from 350 to 500°C, the power density increased t0 500 and 200 mW/cm^2, respectively. Thus, one can expect to obtain more or less the same response with increasing the temperature.

4.5 Summary

We have proposed a new concept for upscaling µSOFC membranes. The idea is based on ring-shaped corrugation which results in a mechanically stable membrane. Stable liberation border, neglectable mechanical buckling, round-shaped opening, as well as increased active area in given volume (contribution of sidewalls), are the main advantages of this concept. The power density at 350°C, 12.5 mW/cm^2, is comparable to the published results at the same temperature. Our studies show that the main polarization that needs to be dealt with is the activation polarization which is highly dependent on the operation temperature and electrodes. The ideal temperature might be 600-800°C to be able to use mixed-electronic ionic conductor electrodes, and meanwhile, increase the electrolyte thickness to few microns. In this way, besides the enhanced electrochemical performance, the mechanical stability and device endurance are secured. Finally, we have seen that the optimal device size, in term of mechanical stability, is 500-750µm. Hence, in order to increase the output power, a multi-array of devices is suggested.

Part II

Resistive Random Access Memories (ReRAMs)

5 Physical Principle and Status

5.1 Towards Resistive Switching Memories

Semiconductor memories are essential components of today's electronic market and systems. Functionalities and performance of computing systems are highly dependent on the memory block, known as Von Neumann bottleneck. Von Neumann architecture for a classical computer is compromised of a central processing unit (CPU) and a memory holding instructions and data [99]. Due to recent advancement in CPU technology the holding unit is the memory block. Thus, there is an ever increasing effort to improve the performance or finding an alternative for currently used memory technologies. Fig. 5.1 shows the classical hierarchy of memory technologies.

On top of the memory hierarchy (see Fig. 5.1), Static Random Access Memories (SRAMs) are providing the fastest operation speed (write/read 10/10 ns) close to the CPU unit [100], below is occupied by Dynamic Random Access Memories (DRAMs). They have at least 30 times lower operation speed, but higher scalability [101]. SRAMs are consist of 6 transistors while DRAMs have only one transistor and a capacitor. Thus, SRAMs are normally used in cache memories where speed is very crucial and DRAMs are used as main memory where the capacitance is important for temporary information [102]. At the bottom, we find Flash memories (NAND and NOR type[1]) which is much slower than DRAM and SRAM. Their write/read is in order of 1/0.1 ms, therefore they are mostly used as the second storage. Finally, the slowest memories are hard disks, stocking information in a ferromagnetic domain of Co films. The main difference between DRAMs/SRAMs and Flash memories is the memory retention where DRAMs/SRAMs are volatile memories meaning that the information will be lost by power shut down and Flash memories and hard disks are non-volatile that can keep the information without an applied power. Flash memories have become very cheap. Their endurance

[1] A logic-gate which generates an output when all the inputs are true. In NOR an output is produced when all the inputs are false

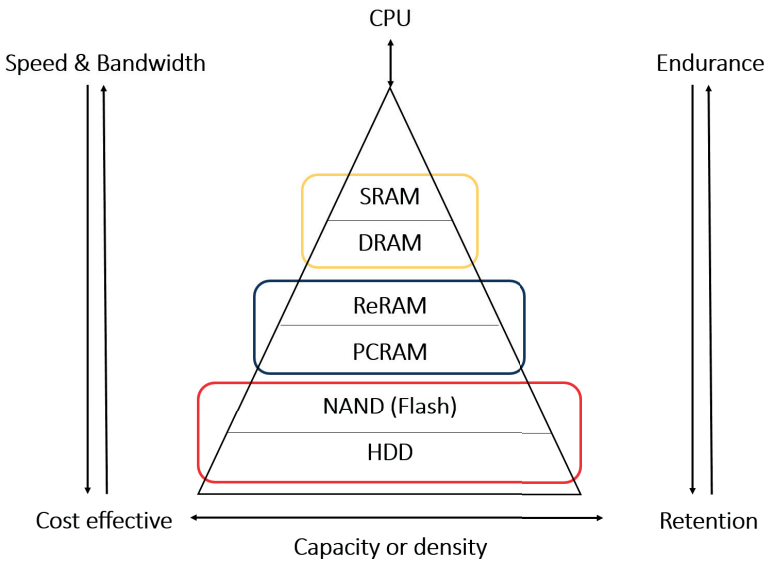


Figure 5.1 – The memory storage hierarchy showing the potential of ReRAM and PCRAM memories for combining the advantages of currently used memories while avoiding their short comes.

is not as high as the one of a magnetic disk. Nevertheless, they have replaced the latter in portable computers. Still, one would like to dispose of memories that have a better endurance, and a faster writing speed. Like DRAMs/SRAMs, Flash memories are charge based. The endurance is assured by electrons that are trapped in floating gates. The main issue with the charge-based memories is the scalability since a minimal dielectric wall thickness is required to keep electrons permanently trapped. This appears to be impossible below 10 nm technology node [2]. Nowadays, lots of efforts are spent to find an alternative solution combining the advantages of existing memories while avoiding their drawbacks [103]. The new technologies are required to have simple fabrication, high stability, low switching time, high scalability and a good compatibility with complementary metal-oxide semiconductor (CMOS) technology.

Among different concepts that have been proposed so far, Phase Change Random Access Memories (PCRAMs) [104] and Resistive Random Access Memories (ReRAMs)[105] are the most promising emerging technologies. In both memories, the information is stored based on bistable resistance states. In PCRAMs the resistance switching is due to the phase change between a crystalline and an amorphous phase of a chalcogenide material, whereas, resistance switching in ReRAM is based on the creation and rupture

[2]Different nodes often imply the circuit generation and design in which the smaller technology node means the smaller feature size (transistors)

of a conductive path in an insulating thin film. The ion-migration at nanoscale turned out to be the key element in ReRAM performance. ReRAMs thus has become a topic in Nanoionics.

5.2 ReRAM Characteristics and Switching Mechanisms

A resistive memory is a capacitor like structure in which an insulating layer is sandwiched between two conductive electrodes a so-called MIM. The MIM cells can be electrically switched between at least two resistance states. By applying appropriate voltage to the structure, the device can change its resistance between high resistance state (HRS) and low resistance state (LRS). Pristine state of ReRAMs have high initial resistance and an electroforming process is required to form a conductive path [106]. After the forming process, the resistive state can be switched by applying a bias across the device which is smaller than the forming voltage. The switching from HRS to LRS is the "Set" process and in the "Reset" process, the switching is bi-directional. One or several conductive filaments (CF) formed during the formin step are responsible for achieving the low resistance state. The filament formation occurs in kind of soft break-down. For both forming and set process the maximum current flowing through the device has to be limited in order to prevent the hard breakdown. This is normally done by a parameter analyzer (a resistor or transistor) in series to the memory device. Rupture and re-creation (repair) of the filament is happening at nano-scale time and size which means that the size and operation speed of the memory devices can potentially reach nanoseconds.

The I-V characteristics of devices are normally shown as semi-log plots, where the x-axis is the applied voltage and y-axis is the measured current in logarithmic scale. Depending on the bias polarity, unipolar switching Fig. 5.2 (a) and bipolar switching Fig. 5.2 (b) are observed.

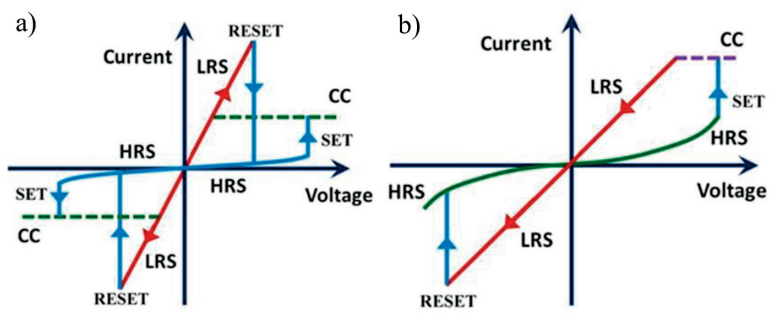


Figure 5.2 – a) Unipolar Switching mode, b) Bipolar Switching mode [106]

After formation of the CF in the set process, the filament is ruptured due to the Joule heating in the reset step when employing unipolar switching. To reset the memory the compliance current is canceled and a voltage signal with the same polarity as the set voltage is applied. After the set process, the material is in LRS, and can be heated by applying an electric field. At high enough temperature, ions start to move -especially around the conductive filament- which eventually leads to in CF rupture [106]. In contrast, in bipolar switching after the creation of conductive filament, a bias voltage with reversed polarity is needed to recover the HRS.

The nature of the conductive filament depends on the chosen materials. Either a metallic filament (Electrochemical metalization cell (ECM)) or oxygen vacancies filament (valance change memory (VCM)) [107] is formed under an electric potential. Fig 5.3 schematically shows the basic principle of ECM memory accompanied by I-V characteristics. The device is made of an electrochemically active electrode such as Ag, Cu, or Ni, as well as an electrochemically inert counter electrode,i.e. Pt, Ir, or Au and a thin ion conducting electrolyte [105]. Due to the fast diffusion of Ag ions through the electrolyte, a conductive filament is formed. By applying an opposite electric field Ag ions move back towards the Ag electrode and the resistance switches back to high values.

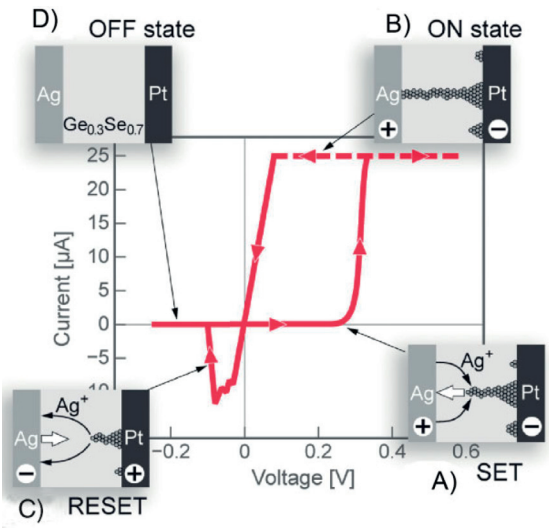


Figure 5.3 – Schematic view of filamentary switching in ECM memories with Pt/Ag-Ge-Se/Pt material stack. a) pristine state of the memory b) the formation of conductive filament (Ag filament) under application of sufficiently high electric field (electroforming) c) reset process by applying sufficiently high reversed potential, d) re-creation of CF at set step [105].

In VCM memories, the oxygen vacancy plays the main role for making the conducting filament. Fig. 5.4 is schematic illustration of VCM filamentary switching. During forming, a soft breakdown happens and oxygens drift toward the top electrode (with

positive electrical potential). In the case of a noble top electrode, the ions are discharged as non-lattice oxygens. However, if the top electrode is oxidizing, an interfacial oxide layer will be formed which can act as an oxygen reservoir. During the reset process, the oxygen ions go back to bulk oxide and the memory returns to HRS [108]. Since the conductive filament is partially ruptured the recovered resistance state is lower than pristine values. The rupture can take place either at electrodes interfaces or at the middle of the filament. In the set process, the process follows the same mechanism as the forming step, however, with lower applied voltage due to existence of incomplete CF.

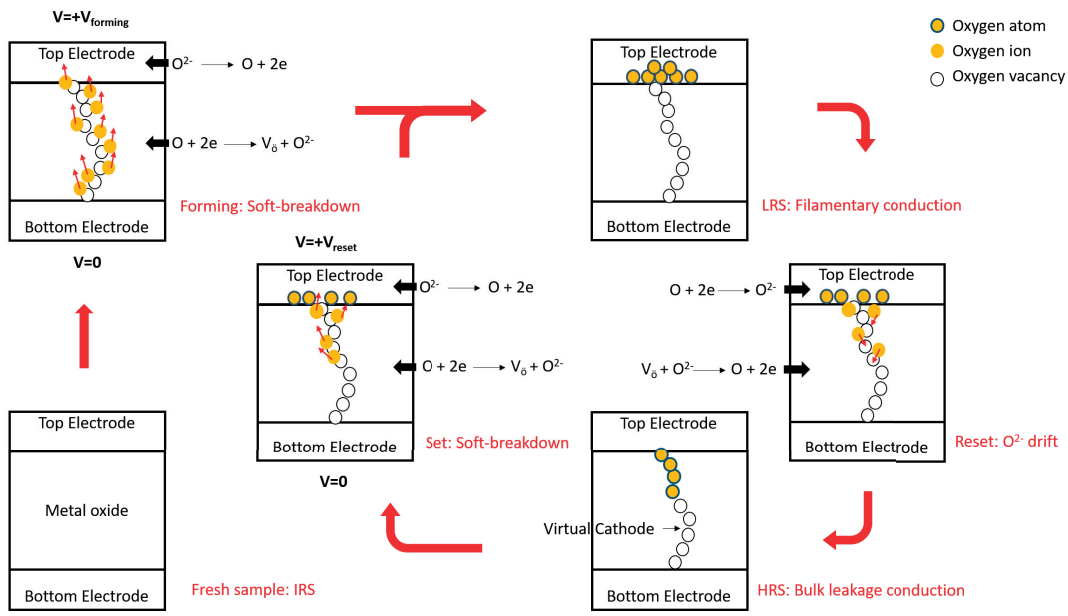


Figure 5.4 – Illustration of switching process in metal-oxide-metal ReRAM adopted from Ref. [108]

While in most cases CF is presented as the responsible mechanism, in some devices an interface modification can lead to resistance switching known as interface-type switching. The fingerprint of the interface-type switching is the scaling of the device resistance with the device size [109], see Fig. 5.5, as the entire electrode area is contributing in resistance switching. Nevertheless, it should be noted that the change of resistance state by the area cannot solely be sufficient for the interface-type switching. As in multi-filament switching, one can also observe the scaling effect.

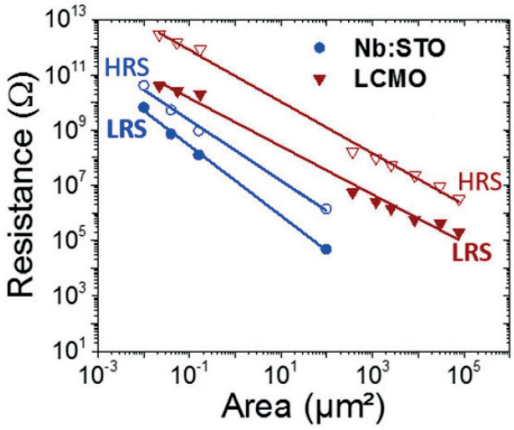


Figure 5.5 – Resistance scaling in interface-type switching with the device size[109].

Among different mechanisms that have been proposed for the interface-type switching [106, 107], VCM is the most commonly understood and used mechanism. Similar to the VCM filamentary type, the resistance switching is due to the movements of defects or more particularly of oxygen vacancies under the application of an electric field, although, the phenomenon is restricted to the electrode interface. Normally, a semiconductor layer is sandwiched between an electrode with ohmic contact (low work function metal) and one with Schottky contact (high work function metal). The applied voltage changes the barrier height by transport of oxygen vacancies into the Schottky barrier region and the resistance switches between HRS and LRS. By applying a negative voltage to the Schottky contact, the oxygen vacancies are attracted to the interface reducing the depletion region and facilitate the electron tunneling. A positive electric field repulses the oxygen vacancies and restores the barrier height, thus, recovering the HRS state, see Fig. 5.6.

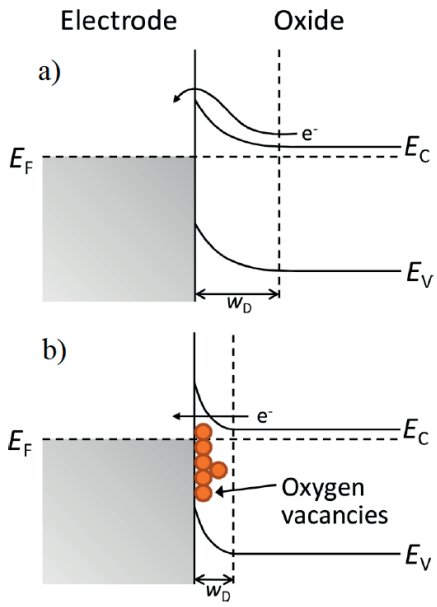


Figure 5.6 – a) At HRS there is a lack of oxygen vacancies at the interface thus the carrier must overcome the Schottky barrier to contribute to current, b) At LRS oxygen vacancies are accumulated at the interface reducing depletion width in a way that electron tunneling is more feasible [110].

5.3 General Requirements

With considering the circuit requirements of high density non-volatile memories such as FLASH and with taking into the account the prediction about technology requirement in near future, one can define some basic needs for ReRAMs [105], in write (set)/read (reset) operation, resistance ratio, endurance, and retention.

- The *write* voltage should be from hundred mV to few volts to be compatible with scaled CMOS and have a great advantage over FLASH memories. The duration of write voltages has to be less than 100 ns to be comparable to DRAMs. If one can obtain less than 10 ns operation speed it can even compete with SRAMs.
- The *read* voltage has to be considerably smaller than *write* voltage in order to avoid any changes in resistance state during the read operation. The operation speed should be in the same range as *write* process or preferably shorter.
- The *resistance ratio* of 1.2 to 1.3 is detectable by dedicated circuit designs, however, more than 10 ratio is needed for small and highly efficient amplifiers which makes ReRAM cost competitive with FLASH memories.
- FLASH memories *endurance* are normally limited to 10^3-10^7 number of cycles

depending on the type thus a comparable number of cycles or even more should be provided by ReRAMs.

- A data *retention* of more 10 years is required which has to be kept at thermal stress up to 85°C and small electrical stress such as a continuous stream of reading voltage [105].

5.4 Thin Films in Use

Binary oxides are the most studied materials as they are showing the best switching properties. GeO_x and TaO_x are showing ultra-high ON/OFF ratio (>10^9), SiO_x, HfO_x and TaO_x are having sub-nano second operation speed, and TaO_x exhibits very high endurance (>10^{12} cycles). One can also add alumina, nickel oxide, tungsten oxide and copper oxide, where the last two ones are the highly compatible with CMOS process [111, 112, 16, 15, 113]. Fig. 5.7, gives an overview of the materials that have been used as switching layer (yellow) or electrode (blue). Furthermore, Table 1 in ref [111] gives a complete summary of common inorganic storage media with corresponding switching characteristics. Recently, HfO_x [114] and TaO_x [115] has been in high attention of research communities due to their fast operation (sub nanosecond) and high endurance, >10^{12} cycles. Therefore, they can be the most promising storage media in future.

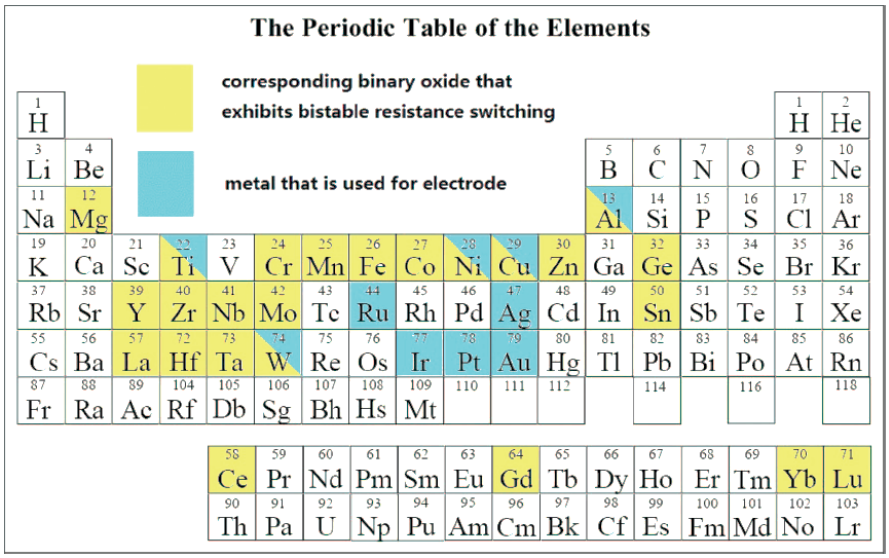


Figure 5.7 – Overview of the materials that have been used as switching layer in ReRAM devices. Yellow: Switching layer, Blue: Electrodes [108].

ALD [116], PLD [117] and Magnetron sputtering [118] are common techniques for depositing switching layers. Sputtering is becoming more popular due to its high yield and

low costs. Moreover, almost all the mentioned materials can be deposited by sputtering. In case of PLD, since it is not a highly used method in the semiconductor industry, basically due to high cost and its local uniformity, it is not a preferable technique for deposition. The interest in ALD deposition is increasing during past years because of its precision in both thickness and uniformity and film quality. In order to obtain superior switching properties, one should deposit <10 nm films, mostly through small via, hence ALD tends to be the best method. However, very limited oxide deposition have been optimized by ALD, e.g Al_2O_3 and TiO_2, and the others are still under developments. Therefore, for the moment, sputtering seems to be the only suitable method for investigating new material and structures.

5.4.1 CeO_2 based ReRAMs

Cerium oxide, CeO_2, is a well-established mixed ionic-electronic conductor that potentially can exhibit fast resistive switching. In fact, the coexistence and reversible valance state transition of Ce^{4+} and Ce^{3+} can lead to rapid creation and rupture of oxygen vacancies which is very critical for resistive switching [119]. So far, there are very limited reports on resistance switching of ceria, see Table 5.1, and in most of them, oxygen vacancies and filamentary switching have been proposed as the switching mechanisms. Different concepts including using an interlayer layer, i.e. Si [120] and Al [121], as well as CeO_2 nano-cubes [119] have been reported. High formation power, either high voltage or high compliance current, was the main short come of published works. Younis et al with using of CeO_2 nano-cubes reported outstanding resistance window (10^4) however at high operation (-2 to 2 V) voltage and compliance current (60 mA). With introducing Al interlayer Ismail and co-workers [121] had improved the cell performance by lowering the compliance current to 10 mA, although, the resistance window decreased to 10^2. The high forming power (P=VI) can be due to a limited number of oxygen vacancies that can be enhanced by using doped structures such as Gd doped ceria.

Table 5.1 – Review of ceria based ReRAM devices. HRS: High Resistance State, LRS: Low Resistance State, CC: Compliance Current

Year	Ref.	Structure	Thickness (nm)	Forming (V)	Set (V)	Reset (V)	HRS/LRS	CC (mA)
2005	[122]	$La_{0.67}Ca_{0.33}MnO_3$-CeO-Ag	400-80-N	-	4	-4	10^5	10
2008	[123]	Pt-CeO-Pt	80-180-80	9	4	1	10^4	5
2009	[124]	Pt-CeO-Al	N-40-100	8	0.7	-1.5	4	5
	[125]	Al-CeO-Pt	100-40-N	-	0.6	-1.5	400	-
2012	[126]	Pt-CeO-TiN	150-50-100	-3.2	-1.1	2.2	100	10
	[120]	W-CeO-Si-TiN	50-20-1-15	3	3	-3	10	1
	[120]	W-CeO-TiN	50-20-15	7.2	3	-3	2	5
	[127]	Au-CeO-ITO	-	-	3	-3	4	50
	[128]	TaN-CeO-Ru	80-20-100	-	2	-3	10^6	0.5
2013	[119]	Au-CeO (cubes)-Au	50-162-N	-	2	-2	10^4	60
	[129]	SnO_2-$Ce_{(1-x)}Co_xO$-Au	-	-	2.2	-2.2	10^3	-
	[130]	In-Nb:$SrTiO_3$-CeO/ZnO-Ag	N-10/100-N	-	2	-3	100	5
2014	[18]	Pt-CeO-TiN	50-20-80	-	-3	2	10^3	1
			50-30-80	-	-2	2	10^4	1
			50-40-80	-	-1	2	10^5	1
	[131]	$La_{0.5}Sr_{0.5}CoO_3$-CeO-Ag	500-80-300	-	4	-4	-	-
	[132]	Au-CeO-Nb:$SrTiO_3$	-	-	1.8	-4	5×10^4	1
	[133]	Pt-$La_{0.7}(Sr_{0.1}Ca_{0.9})MnO_3$-CeO	-	-	4	-4	100	-
2015	[134]	ITO-CeO-CeO_x-Ti-TiN	N-15-6/8-50-20	2	2	-2	200	0.5
2016	[121]	Pt-CeO-Al-CeO-Ti	N-3-1-2-N	-	2	-2	100	10
2017	[135]	Pt-CeO-Cu	N-3.4-N	10	10	-10	-	-
	[136]	Pt-$Ce_{0.9}Gd_{0.1}O_x/Er_2O_3$-Cu	N-3.4-N	-	200	-200	15	-
	[137]	Pt-$Ce_{(1-x)}Gd_xO_x$-Pt	N-500-N	-	10	-10	200	-

Recently, Younis et al [17] have studied the filamentary switching in 10% Gd doped ceria, where it has been shown that the switching performance can be manipulated by means of UV radiation. By application of UV light due to the high concentration of oxygen vacancies one can form multi-filament in CGO thin films and consequently obtain multi-step switching. The ON/OFF ratio was enhanced by a factor of 100 under radiation of UV light. The set voltage was reduced from 2.56 V to 2.2 V. In reset process two resistance steps have been obtained, Fig. 5.8. Fifty consecutive cycles have been made and three resistance states were clearly separable. This finding confirms the potential of Gd doped ceria thin films to be studied for memory devices, however, the compliance current is still high (10 mA).

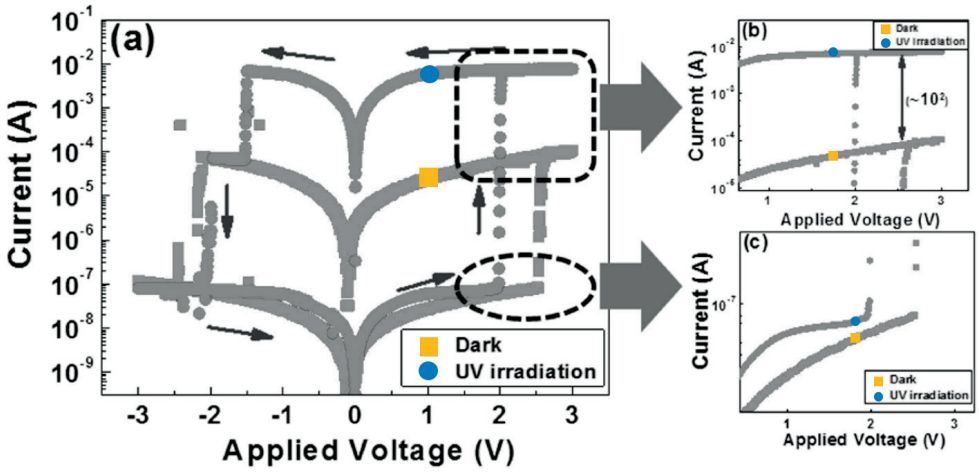


Figure 5.8 – a) I-V curve in semi-logarithmic scale under dark conditions (blue) and under UV irradiation (pink). b,c) magnified images of low-resistance and high-resistance states adopted from Ref. [17].

Furthermore, $Ce_{(1-x)}Gd_xO_{2-y}$ solid solution was investigated by Schmitt and co-workers [137] to probe the role of oxygen vacancies either as "free", or as "immobile and clustered" for the resistive switching performance. The strongest ON/OFF ratio was obtained for 20% Gd doping which coincides with the known composition leading to the maximum ion conductivity [138]. The analogy between ion conductivity and resistive switching was explained based on the configuration of oxygen vacancies, referred as "free" versus "clustered". By increasing the oxygen vacancy concentration, they start to interact with each other which results in less effective mobility (ion conductivity). This is expected to affect the forming step in resistive switching. Increasing the dopant concentration to 30% almost kills the switching behavior as result of defect clustering. Unfortunately, the film thickness in this study was chosen as 500 nm, thus one cannot evaluate the I-V characteristics for device implementation.

5.4.2 ZrO_2 based ReRAMs

The number of studies on zirconium oxide is even more limited than ceria as it is expected to show similar behavior to HfO_2 and an enhanced performance is not expected. The advantage of zirconia is its stability due to its single valance state, and within the operation conditions, the phase transition is not an issue. Table 5.2 summarizes the works that has been published on zirconia based devices.

The common feature for zirconia thin films is high forming voltage which can be due to the limited number of oxygen vacancies [139, 146]. One can expect that adding

Table 5.2 – Review of zirconia (ZrO_2) based ReRAM devices. HRS: High Resistance State, LRS: Low Resistance State, CC: Compliance Current

Year	Ref.	Structure	Thickness (nm)	Forming (V)	Set (V)	Reset (V)	HRS/LRS	CC (mA)
2010	[139]	Ti-ZrO-Pt	150-40-	8	0.7	-1.5	100	10
2011	[140]	Cu-ZrO-Pt	70-20-80	-	4.43	-0.76	10^4	1
	[141]	W-YSZ-$Pr_{0.7}Ca_{0.3}MnO_3$-Pt	70-10-80	-	3	-5	10^4	-
2014	[142]	Cu-ZrO-TaN	200–200	-	1.5	0.5	10^5	0.1
	[143]	Ti-ZrO-Pt	90–90	-	1.2	1.7	100	0.5
	[144]	Nb:$SrTiO_3$-YSZ-Pt	N-80-N	-	3	-3	10^5	10
	[145]	Au-YSZ-TiN	N-12-N	-3	3	-2	-	10
2015	[146]	Pt-ZrO-TiN	100-14-4-30	7-8	2-6	1-4	6	1
	[147]	Si-ZrO-Pt	N-5-N	-	-8	8	-	-
2016	[148]	Au-Zr-YSZ-TiN-Ti	40-40-25	-5.5	5.5	-3.5	10^3	100

yttrium as trivalent dopant can reduce the forming voltage which, in fact, can be seen by comparing the results published on pure and doped zirconia thin films. The puzzling feature about the YSZ thin films is the high set and reset voltage, close to forming voltage, suggesting that in each set and reset the filament is created and destroyed completely [145]. The preliminary results are very interesting, however, further studies are needed to be able to make a precise conclusion about the potential of YSZ to be used as a switching layer.

6 ReRAM Device Fabrication and Characterization

We have studied the potential of CGO and YSZ thin films to be used as the switching layer in ReRAM devices. This work has been done in collaboration with Microsystems Laboratory (LSM) of EPFL. The presented discussion is taken from a paper manuscript that has been prepared with equal contribution of Elmira Shahrabi from LSM.

6.1 Device Fabrication

A Bottom electrode (BE) of Pt/Ti (100 nm/5 nm) is deposited on a 100 mm wide Si wafer using the magnetron sputtering (Pfeiffer SPIDER 600 Cluster) at room temperature. The deposition parameters are presented in Table 6.1. The Ti layer was deposited to improve the adhesion layer of Pt layer on the SiO_2 surface.

Table 6.1 – Pt/Ti bottom electrode deposition conditions prepared by Spider 600

Thin film	Thickness (nm)	DC power (W)	Ar flow (sccm)	Temperature (°C)
Ti	5	1000	15	RT
Pt	100	1000	15	RT

The BE is then patterned via Reactive Ion Etching (RIE) in a Cl_2 /BCl_3 ambient using RIE/ICP (Reactive ion Etching coupled with Inductively Coupled Plasma) reactor (STS,Multiplex ICP). The etching chamber was cleaned before the process by O_2-based plasma (50 sccm O_2, 20 mTorr, 800 W) for 5 min. Afterwards, in order to avoid the bottom and top electrode contact a passivation process (100 nm Low temperature SiO_2 (LTO) deposition using Low Pressure Chemical Vapor Deposition (LPCVD) technique) was carried out. In LPCVD, a SiO_2 layer is deposited by the chemical reaction of Silane (SiH_4) with oxygen at the temperature of 400-450°C. To form the memory active area, 1µm-10 µm wide vias were etched through the LTO layer using BHF solution. Finally, the

wafer was diced into 30 times 2×2 cm^2 chips. Before switching layer and top electrode (TE) deposition a chip-sized shadow mask was installed on the chips to fabricate multi ReRAM cells. The Si-based shadow masks were prepared using conventional Deep Reactive Ion Etching (DIRE) accompanied by wafer grinding to obtain the trenches of 300 µm square side. It is important to have sufficient large trenches for the correct via alignment. Fig. 6.1 shows schematically the principle of shadow mask technique.

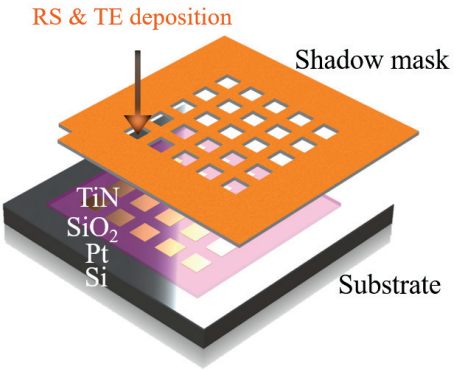


Figure 6.1 – ReRAM fabrication using the shadow mask technique. A 2×2 cm^2 chips with patterned Pt/Ti electrode is placed under a shadow mask prior to CGO and YSZ, as well as top electrode deposition. This method is used for cost effective device fabrication and fast feasibility study

CGO and YSZ depositions were performed using Nordiko RF magnetron sputtering, presented in previous part 3.1.1. The deposition parameters can be found in Table 6.2. The parameters were chosen according to our experience for obtaining highly defective films with good film uniformity.

Table 6.2 – CGO and YSZ switching layer deposition conditions using Nordiko Sys.

Thin film	Deposition pressure (mTorr)	RF power (W)	Ar flow (sccm)	Temperature (°C)
CGO	10	200	10	RT
YSZ	15	200	30	RT

For the final step, a 100 nm TiN top electrode (TE) was sputter deposited at room temperature by Alliance-Concept DP 650 to complete the device structure. The process was done based on the standard receipt provided by CMi. The films are deposited from a Ti target at Ar/N_2 (40/40 sccm) plasma at 1000 W. Fig. 6.2 presents the schematic view of the device fabrication process flow.

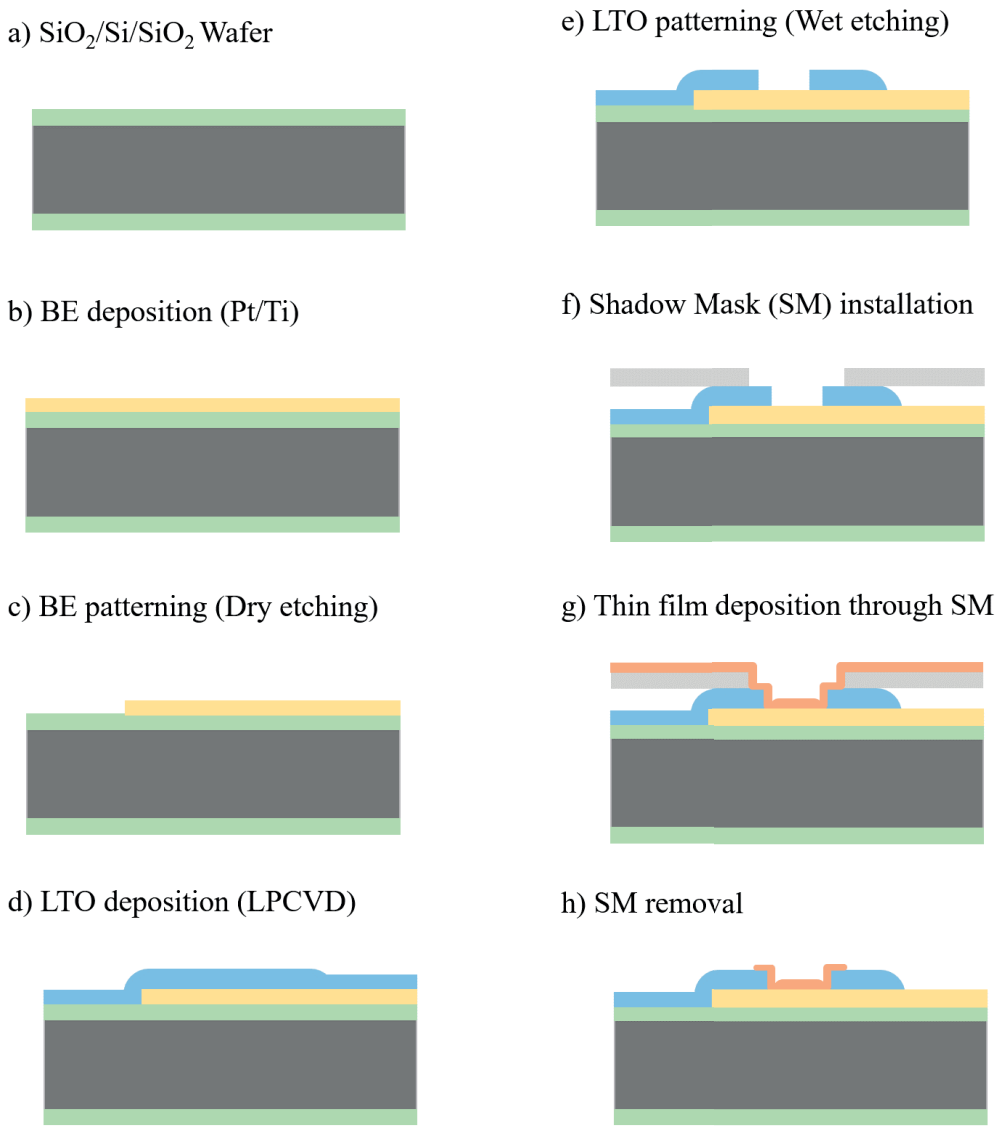


Figure 6.2 – a) the fabrication was done using 380 µm Si wafer passivated with 500 nm SiO_2 b) Pt/Ti (100/5 nm) bottom electrode (BE) was sputter deposited at room temperature, c) the BE was patterned using conventional photolithography and dry etching, d) in order to avoid any cross-talk between the top and bottom electrode a low temperature silicon oxide (LTO) was deposited using LPCVD, e) the LTO layer was patterned using BHF solution (wet etching), f) a shadow mask was installed before the switching layer (CGO or YSZ) and top electrode deposition, g) after thin film depositions the shadow mask was removed.

6.2 Characterization Methods

6.2.1 DC I-V Characterization

The DC electrical characterization was performed using a Keysight B1500 semiconductor device parameter analyzer in the dark room environment and in the quasi-static conditions. The bias voltage was always applied on the ReRAM TE while the BE is grounded during the measurements. Initially, the cells were at the HRS, thus a steady positive voltage was applied with the speed of 0.4 V/s to "form" the devices. After forming, a negative voltage is applied to "reset" the device (LRS to HRS). The process was followed by "set" process (HRS to LRS). Afterwards, the cells were cycled for 50 times within corresponding (-2 to 2 V) voltages, with the step of 2 mV and the voltage speed of 1V/s. During the forming and set operations, 500 μA CC was used to limit the maximum current flowing through the test device while no CC was employed for the reset operation. The DC measurements setup is illustrated in Fig. 6.3 (a).

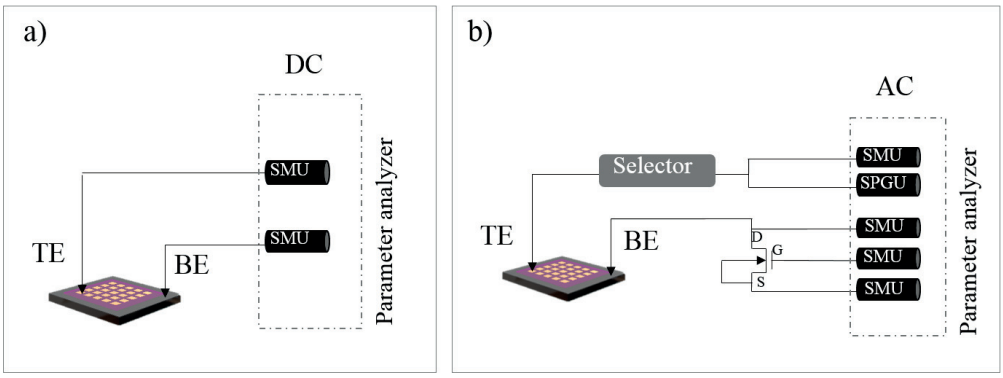


Figure 6.3 – Schematic of electrical measurements setup in a) DC mode. b) Pulse mode operation

6.2.2 AC Pulse Measurement

In order to evaluate the memories endurance, an AC Pulse measurement has been performed. The setup scheme is demonstrated in Fig. 6.3 (b). The system is bridled by a custom python program via GPIB connection. A nMOSFET (IRLB8721PbF) is connected in series to the ReRAM device with the test fixture. The V_{gate} of 1.969 V corresponds to CC of 150 μA limits the current through the transistor during the set pulse operation and the V_{source} is fixed to 0V. For the reset pulse operation, V_{gate} node is set to 0V (no CC) and V_{drain} is set to ground. After certain series of write pulse operation with the pulse width of 50 μs and pulse slope of 20 %, the reset and set pulse are coupled with a DC read operation in order to ascertain the resistance value after and before each write pulse. For the read operation, a small fixed double ramp value between 200 mV to

250 mV is applied to minimize the resistance state variation during the read operation. The details of the pulse parameters are explained for each device accordingly.

6.3 CGO-Based ReRAMs

Fig. 6.4 presents the I-V performance of 14 nm thick CGO-based ReRAMs, as well as its DC stability, over multiple cycles. A forming process has been carried out to switch from HRS to LRS which appears as red in Fig. 6.4 (a). The forming voltage, 2.3 V, has been lowered significantly compared to undoped films 7.2-10 V [120, 121]. This shows the impact of an enhanced number of oxygen vacancies due to the Gd doping that can facilitate the formation of conductive filament. 20% Gd doing is expected to generate 5% oxygen vacancies in addition to the ones that are created due to the reduction of Ce^{4+} to Ce^{3+}. According to our previous work [149], preparing CGO thin films without substrate heating can have 2-4% additional oxygen vacancies due to cerium valance change. A reduction of 5-10% elastic modulus has been observed in room temperature samples that correspond to 2-4% oxygen vacancy concentration [150, 151]. Besides the lower forming voltage, the CC has been significantly reduced (500µA). This means that our forming energy in comparison to the reported results for undoped films, modified structures ($CeO_2/Al/CeO_2$) and even doped films ($Gd:CeO_2$) has been decreased by a factor of 20-110. Lower CC can be also achievable (under investigation).

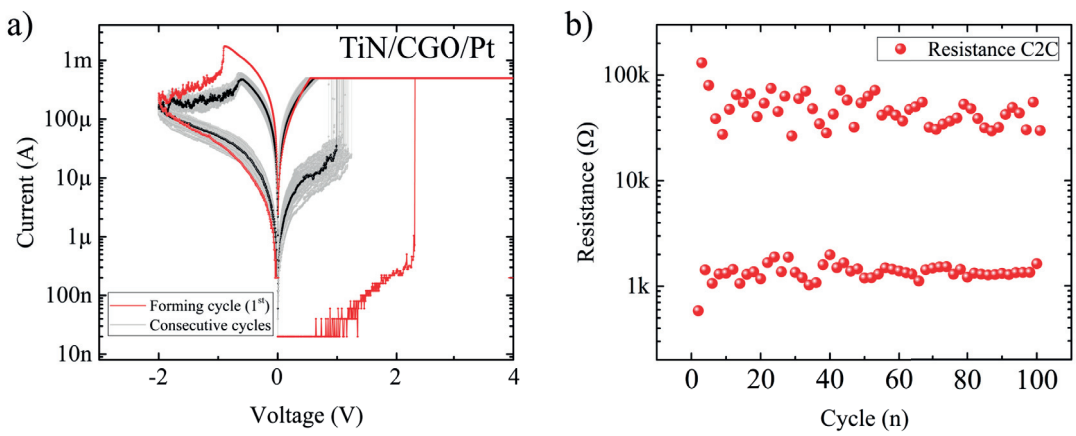


Figure 6.4 – DC measurement results of a) the forming and switching traces for 14 nm CGO in 5μm via size, and b) the resistance states-cycle uniformity extracted by measuring the HRS and LRS for 14 nm CGO at V_{read}=± 0.25V.

After the forming process, the gradual reset operation takes place and the median reset voltage reflected for 50 switching cycles is -0.596 with the variation between -0.616 V and -0.574 V. Subsequently, the calculated median set voltage is 1.053 V and it varies between 1 V and 1.1 V. It has to be noted that the set and rest voltages are corresponding

to the points that a current increase or drop has been recorded, while the applied voltage on the sample was always ± 2V. The cycle-to-cycle stability is represented by the DC endurance tests over 100 cycles (Fig. 6.4 (b)). The plot clearly demonstrates the cycle-to-cycle stability with the median HRS and LRS values of 40 $k\Omega$ and 1 $k\Omega$ respectively (V_{read}=± 0.25 V).

The first reset (marked in red) in Fig. 6.4 (a) shows an overshoot current. The overshoot current is explained by different groups. Switching layer properties (dielectric constant, band gap and...) [152], the device geometry, and the measurement setup [153] can influence the overshoot current. However, the overshoot is not totally inevitable because of the nature of forming operations. During the forming procedure, the vacancies are created by applying an electrical field. The current passing through the vacancies intensify the creation of more thermally-assisted vacancies due to the Joule heating and results in steep current flow. This abrupt current increase is very fast (in range of μs) compare to the DC voltage sweep speed and can not be recorded by the parameter analyzer. The overshoots current in the first reset in Fig.6.4 (a) is equal to the maximum current that the device reaches during the forming operation. Moreover, these devices are fabricated by considerably large TE and the common BE as shown in Fig. 6.1, which creates a series parasitic capacitance with ReRAM cells. After the fast transition from HRS to LRS in the forming step, the charges stored in the capacitance continues to discharge causes the overshoot current in the first reset operation.

To further investigate the switching mechanism in CGO thin films, the effect of active area has been studied (Fig.6.5 (a,b)). Independent from the device size, all cells were showing stable behaviour over multiple cycles. The interesting point is that while HRS does not change significantly (Fig.6.5 (a)) with the device size, the LRS tends to decrease (Fig.6.5 (b)) by increasing the area.

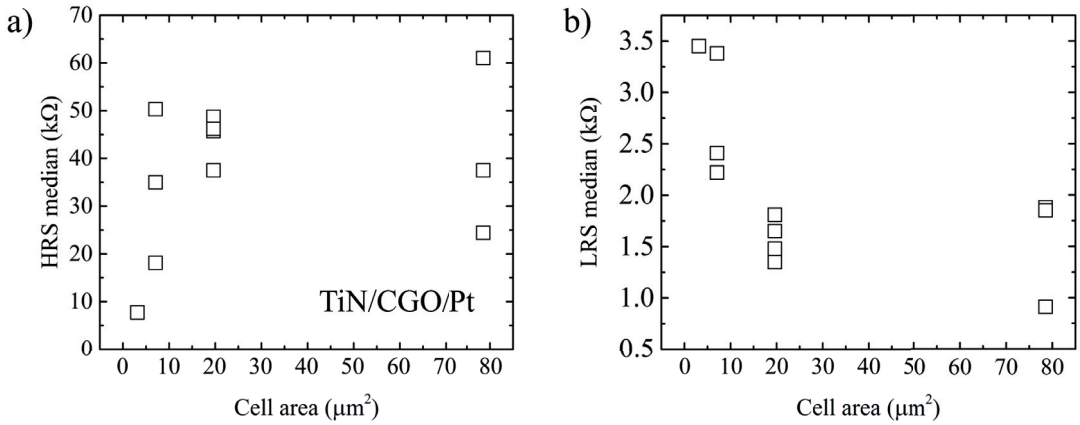


Figure 6.5 – a) the HRS change as a function of device size and b) The LRS change as a function of device size for 14 nm CGO at V_{read}=± 0.25V

The change of resistance by the device size is normally attributed to the interface type switching, however, one does not expect only LRS to decrease by the device size. Furthermore, the sharp change in resistance that has been observed in Fig. 6.4 is suggesting that the acting mechanism is rather filamentary switching. Thus, we shall explain the behaviour based on the multi-filaments switching. All filaments are expected to be broken in the reset step as the HRS does not change significantly with the device area. The simplified schematic view of acting mechanism can be drawn as Fig .6.6.

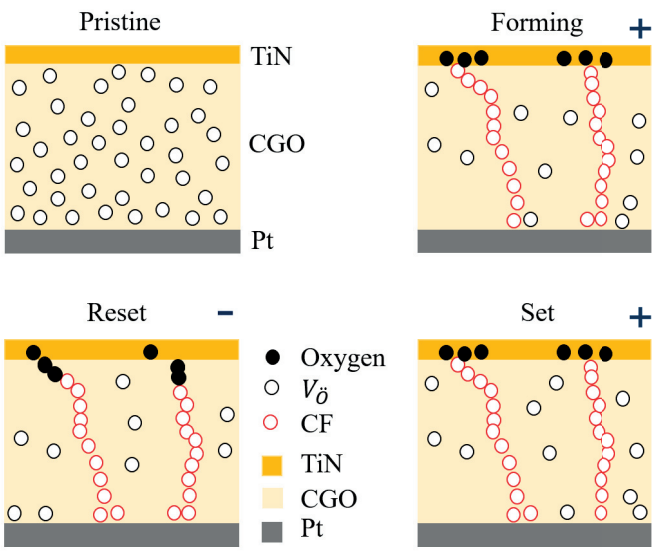


Figure 6.6 – Schematic view of possible mechanism for resistive switching in CGO thin films

At forming step, by applying positive voltage on TE, the oxygen ions move toward TiN electrode leaving oxygen vacancies behind. At high enough electric potential conductive filament(s) will form through the film and results in resistive switching from HRS and LRS. As was discussed earlier, due to the decrease of LRS by increasing the device size a multi-filaments switching is expected to take place. By applying reversed electrical potential, the oxygen ions move back to CGO films and consequently breaks the conductive filaments and recovers the HRS. The lowered electrical potential in set process compare to the forming voltage indicates that the conductive filaments are not completely destroyed at reset step. As the nature of the conductive filament is not clear, it can be either oxygen vacancies or Ce^{3+}, the conductive filament is shown in different color. Further material characterization is needed to clarify this. The storage of oxygen vacancies in TiN layer that can be explained by the oxidation of TiN shall be studied by TEM. Therefore, the presented mechanism is rather a speculation according to the electrical behaviour and the material properties.

The DC characteristics of CGO thin films allow us to perceive the existence of stable hysteric transactions between two different resistive states which confirms the qualified functionality of CGO switching layers for ReRAM devices. In order to examine the more reliable performance of our devices, an endurance tests were carried out under pulse measurements setup, illustrated in Fig. 6.7. Stable resistance switching has been obtained for >10^4 cycles. For each write/read procedure, the pre-reset, post-set and pre-set resistance values are measured. The stable HRS median value of 200 kΩ and LRS median value of 3kΩ have been recorded with the negative pulse voltage of -2.15 V and a positive pulse voltage of 1.5 V. The interesting point is the better recovery of HRS in AC pulse measurement as results of lower CC. By reducing the CC we have lowered the number of conductive filaments which has resulted in higher LRS and better recovery of HRS in reset step. Therefore, the ON/OFF ratio is almost doubled in AC measurement compare to DC.

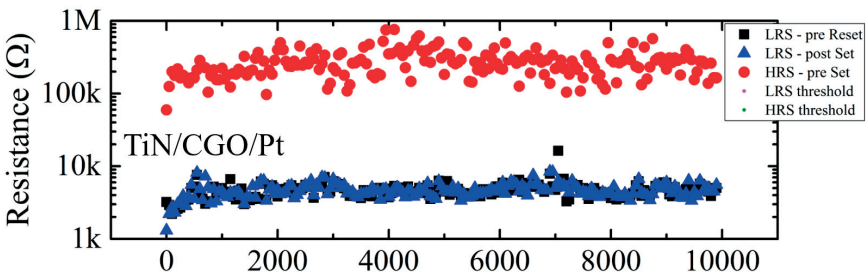


Figure 6.7 – The pulse data analysis of devices endurance over 10^4 cycles with the V_{gate}=1.969V (equal to CC= 150μA) and pulse width and slope of 50μs and 20% respectively

6.4 YSZ-Based ReRAMs

Fig. 6.8 (a,b) shows the I-V characteristics of 20 nm thick YSZ-based ReRAM and also its stability over multiple cycles. The forming voltage in comparison to CGO thin film is more than 2 times higher, 5.9 V. This can be due to the higher thickness of YSZ thin films but nevertheless if we also consider the applied electric field (2.9 MV/cm), CGO thin films are still showing lower values (1.5 MV/cm) at the same CC. On the other hand, if one compares the YSZ switching field to the hafnium oxide with the same compliance current (V_{for}=3.3 V for 5 nm thick hafnia layer), it can be seen that YSZ switches almost at half of the electric field. However, it is crucial to consider what would be the minimum thickness of YSZ that can exhibit a stable resistive switching. For CGO thin films, it is very challenging to obtain stable switching at thickness lower than 14 nm (presented in the previous section) thus one can consider the presented results as the optimal conditions. Although, in case of YSZ, it seems that we can further decrease the thickness since considerably stable results have been also obtained for 10 nm thick films in which the forming voltage dropped to <3 V. One might be able to further decrease the thickness by using Atomic Layer Deposition (ALD). While, the forming voltage has decreased dramatically with reducing the film thickness, the set/reset voltage was almost the same for both 20 nm and 10 nm samples. The device switched from LRS to HRS at the reset voltage of -0.6 V and the set transaction from HRS to LRS occurred at 1 V. Like CGO thin films the set and rest voltages are recorded as soon as a current increase or drop has been recorded, while the applied voltage on the device was ± 2V. The cycle-to-cycle resistance states readout is measured for 120 cycles at V_{read}=± 0.25V, showing the HRS of 80 kΩ and the LRS of 3 kΩ.

Unlike CGO-based devices, the LRS and HRS do not follow a trend with the device scaling, see Fig.6.8 (c,d). Normally, such behavior is attributed to localized filament formation independent from the device size. YSZ, similar to CGO-based devices has filamentary switching, however, with lower number of filaments. This can be explained by a lower number of mobile oxygen vacancies for formation of multi conductive filaments in YSZ thin films compare to CGO. Or, due to the higher thickness of YSZ than CGO, the provided forming energy cannot complete multi filaments. This has to be further investigated by lowering the YSZ thickness.

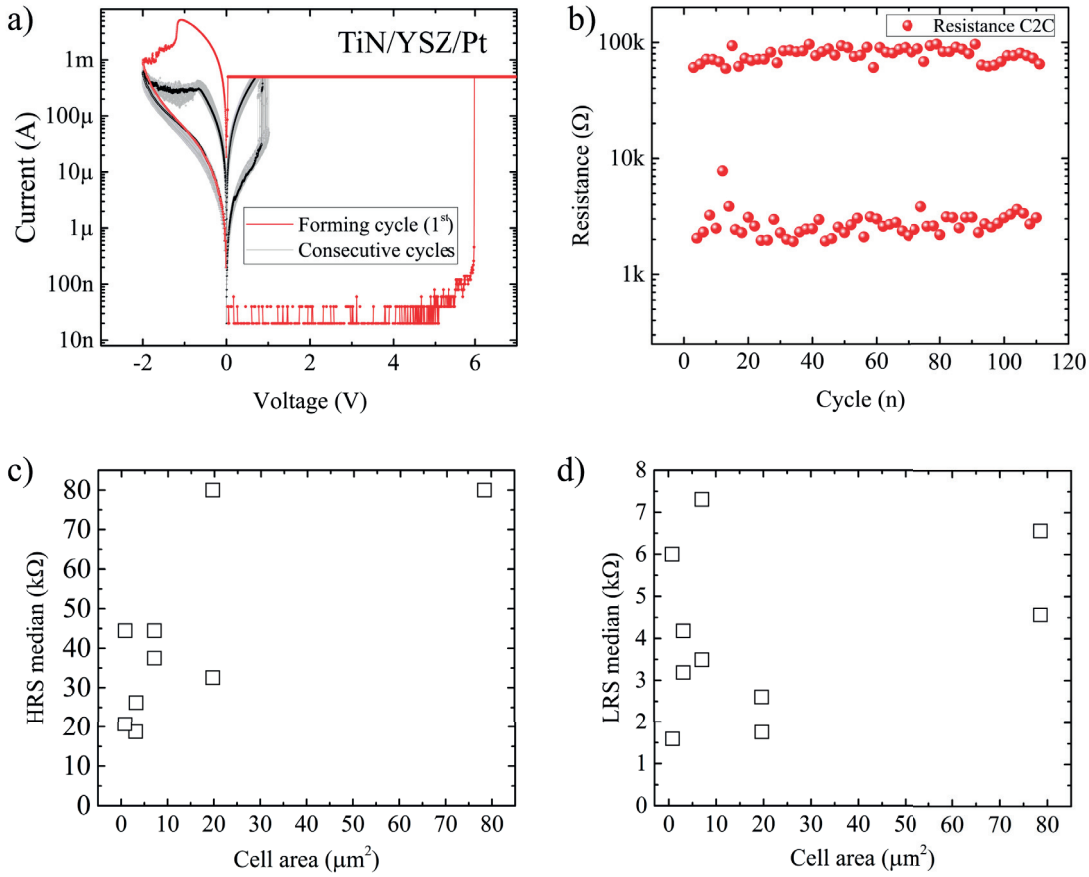


Figure 6.8 – DC measurement results of a) the forming and switching traces for 20nm YSZ of 5μm via size. b) the resistance states-cycle uniformity extracted by measuring the HRS and LRS for 20nm YSZ at V_{read}=± 0.25V. c) the HRS variation as a function of device size and d) The LRS variation as a function of device size.

The AC pulse measurement shows high switching endurance up to >10^4 of YSZ based devices (Fig. 6.9). However, it can be seen that the ON/OFF ratio decreases to 5. The median HRS value of 100kΩ and median LRS value of 20 kΩ are obtained with the reset pulse value of -1.75 V and the set pulse value of 1.5 V. The HRS is comparable to the DC measurements while the LRS is >6 times higher. Since in AC pulse measurement the compliance current is set to 150μA one can imagine that the created filament is not as strong as DC measurement which results in better HRS recovery and higher LRS. While the lower compliance current was helpful in CGO thin films, in case of YSZ it has lowered the ON/OFF ratio below the minimum requirement (>10 [105]). This also can be enhanced by lowering the YSZ thickness which is under study.

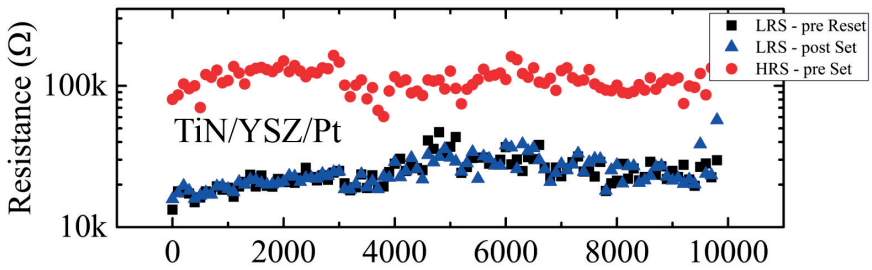


Figure 6.9 – The pulse data analysis of devices endurance over 10^4 cycles with the V_{gate}=1.969V (equal to CC= 150μA) and pulse width and slope of 50μs and 20% respectively

6.5 Electrical Forming Process

Scalability is one of the main advantages of resistive memory. However, it has been seen that the forming voltage increases by scaling the device size [154] [155]. This has been also observed in CGO and YSZ based devices, Fig.6.11. The forming change can be explained based on the defect population theory as the number of oxygen vacancies decreases with reducing the device size. Even though the forming voltage is not needed for the continuous device operation, the circuitry needs to provide this one time process at the beginning. Hence, for the circuit design, it is crucial to determine the forming voltage depending on the required memory sizes.

Chen et al [156] have proposed a first-order analytical model based on stochastic nature of forming to predict the scaling behavior of forming voltage. This model assumes that the ReRAM device is divided into small cubic cells with certain probability of transition into a conductive state. The forming happens when statistically there is a chain of cells with sufficient concentration of oxygen vacancies (weakest link) between TE and BE, see Fig. 6.10.

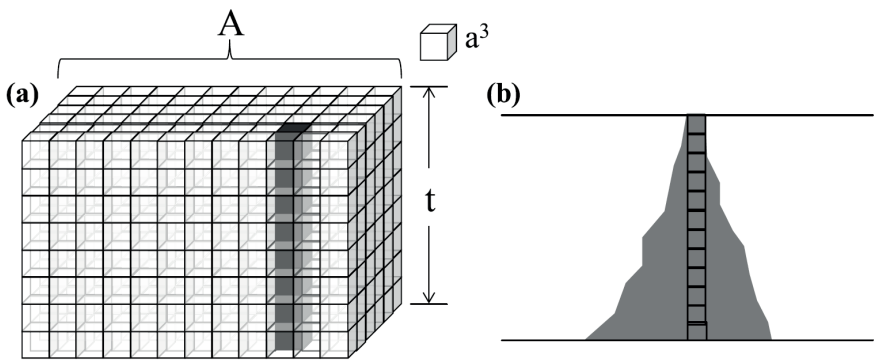


Figure 6.10 – a) The switching layer in ReRAM device is divided into small cubic cells with certain probability of transition into a conductive state, b) a vertical filament is shown which illustrates a conical filamend (shaded area) with the "weakest-link" chain of cells that determines the forming probability [156].

While the model is basically reported for single filament switching, it can be applicable for multi-filament formation since the only change between multi and single filament forming is the number of segments that are involved in the forming operation. The simplified model formula can be presented as Eq. 6.1-6.3 where α and β are reflecting the geometry and physical characteristics of the oxide layer [156].

$$V_f = \alpha + \beta ln(\frac{A}{a^2}) \tag{6.1}$$

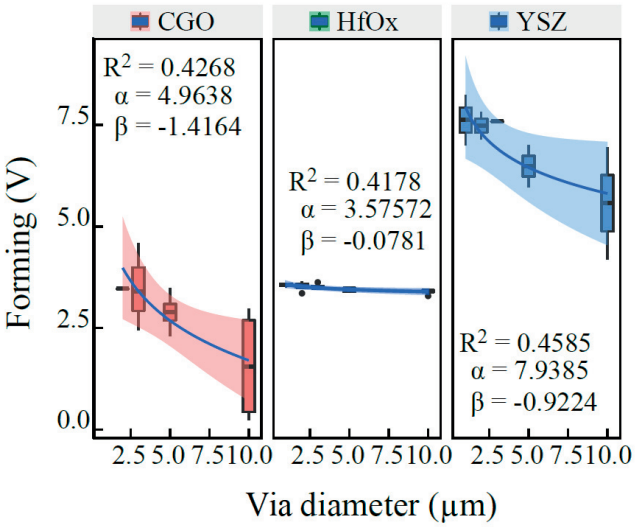


Figure 6.11 – Forming voltage versus via diameter for CGO (14nm), HfO_2 (5nm) and YSZ (20 nm) ReRAM.

where

$$\alpha = (\frac{a}{k})ln(-ln(1-P_f)) + (\frac{t}{k})ln(\frac{1}{r_0}) \tag{6.2}$$

$$\beta = -\frac{a}{k} \tag{6.3}$$

in which (A) is the device active area, (a) is the segment (cubic) dimension, (k) is Boltzmann constant, (P_f) is forming probability, (t) is the oxide thickness, and (r_0) is the transition rate ($r=r_0 e^{\frac{kV_f}{t}}$) constant. As it can be seen from Fig. 6.11 the model can predict the area dependency of both CGO and YSZ forming voltage. R^2 represents the determination coefficient of the fitting line (in blue) and the colored zone explains the 95% confidence interval of this model. In comparison to HfO_2, the forming voltage in CGO and YSZ thin films are showing strong device size dependency. In case of CGO, due to lower forming voltage even though the forming voltage is scaling with device size, the final value is still comparable to high performance switching layer such as hafnium oxide. In case of YSZ thin films, further studies are carrying on for a more precise conclusion.

6.6 Summary

We have studied the potential of well-known fast ion conducting thin films, i.e. CGO and YSZ, in resistive switching memories. It turned out that both structures can perform at relatively low electric potentials comparable to well-studied transition metal oxides such as HfO_2. CGO thin films are able to switch between HRS and LRS with V_{set} = 1.053 and V_{reset}= -0.596 with high stability over multiple cycles. The study of HRS and LRS as a function of device size suggest that CGO thin films are very likely exhibiting multi-filaments switching as the LRS decreases with device size (not linearly) while the HRS does not change significantly. The nature of conductive filament needs further investigations to be defined. Either Ce^{3+} or oxygen vacancies can make the conduction path. The traces of multi-filament switching has been also seen in the change of forming voltage with the active area. The cells were showing stable switching for more than 10^4 cycles. The resistance window (ON/OFF ratio) was determined as 100 which totally fulfils the technological implementation requirements. YSZ thin films have also shown interesting characteristics, V_{set} = 1.1V, V_{reset}= 0.6V and 10^4, however, the comparison of CGO and YSZ thin films revealed that the number of conductive filament in YSZ is probably less than CGO as the LRS and HRS voltage does not change significantly

with the device size. The comparison of the electrical characteristics of YSZ and CGO thin films to HfO_2 using the same device fabrication process (except the film deposition) shows the high potential of fast ion conducting thin films to be used as switching layer in ReRAMs.

Part III

Novel Properties in Gadolinium Doped Ceria (CGO)

7 Giant Electrostriction (GES) in CGO: Principle and Status

7.1 Electrostriction

Electromechanical thin films have historically evoked great attention because of their potential in different applications, especially in Micro Electro-Mechanical Systems (MEMS) [157]. The goal of development is to achieve high precision and speed, large forces and low fatigue rate [158]. Piezoelectricity is a better-known linear coupling mechanism which is valid only for non-centrosymmetric materials, however, the basic electromechanical coupling that exists in all dielectric materials is electrostriction. Electrostriction is the quadratic relation between the developed strain and the applied electric field in an insulating material [158]. In general, strain (x) caused by the electromechanical response of materials can be expressed as:

$$x_{ij} = d_{ijm}E_m + M_{ijmn}E_mE_n + ... \tag{7.1}$$

which is proportional to first, second or higher order of applied electric field (E). The linear effect, as mentioned, is associated with piezoelectric coefficient d_{ijm}, and the quadratic nonlinear effect to electrostriction coefficient, M_{ijmn}. Electrostriction thus can be defined as ($x_{ij} = M_{ijmn}E_mE_n$) [159]. In the case of stress measurement with taking the elastic modulus (c_{klij} is elastic tensor) into the account the coupling can be written as:

$$\sigma_{kl} = c_{klij}M_{ijmn}E_mE_n \tag{7.2}$$

While most electrostrictive materials are perovskite ceramics, there has been always an

interest to study electrostriction in other families of materials like polymers, polyvinylindene fluoride (PVDF) [158]. Recently, an unexpectedly large electrostrictive response have been observed in fluorite oxide structures, like CGO or (Y,Nb)-stabilized δ-Bi_2O_3 [19] [160]. According to the theoretical understanding which is almost confirmed by studies of Newnham and co-workers [161, 158] the electrostriction should be more or less proportional to the product of compliance and dielectric constant, Fig. 7.1. Thus, ordinary CGO with dielectric constant of ≤ 30 [162] is expected to show 2×10^{-20} m^2/V^2 as electrostrictive coefficient which is 3000 times less than reported values, 6.5×10^{-17} m^2/V^2 [19].

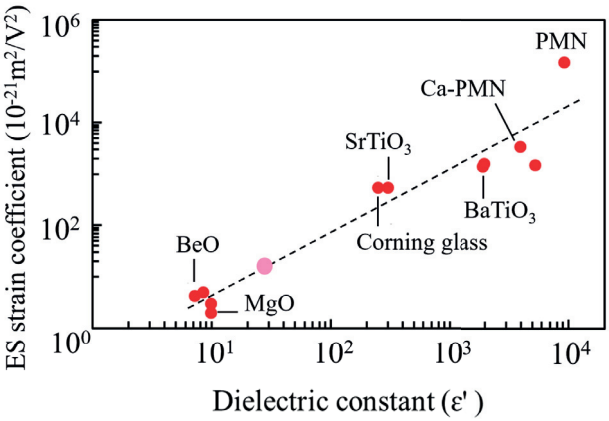


Figure 7.1 – Electrostrictive strain coefficient (M) (m^2/V^2) versus dielectric constant for the materials reported in ref [161, 158].

The size, and also the fact that a compressive stress is generated in the plane of the film – in contrast to the piezoelectric effect in thin films that produces a tensile stress at equal geometry – makes this finding extremely interesting for actuators in micro electro-mechanical systems (MEMS). Since in addition, it is a lead-free material and thus could replace PZT fro micro-actuators.

7.2 Proposed Mechanism

The principle of electrostriction in CGO thin films is explained based on the position of oxygen vacancies after doping ceria with lower valance dopant. The crystal structure of CGO consists of simple cubic oxygen lattice, where cerium or gadolinium ions occupy alternate body centers, Fig. 7.2. The substitution of 20% Ce^{4+} with Gd^{3+} produces 5% vacant oxygen sites in order to maintain the charge neutrality. In other words, for every two Gd^{3+} there is a corresponding creation of one oxygen vacancy $V_{\ddot{O}}$.

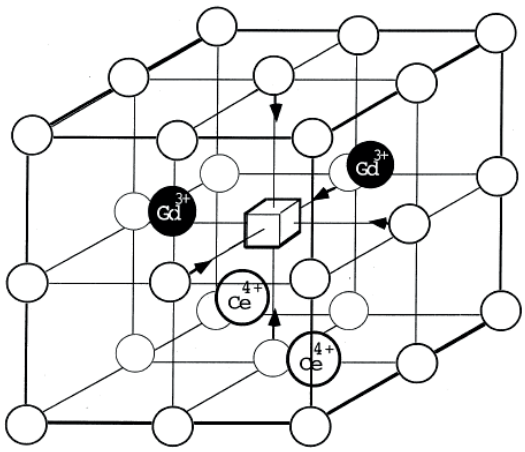


Figure 7.2 – Lattice view of Gd-Doped Ceria crystal structure [163]

On the basis of EXAFS (Extended X-ray absorption fine structure spectroscopy), $V_{\ddot{O}}$ prefers Ce^{4+} than Gd^{3+}. Therefore, the mean distance of Ce-$V_{\ddot{O}}$ increases while Ce-O decreases [164]. Under application of an electric field parallel to the Ce-$V_{\ddot{O}}$ direction Ce^{4+} ion tends to travel towards oxygen vacancy, rendering Ce-$V_{\ddot{O}}$ distance to contract and expansion in the perpendicular plane. A generated compressive stress of -10 MPa at an electric field of 78 kV/cm, Fig. 7.3 [19], or a stress coefficient of 1.7×10^{-7} N/V^2 had been reported. The measurements have been carried out using Cr/$Ce_{0.8}Gd_{0.2}O_{1.9}$ /Cr (100/450/100 nm) cantilever-based structures. The same authors have reported even higher values, in the range of 500 MPa.

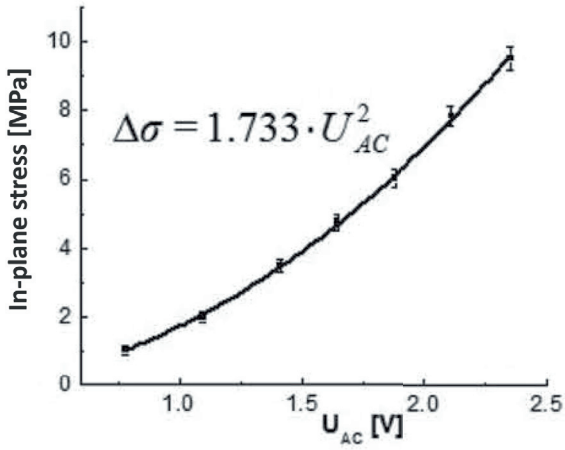


Figure 7.3 – Amplitude of the in-plane stress as a function AC voltage at 10 mHz when DC voltage was switched off [19]

The effect of dopant concentrations (Gd) (10 to 33%) has been also studied [165]. It was seen that pure ceria with only 2% oxygen vacancy can show relatively large electrostriction. By reducing $V_{\ddot{O}}$ concentration to 0.5% the effect was dropped by a factor of 3. In 10% Gd doped films the generated stress was 180 MPa (no graphs reported), while by increasing the dopant concentration (= increasing $V_{\ddot{O}}$ concentration) to 20% the stress decreased to 100 MPa. With further increasing Gd to 33% the generated stress was again increased to 170 MPa but it was still lower than 10% doped structures. Table 7.1 shows the electrostriction performance of mentioned films [165]. This is suggesting that the giant electrostriction is not directly related to the $V_{\ddot{O}}$ introduced by dopant, but rather due to the additional oxygen vacancies that are compensated by Ce^{+3}. This has been confirmed by our studies presented in following chapter [149].

Table 7.1 – Electrostriction performance of 300–500nm thick films of $Ce_{1-x}Gd_xO_{2-x}$ and $CeO_{2-\delta}$. $\%V_O$ is the oxygen vacancy concentration, σ is the measured electrostrictive stress with electric field E≈60 kV/cm. $\gamma=\sigma/E^2$ (kPa/(kV/cm)^2) is the experimental electrostriction stress-field coefficient. Equivalent in-plane strain, $u_{xx}=\sigma\times(1-\nu)$. $M=u_{xx}/E^2$ and $Q=M/[\epsilon_0(\epsilon-1)]^2$ electrostriction coefficients were calculated for the dielectric constant ϵ=28, unrelaxed elastic modulus Y=210±15 GPa, and Poisson ratio ν=0.28 [165].

	$V_{\ddot{O}}$ %	σ (MPa)	γ	$u_{xx}\times10^{-4}$	M ($10^{-4}\times m^2/V^2$)	Q (m^4/V^4)
$CeO_{1.99\pm1}$	0.5	25±2	7±1	0.8±0.08	2.2±0.21	39±3.7
$CeO_{1.96\pm1}$	2	65±3	18±2	2±0.1	5.8±0.4	102±7
$Ce_{0.9}Gd_{0.1}O_{1.95}$	2.5	180±7	50±4	5.8±0.4	16±1	282±17
$Ce_{0.8}Gd_{0.2}O_{1.90}$	5	101±4	28±1	3.2±0.2	9±0.6	157±10
$Ce_{0.67}Gd_{0.33}O_{1.85}$	8.25	173±5	48±1	5.6±0.3	15.5±0.9	271±15

In the same report, the structural changes associated with electric field have been investigated using *in situ* differential X-ray absorption spectroscopy. It has been stated that the stress generated by application of an electric field can be related to the response of a small population of strongly anharmonic chemical bonds, Fig. 7.4. By applying an electric field, the length of contracted Ce-O bonds (2.22 ±0.09 $\dot{A}$) in distorted complex increases and reached the average value (2.33 ±0.02 $\dot{A}$). With removing the electric field the structure returns to distorted configuration [165].

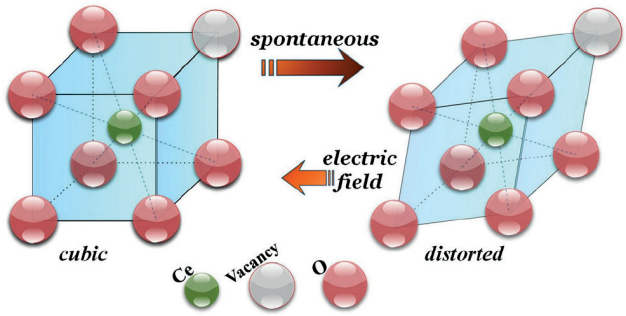


Figure 7.4 – Scheme of the electric field induced reorganization of a distorted Ce near neighbor coordination shell containing an oxygen vacancy [165]

7.3 Effect of Frequency and Temperature

Lately, Ushakov et al [166] have studied the frequency and temperature effects on electromechanical properties of CGO thin films. The work was published after our paper [149] about the frequency dependence of giant ES response. They have fabricated CGO (1.4 μm) liberated round membranes and studied voltage induced displacements using sensitive laser interferometry. The frequency and voltage dependencies of membrane displacement are demonstrated in Fig. 7.5.

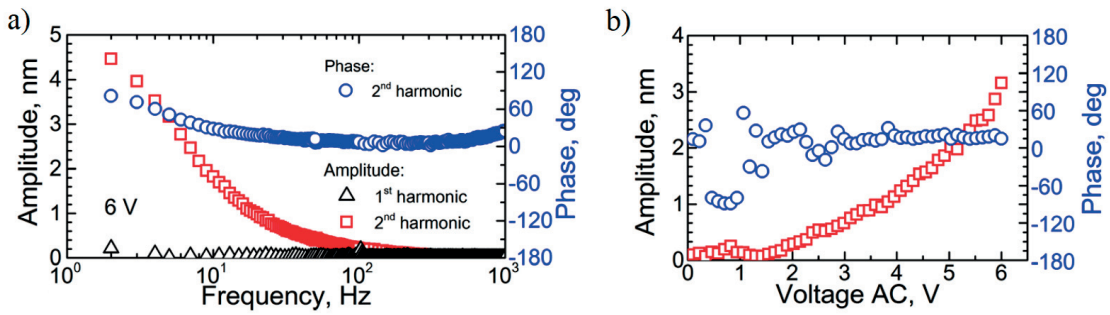


Figure 7.5 – a) Frequency (applied voltage: 6 V), and b) voltage dependency (frequency:5 Hz) of the electromechanical response at the 2nd harmonic of the CGO membrane [166]

As was expected the second harmonic gives the strongest response which is typical for electrostrictive materials. The noticeable 1st harmonic response was dedicated to the internal bias which was claimed that is due to different quantities of bottom and top electrode. The highest response was obtained at 2 Hz which dramatically decreased by going to 1kHz, in agreement to our earlier report [149]. The phase difference was recored as 60° at 2 Hz which had decreased to 0 by increasing the frequency to some hundred Hz, Fig. 7.5 (a). The voltage dependency presented in Fig. 7.5 (b) shows that

the second harmonic amplitude is proportional to square of applied voltage which has been considered as confirmation for electrostrictive response.

They have studied the CGO electromechanical behaviour upon application of rectangular pulse, Fig. 7.6 (a) in order to explain the origin of frequency dependency. A clear time delay in scale of 100 ms between application of electric field and mechanical response has been reported. After the voltage cut the sample was relaxed to initial position with time constant of about 20 ms. The relaxation time was not dependent on the sample temperature, indicating a non-activated process. Therefore, the effect was associated to Joule heating [166]. This can also justify the 60° phase shift.

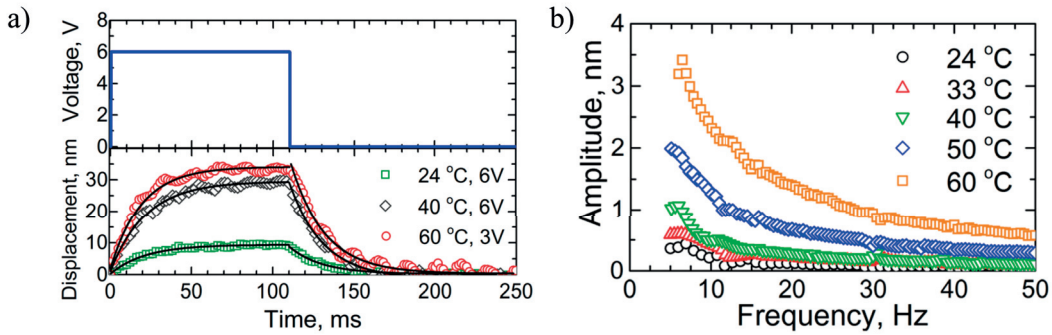


Figure 7.6 – a) Electromechanical response of CGO thin films under rectangular electric pulse, b)Electromechanical response at second harmonic versus frequency at different temperatures, E= 14 kV/cm [166]

Furthermore, it has been seen that GES is highly dependent on the substrate temperature, Fig. 7.6 (b). The amplitude of the response was increased by factor of 6 by increasing temperature to 60°C. This was explained due to the existence of a Schottky barrier that its resistance decreases by increasing the temperature. The presence of the Schottky barrier was confirmed by impedance spectroscopy [166]. The positive impact of lowering the Schottky barrier on GES is suggesting that the conductivity mechanism might also contribute in electromechanical response of CGO thin films. Even though enough evidences have been seen for the contribution of Joule heating, the authors have assumed that the response is fully electrostrictive. Based on finite element simulation, the electrostrictive response was calculated as $5\times10^{-18}\ m^2/V^2$ which is comparable to previously published results [19].

8 Electrochemical and Dielectric Properties in CGO Thin Films

The GES was explained by dynamic response of oxygen vacancies to an external electric field. Verifying this hypothesis is somehow challenging and one has to study the defect density and more particularly the content of oxygen vacancies on the final response. Moreover, it has to be noted that the electrostrictive coefficient in thin films cannot be directly compared to the ones of bulk materials as the films are part of a layered composite structure. In this chapter, the electrostrictive coefficient in thin films configuration is explained both in clamped and free body case. Moreover, the effect of microstructure, processing conditions, as well as excitation frequency is studied to elucidate the origin of the GES. The results and discussion are partially taken from our published paper in Acta Materialia 118(2016) 1-7 and reproduced with kind permission of Elsevier. Another paper is in preparation and will be submitted soon.

8.1 Electrostriction Coefficients in Thin Films

In general, all materials undergo a change in dimensions when they are subjected to an electric field. In non-piezoelectric materials this is due to the electrostrictive effect generating a strain that is proportional to the square of electric field [167]. The electrostrictive coefficients in bulk materials are usually derived for two special situations. Either the body is free to elongate or shrink in all directions at zero stresses (constant stress (T) condition), or the body is kept at zero strain in all directions (constant strain (S) condition). However, thin films are part of a composite structure with the substrate, meaning that the film is clamped in the plane to the substrate (strain S_1 and S_2 must be continuous across the interface), but free to move out of plane (T_3=0). This leads to the definition of coefficients at mixed border conditions: constant strain in the plane, and constant stress out of plane, as in the case of piezoelectric thin films [168]. The searched thin film coefficient is obtained from the constitutive equations (equations 8.1-8.3) by

setting T_3=0, and S_1=S_2=0:

$$S_1 = s_{11}T_1 + s_{12}T_2 + M_{31}^{(T)}E_3^2 = 0 \tag{8.1}$$

$$S_2 = s_{12}T_1 + s_{11}T_2 + M_{31}^{(T)}E_3^2 = 0 \tag{8.2}$$

$$=> T_1 + T_2 = -\frac{2M_{31}^{(T)}E_3^2}{s_{11} + s_{12}} \tag{8.3}$$

The coefficients s_{ik} denote the components of the elastic compliance tensor, $M_{31}^{(T)}$ the electrostriction coefficient at constant stress, following the same notation as for the piezoelectric tensors (first index refers to electric field, and the second index represents the strain component represented in the reduced index notation). Since the film is isotropic in the plane, the two stress components must be equal in magnitude. This leads to the definition of an effective, electrostrictive thin film coefficient, as shown in equation 8.4 ((S) and (T) stand for constant strain, and stress, respectively):

$$T_1 = -\frac{M_{31}^{(T)}}{s_{11} + s_{12}}E_3^2 = -M_{31,f}^{(S)}E_3^2 \tag{8.4}$$

where T_1 is the in-plane stress, and E_3 the electrical field perpendicular to the plane of the film. $M_{31,f}^{(S)}$ is a practical coefficient that is directly measured in beam bending experiments. In order to compare this coefficient with the standard strain coefficient $M_{31}^{(T)}$, one needs to know elastic properties, i.e s_{11}+s_{12}. In cubic or isotropic materials, the latter are expressed in terms of Young's modulus Y and the Poisson's ratio ν , giving the relation as shown in equation 8.5:

$$M_{31}^{(T)} = (s_{11} + s_{12})M_{31,f}^{(S)} = M_{31,f}^{(S)}\frac{(1-\nu)}{Y} \tag{8.5}$$

The M_{31} coefficients were found to be positive [19]. The effect thus produces compressive stress in the clamped case, and a positive strain in the free body case.

8.2 Experimental Methods

8.2.1 Thin Film Synthesis and Sample Fabrication

$Ce_{0.8}Gd_{0.2}O_{2-x}$ thin films were grown by RF magnetron sputtering (Nordiko Sys. section 3.1.1) on polycrystalline metal electrodes of Pt, Al, and Cr. Passivated silicon wafers served as substrates. All electrodes were deposited at 320 °C. CGO was deposited after a vacuum break. Details of the CGO process are given in table 8.1. The electromechanical properties were assessed by beam deflection techniques. The beams had full wafer thickness (525 μm) and were obtained by dicing. The dicing marks were formed together with the top electrodes by sputter deposition of Pt/Cr through a shadow mask (Fig. 8.1).

Table 8.1 – Sputter process conditions for CGO thin film deposition

Target (100 mm dia)	$Ce_{0.8}Gd_{0.2}O_{1.9}$
Base pressure	$< 5 \times 10^{-4}$ mTorr
Sputter pressure (Ar)	10-20 mTorr
Growth temperature	RT - 400 °C (HT)
Ar gas flow	15 sccm
RF magnetron power	200 W
Film thickness	2 μm ($\pm$ 10%)

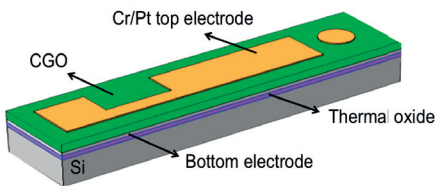


Figure 8.1 – Sample structure for electromechanical characterization of the CGO thin films. The beams had dimensions of 15.0×1.50×0.38 mm and were clamped across the narrow part of the top electrode (left side). The dot on the right hand side serves to reflect the light of the proximity sensor of the electromechanical measurement setup.

8.2.2 Structural Characterization

The texture of the films was determined by Bruker D8 advanced X-ray diffractometer. The Al and Pt electrodes had (111) texture as is expected for FCC sputtered metals, while Cr electrodes texture had (110) texture, also, expected for a BCC metal. The film microstructure was investigated in cross-section by using a FEI Tecnai Osiris Transmission Electron Microscope (TEM) at 200 kV. A chemical mapping by EDX (energy-dispersive

X-ray spectroscopy) measurement was done. Chemical composition was measured using Merlin scanning electron microscopy (SEM) at 3 kV.

8.2.3 Electromechanical Measurement Setup

The cantilever beams were mounted on X-Y-Z stage controlled by micro screw drives. The top and bottom electrodes were accessed via micromanipulators. The films had been subjected to sinusoidal bipolar excitation (zero DC offset). The displacement at the tip was tracked using a MTI 2000 "fotonic" sensor (see Fig. 8.2). From the cantilever deflection, the curvature and thus the film stress is derived. Division by the square of the electric field yields the effective stress ES coefficient $M_{31,f}^{(S)}$. If not stated differently, the values given in this paper correspond to a the maximal effect obtained with a sweeping frequency of 66 Hz. A detailed description of our setup and procedure (derivation of large-signal response) was published by Mazzalai et al [169]. This method is a standard one for evaluating converse piezoelectric coefficients in piezoelectric thin films method.

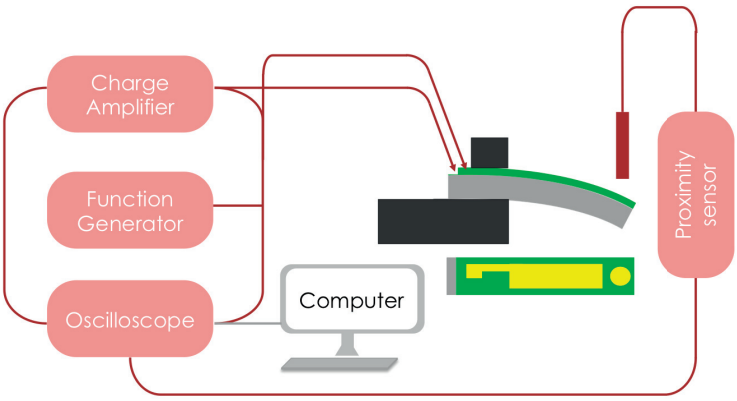


Figure 8.2 – Schematic of the cantilever-tip displacement measurement setup, used for electrostrictive characterization (after [169]).

8.2.4 Nanoindentation

In order to derive $M_{31}^{(T)}$, the elastic modulus (Y) is needed. We determined it by means of nanoindentation. Elastic properties can also be indicative of the oxygen vacancy concentration, as in flourite-structured oxide materials the elastic modulus decreases with increasing concentration of oxygen vacancies [170, 171, 150]. A Nano Indenter XP^{TM} (MTS Nano Instruments) with a three-sided diamond Berkovich indenter was used for the nanoindentation experiments. The compliance of the set-ups as well as tip shape was calibrated using fused silica standard [172]. A linear loading and unloading profile with peak load of 25mN and dwell duration of 20s was applied. The loading and

unloading durations were 20s each. The thermal drift was measured at 10 % of peak load value during unloading for 60 s. 20 indents were performed for each sample. The maximum displacement depths were less than 10% of film thickness in order to avoid elastic substrate effects from affecting the measured modulus values [173]. The elastic modulus was calculated using the method proposed by Oliver and Pharr [172]. The Poisson ratio needed for the calculation was taken as 0.334 as found in the literature for ceramic electrolyte layers of CGO 80/20 [151]. The same work published a modulus Y=187 GPa, which is close to the values obtained in this work. As no single crystal compliance tensors are measured so far for CGO 80/20, we could not calculate modulus values for a specific thin film texture. In the same work, a modulus decrease of 6.5 % was obtained when increasing the Gd content from 10 to 20 %, thus increasing the $V_{\ddot{O}}$ concentration by 2.5 %. Very similar values were derived from density functional theory for pure ceria, i.e. 8 % decrease for a 3% vacancy concentration [150]. In this case the vacancies are apparently compensated by electrons, which are most likely trapped by Ce^{4+} ions, thus becoming negative Ce^{3+} point defects. The existence of these were shown by electron paramagentic resonance in earlier works on reduced CGO[174].

8.2.5 Dielectric Spectroscopy

The dielectric properties at very low frequencies were measured by a lock-in technique [175]. The charge response to an AC signal of 500 mV amplitude was captured by a charge-amplifier (Kistler 5011B), whose output signal was treated in a lock-in signal analyzer (Stanford Research SR 830). The same tool served also as the source of the AC signal. At higher frequencies (>10 kHz) the dielectric measurements were made by an impedance analyzer (HP 4294 A). The complete spectral range covered frequencies from 10^{-1} to 10^{+6} Hz.

For assessing the temperature dependence of the dielectric properties, the samples were mounted in a mini furnace, and contacted with platinum probes. The temperature was controlled by a thermocouple and ramped up at a heating rate of 4°C/min from 1 to 150°C. The temperature dependence of the dielectric properties were measured for five frequencies, from 20 to 1000 Hz.

8.2.6 Electrical Characterization

Capacitance vs. voltage (C-V) curves were measured with the aixACCT TF 2000 analyzer applying a small signal amplitude of 1 V amplitude at 500 Hz. For measuring the current-voltage (I-V) response, the samples were mounted on a PA 200 probe station, and assessed by an Agilent B1500A analyzer.

8.2.7 Raman Spectroscopy

The defects in CGO thin films were investigated by micro Raman analysis using Thermo Nicolet Nexus 470 FTIR with excitation wavelength of 532 nm. The samples were prepared by focusing the laser on small chips using 65μm spot size and 1% laser power. For data quantification all peaks were fitted with Lorentzian peak function.

8.3 Results and Discussion

8.3.1 Microstructure Effect

According to the mechanism described by Korobko et al [19], a (111) film texture is important for obtaining maximum electrostriction effect. Fluorite thin films grow in fact most naturally with this texture, as known from most FCC structures, as a result of nucleating the densest plane parallel to the surface. This is also valid for the iso-structural YSZ thin films, at which deviation from this rule, i.e. growth of (200)-oriented grains, could be attributed to strong ion bombardment during sputter deposition [176]. Within our experimental matrix, we found that high temperature (HT) grown films on Pt showed more prominent (111) texture than those grown at RT (Fig. 8.3 (a)). Nevertheless, as shown in Fig. 8.3(b), RT films show a much stronger effect. The origin of such behavior must lie in the different microstructure, and particularly the higher defect density of low temperature processed films. As oxygen vacancies were proposed to play an essential role in the giant ES effect [19], the formation of additional oxygen vacancies during RT deposition is a likely mechanism. In order to verify this, we performed simultaneous SEM-EDAX measurements of the RT deposited film, and at a piece of the same sample subjected to a post-anneal in oxygen (T=600 °C for 15 minutes), Table 8.2. It was found that the former had 1.5±0.5 % less oxygen content. In agreement to EDAX, nanoindentaion results show elastic modulus of 205 GPa and 185 GPa for HT and RT prepared films on Pt(111), respectively. This variation in principle can be attributed to higher oxygen vacancy content in RT films. This 10 % decrease would be compatible with an increase of oxygen vacancies of 3 to 4 %. The lower measured value with SEM-EDAX is probably caused by an insufficient re-oxidation of the post-annealed sample. It appears that the processing conditions have to be manipulated in a way to increase the concentration of oxygen vacancies - or eventually of another unknown defect forming at the same time and promoting as well the giant ES effect.

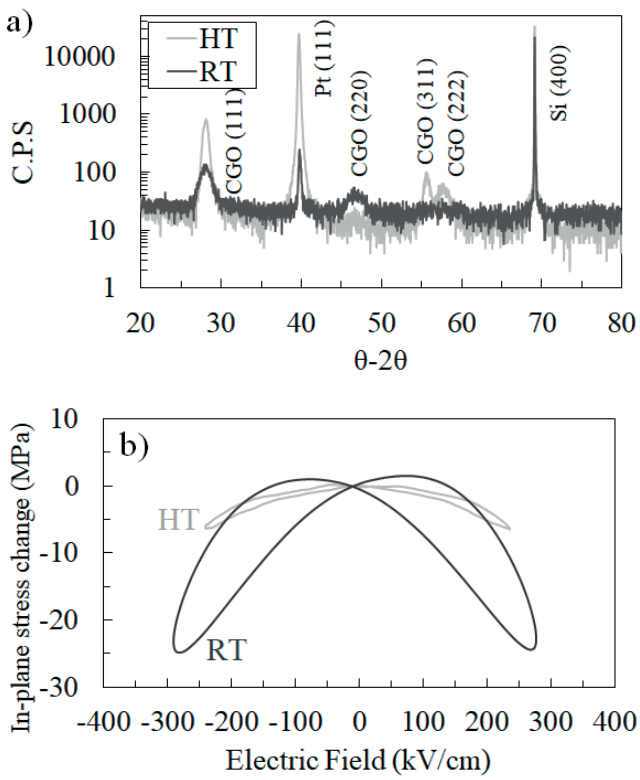


Figure 8.3 – a) XRD pattern, and b) Generated electrostrictive in-plane stress change as a function of the applied electric field swept at 66 Hz of a high (HT) and a room (RT) temperature deposited CGO thin film grown at 15 mT Ar pressure on Pt (111) bottom electrodes.

Table 8.2 – Normalized atomic concentration of Cerium (Ce), Gadolinium (Gd), and oxygen (O) for films grown on Pt bottom electrode for as-deposited and annealed (in oxygen at 600 °C for 15 min) samples.

Sample	Ce	Gd	O
Pt (RT)	20.8±0.3	6.1±0.3	73.1±0.3
Pt(RT)+Annealing	20.2±0.3	5.6±0.3	74.2±0.3

Three different bottom electrodes, namely Pt, Al, and Cr, were used to investigate their influence on CGO electrostriction response. The electrodes were exposed to air prior to CGO deposition, resulting in thin oxide layer formation on Al and Cr electrodes. The STEM-EDAX line scans shown in Fig. 8.4 show evidence of the oxide scales of Al and Cr at their interfaces, as the oxygen atoms extends into these electrodes.

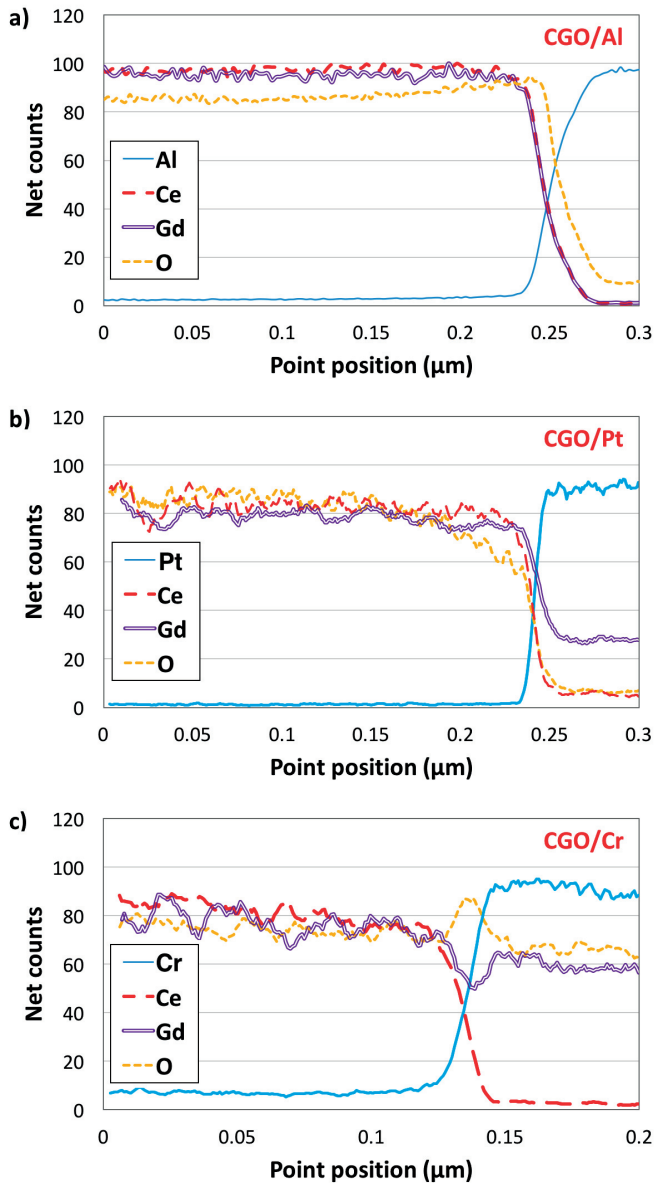


Figure 8.4 – Line scans at the interface film-electrode obtained from STEM-EDAX Hypermaps for CGO films grown on Al (a) Pt (b) and Cr (c) bottom electrodes deposited at room temperature. The Gd signal inside the Pt-electrode (b) and, the Gd and O signals inside Cr-electrode (c) are due to peak overlapping with the respective elements.

The growth mechanism of CGO on Pt electrodes is expected to be quite different in comparison to the one on Al and Cr electrodes. Fig. 8.5 compares CGO films grown on the mentioned electrodes. Cross-section TEM dark field images, Fig. 8.5 (a-c), demonstrate that films grown on Al and Cr bottom electrodes have a columnar structure with fiber shaped grains, whereas in case of Pt, the grains are larger and also show large grains

overgrowing smaller (111)-oriented ones at the interface (as evidenced by high resolution TEM images, not shown here). The ring-shaped diffraction patterns Fig. 8.5 (d-f) confirm the polycrystalline nature. The film on Pt electrodes exhibits a more "spotty" pattern (Fig. 8.5 (b)), which confirms the presence of larger crystals. In case of Al and Cr bottom electrodes, the SAED patterns (Fig. 8.5 (a,c)) with arcs are indicating better preferentially oriented films. Furthermore, the films grown on Al bottom electrodes are showing arcs with greater intensity, confirming that this film is having a better (111) texture, as already observed by X-ray diffraction. From this technique, (111)-texture indexes of 78%, 75%, and 56% were derived for Al, Cr, and Pt electrodes, respectively. The surprising point is the stronger (111) texture on Cr (110) than on Pt (111). This could be due to the oxide layer on Cr that prevents epitaxial attachment to the metal surface.

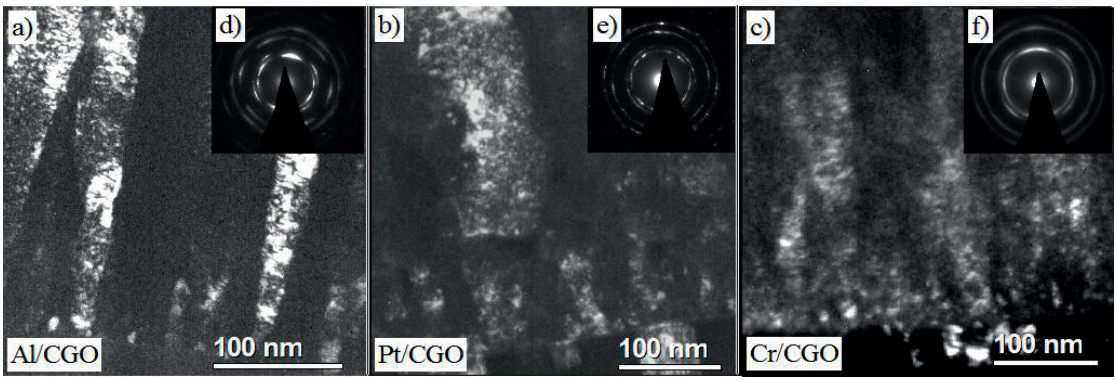


Figure 8.5 – Dark field TEM images for the CGO thin films grown on Al, Pt and Cr bottom electrodes, which are sorted from left to right respectively.

Fig. 8.6 shows the in-plane stress change generated in CGO films for the different electrodes. The highest $M^{(S)}_{31,f}$ coefficient was found in films grown on Al bottom electrode where we have the best (111) texture and narrower, fiber type grains. With an identical process we have obtained electrostriction stress coefficient of 1.4×10^{-07} (N/V^2) on Al, as compared to 3.3×10^{-08} (N/V^2), and 3.7×10^{-08} (N/V^2) for Pt and, Cr bottom electrodes, respectively. These results clearly demonstrate the effect of microstructure on the ES response. ES strain and stress coefficients, (111)-texture indexes, and elastic moduli of films mentioned in this report are listed in Table 8.3. CGO films with Al bottom electrode are showing a roughly 10 % lower young modulus, as compared to high temperature grown films on Pt electrodes, and even considering the measurement error, a lowering of 5 % remains as significant value. Meanwhile, one can also consider the porosity as reason of elastic modulus change [177], which is definitely not the case here as can be seen in the STEM-HAADF (high angle annular dark field) image of Fig. 8.7, showing a dense microstructure. Pores would appear as dark regions or dark spots in the HAADF image.

A 5 to 10 % reduction in elastic modulus corresponds to an oxygen vacancy concentration of 2 to 4 %, according to literature works cited earlier on this article [151][150]. The important finding is that the giant ES effect is not caused by the oxygen vacancies present to compensate the charged Gd point defects - as proposed by Korobko et al [19] - but by additional oxygen vacancies that need to be compensated by electrons close to the conduction band, and normally thought to be trapped in Ce^{3+} states [174]. Possibly, such vacancies are reorienting more easily, as they are not interacting with a Gd^{3+} ions staying at a fixed positions. Moreover, in contrast to earlier findings [178] our results show that the bottom electrode plays a major role in determining the electrostriction coefficient, and thus needs to be selected carefully, as it may change the response by a factor of 5.

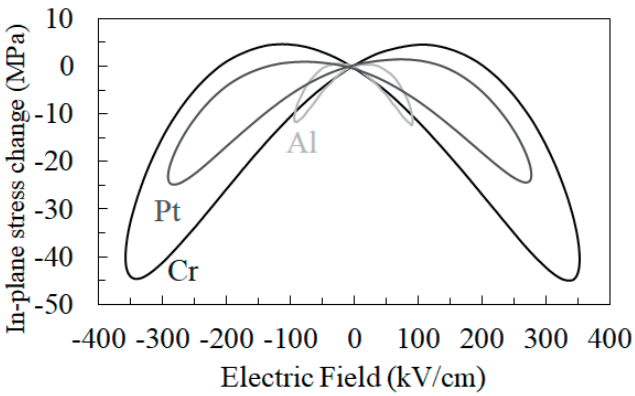


Figure 8.6 – In-plane stress change as function of electric field for CGO films deposited on different bottom electrodes (Al, Pt, and Cr) at room temperature, 15mT working pressure. The characterization frequency was 66 Hz.

Table 8.3 – The electrostriction stress coefficient,$M^{(S)}_{31,f}$, strain coefficient $M^{(T)}_{31}$, (111) texture index, and elastic modulus of CGO films deposited at room temperature on three different bottom electrodes (B.E.), Al, Pt, and Cr. $M^{(T)}_{31}$ was derived according to eq. 5, and with an electric field sept at 66 Hz. (* The Al(5.8) film will be discussed in following section)

B.E.	$M^{(S)}_{31,f}$ (N/V^2) $\times 10^{-07}$	$M^{(T)}_{31}$ (m^2/V^2) $\times 10^{-19}$	(111)-Texture index (%)	Elastic modulus (GPa)
Al (RT)(6.4)	1.4	5.4	78	180 ±7
Pt (RT)	0.33	1.2	56	185 ±9.5
Cr (RT)	0.37	1.3	75	190 ±6.5
Al (RT)(5.8)*	2.3	9	70	180 ±8.5
Pt (HT)	0.12	0.4	84	205 ±8

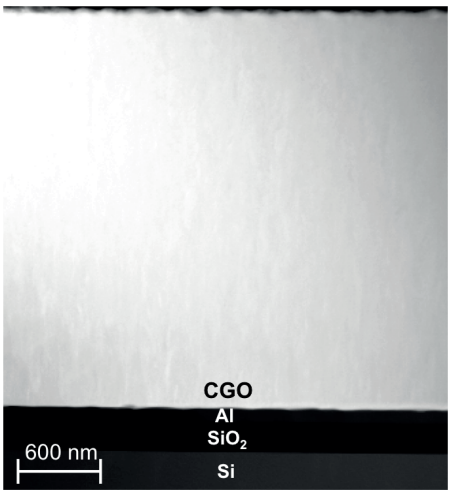


Figure 8.7 – High angle annular dark field (HAADF) TEM image of CGO thin film grown on Al bottom electrode at room temperature.

8.3.2 Ion Bombardment Effect

Besides electrodes and deposition temperature, other processing variables also impact the ES properties. In sputter deposition, ion bombardment is an important parameter, and influences for instance piezoelectricity of AlN thin films [179][180]. Ion energy and flux density are influenced by all process parameters. We varied substrate-target (S-T) distance and the sputter gas pressure to investigate their effect on the ES response. Plasma effects, such as ion bombardment, as well as deposition rate increase with decreasing S-T distance and pressure. As presented in Table 8.4, at a large S-T separation of 10 cm resulted in low ES response (-16 MPa stress at E =850 kV/cm). Smaller S-T distance of 6.4 cm resulted in a film that yielded -12 MPa in-plane stress in a field of only 90 kV/cm ($M^{(S)}_{31,f}$=1.4×10^{-07} (N/V^2). Further lowering of the distance to 5.8 cm lead to even stronger ES properties (-8 MPa at 59 kV/cm, $M^{(S)}_{31,f}$=2.3×10^{-07} (N/V^2), however at the expense of an increased leakage. This film also exhibited a lower modulus (Y=180 GPa), so one may assume that this film contains more oxygen vacancies. When we are going closer to the target, the deposition rate increases. Therefore, there is less time at the surface of the growing film to annihilate oxygen vacancies by oxygen uptake, as the diffusion distances are very limited at room temperature. A further lowering of the S-T separation leads to a loss of the (111) texture - the (111) texture index decreases from 78% to 15% - accompanied by a a strong decrease in ES properties. Moreover, at lower distance the negative O-ions coming from the target have more energy and implant easier in the film. Three different sputter pressures of 10, 15 and 20 mT were applied. The ES coefficients $M^{(S)}_{31,f}$ were measured as 4.6×10^{-09}, 1.4×10^{-07}, and 8.1×10^{-09} (N/V^2), respectively (table 8.4). The highest electrostrictive response was achieved with 15

mT Ar pressure. An optimal ion bombardment is thus needed to induce the giant electrostriction effect.

Table 8.4 – ES stress coefficient [N/V^2] as function of substrate-target (S-T) separation and chamber pressure for the films grown on Al bottom electrode at room temperature

S-T separation / Chamber Pre.	10 cm	6.4 cm	5.8 cm	5.2 cm
10 mT		4.6×10^{-09}		
15 mT	2.2×10^{-09}	1.4×10^{-07}	2.3×10^{-07}	3.4×10^{-10}
20 mT		8.1×10^{-09}		

Finally, as had been presented in this report, in order to obtain an extraordinary ES response, one has to be careful about:i) Film microstructure and texture, ii) Ion bombardment, iii) Bottom electrode, and iv) Deposition temperature. Ideally, the process condition has to be manipulated in a way that results in high oxygen vacancy content while maintaining the (111) texture.

8.3.3 The Effect of Excitation Frequency

If the giant ES effect is due to bond reorientation and local defect rearrangements, it is expected to be slower than a piezoelectric response, which is a pure lattice effect with small ion displacements from the equilibrium positions, and which may work up to the 100 GHz region. Three films with high giant ES have been characterized over a frequency range from 22 to 1052 Hz (Fig. 8.8). The observed ES response was indeed strongly dependent on the frequency. A hysteresis was observed, and the amplitude decreases with frequency above 100 Hz. Thus, for a 180 degree redirection of the polarization, the giant ES effect needs at time in the ms time range to explain the observed time lag. The apparatus has been checked with Aluminum nitride (AlN) samples to see that there is no hysteresis at these frequencies.

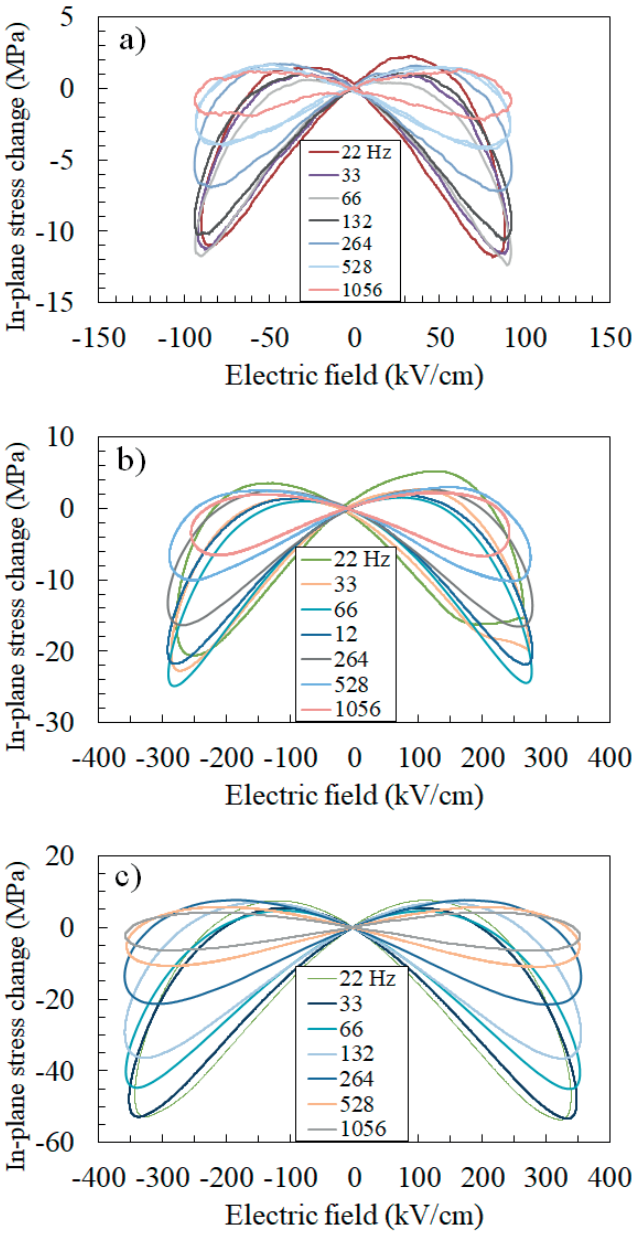


Figure 8.8 – In-plane stress change generated by an electric field as a function of frequency for CGO films deposited on three different electrodes, a) Al , b) Pt, and c) Cr. All films were deposited at room temperature with 15mT working pressure and 6.4 cm S-T separation (same as in Table 8.3).

8.3.4 Dielectric Spectroscopy

The observed time delay of GES in response to time varying electric fields are typical for space charge polarization in dielectric materials. Such phenomena may lead to

dielectric anomalies, such as to colossal dielectric permittivity (CDC) as was shown in perovskite structure $CaCu_3Ti_4O_{12}$ (CCTO) that are producing dielectric responses exceeding by far the values of known high-permittivity materials like $BaTiO_3$, and reaching $\epsilon_r \approx 10^5$ [181]. The same phenomenon was also observed at suitably doped $BaTiO_3$ and transition metal oxides like doped NiO [182] and TiO_2[183]. A number of theoretical studies [184] and experimental observations[181] have been done to elaborate the origin of CDC. Finally, an internal barrier layer capacitor model based on resistive grain boundaries surrounding semiconducting grains have been proposed to explain the colossal dielectric phenomenon [185, 186]. In thin films and single crystals, it is rather the electrode interfaces that exhibit a barrier, in the simplest case a Schottky barrier [187]. At thin film capacitors, Deng et al [188] have reported that the interior of the material is basically a doped semiconductor due to the reduction of Cu^{2+} to Cu^{1+} enabled by the relative stability of Cu^{1+} ions in oxides. The electrode interfaces, however, were oxidized by the atmosphere, leading to an interface capacitance of Schottky type. The common feature of colossal permittivity structures is the presence of multi-valent ions (Cu, Ni, and Ti). In CGO, cerium exhibits such an ambivalence of the valence: Ce^{4+} changes to Ce^{3+} in a reducing ambient. This means that in principle the same barrier model as for CCTO thin films should be applicable.

The frequency dispersion of dielectric constant (ϵ') and loss (ϵ'') are shown in Fig. 8.9 (a,b). The permittivity at low frequencies is more than an order of magnitude higher higher than observed at "ordinary" CGO thin films or at CGO ceramics [189]. The observed behavior is very similar to the behaviour of CDC materials[181, 190, 191, 192]. Let us discuss first the spectrum for the sample with the Pt bottom electrode. Its main features can be explained by a series junction of an interface capacitance C_I and a conductance G_B through the bulk of the film. These two elements lead to a Debye-like relaxation behavior with a peak loss at 250 Hz, corresponding to a relaxation time of $\tau = C_I/G_B$. In order to explain the increase of the loss towards lower frequencies, a conductance (leakage) element G_I at the interface, i.e. parallel to C_I, must be introduced. G_I is much smaller than G_B ($C_I << C_B$) and thus governs the behavior of ϵ'' at low frequencies where the C_I is blocking: $Re(Y) = C''\omega = G_I$. At higher frequencies, the capacitance is given by the one of the bulk of the film, i.e. C_B, which is much smaller than C_I (i.e. $C_B << C_I$). Considering all these elements of the equivalent circuit, one obtains a so-called Maxwell-Wagner relaxation behavior. Defining ϵ' as $\frac{Im(Y)}{\omega A} t_f$, and ϵ'' as $\frac{Re(Y)}{\omega A} t_f$ - where A is the area of the capacitor, and t_f the CGO film thickness - we obtain:

$$\epsilon'_{MW} = \epsilon_\infty + \frac{\epsilon_s - \epsilon_\infty}{1 + \omega^2 \tau_i^2} \tag{8.6}$$

$$\epsilon''_{MW} = \frac{(\epsilon_s - \epsilon_\infty)\omega\tau_i}{1+\omega^2\tau_i^2} + \frac{\sigma_{DCI}}{\omega\epsilon_0} \tag{8.7}$$

The ϵ_∞ and ϵ_s are dielectric permittivity at high and low frequencies, ω is the angular frequency, and τ is the relaxation time which corresponds to the peak in the loss curve, and σ_{DCI}=$G_I At_i$. ϵ_∞ is the intrinsic dielectric constant of CGO (ϵ_∞) and σ_{DCB}=$G_B At_f$. Knowing the the relaxation time (τ) and the bulk conductance (G_B), the interface capacitance can be derived. Assuming a dielectric constant of 30 as for intrinsic CGO, a boundary layer width of 55 nm is obtained. The device in question has both electrodes made of platinum (Pt/CGO/Pt), so one could argue that there are 2 identical interfaces, with two identical interface layers, each having a thickness of 27 nm. Experimental and derived date are summarized in supplementary information Table 1. At least the bottom interface layer is quite different when CGO is grown on an Al electrode. The interface capacitance is larger. The interface layer is produced through oxidation of the Al electrode. Curve fitting yields an interface layer thickness of 5 nm on the basis of a dielectric constant of 10. The strong Maxwell Wagner feature at about 220 Hz is due to the AlO_x interface layer. A weak relaxation effect seen at around 8 kHz is thought to be due to the top electrode interface with Pt. The presence of about 5 nm aluminum oxide layer is also evident from the High resolution TEM images presented in Fig. 8.10.

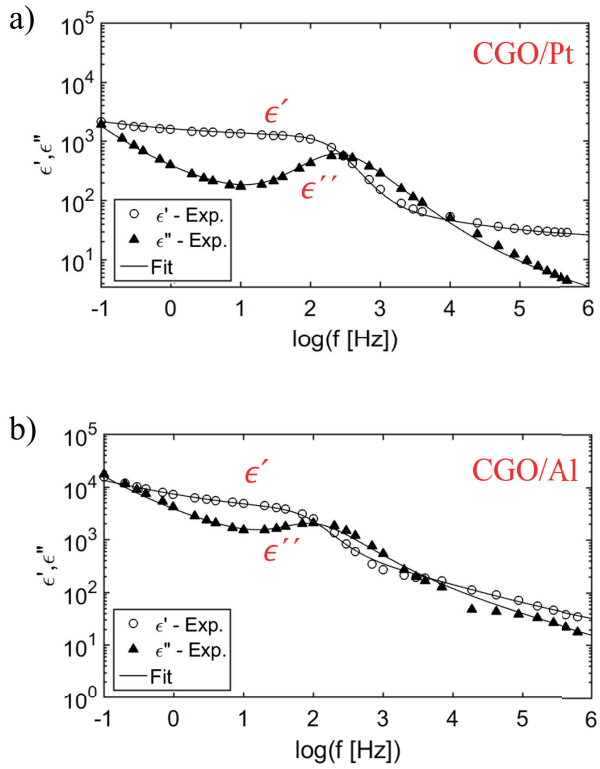


Figure 8.9 – Dielectric properties of 2μm CGO thin films deposited on a) Pt and b) Al bottom electrode. Dielectric constant (ϵ') and dielectric loss (ϵ'') are shown in Log-Log plot.

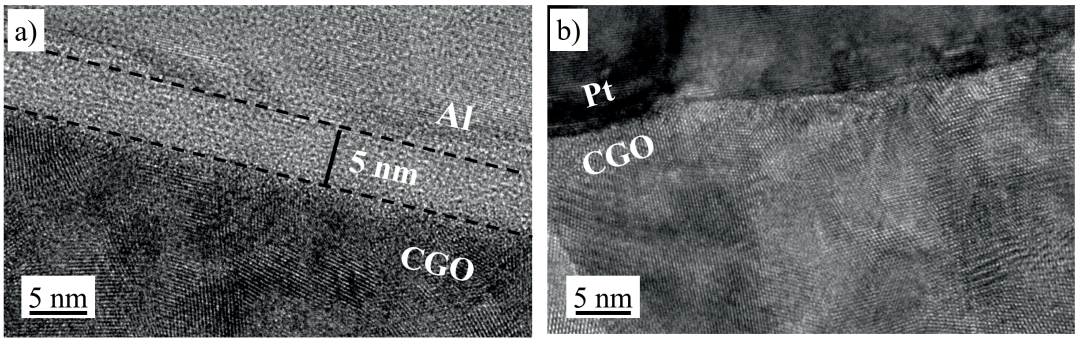


Figure 8.10 – Formation of an amorphous alumina layer with thickness of about 5 nm at Al electrode interface is evident from High resolution transmission electron microscopy (a). b) Shows the CGO/Pt interface

Maxwell-Wagner as well as the Debye relaxation models lead always to slopes of $1/\omega$ when ϵ'' is decaying with frequency. However, as seen in Fig. 8.9, the slopes are not -1,

but between -1 and 0. Also, ϵ' is not flat below the relaxation peak - as given by Maxwell-Wagner or Debye models - but increases when lowering the frequency. Both can be corrected by adding an Universal Dielectric Relaxation (UDR) behavior as introduced by Jonscher [193], and which was also described for CGO ceramics [189]. Its origin is hopping conduction that adds a term with a power-law in frequency to the DC conduction. As a consequence of the Kramers-Kronig relation.

$$\sigma(\omega) = \sigma_{DCI} + \sigma_{UDR}\omega^{s} \tag{8.8}$$

The UDR can be approximately described by a power-law as presented in Eq. 8.9 and Eq. 8.10.

$$\epsilon'_{UDR} = \frac{\sigma_{UDR}}{\epsilon_0} tan(\frac{s\pi}{2})\omega^{s-1} \tag{8.9}$$

$$\epsilon''_{UDR} = \frac{\sigma_{UDR}}{\epsilon_0}\omega^{s-1} \tag{8.10}$$

All the contribution where added together for the total response data fit, see Fig. 8.9. Overall, the equivalent circuit can be presented as Fig. 8.11.

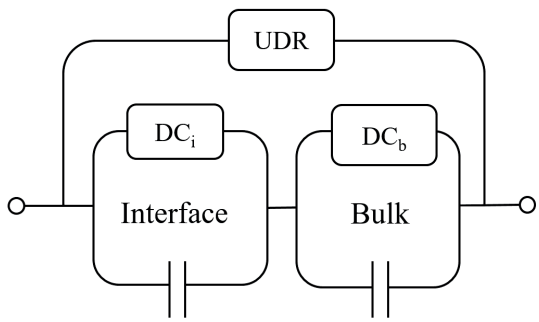


Figure 8.11 – Schematic of equivalent circuit considering MW and UDR relaxation as the main mechanism governing the dielectric response when a CDC is observed in CGO thin films

In order to show visually how each relaxation mechanism is contributing in overall response, Fig. 8.12 exhibits individually the MW and UDR relaxations behaviour as

function of frequency.

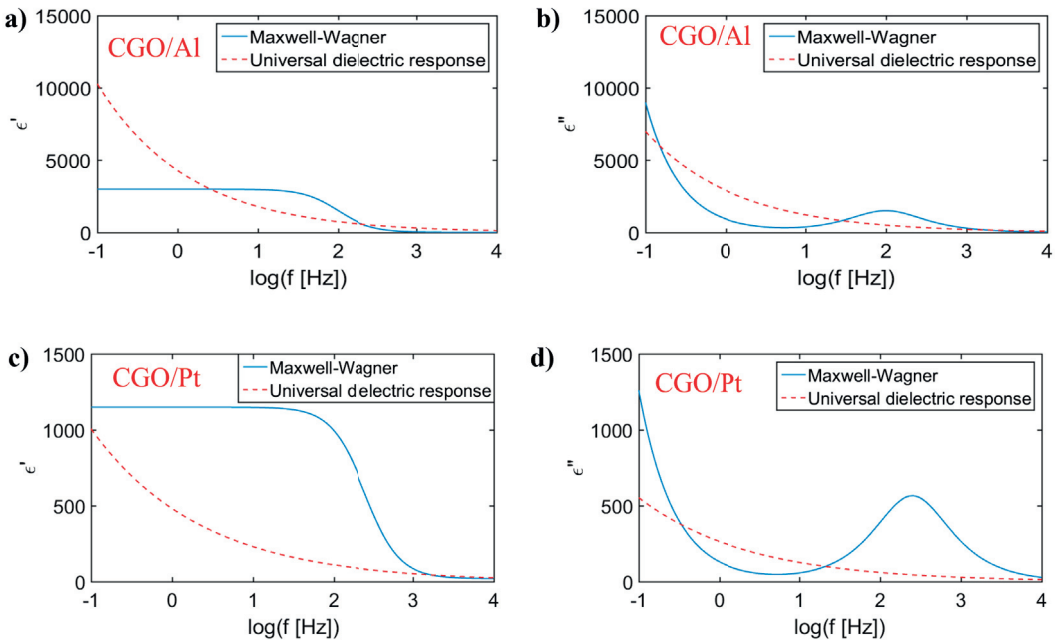


Figure 8.12 – Schematic of equivalent circuit element contribution in overall dielectric behaviour of CGO thin films deposited on Al and Pt bottom electrode, a) dielectric constant (ϵ') b) dielectric loss (ϵ'') for CGO/Al sample, c) ϵ' b) ϵ'' for CGO/Pt sample

A similar graph can be established for log(G) versus log(f), see Fig. 8.13. It shows more clearly the conductance at higher frequency, and shows the Maxwell-Wagner contribution and the Jonscher's universal relaxation.

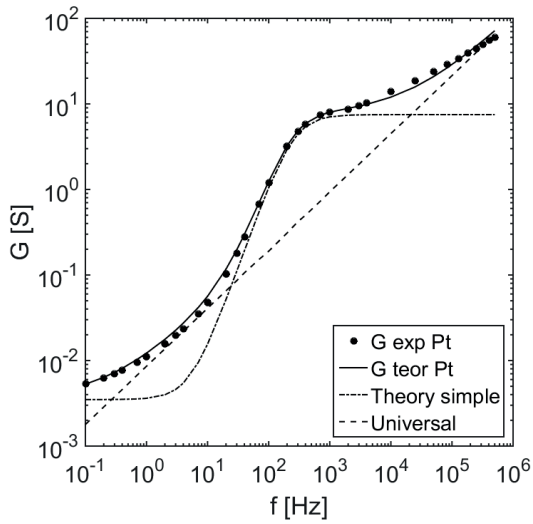


Figure 8.13 – The contribution of Maxwell-Wagner and Jonsher's universal relaxation in overall conductivity for CGO/Pt sample

As $G_B >> G_I$, we can calculate the conductance as follows:

$$G_{MW} = Re(Y) = \frac{G_I + \omega^2 \tau C_I}{1 + \omega^2 \tau^2} = G_I \frac{1 + \omega^2 \tau^2 G_B / G_I}{1 + \omega^2 \tau^2} \tag{8.11}$$

At low frequencies, this value approaches simply G_I, and at high frequencies, it will be G_B, shown as simple theory in Fig. 8.13. For introducing G_{UDR} the question is that where is practicality added over the interface or the bulk. According to the data fit adding it only over interface is sufficient. Thus one can write the G_{UDR} as (s=0.68):

$$G_{UDR} = 0.7 G_I \omega^{0.68} \tag{8.12}$$

It is very remarkable how well the UDR function is able to fit in the whole investigated frequency range, above and below the inverse relaxation frequency, $1/\tau$.

8.3.5 Dielectric Properties at High Temperature

The temperature behavior of ϵ' and ϵ'' show the typical behavior of colossal dielectric constant thin films, particularly the version with Al bottom electrode. At low tem-

peratures, the bulk of the film is insulating and the dielectric response is small. With increasing temperature, hopping conduction through the bulk increases to the point that enough ac current passes the bulk to charge the interface capacitance. The time constant for this phenomenon is the same as discussed above for the Maxwell-Wager relaxation, i.e τ=C_I/G_B. The peaks in Fig. 8.14 (d) of $\epsilon''(T)$ correspond to the match $\omega\tau$=1. In case of the Al sample, the interface capacitance is constant with temperature, and the inverse relaxation time (τ) reflects the temperature behavior of thermally activated hopping conductance. The ln($1/\tau$) vs 1/T plot reveals an activation energy of 0.51 eV (Fig. 8.15). In case of the Pt sample, no clear peaks are observed, because the interface capacitance turned out to be too leaky. However, the activation energy can by derived from the temperature behavior of the $\epsilon''(T)$ directly, see Fig. 8.15.

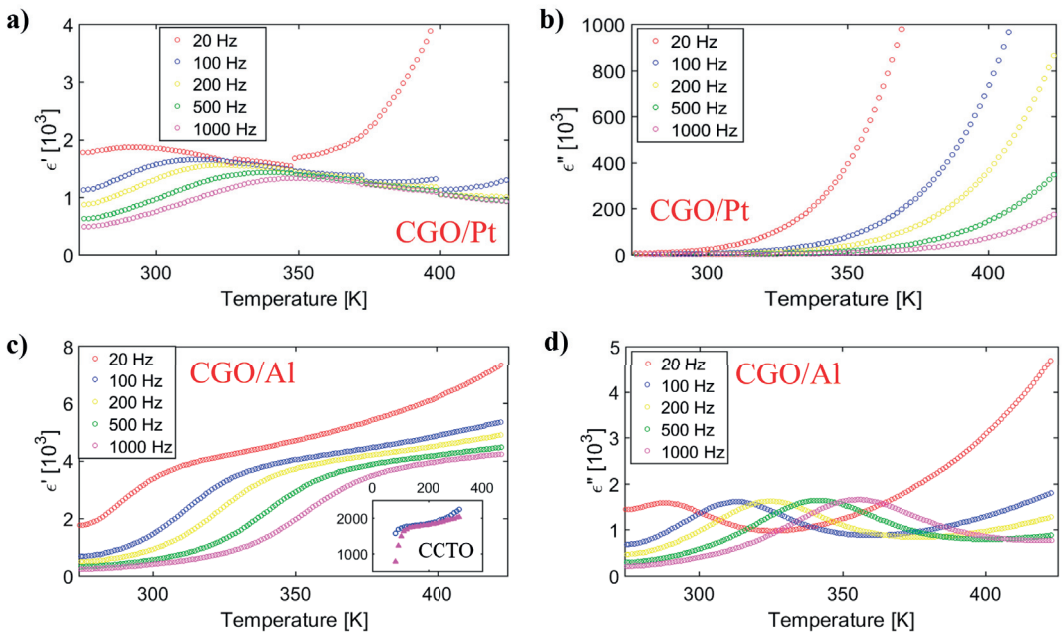


Figure 8.14 – Temperature dependence of dielectric properties of CGO thin films deposited on Al and Pt bottom electrode at Room temperature. a,c) Dielectric constant (ϵ'), b,d) Dielectric loss (ϵ''). The inset plot (c) shows the similar behavior of CCTO recalled from Ref. [194]

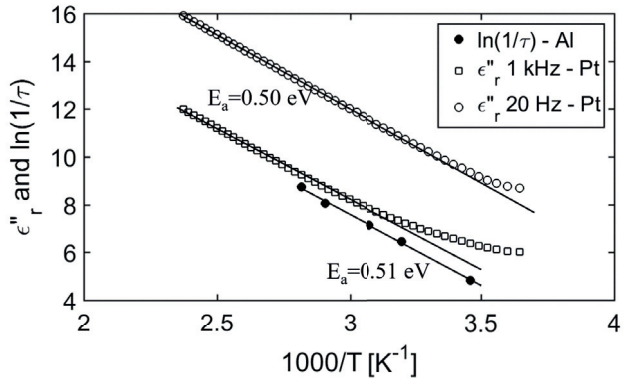


Figure 8.15 – Hopping conduction activation energy for Al sample using $\ln(1/\tau)$ and Pt sample using $\epsilon''(T)$ directly (at 20 Hz and 1kHz).

In ordinary CGO films, we measured activation energies of 0.55 eV for the ionic conduction in temperature range of 100 to 400°C, which corresponds quite well to a literature value of 0.56 eV calculated with a density functional theory [195]. The lower value of 0.51 corresponds rather to electrical conduction as observed in reduced ceria [196] with an activation energy of 0.4 to 0.5 eV in the range from 0 to 12% oxygen vacancies. The conduction mechanism ascribed to a small polaron [197]. Newer insight obtained by density functional theory suggests that the small polaron is an electron trapped as 4f electron on a Ce atom, i.e. forming Ce^{3+} ion, hopping through a 4f band to the next Ce site [198]. This would indeed require an activation energy of around 0.5 eV.

8.3.6 Non-linear Electrical Properties

The insulating interfaces is also evident from the I-V and C-V characterization (see Fig. 8.16) as it leads to non-linear behaviour on both reverse and forward directions. The almost symmetrical response confirms the existence of an insulating layer on both top and bottom electrode interfaces. The non-linear I-V behaviour seen in CGO thin films can be in great interest for varistors that are working as a protector for electronic devices [199]. Varistors can be made from many semiconductor ceramics in different scales, however there are very limited reports on thin film structure [200, 201]. According to rapid development of Large-Scale-Integration (LSI) of electronic devices, integrated surface mountable thin film varistors have a great potential. High threshold voltage, high stability over a wide temperature range, and room temperature preparation are the main advantages of CGO thin films.

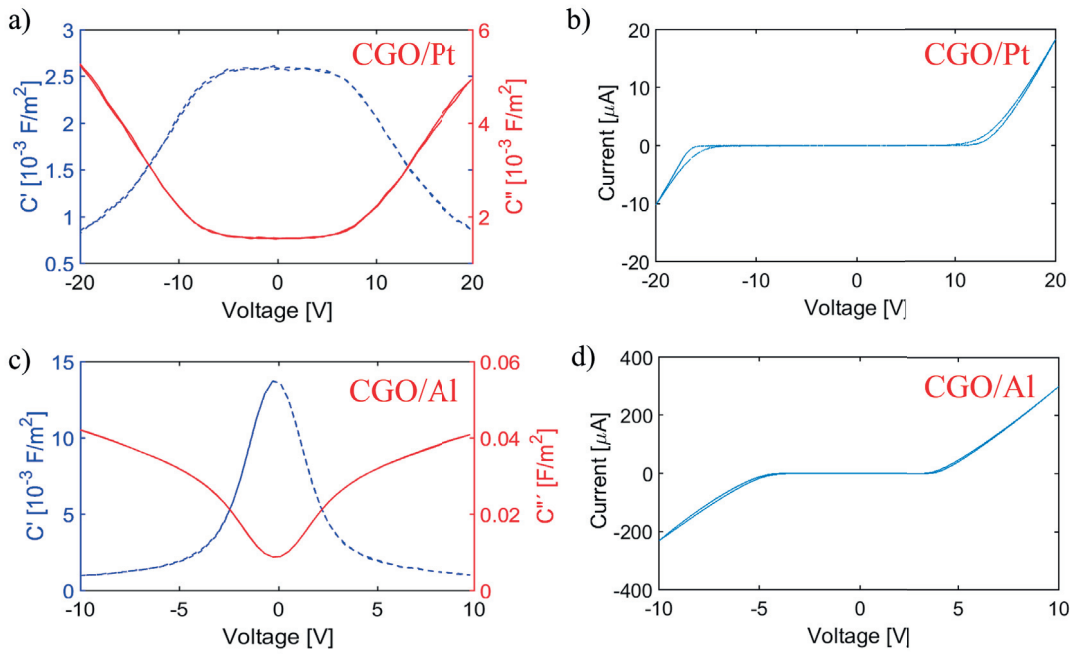


Figure 8.16 – Capacitance-Voltage measurement for CGO thin films deposited on a) Pt and c) Al. The dielectric leakage has been plotted as secondary axis (C″). The measurements have been done under DC bias with small excitation of 1 V at 500 Hz. The Current-Voltage (I-V) curves for both sample b) CGO/Pt d) CGO/Al are presented as well.

8.3.7 The Effect of Joule heating

The dramatic increase of GES response is taking place in a frequency range where the low frequency relaxation is present in the dielectric spectra, and where the capacitance is governed by insulating boundary layers at the electrode interface, see Fig. 8.17. At low frequencies, the GES films show a high leakage above a certain threshold, leading to Joule heating. Thus, very likely, the GES effect is not an intrinsic effect with considering Gd dopant effect as an intrinsic property.

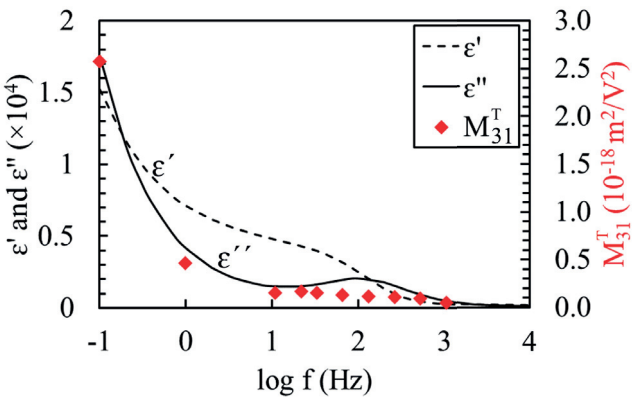


Figure 8.17 – Dielectric properties and electrostrictive strain coefficient of CGO/Al sample as a function of frequency.

In order to study the thermal stress contribution, we monitored the temperature change of the CGO/Al sample surface during the electrostriction measurements using FLIR infra-red camera. The setup is illustrated in Fig. 8.18.

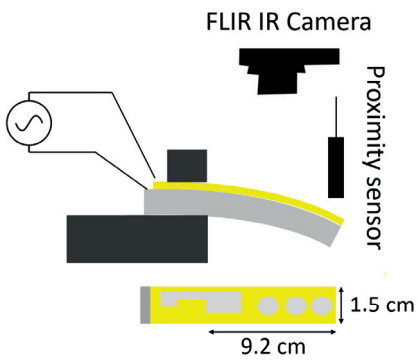


Figure 8.18 – Schematic view of electrostriction measurement setup with IR camera on top for tracking the temperature change.

As presented in Fig. 8.19, the temperature starts to grow after a threshold voltage likewise the tip displacement. This supports the contribution of joule heating in the overall response. The threshold voltage is likely due to the existence of an insulating layer at electrode interface which has been discussed in previous section.

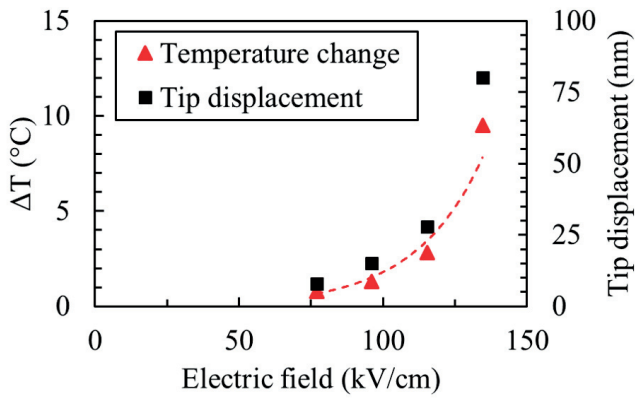


Figure 8.19 – Tip displacement recorded by proximity sensor, as well as the sample temperature change, as function of applied electric field.

At sufficiently high electric field, charges are able to pass over the interface barrier and the voltage drops across the film thickness. Consequently, the sample temperature starts to grow due to the Joule heating. At the same time, the tip displacement starts to increase suggesting that the same mechanism can be responsible for both effects. The temperature change can result in cantilever bending as thermal expansion coefficient of CGO (α_f=9.5 ppm/K [202]) is much higher than silicon (α_s =3.56 ppm/K [203]). The effect can be very similar to the electrostriction as it is proportional to V^2 and it also gives compressive stress.

In order to estimate the temperature change needed for the recorded displacement by proximity sensor (Fig. 8.19), one can use Stoney's equation where the beam radius of curvature (R) can be derived as Eq. 8.13 [50].

$$\frac{1}{R} = 6\frac{(1-\nu_s)}{(1-\nu_f)}\frac{t_f Y_f}{t_s^2 Y_s}(\alpha_s - \alpha_f)\Delta T \tag{8.13}$$

With noting that the curvature is related to the second derivative of the beam displacement, i.e. $1/R = d^2y(x)/dx^2$, after integration, one can write the free-end displacement (δ) for a cantilever with beam length of l as $\delta = l^2/2R$. Similar study has been made by Ohring [50]. Accordingly, the recorded 75 nm tip displacement under application of 130 kV/cm electric field at 60 Hz (Fig. 8.19) shall come from a temperature change of 25 °C. This is much higher than the recorded temperature by IR-camera even at stationary zone, see Fig. 8.20. The temperature profile shows the overall temperature change. The temperature modulation due to the AC field was not detectable at 60 Hz.

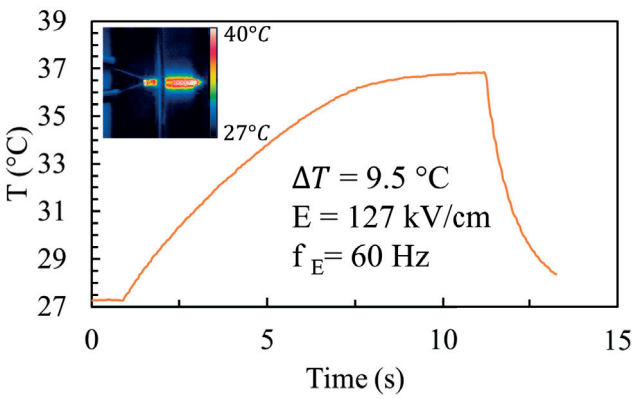


Figure 8.20 – Temperature profile of CGO/Al cantilever under application of 127 kV/cm electric field at 60 Hz. b) Schematic view of measurement setup

In order to be able to record the AC modulation, a low frequency measurement has been carried out, Fig. 8.21. However, at low frequencies (<20 Hz), the function generator used for the electrostriction characterization was not able to keep the electrical potential, thus the applied field on the sample was lower than high frequency measurements. But nevertheless, one can compare the recorded displacement and the thermal strain. The AC temperature modulation is about 0.4°C that can result in 4 nm peak to peak displacement. This is less than 15% of the recorded displacement by proximity sensor (30 nm).

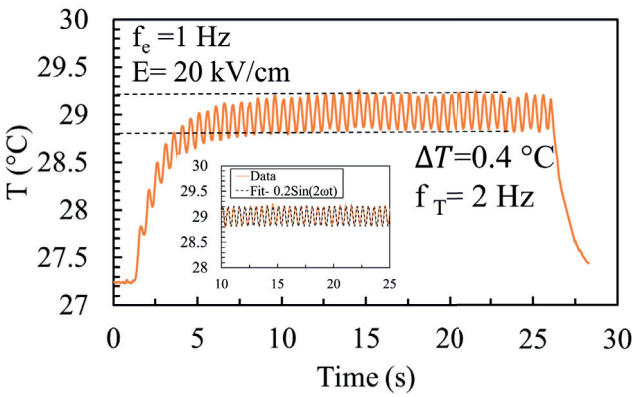


Figure 8.21 – Temperature profile of CGO/Al cantilever under application of 127 kV/cm electric field at 60 Hz. b) Schematic view of measurement setup

The difference might come from an inadequate calibration of IR-camera, especially due to emissivity correction for our complex structure. Therefore, we cannot arrive at clear theory. The obvious behaviour is, in fact, the absence of tip displacement without sample heating (Fig. 8.19). One can imagine that finite element simulation (FEM) can be an

useful method for extracting the Joule heating effect.

8.3.8 Raman Spectroscopy

To further explore the mechanism underlying the observed behavior CGO thin films were characterized by Raman spectroscopy, see Fig. 8.22. The spectra consist of one band close to 460 cm^{-1} due to Raman active vibrational mode (F_{2g}) of fluorite structure and two other bands close to 580 cm^{-1} and 640 cm^{-1} accounted for the formation of defect species related to the oxygen vacancies [204].

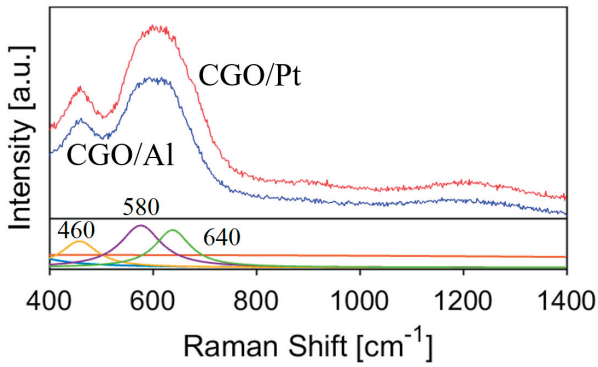


Figure 8.22 – The Raman spectra of CGO thin films deposited on Al and Pt electrodes. For data quantification all peaks were fitted with Lorentzian peak function presented at bottom of the figure.

While, the band near 580 cm^{-1} is allotted to defect spaces generated due to extrinsic oxygen vacancies that are induced by adding Gd^{3+} dopant, the band at 640 cm^{-1} is assigned to intrinsic oxygen vacancies because of cerium reduction [205, 204]. The relative concentration of an intrinsic to extrinsic oxygen vacancy defect can be estimated based on the ratio of these two band intensities [206]. With a rough estimation one can say that both peaks are having more or less the same intensity. Considering of 5% oxygen vacancies due to 20% gadolinium doping, it can be stated that the amount of oxygen vacancies due to reduction of cerium shall be in the same range as the ones coming from Gd doping. This is in agreement with our earlier finding about the excess of oxygen vacancies in especially prepared CGO thin films, where the concentration of additional oxygen vacancies were estimated between 2-4 % based on the elastic modulus change and SEM-EDAX[149].

8.4 Summary

We have shown that specially prepared CGO thin films show the phenomenon as described by Korobko et. al, and that our films achieve electrostrictive strain coefficients of up to $M_{31}^{(T)}$=2.7×10^{-18} (m^2/V^2). The particular microstructure required for the giant ES effect was obtained by employing a low deposition temperature, a higher ion bombardment, and an higher deposition rate, as compared to the usual process for an electrolyte membrane fabrication. All these parameters ranges are known to produce a higher defect density. In the end, we obtained a 70 fold increase of the ES coefficient as compared to ordinary CGO thin films. There is evidence that a higher oxygen vacancy concentration than introduced by the Gd doping is needed. We found by SEM-EDAX investigations that this excess concentration is 1 % or higher. These additional oxygen vacancies are compatible with the observed lowering of the stiffness, a maximal concentration of less than 4%. We also have shown that the bottom electrode has a crucial impact on the efficiency of the microstructure. Best electrostrictive responses have been obtained for films deposited on Al bottom electrodes, i.e., $M_{31,f}^{(S)}$=2.3×10^{-07} (N/V^2). This could indicate that a reduction of CGO at the interface plays a role for increasing oxygen vacancy concentration. Additional defects, and most likely the mentioned oxygen vacancies compensated by Ce^{3+}, are in fact needed to explain why ordinary CGO with the vacancies compensating the Gd dopants do not lead to the giant ES effect. We also have observed a strong frequency dependence of the ES response in case of bipolar operation. The change of sign of the electric field is leading to hysteretic behavior in terms of a voltage shift of the stress curve. There is an obvious time delay in increasing and decreasing the giant ES effect in a time varying electric field, supporting the hypothesis advanced in the literature that bond reorientation in the electric field, eventually accompanied by a vacancy hop, is at the origin of the effect. The involved time delays are typical for space charge effects in the response of dielectric materials.

The dielectric characterization revealed that specially prepared CGO thin films with GES are exhibiting a complex behaviour of dielectric relaxation leading to a large dielectric response at low frequencies. The dielectric response shows the same features as known from colossal dielectric thin films. We deal with a boundary layer capacitor structure. The interior of the film has a higher oxygen vacancy concentration that the electrode interfaces, caused by re-oxidation after thin film deposition. We have shown that depending on the bottom electrode or contact type CGO thin films are able to show colossal dielectric contact (CDC), 1.5×10^4. Moreover, a strong nonlinear I-V behaviour have been seen in CGO thin films with threshold voltage of ≈10V, very much like a varistor.

The general finding that large electrostrictive coefficients are accompanied by large dielectric response is also valid for CGO. The high electrostricive response is restricted

to low frequencies as is the large dielectric response, and where the capacitance is governed by insulating boundary layers at the electrode interface. The dramatic increase of GES is at very low frequencies where the films are showing a high leakage above a certain threshold, leading to Joule heating. This was observed by recording the sample temperature change under application of an electric field at low frequencies. Therefore, one can imagine that the GES effect is not an intrinsic effect with considering Gd dopant effect as an intrinsic property.

Part IV

Summary and Outlook

Thesis Summary

In this thesis, we have studied the Nanoionics phenomena and devices based on solid ion-conducting thin films and studied three topics towards applications in micro and nanotechnology. The first one was a novel fabrication approach to deal with thermal stress in electrolyte membranes for micro Solid Oxide Fuel Cells to be used as a power source in portable electronic devices. The second one was the study of fast oxide ion conductors in Resistive Random Access Memories. And finally, we have investigated the recent discovery of giant electromechanical response in cerium gadolinium oxide ion conducting thin films, which look interesting not only from point of view of their electromechanical, but also from point of view of their varistor properties.

Micro Solid Oxide Fuel Cells (µSOFC)

Even though very promising results were reported in the literature, the mechanical stability of the PEN membrane is still a challenging issue and limits the upscaling of µSOFC. In order to lower the SOFC operation temperature, the electrolyte thickness must be reduced to a sub-micron value.The active area has to be large enough to provide a sufficiently high power output of several watts to meet the power needs of portable devices. Fulfilling these two conflicting requirements at the same time is in practice very challenging. In this work, we have proposed and studied the use of ring-shaped corrugated membranes allowing the membrane to adapt to thermal stress by breathing. The advantage of such more stress tolerant structure over the other concepts, e.g. metallic grid support, hole-based corrugation or supported membranes, is more stable liberation borders, the absence of severe mechanical buckling, and the increase of surface for a given footprint. We fabricated 1.5 mm wide circular membranes with high mechanical stability. Nevertheless, the assessment of membrane buckling suggests the optimal opening diameter is in the range of 500-750 µm. The electrochemical performance of 500 µm wide µSOFC with layer stack of pPt/YSZ/pPt (200/500/200 nm) have been studied. The electrical power density delivered at 350°C with diluted H_2 fuel was measured as 12.5 mW/cm^2. The low power density appears to be due to large activation polarization, which is highly dependent on the operation temperature and the electrode quality. The power density is comparable to published values at same operation temperature. The same reports had studied higher operation temperatures and it has been seen that the power density can raise to 200-500 mW/cm^2 by increasing the temperature to 500°C. Therefore, one can expect to obtain a power output of 1-2 Watts with using a multi-array devices with a chip size of 2×2 cm^2 at 500°C. This can be very interesting for using µSOFC in portable devices. The problem encountered in this work was a limitation of 350°C of the used apparatus.

In addition, we have studied the potential of hafnium oxide based thin films to be used as an electrolyte in µSOFC. Hafina and zirconia are both fluorite structures, however, hafnia is not as good in oxygen ion conduction as zirconia. Nevertheless, it was hoped that a few nanometers of hafnia deposited by ALD would strengthen the membrane, and not too much increase the resistance. ALD process are very suitable to deposit ultra-thin films conformally onto corrugated surfaces. Up to 300°C the ion conductivity in hafnia thin films were comparable to YSZ thin films, however, at higher temperature a phase transition seemed to take place and resulted in reduced ion conductivity. Very likely a phase transition from monoclinic to the tetragonal structure is happening at 300-350°C. The observed phase transition in pure hafnia has not been reported in the literature. We have also investigated the effect of yttrium doping on microstructure and ion conductivity. It turned out that doping hafnia with 30% yttrium stabilizes the cubic structure at room temperature, nonetheless, like hafnium oxide, a phase transition seems to take place shifted to the higher temperature of 400°C. The ion conductivity at very high temperature was comparable to YSZ thin films, Although, with higher activation energy 1.21 eV (in comparison to YSZ with an activation energy of 0.90 eV). According to theoretical predictions, hafnium oxide is expected to show similar activation energy to YSZ. Thus the higher measured value can be either due to contribution of grain boundaries, or defect clustering as result of high doping concentration.

Resistive Random Access Memories (ReRAMs)

ReRAMs have been proposed many years ago and appears now as one the most promising emerging technologies for future non-volatile memories. The resistive switching is mostly due to the formation/rupture of a conductive filament in an insulating (semiconductor) layer. Metal-oxides have been studied extensively, e.g. TaO_x, HfO_x, and TiO_x, in which the formation of conductive filaments made of oxygen vacancies are thought to lead to resistive switching between at least two resistance states. Having high concentration of mobile oxygen vacancies is thought to lead to a more easy formation of such filaments and may lead to lower switching voltages. It is thus legitimate to consider fast ion conductors, CGO and YSZ thin films, will be very promising candidates for resistivity switching. However, they were almost ruled out from the long list of materials that have been investigated. In this work, we have studied the potential of both materials to be used as switching layer in ReRAMs. We have prepared chip sized ($2\times2\,cm^2$) test structures in which the memory active area was defined based on the via opening that was made through a silicon oxide (SiO) layer. The SiO layer was separating the top and bottom electrodes for avoiding any cross-talk. The device structure was composed of 100 nm Pt layer as bottom electrode and 100 nm TiN as top electrode. The I-V DC characterization, as well as AC pulse measurement, have been carried out. Both films have shown outstanding electrical characteristics comparable

to high-performance switching materials with high stability and endurance. CGO thin films are able to operate at V_{set} = 1 V and V_{reset}= -0.6 V over multiple cycles. YSZ thin films are showing similar behaviour with V_{set} = 1.1 V and V_{reset}= -0.6 V. Both cells have shown stable response over 10^4 cycles with ON/OFF ratio of 100 and 5 for CGO and YSZ, respectively. It turned out that the switching mechanism in CGO films is rather a multi-filament switching as the LRS and forming voltage decreases with increasing the device size, whereas, in the YSZ-based memories less filaments are expected to be formed since the scaling effect was not clearly observed.

Novel Properties in CGO thin Films

The recent discovery of giant electrostriction (GES) in Gd doped ceria put the question on the table whether ion conducting oxides must be also considered as electromechanical materials. The size and also the fact that a compressive stress is generated in the film plane, in contrast to piezoelectric effect that produces a tensile stress at equal geometry, makes this finding extremely interesting for actuators in MEMS. In addition it is a lead free material and and thus could replace PZT in micro actuators. In this work, this phenomenon was investigated in more detail with the goal to elucidate its origin. The term giant was used to name the fact that the observed electrostriction was about 3000 times larger than expected for relatively modest dielectric constant of this material. The effect was ascribed to high density of oxygen vacancies that are introduced by the choice of trivalent dopant. In our work, we have succeeded to reproduce the giant electrostriction (9.0×10^{-19} (m^2/V^2) for the strain coefficient, and 2.3×10^{-7} N/V^2 for the effective stress coefficient) at low frequencies (<1kHz). We have shown that the giant electrostriction is related to defect that are produced during rather specific deposition parameters such as low deposition temperature, an optimal ion bombardment and high deposition rate. It has been found that a higher oxygen vacancy concentration than introduced by Gd doping is needed. Additional oxygen vacancies are most likely compensated by the reduction of Ce^{4+} to Ce^{3+}. Furthermore, we have seen that the giant electrostriction is depends on the bottom electrodes. Al gave higher coefficients as compared to Cr and Pt.

As the GES effect was found to be quite slow, it was obvious to investigate particularly dielectric properties at low frequencies in order to elucidate the discrepancy of large electrostriction at low dielectric constant. Indeed, large dielectric constants of over 1000 were observed, reminding at the phenomenon of the colossal dielectric constant. The films are characterized by a strong nonlinear I-V behavior with a threshold voltage of about 10V. The basic reason for the phenomenon was found in the fabrication process in slightly reducing atmosphere leading to excess oxygen vacancies (3-5%) being compensated by Ce^{3+}. This finding is also supported by Raman spectroscopy. The trapped electrons on

Ce^{3+} lead to hopping conduction through the bulk of the film. Dielectric spectroscopy gives evidence that the interfaces are insulting by their nature or re-oxidation from the air. The films thus form Schottky barriers or metal-insulator-semiconductor interfaces with their electrodes.

The dramatic increase of GES response is taking place in a frequency range where the low frequency relaxation is present in the dielectric spectra, and where the capacitance is governed by insulating boundary layers at the electrode interface. At low frequencies, the GES films show a high leakage above a certain threshold, leading to Joule heating. Thus, very likely, the GES effect is not an intrinsic effect, but an extrinsic one arising from thermal expansion mismatch with the substrate. This, in fact, needs to be further investigated.

Thesis Outlook

Micro Solid Oxide Fuel Cells (µSOFC)

While the ring-shaped corrugated structures have addressed most of the mechanical issues, the cell performance still needs to be improved. The first attempt shall be the optimization of electrodes deposition in order to increase the TPB and facilitate the gas access to the electrolyte interface. Study of perovskite electrodes for increasing the device endurance would be the second task. This should lead to a power density of $1\,W/cm^2$. Afterwards, the study of arrays concept with 500 µm wide membranes should be entackled to a achieve a total power o several watts. Finally, mounting the µSOFC on micro-heaters with embedded gas micro-channels would be the ultimate goal for making a demonstrator and confirm the potential of µSOFC to be used as portable power source.

Resistive Random Access Memories (ReRAMs)

The potential of CGO and YSZ thin films to be used as switching layer in ReRAMs have been shown using shadow mask based fabrication method. Nevertheless, due to the big electrode sizes in this method, one cannot eliminate the effect of the device geometry from the material characterization. Hence, fabricating the same devices using photo-lithography and consequently lowering the electrode size can give better understanding of the material properties. Furthermore, the positive impact of different buffer layers such as aluminum oxide, hafnium, titanium and etc, have been seen on most of studied switching layers. Therefore, one should investigate the effect of the buffer layer on CGO and YSZ thin films. Furthermore, in the cell characterization, we have seen a large preforming region (difference between the pristine resistance state and HRS) that can be enhanced by lowering the compliance current. Finally, the study of resistive switching mechanism has to be enriched by conductive AFM in order to support the hypothesis of having multi-filament switching.

Novel Properties in CGO thin Films

The GES in CGO thin films seems to be an extrinsic effect due to the contribution of Joule heating. Furthers studies are needed to completely understand the acting mechanism. We have seen that the hopping conduction is contributing the most, however, drawing a clear picture is still under investigation. Finite element simulation can be very helpful for simulating the experimental conditions and derive the temperature change under an AC electric field at different frequencies.

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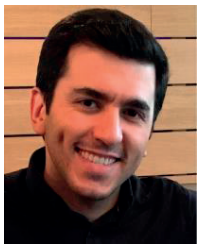
Curriculum Vitae



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Publications

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2015 Material Workshop, Leysin, Switzerland
Poster presentation : *The role of point defects on giant electrostriction in CGO thin films*

2016 PiezoMEMS Workshop, Grenoble, France
Poster presentation Electromechanical response in CGO thin films

2016 Electroceramics, Limoges, France
Oral presentation *Key-features in processing and microstructure for achieving giant electrostriction in gadolinium doped ceria thin films*

2017 Advanced ceramic and composite materials, ceramic society, Florida, United states
Oral presentation *Thermal strain control in free-standing micro solid oxide fuel cells*