A Nine Decade Femtoampere Current to Frequency Converter

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Beyond the horizon of the place we lived when we were young
In a world of magnets and miracles
Our thoughts strayed constantly and without boundary
The ringing of the division bell had begun...
—High Hopes, Pink Floyd

To my family.

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Lausanne, 16 June 2017 Εύη

Abstract

Various applications require ultra-low current sensing. Some of these applications are related to ionizing radiation detection. Radiation monitoring is important in particle physics experiments, nuclear facilities, hadron therapy institutes and hospitals. In these cases the detectors used are mostly gas-filled detectors like ionization chambers. The output of these detectors is a current that is normally proportional to the energy deposited by the incident radiation.

The European Organization for Nuclear Research (CERN) has a legal obligation to comply with the legislation in matters of radiation protection in order to avoid any unjustified dose to people or pollution of the environment. According to the existing detectors, the current output varies from a few femtoamperes up to the microampere range.

The scope of this thesis is the design of a microelectronic integrated wide dynamic range front-end for radiation monitoring.

Firstly, the state of the art has been investigated and different technologies have been compared. The selected architecture is based on current to frequency conversion with charge balancing. The main limitation in ultra-low current sensing is related to the leakage currents that are present in the front-end input. A demonstrator Application Specific Integrated Circuit (ASIC) named Utopia 1 was built in AMS 0.35 μm technology to estimate the different sources of leakage currents and provide guidelines or design solutions for femtoampere measurements. According to the achieved results, a new ASIC named Utopia 2 was designed that has been optimized to minimize the non-ideal effects.

The Utopia 2 is able to digitize currents from 1 femtoampere (fA) up to 5 microamperes (μA). To achieve such performance, the ASIC includes an active on-chip leakage current compensation circuit and a multi-range charge balancing circuit. The ASIC integrates the input current in a constant acquisition time, but for the sub-picoampere current measurements the measuring time needs to be increased.

The ASIC has been characterized for its low current performance in the Swiss Federal Institute of Metrology (METAS). The ASIC's calibration procedure and qualitative radiation measurements with the detector in the presence of radiation sources have been performed. The designed ASIC is the ultra-low current sensing circuit and digitizer that will be used at CERN for radiation monitoring for personnel and environmental safety.

Abstract

Key words: radiation monitoring, femtoamperes, leakage currents, current to frequency conversion, active leakage compensation

Résumé

De nombreuses applications nécessitent la détection de courants ultra-faibles. Certaines de ces applications sont liées à la détection des rayonnements ionisants. La surveillance des radiations est importante dans les expériences de physique des particules, les installations nucléaires, les centres de thérapie hadronique et les hôpitaux. Les détecteurs utilisés sont principalement des détecteurs remplis de gaz telles les chambres à ionisation. Le signal de sortie de ces chambres est un courant qui est généralement proportionnel à l'énergie déposée par le rayonnement incident.

L'Organisation européenne pour la recherche nucléaire (CERN) a l'obligation légale de se conformer à la législation en vigueur en matière de radioprotection pour empêcher toute dose injustifiée pour les personnes et l'environnement. Selon les détecteurs actuellement utilisés, leur courant de sortie varie de quelques femtoampères (fA) jusqu'à atteindre la gamme du microampère (μA).

Le sujet de cette thèse est la conception d'une interface microélectronique intégrée à large dynamique de mesure adaptée à la surveillance des radiations.

Tout d'abord, l'état de l'art dans le domaine de la mesure de courants ultra-faibles a été investigué et les différentes technologies ont été comparées. L'architecture finalement retenue est basée sur la conversion de courant en fréquence avec équilibrage de charges. La principale limitation de la mesure de courants ultra-faibles est liée aux courants de fuite présents à l'entrée du circuit de mesure. Un démonstrateur, basé sur la mise en œuvre d'un circuit intègré spécialisé ou ASIC (Application Specific Integrated Circuit), a été réalisé en technologie 0.35 μm d'AMS pour estimer les différentes sources de courants de fuite et fournir des lignes directrices ou des solutions de conception pour la mesure au niveau du femtoampère. Sur la base des résultats obtenus, un nouvel ASIC Utopia 2 a été conçu et optimisé afin de minimiser les effets non idéaux.

L'ASIC Utopia 2 est capable de numériser des courants de 1 femtoampére (fA) jusqu'à 5 microampères (μA). Pour obtenir une telle performance, l'ASIC comprend un circuit actif de compensation des courants de fuite et un circuit d'équilibrage de charges à plusieurs gammes. L'ASIC intègre le courant d'entrée avec un temps d'acquisition constant, mais pour la mesure de courants inférieurs au picoampère (pA), le temps de mesure doit être augmenté.

Les performances de mesure de bas courants de l'ASIC ont été caractérisées à l'Institut fédéral

de métrologie suisse (METAS). La procédure d'étalonnage de l'ASIC et les mesures qualitatives réalisées avec un détecteur de rayonnements ionisants en présence de sources radioactives ont été effectuées. L'ASIC conçu sera le circuit de détection de courants ultra-faibles et le numériseur utilisés au CERN dans le cadre de la surveillance des rayonnements ionisants pour la protection du personnel et de l'environnement.

Mots clés : surveillance des rayonnements, femtoampères, courants de fuite, conversion de courant en fréquence, compensation active des courant de fuite

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1 Introduction

1.1 CERN

The European Organization for Nuclear Research (CERN) sits astride the Franco-Swiss border near Geneva and was founded in 1954. It has since become the largest particle physics laboratory in the world. The purpose of CERN is to study the basic constituents of matter, the fundamental particles and enhance our understanding of the fundamental laws of nature. Inside CERN's accelerator complex, particle beams collide with targets or against each other at speeds close to the speed of light. The detectors that monitor the collisions give the physicists clues about how particles interact.

Protons and lead ions are accelerated in the Large Hadron Collider (LHC). For the protons firstly, Linac 2 accelerates them to the energy of 50 MeV. The proton beam is then injected into the Proton Synchrotron Booster (PSB), which accelerates it to 1.4 GeV, followed by the Proton Synchrotron (PS), which enhances the beam to 25 GeV. Protons are then sent to the Super Proton Synchrotron (SPS) where they are accelerated to 450 GeV. The protons are finally transferred to the two beam pipes of the LHC, where the beam in one pipe circulates clockwise, while the beam in the other pipe circulates anti-clockwise. There, beams are accelerated to energy up to 6.5 TeV and then circulate for many hours being focused and brought into collision inside the four detectors installed in underground caverns. The detectors are [1]:

- A Large Ion Collider Experiment (ALICE)
- ATLAS
- Compact Muon Solenoid (CMS)
- Large Hadron Collider beauty (LHCb)

The total energy at the collision point is equal to 13 TeV.

Similarly, the lead ions for the LHC start from Linac 3, before being collected and accelerated in the Low Energy Ion Ring (LEIR) and then follow the same route as the protons. The current CERN accelerator complex is shown in figure 1.1 [2].

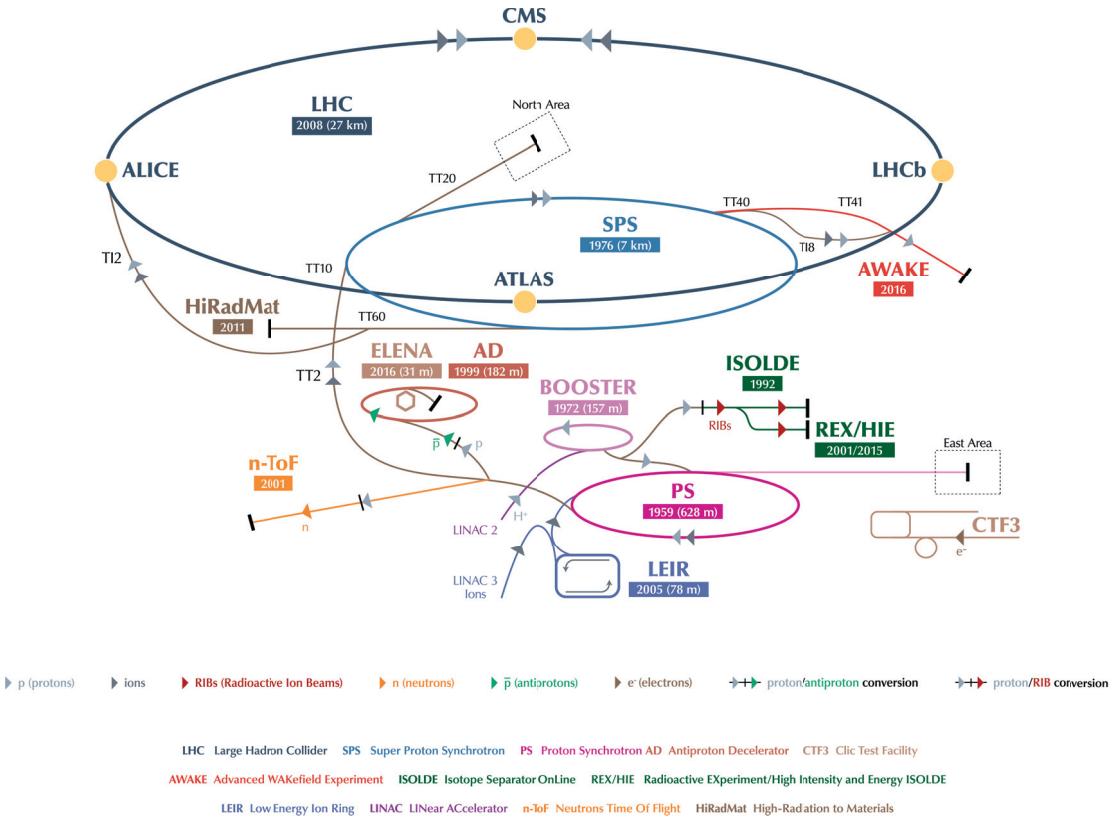

Figure 1.1 – CERN accelerator complex [2]

1.2 Radiation Monitoring at CERN

The operation of the CERN accelerators induces ionizing radiation and radioactivity due to the interaction of high energy beam particles with matter. Monitoring of the ionizing radiation inside and around CERN's accelerator complex is challenging due to the pulsed nature of the particle beams and the large dimensions of the CERN facilities [3]. The radiation levels should be continuously monitored in order to protect the public and the personnel from any unjustified exposure to ionizing radiation. This is a legal obligation set by national and international regulations. CERN has to comply with the environmental regulations that set an annual dose limit which must not be exceeded [4].

The CERN's radiation protection policy [5] stipulates that the exposure of persons to ionizing radiation and the radiological impact and pollution of the environment should be As Low As Reasonably Achievable (ALARA) [6], [7]. The ALARA principle sets the requirements for a sophisticated radiation monitoring system. The general principles of the radiation protection

legislation and the classification of radiological risks and areas inside CERN are analyzed in the "Radiation protection at CERN" article [8].

CERN's Occupational Health & Safety and Environmental Protection (HSE) Unit monitors the ambient dose equivalent rates inside and outside CERN's perimeter. The radiation monitoring allows the preventive assessment of the radiological hazards and the minimization of individual and collective doses to the public or workers. The RAdiation Monitoring System for the Environment and Safety (RAMSES) comprises more than 350 monitors that perform continuous real time measurements of the radiation levels on the surface of CERN premises and in underground accessible areas [9]. The RAMSES system includes the radiation monitors, the data acquisition and the processing unit. The system also generates alarms and interlock signals. It provides long term data logging of the measured values and of the alarms. The recorded data are required to prove CERN's compliance with the relevant legislation and to report to the host states authorities.

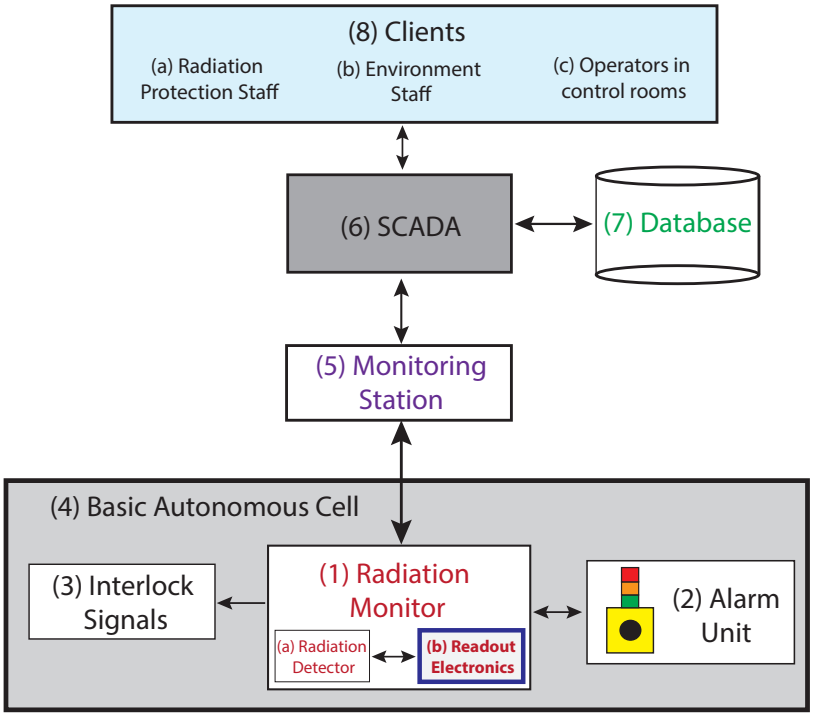

Figure 1.2 – Functional diagram of the CERN radiation monitoring system [3]

The functional diagram of the CERN's radiation monitoring system is illustrated in figure 1.2. The ionizing radiation monitor (1) is selected according to the specific properties of the monitored area and includes the ionizing radiation detector (a) and its readout electronics (b). The system includes an alarm unit (2) and can generate interlock signals (3) if required. Parts (1), (2) and (3) form a Basic Autonomous Cell (4) that is supplied by the monitoring station (5) that acquires and stores the produced data. The Supervisory Control and Data Acquisition (SCADA) system noted as (6) transfers the monitored data to the Database (7). Finally, the data can be assessed by the Clients (8) using a user friendly interface [3].

1.3 Thesis Outline

A state of the art radiation monitoring system is important for CERN for avoiding any unjustified doses to the public or pollution of the environment. To achieve its objectives the system should integrate a set of functions presented in the functional diagram of figure 1.2. The current thesis focuses on the dedicated integrated circuit design of the most demanding part of the system, the readout front-end electronics (b) used to digitize the signals that are generated by the radiation detector (a). Up to now, commercial off-the-shelf (COTS) electronics were used for the readout system at CERN. These components do not meet all the required specifications. The design of an integrated circuit is motivated by the need to digitize ultra-low input currents over a wide dynamic and temperature range.

The thesis is organized as follows:

In the **second chapter**, the various radiation detectors currently used at CERN are presented. The main challenge is that the detectors produce output currents that start from the femtoampere range (fA) and span up to microamperes (μA). The existing systems for monitoring ionizing radiation used in High Energy Physics (HEP) experiments, nuclear facilities and hospitals are reviewed and the state of the art is presented.

The **third chapter** focuses in sub-picoampere current measurements and discusses the main limitations when measuring in the femtoampere (fA) range. The net leakage current in the input of the front-end is comparable to the signal to be measured. The different leakage current sources present at the input of the readout system are identified and characterized in order to set the achievable limits for ultra-low current measurements. The development of an Application Specific Integrated Circuit (ASIC) named Ultra-low Picoammeter 1 (Utopia 1) is presented. Its design aims at estimating the lowest possible current that can be measured with a system built with the selected technology. The guidelines that this prototype set for ultra-low current measurements are outlined.

The **fourth chapter** presents the design procedure and the architecture of the Ultra-low Picoammeter 2 (Utopia 2) ASIC. This ASIC is the proposed integrated solution for the front-end of the new radiation and environmental monitoring system for personnel and public safety at CERN. This ASIC is designed in a way that the net leakage current is minimized according to the guidelines that were set with the demonstrator Utopia 1 ASIC. It operates faster than Utopia 1 and incorporates an on-chip active leakage current compensation technique that makes the chip performance insensitive to temperature variations. The automatic two-range charge balancing circuit that manages the higher input currents is also presented.

In the **fifth chapter**, the data acquisition system, the calibration procedure, the characterization and the measurements of Utopia 2 ASIC are reported. The results of the tests performed at the Swiss Federal Institute of Metrology (METAS) are shown. Qualitative radiation measurements with the detector are also presented.

Finally, the conclusions and the contributions of the current thesis are drawn. The performance of the designed ASIC is discussed. The presented guidelines for the femtoampere current measurements can be followed in any system that targets ultra-low current sensing performance.

2 Front-end Electronics for Gas-Filled Detectors

2.1 Introduction

The most widely used ionizing radiation detectors are ionization chambers. In this chapter, the available radiation detectors used at CERN are presented. The specifications for the front-end readout electronics for the new radiation monitoring system are set according to the detectors in use at CERN. The readout system should be able to cover the required dynamic range of the various detectors. Depending on the detector, the output current is as low as a few femtoamperes (fA) and spans up to the microampere (μA) range. This chapter also presents the Current to Frequency Converter (CFC) architecture that is suitable for current digitization over the required wide dynamic range. The state of the art for radiation monitoring front-ends is reviewed and the most recent developments in particle physics experiments and hadron therapy institutes are briefly explained.

2.2 Gas-Filled Detectors

When radiation passes through a gas, it ionizes the gas molecules. The produced electron and ion pairs move in opposite directions due to the applied external electric field, thus resulting in an electric charge that can be collected and measured [10]. A gas-filled detector consists of the enclosure, the positive and the negative electrodes as shown in figure 2.1. The bias voltage is applied to the electrodes in order to produce the desired electric field. Based on the applied bias voltage, the gas detectors operate in different regions. In the ion chamber region, all the produced charges are efficiently collected by the electrodes. The gas detectors that operate in this region are called ionization chambers.

2.2.1 Ionization chambers

Ionization chambers are the most widely used radiation detectors because of their design simplicity and their well understood operating principle [11]. The output current measured

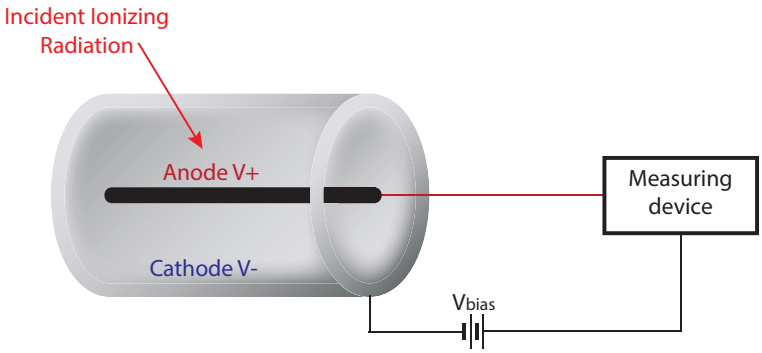

Figure 2.1 – Cylindrical gas-filled detector

by the readout electronics is proportional to the energy deposited by the incident radiation as shown in figure 2.2. An advantage of the ionization chamber is the existence of a plateau region without significant slope, where the measured current does not increase with a bias voltage increase.

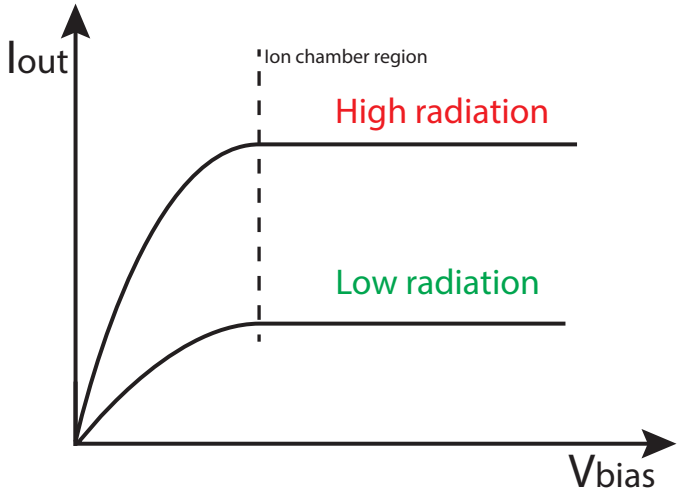

Figure 2.2 – Output current and bias voltage characteristic curves of an ionization chamber at different incident radiation intensities

Apart from the applied voltage, the production of charge pairs also depends on the geometry of the detector and the choice of the gas. Regarding the geometry, the most common are the parallel plates ionization chambers and the cylindrical ionization chambers [12]. The choice of the gas and its pressure is application dependent.

2.2.2 Ionization chambers used at CERN

The monitoring of the mixed radiation fields is important when performing High Energy Physics (HEP) experiments. In case of high energy accelerators like the LHC, the radiation fields consist of neutrons, charged hadrons and photons [13]. This is why it is important

to use detectors that respond to the different types of radiation without compromising the required sensitivity, according to the area and to the parameters that need to be monitored [14]. The detectors currently used at CERN for radiation monitoring of the work places are high pressure ionization chambers. These ion-chambers are also suitable for environmental radiation monitoring.

The characterization and the calibration of the Argon IG5-A20 and Hydrogen IG5-H20 filled high-pressure ionization chambers manufactured by Centronic Ltd [15], is performed at CERN using standard source generated photon and neutron fields. The selected chambers were characterized by simulating their response using the FLUKA software [16] [17]. These chambers have an active volume of 5000 cm^3 and a pressure of 20 bar.

Inside CERN's accelerator complex, simple and robust air-filled plastic chambers (PTW T32006) [18] are installed. These ionization chambers, that operate at atmospheric pressure, are used for the remote reading of the ambient dose equivalent rates inside the tunnels and the experimental caverns after the beam has been stopped. They measure the radiation that is emitted by the decay of the radionuclides induced during operation [19]. These air-filled detectors are made of polyethylene (PE) and have an active volume of 3079 cm^3. These devices have also been characterized using FLUKA simulations and experimental measurements at the CERN facilities [20].

Table 2.1 – Radiation Protection Ionization Chambers used at CERN

Monitor type	**Detector model**	**Radiation type**	**Detector type**	**Measurement range**
Area gamma monitor AGM	CENTRONIC IG5-A20	Photons, muons	High pressure Argon ionization chamber	50 nSv/h - 0.1 Sv/h
Area mixed field monitor AMF	CENTRONIC IG5-H20	High energy charged particles, neutrons and photons	High pressure Hydrogen ionization chamber	50 nSv/h - 0.1 Sv/h
Induced activity monitor IAM	PTW T32006	Photons	Air filled ionization chamber	1 μSv/h - 10 Sv/h

Table 2.1 presents the ionization chambers used at CERN and the radiation type that they are sensitive to. It also shows the requested measurement range. By using the typical conversion factor for each detector, the output current is calculated as shown in Table 2.2 [3], [21]. The input current requirements for the front-end electronics are determined by this table.

The readout electronics should be able to digitize input currents starting from 2 fA up to 250 nA. In extreme cases, due to the pulsed radiation fields the output current can reach a few μA.

Table 2.2 – Detector Types with Associated Conversion Factors and Derived Output Current Ranges [21]

Monitor type	Measurement range	Typical conversion factor [A/Sv/h]	Output current range
AGM	50 nSv/h - 0.1 Sv/h	γ: $1.6 \cdot 10^{-6}$	80 fA - 160 nA
AMF	50 nSv/h - 0.1 Sv/h	γ: $1.13 \cdot 10^{-7}$ n: $4 \cdot 10^{-8}$	5.7 fA - 11.3 nA 2 fA - 4 nA
IAM	1 μSv/h - 10 Sv/h	γ: $2.5 \cdot 10^{-8}$	25 fA - 250 nA

Table 2.3 – Readout Electronics Performance Requirements [21]

Parameter	Range / Value	Remark
Measurement range	2 fA to 5 μA	Input current range
Resolution	1 fA	Smallest change in the input current which causes change in the indication
Accuracy	± (1 fA + 5% of the reading)	Closeness of the agreement between the measurement and the conventionally true value of the measured quantity
Measurement time	100 ms for $I_{in} \geq 1$ pA >100 ms for $I_{in} < 1$ pA	Data acquisition time for current measurements
Operational temperature range	10°C to 40°C -15°C to 55°C	Inside temperature Outside temperature

The specifications for the new front-end electronics for radiation monitoring at CERN, are presented in Table 2.3. A single readout circuit is required for all detector types.

2.3 Evaluation of the Total Integrated Dose over Time

The radiation monitoring system has to evaluate the total ionizing radiation dose over time. This is possible by using charge sensitive amplifiers where the input current is integrated in a capacitor. Historically, in nuclear physics experiments, for example for ionizing radiation monitoring or when measuring electric charge for dosimetry, the most common and widely used approach is the Current to Frequency Converter (CFC).

The CFC is the best way to evaluate the total integrated dose in terms of linearity, simplicity and dynamic range. In a CFC, the input current is integrated using an integrator. The inte-

grator's output voltage V_{out} ramp slope varies according to the input current I_{in}. When that ramp voltage reaches a predetermined threshold V_{th} set by a comparator, the integrator's feedback capacitance C_f is discharged and the cycle repeats. Therefore, the output frequency of operation is proportional to the input current.

The circuit's operating frequency f is given by equation (2.1), where Q_{ref} is the reference charge that balances the operation.

$$f = \frac{I_{in}}{Q_{ref}} \tag{2.1}$$

The discharge of the feedback capacitance is possible by using a switch to short out the feedback capacitor. The approach of using a feedback switch S_1 for discharging the feedback capacitor C_f is presented in figure 2.3(a). After the comparator threshold V_{th} crossing, the one-shot produces a pulse that closes the switch S_1 and discharges the capacitor. The capacitor C_f loses a charge Q_{ref} equal to $C_f V_{th}$ and the cycle restarts. This approach has the disadvantages of charge loss and linearity error [22], [23]. The circuit is insensitive during the discharge-reset time because the integrating capacitor is shorted and the input current is not integrated. Additionally, the reset time t_{reset} has an effect on the linearity of the circuit since:

$$I_{in} = \frac{C_f V_{th}}{T - t_{reset}} \tag{2.2}$$

where T is the output period. From equation (2.2) it can be seen that the output frequency and the average input current are not proportional especially when the circuit operates at high frequencies.

An alternative method that has more advantages is based on the recycling integrator circuit through charge balancing, where the input current is continuously integrated and thus there is no charge lost [24], [25], [26], [27], [28] and [29]. When the integrator's output voltage reaches a threshold voltage V_{th}, a reference charge Q_{ref} is added to or subtracted from the input according to the input current polarity. A pulse is issued at the output every time the reference charge is injected. By pulse counting, the input ionization current can be measured.

Figures 2.3(b) and 2.3(c) present two different implementations of the CFC with charge balancing. The reference charge injected in the input can be realized using current sources or switched capacitors. In the first case, an accurate current I_{ref} is injected into the input for a precise time t_{ref}. In that case $Q_{ref} = I_{ref} t_{ref}$. In the second case, a capacitor C_{ref} is charged to a precise voltage V_{ref} and then is connected to the integrator's input so $Q_{ref} = C_{ref} V_{ref}$.

The current to frequency conversion through charge balancing is suitable for radiation mon-

itoring because the current integration is not interrupted, the input charge is not lost due to switching and the conversion depends only on the reference charge Q_{ref}. This method demonstrates good linearity and wide dynamic range [22].

2.4 State of the Art

The most recent developments for radiation monitoring for beam monitor chambers are based on the same principle of current to frequency conversion through charge balancing.

A family of multipurpose ASICs named TERA [30] has been developed by the Istituto Nazionale di Fisica Nucleare (INFN) and the University of Torino for the monitoring and control of hadron therapy beams. In the past years there have been many developments in many technologies starting from 1.2 μm CMOS [31] and 0.8 μm CMOS [32], [33], [34], with the most recent implemented in 0.35 μm technology [35], [36], [37], [38]. The ASICs are used to equip ionization chambers for medical treatment facilities. They are based on the current to frequency conversion and the recycling integrator principle. These 64-channel ASICs demonstrate a wide dynamic range. The measured background current has a mean value of 230 fA in TERA07 designed in 0.35 μm technology. The recently developed ASIC in 0.35 μm technology named TERA09, has extended the maximum current range up to 750 μA in order to comply with clinical pulsed particle beams [39], [40].

Another important development is an ASIC that was designed for CERN's beam loss monitoring (BLM) system. The BLM ASIC aims at digitizing current signals from ionization chambers and diamond detectors [41], [42], [43], [44]. It is a radiation tolerant 120-dB dynamic range incremental charge to digital converter. The conversion is performed using an adjustable temperature-compensated current reference in a 40 μs integration time window. This two-channel synchronous multi-ranging converter is implemented in a commercial 0.25 μm CMOS technology and is able to digitize bipolar input currents from a few pA after averaging, up to 1.05 mA.

Another ASIC for radiation monitoring was designed by the GSI Helmholtz Centre for Heavy Ion Research in AMS 0.35 μm technology [45]. This ASIC demonstrates a dynamic range of more than 7 decades without range switching. The operating principle again is based on the charge to frequency converter. The integrator's output voltage is continuously compared with a threshold voltage generated by a Digital to Analog Converter (DAC). The first version of the ASIC named QFW I, can measure currents from 1.6 pA up to 180 μA. The readout chip interfaces with Multi-Wire Proportional Chambers (MWPC) and other beam devices like Faraday-cups and ionization chambers [46], [47].

The aforementioned works and their upgrades, mostly aim at increasing the dynamic range at the upper end [38]. However, all these ASICs are limited at the lower end by the net input leakage currents. This is the reason why the lowest reported measurable current is limited to 194 fA for TERA06 [34] and -188 fA for BLM ASIC [41]. The specifications for the CERN's

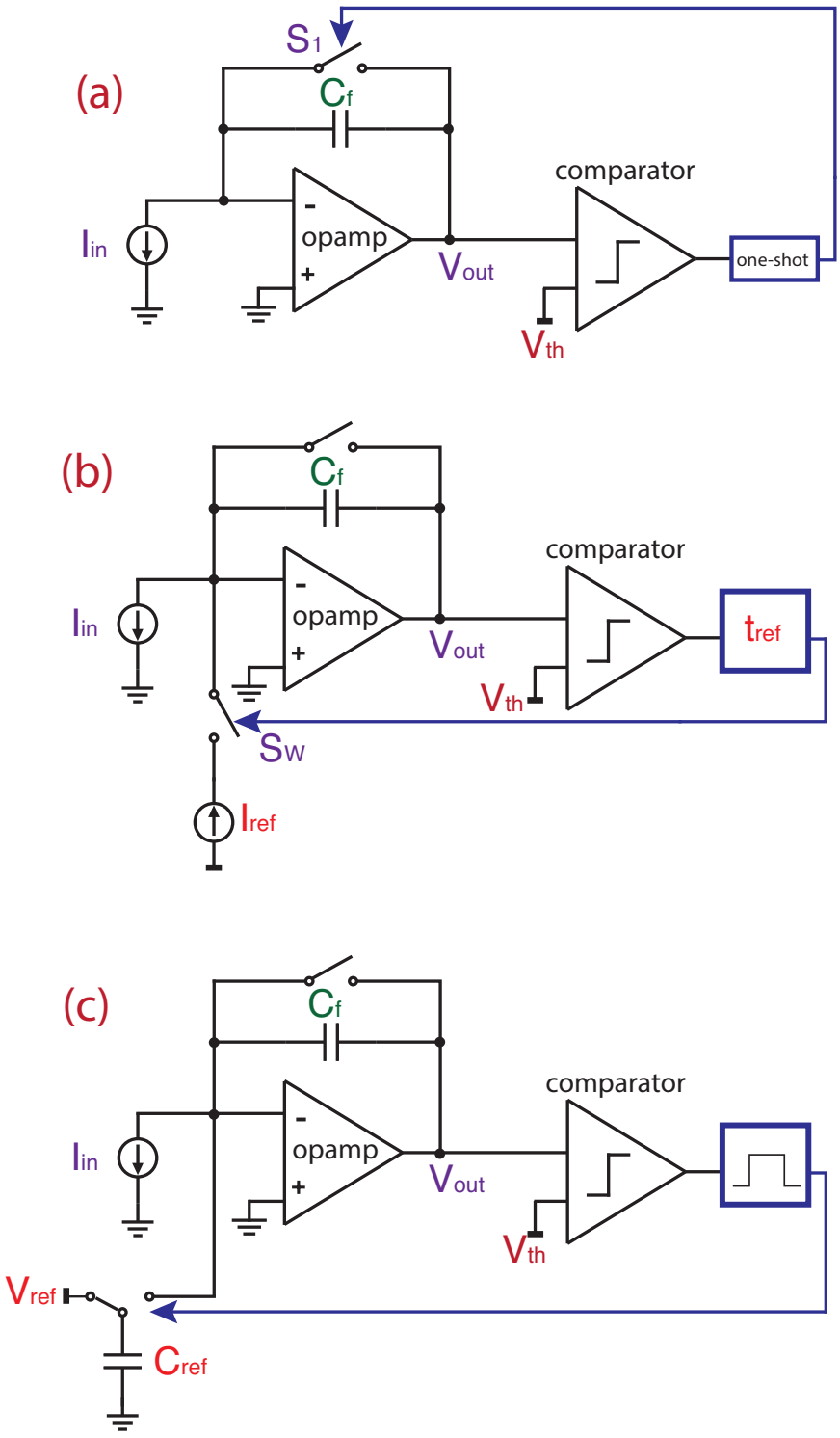

Figure 2.3 – (a) CFC with shorting switch, (b) CFC with charge balancing using a current source, (c) CFC with charge balancing using a switched capacitor

readout electronics require a minimum measurable current of 2 fA.

Table 2.4 summarizes the characteristics of these ASICs.

The commercial system currently used at CERN for radiation monitoring is built with COTS components. It is based on the current to frequency converter architecture where a feedback switch is shorting the input and the output to reset the integrator. The switched capacitor integrator currently used at CERN is the IVC 102 from Texas Instruments [48] which has a typical leakage current of 100 fA at 25°C.

Some other commercial ultra-low leakage amplifiers are available on the market [49], [50], [51].

2.5 Chapter Conclusions

Ultra-low current measurements are important for radiation monitoring when using ionization chambers. The output of the detector, especially when the natural background radiation is measured, is in the order of femtoamperes. The current to frequency converter topology can be used for the evaluation of the total ionizing radiation dose over time. The design of the readout circuit for radiation monitoring is challenging because of the dynamic range requirements, the linearity constraints and the leakage currents present at the input of the system.

The ASIC implementations presented in Table 2.4 are limited in the low range because of the leakage currents that are injected from various sources and are added to the input signal. The strict requirements for the background radiation monitoring at CERN require a digitizer that demonstrates better performance than the current state of the art. Currents as low as 2 fA should be digitized and measured.

Table 2.4 – Comparison among ASICs for Radiation Monitoring

Characteristics	**TERA06 [33], [34]**	**TERA09 [39], [40]**	**QFW I ASIC [45]**	**BLM ASIC [41]**
Publication Year	2004	2016	2004	2012
Technology	AMS 0.8 μm	AMS 0.35 μm	AMS 0.35 μm	IBM 0.25 μm
Die Size	6mm x 7mm	4.68mm x 5.8mm	3.28mm x 3.38mm	2.4mm x 3.775mm
Dynamic Range	5 decades	6 decades	1.60 pA to 180 μA	1 pA to 1.05 mA
Leakage Current	194 fA	2 pA	1.65 pA	-188 fA
Linearity Error	± 1%	±2%	± 1.5%	± 5%
Polarity	Unipolar	Bipolar	Unipolar	Bipolar
Clock Frequency	20 MHz	250 MHz	10 MHz	12.8 MHz

3 Evaluation of Leakage Current and Dynamic Range in a CFC Architecture

3.1 Introduction

The scope of this chapter is to discuss the main limitations when measuring ultra-low currents, namely the leakage currents in the input of the system. The signal to be measured is comparable to the sum of the leakage currents in the input of the circuit. A basic Current to Frequency Converter (CFC) architecture is presented and the related leakage current contribution is evaluated. The proposed technologies are theoretically compared in terms of leakage current and the selected technology AMS 0.35 μm, is verified experimentally by building a demonstrator that allows to measure the different potential sources of leakage currents in the input of the measuring system.

A set of guidelines that can be followed in order to minimize or compensate for the leakage currents is established. These guidelines were not specifically outlined or followed in the previous designs of radiation monitoring systems. The main principles may, however, be used in any similar application that aims at measuring femtoampere currents.

3.2 Operating Principle of a Current to Frequency Converter

The front-end electronics that interface with radiation detectors have to digitize the generated current over a wide dynamic range. The simple CFC topology that is depicted in figure 3.1, is based on the recycling integrator scheme and charge balancing. The integrator is continuously integrating without inflicting any dead time. The current I_{det} that is generated from the current source, in this case the radiation detector, is integrated along with the sum of the leakage currents I_{leak} in a capacitor C_f and the output voltage V_{out} of the integrator is compared with a voltage threshold V_{th}. When the discriminator triggers, a fixed amount of charge Q_{ref} is injected into the input through a discharging circuit to discharge the C_f and balance the accumulated charge. Additionally, a pulse is issued at the output. The injected reference charge Q_{ref} sets the gain of the conversion. By counting how many times N_{counts} the reference charge Q_{ref} is injected in a measuring time window T_w, the total input current

I_{in} can be calculated using equation (3.1):

$$I_{in} = \frac{N_{counts} Q_{ref}}{T_w} \tag{3.1}$$

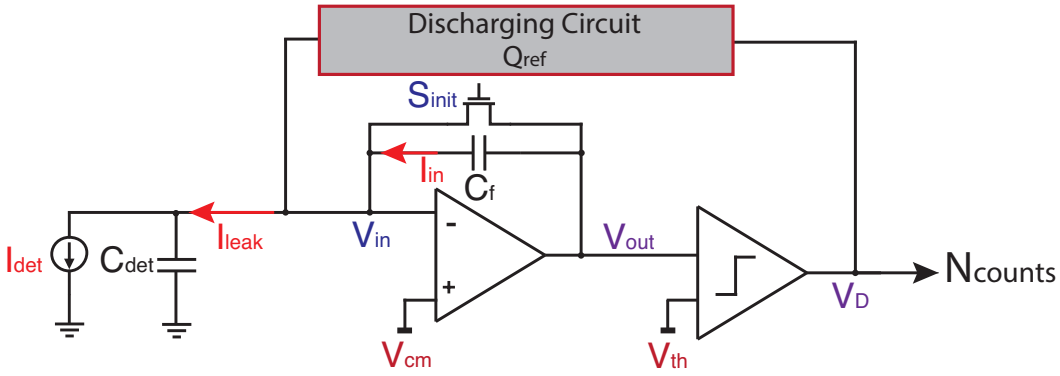

Figure 3.1 – Simple Current to Frequency Converter (CFC) scheme

3.3 Leakage Currents in the Input of the System

The total current I_{in} in the input of the system consists of the current signal from the detector I_{det}, and the sum of all leakage currents that are also injected into the input from various sources. The potential leakage current sources in the input of the integrator, which is the basic structure in the selected system architecture, are depicted in figure 3.2. The net leakage includes the intrinsic leakage related to the chip, but also the leakage that is related to the testbench and the laboratory setup. The leakage related to the chip is dominated by the leakage of the switches (1) $I_{leak\_switches}$ that are connected to the input and the leakage of the Electrostatic Discharge (ESD) protection diodes (2) I_{leak_ESD}. On top of that, the leakage of the package (3) $I_{leak\_package}$, the leakage of the Printed Circuit Board (PCB) (4) I_{leak_PCB}, the leakage of the cable and the connector (5) I_{leak_cable} and finally the leakage of the detector (6) $I_{leak\_detector}$ should be added as shown in equation (3.2). It should be noted that any contamination with dust or other conductive means close to the signal traces could induce stray leakage current.

$$I_{in} = I_{det} + I_{leak\_detector} + I_{leak\_cable} + I_{leak\_PCB} + I_{leak\_package} + I_{leak\_ESD} + I_{leak\_switches} \tag{3.2}$$

One of the major challenges in the design of the front-end electronics for radiation monitoring is the leakage current suppression. Depending on the detector's output signal, the net leakage seen in the input of the front-end is comparable or in some cases higher than the ion-current

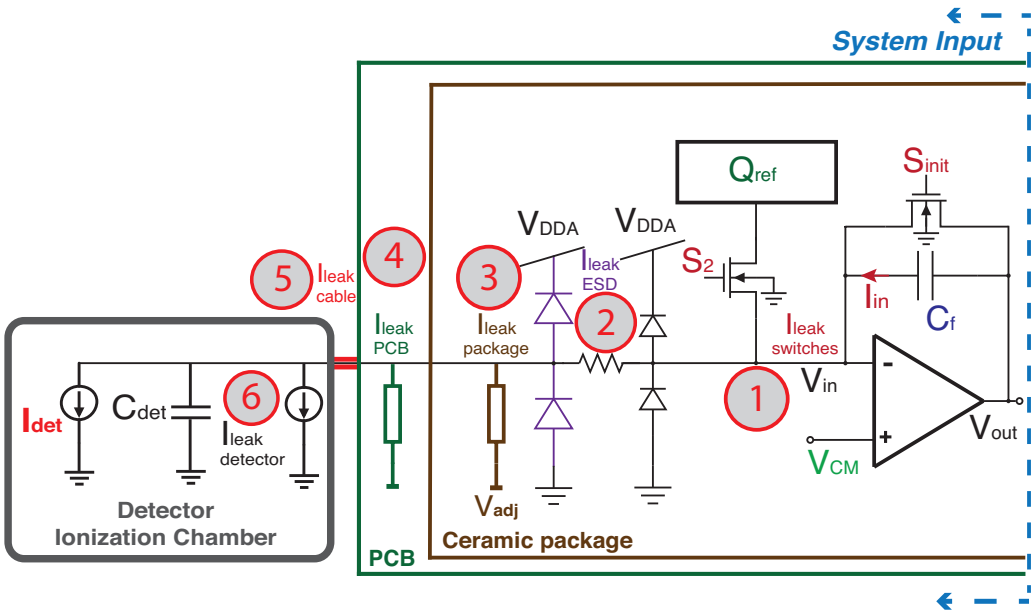

Figure 3.2 – Potential leakage current sources in the input of the integrator

generated from the detector. This is the limiting case for CERN's ionization chambers that can have an output current starting from a few femtoamperes. The various leakage current sources shown in figure 3.2 are analyzed in this section.

3.3.1 Leakage current of the switches

The leakage of the switches $I_{leak\_switches}$ that are connected to the input can be estimated by studying the leakage current mechanisms for a single MOS device in the OFF-state. A detailed analysis of the leakage current sources in CMOS technologies is presented in [52], [53], [54]. The leakage current mechanisms for an nMOS transistor are depicted in figure 3.3 and namely are the reverse bias p-n junction leakage I_1, the subthreshold leakage I_2 and the oxide tunneling gate leakage current I_3. There are also the secondary leakage mechanisms like the Gate-Induced Drain Leakage (GIDL) I_4 and the channel punchthrough current I_5.

The total OFF-state current can be generally grouped into two categories, the source to drain current and the substrate current. The source to drain includes the subthreshold current I_2 and the punchthrough current I_5 and the substrate current includes the conventional p-n junction leakage I_1 and the GIDL I_4.

In [55], the drain and bulk current components are simulated and plotted as a function of the gate voltage for the technologies 0.35 μm, 0.18 μm and 0.13 μm. For the sake of clarity these plots taken from that article, are also reproduced with permission and shown in figures 3.4 and 3.5.

These technologies will be considered and compared in terms of leakage currents in order to

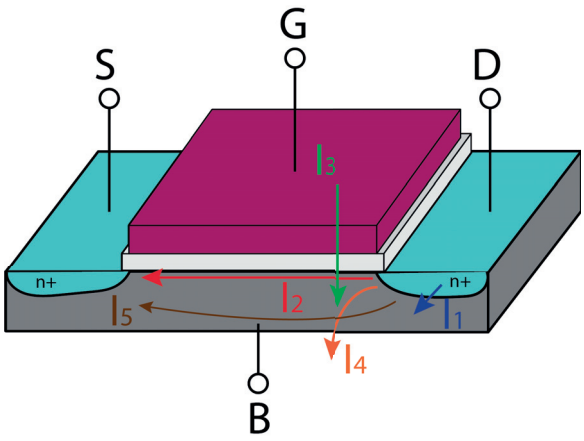

Figure 3.3 – Leakage current mechanisms in an nMOS transistor

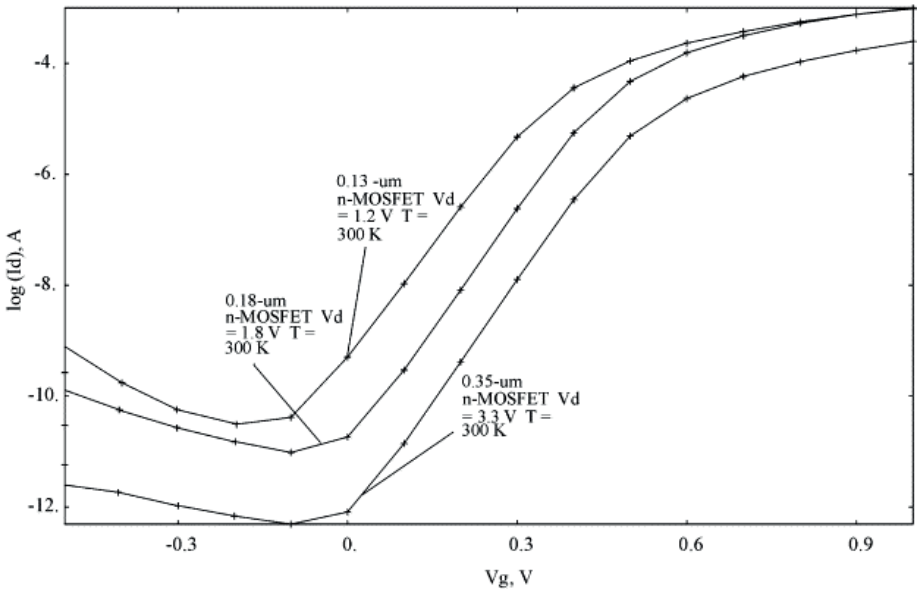

Figure 3.4 – Drain current versus gate voltage for different CMOS technologies ($T = 300K$, drain voltage has the nominal value for the given technology). Reproduced with permission from [55]

find the most suitable technology for our application. In the considered technologies, the two dominant contributors are the reverse diode leakage I_1 and the subthreshold leakage I_2.

Regarding the transistor's leakage mechanisms, the reverse biased drain and source to well junctions, cause a leakage current I_1 that is a function of the junction geometry area and perimeter and the physical parameters of the semiconductor material like doping concentration [56]. The I_1 has two main components, the minority carrier diffusion/drift near the edge of the depletion region and the leakage due to electron-hole pair generation [52], [57].

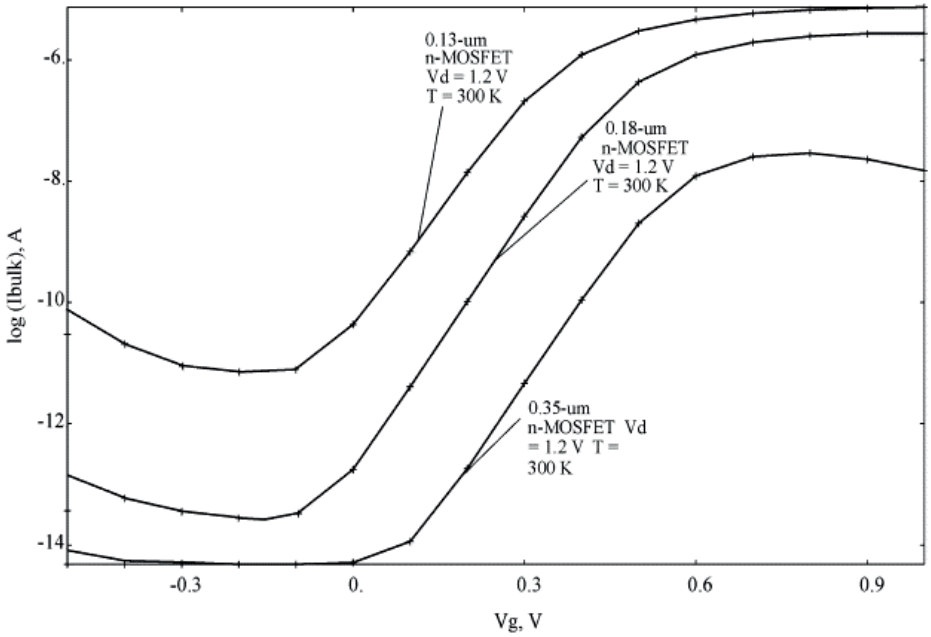

Figure 3.5 – Bulk (substrate) current versus gate voltage for different CMOS technologies ($T = 300K$, V_D=1.2 V). Reproduced with permission from [55]

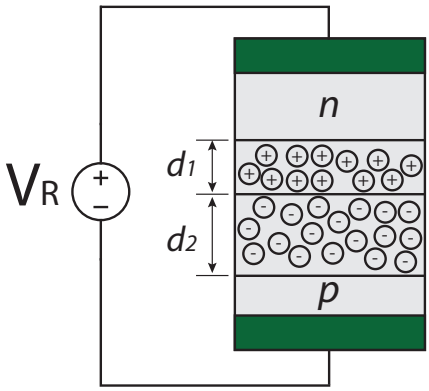

Figure 3.6 – p-n junction with reverse bias

The physical mechanism of the p-n junction, that is shown in figure 3.6 under reverse biasing, is important in order to understand the effects of reverse bias voltage and temperature on the leakage current. If a reverse bias $V_R > 0$ is applied from the n terminal to the p terminal, the electrostatic potential across the depletion region will increase by V_R. This leads the depletion region to widen more than in the zero bias, since the reverse biasing moves the electrons upward away from the upper edge of the depletion region and the holes downward away from the lower edge of the region. More impurity atoms are uncovered that contribute to a larger electric field [58]. However, although the polarity of the reverse bias does not help the flow of the majority carriers, a small junction leakage current does flow because some of the minority

carriers near the depletion region of the n side are swept down by the field. Equivalently, some of the electrons near the depletion region edge of the p side are swept upwards by the field. A net external leakage current flows. In reality the reverse bias current is higher than the theoretical model, since other phenomena, like the electron-hole pair thermal generation in the depletion region, make the reverse current magnitude larger [59].

It should be noted, that the diode reverse leakage current I_1 is highly affected by temperature and can double for every 10°C or even less of temperature change [58].

As the CMOS devices are scaled down to increase their performance and to achieve lower power consumption, the supply voltage V_{DD} and also the threshold voltage V_{T0} are scaled. The ion implantation for lowering the threshold voltage of modern CMOS devices has a dramatic effect on the subthreshold or weak inversion leakage current I_2 [54], [60], [61].

The subthreshold current between source and drain occurs when the gate voltage V_G is smaller than the threshold voltage V_{T0} [58], [62]. In the weak inversion, although the drift component of the subthreshold current is negligible, the subthreshold conduction is dominated by the diffusion current. The carriers move by diffusion along the surface similarly to the charge moving across the bipolar transistor's base [62].

The analytical MOS transistor model valid in all regions of operation [63] and details on the weak inversion operation can be found in [64].

The drain current I_D for an nMOS transistor in weak inversion according to the EKV model [64] is given by equation (3.3)

$$I_D = I_{spec} exp\frac{V_G - V_{T0}}{nU_T}\left(exp\frac{-V_S}{U_T} - exp\frac{-V_D}{U_T}\right), \quad IC \ll 1 \tag{3.3}$$

where I_{spec} is the specific current of the transistor, V_G is the gate voltage, V_{T0} is the threshold voltage, n is the slope factor, U_T is the thermal voltage and V_S and V_D are the source and the drain voltages respectively. According to the EKV model, the level of inversion of the transistor can be characterized by an inversion coefficient IC. When the transistor operates in the weak inversion, the condition $IC \ll 1$ holds.

The specific current I_{spec} is defined as:

$$I_{spec} = 2n\mu C_{ox}\frac{W}{L}U_T^2 = 2n\beta U_T^2 \tag{3.4}$$

where β is the transfer parameter that depends on the width W and the length L ratio of the channel, μ is the equivalent mobility of electrons in the channel and C_{ox} is the gate oxide

capacitance per unit area. The thermal voltage U_T is defined as:

$$U_T = \frac{kT}{q} \tag{3.5}$$

where k is the Boltzmann constant, q is the elementary charge and T is the absolute temperature.

The first and the second term in the parentheses of the equation (3.3) are the distinctive parts of the forward current I_F and the reverse current I_R [62], [64].

The equation (3.3) for V_{GB}=0 and $V_D >> V_S$ gives the residual current of the transistors in the OFF-state.

$$I_{D0} = I_{spec} exp\frac{-V_{T0}}{nU_T} \cdot exp\frac{-V_S}{U_T} = I_{spec} exp\frac{-(V_{T0} + nV_S)}{nU_T} \tag{3.6}$$

For the technologies of interest, the subthreshold leakage current is the dominant leakage source for a single device. One method that can be used in order to decrease that subthreshold leakage current is to drive the gate G to a voltage outside the existing rail voltages so that $V_{GB} < 0$. In that case, the complete available weak inversion range can be exploited down to the diffusion diodes' reverse leakage [60].

A better alternative to this strategy is the source shifting technique as explained in [60], [61], [65], [66], [67], [68], where the subthreshold current can be reduced by increasing the source to body biasing V_{SB} by connecting the source to a different potential relative to the bulk as shown in figure 3.7. That way, the subthreshold leakage current I_{D0} decreases as shown in equation (3.6).

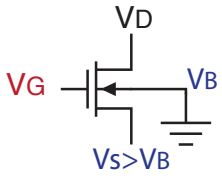

Figure 3.7 – Source shifting in an nMOS switch

A simulation of the source shifting technique is depicted in figure 3.8 for a minimum size nMOS switch in AMS 0.35 μm technology. The simulated nMOS transistor has W= 0.6 μm and L= 0.35 μm and the I_D is plotted as a function of V_G for different source voltages starting from 0 V and sweeping up to 1.5 V. The drain voltage is at 1.65 V. As the V_{SB} increases, the

subthreshold leakage current decreases when $V_G = 0$.

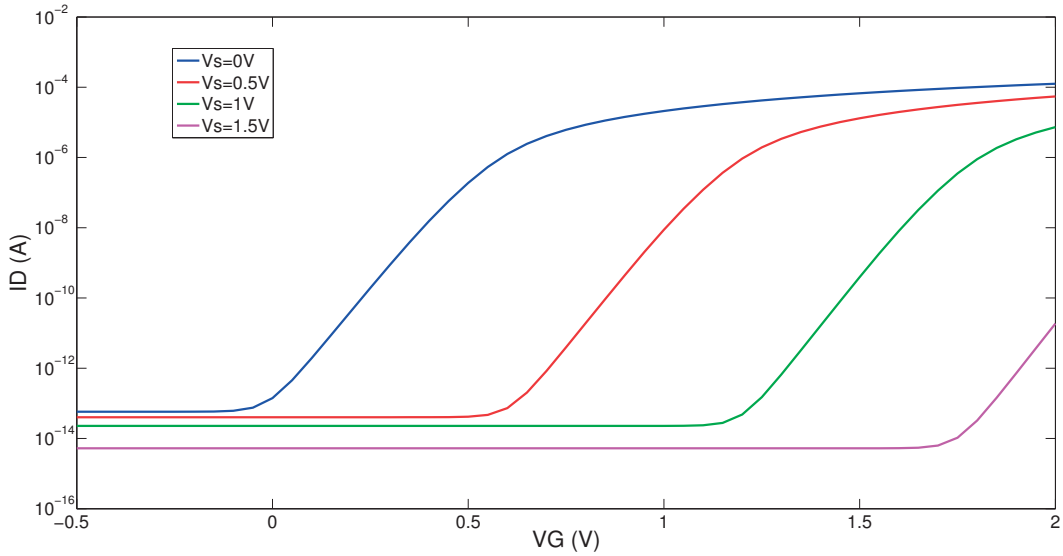

Figure 3.8 – Simulation of the drain current versus gate voltage for different V_S for a minimum size switch in AMS 0.35 μm technology

The subthreshold leakage current can be also minimized by keeping the V_{DS} voltage as small as possible, since for small V_{DS}, i.e. $V_{DS} < U_T$, the I_{D0} is given by equation (3.7):

$$I_{D0} = I_{spec} exp \frac{-(V_{T0} + nV_S)}{nU_T} \frac{V_{DS}}{U_T} \tag{3.7}$$

The switches that are connected to the input can operate at or close to $V_{DS} = 0$ in the OFF-state whenever this is possible.

The subthreshold leakage current of the switches is also a temperature dependent parameter and it is reduced with cooling, mainly due to the increase of the threshold voltage V_{T0} [69], [70].

Another leakage current mechanism for the transistor is the oxide tunneling current I_3. Again, the technologies of 0.35 μm, 0.18 μm and 0.13 μm will be considered. The 0.35 μm technology has a relatively thick gate oxide ($T_{ox} = 7.5$ nm) compared to the 0.18 μm and 0.13 μm technologies, so the oxide tunneling current is not significant [71]. The assumption that the gate leakage current is typically very small compared to the subthreshold leakage holds for process technologies with T_{ox} of at least 2 nm. On the other hand, in recent scaled technologies, although the subthreshold leakage rises by a factor of 5x per generation, the 30% thinner oxide in each new process leads to around 1000x rise in gate tunneling leakage I_3 [53].

Finally, the secondary leakage currents related to the gate-induced drain leakage I_4 and

channel punchthrough current I_5, are insignificant compared to the subthreshold leakage I_2 for the technologies of interest [54], [55]. They are beyond the scope of this research that focuses on measuring femtoamperes and won't be analyzed further.

It should be noted that the front-end electronics are not supposed to be irradiated. Radiation hardness therefore was not required by the specifications since the system will be used for background radiation monitoring and radiation protection. During calibration or in high radiation cases, the electronics will be protected and connected to the detector with a cable.

As a general conclusion, the leakage currents present in a single device, increase with technology scaling and can be reduced with cooling.

3.3.2 Leakage of the electrostatic discharge (ESD) protection diodes I_{leak_ESD}

An Electrostatic Discharge (ESD) event occurs when static high voltage is accidentally applied across the pins of an ASIC. The externally accessible transistor gates should be protected. The simplest structure that is used to prevent an electrostatic discharge is a resistor and two reverse-biased p-n junctions as shown in figure 3.9. The ESD protection clamps the external discharge to ground or V_{DD} limiting the potential applied to the circuit. The resistor is used in order to limit the breakdown current. The I/O cells that include the ESD protections are available from the foundries as standard cells [72].

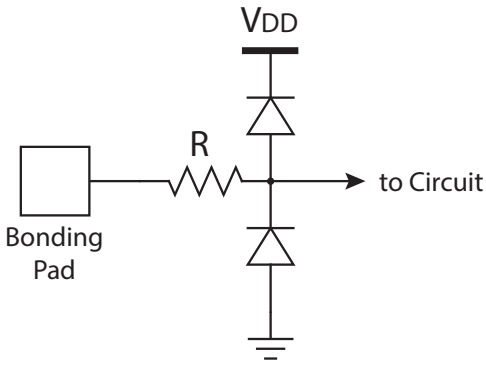

Figure 3.9 – Simple Electrostatic Discharge (ESD) protection circuit

The reverse biased p-n junctions leakage current is expected to be one of the most critical leakage current sources in the input of the system. Additionally, the temperature dependence of the p-n diodes is important since the leakage is strongly affected by changes in temperature.

3.3.3 Extrinsic leakage current sources

The leakage of the package $I_{leak\_package}$ that encapsulates the ASIC, the leakage of the printed circuit board (PCB) I_{leak_PCB} that hosts the package, the leakage of the cable and the connector I_{leak_cable} that joins the measuring system to the detector and finally the leakage of the

detector $I_{leak\_detector}$ itself are added and disturb the accurate measurement of the signal. Even if the intrinsic leakage current of the ASIC is minimized, at the femtoampere level, the resistivity of the materials that are used for the system level design becomes important. In general, high resistance insulation is a prerequisite for ultra-low current measurements, since leakage currents can be generated by the existence of stray resistive paths between the measuring circuit and adjacent voltage sources. The volume resistivity for some materials used as insulators is shown in Table 3.1 [73].

Table 3.1 – Volume Resistivity of Various Insulating Materials [73]

Material	Volume Resistivity (Ohm x cm)
Sapphire	$> 10^{18}$
Teflon PTFE	$> 10^{18}$
Polyethylene	10^{16}
Polystyrene	$> 10^{16}$
Ceramic	10^{14} - 10^{15}
Glass Epoxy	10^{13}

The choice of the device package is important since the adjacent signals influence the leakage current in the input node [74]. Guards around the input pads can potentially prevent external leakage currents from reaching the sensitive input node. The principle of guarding is based on the fact that the low impedance point, that is nearly at the same potential as the high impedance nodes, can absorb the external leakage currents.

The guarding concept can be extended to the cables and the connectors. The coaxial cables and connectors consist of the central conductor and the shield. However, the triaxial cables and connectors also include a second shield around the first that can be connected to a guard voltage to minimize the leakage current and to close the common mode path for ambient noise.

3.4 A Demonstrator Chip for Evaluation of the Leakage Currents

A demonstrator ASIC named Ultra-low Picoammeter 1 (Utopia 1) was built to evaluate each leakage current source present at the input of the CFC. This chip will demonstrate the lowest possible current that can be measured based on the current to frequency converter operating principle.

3.4.1 Technology selection

A low leakage current technology should be selected for the design of the ASIC. As explained previously, after the drain and bulk leakage currents comparison among the 0.35 μm, 0.18 μm and 0.13 μm technologies (figures 3.4 and 3.5), the 0.35 μm technology demonstrates lower leakage current compared to the other standard technologies that were considered. This is

the main reason why AMS 0.35 μm CMOS C35B4C3 4M/2P/HR/5V technology was chosen to be used in this design. The principle application is environmental background radiation and radiation protection monitoring. The chip is not supposed to operate in high radiation environments and radiation hardness is not required from the specifications.

3.4.2 Architecture of the Utopia 1 ASIC

Figure 3.10 presents the architecture of one channel of the Utopia 1 ASIC and the potential leakage current sources. The design is based on the recycling integrator current to digital converter topology. It is a single range implementation designed to accept negative polarity input currents. This is related to the biasing of the detector and its expected ion-current polarity. However, should the polarity of the leakage current become positive, it can be measured indirectly by injecting a small negative current into the input through an accurate instrument and by observing the perturbation from the expected value [24]. The ASIC has four channels designed with minor variations. The first three channels are synchronous and the fourth channel can operate either synchronously or asynchronously. A microscopic picture of the ASIC is shown in figure 3.11.

The integrator is a two-stage Miller amplifier with wide pMOS transistors input differential pair for lower $1/f$ noise. The GBW= 127 MHz, the phase margin ϕ= 62° and the open loop gain A_0 = 86 dB. The Miller compensation capacitor C_c= 2 pF and the feedback capacitor C_f= 1 pF.

The discriminator was designed with internal positive feedback. The discharging circuit that is used for the reference charge balancing is based on a stray insensitive switched capacitor circuit [75]. The reference capacitor C_{ref} was selected to be 1 pF. The reference voltage that the switched capacitor is charged to is V_{ref}= V_{charge}-V_{cm}= 1 V. So the reference charge is Q_{ref} = 1 pC. The switches of the switched capacitor circuit are managed with non-overlapping clocks (NOC) that guarantee that the reference charge is not lost [76].

A data acquisition (DAQ) system based on Spartan-6 LX9 MicroBoard [77] and NI LabVIEW software was developed and connected to the digital output V_{D_out} of the ASIC. The external digital logic circuit counts the number of reference charge injections N_{counts} in a measuring time window T_w according to equation (3.8).

$$N_{counts} = \frac{I_{in} T_w}{Q_{ref}} \tag{3.8}$$

For a fixed current, the respective number of counts N_{counts} depends only on the reference charge Q_{ref} and the measuring time window T_w. In a single range implementation like in the current chip, the Q_{ref} should be selected as a compromise to satisfy both the low (fA) and the high current (μA) requirements and be able to cope with the input currents of interest [78]. A

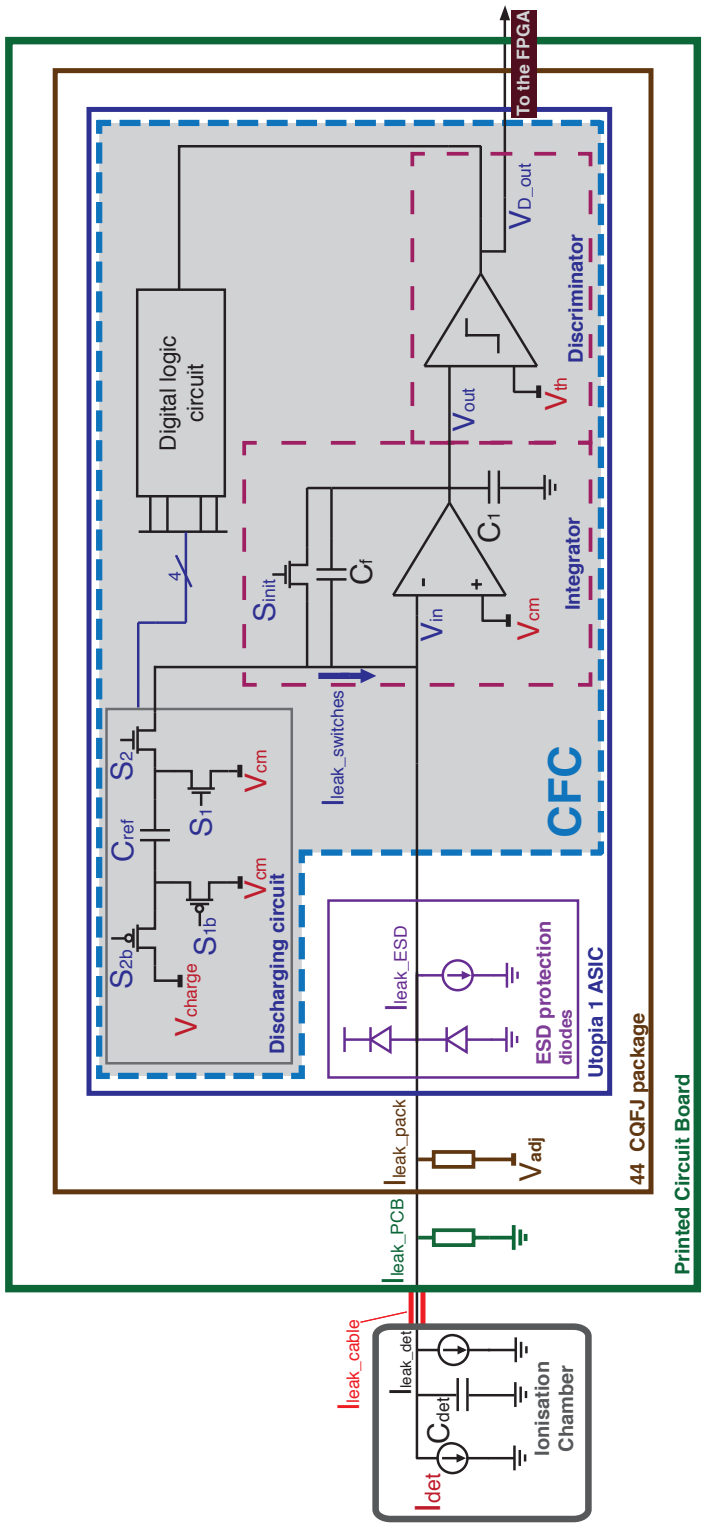

Figure 3.10 – Architecture of the system and potential leakage current sources

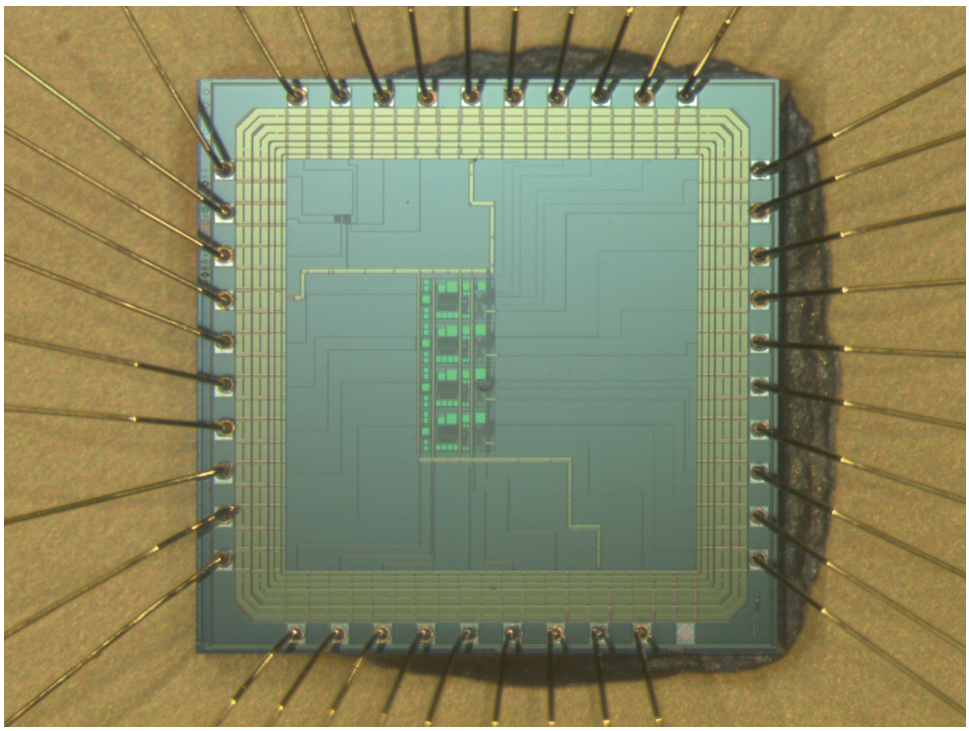

Figure 3.11 – Microscopic picture of Utopia 1 ASIC

multiple range implementation was beyond the scope of this prototype. If Q_{ref}= 1 pC and the measuring time window T_w is 100 ms, then the minimum current I_{min} that corresponds to the least significant bit (LSB) step of the digitizer is given by equation (3.9):

$$I_{min} = \frac{Q_{ref}}{T_w} = \frac{1pC}{100ms} = 10pA \tag{3.9}$$

However, this is not a hard limit, because if the measurement time is increased above 100 ms, lower currents can be integrated and measured. Equivalently, multiple T_w can be added together in order to increase the resolution and provide a non-zero count, since the input charge is accumulated in C_f until the integrator's output reaches the threshold voltage V_{th} that is set by the discriminator [79].

On the other hand, the maximum current I_{max} that can be measured using the CFC can be calculated by equation (3.10):

$$I_{max} = \frac{Q_{ref}}{t_{charge} + t_{discharge}} \tag{3.10}$$

where t_{charge}+$t_{discharge}$= t_{cycle} are respectively the charging and discharging times of the switched capacitor circuit.

The charging and discharging times of the discharging circuit can be either provided from a clock or from a monostable. In the first case the discharge occurs in the next rising edge of the clock after the discriminator's threshold is crossed, whereas in the second case the discharge is level triggered.

If the clock frequency is f_{clk}= 10 MHz then t_{charge}+ $t_{discharge}$= 200 ns and for Q_{ref}= 1 pC, the maximum possible measurable current is 5 μA.

The summary of the front-end characteristics is shown in Table 3.2. It should be noted that this prototype was not optimized for low power consumption since its purpose was to evaluate the leakage currents in the input of the integrator.

Table 3.2 – Summary of Utopia 1 ASIC Characteristics

Technology	AMS 0.35 μm
Power Supply	3.3 V
Power Consumption	50.16 mW
Clock Frequency	10 MHz
Die Size	2.6 mm x 2.6 mm
Polarity	Negative
Number of Channels	4
Gain A_0	86 dB
GBW	127 MHz
Phase margin ϕ	62 deg
C_f	1 pF
C_c	2 pF
C_{ref}	1 pF
Q_{ref}	1 pC
V_{ref}	1 V
V_{charge}	2.5 V
V_{cm}	1.5 V
V_{th}	2.5 V

3.4.3 Design variations for leakage current measurement

As shown in figure 3.12, four channels were implemented to test different variants and to measure independently the contribution of each leakage current source [80]. The variations among the reference channel CH1 and channels CH2, CH3 and CH4 are marked as a), b) and c) as seen in figure 3.13. The voltages V_{cm}, V_{charge} and V_{th} and the initialization signal S_{init} are common for all the channels and can be provided externally. The clock can be provided either by an on-board oscillator, which in this case is 10 MHz, or by an external source.

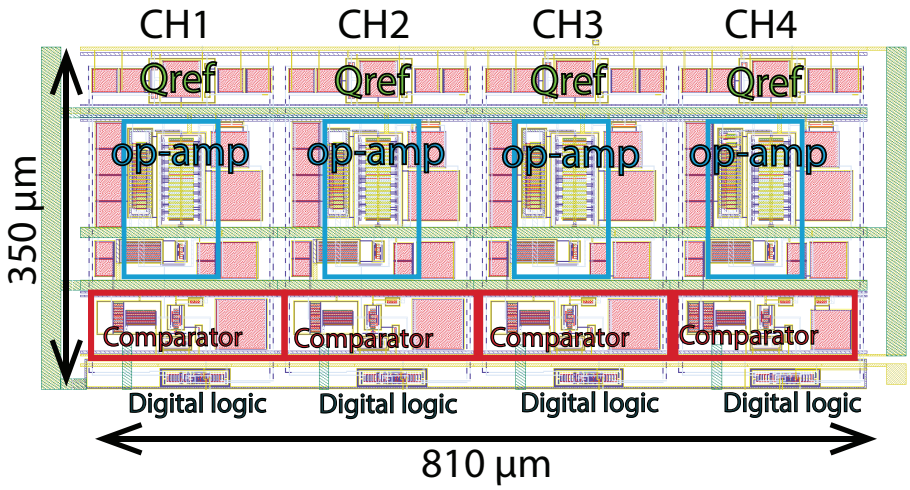

Figure 3.12 – Layout of the core of Utopia 1 ASIC

Briefly, CH1 is used as the reference channel and was implemented using the standard ESD protection pad. The ESD protection of CH2 was modified and the upper diode of the standard library cells was removed as can be seen in variation b) of figure 3.13. This was intentionally done to estimate the effect of the ESD protection leakage current. CH3 has normal ESD protection, but an nMOS switch was put in the input as seen in a), in order to isolate the external sources of leakage i.e. the diodes and the package from the integrator's input. This is how the subthreshold leakage current of the switches can be measured. Finally, CH4 has the same input structure as CH1 but different adjacent pins (as seen in c)). The external leakage current due to the package and the adjacent pins' voltages can be measured with this channel.

3.5 Leakage Current Measurements

In order to identify each leakage current source, multiple measurements were performed with the four channels of the ASIC in different steps. The leakage current can be measured directly when the input is kept open. The following measurements were performed inside a climatic chamber, where the temperature and the humidity were controlled. In general the leakage currents increase with temperature increase, so cooling down the whole system will reduce leakages and relax the requirements for long term stability. Since fA measurements are very delicate, the testbench was carefully designed and the testing PCB was put inside a metal box

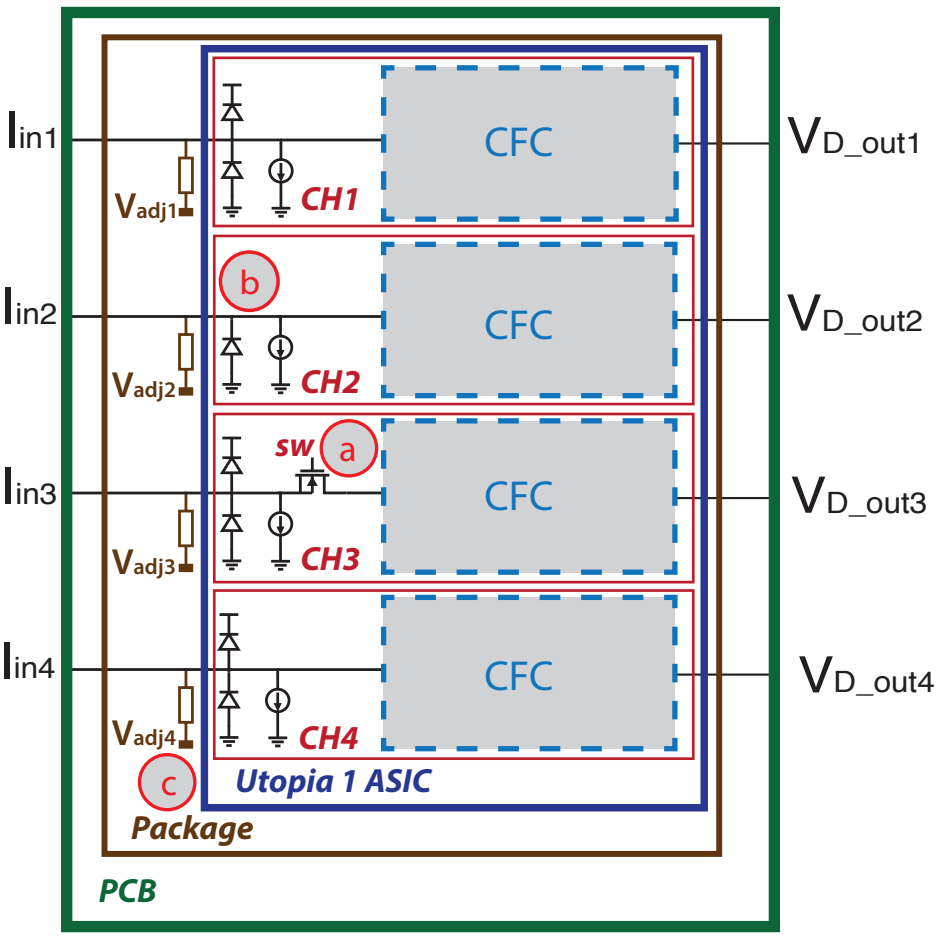

Figure 3.13 – Block diagram of the four channels of Utopia 1 ASIC

to be shielded from external interference.

3.5.1 Input switch leakage current measurement

As explained previously regarding the transistor leakage mechanisms, the dominant leakage current source of a transistor in the OFF-state, is the weak inversion subthreshold leakage current. In design level, for decreasing the subthreshold leakage $I_{leak\_switches}$ of the switches S_2 and S_{init} that are connected to the input, the source shifting technique was used. The common mode voltage V_{cm} of the amplifier was set to a different potential relative to the ground that is V_{cm}= 1.5 V. This allows the indirect control of the source voltage of the nMOS switches that are connected to the V_{in} node.

In order to estimate the leakage current related to the input switches, CH3 is identical to CH1 but there is also another minimum size switch S_W in the input as shown in figure 3.14. If the nMOS switch in the input of CH3 remains open, the integrator's input is disconnected

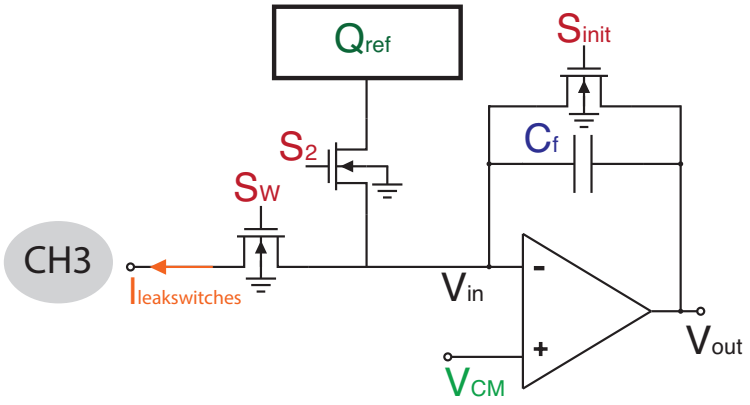

Figure 3.14 – Input of CH3 of Utopia 1 ASIC

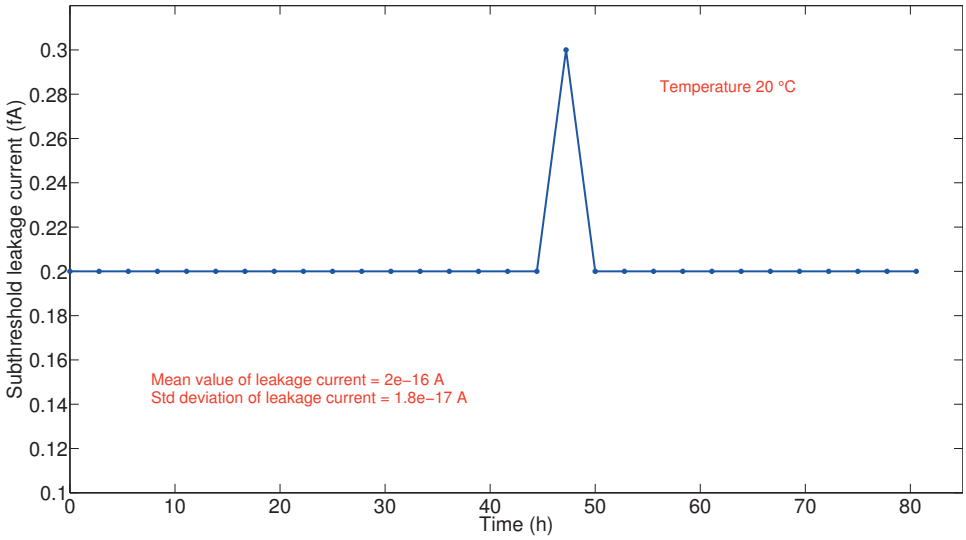

Figure 3.15 – Subthreshold leakage of switches S_W, S_{init} and S_2 when measuring CH3

from the PCB, the package and the ESD protection diodes. The remaining current in the input named $I_{leak\_switches}$ is basically dominated by the sum of the subthreshold leakage current of the switches S_W, S_{init} and S_2 and the p-n junction leakage of these transistors.

As depicted in figure 3.15, the $I_{leak\_switches}$ of CH3 was measured at a constant temperature of 20°C and its mean value was below 1 fA with a long acquisition time of 82 hours. The measured current was negative, but all the presented plots in this chapter are shown without the negative polarity sign.

This experiment verifies the hypothesis that the source shifting method can limit the subthreshold leakage current considerably.

3.5.2 ESD protection leakage current measurement

In order to measure the effect of the protection diode related leakage, CH2 was implemented as shown in figure 3.16.

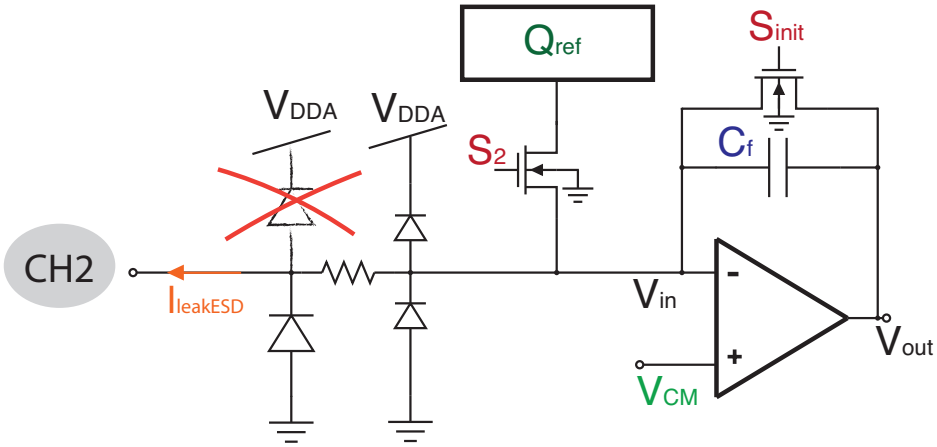

Figure 3.16 – Input of CH2 of Utopia 1 ASIC

The upper diode of a standard pad, that is connected to the positive power supply was removed. Then the leakage currents of the two channels CH1 and CH2 were measured at the same temperature and with the same V_{cm} value. The measured values are plotted and compared in figure 3.17 as a function of time. In both cases the leakage current is in the order of hundreds of femtoamperes and the difference due to the different ESD protection structures is evident.

For CH1 the bottom diodes leak more compared to the upper for the selected V_{cm} and the mean value of the whole structure is 30 fA. For CH2, the leakage current over time has a mean value of 80 fA and is related to the bottom ESD protection diodes. The measured current has negative polarity.

CH1 that has the standard ESD protection exhibited leakage current of different polarity according to the selected V_{cm} value. The difference in the leakage current according to the selected V_{cm} can be observed in figure 3.18, where the leakage current of CH1 at 10°C is plotted as a function of V_{cm}. The V_{charge} was changed accordingly in order to maintain the same V_{ref}= 1 V and the same reference charge Q_{ref}. When the V_{cm} was set below 1.55 V, the measured current changed polarity. When it changed polarity the analog output was saturated to the negative power supply rails. In figure 3.18, as in all the figures presented in this chapter, the negative leakage current is plotted with its absolute value.

On the other hand, CH2 exhibited only negative leakage current that could be directly measured with the CFC. The measured leakage current values were stored and can be used for compensation when currents are injected by a laboratory instrument.

The fact that the total leakage current in a channel with normal ESD protection is affected by a change in the V_{cm} can be used to find a proper V_{cm} value at which there is no net leakage

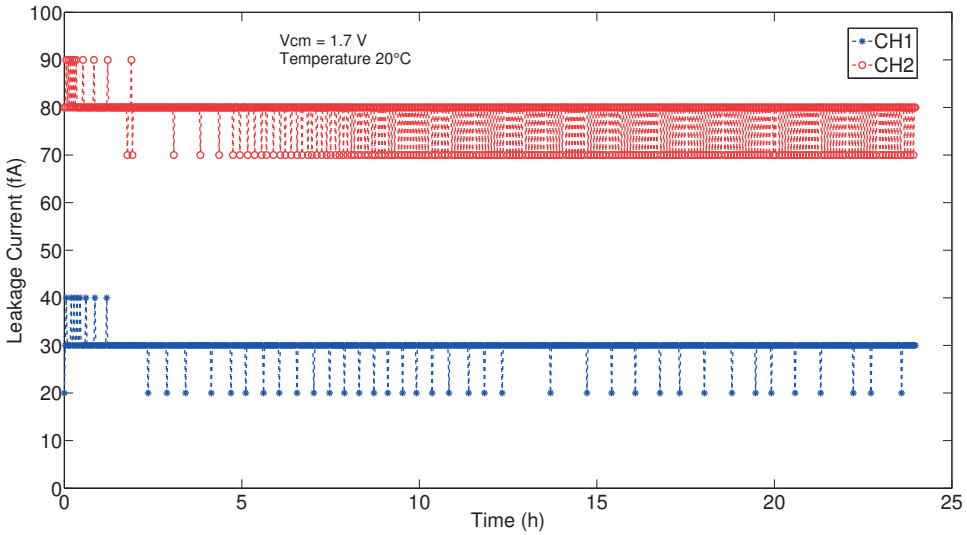

Figure 3.17 – Absolute value of the leakage current of CH1 and CH2 as a function of time measured at the same temperature and with the same V_{cm} (negative polarity)

current (that in this case was V_{cm}= 1.58 V). Another way to do that is to keep the same V_{cm} voltage, but use an independent power supply for the ESD protection of the input pads that could be trimmed in order to compensate the net leakage current. However, fine tuning is difficult to achieve and since the leakage current depends also on temperature, a system design based on net leakage current compensation looks more appealing for this application.

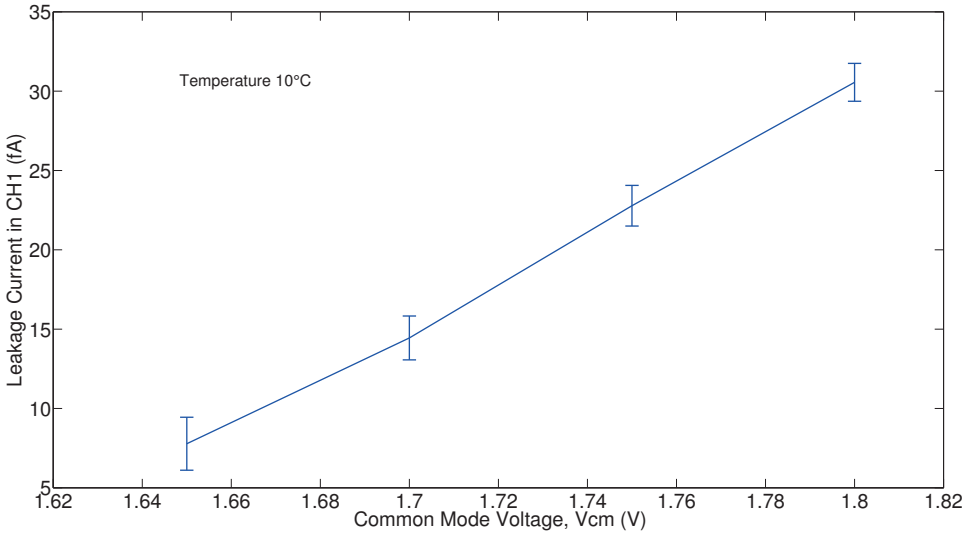

Figure 3.18 – Mean value of leakage current of CH1 versus common mode voltage V_{cm}

To verify the dependence of the ESD p-n junctions leakage on temperature, the following experiment was performed. The temperature in a climatic chamber was swept from 0°C to 50°C. The bondwire that connects the pad of the input of CH2 to the package was removed, so the leakage was mainly related to the ESD protection reverse bias current. In figure 3.19

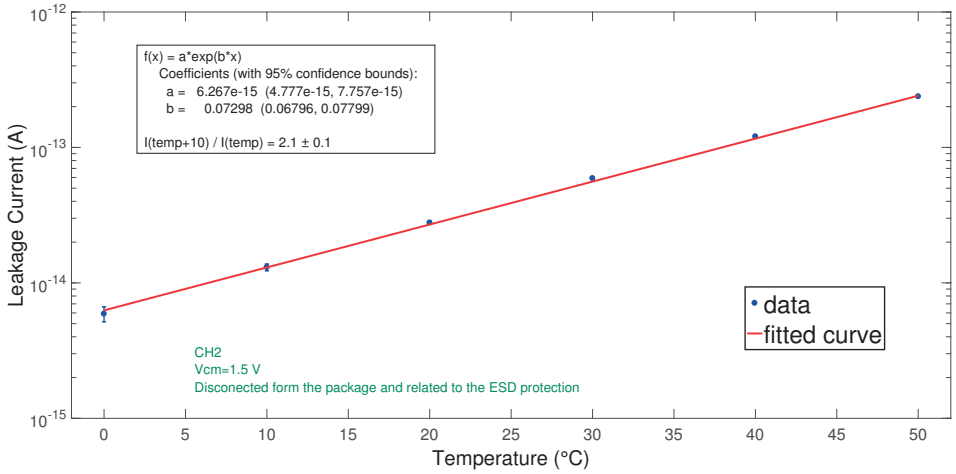

Figure 3.19 – Mean value of ESD protection leakage current of CH2 versus temperature

the leakage current of this channel is plotted as a function of temperature. An exponential fit is used and it is calculated that the measured leakage current increases by a factor of 2.1 ± 0.1 for every 10°C increase of temperature, as expected [58]. The temperature of the ASIC was also measured with an infrared camera and it was at most 2°C higher than the temperature inside the climatic chamber.

3.5.3 Package and adjacent pins leakage current measurement

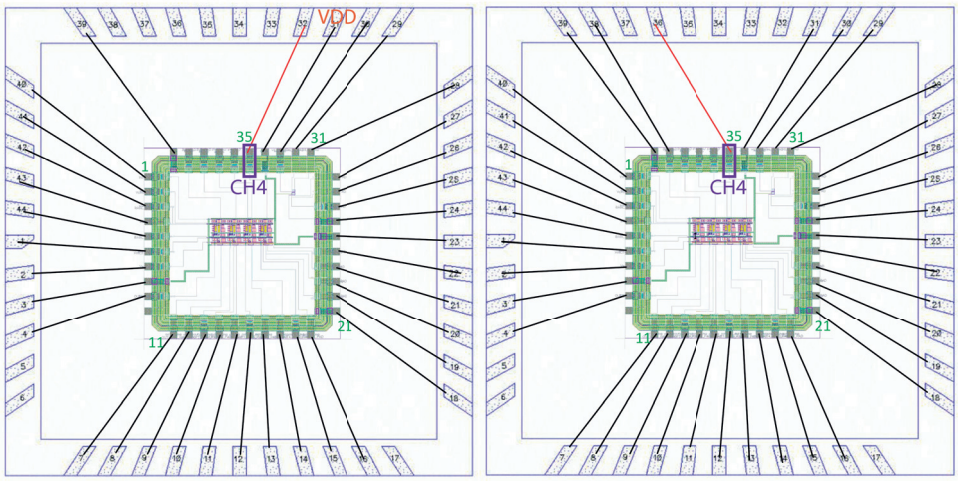

Figure 3.20 – Difference in CH4 bonding that resulted in different leakage current

The chip is encapsulated in a 44 pin ceramic package [81]. In order to limit any leakage current related to dust or other residues, the package was cleaned before the bonding procedure. The different voltage on the pins adjacent to the measuring channel is another potential source of leakage current. This was observed when the leakage of the same channel was measured with

the bondwires connected to the package and when the bondwires were disconnected from the package. This was also evident when measuring CH4. When CH4 had V_{DD} as one adjacent pin, it demonstrated "high" leakage current of +120 fA. When the bondwires were removed and CH4 was bonded back, as shown in figure 3.20, further and not adjacent to the V_{DD}, the leakage current was measured to be +14 fA under the same conditions (V_{cm} and temperature). However the polarity of the leakage current in that channel was opposite compared to CH1 that had ground as an adjacent pin.

In order to limit the leakage current related to the different voltage of the adjacent pins, the V_{cm} pads could be used as a guard around the input pads [73]. That way, there would be no voltage drop and the leakage current due to the adjacent pins would decrease. Moreover, the chip could be directly bonded on the PCB in order to limit any influence from the package.

3.5.4 Leakage current measurement of the printed circuit board

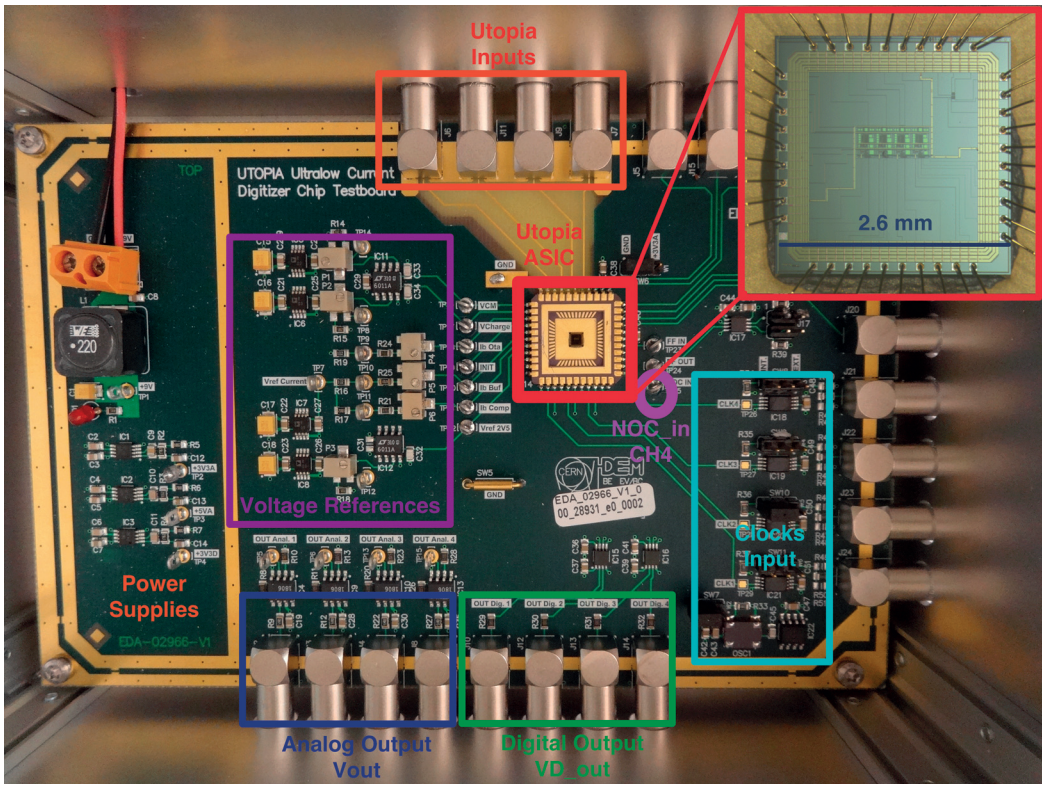

Figure 3.21 – The testboard of the Utopia 1 ASIC

The PCB that hosts the ASIC is shown in figure 3.21. The material that was used is the standard glass-reinforced epoxy FR-4. The PCB traces connecting the LEMO [82] connectors to the ASIC were routed on the top layer with no ground plane and without solder mask, for better insulation. A relative measurement of the leakage current due to the PCB was performed. The leakage current of CH2 with a cable connected to the input was measured over a long time.

Then the same test was repeated and another PCB without a chip was connected to the end of the first PCB's cable. The measured leakage current was similar in both cases as it can be seen in figure 3.22, so the PCB leakage I_{leak_PCB} proved to be extremely low compared to the other sources of leakage current. The PCB and the package pins were clean from residues, dust, humidity and any other source of contamination, since these would severely degrade the low current measurements. The dirt between the traces or across insulating materials acts as a conductive medium between two conductors, so proper care has to be taken for a proper ultra-low current measurement.

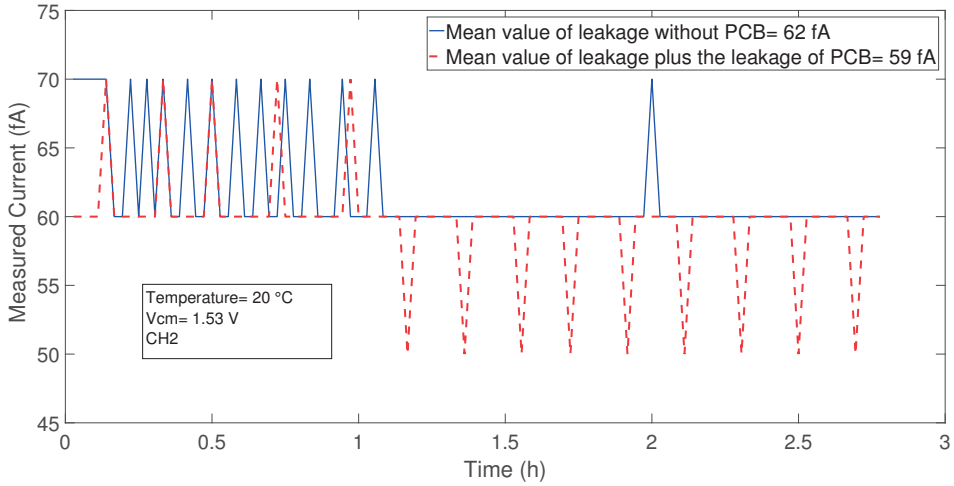

Figure 3.22 – Measurements with and without the PCB connected

To summarize, Table 3.3 includes measurements at 10°C and 20°C of the leakage current of the four different channels of the Utopia 1 ASIC with the same common mode voltage (V_{cm} = 1.7 V). The leakage currents of CH1 and CH2, that are mainly dominated by the leakage of the ESD protection, double with every 10°C increase in temperature. On the other hand, the CH4 leakage current is positive and dominated by the voltage difference due to the adjacent pins [83].

Table 3.3 – Leakage Current Measurements

	Mean Value of the Measured Leakage Current when $V_{cm} = 1.7V$			
Temperature	**CH1**	**CH2**	**CH3**	**CH4**
	Normal ESD	Modified ESD	Input switch	Different adjacent pins
10°C	-14 ± 1 fA	-44 ± 1 fA	≈ 200 aA	+8 ± 1 fA
20°C	-32 ± 2 fA	-80 ± 1 fA	≈200 aA	+28 ± 1 fA

As a conclusion, the ESD protection diodes and the layout affect the measured leakage cur-

rent. In addition, for sub-picoampere current measurements either the temperature of the environment should be kept constant or a leakage current compensating topology should be introduced.

3.6 Synchronous versus Asynchronous Mode

The Utopia 1 ASIC can operate in synchronous and also asynchronous mode. In the synchronous mode, the discriminator output is brought into an externally provided clock domain of typically 10 MHz (for CH1, CH2, CH3 and CH4). In the asynchronous mode (only for CH4), the discriminator output triggers a monostable that discharges the integrator [84]. After comparing the two modes, the asynchronous demonstrated better performance in terms of noise and crosstalk. Noise synchronous with the clock edges was visible on the analog output. This is related to the fact that the clock frequency was fed to the input through the parasitic capacitance of the ESD protection in the inputs. The padring of this prototype was not split into two different power domains for the analog and the digital pads, so the clock was propagated to the input. This was not present in the asynchronous mode.

As shown in figure 3.23, after the discriminator's triggering, in the next clock rising edge, the non-overlapping clocks manage the injection of the reference charge Q_{ref} through the switched capacitors circuit. When higher currents in the nA to the μA range were injected and the system was operating in higher frequencies, a faster clock frequency would be better compared to the selected 10 MHz frequency, since the discharge would happen earlier. For the 10 MHz frequency, in the worst case this would happen after 100 ns. This is a considerable delay for currents above 1 μA. A higher clock frequency though, would make the discharge happen faster, but would be seen in the input through the parasitic capacitance. For the asynchronous case, the delay due to the monostable is constant and can be made short.

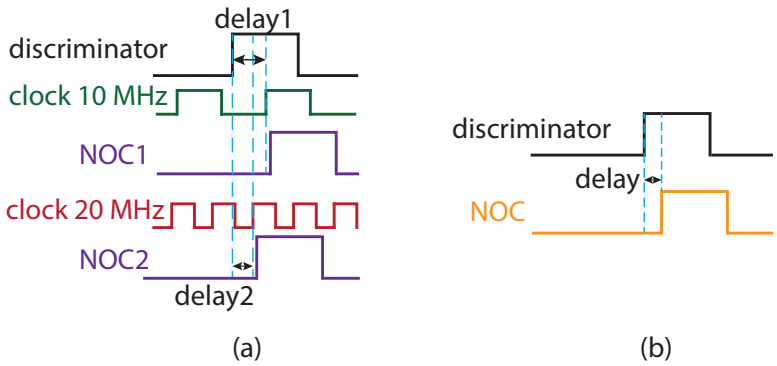

Figure 3.23 – (a) Synchronous versus (b) asynchronous mode pulses in the discriminator and the pulse that generates the non-overlapping clocks (NOC)

A plot of the ratio of the measured current over injected current versus the injected current is shown in figure 3.24. The asynchronous mode demonstrates better performance in the high input current compared to the synchronous mode.

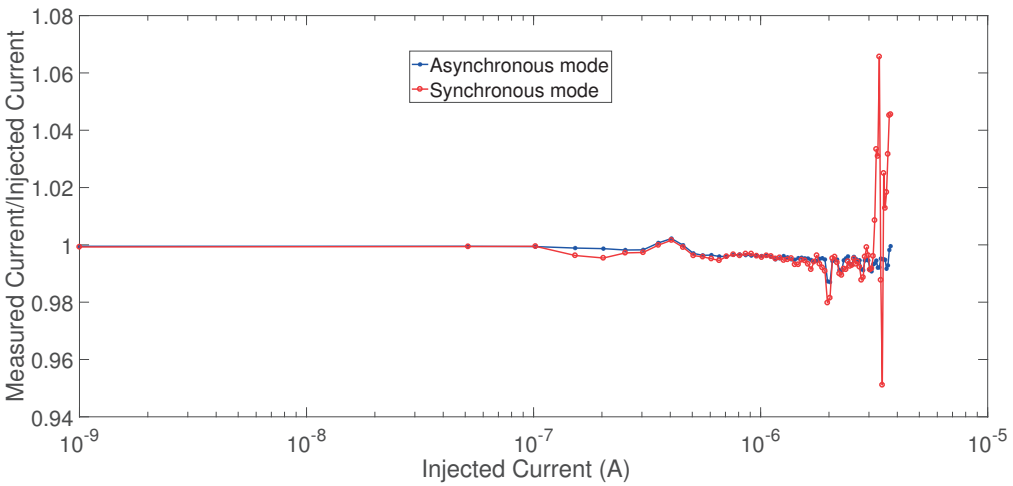

Figure 3.24 – Synchronous versus asynchronous mode in CH4

3.7 Dynamic Range Measurement

After measuring the different leakage currents present in the input of the CFC, two precise laboratory current sources from Keithley, Keithley 6430 [85] and Keithley 263 [86], were connected to the front-end to study the performance of all the channels of the single range digitizer. The experimental setup included a LabVIEW user interface and an automatic routine that was sweeping and injecting the requested current values from the source in different steps.

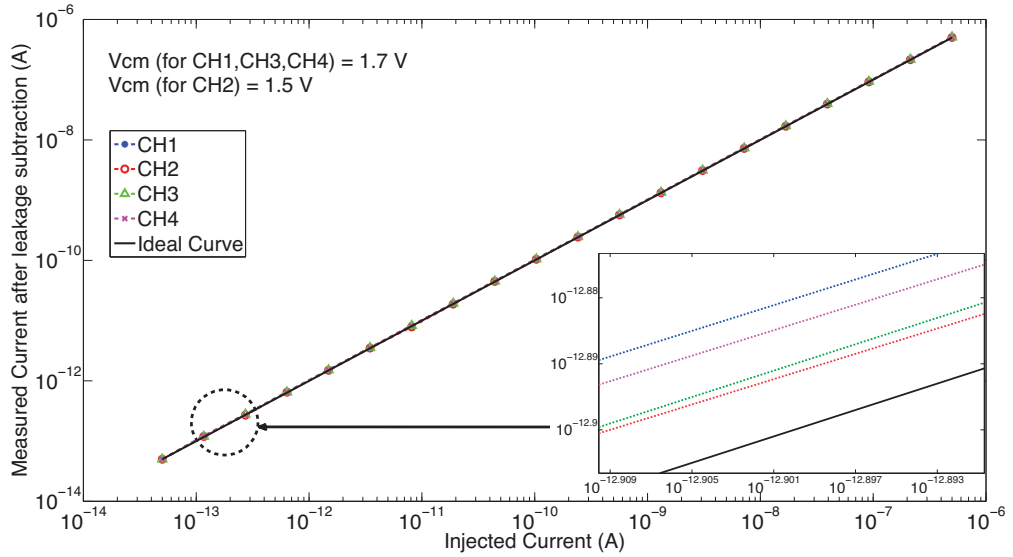

Figure 3.25 – Measurements when input currents from 50 fA to 500 nA are injected into the channels of Utopia 1 in synchronous mode

All the channels of one chip were tested by injecting currents starting from 50 fA and increasing

up to 500 nA in different steps. The leakage current of each channel was initially measured at a constant temperature and its value was stored and used for post processing. The injected versus measured current plot is presented in figure 3.25. The negative currents are plotted with the opposite sign. All the channels were operating in synchronous mode.

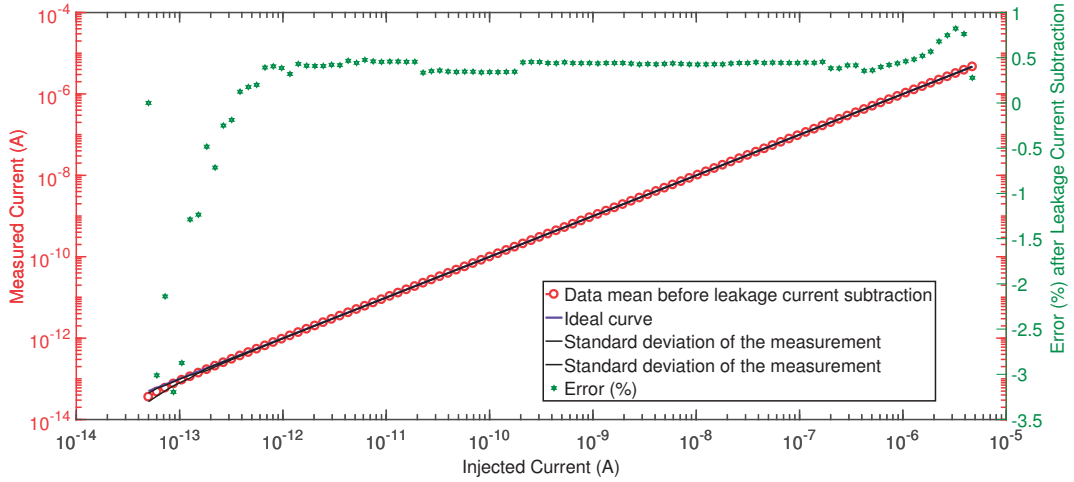

Figure 3.26 – Dynamic range measurements when input currents from 50 fA to 5 μA are injected using Keithley 6430 in CH4 in asynchronous mode

The mean value of the measured current before and after post processing is presented in figure 3.26 as a function of a testing injected current for CH4 in asynchronous mode. Input currents starting from 50 fA and increasing up to 5 μA were measured. The error is higher at the low and the high limits of operation due to the leakage current for the low currents and to bandwidth limitations for the high currents.

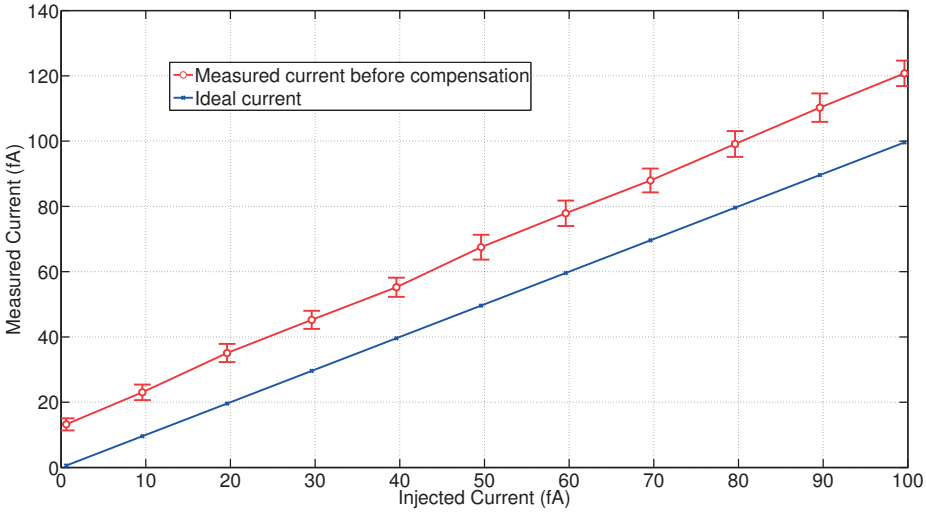

Figure 3.27 – Mean value of ultra-low injected current from 1 fA to 100 fA versus measured current for CH1 at 10°C with 0% humidity

For ultra-low current measurements, currents starting from 1 fA up to 100 fA were injected in 11 steps using the Keithley 6430 current source. The mean value of the measured current is shown in figure 3.27. For such low currents the time window was increased to T_w= 600 s, so the acquired data were averaged over 600 s. The leakage current of the CH1 of the chip under test was measured to be 12 fA for the selected V_{cm} value. The presented results are shown before the leakage current compensation using post processing with Matlab. For these sensitive measurements, the temperature and the humidity were kept constant at 10°C and 0% respectively.

3.8 Chapter Conclusions

The methodology of evaluating all the critical leakage current sources in the input of a front-end for ultra-low current measurements was presented. It was demonstrated that after special attention for an ultra-low leakage current design, where the subthreshold leakage and the adjacent pins leakage are eliminated, the remaining dominant source of leakage current is related to the ESD protection diodes in the input pads, whose value varies according to temperature. This implies that with proper compensation of the input ESD protection diodes leakage current, the system would be able to digitize currents starting from a few fA.

The presented current to digital converter is able to digitize femtoampere currents comparable to the ESD protection diodes leakage current. In the meantime, it could also measure input currents that were injected from a precise laboratory current source. Table 3.4 compares Utopia 1 with the ASICs that were presented in chapter 2, in Table 2.4.

The 0.35 μm technology from AMS was experimentally evaluated in a practical example and is suitable for the new CERN's radiation monitoring system.

One of the initial goals of this demonstrator ASIC was to establish a list of guidelines to be used in the development of the front-end for radiation monitoring. These guidelines can be also used in any system that targets measuring extremely low currents. These guidelines were outlined in this chapter and are summarized here for the sake of clarity. They will be the starting point for the design of the integrated circuit for radiation monitoring at CERN that is presented in the next chapter.

Leakage current of the switches

The leakage current of the switches that are connected to the input of the front-end was successfully minimized using the source shifting technique.

Leakage current of the package and of the adjacent pins

The ceramic package is adding some leakage current that can be regarded as an offset. This current can be included in the compensation procedure but can be also decreased. In general the layout of the chip and the proximity to the power supply lines and other pins increase

the leakage current. This fact was demonstrated and measured in Utopia 1 using the fourth channel of the ASIC, where the voltage of the adjacent pins induced considerable leakage current through the package. An alternative solution would be to bond the chip directly to the PCB in order to limit any influence from the package.

Both the PCB and the chip layout are important for an ultra-low leakage design. A guard voltage can be buffered and surround the input pads in order to limit any voltage drop across the inputs. The input signal pads should be surrounded by V_{cm} pads, so all the external leakages would flow in the low impedance guard traces.

Leakage current of the PCB, cables and connectors

The characteristics of the PCB material are important. In this prototype, the standard FR-4 PCB did not leak considerably compared to the other sources of leakage. However, dirty PCB traces can cause extremely high leakage, since the dirt between the traces or across insulating materials acts as a conductive medium between two conductors. This is why proper cleaning procedures are a prerequisite.

In this first design, coaxial cables and standard LEMO [82] connectors were used. However, for proper guarding a guard should be connected to a potential equal to the input signal level. The use of triaxial connectors and triaxial cables would favor the low leakage design. The inner guard shield could surround the signal and extend the guard all the way up to the signal source.

ESD protection diodes leakage current

Since the combination of various net leakage currents is more difficult to compensate, if all the previous leakage current guidelines are met, the net leakage is mainly dominated by the ESD protection leakage. The leakage current related to the ESD protection varies according to the temperature and cannot be eliminated. This is why the use of a dummy channel that replicates the leakage due to the ESD protection structures can be considered as a solution to cancel that leakage and its increase due to temperature.

ESD trimming or fine tuning, by moving either the V_{cm} or the power supply of the ESD diodes to a different voltage in order to partially minimize the net leakage, can partially limit the additional current.

A leakage current measuring procedure for different temperatures and the introduction of a learning curve, is another alternative that can be used in order to subtract the leakage current that is mainly related to the ESD protection.

Separation of analog and digital padrings

In this first ASIC, the analog and the digital padrings were not separated. This is why in the synchronous channels, noise from the clock was fed back to the inputs. The synchronous architecture does not demonstrate any advantage over the asynchronous one, so the latter

architecture can be adopted. Moreover, the introduction of powercut cells in the padring could benefit the design in terms of noise.

Table 3.4 – Updated Comparison among ASICs for Radiation Monitoring

Characteristics	**TERA06 [33], [34]**	**TERA09 [39], [40]**	**QFW I ASIC [45]**	**BLM ASIC [41]**	**UTOPIA 1**
Publication Year	2004	2016	2004	2012	2015
Technology	AMS 0.8 μm	AMS 0.35 μm	AMS 0.35 μm	IBM 0.25 μm	AMS 0.35 μm
Die Size	6mm x 7mm	4.68mm x 5.8mm	3.28mm x 3.38mm	2.4mm x 3.775mm	2.6mm x 2.6mm
Dynamic Range	5 decades	6 decades	1.60 pA to 180 μA	1 pA to 1.05 mA	-12 fA to -5 μA
Leakage Current	194 fA	2 pA	1.65 pA	-188 fA	-12 fA to -80 fA
Linearity Error	± 1%	±2%	± 1.5%	± 5%	± 2.5%
Polarity	Unipolar	Bipolar	Unipolar	Bipolar	Unipolar
Clock Frequency	20 MHz	250 MHz	10 MHz	12.8 MHz	10 MHz

4 Design of an Ultra-low Picoammeter for Radiation Monitoring

4.1 Introduction

The front-end for the radiation measurements at CERN should be able to digitize input currents over nine decades. The proposed ASIC named Ultra-low Picoammeter 2 (Utopia 2), was designed to be able to digitize currents starting from a few fA up to 5 μA according to the CERN specifications.

This chapter is organized as follows. In the first section, the architecture of the front-end ASIC is explained and a detailed description of the circuit's behavior is given. The expected non-idealities are outlined along with their impact on the performance of the system. The circuit level design of the most important blocks is presented and analyzed step by step. The noise is also evaluated. Finally, the system level integration and the guidelines that were used to minimize the leakage currents are presented.

4.2 System Architecture

The designed system will be used with ionization chambers to monitor radiation levels as low as the natural background radioactivity. Thus, the input signals are in the order of femtoamperes to picoamperes. The variation of the leakage current in the input of the system due to temperature and humidity changes, leads to the consideration of a leakage current compensation solution. This is made possible with the introduction of a second channel that replicates the input structures of the measuring first channel and will measure only the net leakage current.

As explained and demonstrated in chapter 3, the ESD protection is the dominant source of leakage current in the input of a current to digital converter implemented in AMS 0.35 μm technology. By matching the ESD protection structures, eliminating all the other possible sources of leakage current and performing an initial calibration of the system, the second channel can compensate for the leakage current of the first channel.

The operating principle is based on the asynchronous current to frequency converter (CFC) and charge balancing without dead time or charge loss. A simplified leakage compensation scheme for the CFC is presented in figure 4.1.

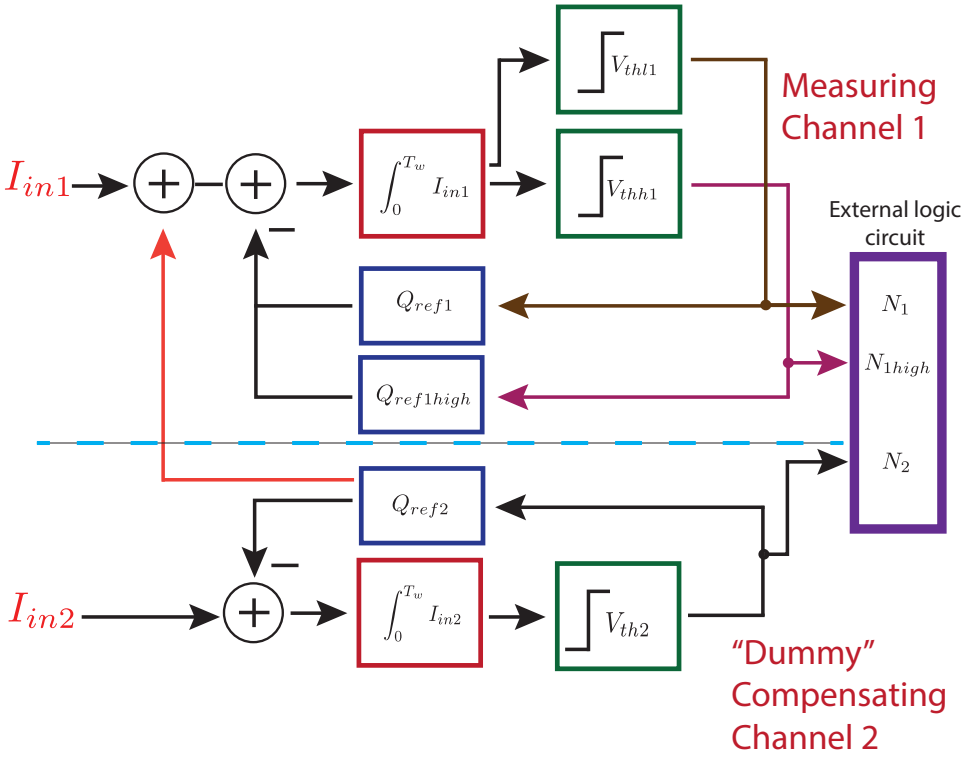

Figure 4.1 – Utopia 2 leakage current compensation CFC scheme

Based on the CFC architecture, for the measuring channel 1, lower input current I_{in1} is supposed to provide less counts N_1 in a measuring time window T_w, compared to a higher input current that provides more counts. The system's operating frequency f_1 depends on the reference charge Q_{ref1} that balances the integrated charge and not on the comparators' thresholds, as shown in equation (4.1).

$$f_1 = \frac{N_1}{T_w} = \frac{I_{in1}}{Q_{ref1}} \tag{4.1}$$

There are two requirements regarding the operating frequency of the system that are related to the lower and higher limits of operation. For a faster acquisition time in the sub-picoampere current range and in order to be able to cover the required wide dynamic range when the input current is in the μA range, the reference charge has to be adjusted. For this reason we

introduced a second reference charge injection implementation $Q_{ref1high}$ for the measuring channel 1.

The "dummy" compensating channel 2 measures the leakage current I_{in2} related to the input structures and subtracts it from channel 1. This is possible due to the charge balancing principle and the injection of the reference charge Q_{ref2} directly to channel 1. As a result, channel 1 will digitize the input current that is only related to the detector's output current I_{det} after the cancellation of any additional leakage.

4.3 Detailed Description of Circuit's Behavior

A more detailed circuit diagram of the Utopia 2 system is shown in figure 4.2.

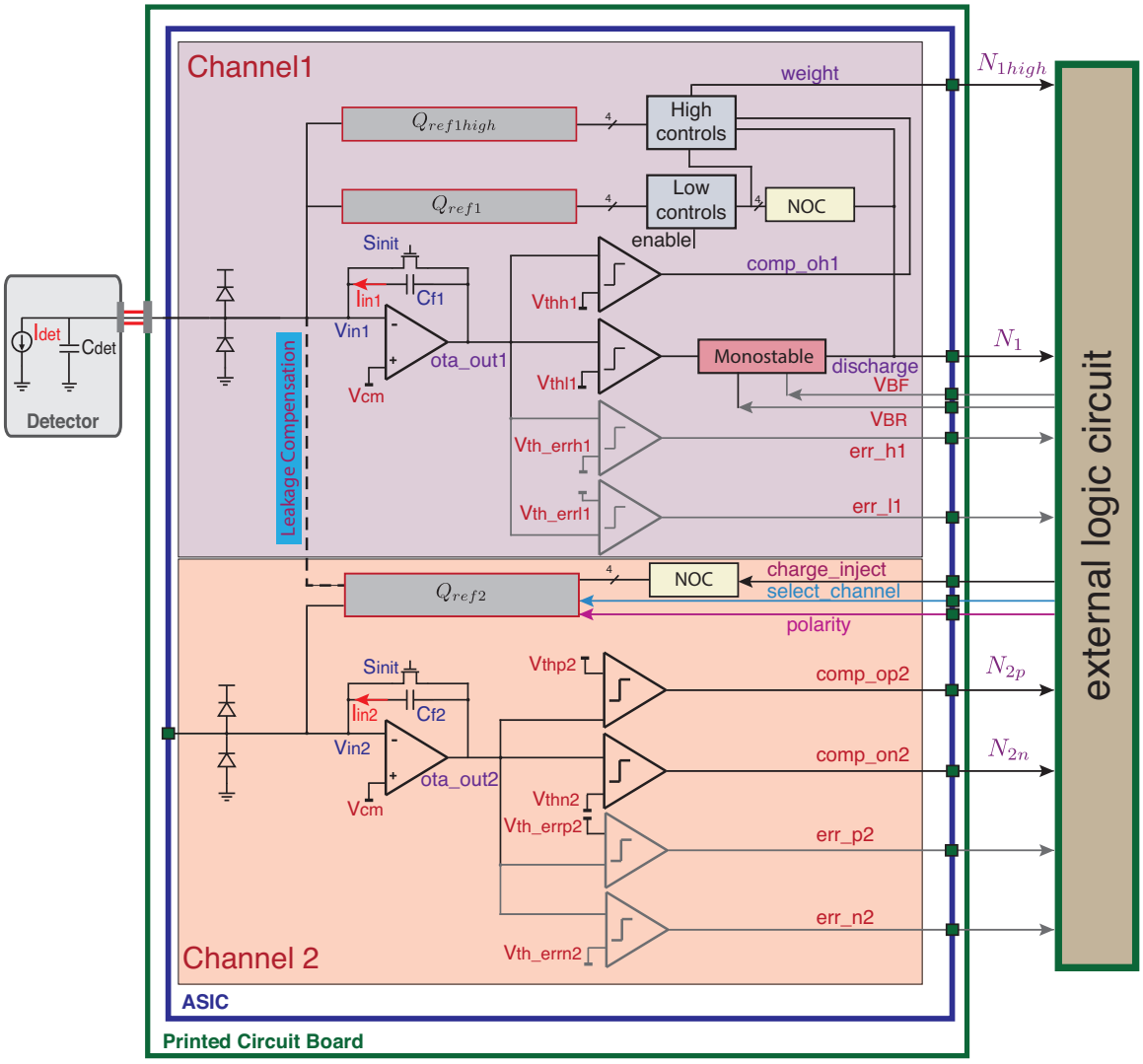

Figure 4.2 – Utopia 2 block diagram

The first channel is designed to accept negative polarity input currents, as required from the biasing of the existing radiation detectors and consists of the integrator, four comparators, the digital logic and the reference charge injection circuits. The input current I_{in1} is integrated in the feedback capacitor C_{f1}, until the first comparator detects the crossing of a low threshold V_{thl1} or/and the second detects the crossing of a higher threshold V_{thh1}. The other two discriminators detect when the output of the integrator saturates to the power supply rails and generate corresponding error signals.

After the low threshold set by the discriminator that has V_{thl1} as a reference voltage is crossed, a monostable triggers the injection of a constant charge Q_{ref1}. As long as the integrator's output *ota_out1* stays above that low threshold, the monostable alternates and controls the charge and discharge phases of the reference charge circuit. At each cycle of the monostable, the same amount of charge Q_{ref1} is injected into the input to discharge the feedback capacitor C_{f1}. The V_{BF} and V_{BR} inputs are used to set the duration of the *"discharge"* signal that is the output of the monostable and sets the period t_{cycle} of the charge and discharge phases of the reference charge switching circuit.

For low input current, only the low threshold comparator triggers. When the input current increases, the second comparator triggers when the V_{thh1} is crossed. The second discharging circuit that can inject charge equal to $Q_{ref1high}$ is introduced and is connected in parallel to the circuit that can inject Q_{ref1}, so finally the total reference charge that is injected to the input is equal to the sum of the reference charge of the two ranges Q_{ref1} and $Q_{ref1high}$. That second discharging circuit is automatically activated by the high controls circuit, so that the system is able to measure and digitize higher input currents. When the second range is active the *"weight"* signal has a logic '1' otherwise it is '0'. From the *"discharge"* and *"weight"* signals, the external digital logic circuit implemented in the FPGA, counts the number of charge injections N_1 and N_{1high} of the discharging circuits. The input current related only to channel 1, is given by equation (4.2):

$$I_{in1} = \frac{N_1 Q_{ref1} + N_{1high} Q_{ref1high}}{T_w} \tag{4.2}$$

where N_1 is the number of charge injection cycles of the low reference charge Q_{ref1} and N_{1high} is the number of charge injection cycles with both discharging circuits activated. T_w is the selected measuring time window.

Channel 2 acting as the compensating channel, operates similarly to channel 1 and integrates only the net input leakage current I_{in2}. The leakage current can be positive or negative, so there are two comparators, one to detect the positive leakage current when the threshold V_{thp2} is crossed and another one to detect the negative input current whose threshold is V_{thn2}. Moreover, there are also two error signals err_{n2} and err_{p2}, in case the integrator output saturates to the positive or negative power supply rail. The reference charge circuit of channel

2 is able to inject bipolar charge according to the polarity of the input leakage current. Since channel 2 is supposed to measure only leakage current, the charge Q_{ref2} is scaled down to $Q_{ref1}/10$ and so does C_{f2}, being $C_{f1}/10$. That way, the compensating channel 2 has a finer granularity and the same amount of input charge is integrated 10 times faster compared to the measuring channel 1.

The comparator outputs of channel 2 are sent to the FPGA, where two counters count the number of times N_{2p} or the number of times N_{2n} that the respective comparator triggered. The FPGA also generates and feeds back to the ASIC three control signals. The *"charge_inject"* signal is the pulse that is needed to activate the Q_{ref2} bipolar charge injection circuit. The *"polarity"* is the signal that manages the positive or negative charge injection according to the polarity of the input leakage current. Finally, the *"select_channel"* signal manages the injection of the reference charge Q_{ref2} either to channel 2 or to channel 1.

The leakage current of channel 1 can be internally and actively compensated, because the channel 2 discharging circuit output is physically connected to the input V_{in1} of channel 1. As an alternative to the on-chip compensation with Q_{ref2} being injected to channel 1, post processing can be used after the data acquisition for the leakage current compensation.

The matching of the input structures for the leakage current compensation is related to the matching of the ESD protection devices and the matching of the switches. This means that the ESD diodes and the switches that are connected to the input should have the same operating conditions and the same biasing. Additionally they should match in terms of layout that means that they should have the same size, the same shape, the same orientation and the same surroundings [87].

Although the input structures of the two channels should be matched by design, calibration is mandatory for the calculation of the accurate ratio ρ of the leakage currents between channel 1 and channel 2 for different temperatures. This ratio can be provided to the FPGA in order to perform the active leakage compensation properly or to be used for the post processing of the acquired data.

The leakage current related only to channel 2, is given by equation (4.3):

$$I_{in2} = \frac{N_{2p}Q_{ref2} - N_{2n}Q_{ref2}}{T_w} \tag{4.3}$$

where N_{2p} and N_{2n} are the number of times that the second channel's integrator output crosses the V_{thp2} or V_{thn2} thresholds respectively. In most cases the leakage current is expected to be either positive or negative, so either N_{2n} or N_{2p} will be zero.

After the leakage current compensation, the detector current I_{det} can be obtained by equation

(4.4):

$$I_{det} = \frac{N_1 Q_{ref1} + N_{1high} Q_{ref1high} + \rho \left(N_{2p} Q_{ref2} - N_{2n} Q_{ref2} \right)}{T_w} \tag{4.4}$$

where ρ is the ratio of the leakage currents I_{in1} / I_{in2} of the two channels. The ratio ρ will be calculated during the leakage current calibration procedure.

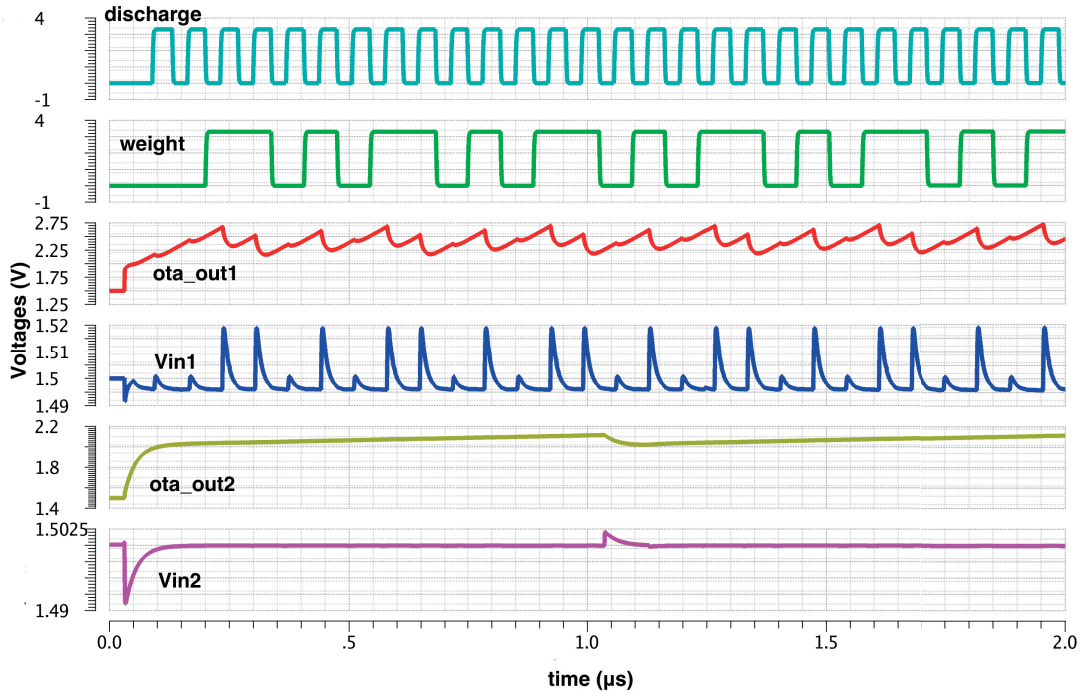

Figure 4.3 – Simulation of the signals *"weight"*, *"ota_out1"*, "V_{in1}", *"ota_out2"*, "V_{in2}" (values expressed in (V)), when I_{in1}= -5 μA and I_{in2}= -10 nA in a measuring time window T_w= 2μs

Figure 4.3 presents the simulation of the signals *"discharge"*, *"weight"*, *"ota_out1"*, "V_{in1}", *"ota_out2"*, and "V_{in2}", when an input current of I_{in1}= -5 μA is injected into channel 1 and the leakage current into channel 2 input is I_{in2}= -10 nA (this high value of leakage current is not expected in reality and was used only for simulations in a short measuring time window). The waveforms are plotted for a simulation time of T_w= 2 μs.

Figure 4.4 presents the simulation of the signals *"ota_out1"* of channel 1 and *"ota_out2"*, *"comp_on2"*, *"charge_inject"*, *"select_channel"* and *"polarity"* of channel 2. This simulation demonstrates the operation of the active leakage current compensation. The leakage current is negative so the comparator that has V_{thn2} as a reference voltage triggers. The FPGA sets the *"charge_inject"* signal that initially injects to channel 2 and then to channel 1. For the injection to channel 1, the *"select_channel"* signal changes from "low" to "high". The *"polarity"* is low

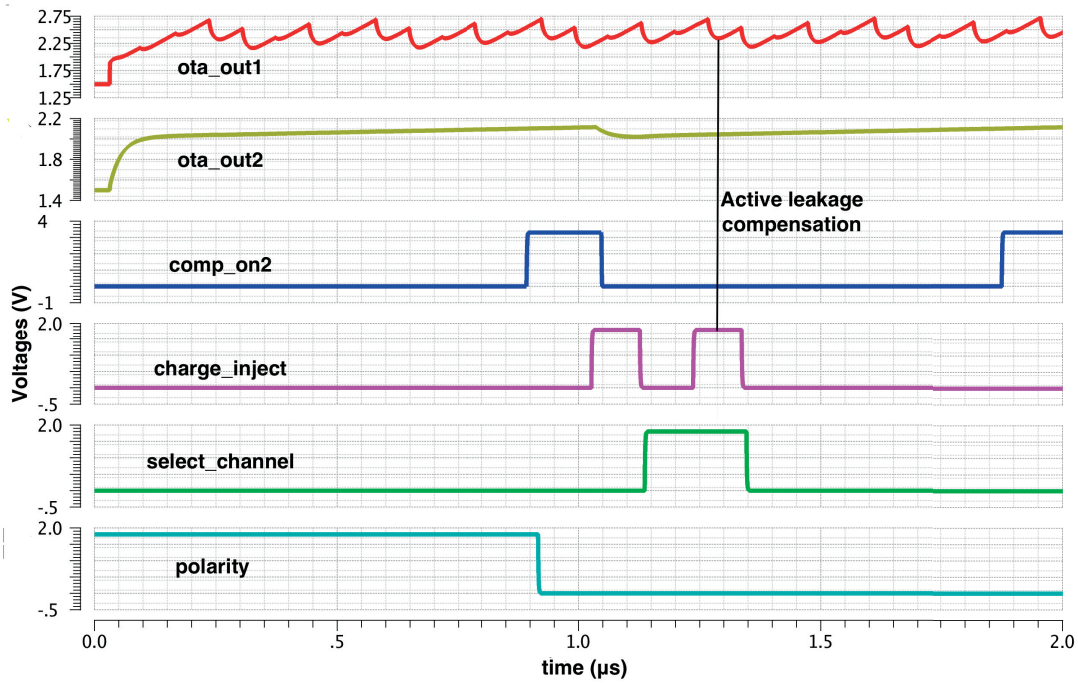

Figure 4.4 – Simulation of the signals *"ota_out1"*, *"ota_out2"*, *"comp_on2"*, *"charge_inject"*, *"select_channel"*, *"polarity"* (values expressed in (V)) during active leakage current compensation

because the leakage current is negative.

To summarize, Tables 4.1 and 4.2 present the outputs and the inputs of the Utopia 2 ASIC.

Table 4.1 – Utopia 2 Outputs

Utopia 2 Outputs		
Channel 1	Discharge	Monostable output, produces N_1 of the low range
	Weight	High controls output, produces N_{1high} of the high range
	Err_{h1}	Out of range to the positive rail
	Err_{l1}	Out of range to the negative rail
	Ota_out1	Analog output of OTA 1
Channel 2	$Comp_{op2}$	Positive leakage detection comparator output
	$Comp_{on2}$	Negative leakage detection comparator output
	Err_{p2}	Out of range to the negative rail
	Err_{n2}	Out of range to the positive rail
	Ota_out2	Analog output of OTA 2

Table 4.2 – Utopia 2 Inputs

Utopia 2 Inputs		
Channel 1	IN_1	Connected to the detector
	V_{BF} / V_{BR}	Set t_{cycle} period of the *"discharge"* signal
Channel 2	IN_2	Not connected to the detector
	Polarity	Leakage current polarity
	Select_Channel	Discharge Q_{ref2} either to channel 2 or to channel 1
	Charge_Inject	Signal that manages the injection of Q_{ref2}

4.4 Reference Charge

As shown in equations (4.2), (4.3) and (4.4), the reference charges are the most important parameters of the charge balancing architecture, since they set the gain of the conversion. The stability of the measuring instrument depends on the stability of the reference charges. The discharging circuits can be implemented using switched capacitors or current sources. The characteristics of each implementation are shown in Table 4.3.

Table 4.3 – Possible Q_{ref} Implementations

Injection through a switched capacitor	Injection through a current source
no precise time reference required	requirement for a precise clock
dependence on voltage and capacitor values (calibration needed)	dependence on a reference current (calibration needed)
dependence on virtual ground quality	dependence on timing (calibration needed)
the same circuit can inject charge of both polarities (for channel 2)	requires extra circuitry to inject charge of both polarities (for channel 2)

Since both implementations have advantages and disadvantages and in both cases calibration is needed for the precise generation of a reference charge, the switched capacitor implementation was selected for its simplicity. It was also used and tested in the prototype Utopia 1 ASIC. Additionally, the Utopia 2 ASIC is designed to operate asynchronously and therefore an accurate timing reference should be added in case of the current source implementation. The switched capacitor circuit can also easily inject charges of both polarities without any additional circuitry. The bipolar injection is required for channel 2 as it needs to be able to integrate positive or negative leakage current.

The basic delay-free stray insensitive switched capacitor circuit is presented in [75], [88], [89], [90]. The idea behind this circuit is the sampling of a predefined quantity of charge that is proportional to an input voltage V_{ref} and a reference capacitor C_{ref}. Then this charge is delivered to the integrator's input. This procedure happens in two steps according to the phases of some non-overlapping clocks [91]. These clocks determine when the transfer of the charge occurs and guarantee that the transition from one step to the other does not cause any

charge losses. The integrator's output voltage $V_{out(i)}$ after the second step equals:

$$V_{out(i)} = V_{out(i-1)} - V_{ref(i)} \frac{C_{ref}}{C_f} \tag{4.5}$$

Referring to figure 4.5 for an inverting stray parasitic insensitive switched capacitor circuit, the reference charge Q_{ref} depends on the switched capacitor circuit capacitance value C_{ref} and the voltages $V_{charge+}$, $V_{charge-}$, V_{cm} and V_{in}. In the first step, C_{ref} is connected between the voltages $V_{charge-}$ and V_{cm} and in the second step, the $V_{charge+}$ discharges the feedback capacitor C_f through C_{ref}. The reference charge Q_{ref} is given by equation (4.6). The voltage V_{ref} is equal to $V_{charge+}$-$V_{charge-}$ and the difference ΔV_{in} is not zero due to static and dynamic offsets.

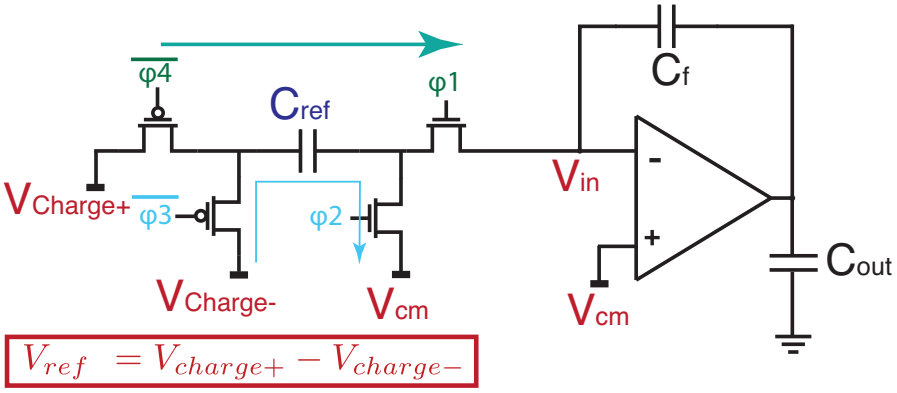

Figure 4.5 – Parasitic insensitive switched capacitor inverting integrator

$$Q_{ref} = C_{ref}\left(V_{charge+} - V_{charge-} + V_{cm} - V_{in}\right) = C_{ref}\left(V_{ref} - \Delta V_{in}\right) \tag{4.6}$$

The signals φ_1, φ_2, φ_3 and φ_4 generated from the non-overlapping clocks, control the switches of the switched capacitor integrator. These control signals required for the charge subtraction using the circuit of figure 4.5 are shown in figure 4.6 [87].

By changing the phases of the switches, the same circuit can be used for the opposite polarity charge injection [76]. A tutorial and detailed analysis of the design of switched capacitor circuits, can be found in the appendix of [72].

4.5 Utopia 2 Design Values

Compared to the Utopia 1 ASIC, the reference charge Q_{ref1} is scaled down 10 times making a faster measurement possible. The selected design values are shown in Table 4.4.

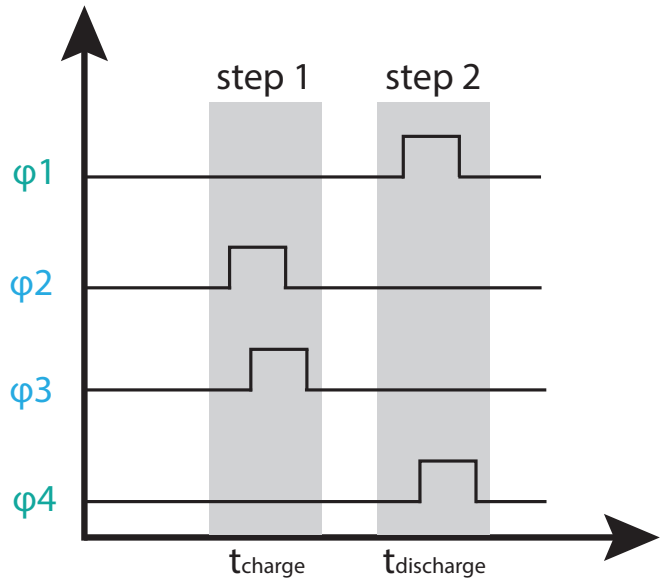

Figure 4.6 – Switch timing for a charge subtraction

Table 4.4 – Utopia 2 Design Values

Channel 1	Channel 2
Q_{ref1}= 100 fC $Q_{ref1high}$= 400 fC	Q_{ref2}= 10 fC
C_{ref1}= 100 fF $C_{ref1high}$= 400 fF	C_{ref2}= 10 fF
C_{f1}= 1 pF	C_{f2}= 100 fF
V_{thl1}= 2.1 V	V_{thp2}= 1.9 V
V_{thh1}= 2.3 V	V_{thn2}= 2.1 V
V_{cm}= 1.5 V, V_{init}= 2 V $V_{charge+}$= 2.5 V, $V_{charge-}$= 1.5 V	

The minimum current that can be measured corresponds to one count and one charge injection in the reference time window of T_w= 100 ms. The I_{min} is given by equation (4.7) and for the selected reference charge and time window values is equal to 1 pA.

$$I_{min} = \frac{Q_{ref1}}{T_w} = \frac{100fC}{100ms} = 1pA \tag{4.7}$$

The requirements of the background radiation measurements have relaxed the constraints of the system when low current has to be measured. By measuring for longer time periods or adding consecutive time windows of 100 ms, the resolution increases and lower input currents can be integrated. Since the system is continuously integrating and there is no forced reset,

the charge accumulated in the feedback capacitor will provide a count if the measurement time increases. This is the reason why the minimum measured current can be less than 1 pA when $T_w{}' = n \cdot T_w$, n>1.

The maximum current that can be measured is related to the maximum reference charge, that in this case is Q_{ref1}+$Q_{ref1high}$= 500 fC. As shown in equation (4.8), it also depends on the maximum period of operation t_{cycle} of the charge injection circuits. The t_{cycle} is the sum of the t_{charge} and $t_{discharge}$ that are controlled respectively by the externally set voltage values V_{BF} and V_{BR}.

The requested maximum current of 5 μA is possible with this circuit, when t_{cycle} equals 100 ns. By changing the V_{BF} and V_{BR} voltages and decreasing the duration of t_{cycle}, an even higher current can be measured. However, the t_{charge} and $t_{discharge}$ pulses should be long enough to allow the formation and delivery of an accurate reference charge, as will be shown later.

$$I_{max} = \frac{Q_{ref1} + Q_{ref1high}}{t_{cycle}} = \frac{500fC}{100ns} = 5\mu A \tag{4.8}$$

4.6 Integrator Requirements

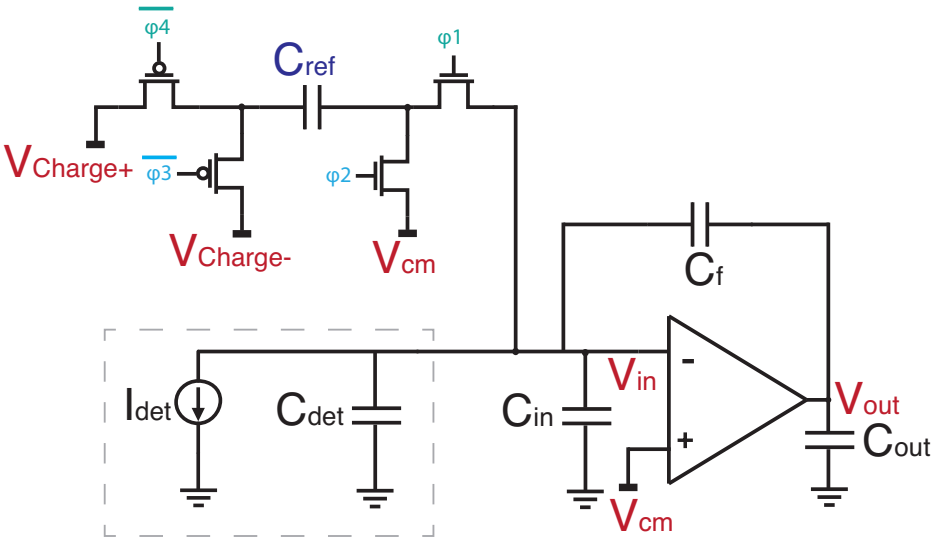

Figure 4.7 – Integrator with switched capacitor circuit

An integrator with the switched capacitor circuit used to discharge the input current I_{det} is shown in figure 4.7.

The integrator's dynamic offset has to be evaluated since the reference charge Q_{ref} depends

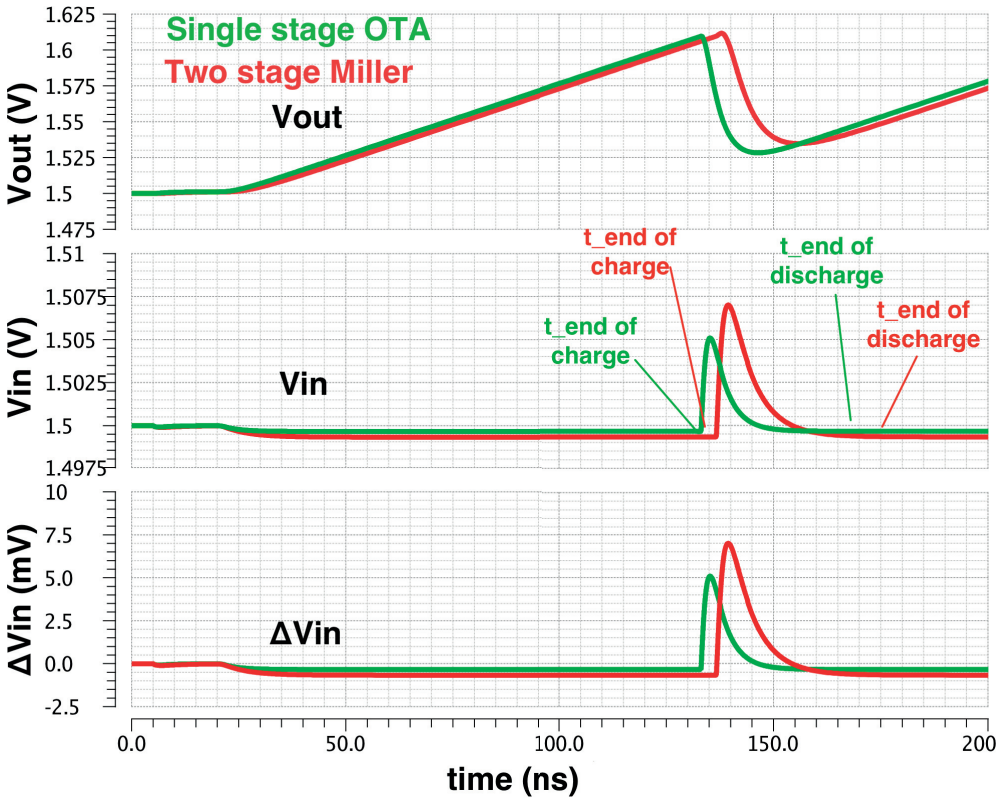

Figure 4.8 – The integrators' output voltage V_{out}, input voltage V_{in} and ΔV_{in} for a single stage OTA and a two stage op-amp

on ΔV_{in} as shown in equation (4.6).

A behavioral model simulation was performed, where the integrator was initially implemented as a single stage OTA with g_m= 3 mS and later as a two stage op-amp with g_{m1}= 3 mS and g_{m2}= 6 mS. The simulated outputs V_{out}, inputs V_{in} and offset voltages ΔV_{in} of the integrators after the Q_{ref} discharge when I_{in}= 1 μA are shown in figure 4.8. The single stage OTA demonstrates lower ΔV_{in} offset compared to the two stage op-amp.

Following some approximations, this behavior will be analyzed using the single stage OTA integrator shown in figure 4.9.

If the $\Delta V_{in} \approx 0$ because the virtual ground is considered not to move significantly compared to V_{cm}, then for the voltage V across the feedback capacitor C_f:

$$\frac{dV}{dt} = \frac{I_{det}}{C_f} \tag{4.9}$$

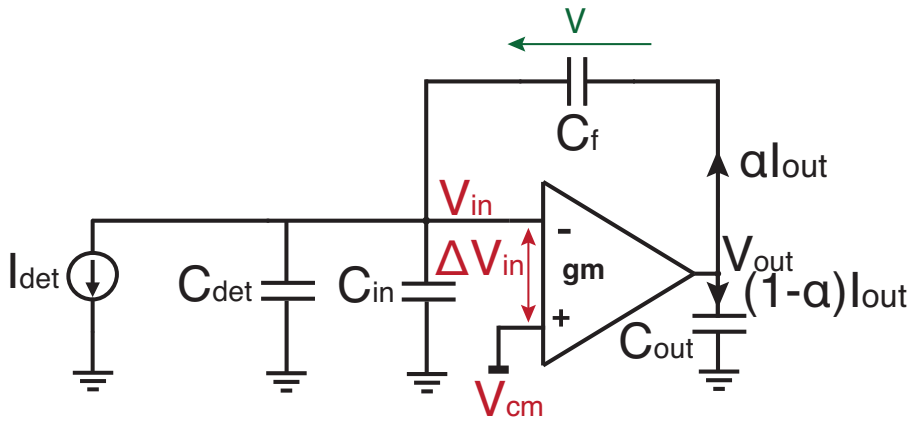

Figure 4.9 – Single stage OTA

The output current I_{out}= $g_m \Delta V_{in}$, so the detector current I_{det} is given by equation (4.10):

$$I_{det} = \alpha g_m \Delta V_{in} \tag{4.10}$$

where α= $C_f / (C_f + C_{out}) \leq 1$.

So equation (4.9) is written as:

$$\frac{dV}{dt} = \frac{\alpha g_m \Delta V_{in}}{C_f} \tag{4.11}$$

Then the virtual ground voltage V_{in} where the switched capacitor is discharged to is given by equation (4.12):

$$V_{in} = V_{cm} - \frac{I_{det}}{\alpha g_m} \tag{4.12}$$

So substituting (4.12) in the reference charge equation (4.6) results in equation (4.13):

$$Q_{ref} = C_{ref} \left(V_{ref} + \frac{I_{det}}{\alpha g_m} - V_{os} \right) \tag{4.13}$$

that includes both the static offset V_{os} and the offset due to the limited g_m.

The respective measured number of counts for a single stage OTA is given by equation (4.14):

$$N_{counts} = \frac{I_{det} \cdot T_w}{C_{ref}\left(V_{ref} + \frac{I_{det}}{\alpha g_m} - V_{os}\right)} \tag{4.14}$$

A two stage Miller integrator is shown in figure 4.10.

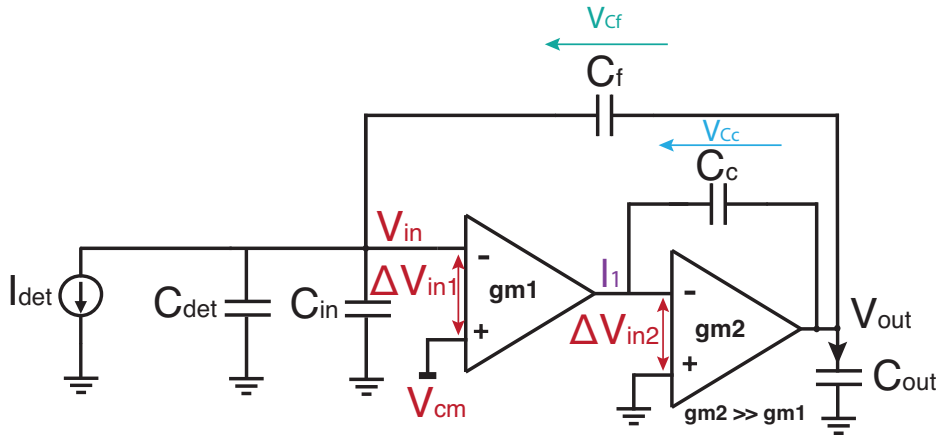

Figure 4.10 – Two stage op-amp

If $g_{m2} \gg g_{m1}$ where g_{m2} is the transconductance of the second stage and g_{m1} is the transconductance of the first stage, then if $\Delta V_{in2} \approx 0$ and $\Delta V_{in1} \approx 0$ because the input nodes do not move significantly, then equation (4.15) is true for the voltages V_{Cf} and V_{Cc} across C_f and C_c:

$$\frac{dV_{Cf}}{dt} \approx \frac{dV_{Cc}}{dt} = \frac{I_1}{C_c} = \frac{g_{m1}\Delta V_{in1}}{C_c} \tag{4.15}$$

So using equation (4.11) referred to a single stage OTA and equation (4.15), it can be concluded that:

$$\frac{\alpha g_m \Delta V_{in}}{C_f} = \frac{g_{m1}\Delta V_{in1}}{C_c} \tag{4.16}$$

which results in (4.17) that shows the ratio between the ΔV_{in} of a single stage OTA and the

ΔV_{in1} of a two stage op-amp:

$$\frac{\Delta V_{in}}{\Delta V_{in1}} = \frac{g_{m1}}{\alpha g_m} \cdot \frac{C_f}{C_c} \tag{4.17}$$

For a two stage Miller amplifier, the $GBW = g_{m1}/2\pi C_c$ can be identified in equation (4.17). In the Utopia 1 ASIC where the integrator was implemented using a two stage Miller amplifier the GBW= 127 MHz, g_{m1}= 1.6 mS and C_c= 2 pF. The amplifier was not optimized for its GBW. Nevertheless, to increase the GBW and decrease the dynamic offset, the power budget has to be increased. A single stage OTA can achieve higher GBW for the same power budget [91].

As a numerical example, if g_{m1} = 3 mS, g_m = 3 mS, C_f= 1 pF, C_c = 2 pF, C_{out}= 200 fF and α= 0.83, then equation (4.17) results in:

$$\frac{\Delta V_{in}}{\Delta V_{in1}} = 0.6 \tag{4.18}$$

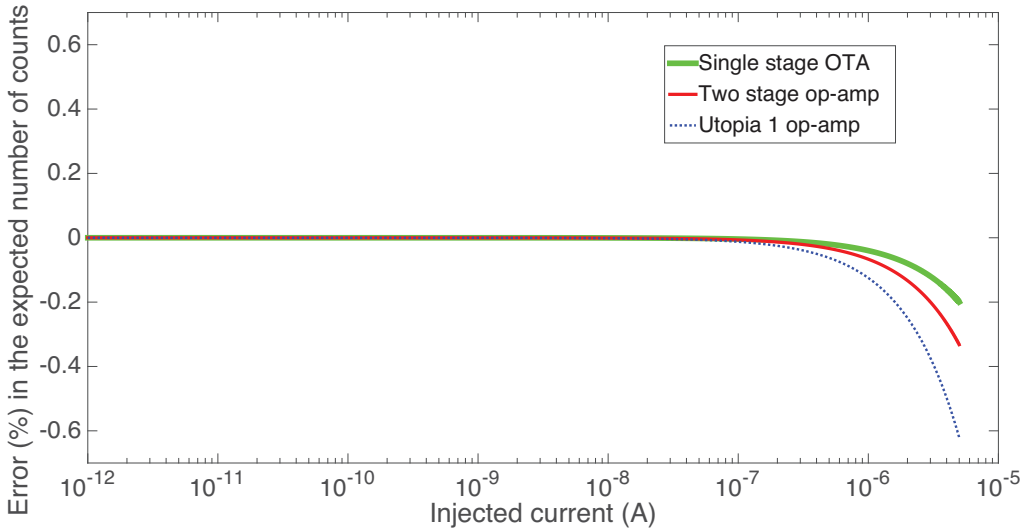

Figure 4.11 – Percentage error in the expected number of counts in a single stage OTA, a two stage op-amp and the Utopia 1 Miller op-amp

A comparison of the error in the expected number of counts between the single stage OTA, a two stage op-amp and the Utopia 1 Miller op-amp is depicted in figure 4.11. The number of counts for the single stage is derived from equation (4.14) and the ideal number of counts from the same equation without the offset. It can be seen that the dynamic offset affects the measured number of counts for the highest injected currents. This plot, in addition to the behavioral model simulation shown in figure 4.8 is the reason why a single stage OTA was

selected for the design of the integrator.

4.7 Expected Non-Idealities

This section focuses on how to deal with the expected non-idealities and demonstrates their impact on the performance of the system.

4.7.1 Capacitor values

The non-ideal capacitor values have an effect on the reference charge Q_{ref}. This impacts the conversion as shown in equation (4.14). Calibration has to be performed to calculate the total Q_{ref} value that includes the non-ideal value of the reference charge capacitors C_{ref}. The $V_{charge+}$, $V_{charge-}$ and V_{cm} voltages that are also responsible for the reference charge's value, are high accuracy voltage references that are provided externally and will be calibrated often.

4.7.2 OTA DC offset, limited g_m and DC gain

The DC offset V_{os} of the OTA, the limited transconductance g_m and the non-ideal DC gain have also an impact on the reference charge Q_{ref}. A target value of <1% error on the Q_{ref} is set.

The static offset V_{os} of the OTA should be considered during the design procedure. Since the selected low range reference charge in channel 1 is Q_{ref}= 100 fC, the static offset has to be below ± 5 mV to have an impact of 0.5% on the reference charge. So the OTA has to be designed with a target for V_{os} < 5 mV.

For the maximum input current I_{max} the limited transconductance g_m affects the reference charge and consequently the measured number of counts. The dynamic offset of the single stage OTA is responsible for a non-linearity error in the highest input currents. During the design phase, the selected transconductance will determine the dynamic error.

For example, for an input current I_{max}= 5 μA and with g_m= 3 mS and α< 1 the error in the virtual ground due to the dynamic offset is given by equation (4.19) and corresponds to an error less than 0.5 % of the reference charge.

$$\Delta V_{in} = \frac{I_{in}}{\alpha \cdot g_m} < 5mV \tag{4.19}$$

The effect of the limited DC gain has to be also considered. In the case of the low input current after a reference charge injection, V_{out} returns to the initial value from where the integration started. The worst case corresponds to the maximum input current. In that case, at the end

of the discharge the V_{out} is closer to the high threshold V_{thh1} value. For example, when the output V_{out} swings from 2 V to V_{thh1}= 2.3 V, for a minimum open loop gain of A_0= 60 dB, the maximum $\Delta V_{in(max)}$ equals 300 μV. This can be accepted because it is below the offset due to the limited g_m.

$$\Delta V_{in(max)} = \frac{\Delta V_{out}}{A_0} = \frac{300mV}{10^3} = 300\mu V \tag{4.20}$$

4.7.3 Comparator and logic delay

The comparator's offset is equivalent to a threshold offset, so it does not impact the conversion. The comparator's and the digital logic's delays introduce a propagation delay for the reference charge injection, which is important mostly in the maximum current's case. For the higher input currents, that leads to a V_{out} increase. This is not a problem for the application since that delay is short compared to t_{cycle}, but preferably, the overall delay has to be short in order to discharge immediately after the comparator's threshold crossing.

4.7.4 Charge injection and clock feedthrough

The non-ideal effects associated with the switched capacitor circuit switches are the charge injection and the clock feedthrough. The flow of the charge from the channel to the source and drain terminals when the switch turns OFF, is the channel charge injection. The charge that is stored in the channel when the switch is ON is given by equation (4.21):

$$Q_{channel} = -WLC_{ox}(V_H - v_{in} - V_{T0}) \tag{4.21}$$

where W is the width of the transistor, L is the length, V_H is the value of the clock when the switch is ON and refers to VDD for an nMOS transistor, v_{in} is the sampled voltage and V_{T0} is the threshold voltage. When the switch turns OFF fast, it can be assumed that this charge splits equally between the source and drain nodes [70], [92].

The gate-drain and gate-source overlap capacitors are coupling the clock signal from the gate of the switch to the drain and source terminals. The effect of the signal voltage coupling to the switch terminals is called clock feedthrough.

It is desirable to minimize the charge injection and the clock feedthrough. Minimum size nMOS switches with W= 0.6 μm and L= 0.35 μm were selected for the switched capacitor circuit to be connected to V_{in}. The signal dependent charge injection can be minimized by turning OFF the switches connected to the virtual ground first [76]. The error in the reference charge caused by clock feedthrough, should be below 1%.

4.7.5 Effect of noise

The current to digital conversion is based on averaging over time. Averaging will improve the Signal to Noise Ratio (SNR) related to the white noise and the calibration will remove the systematic offset. The effect of the noise on the circuit's operation has to be considered.

The noise in the OTA output and the noise of the discriminator can be regarded as a jitter. This jitter should not cause any error in the expected number of counts. The jitter has to be estimated by simulation in comparison to the t_{cycle} of the charging and discharging operation.

The noise in the switched capacitor circuits is affecting the charge that is stored in the capacitor and therefore the conversion. The sampled noise voltage is superimposed on the reference voltage. The noise has to be estimated across the reference capacitor C_{ref} at the end of the charging and at the end of the discharging operation.

The noise consists of the thermal and the $1/f$ noise. The worst case estimate of the SNR is referred to one single cycle. Averaging improves the wideband noise since the samples are not correlated [93]. The RMS value of the noise can be reduced by $\sqrt{N}$ where N is the number of counts. On the other hand, no improvement is expected for the $1/f$ noise [70].

4.7.6 Mismatch in leakage currents between channel 1 and channel 2

A possible mismatch in the net leakage current between channel 1 and channel 2 is related to a mismatch in the input ESD protection diodes. Calibration should be performed to find the ratio ρ between the leakage currents 1 and 2 over the operating temperature range. This ratio will be used for the Q_{ref2} injection during the active leakage current compensation or during the post processing of the acquired raw data.

The expected non-idealities are summarized in Table 4.5. They were taken into account during the circuit's design phase. When the non-idealities are translated to an error in the injected reference charge Q_{ref}, a target design value of <1% is set. The reference charge calibration in each chip is mandatory for an accurate current to digital conversion.

4.8 Circuit Level Design

The circuit level design and the most salient characteristics of each specific block are presented in this section.

4.8.1 Folded cascode OTA design

As discussed in section 4.6, the OTA should be a single stage OTA. For the design of that OTA, the main requirement was the high transconductance g_m, since the front-end should be able to handle input currents up to 5 μA. The g_m should be large enough, so that the discharging

Table 4.5 – Expected Non-Idealities Summary

Non-idealities	Effect on:	Target Value	Solution (constant temperature)
Capacitor Values	Q_{ref}	-	Calibration
OTA DC offset	Q_{ref}	<1%	Calibration
OTA limited gm	Q_{ref}	<1%	
Charge injection clock feedthrough	Q_{ref}	<1%	Minimum size nMOS switches, calibration
Comparator and logic delay	Propagation delay, V_{out} increase	-	No impact in the conversion
Comparator offset	Is equivalent to a threshold offset	-	No impact in the conversion
Noise	Output jitter, Accuracy of Q_{ref}	$\frac{V_{rms}}{V_{ref}} < 1\%$	No impact in the conversion Evaluation in section 4.8.8
Mismatch in leakages ESD diodes mismatch	On-chip leakage compensation	-	ρ calibration

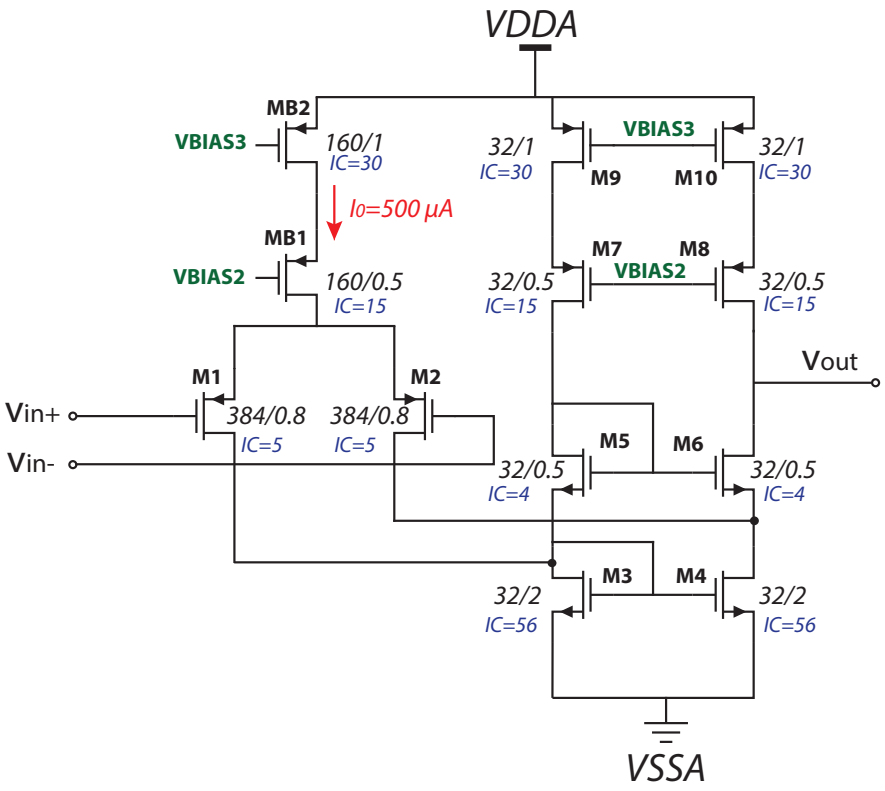

Figure 4.12 – Folded cascode OTA of Utopia 2 ASIC. The presented transistor sizes are in μm

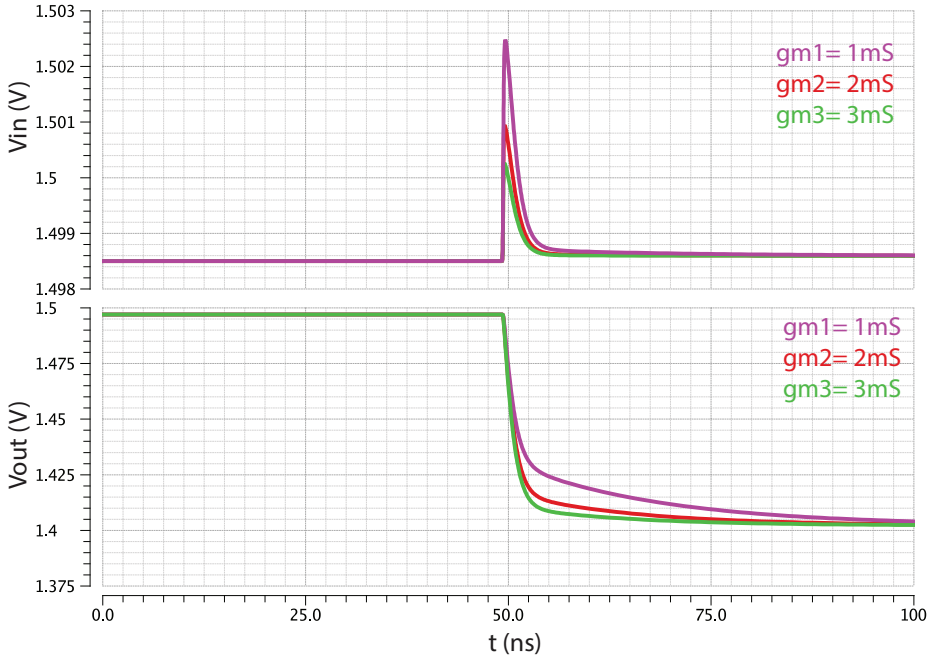

Figure 4.13 – Simulation of the discharging phase in a single stage OTA for different g_m values

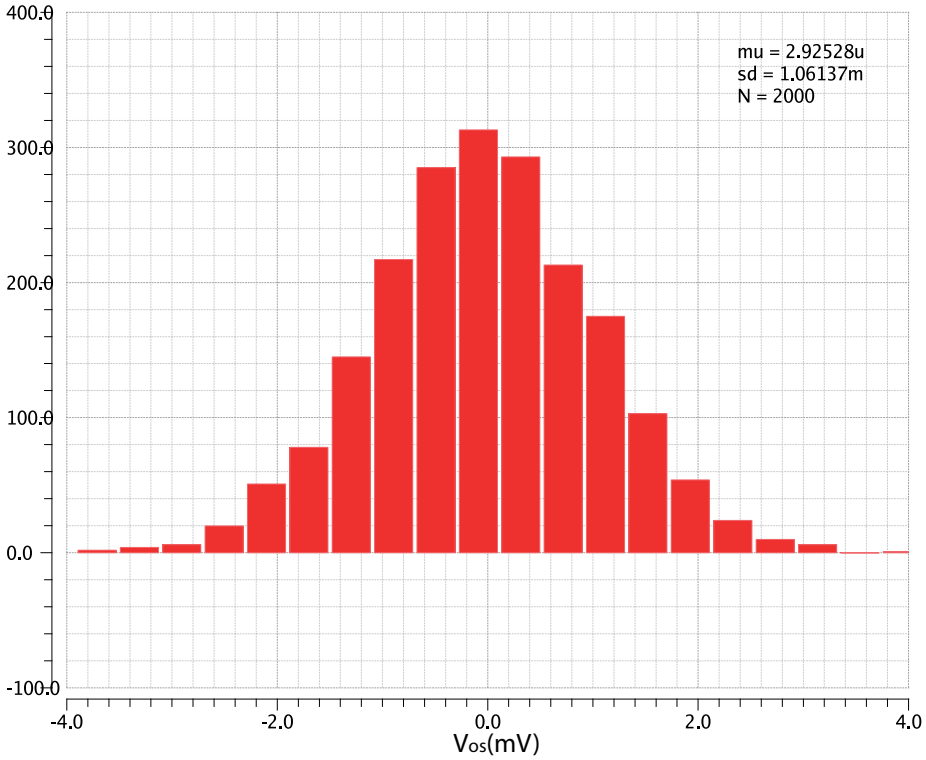

Figure 4.14 – Offset voltage of the folded cascode OTA

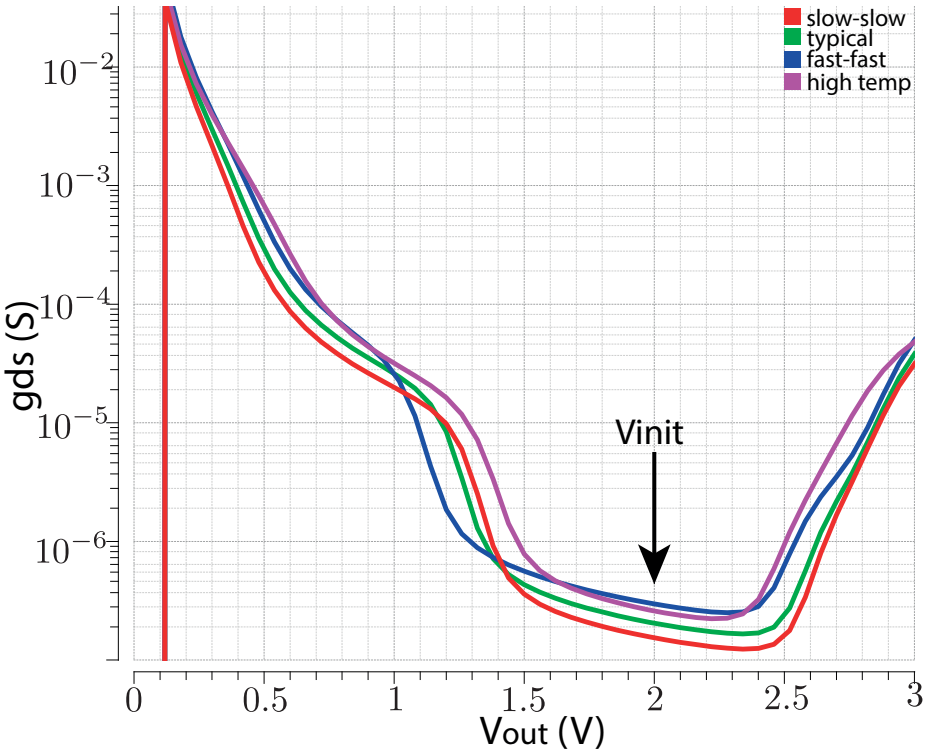

Figure 4.15 – Output conductance of the folded cascode OTA of Utopia 2 ASIC

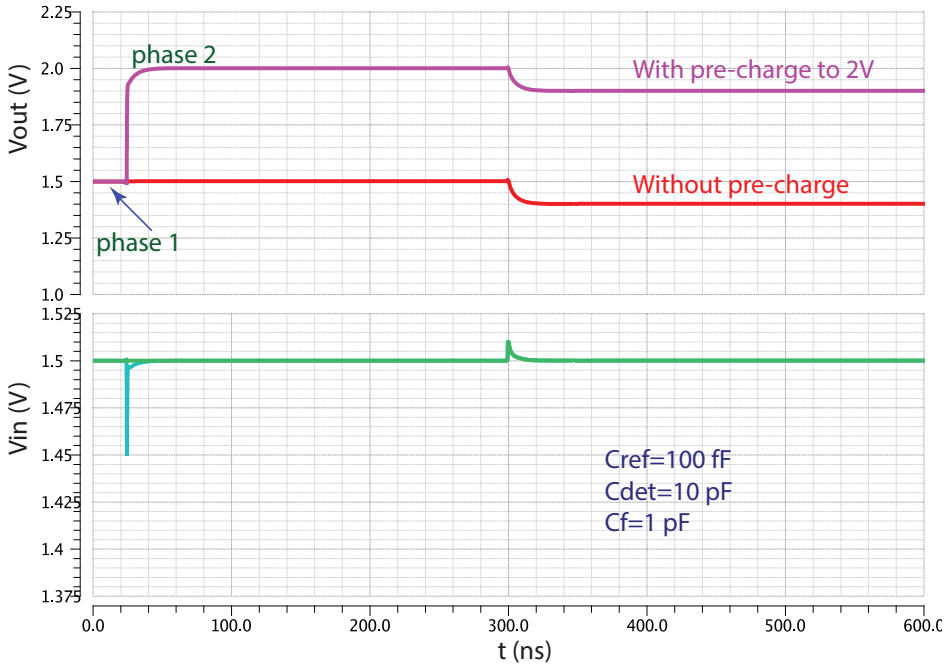

Figure 4.16 – Transient analysis (V_{out} and V_{in}) during charge injection in channel 1

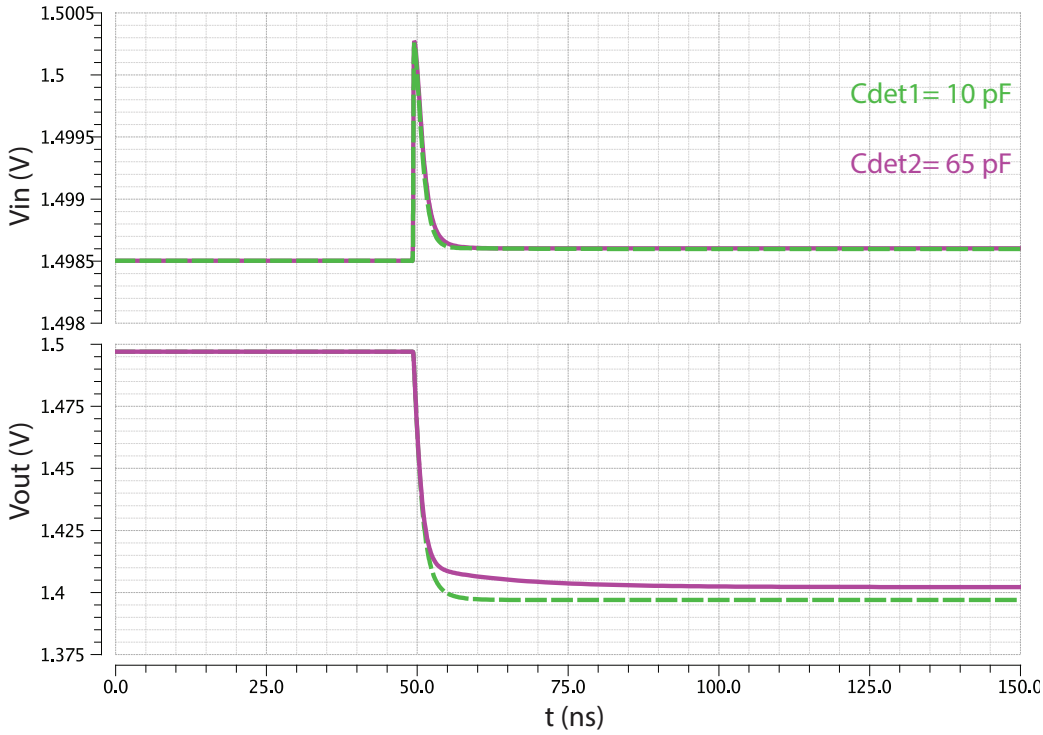

Figure 4.17 – Transient simulation (V_{in} and V_{out}) for the two different detector capacitances C_{det1}= 10pF and C_{det2}= 65pF

reference charge circuit delivers an accurate Q_{ref} to the input before the beginning of the next step. The proposed single stage OTAs were the telescopic and the folded cascode OTA.

The folded cascode topology gives the freedom to optimize better the devices of the input and output stage independently, compared to the telescopic where the devices should be both optimized at the same time for g_m and g_{ds}. So, if the folded cascode OTA does not penalize the design in terms of power consumption, it is a good choice for this application and it provides more flexibility.

The designed single stage folded cascode OTA is shown in figure 4.12. The transistors of the OTA were sized according to the parameters of the EKV model for 0.35 μm technology [94]. The transconductance g_m and respectively the GBW should be as high as possible to reduce the effect of the dynamic offset for the higher input currents. Initially, a behavioral model of the system was used for the simulation of a single stage OTA with different transconductance values. The input V_{in} and the output voltage V_{out} of the integrator for g_{m1}= 1 mS, g_{m2}= 2 mS and g_{m3}= 3 mS are shown in figure 4.13. The OTA was designed with g_m= 3 mS. The simulated GBW= 430 MHz.

The input differential pair transistors are pMOS transistors for lower $1/f$ noise and they were sized to operate in the moderate inversion with an inversion coefficient IC= 5. The bias current of the input transistors is I_1= 250 μA and the transistors MB1 and MB2 operate in

strong inversion. The nMOS transistors of the load were sized to operate in strong inversion in order to reduce their noise contribution. The amplifier was designed with an open loop gain of A_0= 76.4 dB.

The Monte Carlo analysis of the offset voltage V_{os} between V_{in-} and V_{in+} when the output V_{out} is at 2 V, is shown in figure 4.14. The mean value of the offset is 2.925 μV, the minimum value is -3.872 mV, the maximum value is 4.181 mV and the sigma is 1.061 mV. The number of points was 2000 and the statistical variation included mismatch and process variations. The sizing of the bottom current mirrors was optimized for lower offset. The static voltage offset is below 5 mV for 3σ as discussed in the non-idealities section, so the effect on the reference charge is < 0.5 fC that corresponds to < 0.5% of error. The widths of the cascode transistors were selected to be W= 32 μm for layout purposes. Their biasing current is 100 μA.

Regarding the DC output swing of the OTA, corner analysis was performed for the output conductance and g_{ds} is plotted as a function of the output voltage V_{out} in figure 4.15. It can be seen that g_{ds} is constant and optimized when V_{out} is close to 2 V. This is the reason why, during the initialization phase of the chip, the integrator's output is pre-charged at 2 V. That way, the output voltage of the OTA will start ramping up from 2 V and not from the V_{cm} that is set at 1.5 V.

The transient behavior during the charge injection into the input of channel 1 is shown in figure 4.16, where the reference capacitance of the switched capacitor circuit is C_{ref1}= 100 fF and the detector's capacitance is C_{det}= 10 pF. The input resistance R_{in}, i.e. the resistance of the pad, is 200 Ohms. The output voltage V_{out} and the input voltage V_{in} were simulated for both cases, with and without the pre-charge at V_{init}= 2 V.

Various ionization chambers are used at CERN with different characteristics. The detector capacitances vary from C_{det1}= 10 pF to C_{det2}= 65 pF. When the capacitance of the detector is C_{det2}= 65 pF, the time constant that is needed for the discharge of the feedback capacitor C_{f1} increases as shown in the simulation of figure 4.17. However, this is not a major problem for the application, because ionization chambers with higher C_{det} are used in environments with low radiation, so low current is expected. In that case, the CFC integrator can integrate over longer time periods and the output frequency is lower. In order to have a long discharging time for the accurate transfer of a defined reference charge, the duration of the *"discharge"* signal of the monostable that generates the non-overlapping control signals of the switched capacitor circuits can be externally adjusted using the V_{BR} voltage.

4.8.2 Feedback circuit of the integrator

The feedback circuit of the integrator consists of the feedback capacitor and the initialization switches. The feedback capacitor of channel 1 is C_{f1}= 1 pF. On the other hand, the feedback capacitor C_{f2} of channel 2 is scaled down ten times being 100 fF, in order to integrate the low leakage current faster. The sizes of the switches in channel 1 and channel 2 are scaled

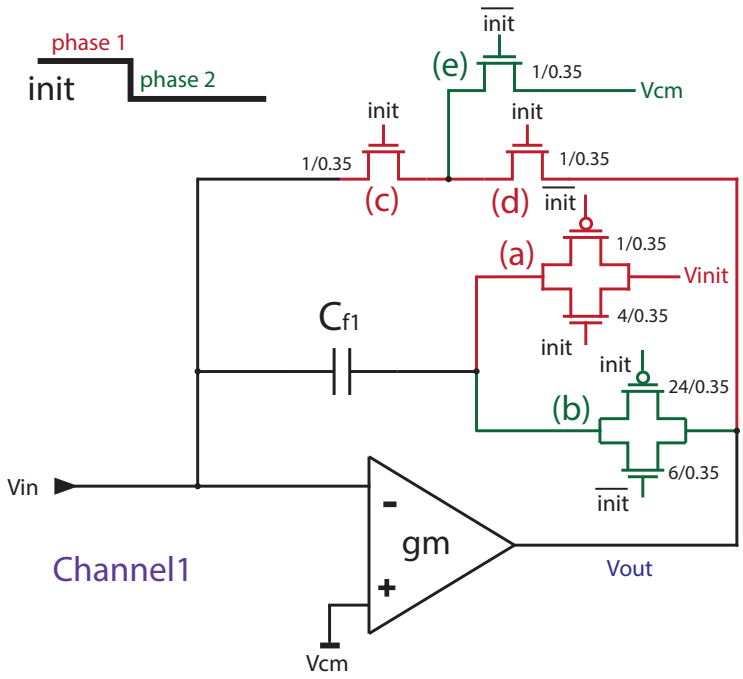

Figure 4.18 – Initialization (phase 1) and operating (phase 2) phases of the integrator for channel 1. All the transistor sizes are in μm

accordingly in order to establish the same time constant. As shown in figure 4.18 for channel 1, the transmission gate labeled (b), that connects the feedback capacitor to the output of the OTA, consists of an nMOS switch with W= 6 μm and L= 0.35 μm and a pMOS switch with W= 24 μm and L= 0.35 μm, while for the channel 2 the nMOS size is W= 0.6 μm and L= 0.35 μm and the pMOS W= 2.4 μm and L= 0.35 μm. The corresponding R_{on} are calculated to be 340 Ohms and 3.4 kOhms respectively so finally the time constants are RC= 340 ps.

Referring to figure 4.18, when the $init$ signal is high, the integrator is reset (switches (c) and (d) are ON) and the feedback capacitance C_{f1} is initially connected and pre-charged to V_{init}= 2 V through the transmission gate labeled (a). The aim of this pre-charge is to have a constant output conductance in the OTA, as explained in section 4.8.1. After initialization (the $init$ signal is driven low), in the circuit's normal operation named phase 2, the nMOS switch (c) drain, is connected to V_{cm} via switch (e). This is done to decrease the subthreshold leakage current of the (c) switch that is connected to the input, since its $V_{DS}\approx$ 0. By keeping the V_{DS} of a transistor as small as possible, the leakage current can be decreased. For the normal operation, the transmission gate (b) connects the capacitor's C_{f1} terminal that is pre-charged at 2 V, to the output V_{out} of the OTA and the integration starts.

It should be noted that in this design the analog and the digital power supplies are separated. All the analog control signals for the switches are connected to the analog power supplies.

4.8.3 Comparator

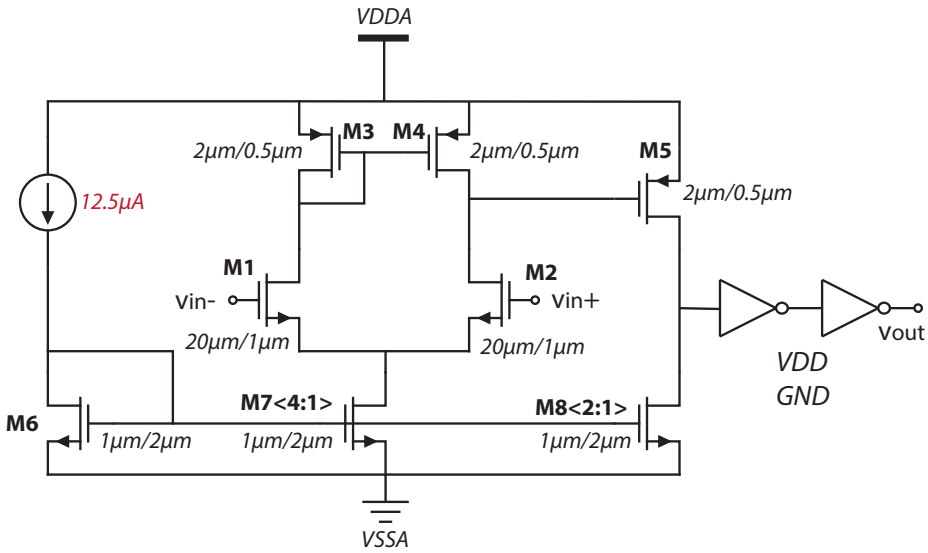

Figure 4.19 – Comparator schematic

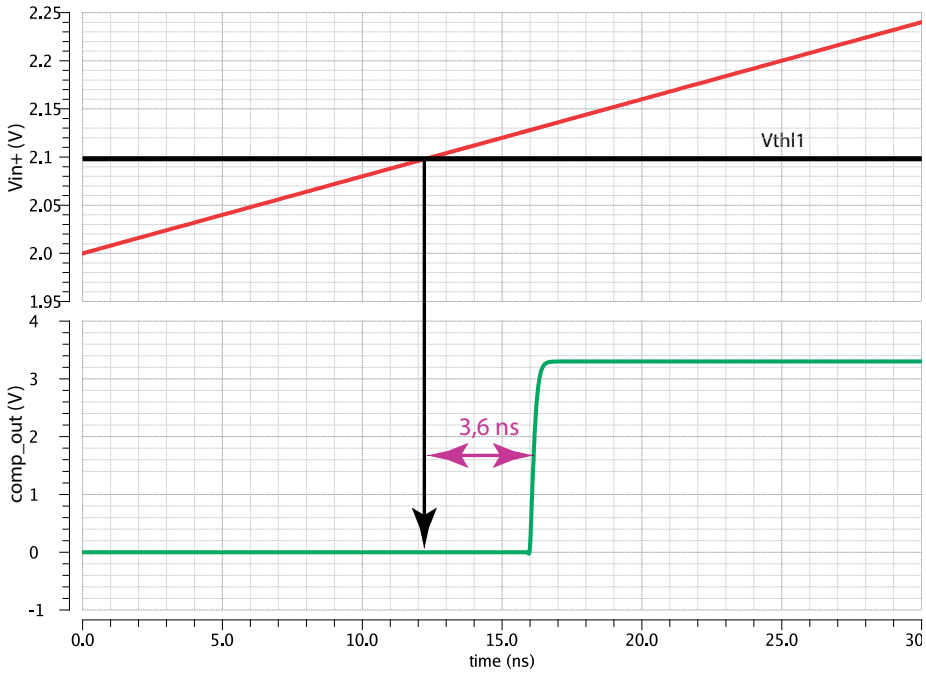

Figure 4.20 – Transient simulation of comparator's input and output voltages

There are four similar comparators in each channel. Each comparator is designed as an open loop two stage amplifier and its schematic is presented in figure 4.19. The open loop gain of the comparator is 68 dB. The simulation of a transition is shown in figure 4.20 for a threshold value of V_{thl1} = 2.1 V. The comparator triggers after 3.6 ns for an input current of I_{in}= 1 μA and this delay is added to the total time for the discharging circuit's operation t_{cycle}. In order to

be able to accurately measure 5 μA, the t_{cycle} is required to be less than 100 ns. Regarding the expected non-idealities, the comparator offset is equivalent to a threshold offset. Since the conversion is carried out through charge balancing there is no dependence between the conversion and the comparator's threshold voltages and offset.

4.8.4 Discharging circuits of channel 1

The discharging circuits of channel 1 are implemented as parasitic insensitive switched capacitor circuits. The schematic of the low range discharging circuit is presented in figure 4.21. Both circuits are identical and share the same voltages $V_{charge+}$, $V_{charge-}$ and V_{cm} and their only difference is the value of the capacitor C_{ref} and the width W of their switches.

For the low range discharging circuit of channel 1, C_{ref1}= 100 fF and the sizing of the $M1$ and $M2$ switches is $W/L(nmos)$= 0.6μm/0.35μm. The non-overlapping control signals s_1, s_2, s_3 and s_4, generated from the monostable's *"discharge"* signal, are shown in figure 4.22. The sequencing of the switches is designed in order to avoid any charge loss.

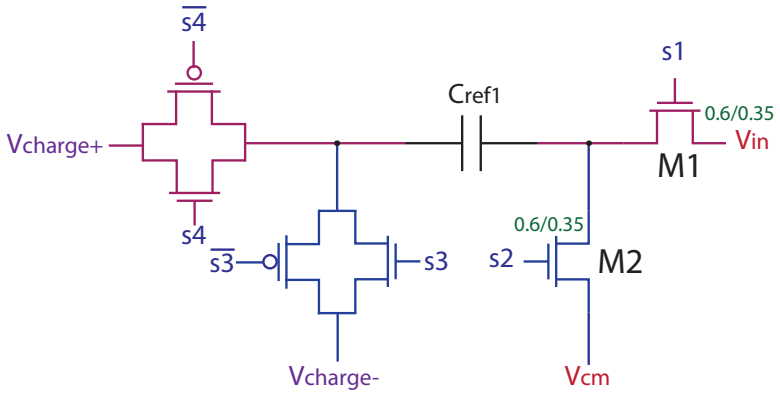

Figure 4.21 – Low range switched capacitor discharging circuit

Table 4.6 – Simulated Charge Injection Error

M1	M2	Integrator's output voltage difference	Injected charge
W_1 = 0.6 μm	W_2 = 0.6 μm	8.8 μV	8.8 αC
W_1 = 0.7 μm	W_2 = 0.5 μm	-177 μV	-177 αC
W_1 = 0.5 μm	W_2 = 0.7 μm	195 μV	195 αC

The switches $M1$ and $M2$ are connected to the virtual ground V_{in} and to the common mode V_{cm} nodes respectively. They are implemented using single nMOS transistors. The transmission gates that connect the reference capacitor to $V_{charge+}$ and $V_{charge-}$ voltages, allow the selection of rail-to-rail signals. The single nMOS transistors $M1$ and $M2$ are selected to be of minimum size to reduce the effects related to charge injection. By opening first the $M2$ switch, signal dependent charge injection is avoided [87], [95].

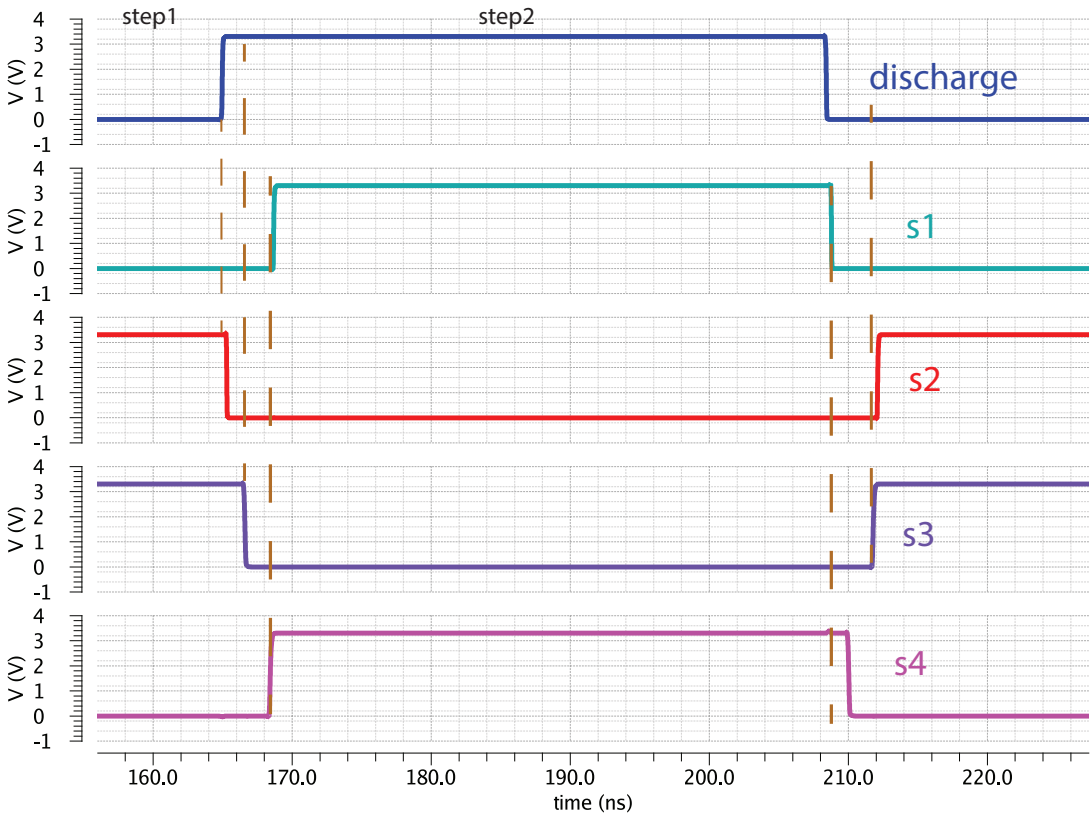

Figure 4.22 – Signals generated from the NOC that manage the switches of the switched capacitor circuits. The presented signals correspond to nMOS switches

The charge injection of the switched capacitor circuit switches in channel 1 is simulated for a variation of the width of the switches. This is performed by intentionally modifying the width of the switches M_1 and M_2. The $V_{charge+}$ and $V_{charge-}$ are connected to the same voltage as V_{cm}. A behavioral model of the OTA is used for this simulation to avoid the effects due to offsets. Table 4.6 shows the simulated charge injected from the switches by observing the integrator's output voltage. The resulting error due to charge injection is less than 0.2% of the ideal reference charge Q_{ref1}. This error is acceptable, so alternative techniques like half-sized dummy switches or differential operation for charge injection cancellation [92], [96] were not considered necessary.

4.8.5 Monostable

The monostable's schematic is depicted in figure 4.23. As an input, it accepts the comparator's output and an external signal named *"mono_test"* that is only used for calibration. As long as the comparator's positive input stays above the threshold V_{thl1}, the comparator's output signal *"comp_ol1"* is high and the monostable alternates between charging and discharging phases as shown in figure 4.24. The monostable's output is the converter's output and also the signal that generates the controls for the reference charge circuits. Multiple charge injections

of the Q_{ref1} occur until the charge accumulated in the feedback capacitance C_{f1} is balanced.

The duration t_{cycle} of the charging t_{charge} and discharging $t_{discharge}$ phases of the *"discharge"* pulse, can be controlled through the externally set voltages V_{BF} and V_{BR}. These voltages control the I_n and I_p currents of the current mirrors shown in figure 4.23. A lookup table has to be created when calibrating the chip, where the V_{BF} and V_{BR} voltages are matched to the t_{charge} and $t_{discharge}$ times.

Since *"discharge"* is the signal that generates the non-overlapping clocks that manage the reference charge injection, its duration can be adapted according to the input current and the different detector capacitances. The aim of this is to form and deliver to the input an accurate charge Q_{ref} for the charge balancing operation. If t_{cycle} is too short, the delivered charge is not accurate and if it is too long, the measured counts will deviate from the real number of counts for high input currents. This is why the calibration of the t_{cycle} duration is mandatory.

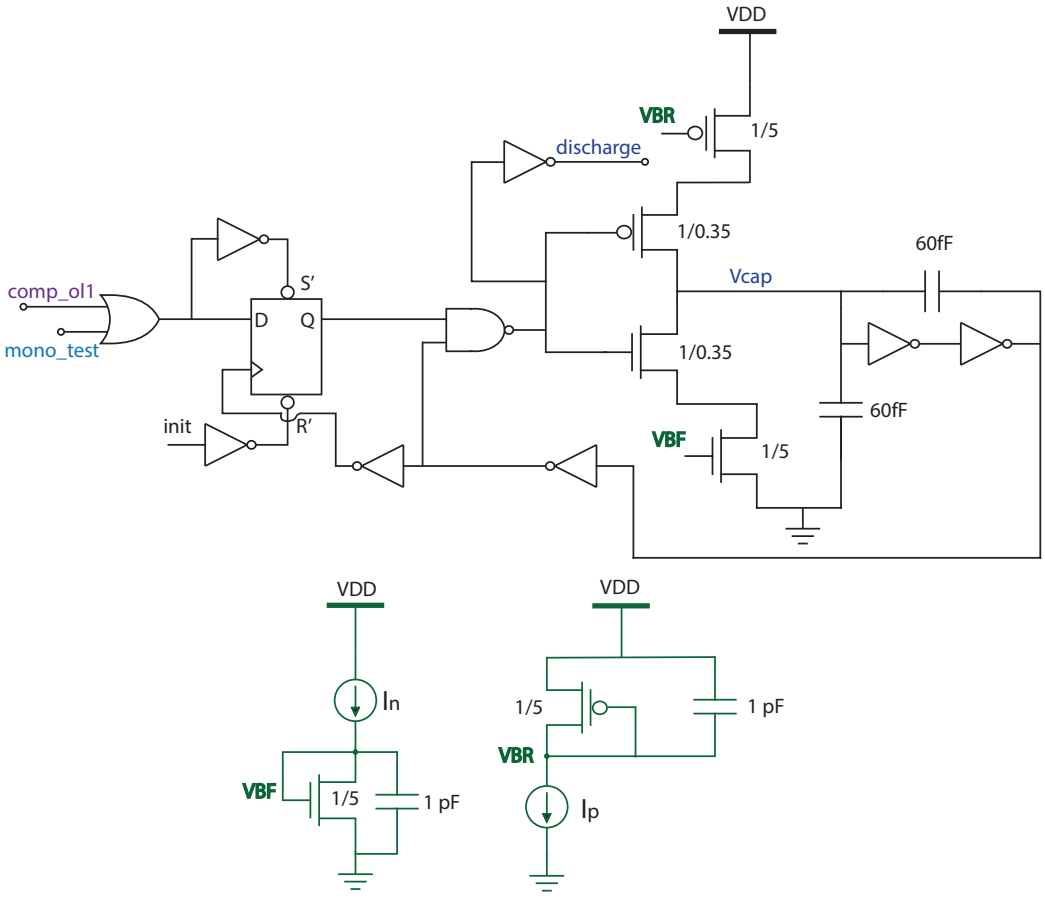

Figure 4.23 – Monostable schematic

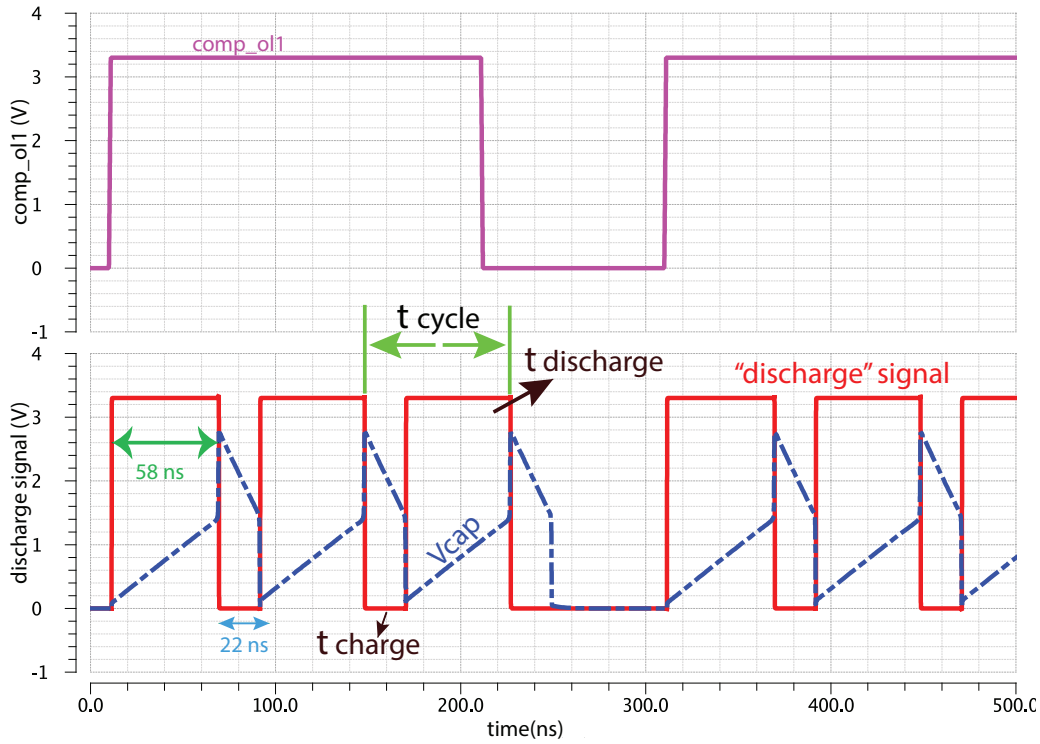

Figure 4.24 – Simulation of *"comp_ol1"* and *"discharge"* when V_{BR}= 1.68 V and V_{BF}= 1.94 V

4.8.6 Non-overlapping signals and control of the two ranges in the measuring channel

The s_1, s_2, s_3 and s_4 non-overlapping signals presented in figure 4.22 guarantee that the charge transfer happens correctly and no charge is lost. They refer to nMOS switches for simplicity. The schematic of the non-overlapping circuit is shown in figure 4.25.

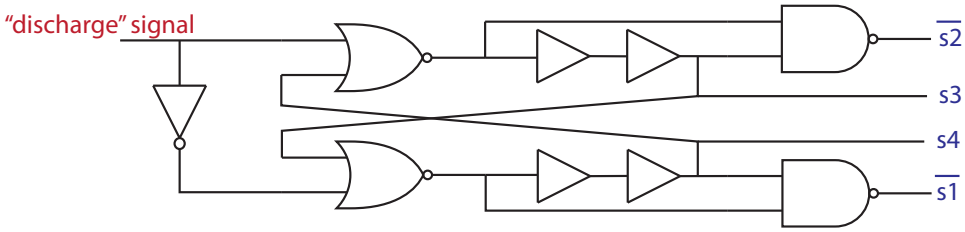

Figure 4.25 – Non-overlapping clock circuit

When the input current is low and only the V_{thl1} is crossed, only the low range control is active. When the second comparator triggers and its output *comp_oh1* goes high, the high range control is also activated and the $Q_{ref1high}$ discharging circuit is connected in parallel to the Q_{ref1} discharging circuit. The schematic of the control circuit of the high and low range is shown in figure 4.26, where both switched capacitor circuits are injecting the total reference charge. As shown in figure 4.27 of the high range control circuit, when the second range is

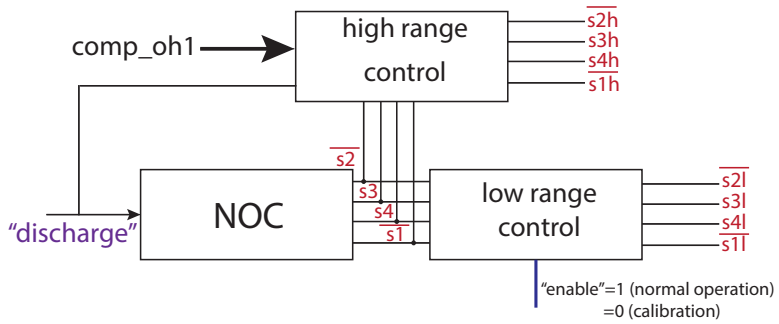

Figure 4.26 – Controls of high and low range for channel 1

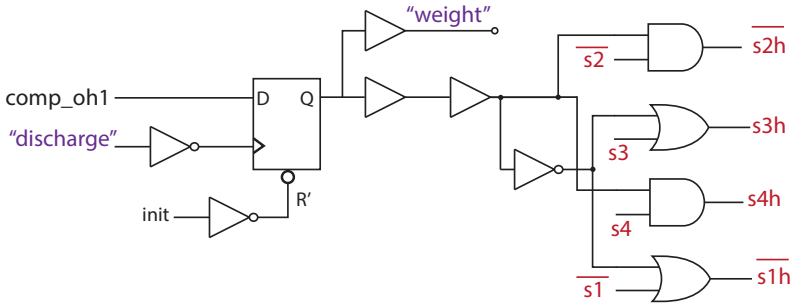

Figure 4.27 – High range control circuitry

enabled, the signal *"weight"* that is the second output of the first channel becomes logic '1'. By combining both *"discharge"* and *"weight"* signals, the input current can be calculated as shown in equation (4.4). In the low range control block, there is an additional *"enable"* signal that can disable the low range injection for calibration purposes.

4.8.7 Discharging circuit of channel 2

The schematic of the discharging circuit of the second channel of the ASIC is shown in figure 4.28. This switched capacitor circuit is able to inject bipolar charges by changing the phases of the switches $s3$ and $s4$ using multiplexers and the external signal named *"polarity"*. The *"polarity"* signal depends on the comparator that is triggered according to the leakage current polarity. The reference charge Q_{ref2} balances the integrated charge in channel 2, but also compensates for the leakage current of channel 1. The Q_{ref2} injection to channel 2 or to channel 1 is managed by the *"select_channel"* control signal that injects into channel 2 when it is "low" and into channel 1 when it is "high". The *"charge_inject"* signal, similarly to the *"discharge"* signal of channel 1, manages the switches s_1, s_2, s_3 and s_4 of the discharging circuit.

The discharging circuit of channel 2 can be also used for calibration purposes, for the estima-

tion of the relative charge ratio between Q_{ref1} and Q_{ref2} and between $Q_{ref1high}$ and Q_{ref2}. The calibration of the ASIC will be presented in chapter 5.

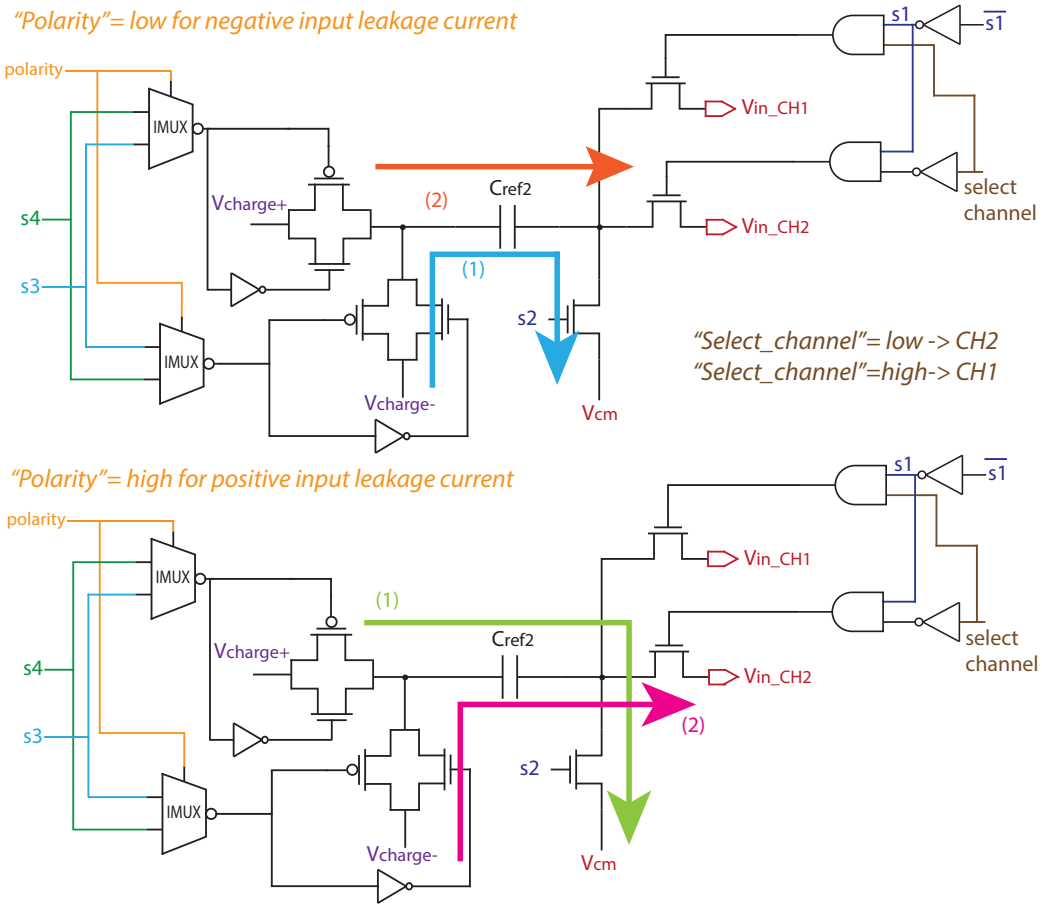

Figure 4.28 – Schematic of the discharging circuit of channel 2 for both polarities

4.8.8 Noise evaluation

The simulations of the noise related to the circuit's operation are presented in this section. As explained earlier, the jitter in the *"discharge"* signal caused by noise in the OTA's output and noise in the comparator, should not cause any error in the expected number of counts.

The histogram of the jitter when the input current is I_{in}= 1 μA is shown in figure 4.29. It is calculated as the difference between the *"discharge"* and the first crossing of the comparator's threshold V_{thl1}. The standard deviation is calculated to be 0.4 ns, which is well below t_{cycle}.

Figure 4.30 shows the noise sources across the switched capacitor C_{ref} for the two phases of operation. The Power Spectral Density (PSD) of the voltages across C_{ref} during charging and discharging phase is shown in figure 4.31. It can be observed that during the charging phase the noise is due to the switches. During the discharging phase the $1/f$ noise due to the OTA can be also identified.

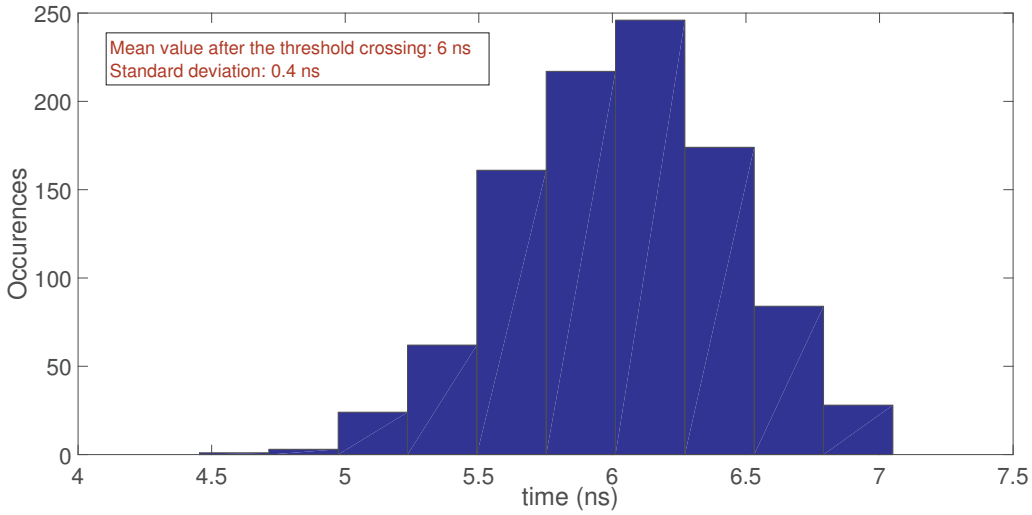

Figure 4.29 – Jitter in the *"discharge"* signal

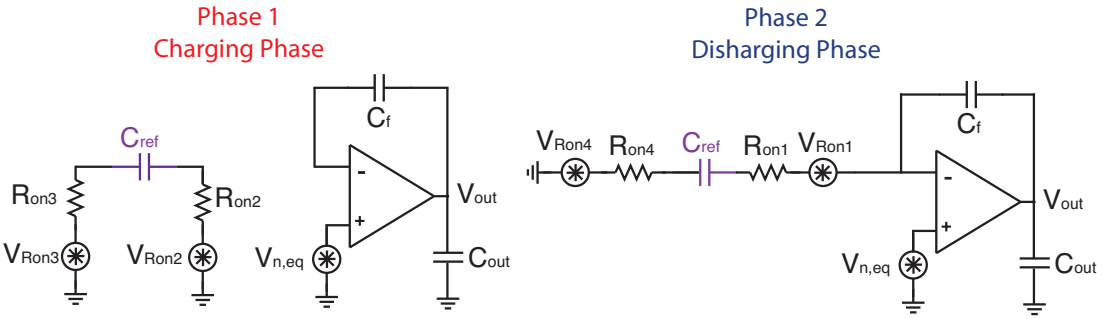

Figure 4.30 – Noise across C_{ref} capacitor during charging and discharging phase

The $V_{RMS(dis)}$ during the discharging phase for a continuous circuit operation of 10 years is calculated as:

$$V_{RMS(dis)} = \sqrt{\int_{3.17 \cdot 10^{-9}}^{10^{10}} PSD(f)df} = 201.3\mu V \tag{4.22}$$

The $V_{RMS(ch)}$ during the charging phase for a continuous circuit operation of 10 years is calculated as:

$$V_{RMS(ch)} = \sqrt{\int_{3.17 \cdot 10^{-9}}^{10^{10}} PSD(f)df} = 200.3\mu V \tag{4.23}$$

So the $V_{RMS(cycle)}$ for a single charging and discharging operation is calculated to be 284 μV.

The $V_{RMS(1/f)}$ due to the $1/f$ noise can be evaluated from the $1/f$ part of the curve of figure 4.31. The $V_{RMS(1/f)}$ can by expressed by equation (4.24), since PSD= $1 \cdot 10^{-12} V^2/Hz$ when f= 1 Hz.

$$V_{RMS(1/f)} = \sqrt{\int_{3.17 \cdot 10^{-9}}^{10^{10}} \frac{1 \cdot 10^{-12}}{f} df} = 6.52 \mu V \tag{4.24}$$

The evaluation of the $1/f$ noise was performed from a very low frequency that corresponds to the time between two calibrations. It was estimated for the worst case that a calibration is performed every 10 years.

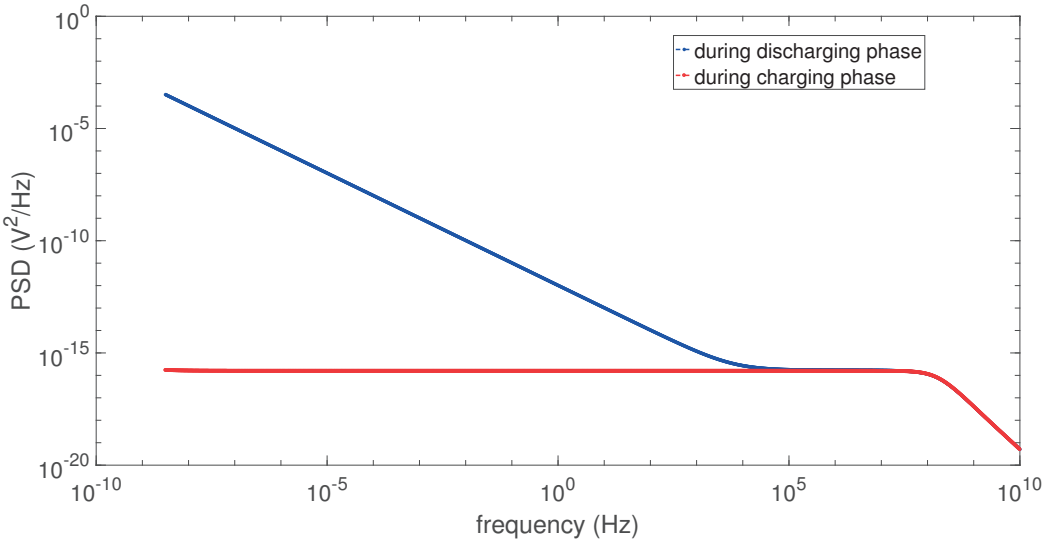

Figure 4.31 – PSD of the voltages across C_{ref} during charging and discharging phase

The wideband noise is improved by averaging if more samples are taken, because the samples are not correlated. This is why the worst case corresponds to one single cycle. The RMS value of the noise can be reduced by $\sqrt{N_{counts}}$. However it cannot be reduced below the $1/f$ noise floor. For C_{ref1}= 100 fF that is the capacitance of the low range of channel's 1 switched capacitor circuit, the equivalent noise on the V_{ref} is given by equation (4.25).

$$ENV_{ref} = \sqrt{\frac{284^2}{N_{counts}} + 6.52^2} \mu V \tag{4.25}$$

The SNR when V_{ref}= 1 V is given by equation (4.26).

$$SNR = 20log\frac{V_{ref}}{ENV_{ref}} \tag{4.26}$$

In figure 4.32 that shows the equivalent noise on the V_{ref} contribution and the SNR versus the number of counts N_{counts}, the SNR improves until it reaches the $1/f$ noise floor. It can be concluded that when the V_{ref} decreases below 1 V in order to scale the Q_{ref}, the SNR will decrease.

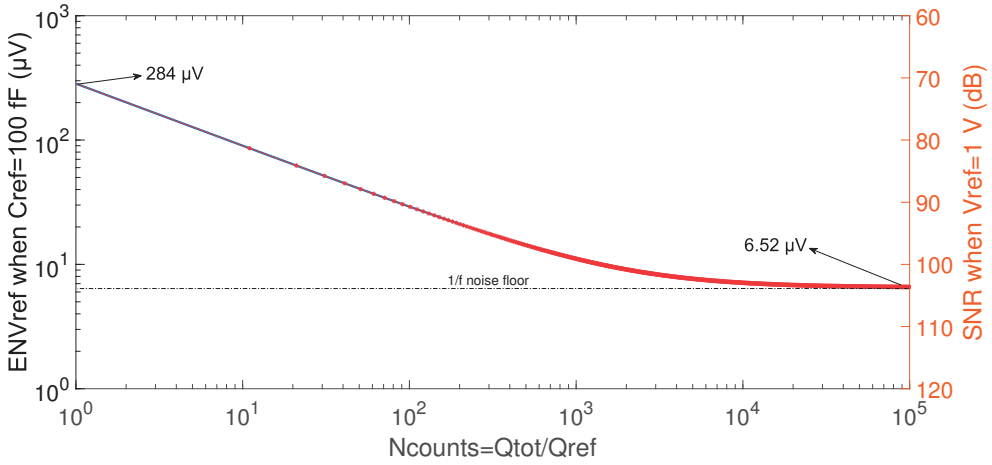

Figure 4.32 – V_{ref}-referred noise contribution of C_{ref} switching noise versus number of counts N_{counts}

4.9 System Integration

Table 4.7 summarizes the electrical characteristics of Utopia 2 ASIC.

The Utopia 2 ASIC picture is shown in figure 4.33. The chip size is 2.75 mm x 2.75 mm including 13 pads per side. The chip is implemented in AMS 0.35 μm CMOS C35B4C3 4M/2P/HR/5V IO process as part of a Multi Project Wafer (MPW) run. The large devices i.e. the ESD protection diodes of this technology are better for a good matching, which is a prerequisite for the proposed leakage current compensation technique. The power consumption of the Utopia 2 ASIC is 8.25 mW.

The padring is designed with three different power domains. There is the first analog domain for the analog inputs and outputs, the digital power domain and a second analog power domain dedicated to the ESD protection power supply of the inputs. This second analog domain includes the sensitive input nodes IN_1, IN_2 and the V_{cm}.

Table 4.7 – Summary of Utopia 2 ASIC Characteristics

Technology	AMS 0.35 μm
Power Supply	3.3 V
Power Consumption	8.25 mW
Die Size	2.75 mm x 2.75 mm
Number of Channels	2
Gain A_0 of OTA	76.4 dB
g_m of OTA	3 mS
GBW of OTA	430 MHz
Phase margin ϕ	50 deg
V_{os} of OTA (3σ)	< 5 mV

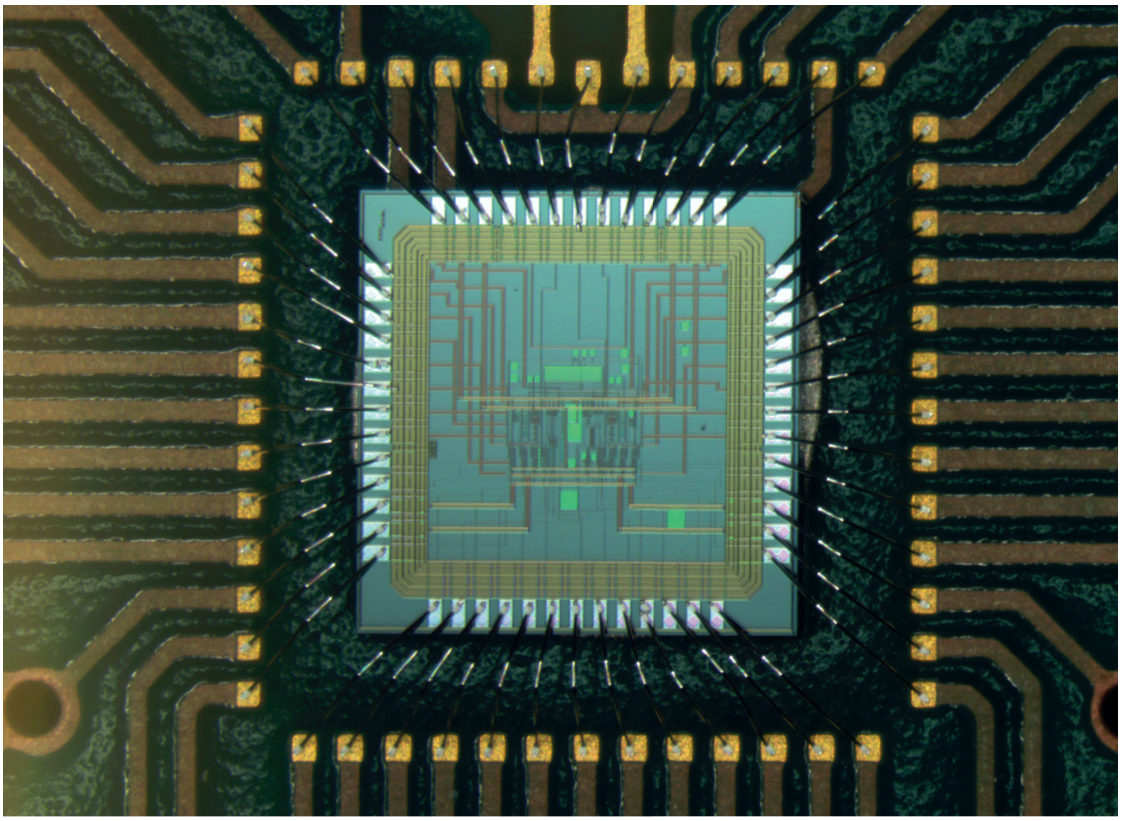

Figure 4.33 – Utopia 2 microscopic picture

4.9.1 Minimize leakage currents at system level

The Utopia 1 ASIC revealed the challenges and proposed solutions in leakage current measurements. According to the guidelines that it set, the Utopia 2 ASIC is directly bonded on the

PCB to avoid any leakage current related to the package. Additionally, in order to limit the leakage current related to the different voltage of the adjacent pins, the input pads IN_1 and IN_2 are surrounded by V_{cm} pads as shown in figure 4.34. The guarding principle is based on surrounding the high impedance conductors with another guard conductor that is at the same potential, so there is no voltage drop across the insulation resistance. At system level, triaxial connectors and low noise triaxial cables [97], guarantee that all external leakage currents are minimized. The input nodes are surrounded by traces connected to V_{guard} voltage. The V_{guard} can be driven to a voltage equal to V_{cm}. The PCB was carefully designed to avoid any stray leakage currents close to the input nodes. Internal power planes were not placed under the sensitive nodes.

The *VDDA1* is the adjustable upper power supply voltage of the second analog domain that surrounds the input pads. The leakage current related to the ESD protection diodes of the input IN_1 and IN_2 pads can change according to the selected voltage *VDDA1*. The schematic of the inputs, including the ESD protection diodes that are connected to *VDDA1*, is shown in figure 4.35.

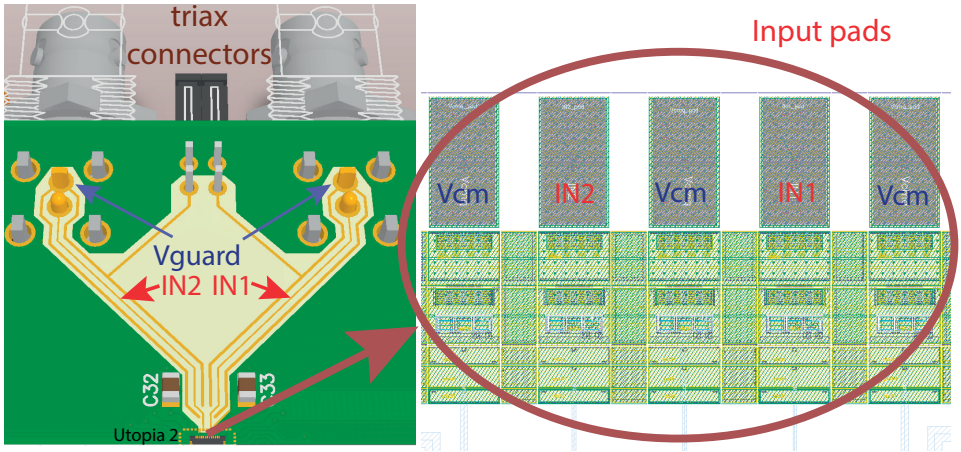

Figure 4.34 – Utopia 2 PCB input and pads

4.9.2 Printed circuit board (PCB)

The printed circuit board that hosts the Utopia 2 ASIC is shown in figure 4.36. Digital to analog converters (DACs) were placed on the PCB to set the required reference voltages V_{cm}, $V_{charge+}$, $V_{charge-}$, V_{BR} and V_{BF}. These accurate ultra-low noise voltage references have a temperature coefficient equal to 3ppm/°C [98]. All the internally generated voltages V_{thl1}, V_{thh1}, V_{th_errh1}, V_{th_errl1}, V_{thp2}, V_{thn2}, V_{th_errp2}, V_{th_errn2} and V_{init} can be also set externally using DACs for correction purposes.

For the PCB design, the mounting holes for the input triaxial connectors were enlarged to provide more flexibility during the measurement procedure. That way, even simple BNC connectors could fit and measurements using coaxial cables could be also performed [99].

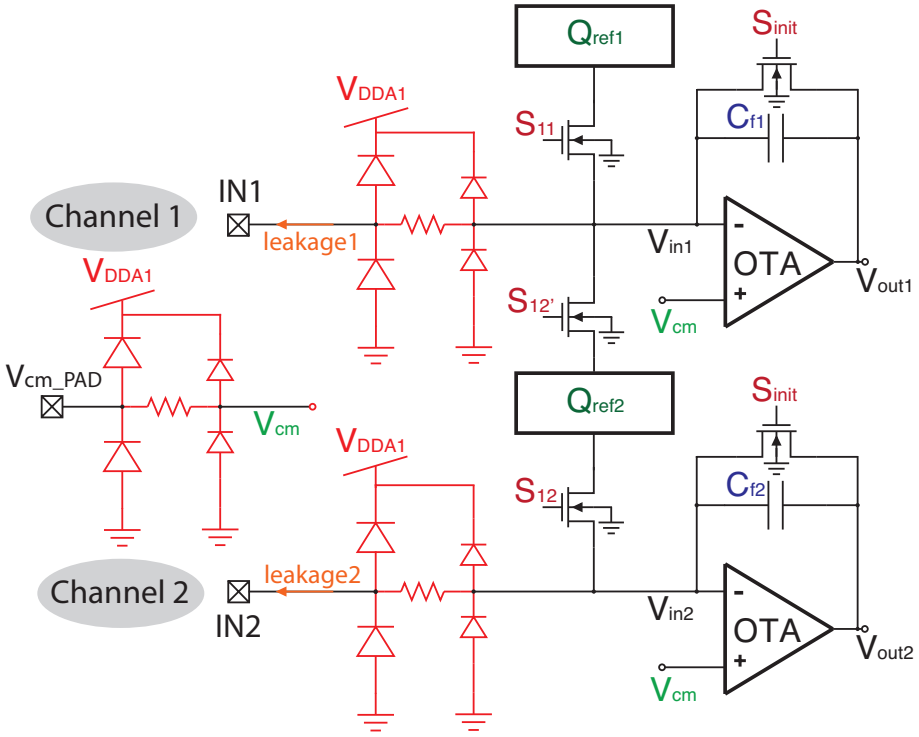

Figure 4.35 – Utopia 2 input pads with their ESD protection diodes

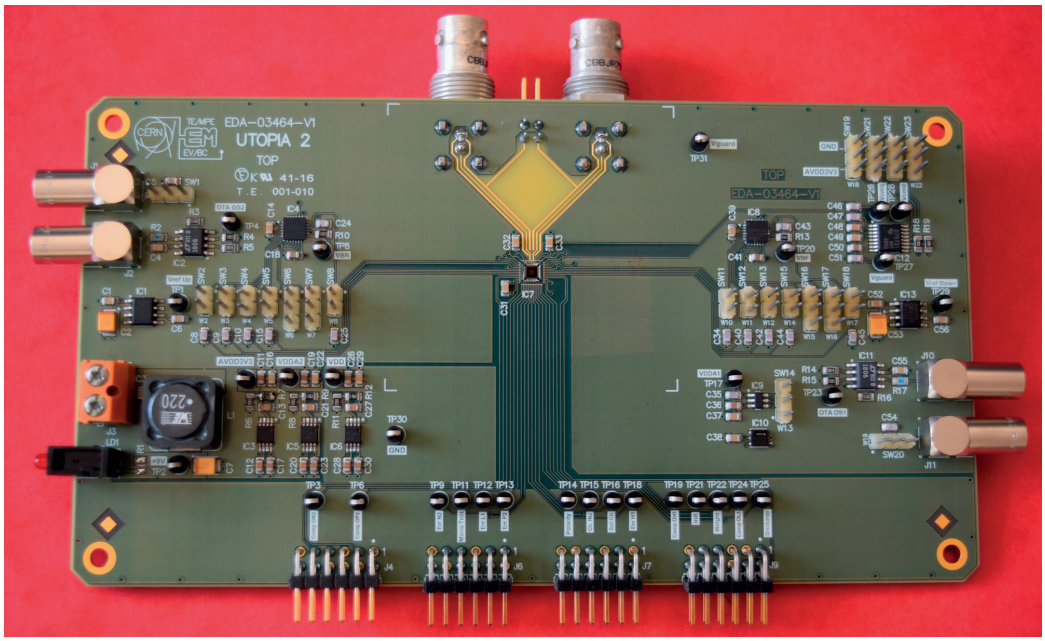

Figure 4.36 – Utopia 2 PCB

The ionization chambers that are currently used by CERN's radiation protection group are connected using coaxial cables.

A temperature and humidity sensor [100], was also placed on the printed circuit board to evaluate the environment conditions during testing, since the delicate leakage current measurements are strongly influenced by temperature and humidity.

The PCB was placed inside a metallic shield box to limit interference from external sources. Furthermore, the input ESD protection diodes are light sensitive so the chip should be covered and properly sealed.

4.10 Chapter Conclusions

The architecture of the Utopia 2 ASIC was presented. The system is based on the asynchronous CFC topology and charge balancing, where the input current is integrated and the corresponding number of counts is calculated according to the number of reference charge injections that balance precisely the charge that is integrated. Compared to the Utopia 1 ASIC, this chip includes the following extra functionalities. The measuring channel's output frequency is 10 times higher, since the reference charge is scaled down 10 times. In order to maintain the same dynamic range in the upper end, a second switched capacitor circuit is connected in parallel with the first one to increase the injected reference charge. A second channel whose input structures are matched to the first channel is used for the leakage current compensation.

The ASIC's design procedure was described along with the expected non-idealities. The schematics of the most important blocks were presented and analyzed. The Utopia 2 ASIC will be used as the basis for the front-end of the new radiation monitoring system at CERN. The next chapter presents the calibration procedure and the characterization of the designed chip.

5 Characterization of the Utopia 2 ASIC

5.1 Introduction

This chapter presents the characterization and the measurements of the Utopia 2 ASIC and is organized as follows.

The calibration procedure of the charging and discharging times of the switched capacitor circuit and the calibration of the reference charges are presented. Then the ratio of the leakage current between channel 1 and channel 2 is calculated and will be used for the active leakage current compensation.

The rest of the chapter shows the achieved measurement range of the Utopia 2 ASIC using laboratory current sources. It also presents additional and more precise measurements that were performed at the Swiss Federal Institute of Metrology (METAS), using an accurate calibrated current source. Finally the qualitative radiation measurements that were taken as a proof of concept with the ASIC connected to an ionization chamber detector are shown.

5.2 Data Acquisition System

A data acquisition (DAQ) system was designed based on the ARTY Evaluation board that includes an Artix-7 Field Programmable Gate Array (FPGA) from Xilinx [101]. The DAQ system provides the necessary counters used for counting the number of charge injections for channel 1 and channel 2 of the ASIC under test. For channel 1, the number of charge injections N_1 of Q_{ref1} in the measurement time window and the number of times N_{1high} that the $Q_{ref1high}$ is activated and injects in parallel with Q_{ref1} are counted. These counts are measured using the *"discharge"* and the *"weight"* signals.

For channel 2, the counters measure the number of times N_{2p} or N_{2n} that the integrator's output crosses the V_{thp2} or V_{thn2} thresholds respectively. These counts are measured using the *"comp_op2"*and the *"comp_on2"* signals. The data is transferred to a PC via a UART to USB connection. Additionally, the FPGA controls the *"charge_inject"*, *"select_channel"* and

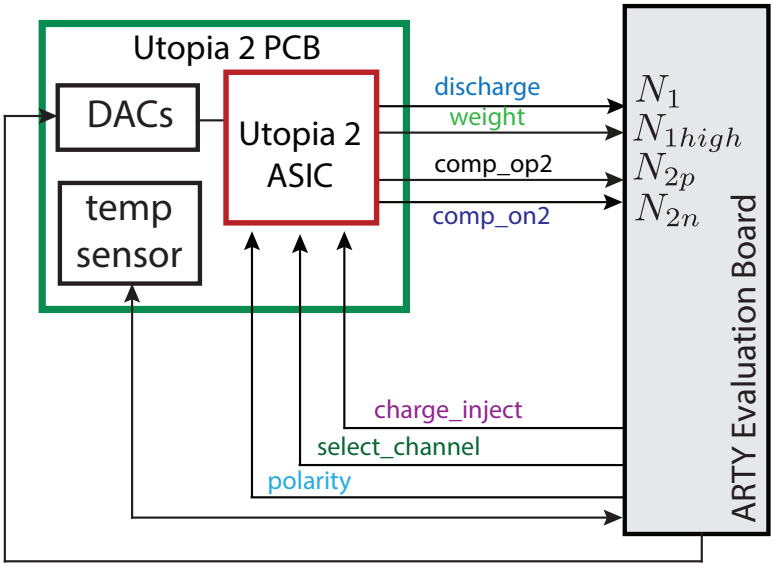

Figure 5.1 – Block diagram of Utopia 2 measuring system

"polarity" signals of channel 2. It also sets the values of the digital to analog converters (DACs) of the Utopia 2 PCB via an I2C bus. The Utopia 2 PCB and the DAQ board with their interface card are depicted in figure 5.2.

Python routines control the operation of the DAQ. The acquired data are then processed using Matlab. The DAQ system was implemented by Dr. Matthew Noy.

5.3 Calibration Procedure

In section 4.5, where the design procedure of the Utopia 2 ASIC was analyzed, the expected non-idealities were presented. They were taken into consideration and were included in the calibration phase of the system. Some extra inputs and circuitry were introduced to facilitate the calibration procedure. These additional inputs are the *"mono_test"* input and the *"enable_low_controls"* input for channel 1.

The calibration procedure is performed in three steps, as shown in figure 5.3. Firstly, a lookup table should be built where the charging t_{charge} and discharging $t_{discharge}$ times of the phases of the switched capacitor circuits are linked to the input voltages V_{BF} and V_{BR}. Secondly, the reference charges that set the gain of the conversion should be calibrated. Finally, the leakage currents of channel 1 and channel 2 should be measured for different temperatures and their ratio has to be calculated. This is the ratio ρ that will be used for the active leakage current compensation.

In the end of the calibration procedure, the parameters that should be fixed are the voltages $V_{charge+}$, $V_{charge-}$, V_{cm}, V_{BR}, V_{BF}, $VDDA1$ and V_{guard}.

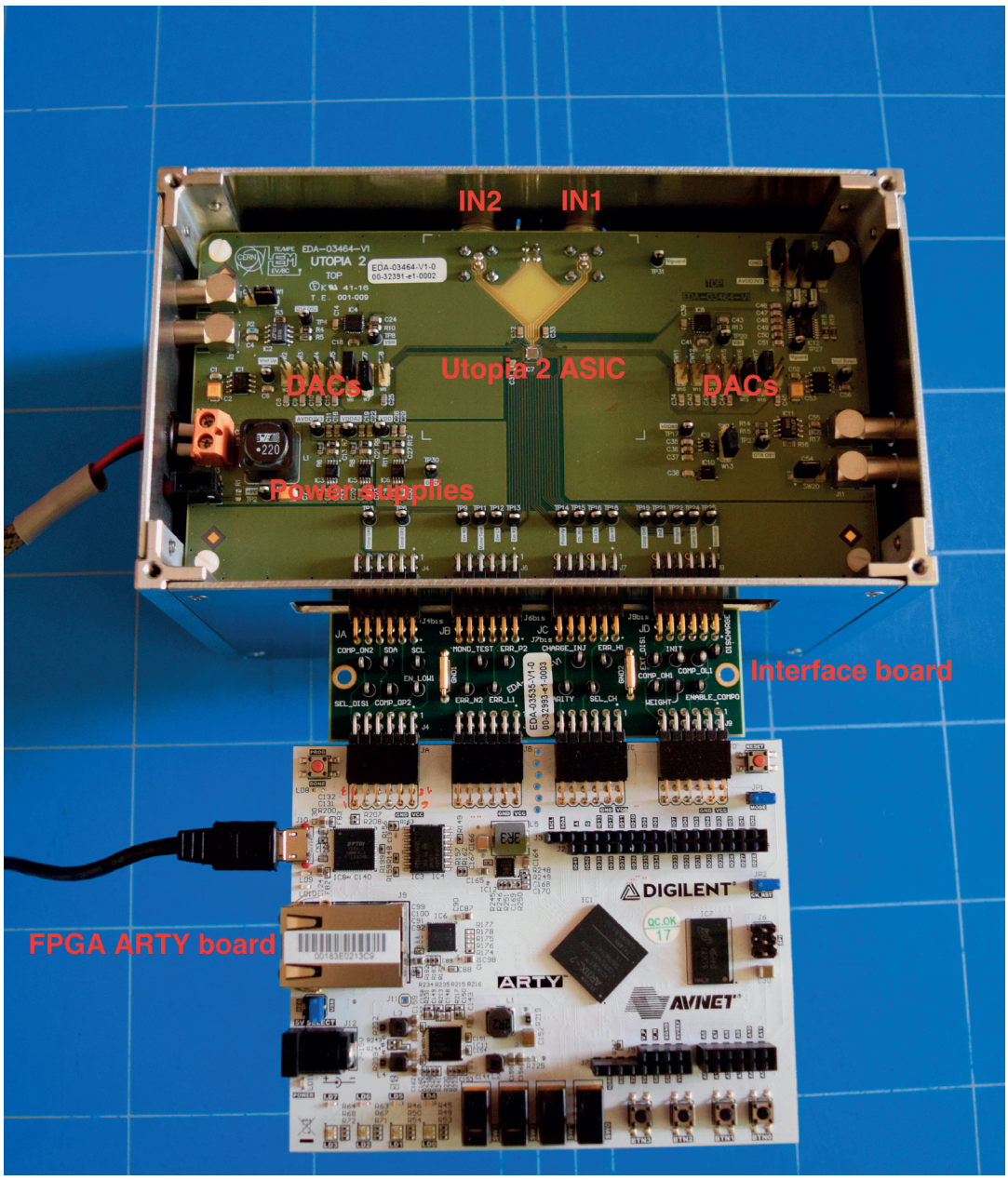

Figure 5.2 – Utopia 2 PCB and DAQ board

5.3.1 Charging and discharging time calibration

To guarantee that the conversion is correct, the total reference charge should be delivered to the input. As already discussed in chapter 4, the charging t_{charge} and discharging $t_{discharge}$ times of the *"discharge"* signal of the monostable, are responsible for the timing of the switched capacitor circuit operation. The *"discharge"* signal generates the s_1, s_2, s_3 and s_4 signals shown in figure 4.22. The $t_{discharge}$ that is the time during which the *"discharge"* signal is high, should be long enough so that the switched capacitor circuit delivers an accurate reference charge

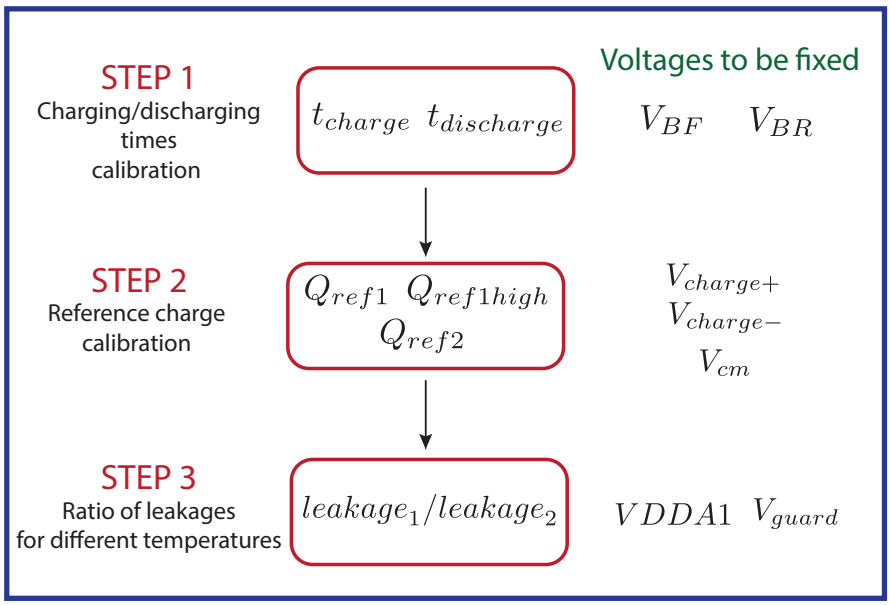

Figure 5.3 – Utopia 2 ASIC calibration procedure

to the input. The time constant of the discharging operation is affected by the detector's capacitance C_{det}, especially in the μA range. The t_{charge} is responsible for the sampling time of Q_{ref} and should be long enough for the accurate formation of Q_{ref}.

For the highest input current the system's operating frequency increases and there is a limit in the value of t_{cycle} as shown in equation (5.1).

$$t_{charge} + t_{discharge} = \frac{Q_{ref1} + Q_{ref1high}}{I_{max}} = \frac{500fC}{5\mu A} = 100ns \tag{5.1}$$

These are the reasons why the t_{charge} and the $t_{discharge}$ have to be externally adjustable according to the detector's input characteristics and the circuit's operating conditions.

Initially, the t_{charge} and the $t_{discharge}$ times were measured with respect to the selected V_{BF_DAC} and V_{BR_DAC} values. The V_{BF_DAC} and V_{BR_DAC} voltages are provided externally through DACs, the V_{BF} and the V_{BR} voltages are the measured voltages in the inputs of the chip and the I_n and I_p are the corresponding biasing currents in the current mirrors of the monostable that are calculated from equations (5.2) and (5.3), where R_1= 300 kOhms and R_2= 100 kOhms respectively.

$$I_n = \frac{V_{BF} - V_{BF\_DAC}}{R_1} \tag{5.2}$$

$$I_p = \frac{V_{BR} - V_{BR\_DAC}}{R_2} \tag{5.3}$$

In order to perform the t_{charge} and $t_{discharge}$ calibrations, positive input current was injected into channel 1 and the analog output *"ota_out1"* was saturated to the negative power supply rail. The *"mono_test"* signal forced the monostable to alternate between charging and discharging phases.

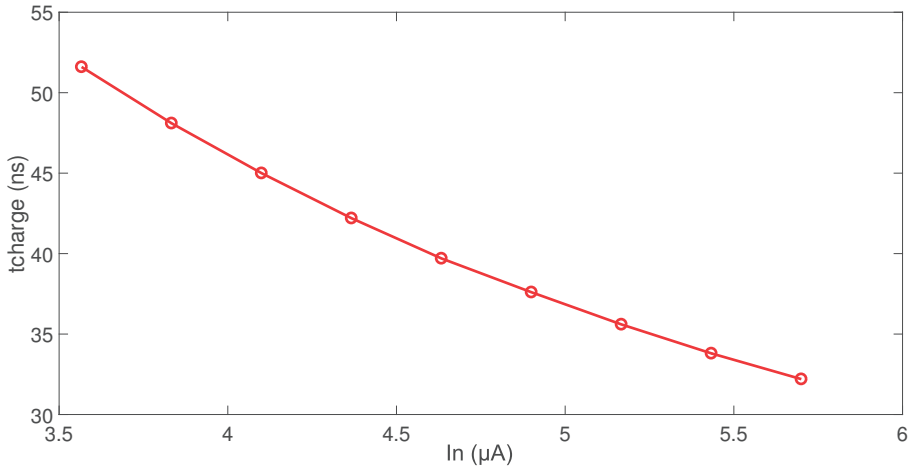

Figure 5.4 – Charging time t_{charge} of the switched capacitor circuit versus I_n

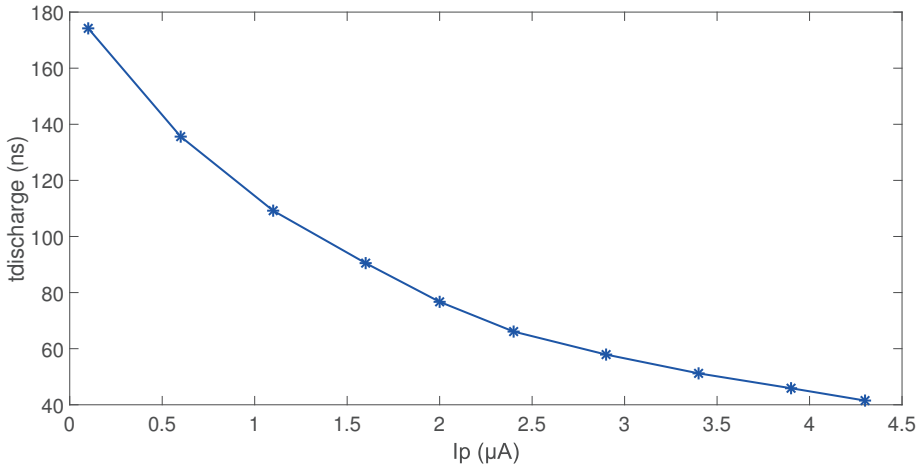

Figure 5.5 – Discharging time $t_{discharge}$ of the switched capacitor circuit versus I_p

The pulse width of these cycles was measured using an oscilloscope and a lookup table was created. The t_{charge} and $t_{discharge}$ times versus the injected biasing currents I_n and I_p plots are shown in figures 5.4 and 5.5.

For the measurements presented in this chapter the selected values are I_n= 5 μA and I_p= 3 μA.

5.3.2 Reference charge calibration

As discussed in chapter 4, the reference charge depends on the capacitor value C_{ref}, the reference voltages $V_{charge+}$ and $V_{charge-}$, the static offset voltage V_{os} and the quality of the virtual ground. The reference voltages that are common for the three discharging circuits are externally set using ultra-high precision voltage references [98].

The calibration procedure that is followed in order to characterize the Q_{ref1}, $Q_{ref1high}$ and Q_{ref2}, is depicted in the block diagram of figure 5.6 and in the flowchart of figure 5.7.

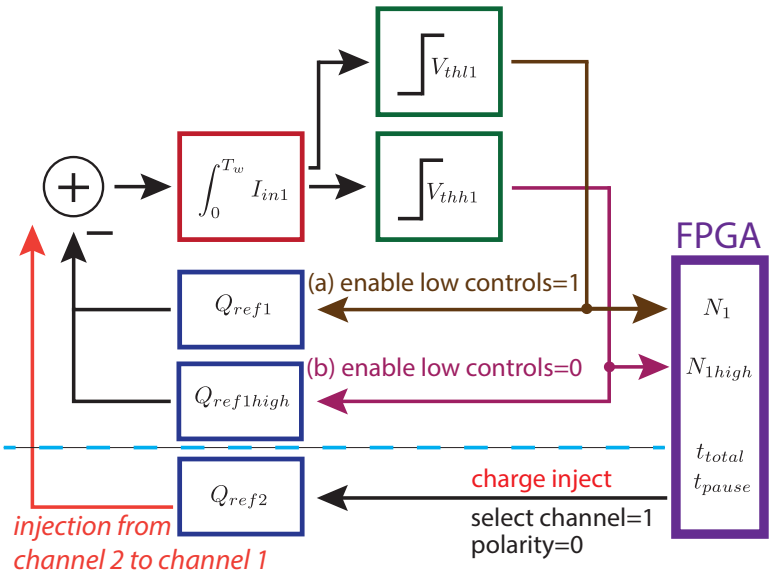

Figure 5.6 – Block diagram of the reference charge calibration

In order to find the relative ratio between the reference charges Q_{ref1} and Q_{ref2} and between $Q_{refhigh}$ and Q_{ref2}, the reference charge of the switched capacitor circuit of channel 2 is used as a charge injection source for channel 1. The *"polarity"* signal is set by the FPGA to inject negative charge and the *"select_channel"* signal is set to inject only to channel 1. The *"charge_inject"* signal pulse width can be adjusted so that the injected current from channel 2 to channel 1 varies. The timing of the *"charge_inject"* signal is shown in equation (5.4) and figure 5.8.

$$t_{total} = t_1 + t_2 + t_{pause} \tag{5.4}$$

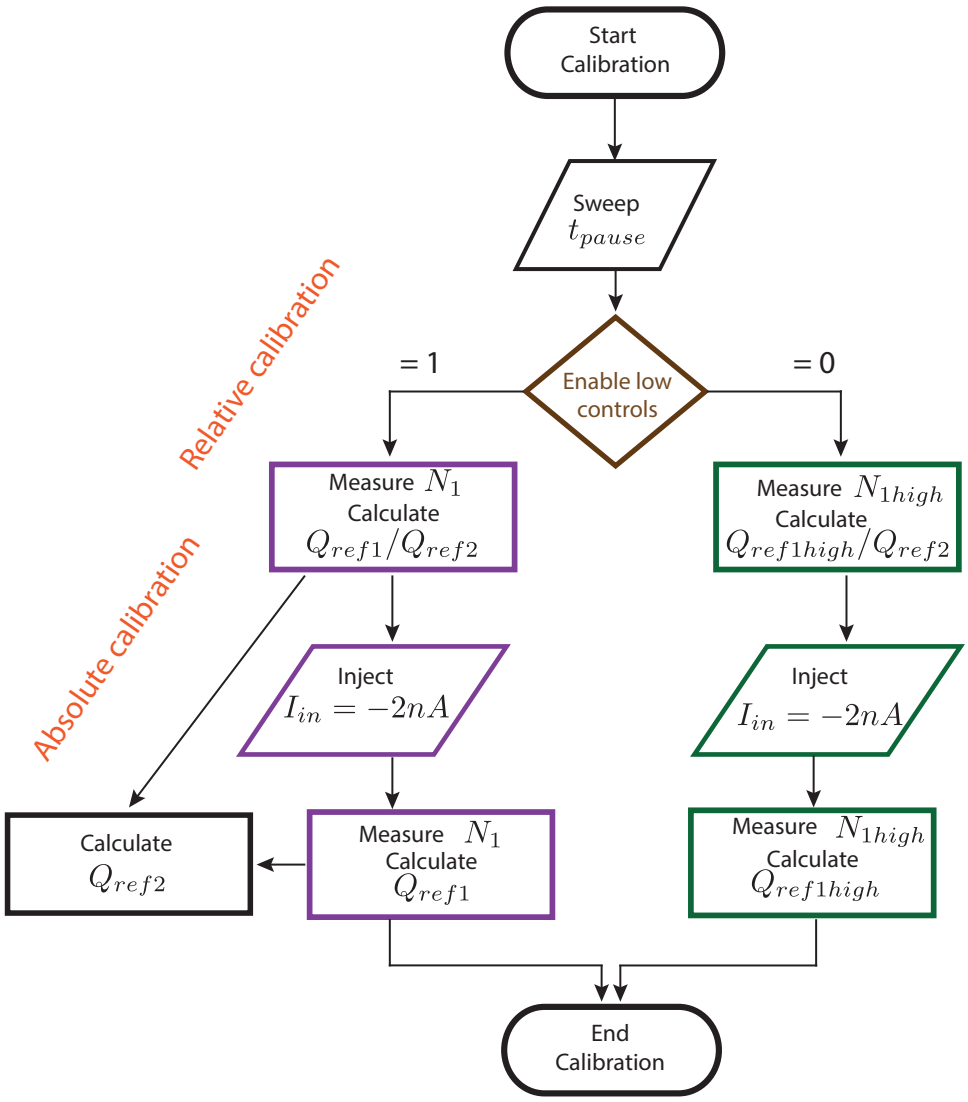

Figure 5.7 – Flowchart of the reference charge calibration procedure

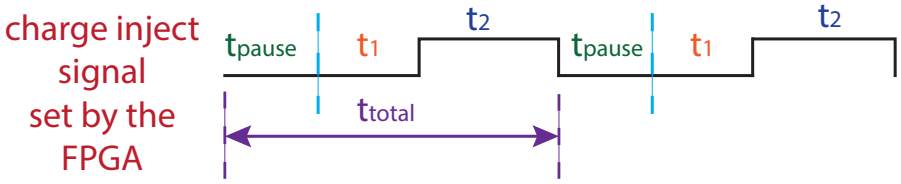

Figure 5.8 – *"Charge_inject"* signal during Q_{ref1}, $Q_{ref1high}$ and Q_{ref2} calibration

The number of charge injections N_2 from channel 2 to channel 1, in a specific time window T_w, is given by equation (5.5), so by controlling the t_{pause}, the injected current into channel 1 can be also controlled. The measured number of counts in channel 1 is noted as N_1. For the calibration procedure, the injected current should be in the nA range to avoid being affected

by the leakage currents.

$$N_2 = \frac{T_w}{t_{total}} = \frac{T_w}{t_1 + t_2 + t_{pause}} \tag{5.5}$$

The relative ratio between Q_{ref1} and Q_{ref2} is given by equations (5.6) and (5.7) for N_1 and N_2 sufficiently big.

$$\frac{Q_{ref1}}{Q_{ref2}} = \frac{N_2}{N_1} \tag{5.6}$$

$$\frac{Q_{ref1}}{Q_{ref2}} = \frac{T_w}{t_{total}} \cdot \frac{1}{N_1} \tag{5.7}$$

When the injected current is low enough such that the second comparator's V_{thh1} is not crossed, only the switched capacitor circuit that injects Q_{ref1} is activated. The ASIC is equipped with an input named *"enable_low_controls"*. In the normal operation of the ASIC the low range switched capacitor circuit is always enabled. However, for calibration purposes it can be disabled in order to evaluate the ratio between $Q_{ref1high}$ and Q_{ref2}, as shown in equation (5.8).

$$\frac{Q_{ref1high}}{Q_{ref2}} = \frac{T_w}{t_{total}} \cdot \frac{1}{N_{1high}} \tag{5.8}$$

Table 5.1 shows the t_{pause} values used to evaluate the ratio of the injected charge from channel 2 to channel 1 in a time window T_w. It also shows the measured number of counts N_1 in channel 1 when the *"enable_low_controls"* was active, the number of counts N_{1high} when the *"enable_low_controls"* was inactive and finally the relative reference charge ratio Q_{ref1} / Q_{ref2} and $Q_{ref1high}$ / Q_{ref2}. The ratios were calculated to be 11.5 and 47.6 respectively. For these measurements the t_1 was selected to be 120 ns and the t_2 was 100 ns.

To calculate the absolute value of the reference charges a constant current equal to I_{in}= - 2 nA was injected into channel 1 using a precise laboratory current source from Keithley [86]. In the time window T_w = 0.1 s the respective mean number of counts using the low range switched capacitor circuit was N_1 = 2138 and using the high range switched capacitor circuit was N_{1high} = 518. By using these values, the reference charges were calculated to be Q_{ref1}= 93.5 fC and $Q_{ref1high}$= 386 fC respectively.

Table 5.1 – Relative Calibration of Q_{ref1} and $Q_{ref1high}$

t_{pause} (μs)	t_{total} (μs)	N_1	Q_{ref1} / Q_{ref2}	N_{1high}	$Q_{ref1high}$ / Q_{ref2}
0.28	0.5	17400	11.504	4200	47.608
0.78	1	8690	11.506	2100	47.605
1.28	1.5	5800	11.504	1400	47.609
1.78	2	4350	11.505	1050	47.615
2.28	2.5	3480	11.505	840	47.608
2.78	3	2900	11.505	700	47.605
3.28	3.5	2480	11.505	600	47.611
3.78	4	2170	11.504	525	47.610

Table 5.2 – Calibrated Q_{ref1}, $Q_{ref1high}$ and Q_{ref2} values

	CHIP 1	**CHIP 2**	**CHIP 3**
Q_{ref1}	93.5 fC	93.5 fC	93.8 fC
$Q_{ref1high}$	386 fC	387 fC	388 fC
Q_{ref2}	8.12 fC	8.24 fC	8.12 fC

By solving one of the previous equations, for example equation (5.7), the reference charge Q_{ref2} of channel 2 is calculated to be Q_{ref2}= 8.12 fC.

The same procedure has to be repeated for all the chips. Table 5.2 presents the calibrated reference charges Q_{ref1}, $Q_{ref1high}$ and Q_{ref2} for three measured ASICs. The calibrated reference charge values will be used for the calculation of the current when performing measurements with the ASICs.

Additionally, the stability of the reference charge as a function of temperature was verified. The system was put inside a climatic chamber where the temperature was controlled and the voltages $V_{charge+}$ and $V_{charge-}$ were monitored using two multimeters. The measured reference voltages did not deviate with temperature.

5.4 Leakage Current Measurements

The leakage currents at the inputs of the ASIC are strongly affected by temperature. This is why the leakage current measurements were initially performed inside a climatic chamber, where the temperature and humidity were controlled.

5.4.1 Leakage current versus *VDDA1* and V_{guard}

The leakage current into the input of the Utopia 2 ASIC can be externally adjusted using the *VDDA1* voltage. *VDDA1* is the highest potential voltage to which the cathode of the upper ESD protection input diode is connected (figure 4.35).

In figure 5.9 the leakage current of channel 1 and the leakage current of channel 2 are plotted as a function of *VDDA1*. The temperature was kept constant at 20°C and the humidity was 20%. The V_{cm} voltage was 1.5 V. In this plot it can be seen that the leakage current of channel 1 is smaller than the leakage current of channel 2 and that the net leakage increases when the voltage drop across the upper diode decreases. In that case, the leakage had a negative value and depended mostly on the contribution of the bottom ESD protection diode. When the *VDDA1* increased above 2.6 V the leakage current changed polarity and became positive.

According to this plot, the selected *VDDA1* value affects the polarity and the net leakage current. This is similar to the Utopia's 1 CH2 design, where the upper ESD protection diode was removed and the channel demonstrated only negative leakage current. For Utopia 2, channel 1 was designed to accept negative input current compared to channel 2 that was designed bipolar. The positive leakage current forces the analog output of channel 1 to saturate. This is identified in figure 5.9 when *VDDA1* increases above 2.6 V. On the other hand, the bipolar channel 2 can measure the positive current.

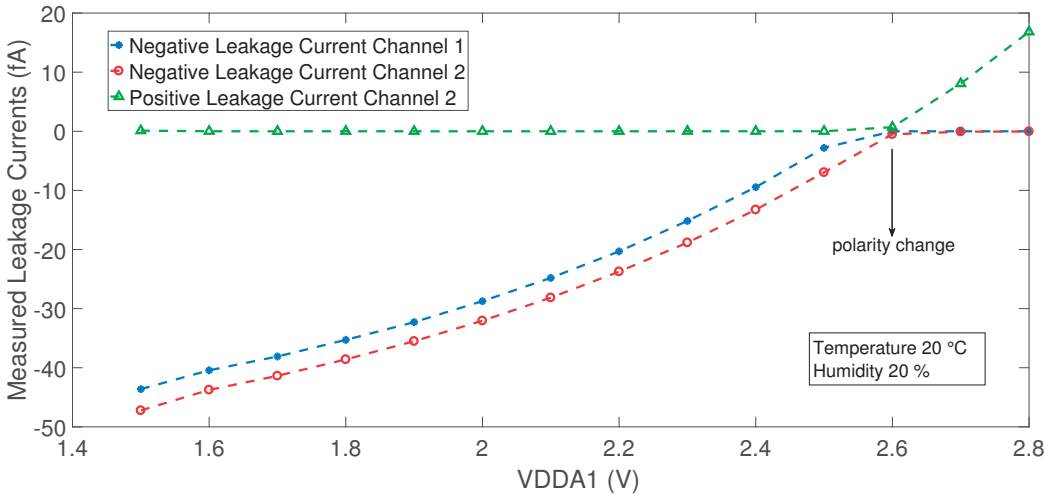

Figure 5.9 – Measured leakage currents versus *VDDA1* at 20°C and 20% humidity

At PCB level, guards surround the input traces. The leakage current versus V_{guard} measurement was performed, when the *VDDA1* was at 2.5 V potential and the temperature and the humidity remained at 20°C and 20% respectively. Figure 5.10 shows the leakage current of channel 1 and channel 2 as a function of V_{guard}.

When the temperature is constant, the factors that affect the input leakage current that is

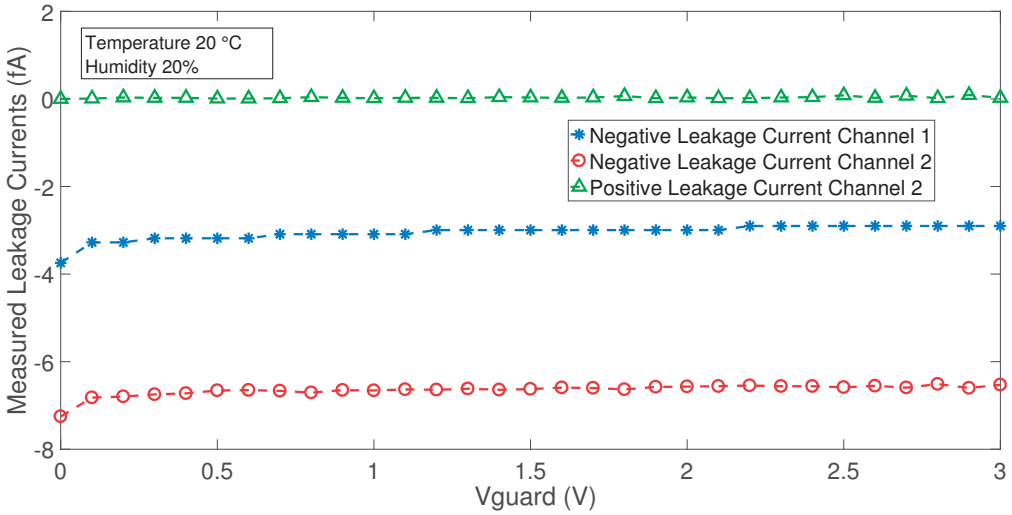

Figure 5.10 – Measured leakage currents versus V_{guard} at 20°C and 20% humidity

dominated by the ESD protection diodes, are primarily the *VDDA1* voltage and secondly the V_{guard} voltage of the guards that surround the input traces. For the next measurements, these two parameters were set to *VDDA1* = 1.6 V and V_{guard}= V_{cm} = 1.5 V in order to observe the effect of temperature on the leakage currents.

When *VDDA1* = 1.6 V, the leakage current had negative polarity. For the next plots and to be consistent with the measurements presented in chapter 3, the negative measured and injected current will be presented as an absolute value without its negative sign.

5.4.2 Leakage current versus temperature

The leakage currents in both channels as a function of temperature have to be monitored. The principle of operation of the active leakage current compensation is based on the diode leakage current dependence on temperature. Any possible mismatch in the ESD protection diodes is translated in leakage current mismatch. This is why the ratio ρ of the leakage current between channel 1 and channel 2 has to be measured and characterized in order to be used for the compensation. In the following leakage current measurements, the active leakage current compensation in channel 1 is disabled.

The temperature of the climatic chamber was programmed and the humidity was kept constant at 0 %. Specifically, for the measurements presented in figure 5.11, the temperature inside the chamber decreased from 50°C to 0°C in steps of 5°C. The leakage current of channel 1 and the leakage current of channel 2 are plotted over time. The temperature measured by the on-board sensor is shown in the right y-axis of the plot. It can be seen that the leakage current is strongly affected by temperature and follows the temperature decrease step pattern. Similarly to the previous measurements shown in figures 5.9 and 5.10, the leakage current of

channel 2 is higher than the leakage current of channel 1.

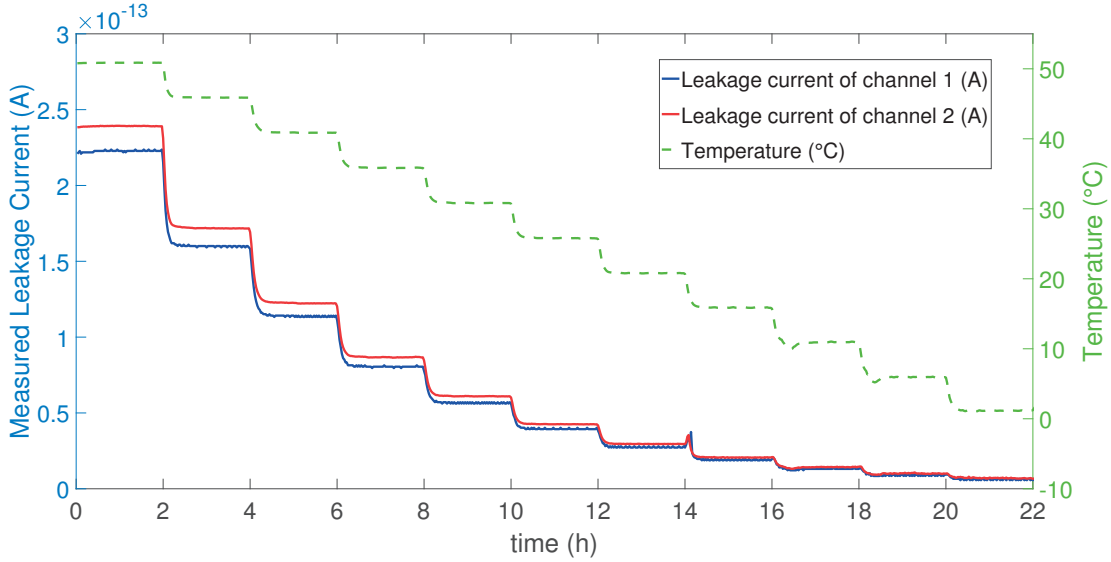

Figure 5.11 – Measured leakage currents and temperature over time when *VDDA1*= 1.6 V

An exponential fit is used as shown in figure 5.12 for the leakage current of the measuring channel 1 that is plotted versus temperature. It is calculated that the leakage current increases by a factor of 2.02± 0.03 for every 10°C increase in temperature. This is expected and also verifies that the leakage current is dominated by the ESD protection diodes leakage.

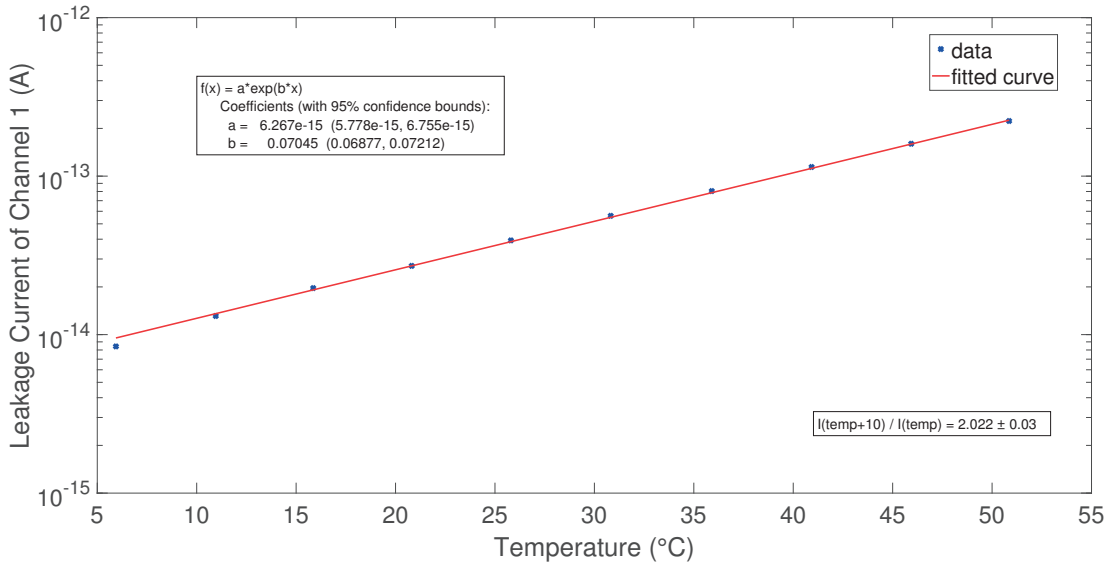

Figure 5.12 – Measured leakage current in channel 1 as a function of temperature

5.4.3 Ratio ρ of leakage currents of channel 1 and 2 for different temperatures

The ratio of the leakage currents between channel 1 and channel 2 versus temperature is shown in figure 5.13 for various temperatures. The ratio is almost constant with a mean value of 0.92 and this value will determine the number of Q_{ref2} injections from channel 2 to channel 1. The error in the lower temperature is bigger due to lower statistics at lower leakage for the same acquisition time.

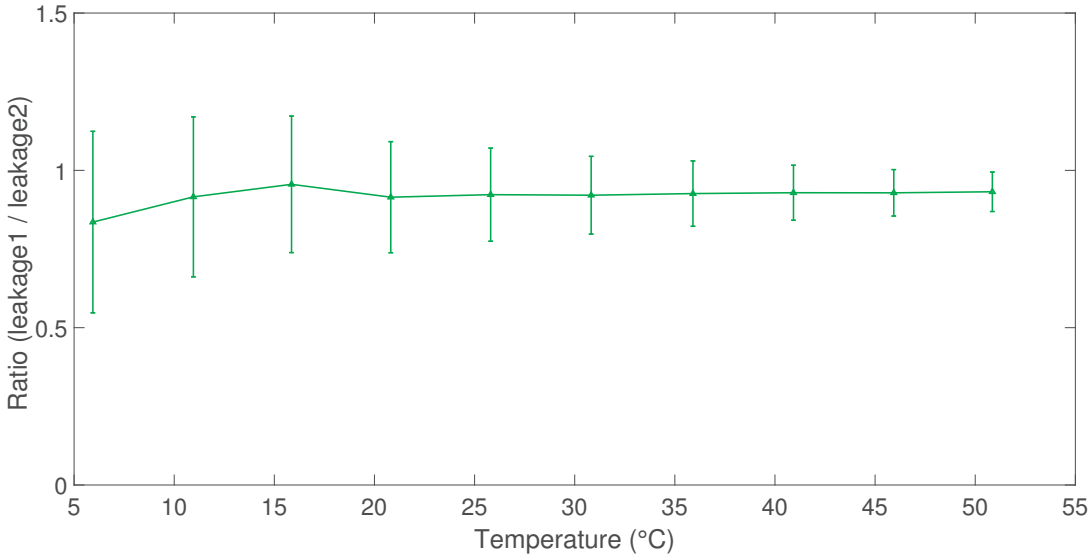

Figure 5.13 – Ratio of the leakage currents between channel 1 and channel 2

The calibration of the ratio ρ is needed to avoid any under-compensation or over-compensation during the on-chip active leakage current compensation. The chip is also equipped with error outputs that can detect any possible errors due to over-compensation or under-compensation.

5.5 Measurements with a Standard Laboratory Current Source

Two laboratory current sources from Keithley, the Keithley 6430 [85] and the Keithley 263 [86], were used to evaluate the dynamic range and the linearity of the Utopia 2 ASIC. Python routines were written to automate the data acquisition. The current sources were controlled using a General Purpose Interface Bus (GPIB) connection to inject in a logarithmically increasing step input currents starting from 20 fA and increasing up to 6 μA in various steps.

The next plots show in logarithmic scales the measured current from the ASIC versus the injected current from the source. Although negative current was injected, the absolute value of the currents is plotted. The error is expressed as a percentage showing the discrepancy between the measured value and the injected current.

The measurements were performed inside a climatic chamber where the temperature was kept constant at 25°C and 50°C respectively, and the humidity was 0 %.

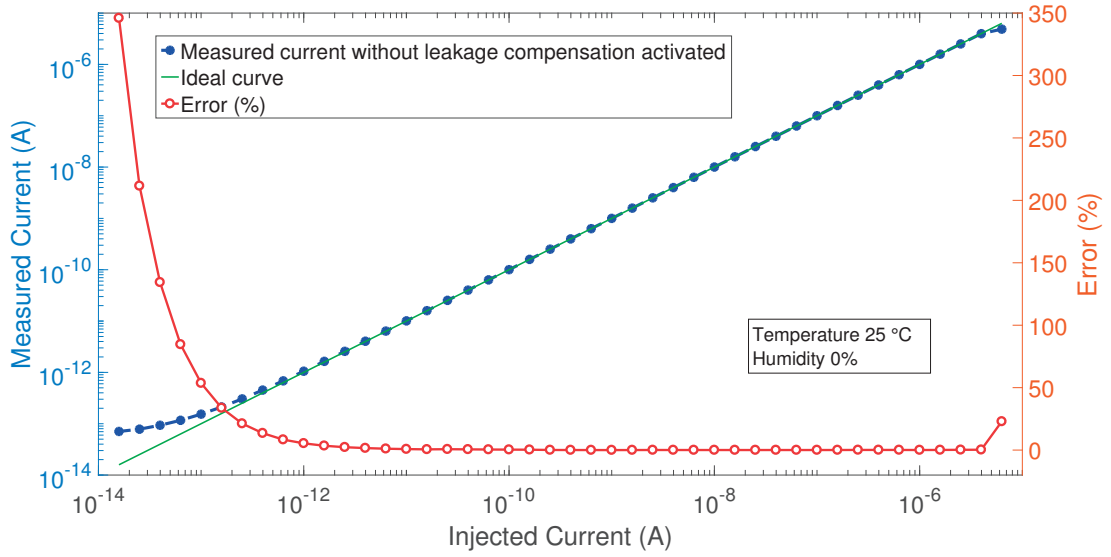

Figure 5.14 – Dynamic range sweep from 20 fA to 6 μA at 25°C without the leakage compensation

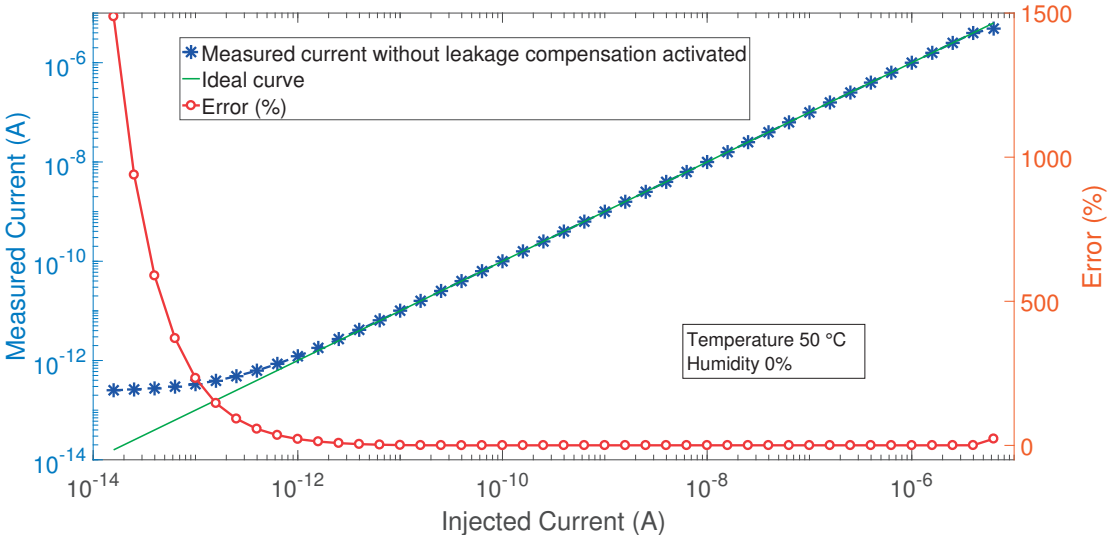

Figure 5.15 – Dynamic range sweep from 20 fA to 6 μA at 50°C without the leakage compensation

In the measurements presented in figures 5.14 and 5.15, the leakage current present in channel 1 input was not compensated. This is the reason why the error in the low range, when currents below 100 fA were injected, is above 350 %. The leakage current increase with temperature increase was studied before and this is why at 50°C the discrepancy between the measured and the injected current is more than 1000 %.

The contribution of the leakage current compensating topology is shown in figures 5.16 and 5.17, where the same measurements were repeated and the leakage current was compensated

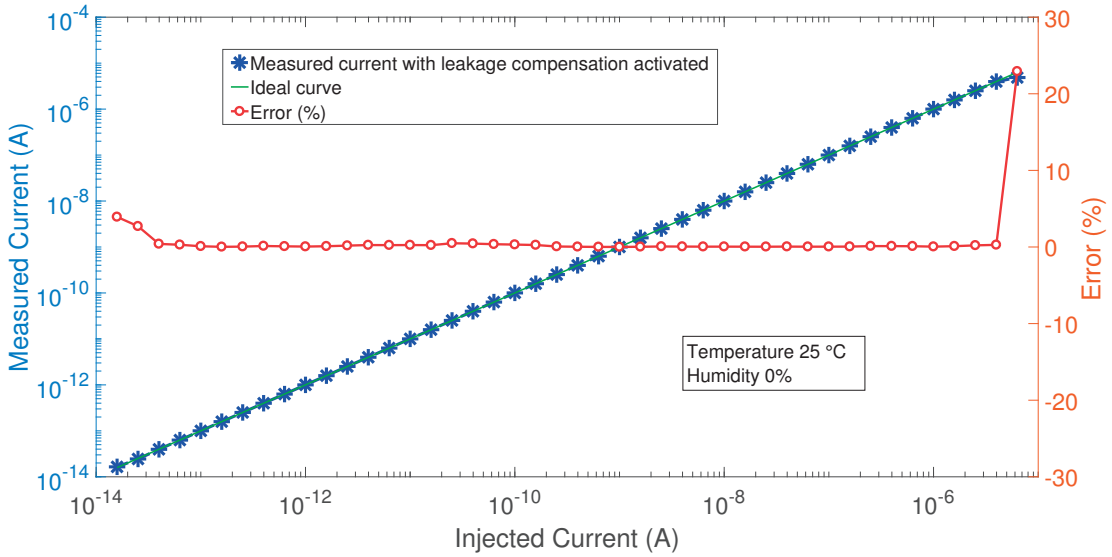

Figure 5.16 – Dynamic range sweep from 20 fA to 6 μA at 25°C with the leakage compensation enabled

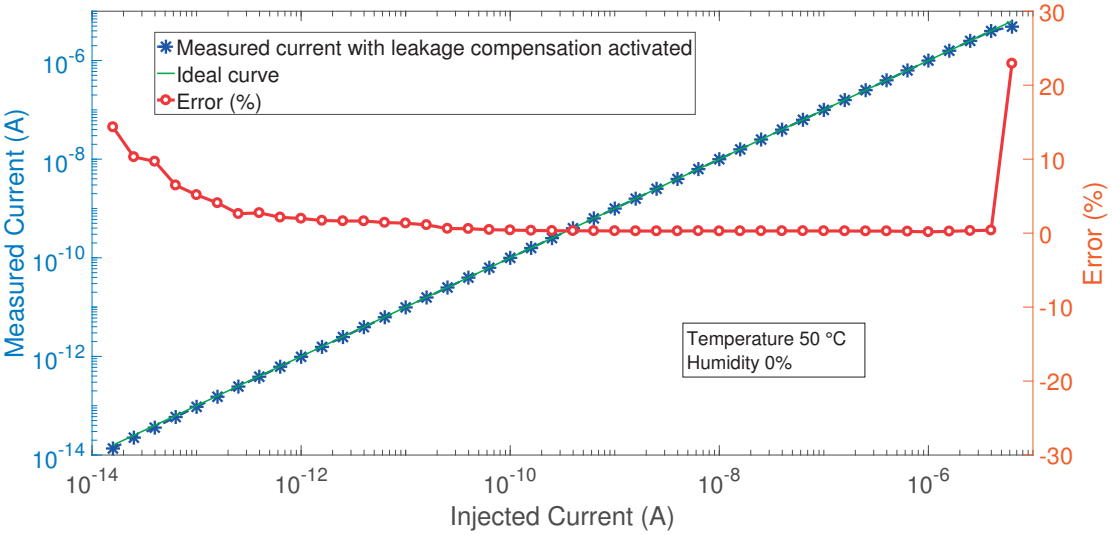

Figure 5.17 – Dynamic range sweep from 20 fA to 6 μA at 50°C with the leakage compensation enabled

on-chip using the "dummy" channel 2.

For these plots the discrepancy in the low range is mainly related to the leakage of the Keithley 263 current source that is not constant and cannot be subtracted as an offset. On the upper end, the error is due to the selected t_{cycle} of the *"discharge"* signal. Between 300 fA and 3 μA the error is below 0.5 % and the ASIC demonstrates excellent linearity.

5.6 Measurements with a Calibrated Current Source at METAS

The need to calibrate electrometers at the femtoampere level led to the design of accurate sub-picoampere current sources. These sources are based on a linear voltage ramp generator connected to one terminal of a known reference capacitor. The other terminal is connected to the input of the front-end readout system [102], [103].

The Swiss Federal Institute of Metrology (METAS) owns a system based on the differentiation of linear voltage into a dc current. This system can accurately inject femtoampere currents for the calibration of electrometers [104]. The testbench that is available at METAS is shown in figure 5.18. The accurate current source is able to inject negative and positive current for some minutes according to the selected reference capacitor.

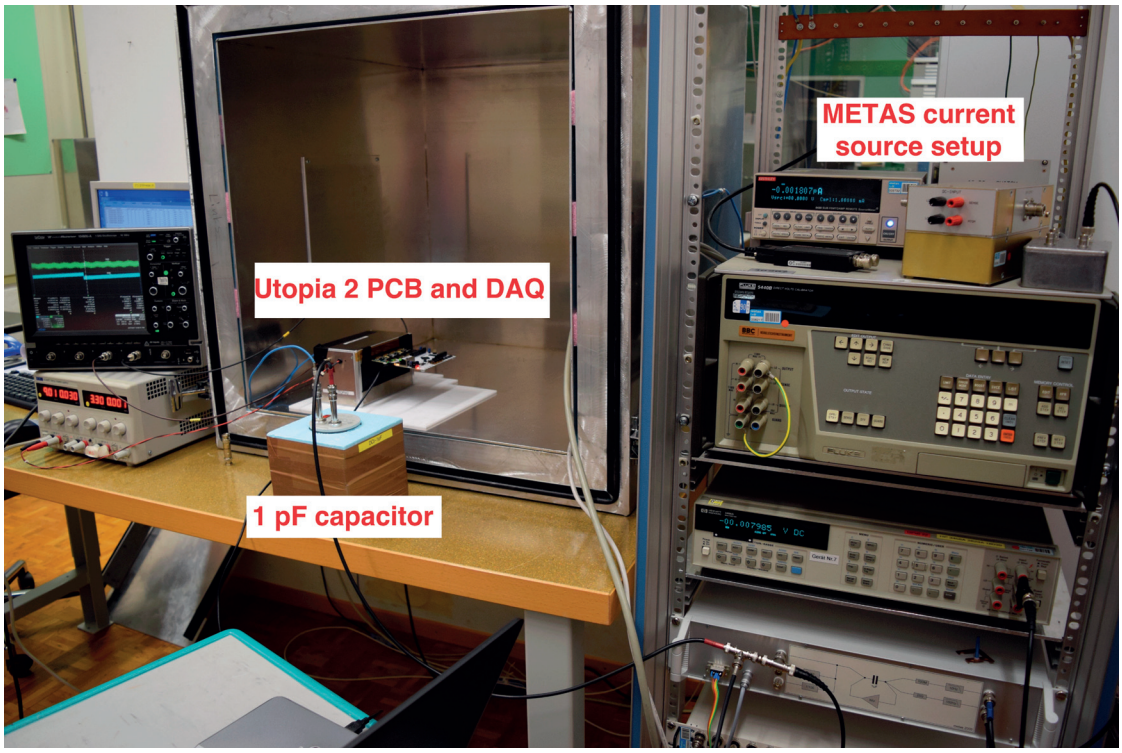

Figure 5.18 – Testbench at METAS

The Utopia 2 ASIC measured femtoampere currents injected by the METAS current source. The presented measurements were taken with the same chip in two different measurement campaigns with one month difference. The calibrated leakage current mean values measured at an ambient temperature of 23°C with 46 % humidity are shown in Table 5.3. This table also shows the injected currents using the accurate METAS current source.

The leakage current compensation in the presented measurements was performed with post processing of the acquired data. Because of the negative polarity constant leakage current in channels 1 and 2, the ASIC was able to measure even positive currents up to +30 fA, that were

Table 5.3 – Measurements at METAS

	First set of measurements	Second set of measurements
Leakage channel 1	-44.94 fA	-39.19 fA
Leakage channel 2	-47.86 fA	-41.70 fA
Ratio ρ	0.938	0.939
Injected currents	±5 fA to ±30 fA	±1 fA to ±128 fA

below that leakage current. For these ultra-low current measurements, the measurement time window T_w was increased to 100 s. Figures 5.19 and 5.20 present the injected current versus the measured current in fA. They also present the discrepancy from the injected value that is calculated as:

$$\frac{MeasuredValue - InjectedValue}{InjectedValue} \cdot 100\% \tag{5.9}$$

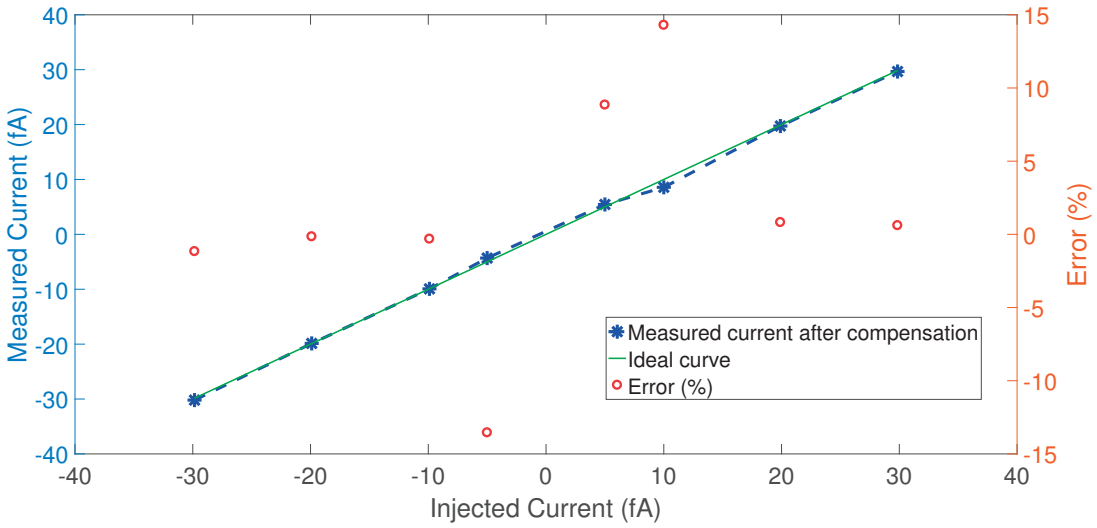

Figure 5.19 – Injected current from ±5 fA up to ±30 fA versus measured current after leakage current compensation

The plot in figure 5.20 demonstrates that the Utopia 2 ASIC is able to measure 1 fA and 2 fA if enough measurement time is allocated for the measurements. For the sake of clarity, the same plot is shown again in figure 5.21 focused on the ultra-low current range.

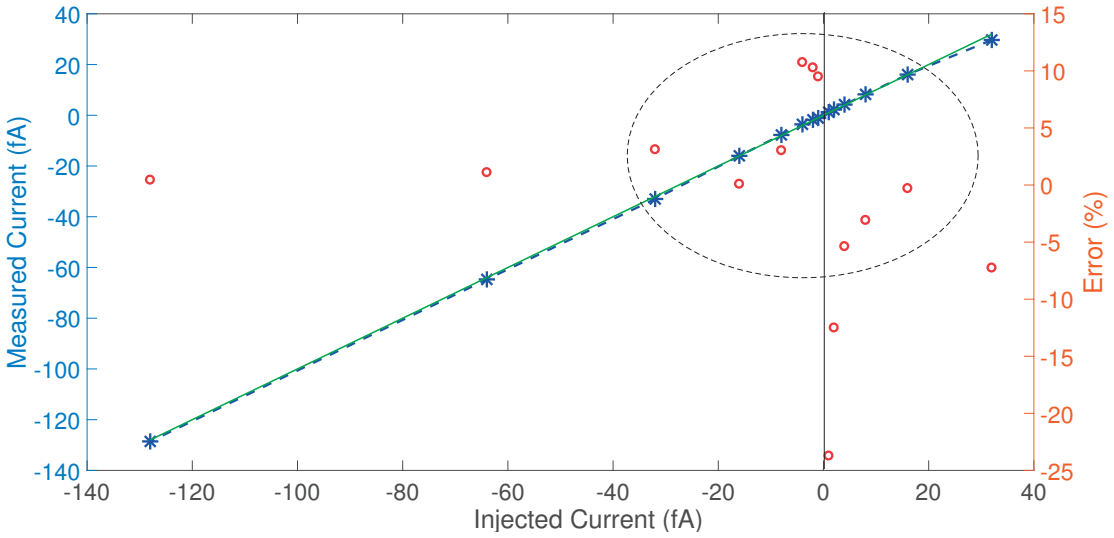

Figure 5.20 – Injected current from ±1 fA up to ±128 fA versus measured current after leakage current compensation

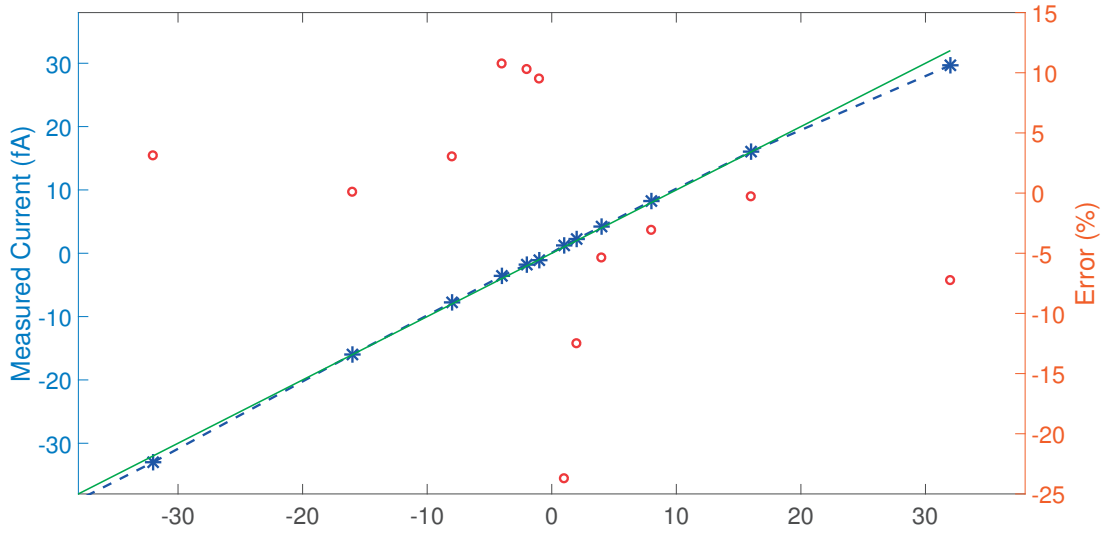

Figure 5.21 – Injected current from -30 fA up to +30 fA versus measured current after leakage current compensation

5.7 Dynamic Range of Utopia 2 ASIC

After the combination of the measurements performed at METAS and in the laboratory using standard current sources, it is demonstrated that the Utopia 2 ASIC is able to measure over a wide dynamic range of 9 decades. For the femtoampere measurements the time window has to be increased.

The dynamic range DR is given by:

$$DR = \frac{I_{max}}{I_{min}} = \frac{5\mu A}{1fA} = 5 \cdot 10^9 \tag{5.10}$$

5.8 Measurements with the Ionization Chamber

The Utopia 2 ASIC was eventually tested with the detector. A hydrogen ionization chamber of type IG5-H20 [16] was connected to the front-end, as shown in figure 5.22. The detector was biased using V_{bias}= -1 kV voltage provided by a Keithley laboratory voltage source.

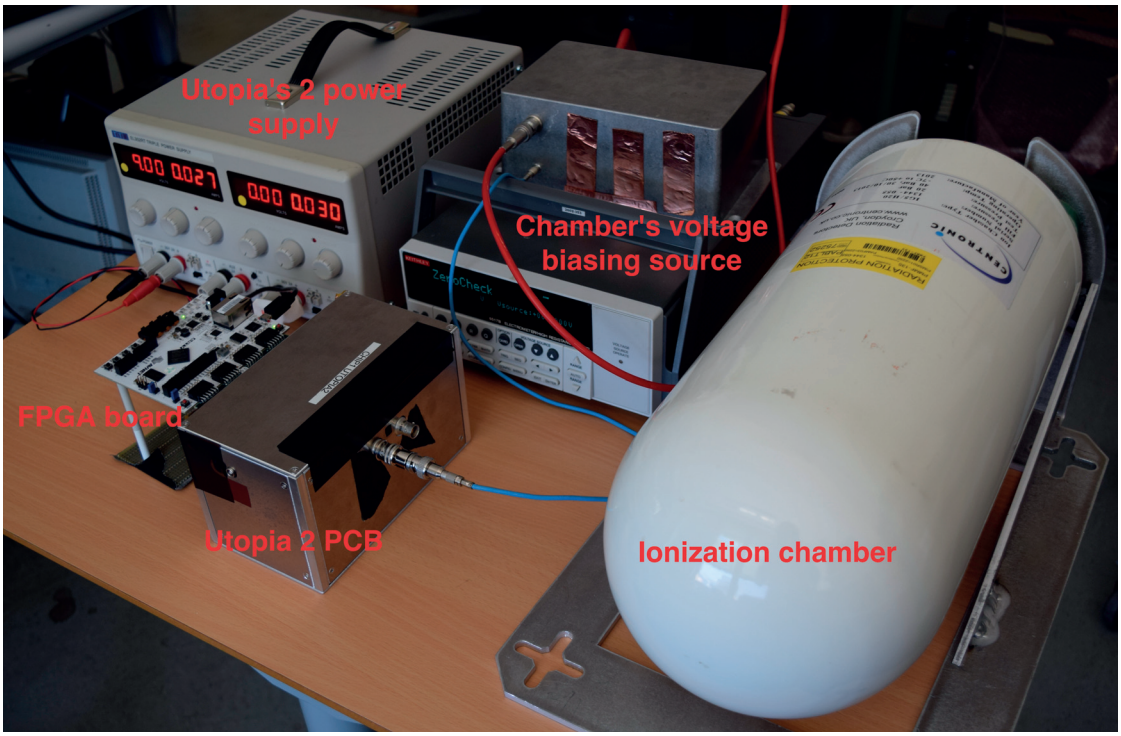

Figure 5.22 – Laboratory setup for the detector measurements

The detector's output current corresponding to the natural radiation background at the location of the test is shown in figure 5.23. In this plot, the measured current in channel 1 and the leakage current of channel 2 are plotted as a function of time. The on-board temperature and humidity sensor was also monitoring the temperature and humidity variations as shown in the right y-axis. The measured currents were following the day cycle and this is why when the temperature increases both currents increase.

However, due to the active leakage current compensation, the ionization chamber's current output due to the background radiation can be measured, as shown in figure 5.24.

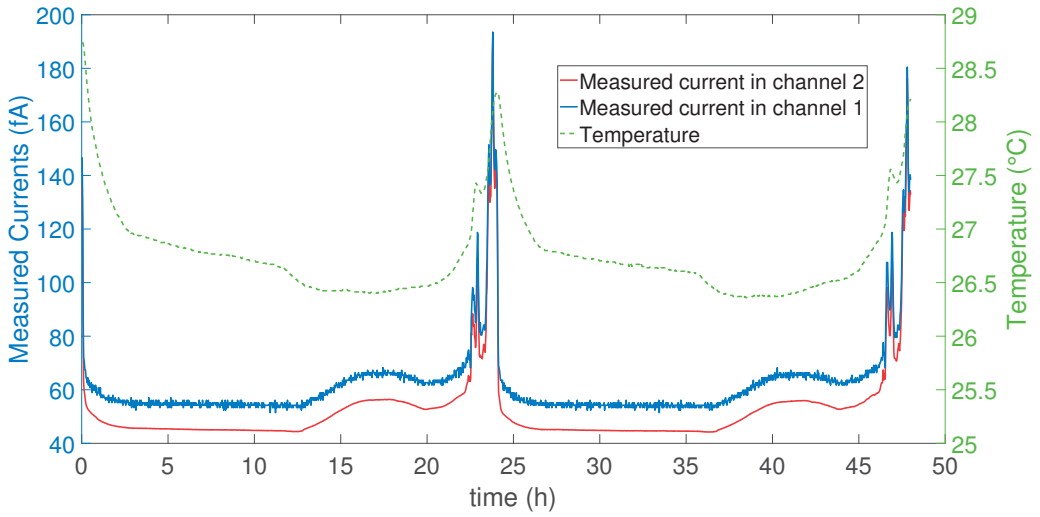

Figure 5.23 – Detector's output current for background radiation measurement and measured leakage current

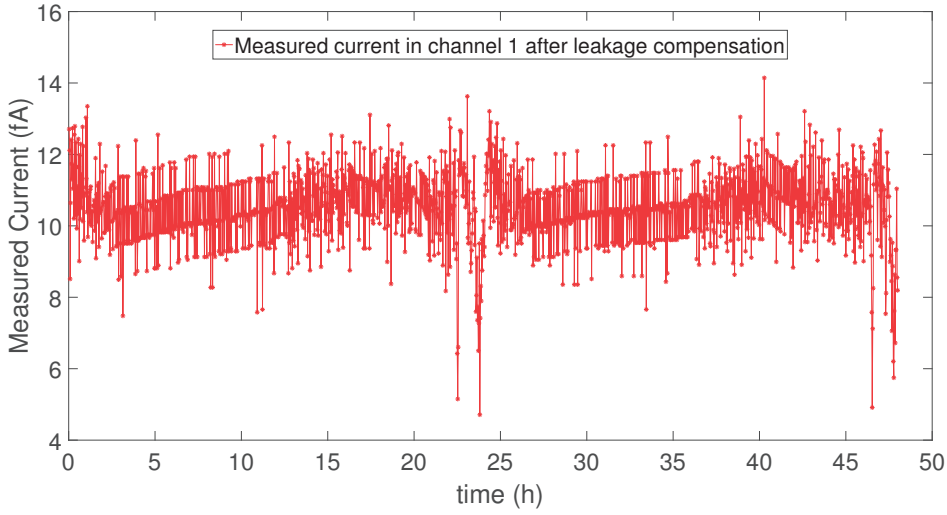

Figure 5.24 – Detector's compensated output current for background radiation measurement

A qualitative demonstration that the designed circuit functions correctly in the presence of radiation sources is shown in figure 5.25. Two radiation sources, one ^{60}Co and one ^{137}Cs, were used and placed close to the detector for a few minutes. They generated currents of I_{det}= 850 fA and I_{det}= 3.8 pA.

However, the sources that were used were not recently calibrated, so the expected output current cannot be precisely calculated. This will be possible with measurements in the CERN calibration laboratory which is a specific facility for calibration of radiation instruments, where sources and testbenches can be remotely controlled [105], [106].

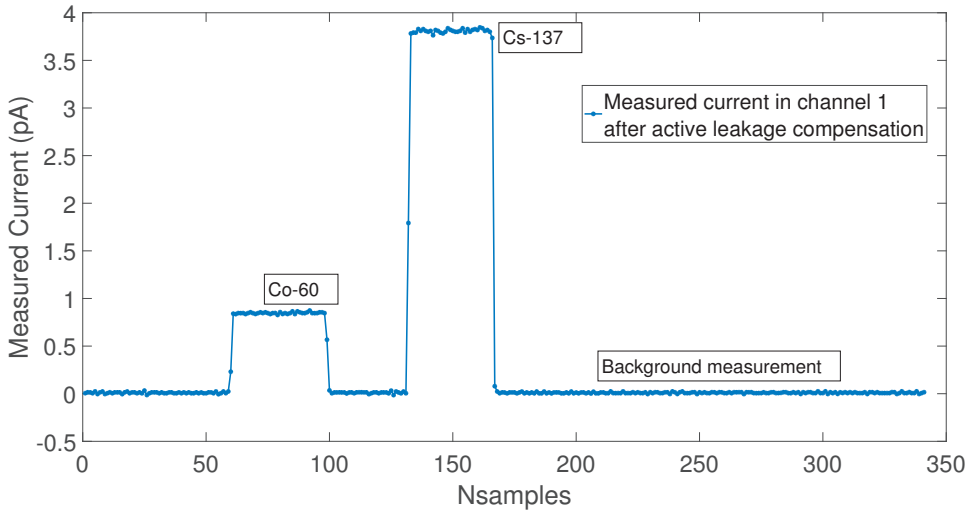

Figure 5.25 – Detector's output current I_{det} for two different radiation sources, ^{60}Co and ^{137}Cs

5.9 Additional Calibration

Utopia 2 ASIC was fully characterized and tested for its electrical behavior in the Swiss Federal Metrology Institute. The detector and the front-end electronics have to be calibrated in the CERN calibration facilities to evaluate the response of the detector to well-known and characterized radiation fields. This is the last step that has to be performed before deployment.

For the normal functionality of the front-end, the chip's reference capacitors C_{ref} are not supposed to drift more than 10 %. While the system is in normal operation and connected to an ionization chamber, an external calibration of the reference voltages, can be performed to guarantee that the reference charge values are correct.

According to the flicker noise simulations presented in chapter 4, there is no need for frequent calibration of the front-end electronics. However the front-end can be calibrated during the scheduled long shutdowns of the CERN accelerator chain.

5.10 Chapter Conclusions

The calibration procedure and the measurements of the Utopia 2 ASIC were presented. The reference charges of the switched capacitor circuits of each chip have to be initially calibrated. The leakage currents of both channels were measured at different temperatures. The leakage current in the input of each channel is dominated by the ESD protection diodes. This is why the leakage can be adjusted according to the selected ESD power supply *VDDA1* voltage. For a constant *VDDA1*, the two channel active leakage current compensation scheme can provide a leakage current-free input in the measuring channel 1.

Multiple measurements were performed using precise laboratory current sources. In order to characterize the ultra-low current behavior of the chip, femtoampere measurements were also performed at the Swiss Federal Institute of Metrology (METAS). The Utopia 2 ASIC successfully measured a calibrated current of 1 fA. The ASIC demonstrates a very wide dynamic range that exceeds 9 decades.

The front-end was also connected to an ionization chamber. Extra calibration with the detector in well known radiation fields is foreseen for the full characterization of the whole measurement system.

At this point, it is useful to show again the updated comparison Table 5.4 where the Utopia 2 ASIC has been added. The present work is shown against the state of the art. The Utopia 2 ASIC can measure 1 fA due to the active leakage current compensation. In Utopia 1, only post processing for the leakage current subtraction was possible. The current ASIC was optimized for radiation protection and environmental monitoring purposes and not for beam loss monitoring. This is the reason why the specifications required measurements up to 5 μA. The other presented ASICs are supposed to measure higher current. Compared to the other ASICs, the Utopia 2 ASIC and the fourth channel of Utopia 1 (CH4) are the only asynchronous.

Table 5.4 – Updated Comparison among ASICs for Radiation Monitoring including Utopia 2 ASIC

Characteristics	**TERA06 [33], [34]**	**TERA09 [39], [40]**	**QFW I ASIC [45]**	**BLM ASIC [41]**	**UTOPIA 1**	**UTOPIA 2**
Publication Year	2004	2016	2004	2012	2015	2016
Technology	AMS 0.8 μm	AMS 0.35 μm	AMS 0.35 μm	IBM 0.25 μm	AMS 0.35 μm	AMS 0.35 μm
Die Size	6mm x 7mm	4.68mm x 5.8mm	3.28mm x 3.38mm	2.4mm x 3.775mm	2.6mm x 2.6mm	2.75mm x 2.75mm
Dynamic Range	5 decades	6 decades	1.60 pA to 180 μA	1 pA to 1.05 mA	-12 fA to -5 μA	-1 fA to -5 μA
Leakage Current	194 fA	2 pA	1.65 pA	-188 fA	-12 fA to -80 fA	<-1 fA
Linearity Error	± 1%	±2%	± 1.5%	± 5%	± 2.5%	± 1%
Polarity	Unipolar	Bipolar	Unipolar	Bipolar	Unipolar	Unipolar
Clock Frequency	20 MHz	250 MHz	10 MHz	12.8 MHz	10 MHz	Asynchronous

6 Conclusions

6.1 Summary

This work focuses on the design of a new front-end readout ASIC for radiation monitoring. When background radiation is measured, the output of the ionization chamber detector is of the order of femtoamperes (fA). However, in the presence of higher levels of ionizing radiation, the output current may reach a few microamperes (μA).

The architecture of an asynchronous current to frequency converter is fully exploited in this application, since for lower radiation and equivalently for lower measured current the measurement time can be increased. The addition of a second reference charge injection circuit gives the possibility to extend the upper measurement range up to the microamperes, by keeping a constant acquisition time. The operating principle is based on continuous integration and charge balancing.

The AMS 0.35 μm process was used due to its low leakage current behavior. A first demonstrator ASIC named Utopia 1, gave us the possibility to investigate the effect of the various leakage current sources present at the input of the front-end. Circuit techniques like source shifting, were used to eliminate the contribution of the subthreshold leakage of the switches. The contribution of the external leakage current sources, like the printed circuit board leakage or the leakage of the adjacent pins, were minimized by careful system level design.

The dominant leakage current in the input of the current to frequency converter is the leakage related to the ESD protection diodes. To compensate that leakage current, a second "dummy" compensating channel whose input structures were matched to the first measuring channel was introduced in the second ASIC named Utopia 2. The leakage current of the ESD diodes is susceptible to temperature variations. The compensating channel is physically connected to the input of the first measuring channel and can subtract the leakage current that it is measuring, from the first channel's input. Thus, by active leakage current compensation, channel 1 can measure the current that is related only to the radiation detector's output. The two channel compensation approach adopted in this design, guarantees the leakage current

minimization, provided an initial calibration has been performed. The conversion depends on the switched capacitors' reference charges. While the system remains fully functional and connected to the detector, only calibration of the external voltage references is required.

The Utopia 2 ASIC is able to measure input currents over a wide dynamic range of 9 decades. If sufficient time is allocated for the measurements, input currents as low as 1 fA can be measured. Such a low current was measured in the Swiss Federal Institute of Metrology (METAS) where an ultra-low accurate current source was available. Additionally, the ASIC successfully measures currents up to 5 μA due to its second range charge injection circuit that is activated in parallel to the first when high current is integrated in the input. The front-end was also tested with the ionization chamber detector and was able to measure current generated by radiation sources.

The main objectives for the ultra-low leakage wide dynamic measurement front-end were reached. The presented ASIC achieves the digitization of currents as low as 1 fA that are far lower than the existing state of the art for readout systems for radiation monitoring (Table 5.4). Compared to the other ASICs the Utopia 2 ASIC is able to measure even the background radioactivity. The designed system fulfills the specifications that are required for the new state of the art radiation monitoring system for environmental and personnel safety at CERN. The current thesis summarizes the design and the testing of the front-end that will be installed and used at CERN.

6.2 Thesis Contributions and Future Perspectives

The designed ASIC that can measure currents over a wide dynamic range of nine decades starting from the fA range without any charge loss or insensitivity during reset time, was motivated by the strict legislation in matters or radiation protection and environmental radiation monitoring. The existing commercial system used at CERN that consists of COTS components do not meet all the requirements in terms of dynamic range and reset time. The leakage currents in the low range and the bandwidth limitations limit the dynamic range of the existing system.

The guidelines set for the design of an ultra-low leakage current converter can be used in any system that targets femtoampere current measurements. The design techniques that mitigated the effect of the leakage currents and the measurement principles that allowed the testing of the front-end were presented in this manuscript.

Apart from environmental radiation and radiation protection measurements and in general beam monitoring, there are various other applications that require ultra-low current sensing. Some of these applications are related to sensor and device characterization, biochemical and biomedical measurements and photomultiplier measurements. Some wearable biosensing applications require low power consumption but not so wide dynamic range since their output is normally in the pA or nA range. The power consumption of Utopia 2 ASIC was determined by the high GBW that was required in order to be able to measure up to 5 μA. However the

architecture of Utopia 2 ASIC can be used in low consumption applications when a low current needs to be measured. The power consumption has to be optimized for a lower GBW.

The presented system can be used in these current sensing applications in case their requirements are compatible with the intrinsic properties of the current to frequency conversion. In other words, for the ultra-low current measurements, sufficient measuring time has to be allocated for the integration. For the CFC topology, when the measuring time window T_w increases, lower current can be integrated.

For shorter T_w and faster measurements, the reference charge Q_{ref} that is used for the charge balancing has to be reduced to the limit where the parasitic effects become dominant and the components cannot be scaled lower. The Q_{ref} for the switched capacitor circuit is equal to $Q_{ref} = C_{ref}V_{ref}$. This means that either the reference capacitor C_{ref}, or the reference voltage V_{ref}, or both have to be scaled. Figure 6.1 shows the effect of the scaling of the C_{ref} on the measurement time represented by the T_w in the sub-picoampere range. For this plot, the V_{ref} was constant and equal to V_{ref}= 1 V. However, the C_{ref} cannot be scaled below the minimum process capacitor. The parasitic capacitances have to be also taken into account. Scaling of the reference voltage V_{ref} is also limited by the offset voltages. In addition the scaling of the V_{ref} is affecting the SNR. Figure 6.2 shows the SNR for different V_{ref} values when C_{ref}= 100 fF. As discussed in the noise evaluation chapter 4.8.8, in general, averaging improves the SNR until the signal reaches the $1/f$ noise floor. The non-ideal effects have to be considered during scaling of the Q_{ref}.

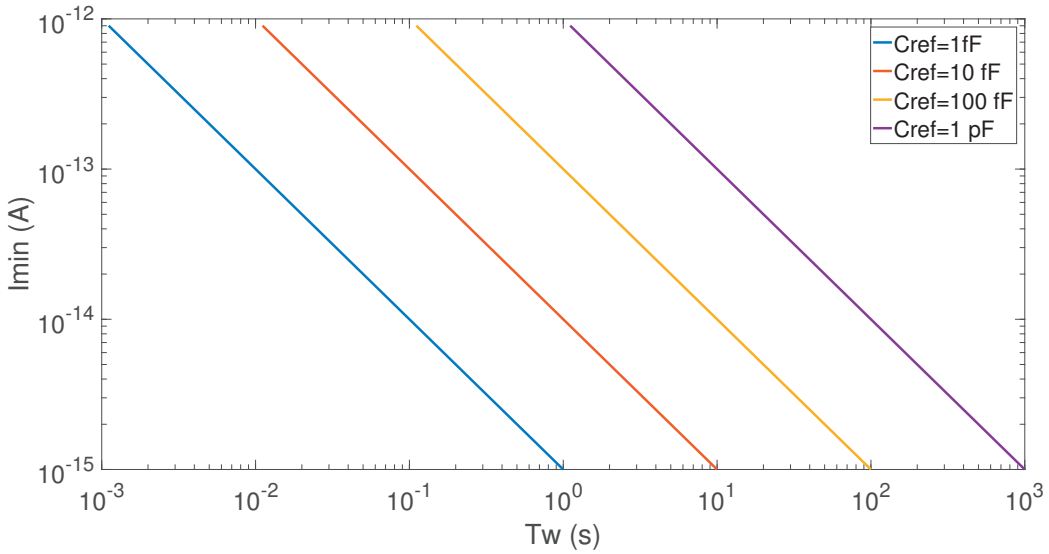

Figure 6.1 – Sub-picoampere currents I_{min} versus T_w for different C_{ref} values

The dominant source of leakage current in AMS 0.35 μm technology that was used for this design is the ESD protection diode structures. The active leakage current compensation was used as a solution to subtract on-chip the net leakage current due to the ESD diodes that

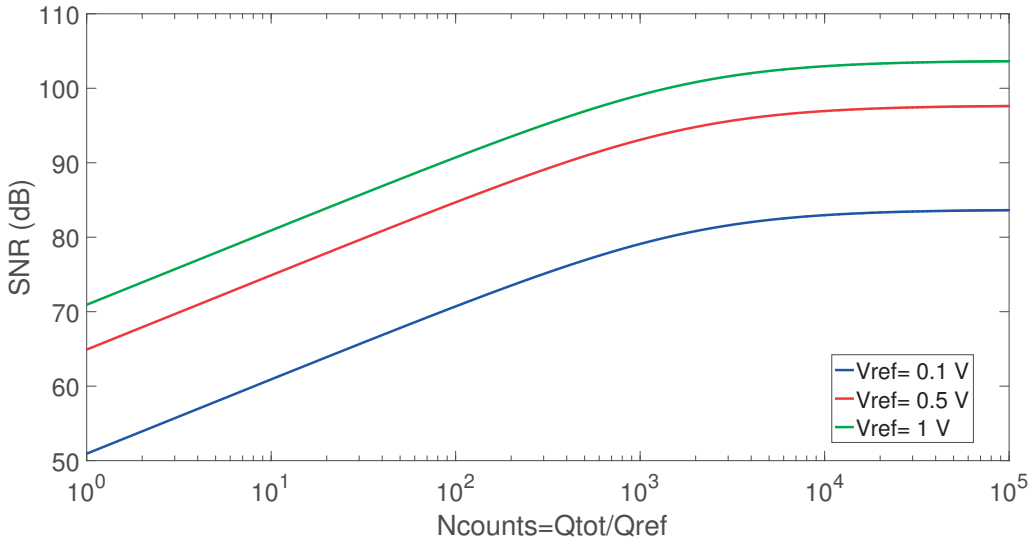

Figure 6.2 – SNR versus N_{counts} for different voltage reference V_{ref} values

varies with temperature. The standard ESD protection pads were provided by the foundry and were not optimized for low leakage current. A new alternative low leakage ESD protection pad could provide a lower net leakage current input to the integrator.

The AMS 0.35 μm technology was selected for its low leakage current behavior. In case of a more recent process than the AMS 0.35 μm, short channel effects will arise and the sum of the leakage currents will be increased considerably. The key for the femtoampere current measurements is the active leakage current compensation and the matching of the ESD protection structures and input switches. The circuit and the measurement techniques that were explained in this thesis that mitigate the effects of the leakage currents can be used. A new demonstrator with multiple channels that allow the characterization of each leakage current source like the Utopia 1 ASIC, can reveal the limitations of the finer technology.

Finally the Utopia 2 ASIC is not rad-hard by design since it is meant to measure the low level background radiation. For applications with high radiation fields (like in the close vicinity of accelerators), technologies like 0.13 μm could provide radiation hardness and the same architecture of CFC through charge balancing could be used for measuring higher detector currents. In that case the dynamic range has to be shifted and measure from pA up to hundreds of mA.

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Abbreviations and Acronyms

AGM Area Gamma Monitor

ALARA As Low As Reasonably Achievable

ALICE A Large Ion Collider Experiment

AMF Area Mixed Field

ASIC Application Specific Integrated Circuit

BLM Beam Loss Monitor

CERN European Organization for Nuclear Research

CFC Current to Frequency Converter

CMOS Complementary Metal Oxide Semiconductor

CMS Compact Muon Solenoid

COTS Commercial off-the-shelf

DAC Digital to Analog Converter

DAQ Data Acquisition

ESD Electrostatic Discharge

FPGA Field Programmable Gate Array

FR-4 Flame Retardant 4

GBW Gain Bandwidth Product

GIDL Gate-Induced Drain Leakage

GPIB General Purpose Interface Bus

HEP High Energy Physics

HSE Occupational Health & Safety and Environmental Protection

I2C Inter-Integrated Circuit

IAM Induced Activity Monitor

INFN Istituto Nazionale di Fisica Nucleare

LEIR Low Energy Ion Ring

LHC Large Hadron Collider

LHCb Large Hadron Collider beauty

LSB Least Significant Bit

METAS Swiss Federal Institute of Metrology

MOS Metal Oxide Semiconductor

MPW Multi Project Wafer

MWPC Multi-Wire Proportional Chambers

nMOS n-type Metal Oxide Semiconductor

NOC Non-Overlapping Clocks

Op-amp Operational Amplifier

OTA Operational Transconductance Amplifier

PCB Printed Circuit Board

pMOS p-type Metal Oxide Semiconductor

PS Proton Synchrotron

PSB Proton Synchrotron Booster

PSD Power Spectral Density

RAMSES RAdiation Monitoring System for the Environment and Safety

RMS Root Mean Square

RP Radiation Protection

SCADA Supervisory Control and Data Acquisition

SNR Signal to Noise Ratio

SPS Super Proton Synchrotron

UART Universal Asynchronous Receiver/Transmitter

USB Universal Serial Bus

Utopia 1 Ultra-low Picoammeter 1

Utopia 2 Ultra-low Picoammeter 2

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List of publications

- Voulgari E., Noy M., Anghinolfi F., Krummenacher F. and Kayal M., 2015, June. Design and measurement methodology for a sub-picoampere current digitiser. In Mixed Design of Integrated Circuits and Systems (MIXDES), 2015 22nd International Conference (pp. 525-529). IEEE., **Outstanding Paper Award**.

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- Voulgari E., Noy M., Anghinolfi F., Perrin D., Krummenacher F. and Kayal M. A 9-decade current to frequency converter with active leakage compensation.

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- Voulgari E., Noy M., Anghinolfi F., Perrin D., Krummenacher F. and Kayal M. Characterization of a 9-decade femtoampere ASIC front-end for radiation monitoring.

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