Negative Capacitance as Performance Booster for Tunnel FETs and MOSFETs: an experimental study

Ali Saeidi, Farzan Jazaeri, Francesco Bellando, Igor Stolichnov, Gia V. Luong, Qing-Tai Zhao, Siegfried Mantl, Christian C. Enz, and Adrian M. Ionescu

***Abstract*—This letter reports for the first time a full experimental study of performance boosting of Tunnel FETs (TFETs) and MOSFETs by Negative Capacitance (NC) effect. We discuss the importance of capacitance matching between a ferroelectric NC and a device capacitance to achieve hysteretic and non-hysteretic characteristics. PZT ferroelectric capacitors are connected to the gate of three terminals TFETs and MOSFETs and partial or full matching NC conditions for amplification and stability are obtained. First, we demonstrate characteristics of hysteretic and non-hysteretic NC-TFETs. The main performance boosting is obtained for the non-hysteretic NC-TFET, where the on-current is increased by a factor of 500x, transconductance is enhanced by three orders of magnitude, and the low slope region is extended. The boosting of performance is moderate in the hysteretic NC-TFET. Second, we investigate the impact of the same NC booster on MOSFETs. Subthreshold swing as steep as 4mV/dec with a 1.5V hysteresis is obtained on a commercial device fabricated in 28nm CMOS technology. Moreover, we demonstrate a non-hysteretic NC-MOSFET with a full matching of capacitances and a reduced subthreshold swing down to 20mV/dec.**

***Index Terms*—negative capacitance, ferroelectric, NC-TFET, NC-FET, hysteretic, non-hysteretic**

I. Introduction

THE negative capacitance (NC) effect in ferroelectric materials has been proposed to serve as a step-up transformer [1], amplifying the variation of the surface potential (ψ_s) in field effect transistors as a function of the gate voltage (V_g) change. This principle can be used for reducing the supply voltage of electronic switches and for alleviating the increase of the static power consumption in ultra-scaled CMOS devices [2]. The idea is to benefit of NC region of ferroelectric materials [3]. The practical implementation of the NC involves the series combination of a ferroelectric capacitor, operated in the NC region [4], with a positive capacitor capable of stabilizing the NC effect. A negative capacitor in the gate stack can make the total capacitance larger than its classical value, which leads to the decrease of the required ΔV_g to provide the same $\Delta\psi_s$. The challenges of ferroelectrics NC integration with conventional transistors are related to achieving simultaneously a matched design of the ferroelectric and in-series stabilizing MOS capacitors [5], [6]. In this context, a significant boosting can occur while the device behavior is still non-hysteretic [6]. This paper experimentally investigates the impact of the NC on DC electrical characteristics of Tunnel FETs (TFETs) and MOSFETs. This work demonstrates that the main beneficial effects of the NC on TFETs are the overdrive and transconductance amplification, which addresses exactly the most limiting performances of the current TFETs [2], [7]. Multiple improvements in *on*-current (I_{ON}), transconductance (g_m), and subthreshold swing (SS), by mean of NC, in a non-hysteretic NC-TFET is achieved. Moreover, a sub-thermal swing well below $60mV/dec$ is observed in both hysteretic and non-hysteretic NC-FETs.

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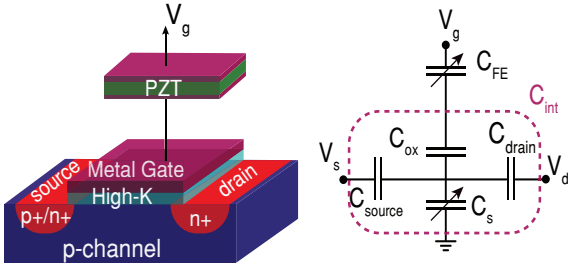

Fig. 1. Experimental configuration of the NC-TFET(p-i-n) /NC-FET(n-i-n) (left) and the capacitance model of the structure (right). C_{int} is the total capacitance of the reference device, including the effect of parasitic capacitors.

II. Capacitance Matching: Hysteretic and non-Hysteretic Operation Modes

A negative capacitance transistor has the unique properties that its gate stack is not passive and includes a mechanism of surface potential amplification [8]. Fig. 1 depicts the equivalent circuit of a MOSFET and of a TFET with a connected NC capacitor (C_{FE}) in-series with the gate stack. In both cases, one can define an internal amplification factor,

$$\beta = \partial V_{int}/\partial V_g = C_{FE}/\left(C_{FE}+C_{int}\right), \qquad (1)$$

where C_{FE} is the ferroelectric capacitance and C_{int} is the equivalent capacitance of the base transistor from the gate terminal, including all parasitic capacitances. In order to have a sufficient boosting of performance due to the NC effect, the absolute value of the ferroelectric negative capacitance ($|C_{FE}|$) and the intrinsic gate capacitance (C_{int}) need to be relatively close [5], [9]. In order to achieve a negative capacitance transistor in the non-hysteretic operation mode, the series combination of the ferroelectric negative capacitance and C_{int} should remain positive in the whole range of the operation [6]. A negative value of the total capacitance leads

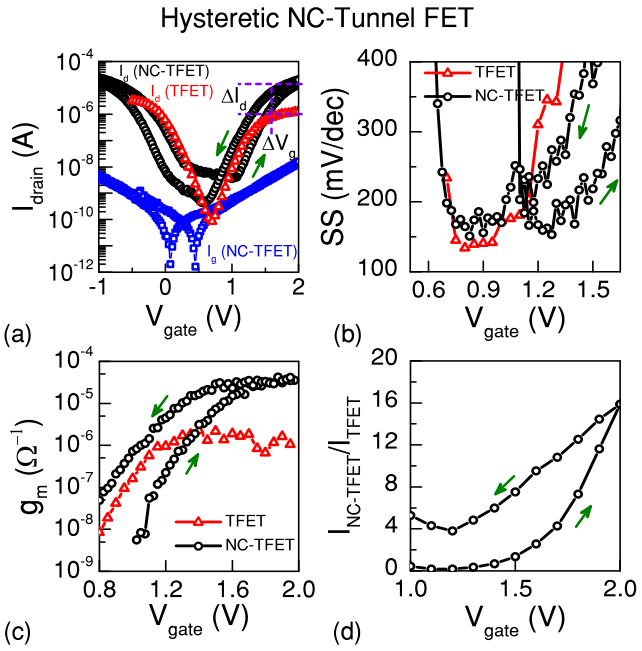

Fig. 2. (a) Transfer characteristic of an *n*-type hysteretic NC-TFET comparing the base device (nanowire array TFETs made of five silicon nanowires with a cross section of $30 \times 5nm^2$ and a gate length of $350\mu m$) where the intrinsic gate capacitance and the NC are matched only in a limited range of the gate voltage. While NC provides no improvement on the SS of the hysteretic TFET (b), the transconductance (c) and *on*-current (d) of the device is slightly boosted especially at high V_g. The drain voltage is $500mV$.

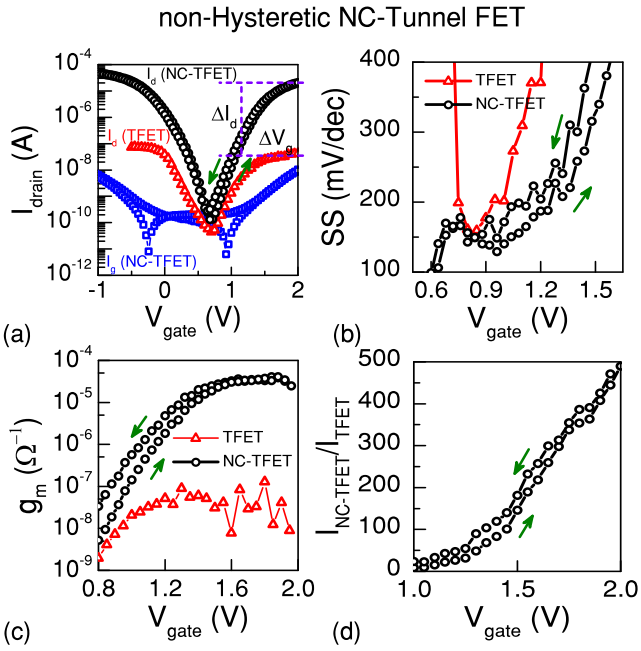

Fig. 3. (a) An outstanding performance boosting is simultaneously achieved together with an improvement of the swing, where the ferroelectric NC and the gate capacitance of the transistor (nanowire array TFETs made of five silicon nanowires with a cross section of $30 \times 5nm^2$ and a gate length of $350\mu m$) are matched in the whole range of the gate voltage. An extended low slope region (b), transconductance boosting up to 3 orders of magnitude (c), and up to 500x current improvement are obtained (V_{drain}=$500mV$).

to instability and hysteretic jumps in the polarization that results in a hysteretic transfer characteristic. Accordingly, the matching conditions of a negative capacitance transistor to have a considerable amplification in the non-hysteretic operation of the device can be expressed as

$$\beta = \partial V_{int}/\partial V_g = C_{FE}/\left(C_{FE} + C_{int}\right) \gg 1, \tag{2}$$

$$C_{total} = \left(C_{FE}^{-1} + C_{int}^{-1}\right)^{-1} > 0. \tag{3}$$

One important consequence of a large internal amplification factor , β, is the lowering of the body factor, m:

$$m = \frac{1}{\beta} \times \frac{\partial V_{int}}{\partial \psi_s} = \frac{1}{\beta} \times \left(1 + \frac{C_S}{C_{OX}}\right) \ll 1. \tag{4}$$

where C_S and C_{OX} are the semiconductor and gate oxide capacitances respectively.

III. Negative Capacitance Tunnel FET

In this section, we report experimental results obtained by connecting an external PZT capacitor to the gate of an *n*-type strained Silicon-NanoWire (Si-NW) array TFET. The device consists of five common gate nanowires with a cross section of $30 \times 5nm^2$ and a gate length of $350\mu m$. This external connection offers the advantage of testing many PZT capacitors and transistors until the best matching is obtained. For this experiment, $50nm$ of $Pb(Zr_{43}, Ti_{57})O_3$ (PZT) ferroelectric film has been grown via the chemical solution deposition root on a Pt-coated silicon wafer. The stack of $Pt(100nm)/TiO_2(30nm)$ has been sputtered on a $SiO_2(500nm)/Si$ wafer at $300°C$ [10]. The relative permittivity, coercive field, and remanent polarization of $220-240$, $260kV/cm$, and $32\mu C/cm^2$ have been measured through the *Pt* top electrode. Generally, high-quality epitaxial layers are employed for negative capacitance devices. The demonstration of NC effect using a polycrystalline ferroelectric layer constitutes a significant step towards the integration of NC gates in CMOS technology. In fact, fabrication of epitaxial perovskite layers on silicon is an extremely challenging task, whereas polycrystalline ferroelectrics (like PZT) can be integrated.

Fig. 2 and Fig. 3 depict experimental performance boosting, reached on relatively fair homojunction TFETs with an *on*-current of $0.1\mu A$ ($V_g = 2V$ and $V_d = 0.5V$) and a swing is in the order of $100-150mV/dec$, in hysteretic and non-hysteretic modes of operation. Fig. 2-a reports a hysteretic characteristic where the values of C_{PZT} and C_{int} are verifying conditions (2) and (3) only in a limited range of operation (for gate voltages larger than the threshold voltage). In this case, the performance boosting is narrowed down to a reduced region. Figs. 2-b, 2-c, and 2-d summarize the effects of the PZT negative capacitance on the SS (no improvement), g_m (1 to 2 orders of magnitude), and I_{ON} (a factor of up to 16x). Such a hysteretic NC Tunnel FET can still be considered for low power hysteretic logic applications or as a 1 TFET ferroelectric memory cell with improved *on*-current performance [11].

In the other case, we exploit another NC-TFET in the same configuration with a different TFET and PZT capacitor, matching in the entire range of the gate voltage (Fig. 3). The area of

the utilized PZT capacitor is half of the previous experiment that is providing lower negative capacitance. Therefore, the total capacitance of the structure remains positive and the non-hysteretic operation of the device can be achieved. In this late case, a significant double improvement in the SS and overdrive is observed in a hysteresis-free NC-TFET. The NC effect appears to reduce only moderately the subthreshold swing and extends the region of low slope values (Fig. 3-b); this is probably due to the low β value in the matching equation (1). Moreover, due to the poor swing ($150mV/dec$) of the initial TFET, the represented NC-TFET does not reach sub-thermionic slope values. Other limiting factors of TFETs are their poor transconductance and *on*-current. Fig. 3-c shows the obtained boosting of g_m, ranging from 10 to 5×10^3 times of its original value, due to the differential amplification of the surface potential by NC effect. The *on*-current is boosted over the whole operation range, reaching a factor of about 500x at the maximum gate voltage (Fig. 3-d). This is reflected by a body factor reduction below 1, acting as a performance booster in the region of low *on*-current [12]. In equation (2), at higher V_g, the C_{int} is close to C_{FE} and $\beta \gg 1$. Consequently, the body factor, m, becomes significantly smaller than 1 (see equation 4). It follows that the gate voltage can be reduced by 65%, maintaining the same level of the output current [13]. The non-hysteretic NC-TFET could be a potential candidate for low-power steep slope switches for both analog and digital applications. It should be remarked that the leakage and charge trapping mechanisms are neglected due to the fact that the gate leakage in both hysteretic and non-hysteretic devices is systematically lower than the *on*-current.

IV. Negative Capacitance MOSFET

The same negative capacitance booster is externally connected to the gate of various *n*-MOSFETs that are manufactured in 28nm CMOS technology and also larger devices which are fabricated on an SOI substrate. Different combinations of PZT capacitors and MOSFETs have been examined to obtain NC-FETs in hysteretic and non-hysteretic operation modes. The experiments are conducted with the same PZT capacitors reported in the previous section. All measurements have been carried out at low drain voltages due to the fact that a high drain voltage provides a non-uniform potential profile along the channel and the NC effect cannot be observed [14].

Fig. 4-a shows the hysteretic behavior of an NC-FET with a 28nm CMOS process MOSFET ($W = 333\mu m$, $L = 30nm$) and a PZT capacitor with an area of $30\mu m \times 30\mu m$. In this late case, a swing of $4mV/dec$ is achieved over six decades of current in the linear operation mode ($V_d = 100mV$). It should be remarked that due to the small intrinsic gate capacitance of 28nm commercial MOSFETs, the total capacitance of the NC-FET cannot be positive in the whole range of experiment ($C_{total} > 0$ condition is not fulfilled).Therefore, the NC-FET is not stable and provide hysteresis [6].

MOSFETs on an SOI silicon wafer with relatively large dimensions are fabricated to fulfill the condition for non-hysteretic operation of a non-hysteretic NC-FET. The devices are built on a *p*-type SOI substrate with $88nm$ of epitaxial

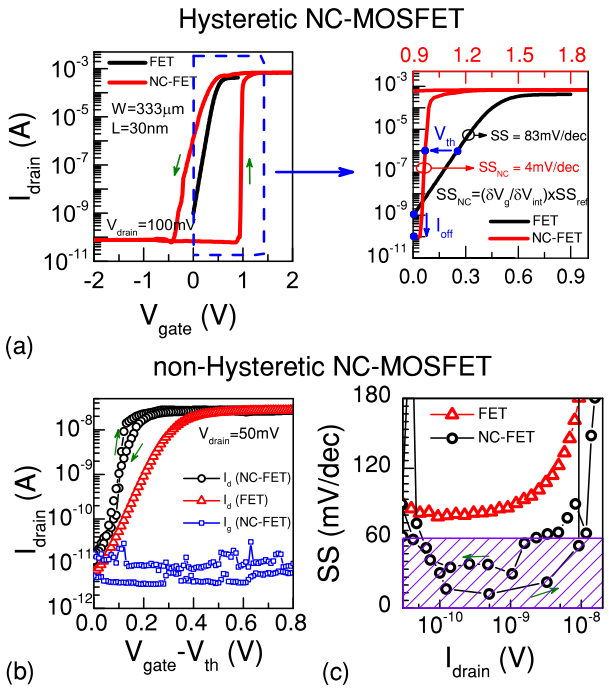

Fig. 4. (a) Effect of the NC on DC characteristics of an *n*-type commercial MOSFET fabricated in 28nm CMOS technology (W=333μm, L=30nm). Subthreshold swing of $4mV/dec$ over six decades of current is achieved together with a $1.5V$ hysteresis. A MOSFET with approximately 4x larger gate area/capacitance (W=19μm, L=2μm) fabricated on an SOI substrate with a full matching of the MOS and ferroelectric NC is demonstrated in (b) where a sub-thermal swing is achieved in a hysteresis-free NC-FET.

silicon (thinned down to $30nm$) and $145nm$ of BOX. A $3nm$ layer of HfO_2 has been deposited by ALD on an ultra thin layer of SiO_2 as the gate dielectric. Fig. 4-b demonstrates the transfer characteristic of a hysteresis-free NC-FET with a drain voltage of $50mV$. The gate width and gate length of the reference MOSFET are respectively $19\mu m$ and $2\mu m$ while the PZT capacitor has an area of $20\mu m \times 20\mu m$. A significant enhancement in the SS of the device is obtained when the ferroelectric and gate capacitances are fully matched so that a non-hysteretic NC operation can be achieved. The ferroelectric provides an effective NC in the subthreshold region of MOSFETs ($\beta < 1$) which results in a sub-thermal swing ($20mV/dec$) [15].

V. Conclusion

The hysteretic and non-hysteretic behavior of negative capacitance tunnel FETs and MOSFETs are experimentally investigated in this letter. It has been evidenced that the negative capacitance can be efficiently utilized to significantly enhance the *on*-current and transconductance of TFETs in the overdrive region while it improves the subthreshold swing of MOSFETs. A matching condition is proposed and satisfied between the ferroelectric and MOS capacitors for the non-hysteretic operation of negative capacitance transistors.

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