Nanoscale MOSFET Modeling for the Design of Low-power Analog and RF Circuits
Part I

Invited Paper
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Abstract—This paper presents the simplified charge-based EKV MOSFET model and shows that it can be used for advanced CMOS processes despite its very few parameters. The concept of inversion coefficient $IC$ is first introduced as an essential design parameter that replaces the overdrive voltage $V_{DS}-V_{TH}$ and spans the entire range of operating points from weak to strong inversion, including the effect of velocity saturation (VS). The simplified model in saturation is then presented and validated for different 40-nm and 28-nm bulk CMOS processes. A very simple expression of the normalized transconductance $G_m/ID$ is described. The normalized transconductance efficiency $G_m/ID$, which is a key figure-of-merit (FoM) for the design of low-power analog circuit, is then derived as a function of $IC$ including the effect of VS. It is then successfully validated from weak to strong inversion with data measured on a 40-nm and two 28-nm bulk CMOS processes. It is then shown that the normalized output conductance $G_{ds}/ID$ follows a similar dependence with $IC$ than the normalized $G_m/ID$ characteristic but with different parameters accounting for DIBL. The methodology for extracting the few parameters from the measured $I_D-V_T$ and $I_D-V_{DS}$ characteristics is then detailed. Finally, it is shown that the simplified EKV model can also be used for a fully depleted SOI (FDSOI) and FinFET 28-nm processes.

I. INTRODUCTION

With its stringent requirements on the energy consumption of electronic devices, the Internet of Things (IoT) has become the primary driver for the design of low-power analog and RF circuits [1]. The implementation of increasingly complex functions under highly constrained power and area budgets, while circumventing the challenges posed by modern device technologies, makes the analog/RF design exercise ever more challenging. The designer often needs to make optimum choices to achieve the required gain, current efficiency, bandwidth, linearity and noise performance [2], [3]. To this purpose, he often starts his new design using simple transistor models to explore the design space and identify the region offering the best trade-off, before fine tuning his design by running more accurate simulations using the full fetched compact model available in the design kit [4], [5]. This task has been made more difficult in advanced CMOS technologies due to the down-scaling of CMOS processes and the reduction of the supply voltage, which has progressively pushed the operating point from the traditional strong inversion (SI) region towards moderate (MI) and even weak inversion (WI), where the simple quadratic model is obviously no more valid [6], [7]. This has led to an increased interest in the concept of inversion coefficient as the main design parameter replacing the overdrive voltage even for advanced technologies [8], [9].

This paper presents the simplified EKV transistor model in saturation since, except for switches, most transistors in CMOS analog circuits are biased in saturation. The paper is split in two parts: the first part introduces the simplified EKV model in saturation and shows that it can be used even for advanced bulk CMOS technologies. The second part of the paper will show how the inversion coefficient can be used as the main design parameter to describe various figures-of-merit (FoM) to explore basic trade-offs faced in analog and RF design.

This first part of the paper is organized as follows. Section II introduces the concept of inversion coefficient and shows how the specific current can be extracted by means of a current reference for a given technology. Section III presents the simplified EKV MOS transistor model in saturation, including the validation of the large- and small-signal models for several advanced 40-nm and 28-nm bulk CMOS processes. The transconductance efficiency $G_m/ID$ and the output conductance-to-current ratio $G_{ds}/ID$ are then introduced in Section IV as key FoMs and validated for the same processes including the important effect of velocity saturation. Section V explains how to extract the few model parameters and Section VI shows that the simplified EKV model can also be used for advanced fully-depleted SOI (FDSOI) and FinFET technologies. The conclusion are finally given in Section VII.

II. THE CONCEPT OF INVERSION COEFFICIENT

A. Definition

The inversion coefficient $IC$ is a measure of the inversion level in the channel of a single MOSFET and is defined as [10]:

$$IC \triangleq \frac{I_D}{I_{spec}}|_{saturation}, \quad (1)$$

where the normalizing factor $I_{spec}$ is called the specific current, and is defined as [10]

$$I_{spec} \triangleq I_{spec\square} \frac{W}{L} \quad \text{with} \quad I_{spec\square} \triangleq 2n\mu_C C_{ox} U_T^2, \quad (2)$$

$$\DeclareMathOperator{spec}{spec}$$
The different regions of operation in terms of inversion coefficient.

where $W$ and $L$ are the width and length of the transistor, $n$ is the slope factor, $\mu_0$ is the low field mobility in the channel region, $C_ox$ the oxide capacitance per unit area and $U_T \triangleq kT/q$ is the thermodynamic voltage. In a given technology, the specific currents per square $I_{spec}$, one for each transistor type (n- and p-channel), are the most fundamental parameters for the designer.

Using $I_C$, the different regions of operation of a MOSFET can be classified as illustrated in Fig. 1 and defined below

$$0.1 < I_C \leq 1 \quad \text{weak inversion (WI)},$$

$$10 < I_C \leq 10 \quad \text{strong inversion (SI)}.$$  \hspace{1cm} (3)

The specific current has originally been defined in [11] using the normalized $G_{m}nU_{T}/I_D$ characteristic as discussed in Section IV. It corresponds to the drain current for which the long-channel SI asymptote $1/\sqrt{I_C}$ crosses the WI asymptote which turns out to be equal to unity as shown in Fig. 2.

The specific current $I_{spec}$ can actually be extracted for a given technology and transistor type using the circuit shown in Fig. 2 [12, 13]. This circuit is based on the Vittoz current reference represented by transistors M1 to M4, where the original resistor is replaced by M6 [14]. M1-M2 are biased in WI and saturation, whereas M6, M7 in SI (M6 in the linear region and M7 in saturation). Assuming that $A \gg 1$, it can be shown that the bias current $I_b$ is proportional to $I_{spec}$ and $I_{spec}^2$

$$I_b = I_{spec} \cdot A \cdot \ln^2(K) = I_{spec} \cdot \ln^2(K),$$ \hspace{1cm} (4)

where $K \triangleq \beta_2/\beta_1$ with $\beta_i = \mu_0 C_ox W_i/L_i$ for $i = 1, 2$. This circuit enables to precisely set the inversion coefficient of any n-channel transistor independently of the value of the threshold voltage from the reference transistor. Indeed, any n-channel transistor Mx can be operated at a given inversion factor $I_{C_x}$ by means of a weighted copy of current $I_b$. For a transistor Mx that has to be biased in WI, it is best to use transistor M1 as a reference transistor whereas M7 should be used as reference transistor for biasing a transistor in SI. The drain current of transistor Mx is then $N$ times the bias current $I_b = N \cdot I_b$ and hence $I_{C_x} \cdot W_x/L_x = N \cdot I_{C1} \cdot W_1/L_1$. The aspect ratio $W_x/L_x$ of transistor Mx is then given by

$$W_x/L_x = N \cdot \frac{I_{C1}}{I_{C_x}} \cdot \frac{W_1}{L_1}.$$ \hspace{1cm} (5)

This circuit is therefore ideal for migrating circuits from one technology to another with a minimum of redesign. Note that another current reference is needed for extracting the specific current for p-channel transistors.

III. THE SIMPLIFIED EKV MOSFET MODEL

A. The Large-signal DC Model

The drain current in saturation normalized to the specific current, which actually corresponds to the inversion coefficient $I_C$ defined above, is given by [15, 16]

$$I_C = \frac{4(q_s^2 + \lambda_c)}{2 + \lambda_c + \sqrt{4(1 + \lambda_c)} + \lambda_c^2(1 + 2q_s)^2}$$ \hspace{1cm} (6)

where $q_s$ is the normalized inversion charge $q_s \triangleq Q_s/Q_{spec}$ taken at the source with $Q_{spec} \triangleq -2nU_T C_{ox}$ [10]. Parameter $\lambda_c$ is accounting for velocity saturation (VS) according to

$$\lambda_c \leq \frac{\lambda_{sat}}{L},$$ \hspace{1cm} (7)

and scales inversely proportional to the transistor length $L$. $\lambda_c$ actually corresponds to the fraction of the channel in which the carrier drift velocity reaches the saturated velocity $v_{sat}$ over a portion of the channel length $L_{sat}$ defined as

$$L_{sat} = \frac{2\mu_0 U_T}{v_{sat}}.$$ \hspace{1cm} (8)

The normalized source charge $q_s$ is related to the terminal voltages by [10]

$$\frac{V_P - V_S}{U_T} = 2q_s + \ln(q_s)$$ \hspace{1cm} (9)

where $V_P - V_S$ is the saturation voltage for a long-channel transistor (i.e. without VS), $V_P \equiv (V_G - V_{T0})/n$ is the pinch-off voltage and $V_S$ is the source-to-bulk voltage. Note that in the EKV model, all the terminal voltages are referred to the local substrate instead of the source terminal, in order to preserve the symmetry of the device in the model [10].

The normalized saturation voltage can be expressed in terms of the inversion coefficient $I_C$ by solving (6) for $q_s$ leading to

$$q_s = \frac{1}{2} \left( \sqrt{4I_C^2 + (1 + \lambda_c \cdot I_C^2)^2} - 1 \right)$$ \hspace{1cm} (10)

and using (10) in (9). Unfortunately, (9) cannot be inverted to express $I_C$ in terms of $V_P - V_S$ and hence of the terminal voltages.

This simplified charge-based model only requires four parameters to fit the $I_P-V_G$ transfer characteristic: the slope factor $n$, the specific current per square $I_{spec}$, the threshold
voltage $V_{T0}$ and the velocity saturation parameter $L_{sat}$. The methodology to extract these parameters from measured data is explained in Section [V]. Typical values for these parameters for a 28-nm bulk CMOS process are given in Table I.

The $I_D$ versus $V_G - V_{T0}$ transfer characteristics are plotted in Fig. 3 and compared to measurements made on wide and minimal length transistors from three different processes, namely a 40-nm and two different 28-nm bulk CMOS processes. Although the drain current is measured from sweeping the gate voltage, the simplified EKV model is calculated from the measured current by first normalizing it to the specific current and minimal length transistors from a 28-nm bulk CMOS process. The difference with the voltages are all referred to the bulk, we can define two gate transconductance $G_{md}$ and drain induced barrier lowering (DIBL).

Fig. 4 shows the inversion coefficient versus the drain voltage $V_D$ for different overdrive voltages measured on a large and minimal length transistor from a 28-nm process. It shows that the current can be approximated in saturation by a simple linear characteristics

$$I_D \approx G_{ds} \cdot (V_D + V_M),$$

where $V_M$ is the channel length modulation (CLM) and $G_{ds}$ is the output conductance which corresponds to the slope and is discussed further in the next section.

B. The Small-signal DC model

The most important small-signal parameter is without doubt the gate transconductance $G_m$. Since in the EKV model the voltages are all referred to the bulk, we can define two other transconductances: the source transconductance $G_{ms} \equiv -\partial I_D/\partial V_S$ and the drain transconductance $G_{md} \equiv \partial I_D/\partial V_D$. Note that $G_{md}$ should not be confused with the output conductance $G_{ds}$. In saturation $G_{md} = 0$ and $G_{ms} = n \cdot G_m$.

\footnote{Note that even though the parameter $V_M$ is called the CLM voltage, it actually embeds all the effects, including VS and DIBL, which is actually dominant in WL.}

Table I: Typical Parameter Values for a 28-nm Process.

<table>
<thead>
<tr>
<th>Channel Type</th>
<th>$I_{spec}$ [nA]</th>
<th>$V_{T0}$ [V]</th>
<th>$L_{sat}$ [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-channel</td>
<td>1.1 - 1.5</td>
<td>850</td>
<td>0.4 - 0.55</td>
</tr>
<tr>
<td>p-channel</td>
<td>1.1 - 1.5</td>
<td>350</td>
<td>0.35 - 0.5</td>
</tr>
</tbody>
</table>

![Fig. 3: IC versus VD measured for different overdrive voltages measured on a minimum length transistor from a 28-nm bulk CMOS process.](image)

![Fig. 4: IC versus VD measured for different overdrive voltages measured on a minimum length transistor from a 28-nm bulk CMOS process.](image)

![Fig. 5: Normalized transconductance $g_{ms}$ versus IC measured on minimum length transistors from a 40-nm and two different 28-nm bulk CMOS processes.](image)
The normalized source transconductance in saturation $g_{ms}$ can be expressed in terms of $IC$ as \[ g_{ms} = \frac{G_{ms}}{G_{spec}} = \frac{n \cdot G_{in}}{G_{spec}} = \frac{\sqrt{(\lambda c IC + 1)^2 + 4IC} - 1}{\lambda c (\lambda c IC + 1) + 2}, \] (12) where $G_{spec} = I_{spec}/U_T = 2n\lambda_0C_{ox}U_T$, $g_{ms}$ is plotted versus $IC$ in Fig. 5 and favorably compares to measurements obtained from the derivative of the characteristics shown in Fig. 3 over a very wide range of bias (more than 4 decades of current). Note that for short-channel devices in SI, the $I_D-V_G$ transfer characteristic becomes a linear function of the gate voltage as illustrated in Fig. 3 and hence the gate transconductance becomes independent of the drain current and of the gate length $L$. It then only depends on $W$ and $v_{sat}$ according to

$$g_{ms} \approx 1/\lambda c \text{ for } IC \gg 1 \text{ or } G_m \approx WC_{ox}v_{sat}. \quad (13)$$

The inverse of the VS parameter $\lambda c$ is therefore a key parameter since it gives the maximum normalized transconductance that can be achieved for a short-channel device in a given technology.

The other key dc small-signal parameter is the output conductance $G_{ds}$ which, together with the transconductance, defines the intrinsic (or self) gain $G_m/G_{ds}$. As mentioned above, the output conductance is the result of several physical effects including VS, CLM and DIBL. In advanced short-channel devices biased in MI or WI, DIBL is the dominant effect. The latter is defined as the variation of the threshold voltage with respect to the applied drain-to-source voltage, i.e., $\partial V_T/\partial V_{DS}$ and can be modeled as \[ V_T \approx V_{TH} \cdot (1 - \sigma_d \cdot V_{DS}), \quad (14) \]

where the parameter $\sigma_d \approx \partial V_T/\partial V_{DS}$ accounts for DIBL and depends on $L$ and $V_{TH}$\cite{18, 19}. The output conductance can then be written as \[ G_{ds} \approx \frac{\partial I_D}{\partial V_{DS}} = \frac{\partial I_D}{\partial V_T} \cdot \frac{\partial V_T}{\partial V_{DS}} = \sigma_d \cdot G_m. \quad (15) \]

where $\partial I_D/\partial V_T = -G_m$ has been used. A model of the output conductance versus $IC$ can now be derived using the expression of $G_m = G_{ms}/n$ in saturation given in \cite{12}, where $\lambda c$ is replaced by an additional parameter $\lambda x$

$$G_{ds} \approx \frac{G_{ds}}{G_{spec}} = \frac{\sigma_d}{n} \cdot \frac{\sqrt{(\lambda x IC + 1)^2 + 4IC} - 1}{\lambda x (\lambda x IC + 1) + 2}. \quad (16)$$

The normalized output conductance versus $IC$ given by \cite{16} is plotted in Fig. 6 and compared to measurements made on a long and a short transistor from a 28-nm CMOS process. Fig. 6 shows that the model fits very well the measured data over more than 5 decades of current and its simplicity.

**IV. THE TRANS CONDUCTANCE EFFICIENCY $G_m/ID$**

The transconductance efficiency $G_m/ID$, sometimes also called the current efficiency, is one of the most important FoM for low-power analog circuit design. It is a measure of how much transconductance is produced for a given bias current and is a function of $IC$. As will be shown in the second part of this paper, the transconductance efficiency (or its inverse) appears in many expressions related to the optimization of analog circuits. In normalized form, the transconductance efficiency is defined as the actual transconductance obtained at a given $IC$ with respect to the maximum transconductance $G_m = I_D/(nU_T)$ reached in WI\cite{4, 15}

$$\frac{g_{ms}}{IC} = \frac{G_m \cdot nU_T}{ID} = \frac{\sqrt{(\lambda x IC + 1)^2 + 4IC} - 1}{IC \cdot [\lambda x (\lambda x IC + 1) + 2]} = \frac{\sqrt{(\lambda c IC + 1)^2 + 4IC} - 1}{IC \cdot [\lambda c (\lambda c IC + 1) + 2]}. \quad (17)$$

The expression in (17), which is continuous from WI to SI and includes the effect of VS, is plotted in Fig. 7. The figure shows that $G_mU_T/ID$ is maximum in WI and decreases as $1/\sqrt{IC}$ in SI for long-channel devices in which VS is absent (dashed blue curve). Note that the specific current has been defined from the $G_mU_T/ID$ vs $ID$ characteristic of a long channel transistor as the current at which the WI and SI asymptotes cross. This is why these two asymptotes cross at $IC = 1$ when $G_mU_T/ID$ is plotted versus $IC$ as in Fig. 7.

As shown in Fig. 3 for short-channel devices subject to VS, the drain current in SI becomes a linear function of the gate voltage, independent of the transistor length. Hence, the transconductance becomes independent of the current and of the length. Since $G_m$ becomes independent of $ID$, and hence
of IC, the $G_m U_T/I_D$ curve scales like $1/(\lambda_c IC)$ in SI (red curve) instead of $1/\sqrt{IC}$ when VS is absent. In essence, the effect of VS is to degrade the transconductance efficiency in SI, meaning that more current is required to obtain the same transconductance than without VS. Nevertheless, irrespective of the channel length, $G_m U_T/I_D$ remains invariant (i.e. $g_{ms}/IC = 1$) in WI, since short-channel effects (SCE), including VS, have the same effect on $G_m$ than on $I_D$ simply because $G_m$ is proportional to $I_D$ in WI. As shown in Fig. 7, the inversion coefficient for which the SI asymptote of a short-channel device crosses the horizontal unity line is equal to $1/\lambda_c$. As discussed in the next Section, this is actually how the parameter $\lambda_c$ is extracted from measurements on a short-channel device.

The normalized transconductance efficiency given by (17) is compared to measurements in Fig. 8 for the same devices as shown in Fig. 3 and Fig. 5. Despite the normalized $G_m U_T/I_D$ only requires one parameter ($\lambda_c$ or $L_{sat}$), the model fits very well to the data over more than 5 decades of IC.

In a similar way, we can define the $G_{ds}/I_D$ ratio, which from (11) turns out to be about equal to $1/V_M$ for $V_D \ll V_M$.

In normalized form, we have

$$U_T \approx \frac{G_{ds} U_T}{I_D} = \frac{g_{ds}}{IC} = \frac{\sigma_d}{IC} \cdot \frac{\sqrt{((\lambda_d IC + 1)^2 + 4IC - 1)}}{\lambda_d (\lambda_d IC + 1)^2 + 2}.$$  (18)

From (18), we can deduce that the highest output conductance for a given current is reached in WI and is equal to $G_{ds-max} = \sigma_d I_D/(nU_T)$. We can then normalize the output conductance to $G_{ds-max}$ in order for the normalized output conductance to reach unity in WI

$$\frac{G_{ds}}{G_{ds-max}} = \frac{n}{\sigma_d} \cdot \frac{g_{ds}}{IC} = \frac{\sqrt{((\lambda_d IC + 1)^2 + 4IC - 1)}}{IC \cdot \lambda_d (\lambda_d IC + 1)^2 + 2}.$$  (19)

Eq. (19) is plotted in Fig. 9 and compared to measurements made on the same transistors than in Fig. 6 and shows good agreement with the measured data. Note that, unlike for the transconductance, where we want to get the highest transconductance for a given current which is reached in WI, the output conductance should be minimized for a given current.

It will be shown in the second part of this paper that, even though the output conductance decreases in SI, the self gain remains actually maximum in WI and simply equal to $1/\sigma_d$.

V. PARAMETER EXTRACTION

The four parameters $n$, $I_{spec}$, $V_{T0}$ and $L_{sat}$ required for fitting the simplified model described in Section III-A to measured $I_D$-$V_G$ data can be extracted from measurements following the procedure described below. The extraction starts from the $I_D$-$V_G$ characteristic measured on a wide and long transistor. After calculating (or measuring) the derivative $G_m$, the slope factor $n$ is extracted from the plateau reached by the $I_D/(G_m U_T)$ curve in WI as shown in Fig. 10. The specific current for this particular device is then obtained by the intersection between the SI asymptote $\propto \sqrt{I_D}$ and the slope factor horizontal line as shown in Fig. 10. For this particular long-channel device, this results in $n = 1.22$ and $I_{spec} = 13 \mu A$ from which we can derive the specific current per square $I_{spec}$ by dividing by the aspect ratio $W/L$.

The VS parameter $\lambda_c$ is extracted as shown in Fig. 11 from the normalized $G_m U_T/I_D$ characteristic of a wide and short
channel transistor as the $1/IC$ corresponding to the intersection of the $1/IC$ asymptote with the unity horizontal line after having properly extracted the slope factor $n$ which is usually affected by short-channel effects ($n = 1.48$ in this case compared to $n = 1.22$ as extracted from the long-channel device). This results in $\lambda_c = 0.48$ and hence $L_{sat} = 19.5 \text{nm}$ for this particular 40-nm transistor.

Finally, the threshold voltage is extracted from the $ID-V_G$ characteristic to fit the measured data as shown in Fig. 3.

The DIBL parameter $\sigma_d$ used for the output conductance can be extracted in a similar way than the slope factor $n$ by looking at the plateau of the normalized $G_{ds}nUT/ID$ curve reached in WI, while the $\lambda_d$ parameter can be extracted in a similar way than the VS parameter $\lambda_c$ from the normalized $G_{ds}/G_{ds-max}$ given by (19) for a short transistor.

VI. SIMPLIFIED MODEL APPLIED TO FDSOI AND FINFET

Although the simplified model described above was developed for transistors fabricated in a bulk CMOS process, it can also be used for transistors fabricated in a fully-depleted silicon-on-insulator (FDSOI) process. However, it doesn’t model the effect of the additional back gate available in FDSOI processes and the extracted parameters would be valid only for a single back gate voltage. An example of $IC$ versus $V_G - V_{T0}$ and $G_m nUT/ID$ versus $IC$ measured on 3 different transistor lengths from a 28-nm FDSOI process are shown in Fig. 12. Except for some deviation observed on the $G_m nUT/ID$ versus $IC$ at high $V_G$ values, which is probably due to additional mobility reduction due to vertical field, the match between the model and the measured characteristics is surprisingly good.

The model was even tried with transistors coming from a 28-nm FinFET process. Fig. 13 show the $IC$ versus $V_G - V_{T0}$ and $G_m nUT/ID$ versus $IC$ measured on 3 different transistor lengths. Again, after proper parameter extraction, the model fits the measured data very well, despite the simplicity of the model.

VII. CONCLUSION

Analog designers usually like to use simple analytical transistor models to help them identify the optimum bias region in the overall design space where they can pick an initial point close to the optimum target by setting the bias and choosing the transistor size. Further optimization can then be conducted using circuit simulators with the full fetched compact model available in the design kit. Because of the down-scaling of the supply voltage inherent to advanced CMOS technologies, the operating points are pushed more and more towards moderate and even weak inversion, where the standard quadratic model obviously doesn’t hold anymore. A simple transistor model valid in all regions of operation from weak to strong inversion is therefore required. This first part of the paper presents the simplified EKV model in saturation and shows that, despite the very few number of parameters, it can successfully model the large- and small-signal behavior over a wide range of bias.

The concept of inversion coefficient $IC$ is first introduced to replace the overdrive voltage as the main design parameter covering the whole range of operating points from weak to strong inversion across moderate inversion. $IC$ is defined as the ratio of the drain current in saturation to the specific current $I_{spec}$. The later is proportional to $W/L$ and to the specific current per square $I_{spec2}$. The slope factor $n$ is the most important parameter for the analog designer. It is shown that the specific current can be extracted using a current reference circuit that provides a bias current that allows to precisely set the inversion coefficient of a given transistor. This bias technique is limited...
by the transistor matching but is completely independent of the threshold voltage and its variations.

The simplified EKV charge-based model in saturation is then presented and the $I_{DG}$-$V_{GG}$ transfer characteristic is validated for different 40-nm and 28-nm bulk CMOS processes. A very simple expression of the normalized transconductance versus $IC$ is presented requiring only a single parameter, namely the VS parameter $\lambda_c$. It is shown that the maximum normalized transconductance reached by a short-channel transistor in SI is simply equal to $1/\lambda_c$. The normalized transconductance efficiency $G_{m}\sqrt{nU_{T}/ID}$, which is a key FoM for the design of low-power analog circuit, is then derived as a function of $IC$. It is shown that the $G_{m}\sqrt{nU_{T}/ID}$ characteristic of a short-channel transistor in SI decreases as $1/(\lambda_c IC)$ instead of $1/\sqrt{I_C}$ for a long-channel transistor. This means that because of VS, more current is required to reach the desired transconductance for a short-channel device compared to the ideal case where VS would be absent. Despite it also requires only the VS parameter $\lambda_c$, the $G_{m}\sqrt{nU_{T}/ID}$ versus $IC$ fits the measured data from 40-nm and 28-nm bulk CMOS processes extremely well over a large range of bias.

It is then shown that the normalized output conductance $G_{ds}U_{T}/ID$ follows the same dependence than the normalized $G_{m}\sqrt{nU_{T}/ID}$ characteristic, but with a different parameter $\lambda_d$ replacing $\lambda_c$ and an additional parameter $\sigma_d$ accounting for the effect of DIBL.

It is then shown how to extract all the required parameters from the $I_{DG}$-$V_{GG}$ and $I_{D}$-$V_{DD}$ characteristics measured in saturation on a long- and a short-channel device.

Finally, it is shown that the simplified EKV model can also be used for transistors from a FDSoI and FinFET 28-nm processes.

REFERENCES