Linear Analysis of Phase Noise in LC oscillators in Deep Submicron CMOS Technologies

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***Abstract*—This paper investigates the phase noise in LC oscillators with NMOS cross-coupled pair by means of a linear analysis. The latter includes the impact of noise sources that are often neglected, such as gate leakage shot noise, induced gate noise and all terminal access resistances noise. Despite not considering up-conversion of flicker noise, this linear analysis still provides reliable and useful results, demonstrated by means of a detailed comparison between the analytical description and simulations results from a 40 nm and a 28 nm CMOS technology.**

***Index Terms*—LC oscillators, phase noise, linear analysis, inversion coefficient**

I. Introduction

The typical architecture of transceivers used in radios relies on frequency synthesizers for generating accurate and low-noise carriers, which are used to up- and down-convert the base-band signal carrying data. Voltage-Controlled-Oscillators (VCO) are one of the key building blocks of frequency synthesizers and they are usually classified in two families: harmonic (i.e. LC-based) and relaxation oscillators (i.e. ring-based). The former category includes the oscillators which are more suited for the aforementioned purpose, since they embed an LC tank to select the target frequency. As a consequence, the output is an almost perfect sinusoid and its phase noise performance is pretty good, compared to the more noisy square wave produced by a ring-oscillator. However, the better output signal quality comes at the price of a larger power consumption.

As a matter of fact, due to technology scaling, the impact of parasitic resistances has increased. Indeed, even if the metallic gate has become a process option for most recent technology nodes (e.g. 28 nm technology), the gate resistance measured on these devices is still relevant and even greater than in older nodes [1] [2]. Moreover, the gate leakage shot noise contribution has increased mainly due to the shrinking of the gate oxide thickness, although the inclusion of high-k dielectric materials in latest nodes should attenuate this effect.

An analytical derivation of phase noise is carried out including all noise sources, highlighting the transfer function of each of them to the output. The complete expressions come also in a simplified form, in order to provide an insight into possible strategies for noise optimization.

The paper is organized as follows. In Section II the description of the circuit and of the transistor model with the noise sources is carried out. Section III details the analysis showing a comparison between analytical and simulated results, followed by conclusions.

II. Equivalent Noise Model

A. Description of the circuit

Fig. 1 shows the schematic of the analyzed LC oscillator, i.e. a Class-B oscillator with an NMOS cross-coupled pair only, one of the best-known and widely employed topologies [3]. When the single-ended oscillation amplitude is lower than the supply voltage V_{DD} (theoretical limit), the oscillator operates in the so-called "current limited" regime. In this condition, the output differential voltage amplitude A_{diff} is set by the nonlinear characteristic of the active transistors.

The bias current is steered from one branch to the other once per period, when the respective transistors are active: the larger the amplitude, the harder the current is steered. When the amplitude reaches V_{DD}, it remains almost constant even if the bias current is increased further, making the oscillator to work in the so-called "voltage limited" regime [4].

Phase noise is the random phase quantity which perturbs the oscillation and shifts the output waveform zero-crossings with respect to the ideal values, corresponding to the integer multiples of the nominal period. It originates from the various noise sources in the circuit. In frequency domain, the phase noise manifests itself as a broadening of the output signal spectrum, ideally represented by a single tone at the nominal frequency. Oscillator phase noise has been studied for decades by means of several different methods and techniques. The main approaches are the linear time-invariant analysis [5] [6] and the linear time-variant analysis [7]. The former consists in representing the circuit with its small-signal equivalent and transferring the contribution of each noise source to the output, which is then converted from voltage noise to phase noise. The latter takes into account the instant in which the noise is injected throughout the oscillation period. As a consequence, the Impulse Sensitivity Function (ISF) is derived looking at the effect produced by such an injection. At the end, the output phase is computed by the convolution of each noise source with its own ISF. This method allows to include the contribution from noise sources at frequencies different from the oscillation frequency since they get up- or down-converted. Nevertheless, the improved accuracy comes at the price of increased complexity. For this reason, the first method still provides a reliable tool for a quicker evaluation of an oscillator phase noise performance in the $1/(\Delta\omega)^2$ region, as it is explained in Section III-A.

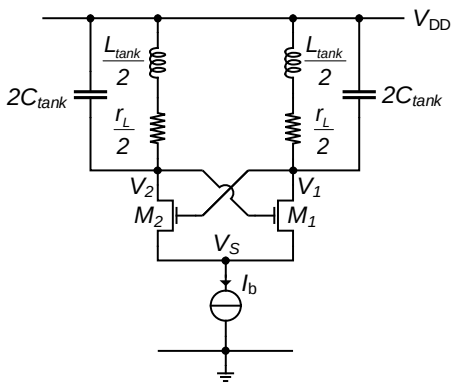

Fig. 1. LC oscillator schematic

B. Description of the transistor model

In this work, the two transistors M_1 and M_2 in Fig. 1 are replaced by their quasi-static (QS) RF small-signal equivalent circuit in saturation with their noise sources, fully described in [1] [8] [9]. The complete RF model includes: the gate and the bulk resistances, $R_{\rm G}$ and $R_{\rm B}$, the source/drain access resistances, $R_{\rm S}$ and $R_{\rm D}$, the parasitic capacitances between gate and source, $C_{\rm GS}$, gate and drain, $C_{\rm GD}$, gate and bulk, $C_{\rm GB}$, source and bulk, $C_{\rm BS}$, drain and bulk, $C_{\rm DB}$. All the capacitances include both extrinsic and intrinsic contributions. Nevertheless, when the operating frequency is in the GHz range, the extrinsic part of the capacitanes dominates. The extrinsic components of $C_{\rm GS}$, $C_{\rm GD}$ and $C_{\rm GB}$ consist of overlap and fringing capacitances, while those of $C_{\rm BS}$ and $C_{\rm DB}$ are junction capacitances. Finally, $I_{\rm m1(2)} = G_{\rm m}(\Delta V_{\rm Gi1(2)} - \Delta V_{\rm Bi1(2)})$ and $I_{\rm ms1(2)} = -G_{\rm ms}\Delta V_{\rm Bi1(2)}$, where $G_{\rm m}$ is the gate transconductance, $G_{\rm ms}$ is the source transconductance and $G_{\rm ds}$ is the output conductance of the cross-coupled transistors. In saturation region, $G_{\rm ms} = nG_{\rm m}$ where n is the slope factor [9].

C. Description of the noise sources

In Fig. 2 the studied noise current sources are reported. $I_{\rm nD1(2)}$ represents the thermal noise generated in the transistor channel, while $I_{\rm nRB1(2)}$ and $I_{\rm nRG1(2)}$ model the parasitic resistances thermal noise. As described in [9], at high frequencies the charge fluctuations within the channel are coupled to the gate terminal through the gate-oxide capacitance. The resulting noise current is called "induced gate noise" and it is modeled by the noise source $I_{\rm nG}$. Moreover, since this noise shares the origin with the channel thermal noise, they are partially correlated [10].

Finally, the noise originated by the gate leakage current due to carrier tunneling through the oxide is represented by the two sources $I_{\rm nlS}$ and $I_{\rm nlD}$. In fact, the gate tunneling current is partitioned between source and drain. Since these leakage currents are due to barrier control processes, they give rise to shot noise, which features a white Power Spectral Density (PSD).

The list of the unilateral PSDs of all the previously described noise sources follows:

$$S_{\rm I_{nD}} = 4\,k\,T\,\gamma_{\rm nD}\,G_{\rm m} \quad (1)$$

$$S_{\rm I_{nRG(B)}} = 4\,k\,T/R_{\rm G(B)} \quad (2)$$

$$S_{\rm I_{nG}} = 4\,k\,T\,\beta_{\rm nG}\,(\omega C_{\rm GS})^2/G_{\rm m} \quad (3)$$

$$I_{\rm nG}\cdot I^*_{\rm nD} = j\,c_{\rm g}\,4\,k\,T\sqrt{\gamma_{\rm nD}\,\beta_{\rm nG}} \quad (4)$$

$$I^*_{\rm nG}\cdot I_{\rm nD} = -j\,c_{\rm g}\,4\,k\,T\sqrt{\gamma_{\rm nD}\,\beta_{\rm nG}} \quad (5)$$

$$S_{\rm I_{nlS(D)}} = 2\,q\,I_{\rm lS(D)} \quad (6)$$

where k is the Boltzmann constant, T is the temperature (300 K), q is the electron charge, $\gamma_{\rm nD}$ is the drain thermal noise excess factor ($2n$/3 in SI and n/2 in WI), $\beta_{\rm nG}$ is the gate thermal noise excess factor ($4/(15n)$ in SI and $1/(5n)$ in WI), $c_{\rm g}$ is the correlation coefficient (0.4 in SI and 0.6 in SI), $\rm I_{lS}$ is the gate to source and $\rm I_{lD}$ the gate to drain leakage current [9].

III. Noise Analysis

A. Description of the analysis

As mentioned in Section II-A, the linear time-invariant analysis consists in computing the transfer functions of each noise current source to the output and then to convert it from voltage noise to phase noise. The last step takes into account that only half on the total noise power is carried by PM components and contributes to phase noise, since AM components are rejected by the oscillator itself.

Fig. 2 shows the small-signal equivalent circuit of the system. To reduce the complexity of the analysis with respect to the complete transistor small-signal model, source and drain access resistances have been excluded, since they are generally so small that the poles associated to them are placed beyond the transistor transit frequency, where this model is not anymore valid. The gate-bulk capacitance $C_{\rm GB}$ has been neglected as well, since it is the smallest among the parasitic capacitances as resulting from device simulations and/or measurements. In the end, the analyzed noise sources are drain noise current, induced gate noise and their correlation, gate and substrate resistance noise current, source and drain leakage noise current. Being a small signal analysis, a small differential oscillation amplitude $A_{\rm diff}$ (a few $U_{\rm T}$) is assumed in order to get valid results. Moreover, this assumption allows to consider the source node $V_{\rm S}$ as a virtual ground.

The first step of the analysis is to apply the KCL to the 6 nodes in the circuit for each noise current, yielding the equivalent differential output noise voltage of the cross-coupled pair $V_{\rm nc} = V_{\rm o2} - V_{\rm o1}$ as a function of the given noise source $I_{\rm ni}$. The second step is to compute the PSD of $V_{\rm nc}$, i.e. $S_{\rm V_{nc}} = V^*_{\rm nc}\cdot V_{\rm nc} = |H_{\rm I_{ni}}|^2 S_{\rm I_{ni}}$, where $H_{\rm I_{ni}}$ is the transfer function from $I_{\rm ni}$ to $V_{\rm nc}$. Then, including the noise coming from the inductor losses, $S_{\rm V_{nL}} = 4\,k\,T\,r$, the total noise voltage PSD $\rm V_n$ is derived as $S_{\rm V_n} \simeq [\omega_0/(2\Delta\omega)]^2\,(S_{\rm V_{nL}} + S_{\rm V_{nc}})$. In the end, the previous result is used to obtain the phase noise in dBc/Hz, $\mathcal{L}(\Delta\omega) = 10\log_{10}(S_{\rm V_n}/A^2)$.

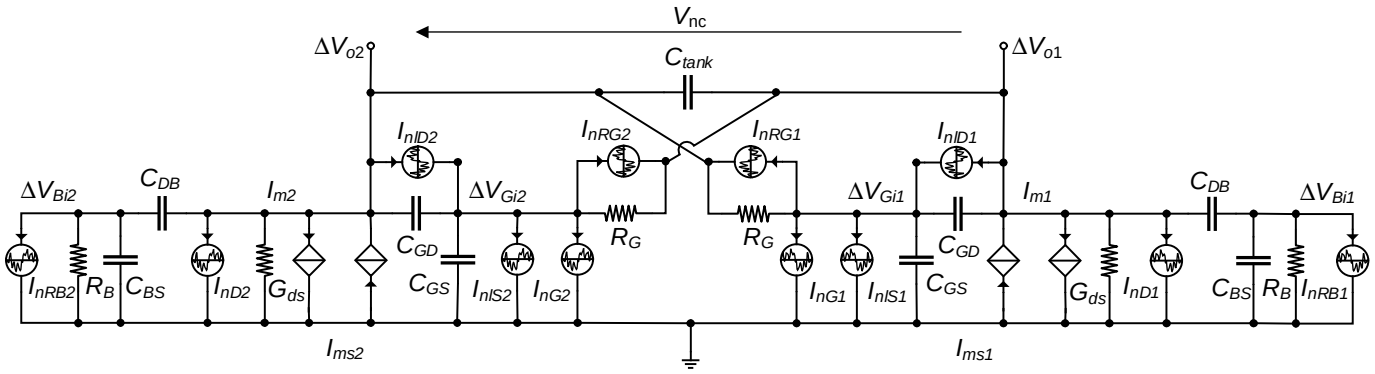

Fig. 2. Cross-coupled pair small signal model with noise sources

B. Analytical expressions

The list of $S_{\mathrm{V_{nc}}}$ of each noise source follows

$$I_{\mathrm{nD}} : 4kT\gamma_{\mathrm{nD}}G_{\mathrm{m}}\ ab/c, \tag{7}$$

$$I_{\mathrm{nRG}} : 4kTR_{\mathrm{G}}\left[G_{\mathrm{m}}^2 + \left(2C_{\mathrm{GD}} + C_{\mathrm{GS}}\right)^2\omega^2\right] a/c, \tag{8}$$

$$I_{\mathrm{nRB}} : 4kTR_{\mathrm{B}}\left[G_{\mathrm{m}}^2\left(n-1\right)^2 + C_{\mathrm{DB}}^2\omega^2\right] b/c, \tag{9}$$

$$I_{\mathrm{nG}} : 4kT\left(\beta_{\mathrm{nG}}C_{\mathrm{GS}}^2\omega^2/G_{\mathrm{m}}\right)\left[\left(1+G_{\mathrm{m}}R_{\mathrm{G}}\right)^2 + C_{\mathrm{GD}}^2R_{\mathrm{G}}^2\omega^2\right] a/c, \tag{10}$$

$$I_{\mathrm{nD}}^{*}I_{\mathrm{nG}} : -4kTc_{\mathrm{g}}R_{\mathrm{G}}C_{\mathrm{GS}}\omega\sqrt{\gamma_{\mathrm{nD}}\beta_{\mathrm{nG}}}\ ad/c, \tag{11}$$

$$I_{nlS} : 2qI_{\mathrm{lS}}\left[1 + \left(2 + G_{\mathrm{m}}R_{\mathrm{G}}\right)\left(G_{\mathrm{m}}R_{\mathrm{G}} + C_{\mathrm{GD}}^2R_{\mathrm{G}}^2\omega^2\right)\right] a/c, \tag{12}$$

$$I_{nlD} : 2qI_{\mathrm{lD}}\left(2 + G_{\mathrm{m}}R_{\mathrm{G}}\right)\left(2 + G_{\mathrm{m}}R_{\mathrm{G}} + C_{\mathrm{GS}}^2R_{\mathrm{G}}^2\omega^2\right) a/c, \tag{13}$$

where

$$a = 1 + \left(C_{\mathrm{DB}} + C_{\mathrm{BS}}\right)^2R_{\mathrm{B}}^2\omega^2, \tag{14}$$

$$b = 1 + \left(C_{\mathrm{GD}} + C_{\mathrm{GS}}\right)^2R_{\mathrm{G}}^2\omega^2, \tag{15}$$

$$c = \left(G_{\mathrm{ds}} - G_{\mathrm{m}}\right)^2 + \left(C_{\mathrm{DB}} + 4C_{\mathrm{GD}} + C_{\mathrm{GS}} + 2C_{\mathrm{tank}}\right)^2\omega^2, \tag{16}$$

$$d = \left[C_{\mathrm{GD}} + \left(C_{\mathrm{GD}} + C_{\mathrm{GS}}\right)\left(1 + G_{\mathrm{m}}R_{\mathrm{G}}\right)\right]\omega. \tag{17}$$

C. Numerical results and comparisons

In order to validate the PSDs shown in Section III-B, the Class-B oscillator has been simulated in ADS and the same parameters have been used to get numerical results from the previous analytical expressions. Two different commercial bulk CMOS technologies have been investigated, namely a 40 nm [1] and a 28 nm. The simulations have been carried out keeping the parameters shown in Table I constant, where $r_{\mathrm{L}} = 2\pi f_0 L_{\mathrm{tank}}/Q_{\mathrm{L}}$ and $C_{\mathrm{tot}} = 1/[(2\pi f_0)^2 L_{\mathrm{tank}}\left(1 + 1/Q_{\mathrm{L}}^2\right)]$. The Inversion Coefficient methodology has been employed in order to validate the results across all the regions of operation of the cross-coupled pair, as described in [9]. Three value of IC have been chosen, i.e. 0.1, 1 and 10, representing Weak, Moderate and Strong Inversion. As pointed out in Section III-B, the bias current I_{b} has been chosen such that A_{diff} = 100 mV for each value of IC and the transistors have been sized accordingly, W/L = $I_{\mathrm{b}}/\left(2\,IC\,I_{\mathrm{spec}_{\square}}\right)$. The parasitic capacitances, G_{m} and G_{ds} have been extracted from the Y-parameters of the transistors, obtained with a separate S-parameter simulation, as described in [1]. Moreover, the leakage currents I_{lS} and I_{lD} have been evaluated using the DC current through the transistors gate. In the end, R_{G} and R_{B} have been estimated from the measurements reported in [1], [2], [11]. As a consequence, they have been removed from the compact model of the transistors.

TABLE I
DESCRIPTION OF SIMULATION PARAMETERS

Tech	$I_{\mathrm{spec}_{\square}}$	n	f_0	L_{tank}	Q_{L}	r_{L}	C_{tot}
40 nm	650 nA	1.48	1 GHz	8 nH	10	5 Ω	3.13 pF
28 nm	850 nA	1.46	1 GHz	8 nH	10	5 Ω	3.13 pF

A Harmonic Balance simulation has been carried out for verifying the oscillator functionality and the phase noise extraction has been run on top of it. In order to carry out a fair comparison between analytical and simulated results, explicit noise sources have been introduced in the schematic. This strategy allows to have direct control on the PSDs of such noise sources. Therefore, in addition to R_{G} and R_{B} and their noise, the drain noise current, the induced gate noise current and the gate leakage currents have been removed from the compact model. As a consequence of the explained approach, the correlation between I_{nD} and I_{nG} couldn't be included and verified.

Figs. 3 and 4 show the phase noise for each noise source separately as $\mathcal{L}_{\mathrm{I_{ni}}}(\Delta\omega)$ evaluated at $\Delta\omega = 2\pi \cdot 1\,\mathrm{MHz}$. The unit of $\mathcal{L}_{\mathrm{I_{ni}}}(\Delta\omega)$ is dBc/Hz, which means difference in dB related to the carrier. For each noise source, analytical and simulated results are reported, including the contribution of both transistors. In general, the simulated values match the analytical counterpart very well for both technologies, except for the phase noise associated to R_{B}. As shown by (9), this contribution depends strongly on the subthreshold slope factor n. This value has been extracted from measurements and it is considered constant from WI to SI although it is actually

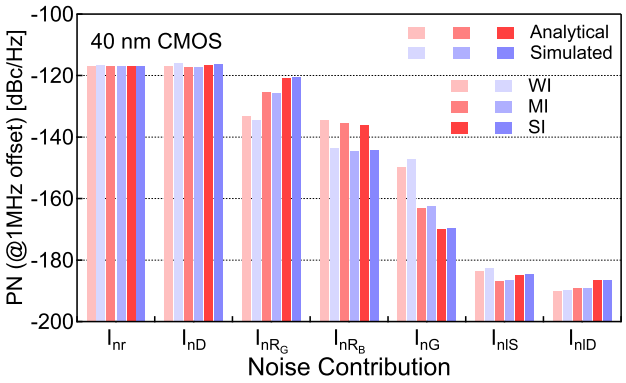

Fig. 3. Phase noise single contributions for 40 nm CMOS technology.

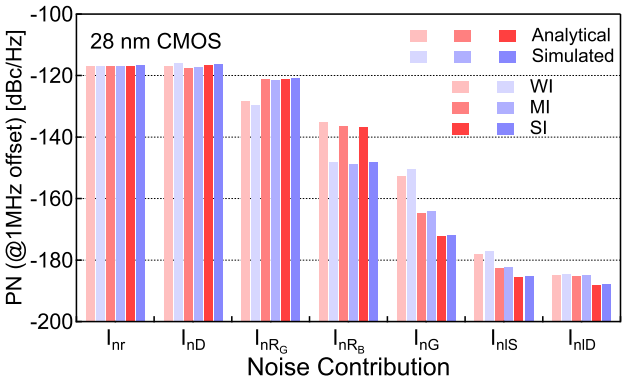

Fig. 4. Phase noise single contributions for 28 nm CMOS technology.

bias dependent [9]. A first explanation for this mismatch is that it is not possible to extract directly the value of n used in BSIM6, where it is bias dependent. The strong dependence on n has been verified with a simplified EKV transistor model in which this parameter is defined externally: the phase noise due to R_{B} changes strongly with n as expected. In order to have a good matching, n should be around 1.2 instead of the values given in Table I. Another reason can be related to the model used to describe the bulk resistance. A single resistance placed between the intrinsic and the extrinsic bulk nodes may not be suited for the purpose and a more complex model may be necessary.

Fig. 5 shows the total phase noise including all contributions as a function of IC. The match between the analytical and simulated results is good across all the values of IC for both technologies. The results coming from the analysis are in both cases slightly underestimating the simulated results (typically 0.5 dB), but remain a very good guess. Moreover, the most relevant contribution after the noise of the tank resistance and the channel thermal noise is the one of the gate resistance, whose value in SI is only 4-5 dB lower than the former ones in both technologies. The reason is that the gate resistance per unit finger has increased dramatically with respect to older technologies [1] [2] . In addition to that, this value increases even further for finger width below 1 µm. For these reasons, a large number of fingers with 2 µm or more per finger is recommended in order to minimize this contribution.

IV. Conclusion

The goal of this work is to understand to which extent an analytical small-signal approach can be suitable to analyze phase noise in class-B LC oscillators. For this, an extended small-signal model of the transistors has been used including all the noise sources, in order to derive the transfer function of each of them and to calculate their contribution to the total phase noise. The analytical expressions have been simplified and compared with the simulated results obtained from a LC oscillator with a 40 nm and a 28 nm CMOS technology.

This linear analysis is capable of predicting the $1/(\Delta\omega)^2$ phase noise contributions with good accuracy throughout all values of IC. The only noise source which shows a consistent

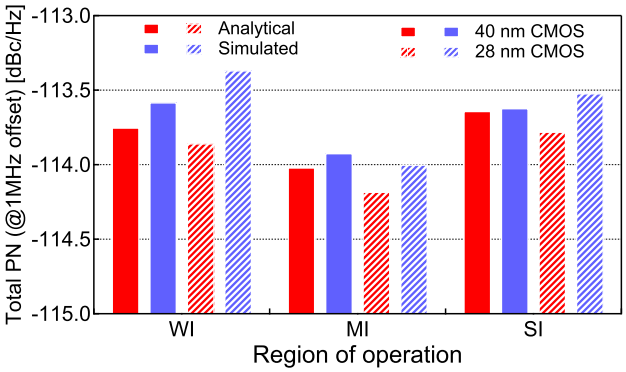

Fig. 5. Total phase noise vs. IC

discrepancy between the two results is the one associated to R_{B}. One possible cause is that the bulk resistance is not modeled accurately enough with a single resistance for this purpose and therefore requires further investigations.

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