

3D nano-acoustic Bragg reflectors for CMOS embedded NEMS

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Abstract—Integration of CMOS electronic circuits and electromechanical resonators has been pursued for a long time by many different research groups and even foundries. This would improve the overall performance of electromechanical oscillators and sensors. However, the postprocessing on the CMOS substrates that is necessary to attain this integration increases the production cost so much that it becomes not interesting in most cases. We present here a method of embedding a nano electromechanical resonator within a CMOS substrate by making use of the metal layers and intermetal dielectrics to build a phononic cage that stops most acoustic energy from being lost, and thus the resonator quality factor can reach values of more than 3000 at a frequency of 3.37 GHz, taking the particular case of a 65nm node. Our results show that the performance of the integrated resonator, both in terms of quality factor and electromechanical coupling will improve when moving to smaller nodes, thus setting the roadmap for future hybrid systems.

Index Terms — CMOS-microelectromechanical systems (MEMS), radio frequency (RF) MEMS, resonators, phononic crystals, Bragg gratings, Q-factor.

I. INTRODUCTION

CMOS has definitely changed our lives. The enormous impact that the integrated circuit and planar technology have had on society is indeed difficult to measure due to its huge reach. A key point to enable this impact has been the staggering technological development that has been performed in order to reach current nodes. Unfortunately, up to now, CMOS is used almost exclusively to produce electronic circuits.

The concept of “More than Moore” aims to bring extra functionalities to CMOS chips. Currently, this is typically done following a System in Package (SiP) approach, where the circuitry is fabricated on one substrate, the extra functionality is fabricated in a different substrate and they both are packaged together [1]. This approach is chosen over the more convenient System on Chip (SoC), where everything is fabricated on the same substrate, due to economic reasons.

However, the integration of functional non-circuit parts on a CMOS chip has been subject of extensive research over the years. Of particular interest has always been the integration with mechanical devices and/or resonators, the so-called MicroElectroMechanical Systems (MEMS) [2-8] or their Nano- counterpart (NEMS) [9-14]. This integration would allow for footprint reduction and performance increase in e.g. communications and sensing devices. One of the main challenges in integrating MEMS and in particular resonators has been and still is the definition and release of the mechanical structures.

The former point can be done within the CMOS process, maybe via some mild violation of the design rules, even though in some cases the resonator is deposited on top of the CMOS circuitry via post-processing. The second point is extremely important because whenever a device is not released from the underlying substrate, it can barely move, to the point that it does not really make sense to talk about a mechanical device. To put it in terms of resonator parameters, the major source of energy loss of a clamped device is acoustic losses through the support, effectively suppressing the quality factor of any vibrational mode [15]. Release has typically been done through a series of post-processing steps which are somehow incompatible with CMOS process steps, and might damage the circuitry in the process [16]. In any case, post-processing is always necessary increasing fabrication cost and decreasing yield.

In order to overcome the challenge of releasing the resonator, solidly mounted resonators (SMRs) were introduced [17]. In this case, the release step is avoided by placing underneath the resonator a set of alternating layers in a stack conforming an acoustic mirror that prevents, or minimizes, acoustic losses to the substrate. Bragg mirrors are very commonly used in optical waveguides and even within distributed Bragg reflector laser (DBR) [18]. In this case the concept is applied to acoustic energy instead of electromagnetic, and the result is that the stack of layers provides energy localization around the resonator.

This concept, though very powerful and with a lot of potential, does not remove the need of post-processing the CMOS wafer. Thus, SMRs have been further developed into embedded resonators in the CMOS layers. In this case, a purely hybrid CMOS-MEMS is developed, and the integration is optimized as no post-processing is required. This approach was first introduced by Weinstein et al. [19, 20], where they defined the resonator using front-end-of-line (FEOL) layer(s), i.e. using silicon as the structural material, in the same way that had been already demonstrated before using an in-house technology [21]. The release is partially bypassed by creating an acoustic bandgap using a phononic crystal (PnC) structure (acoustic metamaterial) [22] fabricated with the back-end-of line (BEOL) metals and dielectrics. On the other side, to reduce the amount of acoustic energy that leaks down to

the bottom substrate, only the buried oxide layer is present. These devices were successfully fabricated and exhibited a maximum quality factor of 252 at a frequency of almost 3 GHz [19], dropping from a quality factor close to 1000 according to simulations. Most of the acoustic energy loss is due to dissipation through the substrate, as the acoustic shielding is very poor. In fact, the vibrational mode that can be seen in the reported cases is a complex shear stress mode. This is very different from the modes that were observed at the single device level (no CMOS integration), which directly affects the electromechanical coupling of the resonator.

Here we introduce an embedded CMOS resonator where the resonant cavity, drive and sense regions as well as the 3D PnCs are built in the BEOL layers as schematically shown in Figure 1. We show that this configuration of the device allows for better localization of energy and we study the metal layer for which acoustic isolation is maximized. We present fully 3D simulations to most accurately describe the 3D acoustic cage around our resonator. A particular implementation is studied using parameters of a typical 65 nm node technology with 7+2 metals. Finally, we discuss on the scalability of this technique.

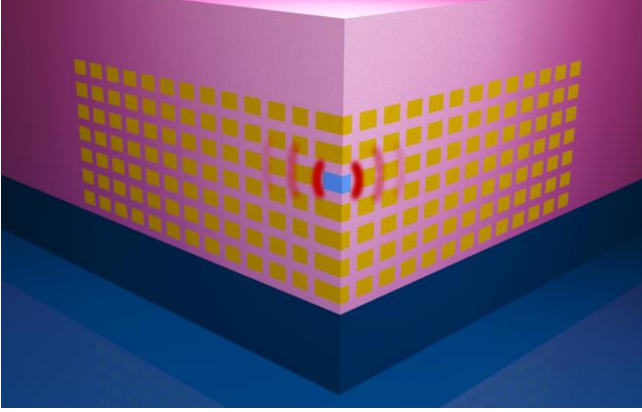


Figure 1: Schematic of a 3D acoustic cage with the embedded metal resonator and a phononic crystal for acoustic confinement around it. The schematic only shows one quarter of the whole system, which actually correspond to the simulated structure to save computing time.

oxide as the inter metal dielectric [24].

The position, width and efficiency of the bandgap are dependent on dimensions, acoustic impedance and number of the repeating unit cells. We define a unit cell as the minimum form of composite structure that repeats within the region of space that defines the PnC. In our case, for example, each unit cell contains a metal region surrounded by a dielectric (see Figure 2). The band structure is found by simulating the unit cell under consideration using finite element method in COMSOL Multiphysics. The Bloch-Floquet periodicity condition is applied to the edges of the cells in Figure 2 (a) and (c) in order to emulate an infinite structure, where a is the length of the unit cell, \vec{u} is the x -displacement vector and k is the wavenumber.

$$\vec{u}(x) = e^{ikx}\vec{u}(x + a) \quad (1)$$

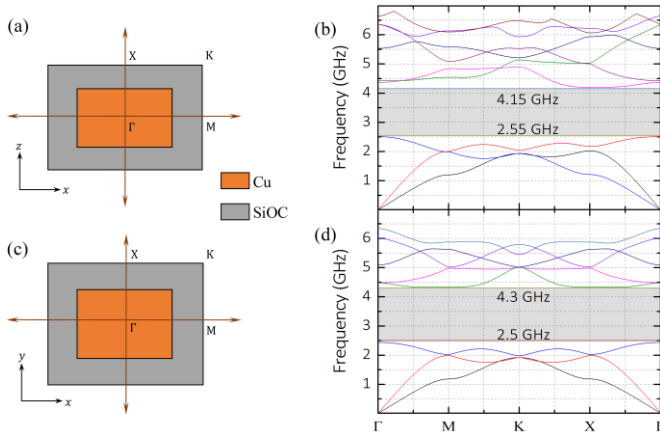


Figure 2: (a) Representation of unit cell along with direction of reduced wave vectors in the 2D cross section view. (b) Band Structure indicating bandgap of the unit cell in (a). Frequency is plotted against the reduced wave vector path Γ -M-K-X- Γ (c) Unit cell of PnC in the top view of 65nm CMOS layout (d) Band Structure indicating bandgap of PnC shown in (c). Frequency is plotted against the reduced wave vector path Γ -M-K-X- Γ

II. PHONONIC CRYSTAL

Phononic crystals are periodic structures designed such that the ensemble (metamaterial) shows a collective acoustic behavior that is different from either of the materials involved in the fabrication. Of particular interest for this paper, one can create phononic bandgaps, i.e. bands of frequencies for which acoustic conduction is not possible, no matter the type or direction of wave propagation. These bands are obtained due to the difference in densities and elastic properties (acoustic impedances) of the materials used in the PnC [23].

In the case of embedded resonators in CMOS, the particular choice of materials will depend on the node that is chosen for the fabrication. As said above, it will be the metal and insulator in the BEOL layers. As a particular example, in the case of CMOS 65nm technology, this means Cu as a metal and low- κ porous

By applying Eq. (1) in both x and z directions, the eigen frequencies of the ‘infinite’ system are found as a function of k along the wave vector directions Γ -M-K-X- Γ . The unit cell in Figure 2(a) represents the reflector pair as seen in the cross section. The particular dimensions are chosen according to the design rules of the CMOS technology, as will be detailed later. A bandgap between 2.55 GHz and 4.15 GHz is achieved for the 2D simulation of the cross section ($x - z$ plane). Similarly, the unit cell in Figure 2(c) is as seen from the top view. In this case, a larger bandgap from 2.5 GHz to 4.3 GHz is obtained. By designing the resonator in the center of the bandgap of the PnCs, a high-Q bulk acoustic resonator can be achieved.

III. PHONONIC CRYSTAL DESIGN

We describe above the concept of PnCs and how we perform simulations to observe the bandgap that is generated by an infinite repetition of unit lattices. However, there are several constraints that stem from the use of CMOS technology: in plane limitations include a minimum size, a minimum lateral step size and a minimum spacing; whereas the vertical dimensions (layer thickness) are completely fixed by each technology, no flexibility.

The way we design our crystals starts from this latter point, which is a “hard” constraint. In order to maximize the reflection of the reflectors in vertical, we take a simplified case and use the theory of 1D acoustic Bragg Mirrors, derived from the optical concept of Bragg’s law for X-ray diffraction[25]. It is well known that the optimal effective acoustic length of each layer forming the reflector pair should be matched to $\lambda/4$ of the required wavelength, in order to be confined for maximum efficiency. However, since thicknesses of the metal and dielectric layers are fixed within a given node, it is not possible to match the condition just described ($\lambda/4$ condition). Instead, we choose to match the effective path length of the *reflector pair* to $\lambda/2$. Thus, if we take n as the ratio of longitudinal speed of sound in the inter metal dielectric (IMD) to that in the metal (see Table 1), the relation between thickness and wavelength are given by Eq. (2).

$$t_{\text{metal}} + \frac{t_{\text{dielectric}}}{n} = \frac{\lambda}{2} \quad (2)$$

By calculating λ from Eq. (2), and using the speed of sound of both materials (Table 1), it is possible now to determine the lateral dimensions for the horizontal (in plane) reflectors, which can be matched to the $\lambda/4$ condition to attain maximum in-plane reflectivity. This can in general be done because the restrictions for lateral dimensions still allow enough flexibility. Using these design rules, the unit cells as shown in Figure 2 are constructed. In addition, considering that the resonator material is the metal, to allow for solid-gap electrostatic transduction [26], the frequency of the resonator is also fixed, which indeed coincides with the center of the bandgaps shown in Figure 2, as expected.

One of the major challenges is to find the actual material properties for the metal and insulator materials. The metal choice for the majority of CMOS nodes below 65 nm is Cu, which is relatively easy to find information for in the literature. On the other hand, below 90 nm nodes, it is known that the inter metal dielectric is not silicon dioxide anymore but a low- κ oxide [24]. In Table 1 we gather the relevant material properties for the metal and inter metal dielectric layers. In the latter case, the properties are estimated using the correlation between κ , porosity and mechanical properties [24, 27]. Importantly, it is the material properties and the thickness of the layers which determines the frequency of operation of the mechanical resonator, which means that for each node a particular frequency would be associated to the optimized mechanical resonators.

Table 1: Material properties of metal and dielectrics in CMOS

	ρ (kg/m ³)	ν	E (GPa)	c (m/s)	Z (MRayls)
Cu	8960	0.34	120	4353	32
SiO₂	2200	0.17	70	5848	12.4
SiOC	1200	0.25	10	8367	3.5

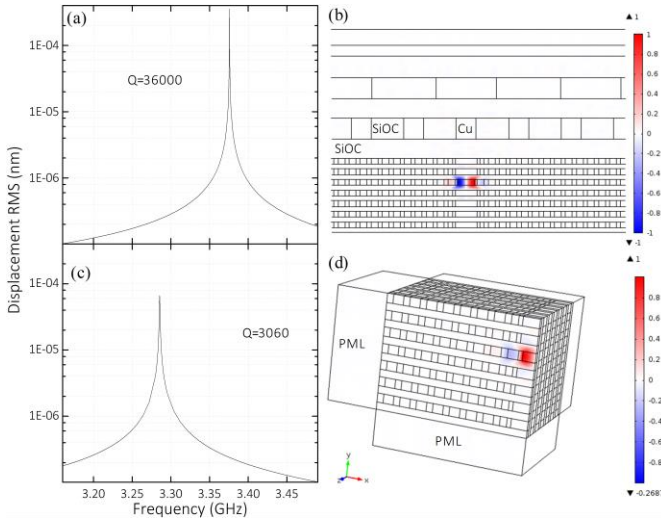


Figure 3: (a) Frequency response of the resonator using 2D cross section of 65nm CMOS technology and including Metal 8 (M8), Metal 9 (M9) and ALUCAP (AP) layers. The frequency of resonance is at 3.37GHz with a quality factor $Q=36000$. (b) Contour plot of normalized displacement in the 65nm 2D cross-section model at resonance from Figure 3(a). (c) Frequency response from 3D FEM Comsol simulation of the resonator with its resonant frequency at 3.29 GHz. The resonant frequency from 2D and 3D simulation is different due to the different mass loading. (d) 3D quarter symmetric contour plot of normalized displacement at resonance.

The finite reflectors simulation is performed gradually, starting by 2D and following by 3D simulations. Figure 3 shows one example of each. The 2D simulations do not provide the full information but they are useful as the computational time is reduced one order of magnitude smaller than for the 3D ones. Our model consists of the metal resonator, lateral capacitors and a phononic cage around them. Importantly, we include both the silicon substrate as a perfectly matching layer (PML), i.e. a region of space

IV. FINITE REFLECTORS

Once the existence of a bandgap in a theoretically infinite lattice (Figure 2) is demonstrated, it is necessary to perform simulations to test the actual efficiency of a finite number of reflectors. In these finite simulations, the resonator is a bulk acoustic resonator made of copper designed to resonate at the frequency calculated with the protocol detailed in the previous paragraph. In our particular case, this frequency is 3.29 GHz, which corresponds to a resonator size of λ along the x -direction. In our implementation, we violate the $\lambda/4$ condition on the very first insulating gap after the metallic body of the resonator. As transduction of the motion is performed through electrostatic coupling, electromechanical coupling (k_t^2) is maximized when that first insulating gap is as small as possible [26].

from which no energy is recovered: all energy that arrives is dissipated. PMLs are also placed in the lateral limits of the simulated structure, i.e. where the PnC finishes. In addition, we also place on top the final metallic and insulating layers for the last two metal levels, which have different thickness and critical dimensions, according to the design rules of the technology. In fact, design rules do not allow the Metal 8 (M8)-ALUCAP (AP) layers to be set to $\lambda/4$ of the propagating waves, unlike the other metal layers. Thus, we choose the width and pitch to be odd multiples of $\lambda/4$.

The resonator is placed in the M5 metal layer of the layout in order to achieve the best acoustic confinement. The optimum position can be found after studying the quality factor of the resonator placed in the different layers, and it can definitely be different for different technology nodes. In this configuration the acoustic energy lost to the substrate is minimized by 4 pairs of reflector layers at the same time that the perturbation due to Metal 8 (M8) to ALUCAP layers (AP) are minimized by the shielding effect due to Metal 6 (M6) and Metal 7 (M7) layers. Lateral confinement of energy is achieved by shielding the resonator with 20 pairs of reflectors on each side of the horizontal plane, i.e. in the x - and in the z -directions.

Result of RMS (root mean squared) displacement of the resonator vibrational mode amplitude vs frequency is shown in Figure 3 both for a 2D and a 3D simulation. In the former case, simulating one of the cross sections of the device yields a quality factor of 36000 (Figure 3.a). Figure 3.b shows the contour plot of displacement to visually demonstrate the effectivity of the 2D PnCs. Similar values for Q and for the acoustic encasing can be found for either of the other two planes defining the system (the perpendicular cross section and the horizontal cut).

In the case of 3D simulations, a drastic decrease in the simulated Q is attained. This is believed to be a consequence of the appearance of new shear acoustic modes that are not present in 2D. As our phononic cage is designed to contain longitudinal modes (in the design protocol we only use longitudinal speed of sound), the cage is much less efficient to contain shear modes. However, we find that the final result it is still best when the phononic cage targets only longitudinal modes. The extracted quality factor from the simulations (Figure 3.c) is ~ 3000 , which means a reduction of one order of magnitude with respect to the 2D simulations. This shows the extreme importance of performing 3D simulations to have a better estimation of the behavior of the designed structures. This is in contrast with some previous works in the literature which have only performed 2D simulations [19, 28, 29]. Comparing Figure 3.d with Figure 3.b offers also a visual proof that the confinement in 3D is not as good as in the case of 2D.

V. PERFORMANCE AND SCALABILITY

As already stated above, a key factor affecting the efficiency of the PnC is the acoustic impedance mismatch between the materials used. Intuitively, one can see the reason behind it because the reflection coefficient (in a 1D case) is given by[20]:

$$R = \frac{Z_1 - Z_2}{Z_1 + Z_2}. \quad (3)$$

As shown in Table I, the acoustic impedance of Copper is 32 MRayls whereas that of the SiOC used in 65 nm nodes is 3.5 MRayls. If we compare this with the acoustic impedance of standard SiO₂, which is 12.4 MRayls, it indicates that the efficiency of the PnC would be worse using standard SiO₂.

In order to show this, we perform a Bloch-Floquet analysis on a unit cell of Cu/SiO₂ to find the band dispersion diagram. The results are as shown in Figure 4. Here, as the material

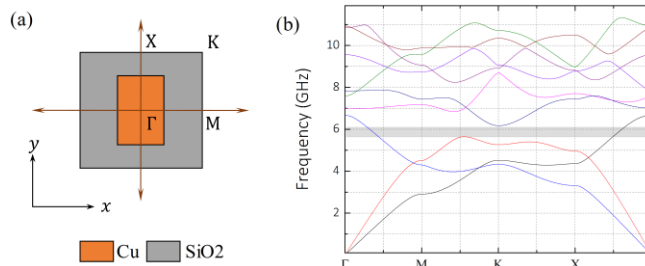


Figure 4: Band diagram of Cu/SiO₂ PnC

(a) Unit cell of PnC in the cross-section (b) Band Structure of Cu/SiO₂ PnC. There is no complete bandgap due to lower mismatch in acoustic impedance between Cu and SiO₂.

properties are different, the size of the unit cell and the central frequency are different than those showed in Figure 2. The results show that, even though the design should provide a bandgap around 6 GHz, due to lower reflectivity of the Cu/SiO₂ pair only a *pseudo* bandgap is obtained. This means that for a region of frequencies between 5.65GHz and 6.15GHz only acoustic modes with odd spatial symmetry are allowed to travel, and these are in principle orthogonal to our resonator movement, which presents an even spatial symmetry. Also the width of this pseudo bandgap is 5 times smaller than that of the bandgap found in Figure 2 for the Cu/SiOC pair. The bandgaps are 0.5 GHz and 1.8 GHz respectively.

A similar point has already been made before comparing performance within different CMOS nodes [19]. In this case, the comparison is done by only changing the material properties and not the critical dimensions associated with the node. The conclusions go in the same direction: larger impedance mismatch helps to create larger bandgaps.

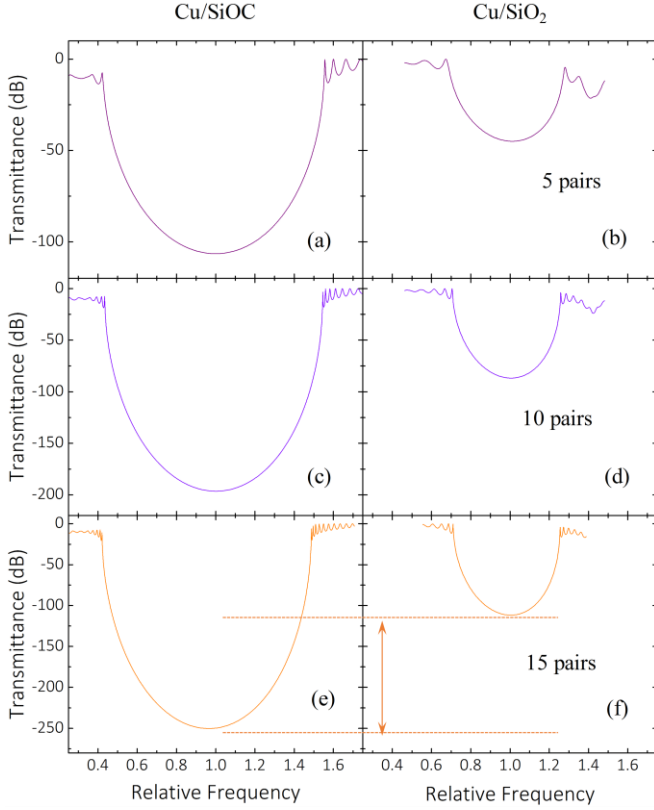


Figure 5: Comparison of efficiency of acoustic confinement for a finite number of reflectors. Distinction is made based on two pairs with the same number of reflectors but different materials (Cu/SiOC and Cu/SiO₂) and same material with different number of reflectors (5, 10 and 15 pairs)(a) & (b) Transmittance vs Normalized frequency of 5 pairs of acoustic reflectors made of Cu/SiOC and Cu/SiO₂ respectively.(c) & (d) 10 pairs of acoustic reflectors made of Cu/SiOC and Cu/SiO₂ respectively.(e) & (f) 15 pairs of acoustic reflectors made of Cu/SiOC and Cu/SiO₂ respectively.

There is a point, however, that might see a downside to the scaling down in the CMOS node. The fact that the permittivity reduces also means that, for the same solid gap between resonator and electrodes, the electromechanical coupling is smaller. Of course it is difficult to draw a very general conclusion from this point because as the node is reduced, the gap size between resonator and electrode also reduces. As we do not have access to all the design rules for the different foundries, we just make a note on this as something to be regarded.

VI. CONCLUSION

An embedded CMOS NEMS resonator has been designed and simulated attaining a resonant frequency of 3.3 GHz with a quality factor of slightly above 3000. In case of confirmation, this would mean an unprecedented Figure of Merit (FOM) $Q \cdot f = 10^{13}$ Hz for an unreleased resonator that would come right of the foundry. In contrast with the state of the art, we use the metallic layers within the CMOS as a structural material for the resonator. The reflectors array is composed by the metal and the inter metal dielectric. We have evaluated the electromechanical coupling of these devices, obtaining 0.015% for a total FOM of 0.46. The use of metal as the structural material for the resonator allows us to better encase the acoustic energy without reducing too much the electromechanical coupling unlike simulated and experimental demonstration in [28]. Further work involves experimental verification of this novel design and scaling down to even smaller nodes than 65 nm, where Q should be able to reach higher values and electromechanical coupling should be boosted.

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In addition, we also look into the efficiency of finite pairs of reflectors. In particular, we perform 1D simulations with both material combinations (Cu/SiO₂ and Cu/SiOC) for 5, 10 and 15 pairs of reflectors. One side of these arrays remains connected to the resonator and is excited. A harmonic analysis is performed, sweeping the frequency around its designed central bandgap frequency. The other edge is connected to a PML to absorb the acoustic radiation that manages to get through the reflectors. The transmittance coefficient (ratio between transmitted and input power) vs a normalized frequency is presented in Figure 5. We normalize the frequency to make the comparison easier. As described above, the central frequency is different for each pair of materials. It is rather evident that the efficiency of the reflector array is better in the case of Cu/SiOC. As a particular example, one can see that to reach the same level of isolation it is necessary to have three times more reflector pairs in the case of SiO₂. But then again, as the bandgap increases with the number of reflectors also for SiOC, we can see how it over performs SiO₂ across the spectrum.

Importantly, this sets the ground for future scalability of this concept. As we move to smaller and smaller CMOS technological nodes, the porous low- κ dielectric materials are even more porous and thus their acoustic impedance will be even smaller than in the case mentioned in Table 1 (for 65 nm node) [27]. This, together with the fact that critical lateral dimensions are smaller for each node, implies that the attainable quality factors for smaller nodes will potentially be higher. Not only this, but the larger the acoustic impedance mismatch, the more tolerance the design has with respect to variations in dimensions and/or material properties. This latter point is important because when reaching these small dimensions one can observe diverse size effects in the materials [30, 31].

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