Characterization of GigaRad Total Ionizing Dose and Annealing Effects on 28 nm Bulk MOSFETs

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***Abstract*—This paper investigates the radiation tolerance of 28 nm bulk *n*- and *p*MOSFETs up to 1 Grad of total ionizing dose (TID). The radiation effects on this commercial 28 nm bulk CMOS process demonstrate a strong geometry dependence as a result of the complex interplay of oxide and interface charge trapping relevant to the gate-related dielectrics and the shallow trench isolation. The narrowest/longest-channel devices have the most serious performance degradation. In addition, *n*MOSFETs present a limited on-current variation and a significant off-current increase, while *p*MOSFETs show a negligible off-current change and a substantial on-current degradation. The post-irradiation annealing annihilates or neutralizes oxide trapped positive charges and tends to partly recover the degraded device performance. To quantify the effects of TID and post-irradiation annealing, parameters including the threshold voltage, the free carrier mobility, the subthreshold swing, and the drain-induced barrier lowering are extracted.**

***Index Terms*—annealing, charge trapping, high-*k*, interface traps, oxide traps, spacer, STI, total ionizing dose, TID, 28 nm bulk MOSFETs.**

I. Introduction

TO extend the discovery potential at the forefront of research in high-energy physics (HEP), the Large Hadron Collider (LHC) at CERN will be upgraded for a tenfold increase in the integrated luminosity. The high-luminosity LHC (HL-LHC) is expected to experience an unprecedented radiation level up to 1 Grad (10 MGy) of total ionizing dose (TID) and $10^{16}\mathrm{neutrons/cm^2}$ of hadron fluence over ten years of operation. Hence, the experimental equipments need highly improved radiation-tolerant tracking systems with higher bandwidth and more radiation-tolerant front-end (FE) electronics [1], [2]. The aggressive down-scaling of deep-submicron CMOS technologies brings analog and mixed-signal circuit designers the benefits of a higher operation speed and an extended circuit functionality [3]. Furthermore, the gate dielectric with ultra-scaled silicon dioxide (SiO_2) demonstrates a higher radiation tolerance and relevant CMOS technologies are promising for radiation-tolerant applications [4].

Nonetheless, since the device dimensions shrank into 45 nm technology node and beyond, hafnium oxide (HfO_2) has been increasingly used for a higher physical oxide thickness to resolve the crucial gate direct tunneling issue [5]. However, a physically thicker gate dielectric degrades the radiation tolerance improvement of the aggressive gate-oxide scaling in terms of oxide charge trapping. Considering also the fact that the interface charge trapping relies on the interface quality instead of the oxide thickness, efforts are still needed for investigating the radiation response of the HfO_2-based material system [6]–[8]. On the other hand, it is reported in [9], [10] that the thick spacers severely affect 65 nm short-channel MOSFETs. Especially, the irradiated short-channel *p*MOSFETs almost degrade to the point of not having any on-current after 1 Grad. Additionally, the shallow trench isolation (STI) oxide is still in the order of 100 nm. The relevant charge buildup imposes strong effects on deep-submicron MOSFETs [11]–[13]. One of the main phenomena is the parasitic sidewall leakage current. Concerning the gate-related dielectrics and the thick STI oxide, it is still of importance to investigate TID effects on ultra-scaled MOSFETs for selecting the most appropriate candidates for radiation-tolerant circuits in the HL-LHC.

This paper studies DC characteristics of 28 nm bulk MOSFETs up to 1 Grad that is the foreseen radiation level in the innermost detectors of the HL-LHC. We also investigate the electrical evolution of the irradiated devices during annealing. Various sizes of individual MOSFETs are explored for comprehending the dominant mechanisms of TID effects. The results are also helpful for circuit designers to better choose the suitable sizes of MOSFETs for their radiation-tolerant applications. Extending our previous work on *n*MOSFETs [14], [15], this paper includes a detailed analysis of TID and annealing effects on important parameters of 28 nm bulk *n*- and *p*MOSFETs. The main mechanism of TID effects on a MOSFET is introduced in Section II. Test structures and the measurement protocol is described in Section III. Then in Section IV, we discuss TID and annealing effects on key device parameters, including the threshold voltage, the free carrier mobility, the subthreshold swing, and the drain-induced barrier lowering. The conclusion

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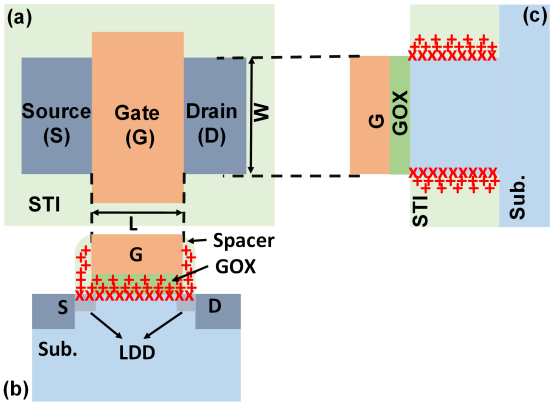

Fig. 1. (a) Top-view of a general MOSFET; (b) cross section along the length of the MOSFET; (c) cross section along the width of the MOSFET. "+" indicates oxide trapped charges (Q_{ot}) and "×" stands for interface charged traps (Q_{it}).

comes in Section V.

II. Basic Physical Processes of TID Effects on a MOSFET

When a MOSFET is exposed to high-energy ionizing radiation, electron-hole pairs are produced by the absorbed energy in oxides [16], [17]. Depending on the magnitude of the electric field and the energy of the incident radiation, some of electron-hole pairs undergo recombination immediately. The remaining electrons are swept out of the oxides toward the corresponding electrodes within picoseconds or so. Through a hopping transport mechanism, the remaining holes move through the localized shallow trap sites arising from the disorder of the oxides [18]. This distorts the local potential field of the oxide lattice and tends to confine a fraction of the transporting holes into the relatively deep hole traps (e.g., oxygen vacancies, oxygen interstitials) within the oxide bulk. Oxide trapped charges (Q_{ot}), labeled by "+" in Fig. 1, are positive for both *n*- and *p*MOSFETs. In addition, the holes remaining in the oxide volume form protons (H^+) via reacting with hydrogen-contained oxide defects [19]. The protons moving to the Si/oxide interfaces break the hydrogen-passivated dangling bonds. This generates electrically active and amphoteric interface defects. Depending on the midgap energy level, interface charged traps (Q_{it}), labeled by "×" in Fig. 1, are negative in *n*MOSFETs and positive in *p*MOSFETs [20].

Fig. 1b is the cross section along the length of a MOSFET and illustrates the charge trapping related to gate oxide and spacers. Fig. 1c shows the cross section along the width of the MOSFET and presents the charge trapping related to the STI. The charge trapping from both the gate-related dielectrics and the thick isolation oxide influences the device behaviors. In particular, TID effects induce several types of performance degradation, including a threshold voltage shift, a free carrier mobility reduction, a subthreshold swing degradation, and a radiation-modified drain-induced barrier lowering.

TABLE I
Device-under-test (DUT) list

Dimension	DUT1	DUT2	DUT3	DUT4	DUT5
Width (W)	3 µm	1 µm	1 µm	1 µm	300 nm
Length (L)	30 nm	30 nm	60 nm	90 nm	30 nm
W/L	100	33.3	16.7	11.1	10
Dimension	**DUT6**	**DUT7**	**DUT8**	**DUT9**	**DUT10**
Width (W)	100 nm	3 µm	400 nm	200 nm	100 nm
Length (L)	30 nm	1 µm	1 µm	1 µm	1 µm
W/L	3.3	3	0.4	0.2	0.1

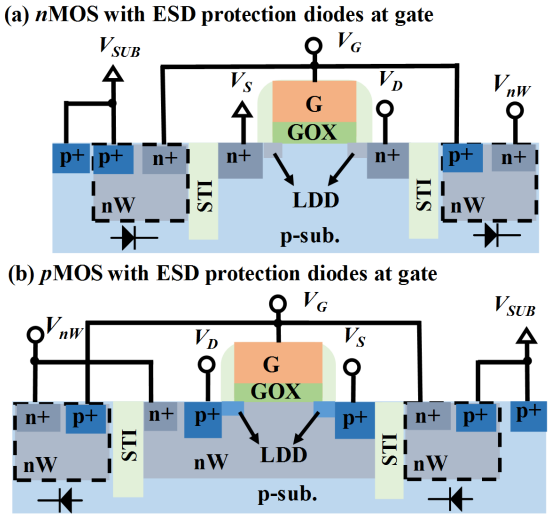

Fig. 2. Cross sections of *n*- (a) and *p*MOSFETs (b) with two diodes for each as the electrostatic discharge (ESD) protection at the gate terminal. The regions with dashed lines form the ESD protection diodes.

III. Experimental Details

A. Test structures

Test chips were fabricated with a commercial 28 nm bulk CMOS process [14], [15]. This work studies *n* and *p* types of standard V_T MOSFETs separately with two chips. Each chip has ten devices-under-test (DUTs) of the same type, which feature widths ranging from 3 µm to 100 nm and lengths from 1 µm to 30 nm, as listed in Tab. I. Each DUT has one sample that was tested comprehensively. Each MOSFET has two diodes connected to the gate terminal as the electrostatic discharge (ESD) protection, as shown in Fig. 2. Field-oxide FETs (FOXFETs) are often used for investigating TID effects on the thick STI oxide. Enclosed-layout transistors (ELTs) are often applied for isolating the effects on the STI from the gate-related dielectrics. However, the strict design rules of this commercial 28 nm bulk CMOS process exclude such special structures.

B. Measurement protocol

The irradiation was conducted at CERN's in-house 10 keV X-ray irradiation system (Seifert RP149). It has a customized probe card with two columns of 16 probe tips installed at a semi-automatic 8-inch wafer prober station (Karl-Suss PA200). Through a switching matrix (Keithley 707), two voltage supplies provided the bias for all DUTs during irradiation

and annealing. The terminals labeled in Fig. 2 were biased with $V_G = V_D = V_{nW} = 1.1\,\text{V}$, $V_S = V_{SUB} = 0$ for *n*MOSFETs and $V_G = V_D = V_{SUB} = 0$, $V_S = V_{nW} = 1.1\,\text{V}$ for *p*MOSFETs. The temperature-controlled chuck equipped with the irradiation system allows a temperature ranging from −50 °C to 200 °C. At a dose rate of 8.82 Mrad/h(SiO_2), the chips were irradiated at room temperature (25 °C) up to 1 Grad with steps of 0, 10, 50, 140, 340, 540, 740, 940, 963, and 1000 Mrad. To study the post-irradiation annealing effects, the irradiated *n*MOSFETs were kept at the same temperature (25 °C) with the same bias condition for 450 hours. To speed up the annealing process, *p*MOSFETs were biased at an elevated temperature (100 °C) for 16 hours. It should be mentioned that with our bias conditions, devices were conducting a high drain current during irradiation. To differentiate the radiation damage from the stress effects, we carried out additional stress tests at the same bias conditions for a comparable time but without irradiation.

Static electrical measurements were performed with the semiconductor parameter analyzer HP4145/55 through the switching matrix at room temperature during irradiation and at the annealing temperature after irradiation. A large amount of measurements were conducted to investigate TID effects on all regions of operation. Transfer characteristics were measured from linear ($|V_{DS}| = 0.01\,\text{V}$) to saturation ($|V_{DS}| = 1.1\,\text{V}$) by sweeping the gate voltage (V_G) from −0.2 V to 1.1 V. The output characteristics were measured from depletion region ($|V_{GS}| = 0.1\,\text{V}$) to strong inversion ($|V_{GS}| = 1.1\,\text{V}$) by sweeping the drain voltage (V_D) from 0 to 1.1 V. Since the radiation damage anneals with time [21], a voltage step of 25 mV was chosen as a suitable compromise between limiting the measurement duration and providing a sufficient measurement resolution. In this paper, the on-current, the threshold voltage, the free carrier mobility, the off-current, and the subthreshold swing are extracted from the measured drain current (I_D) versus V_G curves in the saturation operation. The drain-induced barrier lowering (DIBL) parameter is obtained from the I_D-V_G curves with 0.01 V and 1.1 V of $|V_{DS}|$. *p*DUT10 demonstrates an unexpected abrupt increase in the off-current around 140 Mrad that is not seen for other DUTs. Due to the fact that its source and substrate are connected with other DUTs and its gate is coupled with the ESD protection diodes, we are not able to obtain the intrinsic currents from gate, source and substrate. Therefore, it is not straightforward to clearly identify the source of this off-current increase. In order not to mislead the reader by the suspect behavior of *p*DUT10, we exclude it from our discussion. Note that *n*MOSFETs lost the bias for hours between 540 and 740 Mrad. *p*MOSFETs were not biased for hours between 940 and 963 Mrad. This bias loss explains the discontinuous evolution of the extracted parameters.

IV. Results and discussions

A. Bias-dependence of TID effects

TID effects strongly depend on the applied electric field. It is reported in [9] that for a commercial 65 nm bulk CMOS process, the real worst-bias cases are $V_{GB} = V_{DS} = V_{DD}$ for *n*MOSFETs and $V_{GB} = V_{DS} = -V_{DD}$ for *p*MOSFETs that are different from the historically worst-bias cases ($V_{GB} = 1.1\,\text{V}$, $V_{DS} = 0$ for *n*MOSFETs and $V_{GB} = V_{DS} = 0$ for *p*MOSFETs [22]). We compare the effects of these two bias conditions on 28 nm bulk *n*- and *p*MOSFETs. No big difference is seen between them and the slight difference is actually within the chip variability (∼6%). It is not straightforward to decide which are the worst-bias cases for this 28 nm bulk CMOS process. However, in most analog circuits and particularly the analog front-end electronics used in HEP, the transistors are biased in saturation with a non-zero V_{DS} except the switches working with a zero V_{DS}. In order to reproduce as close as possible the realistic bias conditions for analog circuits, we therefore chose to bias the devices with $V_{GB} = V_{DS} = 1.1\,\text{V}$ for *n*MOSFETs and $V_{GB} = V_{DS} = -1.1\,\text{V}$ for *p*MOSFETs.

Since the devices conducted a high drain current during irradiation with our bias conditions, it is of importance to see how much of the performance degradation comes from TID effects. For *n*MOSFETs, the stress without irradiation does not cause any performance degradation, leaving the whole range of I_D-V_G curves unaffected. Therefore, the performance degradation of the irradiated *n*MOSFETs is attributed only to the radiation effects. However, *p*MOSFETs demonstrate some stress-induced shift in the threshold voltage. The ratio of the stress effects to the radiation damage depends on the transistor dimension. However, except the largest *p*MOSFETs (3 µm/1 µm) for which the damage is mostly due to the stress, the degradation of all the others is dominated by TID effects (70%-95%). Additionally, there might be self-heating during irradiation due to the high conducting current. However, between the end of the irradiation and the start of the first DC measurement, the time (a couple of seconds) should be sufficient for the chips to cool down to the room temperature [23]. Since the self-heating normally appears at the high current level, we believe that the important parameters extracted from the low current region of the measured I_D-V_G curves, such as the threshold voltage, the free carrier mobility, the subthreshold swing, and the off-current, are not affected by self-heating. Nevertheless, we are mostly interested in the realistic bias conditions that are close to the real circuit operating regime, even though there might be self-heating affecting the on-current.

Section III-B mentioned the bias loss between 540 and 740 Mrad for *n*MOSFETs and 940 and 963 Mrad for *p*MOSFETs that causes the parameter discontinuities. Electron tunneling from the oxides to the substrate is expected to be the underlying mechanism. At a positive gate-to-bulk bias, electrons tunnel from the substrate to electron traps in oxides and neutralize the associated holes that are mostly trapped at near-interfacial oxide traps (i.e., border traps). Removing the bias, these electrons tunnel back to the substrate and lead to a higher amount of oxide trapped charges. This decreases the threshold voltage, increases the on-current, and degrades the subthreshold swing. The negative threshold voltage shift also leads to a higher off-current for short-channel *n*MOSFETs. Long-channel *n*MOSFETs present a lower off-current, which could be explained by the compensation of the interface charge trapping. The bias loss between 940 and 963 Mrad for *p*MOSFETs explains the slight fluctuation of the extracted parameters for the last two TID steps.

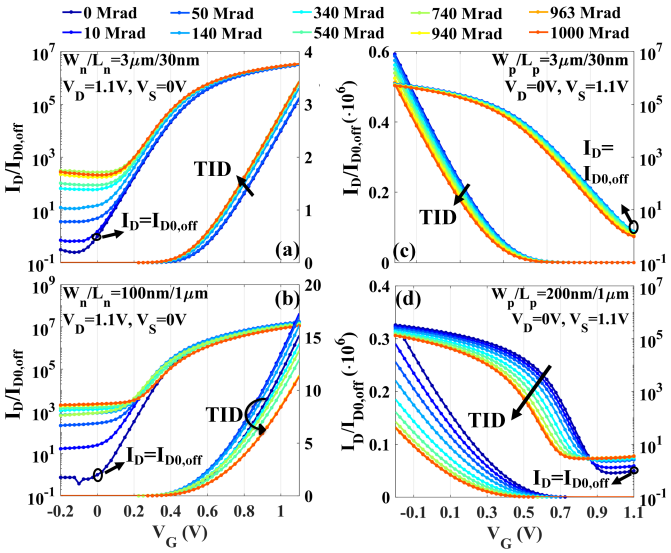

Fig. 3. Transfer characteristics of both n (ab) and p (cd) types of MOSFETs in saturation mode ($|V_{DS}| = 1.1$ V) with respect to TID. (ac) are for DUT1 with the largest W/L ratio (3 µm/30 nm). (b) is for nDUT10 with the smallest W/L ratio (100 nm/1 µm) and (d) is for pDUT9 with 100 nm/1 µm. $I_{D0,\,off}$ is the off-current ($V_{GS} = 0$) before irradiation.

B. TID effects on transfer characteristics

Fig. 3 plots the normalized off-current of nDUT1, nDUT10, pDUT1, and pDUT9 with respect to TID. The on-current ($I_{D,on}$) is defined at $|V_{GS}| = 1.1$ V, and the off-current ($I_{D,off}$) at $V_{GS} = 0$. nDUT1 has a negative threshold voltage shift and a monotonic on-current increase, as shown in Fig. 3a. Nevertheless, as seen in Fig. 3b, the threshold voltage of nDUT10 first decreases and then increases, leading to the corresponding on-current evolution. Both irradiated nDUT1 and nDUT10 have a significant off-current increase. In contrast, the threshold voltage of both pDUT1 (Fig. 3c) and pDUT9 (Fig. 3d) decreases with TID, leading to a continuous on-current loss. Note that when the threshold voltage of a pMOSFET decreases, it becomes more negative and its absolute value increases. The off-current of both pDUT1 and pDUT9 is not sensitive to TID and has a slight off-current change.

C. On-current

The relative on-current variation is plotted as a function of TID in Fig. 4. All nMOSFETs present an on-current improvement at a lower TID (~10 Mrad) in Fig. 4a. Then for nDUT1-5, the on-current increase continues until reaching a ~15% increase. However, the on-current of nDUT6-10 starts to decrease at a higher TID. nDUT10 with the smallest W/L ratio (100 nm/1 µm) evidences as the most dynamic case with a maximum on-current loss of ~25%. Fig. 4b shows that pMOSFETs are grouped into two distinct categories: pDUT1-6 and pDUT7-9. In each group, the narrower the channel, the higher the on-current loss. Eventually, most of pMOSFETs show a less than 30% degradation in the on-current. Narrow-channel pMOSFETs with a smaller W/L (pDUT6 and pDUT8-9) present a more than 50% on-current loss. Nevertheless, these results are much better compared to the commercial 65 nm bulk CMOS technology from the same foundry [9].

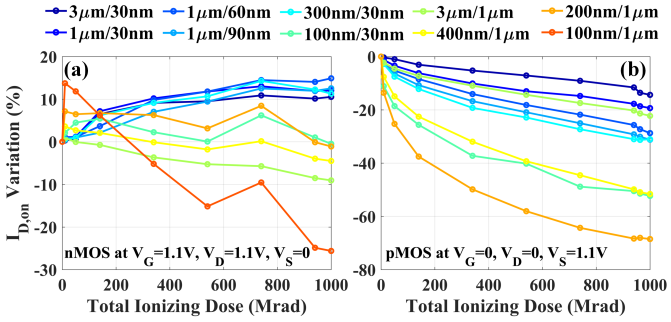

Fig. 4. TID-induced on-current ($I_{D,on}$) variation of both n (a) and p (b) types of MOSFETs in saturation mode ($|V_{DS}| = 1.1$ V). $I_{D,on}$ is obtained at $|V_{GS}| = 1.1$ V.

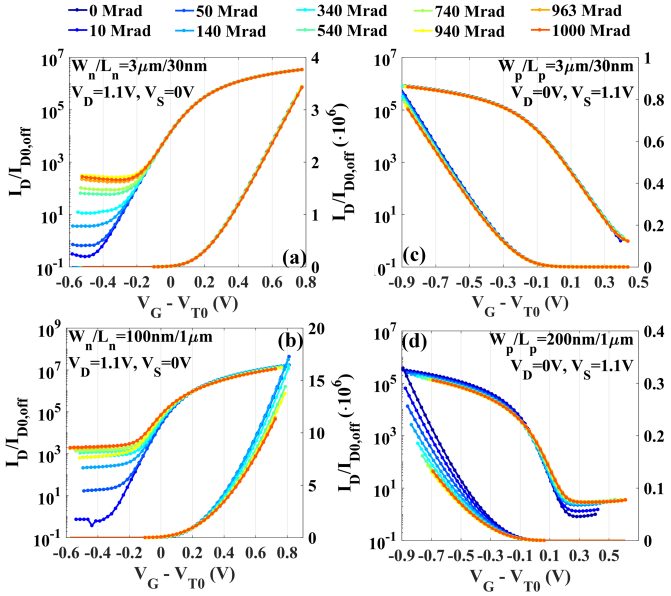

Fig. 5. Drain current (I_D) versus the overdrive voltage ($V_G - V_{T0}$) with respect to TID for both n (ab) and p (cd) types of MOSFETs in saturation mode ($|V_{DS}| = 1.1$ V).

Both the threshold voltage (V_{T0}) shift and the free carrier mobility (μ) reduction influence the on-current. To extract V_{T0} and μ, $\sqrt{I_D}$-V_G curves are extrapolated linearly at the maximum slope. The intercept at the V_G axis is defined as V_{T0}. The slope of the linear extrapolation provides insights into μ. We now plot I_D with respect to $V_G - V_{T0}$ in Fig. 5 to isolate the effects of the free carrier mobility reduction from the threshold voltage shift. It is seen in Fig. 5ac that for the widest/shortest-channel DUTs (3 µm/30 nm), the I_D versus $V_G - V_{T0}$ curves overlap in strong inversion, demonstrating that only the threshold voltage shift accounts for the on-current variation. For the narrowest/longest-channel DUTs, as shown in Fig. 5bd, the I_D versus $V_G - V_{T0}$ curves deviate in strong inversion, indicating the additional contribution of the mobility reduction to the on-current loss. We also suspect that for short-channel pMOSFETs, the positive charges trapped in the spacers reduce the effective doping of the LDD region and increase the resistance for the drain current. This might partly contribute to the significant on-current loss of pDUT6 (100 nm/30 nm). However, with our current measurements, we are not able to

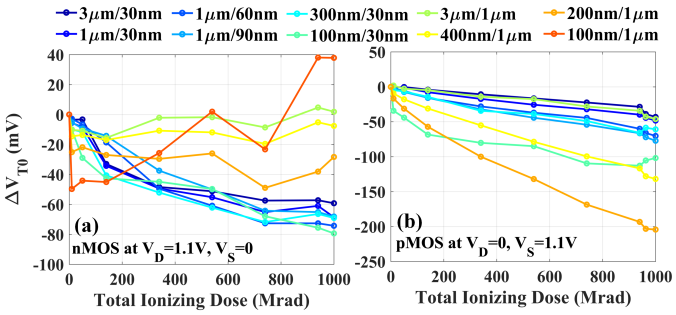

Fig. 6. TID-induced threshold voltage (V_{T0}) shift of both n (a) and p (b) types of MOSFETs in saturation mode ($|V_{DS}| = 1.1$ V).

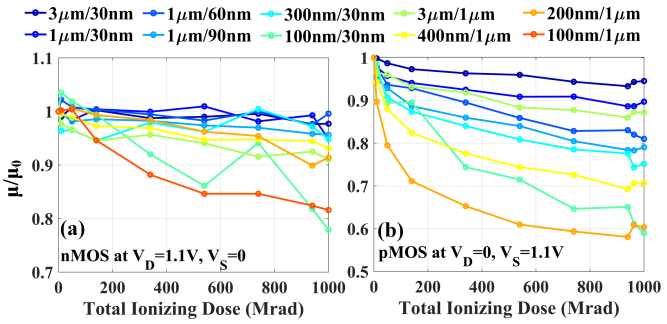

Fig. 7. TID-induced free carrier mobility (μ) reduction of both n (a) and p (b) types of MOSFETs in saturation mode ($|V_{DS}| = 1.1$ V). μ_0 is the free carrier mobility before irradiation.

isolate the effects of the spacers from the gate oxide. Further investigations are therefore needed to verify if this technology does undergo the effects of the charge buildup in the spacers.

1) Threshold voltage: Q_{ot} decreases the threshold voltage of both n- and pMOSFETs, whereas Q_{it} increases that of nMOSFETs and decreases that of pMOSFETs. For nMOSFETs, the counterbalance of Q_{ot} and Q_{it} leads to a limited influence on the switched-on region. Fig. 6a shows a less than 80 mV shift in the threshold voltage, corresponding to a less than 30% variation. This explains the limited on-current variation in Fig. 4a. It is also observed that at a lower TID, the threshold voltage decreases for all nMOSFETs, which is due to the initial oxide trapped charges. Then the threshold voltage of nDUT1-6 continues to decrease until 1 Grad. For nDUT7-10, Q_{it} starts at a certain TID to compensate the Q_{ot}-induced negative threshold voltage shift. Eventually, nDUT10 has an overall positive threshold voltage shift that is consistent with the net on-current decrease. Fig. 6b shows that even with the superposed effects of Q_{ot} and Q_{it}, most of pMOSFETs still have a threshold voltage shift of less than 80 mV. However, the threshold voltage of narrow-channel pMOSFETs with a smaller W/L ratio (pDUT6 and pDUT8-9) decreases by more than 100 mV that corresponds to their significant on-current loss. It should be mentioned that the threshold voltage variation for all pMOSFETs is within 30%. The significant effect on narrow-channel pMOSFETs is attributed to the charge trapping in the thick STI oxide, which modifies the electric field at the STI edges and prevents the inversion of the silicon channel [9], [11], [24].

2) Free carrier mobility: The radiation-induced mobility reduction demonstrates a strong dependence on the Coulomb scattering of the trapped charges at border traps [25] and interface traps [26]. Fig. 7a shows that wide/short-channel MOSFETs have a negligible mobility reduction, which indicates the radiation hardness of the interface of the gate oxide and the silicon channel. The significant negative threshold voltage shift in Fig. 6a actually indicates a large amount of trapped charges at border traps in nDUT6 and at interface traps in nDUT10, which contributes to their high mobility reduction. Compared to nMOSFETs, pMOSFETs demonstrate a higher mobility reduction, as seen in Fig. 7b. The mobility of pDUT6 and pDUT8-9 degrades more that is consistent with their significant on-current loss depicted in Fig. 4b. The highest mobility reduction in narrowest/longest-channel DUTs (nDUT10 and

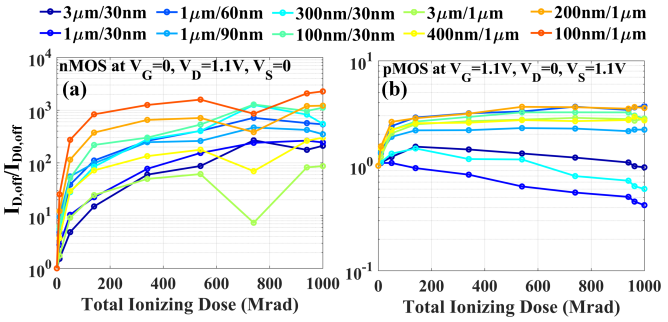

Fig. 8. TID-induced off-current ($I_{D,off}$) increase of both n (a) and p (b) types of MOSFETs in saturation mode ($|V_{DS}| = 1.1$ V). $I_{D,off}$ is obtained at $V_{GS} = 0$.

pDUT9) is clearly illustrated by the down-bending of the I_D-($V_G - V_{T0}$) curves in Fig. 5bd.

D. Off-current

The off-current normalized to pre-irradiation values is plotted as a function of TID in Fig. 8. Fig. 8a demonstrates a significant off-current increase by two to three orders of magnitude for nMOSFETs. It should be mentioned that different mechanisms are dominating the region around a zero V_{GS} for short- and long-channel nMOSFETs, as seen in Fig. 3a and Fig. 3b. The extracted off-current of short-channel nMOSFETs is still in the subthreshold region before irradiation. At a lower TID, trapped holes in the thick STI oxide deplete the channel along the STI edges. This connects the source/drain depletion regions and results in a surface punchthrough current [27]. At a higher TID, the positive charges trapped in the thick STI oxide enhances the drain-induced barrier lowering (DIBL) and further increases the off-current. The radiation-enhanced DIBL will be discussed in detail in Section IV-F.

For long-channel nMOSFETs, the dominant off-current contributor is the parasitic leakage current along the STI edges [11]. Trapped holes in the thick STI oxide could be strong enough to invert the adjacent p-type substrate and to form the n-channel. Thus two parasitic leakage paths forms even when the main transistor is switched off. This effect has a stronger influence on a narrow channel, as seen with the highest off-current increase for nDUT10. Furthermore, up to a certain TID, the off-current of long-channel nMOSFETs enters into a region less dependent on the gate voltage. It almost saturates up

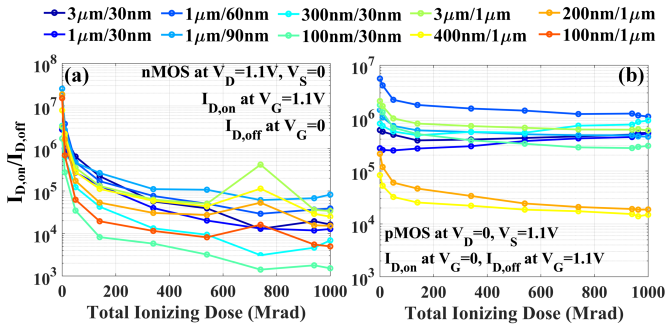

Fig. 9. TID-induced on/off-current ratio ($I_{D,on}/I_{D,off}$) degradation of both *n* (a) and *p* (b) types of MOSFETs in saturation mode ($|V_{DS}| = 1.1$ V).

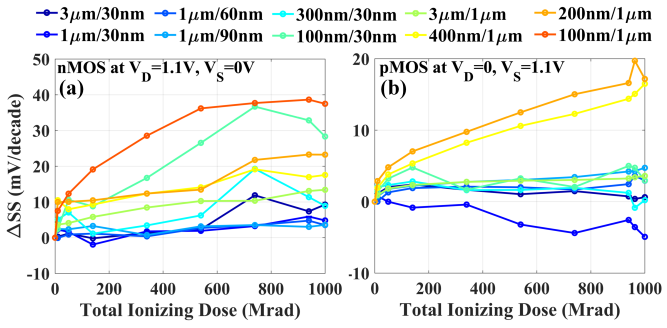

Fig. 10. TID-induced subthreshold swing (*SS*) degradation of both *n* (a) and *p* (b) types of MOSFETs in saturation mode ($|V_{DS}| = 1.1$ V).

to 340 Mrad that indicates the complete filling of the traps in the STI oxide or the compensation of the interface charge trapping from the STI. It should also be emphasized that it is more difficult to invert a highly doped silicon. Therefore, the non-uniform doping profile in nanoscale MOSFETs, including the increased channel doping concentration due to the scaling rule, the surface implantation for adjusting the threshold voltage, and the higher doping from the retrograde well and the halo pockets for suppressing short-channel effects, could be advantageous in terms of the radiation tolerance at the switch-off state [28], [29]. For all *n*MOSFETs, the radiation-induced charge buildup is not strong enough to influence the electrostatic potential in the middle of the channel. Therefore, as shown in Fig. 9a, there is still an on/off-current ratio of three orders of magnitude, leaving a sufficient margin for circuit design.

Compared to *n*MOSFETs, the switched-off region of *p*MOSFETs is much less susceptible to TID. The off-current changes only by a maximum factor of 3. The slight off-current increase might be from the peripheral drain to substrate junction leakage current. It is mostly contributed by the surface generation at the intersection of the depletion region and the STI sidewalls where a high density of interface traps are located [30]. Some of the short-channel *p*MOSFETs present a slight off-current decrease. This is due to the fact that short-channel *p*MOSFETs still work in the subthreshold region around a zero V_{GS}, as shown in Fig. 3c for *p*DUT1. The negative threshold voltage shift together with the radiation-suppressed DIBL (Section IV-F) leads to the off-current decrease. Owing to the negligible influence on the off-current, the irradiated *p*MOSFETs still demonstrate an on/off-current ratio of more than four orders of magnitude, as shown in Fig. 9b.

E. Subthreshold swing

Trapped charges at border traps and interface traps cut off part of the electric field lines from the gate electrode. This reduces the effective gate potential and the transistors could not be switched off effectively. Fig. 10 shows a less than 20 mV/dec increase in the subthreshold swing for most of *n*- and *p*MOSFETs. This confirms the radiation hardness of the interface of the gate oxide and the silicon channel. Two narrowest-channel *n*MOSFETs (*n*DUT6 and *n*DUT10) demonstrate a ~40 mV/dec subthreshold swing increase. Note that the higher increase in the off-current of *n*DUT6 and *n*DUT10 raises up the I_D-V_G curves and starts to mask the subthreshold region. This degrades the precision of the subthreshold swing extraction.

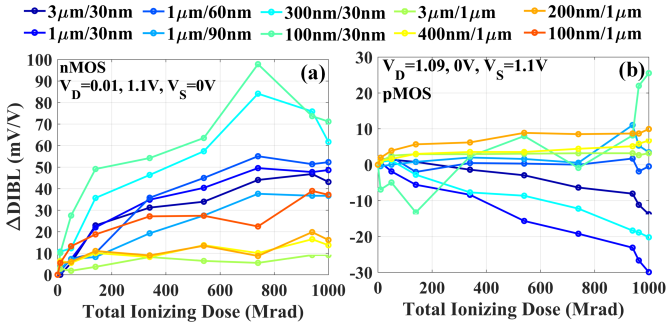

Fig. 11. TID-modified drain-induced barrier lowering (DIBL) of both *n* (a) and *p* (b) types of MOSFETs. The DIBL is extracted as $DIBL = -(V_{T0}^{|V_{DS}|=1.1\text{ V}} - V_{T0}^{|V_{DS}|=0.01\text{ V}})/(1.1V - 0.01V)$.

F. Drain-induced barrier lowering

The drain-induced barrier lowering (DIBL) represents one of the most fundamental short-channel effects in nanoscale MOSFETs. The STI-related charge trapping is among the most important DIBL factors [27]. In the proposed dipole theory [31], Q_{ot} in the thick STI oxide terminates the drain-to-gate fringing field at the switched-off state. This decreased drain-to-gate coupling in turn enhances the drain-to-source coupling. In addition, Q_{ot} in the thick STI oxide enhances the electric field along the STI edges. Thus the electric field lines in the center of the channel will be denser and the drain-to-source coupling will be further strengthened. Both enhance the DIBL of *n*MOSFETs, as shown in Fig. 11a.

As mentioned in Section IV-D, the STI-related charge trapping makes the parasitic depletion regions interact with the source/drain ones and forms a thicker depletion region in short-channel *n*MOSFETs. This will shorten the effective channel length near the corners of the STI and the gate oxide, adding another enhancing factor for the DIBL. If the width is narrow, trapped charges in the thick STI oxide even raise the nearby body potential in the main channel, which significantly lowers down the potential barriers with source and drain. This is shown in Fig. 11a: the narrower the channel, the more severe the radiation-enhanced DIBL.

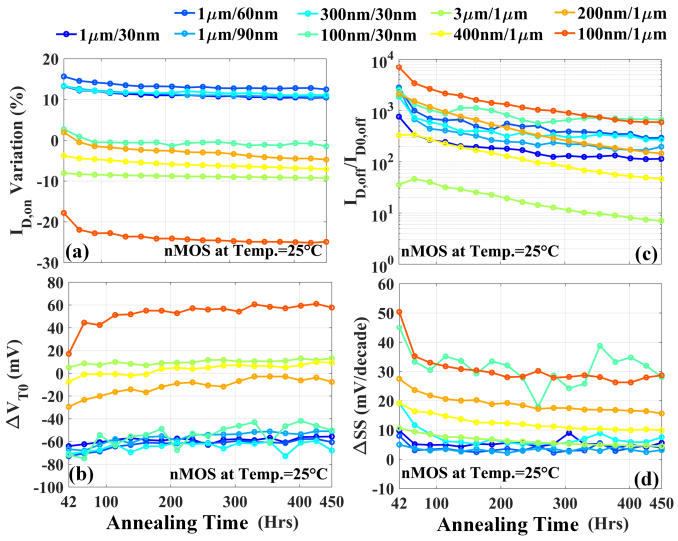

Fig. 12. Post-irradiation annealing effects on the on-current (I_{on}), the threshold voltage (V_{T0}), the off-current (I_{off}), and the subthreshold swing (SS) of nMOSFETs. There is no result for the widest/shortest-channel nMOSFET (3 µm/30 nm) due to the physical damage from moving and reconnecting the chip.

The radiation has a negligible influence on the DIBL of most of pMOSFETs, as seen in Fig. 11b. However, pDUT1-2 and pDUT5 demonstrate an radiation-suppressed DIBL. This could be explained by the proposed dipole theory. Both the trapped charges in the thick STI oxide and the image charges in the gate electrode are positive. This weakens the drain-to-source coupling and suppresses the DIBL [32]. Due to STI-related trapped charges, electrons accumulate around the corners of the gate oxide and the STI. This will lengthen the effective channel near the edges, which further decreases the DIBL of pDUT1-2 and pDUT5.

G. Post-irradiation annealing

The long-term post-irradiation annealing is believed to annihilate or neutralize the oxide trapped charges even at room temperature [33]. This annealing process can be accelerated by a stronger positive gate-to-bulk bias and a higher temperature [34]. It is reported that in some cases the interface-trap annealing can happen below 100 °C [35]. However, a higher temperature is generally required to anneal interface traps effectively [36].

Fig. 12 and Fig. 13a present the room temperature (25 °C) annealing effects on important parameters of nMOSFETs. The first measurement was taken after 42 hours of annealing. Since the room temperature is not high enough to anneal the interface traps, the observation gives more insights into the evolution of the oxide trapped charges. The threshold voltage of nMOSFETs increases due to the trapped-hole annealing, as observed in Fig. 12b. Fig. 13a demonstrates a negligible change in the free carrier mobility, which confirms no annealing evolution for radiation-induced interface traps. Therefore, the room temperature annealing decreases the on-current of nMOSFETs, as seen in Fig. 12a. The trapped-hole annealing also decreases the off-current significantly, as shown

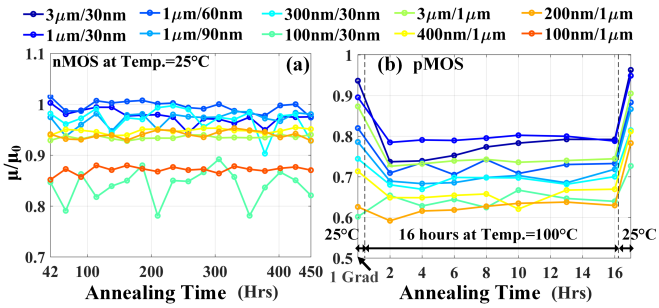

Fig. 13. Post-irradiation annealing effects on the free carrier mobility (μ) of n (a) and p (b) types of MOSFETs. In (b), the first measurement corresponds to 1 Grad at room temperature. The second is with respect to 2 hours of high temperature annealing. The last is a room temperature measurement after the high temperature annealing. The dashed lines indicate the changing of the temperature.

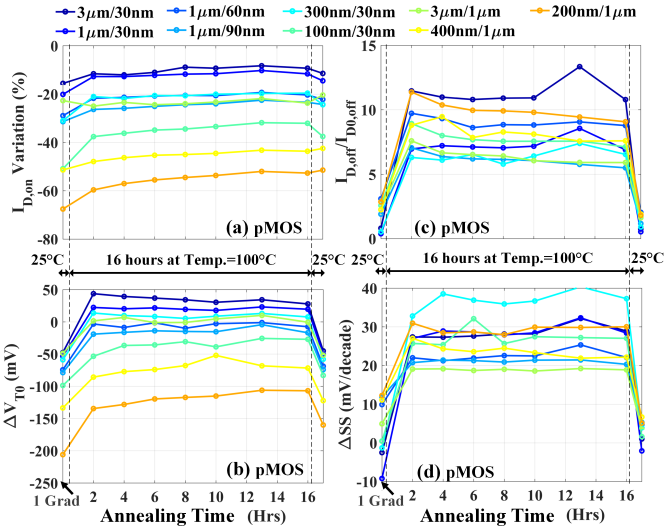

Fig. 14. Post-irradiation annealing effects on the on-current (I_{on}), the threshold voltage (V_{T0}), the off-current (I_{off}), and the subthreshold swing (SS) of pMOSFETs.

in Fig. 12c. An observable improvement in the subthreshold swing is seen in Fig. 12d, indicating the annealing of the trapped holes at border traps. The remaining subthreshold swing degradation for nDUT6 and nDUT8-10 could be attributed to the interface charged traps at the STI/channel edges.

Fig. 14 and Fig. 13b present the high temperature (100 °C) annealing effects on important parameters of pMOSFETs. The chip was annealed at 100 °C for 16 hours and then cooled down to 25 °C. The first measurement point corresponds to 1 Grad at room temperature. The second refers to 2 hours of high temperature annealing. The big differences between these two sets of measurement points include the effects of the temperature dependence that is demonstrated as a higher off-current, an increased threshold voltage, a degraded subthreshold swing and a reduced free carrier mobility. The on-current increase is due to the dominant effects of the positive threshold voltage shift over the free carrier mobility reduction. Since the subthreshold swing increase is less than 1.25 that is the temperature ratio of the first two measurements, the second measurement point also includes the effect of high

temperature annealing. In the following hours, the degraded performance of *p*MOSFETs is partly recovered. The threshold voltage (Fig. 14b) increases and the free carrier mobility improves slightly (Fig. 13b), which leads to an observable on-current increase (Fig. 14a). The differences between two room temperature measurements demonstrate the net performance improvements. It is observed that after 16 hours of high-temperature annealing, the threshold voltage increases by up to 40 mV, the mobility improves by up to 12%, and the on-current recovers by up to 20%. The off-current and the subthreshold swing almost reaches the original values.

V. Conclusion

The effects of total ionizing dose (TID) up to 1 Grad and post-irradiation annealing on 28 nm bulk *n*- and *p*MOSFETs are investigated. The counterbalance of interface and oxide charge trapping results in a limited influence on the switched-on region of the irradiated *n*MOSFETs, which demonstrate a less than 25% free carrier mobility reduction, a less than 80 mV threshold voltage shift and a less than 25% on-current loss. However, due to the STI-induced parasitic leakage paths and the radiation-enhanced DIBL, *n*MOSFETs present a two to three orders of magnitude increase in the off-current. In contrast, most of *p*MOSFETs have a negligible off-current change. Even with the superposed effects of interface and oxide charged traps, most of *p*MOSFETs still undergo a less than 30% performance degradation, which is much less compared to the 65 nm counterparts. Owing to the radiation-induced narrow channel effects, the narrowest/longest-channel *p*MOSFET presents the strongest susceptibility to TID with a 200 mV threshold voltage shift and a 40% free carrier mobility reduction as well as a 70% on-current loss. The limited subthreshold swing degradation indicates the strong radiation tolerance of the interface of the gate dielectric and the silicon channel.

Due to the complex interplay of the charge trapping relevant to the gate-related dielectrics and the STI, TID effects demonstrate a strong geometry dependence. This implies the importance of choosing the suitable sizes of transistors for radiation-tolerant circuit design. In addition, oxide trapped holes anneal with time, which leads to a significant off-current decrease in *n*MOSFETs and a substantial on-current recovery in *p*MOSFETs. Considering the long-term irradiation and annealing in realistic applications, the degradation might be mitigated.

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