In-Plane-Gate GaN Transistors for High-Power RF Applications

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***Abstract*—In-plane-gate field effect transistors (IPGFETs) offer an innovative device architecture in which the channel conductivity is modulated by the electric field from the two-dimensional electron gas (2DEG) in the two adjacent in-plane gates, isolated by etched trenches. The planar nature of the gate electrode yields a huge reduction in parasitic gate capacitance, which can lead to much higher frequency. Moreover, the fabrication process for these devices is extremely simple and with inherently self-aligned gates.**

Here, we combine for the first time the promising architecture of IPGFETs with the exceptional properties of III-Nitrides, such as large carrier density and breakdown field, to reveal their enormous potential for high-power RF devices. AlGaN/GaN IPGFETs demonstrated large drain current up to 1.4 A/mm and transconductance up to 665 mS/mm, which are respectively 9x- and 5x-larger than the best IPGFETs demonstrated in other semiconductors. These devices presented excellent gate control with on-off ratio up to 10^7 along with ultra-low capacitances down to 0.7 aF, leading to an estimated f_T up to 0.89 THz. Extremely large breakdown voltage of 500 V was observed despite their nanoscale dimensions, with small leakage current below 1 nA up to 300 V. These results reveal that III-Nitride IPGFETs offer a promising pathway for future terahertz devices delivering large output powers.

***Index Terms*—In-plane gate, nanowires, high frequency, gate capacitance, GaN, III-Nitrides, HEMTs, 2DEG, terahertz**

I. Introduction

IPGFETs offer an innovative architecture [1] in which the channel and gates lie on the same plane of the 2DEG. The gate control over electrons in the channel is done by the electric field induced from the adjacent 2DEG gates isolated from the channel by a nanoscale etched trench, which results in a small gate capacitance down to a few aF (as predicted by Ref. [2]) and can lead to much higher frequency operation. Gate electrodes are defined with the same ohmic metalization of the source and drain pads, and do not need any gate dielectrics. Thus, these devices present inherently self-aligned processes requiring only two main fabrication steps. IPGFETs demonstrated in the literature are mainly based on narrow-gap III-V heterostructures such as AlGaAs/GaAs at 300 K [1, 3–8], GaAs/InGaAs/AlGaAs at 300 K [9], InGaAs/InP at 4 K [10] and InAlAs at 300 K [11]. Although a good gate control has been demonstrated, the relatively small electron density in the 2DEG and the very low critical breakdown field in these III-Vs semiconductors yield small output current and breakdown voltage, and consequently limited output power.

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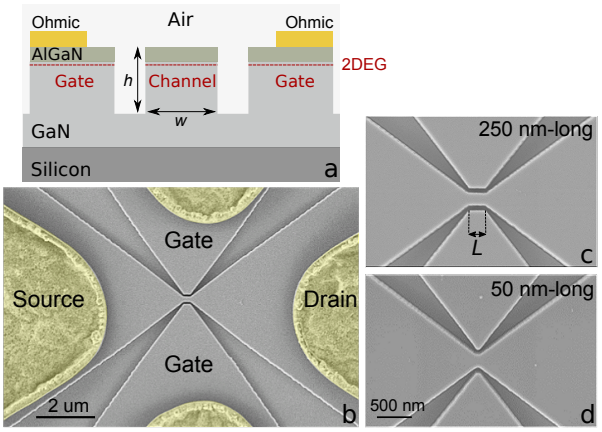

Fig. 1: (a) Schematic and (b) top-view SEM image of a 165 nm-wide and 250 nm-long IPGFET. Zoomed top-view SEM images of a 250 nm-long (c) and 50 nm-long (d) IPGFETs.

In this work, we combine the promising architecture of IPGFETs with the exceptional properties of III-Nitrides to reveal their enormous potential to deliver large output power at very high frequencies. We demonstrate for the first time high-performance IPGFETs on AlGaN/GaN heterostructures on silicon substrates with very large I_{ds} of 1.4 A/mm and g_m up to 665 mS/mm, which are respectively 9x- and 5x-larger than the best IPGFET demonstrated in other semiconductors [9], and much superior than preliminary works published on GaN semiconductors [12, 13]. In addition, our devices presented ultra-low gate capacitance down to 0.7 aF, high on-off ratio of 10^7, and very high breakdown voltage of 500 V. These results reveal the enormous potential of III-Nitride IPGFETs to deliver large output power in high frequency applications.

II. Results and Discussion

IPGFETs were fabricated on $Al_{0.25}Ga_{0.75}N$ (23.5nm)/AlN (8nm)/GaN (300 nm) followed by a 3.75 μm-thick buffer on silicon substrate. The electron mobility (μ_e), carrier concentration (n_s) and sheet resistance (R_{sh}) of the epitaxial structure measured at 300K were 1.05×10^{13}cm^{-2}, 1690cm^2/Vs and 350 $\Omega/\square$, respectively. Their simple fabrication process consists of only two major steps which inherently result in self-aligned gates. The first step is the definition of the channel, gates, source and drain by a single electron beam lithography using hydrogen silsesquioxane 2% (HSQ), followed by Cl_2-based inductively coupled plasma (ICP) etching to isolate the gate and to define mesa regions. We fabricated devices with channel lengths (L) of 250 nm and 50 nm and widths (w) varying from

20 nm to 165 nm. 60 nm-wide isolation trenches were etched with two nominal trench depths (h) of 140 nm (Shallow) and 210 nm (Deep) as measured in the mesa regions (the depth within the narrow trenches may be smaller than these values).

The second step is the deposition of ohmic contacts, defined by optical lithography, for source, drain as well as gate electrodes. A metal stack of Ti (200 Å)/Al (1200 Å)/Ti (400 Å)Ni (600 Å)/Au (500 Å) was deposited in the contact regions by electron-beam evaporation and annealed at 860°C. In this work, we focused on demonstrating the simplest fabrication process, without any oxides or passivation layers. Passivations and surface treatments are the subject of our future work. Figures 1a and b show the cross-sectional schematic and the top-view SEM image of the device after fabrication. Figures 1c and d show the zoomed SEM view of two different geometries investigated with channel lengths of 250 nm and 50 nm, respectively.

Figures 2a and b show the transfer characteristics for L of 250 nm and 50 nm, both for the Shallow and Deep samples. For a fixed L and h, the I_{ds} and $|V_{\text{th}}|$ increased for wider channel devices, due to the smaller resistance in wider channels. In addition, the more pronounced strain relaxation of the AlGaN barrier in narrower channels causes a decrease of carriers induced by piezo-electric polarization fields [14, 15], thus reducing n_s, I_{ds} and $|V_{\text{th}}|$. These devices presented a large on-off ratio up to 10^7 with a small leakage current of less than 10 pA for the Deep and 100 pA for the Shallow devices, revealing an excellent channel control from the in-plane gate with air dielectric. For a fixed w, an increase in I_{ds} along with a more negative V_{th} was observed by reducing the length of the nanowires from 250 nm to 50 nm (Fig. 2b), which is again expected due to the smaller resistance of the wire and the reduced strain relaxation in the 50 nm-long devices. Double-sweep transfer characteristic measurements (not shown) revealed a ΔV_{th} of about 0.2 V - 0.3 V, which was independent from device geometry and channel sizes. Such ΔV_{th} can be associated to the presence of traps in the AlGaN barrier and on the etched sidewalls, which can be mitigated by passivating the device.

The depth of the etched trenches that isolate the gate and channel regions has an important impact on the device performance. By reducing h while maintaining w constant, we observed a significant positive shift in V_{th} for all device widths, which reveals an increase in gate capacitance for the shallower trenches (discussed in more details later).

Figure 3a shows the output characteristics of the 50 nm-long 85 nm-wide shallow IPGFET. A large current density (I_{ds}/w) of 1.4 A/mm was observed, which is over 9x-larger than the best IPGFET [9] based on an InGaAs quantum well, due to the much larger carrier density and very small sidewall depletion in III-Nitrides [16, 17]. Figure 3b shows the transconductance of the 50 nm-long IPGFETs, revealing larger and broader g_m for wider nanowires. A significant increase in the absolute value of g_m was observed for the Shallow devices, along with a reduction on the width of the g_m curves. The normalized g_m/w was larger for smaller w due to the improved modulation over the narrower channels, going from 335 mS/mm for 85 nm-wide channel to 665 mS/mm for the

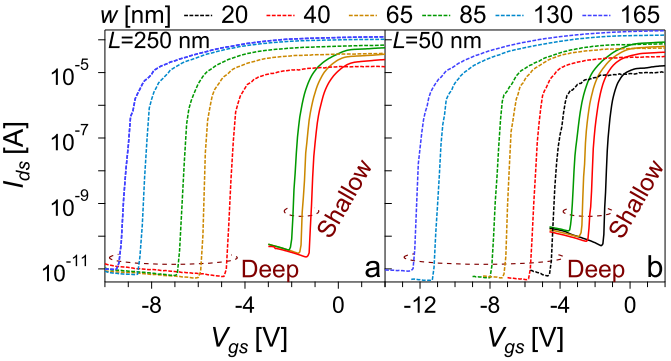

Fig. 2: Transfer characteristics of 250 nm-long and 50 nm-long IPGFETs width different widths for Deep (dashed) and Shallow (solid) IPGFETs. Both Deep and Shallow 20 nm-wide 250nm-long IPGFETs were fully depleted.

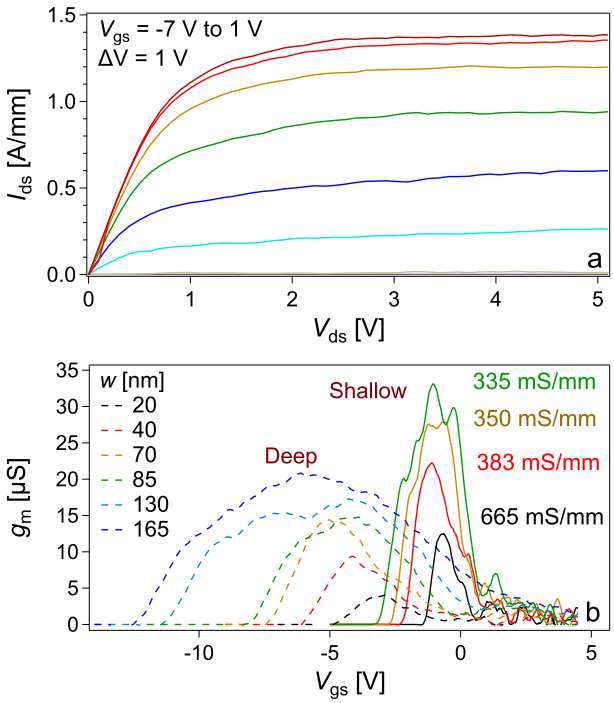

Fig. 3: (a) Output characteristic of a 50 nm-long and 85 nm-wide IPGFET. (b) Transconductance of Deep (dashed) and Shallow (solid) 50 nm-long IPGFETs. The normalized peak transconductance (g_m/w) is shown for the Shallow devices.

20 nm-wide channel, which is nearly 5x-larger than the best IPGFET [9].

High frequency operations require a small gate capacitance in addition to a large g_m, which is an intrinsic advantage of IPGFETs. The effective gate-to-channel capacitance per unit of area (C''_{eff}) was experimentally determined from n_s=$1/q \int_{V_{\text{th}}}^{0} C''(v)dv = C''_{\text{eff}} \times V_{\text{th}}/q$. We measured n_s from Hall bars with similar w, and extracted V_{th} from Fig. 2 at I_{ds} = 1 nA. Figure 4a shows the effective gate capacitance per unit of length $C'_{\text{eff}} = C''_{\text{eff}} \times w$ for the 250 nm-long IPGFETs, which includes contributions from intrinsic and extrinsic capacitances. The intrinsic C'_{int} was numerically calculated using COMSOL (blue curve in Fig. 4a), considering the device cross-section

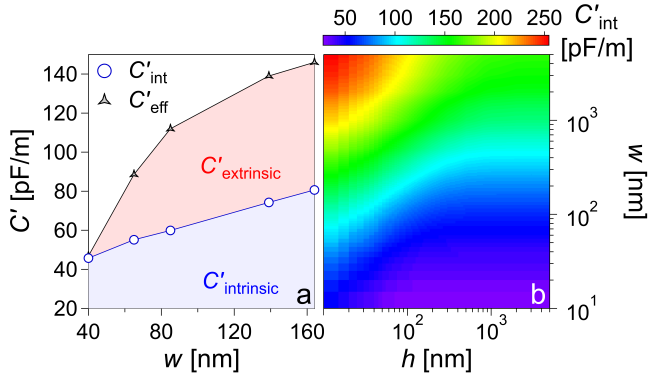

Fig. 4: (a) Measured C'_{eff} (black) and simulated C'_{int} (blue) per unit of length versus w for the 250 nm-long Deep IPGFET. (b) Simulated C'_{int} versus w and h.

TABLE I: Characteristics of the 50 nm-long Shallow and Deep IPGFETs. f_T was estimated as $f_T \approx g_m/2\pi C_{\text{eff}}$.

	w [nm]	n_s [$e12$ cm^{-2}]	C_{eff} [aF]	g_m [μS]	f_T [THz]
Shallow	20	1.9	2.2	12.4	0.89
	40	3.1	4.6	22.1	0.77
	65	4.0	8.5	27.9	0.53
	85	4.3	9.4	33.2	0.56
Deep	20	1.9	0.7	3.9	0.89
	40	3.1	1.8	9.3	0.82
	65	4.0	3.1	14.4	0.75
	85	4.3	3.9	14.7	0.60

with nominal h. Assuming that the difference between C'_{eff} and C'_{int} is due to extrinsic parasitic capacitances C'_{ext} acting on the same unit of length, we can estimate C'_{ext} (red area in Fig. 4a). The trench depth significantly affects C'_{int}, as shown in the simulation in Fig. 4b. For a given w, shallower trenches result in larger C'_{int} since the electric field lines from the gate region overlap more of the unetched semiconductor material, whose dielectric constant is larger than that of air in the trenches. Therefore, shallower trenches offer an improved gate control over electrons in the channel, which suggests an effective gate control through the unetched underlying semiconductor material. This supports the results of Fig. 3b, as the better gate control of the Shallow devices resulted in a larger g_m, and their larger C'_{int} for a given w yielded smaller $|V_{\text{th}}|$ compared to Deep devices. Other effects may also affect the channel for deeper etchings, such as a larger strain relaxation of the barrier that reduces n_s and further shifts V_{th} towards positive values.

The total effective capacitance estimated as $C_{\text{eff}} = C''_{\text{eff}} \times wL$ was in the range of 0.7 aF (20 nm-wide) to 3.9 aF (85 nm-wide) for the Deep, and 2.2 aF (20 nm-wide) to 9.4 aF (85 nm-wide) for the Shallow devices (Table I). These are extremely small values of gate capacitance, which are very promising for high frequency applications. Since these devices have not been designed for high frequency measurements, we estimated the cut-off frequencies as $f_T \approx g_m/2\pi C_{\text{eff}}$ up to 0.89 THz. Table I summarizes the characteristics of the 50 nm-long IPGFETs.

Figure 5 shows the breakdown voltage measurement for the 165 nm-wide 250 nm-long IPGFET in off-state (V_{gs} = -11 V), revealing a small drain I_{ds} and gate I_g leakage currents, below 1 nA and 100 pA respectively, even at 300 V, along with a very

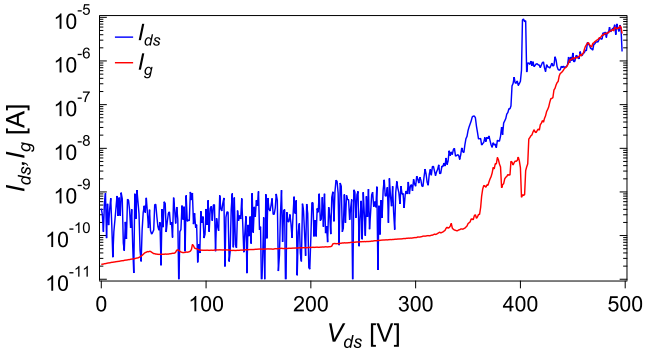

Fig. 5: (a) I_{ds} and $I_g$versus V_{ds} for a 165 nm-wide 250 nm-long IPGFET in off-state (V_{gs} = -11 V).

high breakdown voltage of 500 V (regardless of the width of the devices). The similar behavior of I_{ds} and I_g suggests that at large voltages the leakage current flows entirely through the semiconductor buffer layers, not through the nanowires, since both the drain and gate contacts are ohmic. In addition, the device performance and breakdown characteristics are not hindered by the dielectric quality, since air trenches serve as dielectric in these IPGFETs.

In conclusion, we demonstrated for the first time AlGaN/GaN IPGFETs with a large current density of 1.4 A/mm, g_m up to 665 mS/mm and very large breakdown voltage of 500 V. The in-plane gates resulted in ultra-small gate capacitance down to 0.7 aF, leading to an estimated f_T up to 0.89 THz. These results reveal the enormous potential of III-Nitride IPGFETs for high-frequency and high-power, once this technology is successfully scaled up. Furthermore, the in-plane-gate structure could offer an interesting geometry for studying carrier transport in nanoscale channels.

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