Slanted Tri-gates for High-Voltage GaN Power Devices

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***Abstract*— In this work we introduce and demonstrate the concept of slanted tri-gates to enhance the breakdown voltage (V_{BR}) in lateral GaN power devices. Conventionally field plates (FPs) are used to enhance the V_{BR} by distributing more homogeneously the electric field near the gate electrode, which is mainly determined by their pinch-off voltage (V_p). These FPs however rely on a vertical approach, in which V_p is usually designed via the thickness of the FP oxide. On the other hand, the slanted tri-gate relies on a lateral design to tailor its V_p, by simply changing the width (w) of their nanowires lithographically. Here, we demonstrate this concept for AlGaN/GaN-on-silicon MOSHEMTs resulting in an increase of ~500 V in V_{BR} compared to the counterpart planar devices. These devices presented a high V_{BR} of 1350 V with a small gate-to-drain separation (L_{GD}) of 10 µm, along with a record high-power figure-of-merit (FOM) of 1.2 GW/cm² among GaN-on-silicon lateral transistors.**

***Index Terms*—GaN, HEMT, tri-gate, slanted tri-gate, field plate, breakdown.**

I. INTRODUCTION

Lateral GaN devices are very promising for future power applications, offering large critical breakdown field, high saturation electron velocity and high-mobility 2-dimensional electron gas (2DEG). A current major challenge is the limited voltage-blocking performance in these devices, which is still far from the GaN materials capabilities. An important reason for such early breakdown is the inhomogeneous distribution of the electric field. When a high voltage is blocked in OFF state, the electric field concentrates at the edge of the gate electrode, leading to the early breakdown of the device [1]-[5]. To spread more homogeneously the electric field, various designs of FPs have been developed [4]-[6], among which slant FPs have been proven more effective [7]-[14]. Such slant FPs are achieved by a precise control over the thickness and angle of the sloped oxide in the vertical direction, which is however extremely challenging and difficult to control, and limits the design flexibility of the FPs. More importantly, a large L_{GD} is still needed for high-voltage blocking, which degrades significantly the on-resistance (R_{ON}) of the device [15].

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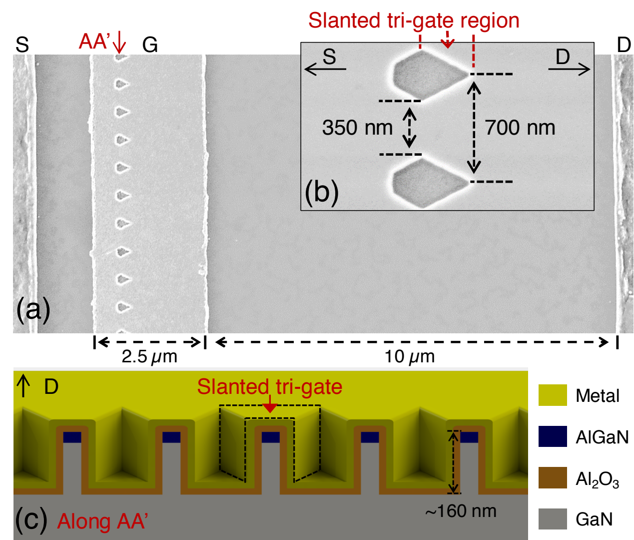

Fig. 1. Top-view SEM images of the slanted tri-gate MOSHEMT (a) with and (b) without the gate dielectric and the metal. (c) A cross-sectional schematic of the slanted tri-gate along the arrow AA'.

In this work, we present a novel concept of slanted tri-gate architecture which, similarly to vertical slant FPs, spreads more effectively the electric field and improves greatly the V_{BR} of lateral power devices. Different from vertical slant FPs, slanted tri-gate can be easily and accurately engineered with a lateral approach, by varying lithographically the width of the tri-gate nanowires. We demonstrate this concept of slanted tri-gates in GaN MOSHEMTs on silicon substrates, as shown in Fig. 1. Compared with counterpart planar transistors, the V_{BR} was enhanced by nearly 500 V using the slanted tri-gate, reaching the buffer limit of ~1350 V at 1 μA/mm with a L_{GD} as small as 10 μm, and rendering a state-of-the-art FOM up to 1.2 GW/cm².

II. PRINCIPLE AND METHODOLOGY

To explain our concept, let us first present the general working principle of FPs. The most important design variable for FPs is their pinch-off voltage (V_p), which effectively controls the distribution of the potential (Φ) and the electric field (E) in a lateral device. Figure 2 shows a simplified model on the effect of the V_p in spreading the electric field within different FP designs [1]-[3]. For devices without the FP (Fig. 2(a)), Φ in the channel increases sharply to the drain voltage V_D at the edge of the gate, where the E peaks. There is nearly no voltage drop between the gate and the drain due to the

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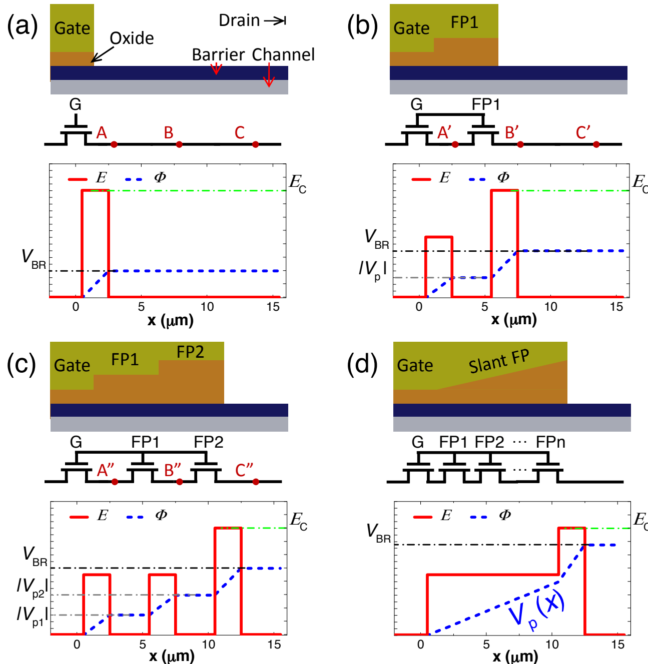

Fig. 2. Schematics, equivalent circuits and distributions of potential (Φ) and electric field (E) in lateral GaN transistors in OFF state with (a) no FPs, (b) a single FP, (c) two FPs and (d) a slant FP.

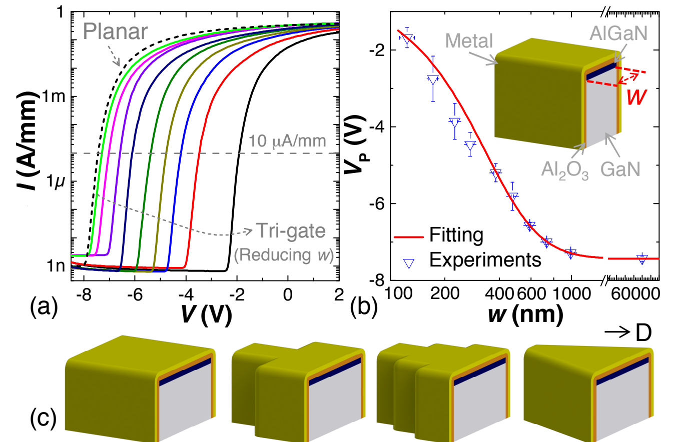

Fig. 3. (a) Average pinch-off characteristics of tri-gate AlGaN/GaN structures with different nanowire widths (w). (b) Dependence of the pinch-off voltage (V_p) on the w, in which the error bars were determined from about eight devices of each kind. The inset shows a schematic of a tri-gate AlGaN/GaN structure. (c) Schematics showing the evolution from a single tri-gate, to multiple tri-gates, and to a slanted tri-gate to engineer the gradient of the V_P with w.

high-conductivity 2DEG channel, thus E ~ 0. When E reaches the critical breakdown field (E_C), the devices breaks and the V_{BR} is determined from the integral of the $E(x)$. A FP operates as a transistor in series with the gate (Fig. 2(b)), with a more negative V_p due to the thicker oxide in the FP region. When the FP pinches off the channel underneath, the Φ at A' is fixed at a certain value (about $|V_p|$ in a simplified model according to Refs. [1] and [2]). This creates a two-step distribution of Φ, thus the total E is shared between two peaks at the edges of both the gate and the FP. The device breaks when either of the two peaks reaches E_C, which results in a larger voltage as compared to the device without the FP due to the larger integral of $E(x)$ spread in two peaks. Since a single FP is insufficient to block large voltages, multiple FPs are usually adopted to distribute better the field. As shown in Fig. 2(c), multiple FPs introduce more equivalent transistors with different V_p, creating more steps in Φ and hence more distributed peaks in E. The ultimate outcome of increasing the number of FPs is a slant FP (Fig. 2(d)), which functions as many incrementally-stepped FPs, offering a continuous gradient of V_p towards the drain. This distributes Φ across the FP as a function of x, spreads continuously the E along the entire FP region and thus improves the V_{BR}.

Therefore, the gradient of the V_p is crucial to spread the field and enhance the V_{BR}. Conventionally such gradient is obtained by a sloped etching of the oxide in a slant FP, which is however complex and difficult to design and control, restricting the realization of optimized FP designs. In this work we propose to achieve this gradient of V_p using a tri-gate structure in which V_p can be easily tailored in a simple fabrication process by varying the width of the nanowire (w) composing the tri-gate, without the laborious engineering of the thickness of the oxide. As shown in Fig. 3(a) and (b), the V_p increases smoothly with narrowing nanowires. This is mainly due to the partial relaxation of the AlGaN/GaN nanowires as well as additional electrostatic control from the sidewall gates (for the range of w investigated in this work) [16,17]. The smooth dependence of V_p on w offers a much more controllable way to obtain the gradient of the V_p with the tri-gate architecture. As shown in Fig. 3(c), a single tri-gate, as we demonstrated recently in Refs. [16,18], can easily evolve into multiple tri-gates, and ultimately into a slanted tri-gate, by simply tuning the w via lithography.

III. Device Fabrication

To demonstrate this concept, we fabricated slanted tri-gate AlGaN/GaN MOSHEMTs on silicon (Fig. 1), in which the AlGaN/GaN nanowires were defined with a slanted width and etched with a depth of ~160 nm. The w of the slanted nanowire varied from 350 nm at its source side to 700 nm at its drain side (Fig. 1(b)). 20 nm of Al_2O_3 was deposited by atomic layer deposition as gate dielectric, followed by gate metallization. As shown in Fig. 1(c), the oxide and the gate metal in the slanted tri-gate region wrap around the slanted nanowires. The source-side and drain-side planar portions of the gate metal were 0.5 μm- and 1.5 μm-long, respectively. We also fabricated MOSHEMTs with conventional planar gates and tri-gates on the same chip for comparison. They shared the same design and dimensions as the slanted tri-gate device, except for the nanowires. The planar device had no nanowires, while the tri-gate device had a constant w of 600 nm, instead of slanted. The drain-side planar portion of the gate metal in the tri-gate device was 1.3 μm-long, which is slightly smaller than in the slanted tri-gate device but does not cause any significant changes in the V_{BR} according to our observation.

All device characteristics in this work, such as drain current (I_D), transconductance (g_m) and OFF-state leakage current (I_{OFF}), were normalized by the width of the device footprint (60 μm). To understand the isolated effect of slanted tri-gate in enhancing the V_{BR}, we did not adopt conventional FPs or passivation in these devices.

IV. Results and Discussion

To understand the enhancement in V_{BR} by the slanted tri-gate, we compare the breakdown characteristics the planar, tri-gate

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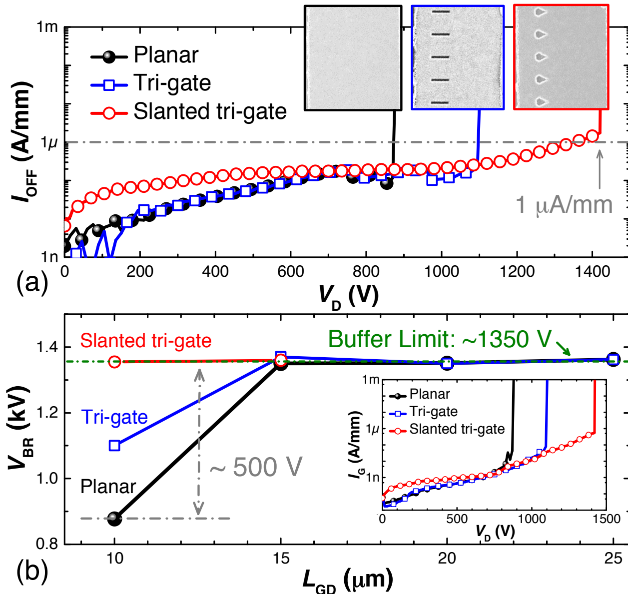

Fig. 4. (a) Typical breakdown characteristics of MOSHEMTs with planar gates, tri-gates and slanted tri-gates and (b) their L_{GD}-dependent V_{BR} (at 1 μA/mm), measured at V_G of -10 V with a floating substrate, in which the I_{OFF} for all devices was normalized by their footprint width. The insets in (a) show the top-view SEM images of the gate region of the three types of devices. The inset in (b) shows the gate leakage current of the devices. The gate-to-source distance (L_{GS}), gate length (L_G) and L_{GD} are 1.5 μm, 2.5 μm, and 10 μm, respectively.

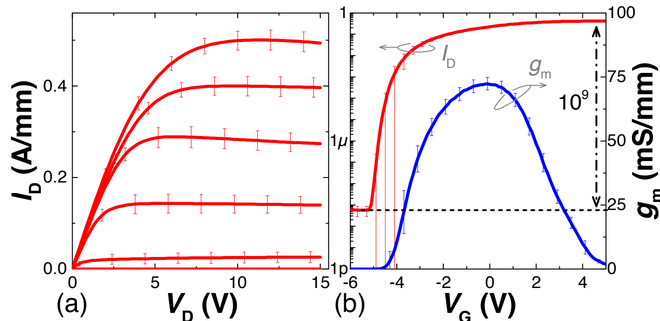

Fig. 5. (a) Average output and (b) transfer characteristics of the slanted tri-gate devices, normalized by their footprint width. The error bars were determined from measurements on six devices. The L_{GS}, L_G, and L_{GD} of all devices are 1.5 μm, 2.5 μm and 10 μm, respectively.

and slanted tri-gate devices in Fig. 4(a). An improvement in V_{BR} from 877 to 1100 V at 1 μA/mm was observed with the introduction of the tri-gate region in a portion of the gate (as shown in the insets of Fig. 4(a)), which creates a region of a smaller $|V_p|$ within the gate and converts the planar part of the gate towards the drain side into an effective FP, spreading more effectively the electric field as discussed previously (Fig. 2(b)). The V_{BR} was further improved with the slanted tri-gate to 1350 V at 1 μA/mm. Figure 4(b) shows the large improvement in V_{BR} reaching the limit of our buffer layers with a L_{GD} as small as 10 μm due to the more effective spreading of the electric field by the slanted tri-gate. More importantly, the significant enhancement observed from the planar to the tri-gate and slanted tri-gate transistors was achieved by simply patterning the tri-gate and slanted tri-gate regions during the mesa etching to engineer the pinch-off voltage. The remainder of the device structure and fabrication process is exactly the same of the planar device. The larger I_{OFF} of the slanted tri-gate device at small voltages is likely due to its much smaller effective gate

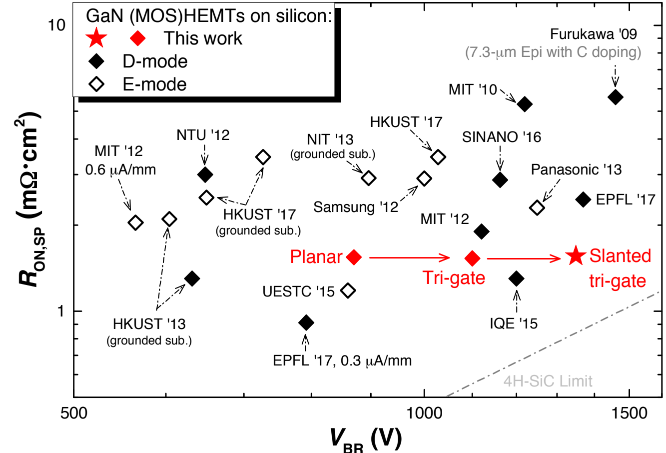

Fig. 6. Specific on-resistance ($R_{ON,SP}$) versus V_{BR} benchmarks of the slanted tri-gate MOSHEMTs against state-of-the-art GaN E/D-mode (MOS)HEMTs on silicon by defining the V_{BR} at $I_{OFF} \leq 1$ μA/mm. A 1.5-μm transfer length for each ohmic contact was considered for calculation of the $R_{ON,SP}$, and the V_{BR} for all reference devices was re-calculated based on the reported data following the definition of V_{BR} at $I_{OFF} \leq 1$ μA/mm.

length, since the three devices have the same buffer leakage current as they were fabricated on the same chip, and exhibited small gate leakage currents ≤ 2 nA/mm at 750 V (the inset of Fig. 4(b)). The I_{OFF} of the slanted tri-gate devices at high voltages was similar to the other devices, which shows that the larger I_{OFF} at low biases does not degrade the value of the slanted tri-gate in enhancing the V_{BR} of the device.

In addition to the high V_{BR}, the slanted tri-gate device also exhibited excellent ON-state performance (Fig.5), presenting a high ON/OFF-current ratio over 10^9 and a maximum g_m of 72.4 ± 2.4 mS/mm (at V_D of 5 V), higher than in the planar device (66.1 ± 2 mS/mm). The R_{ON} was 9.4 ± 0.5 Ω·mm, very close to that of the planar device (9.1 ± 0.2 Ω·mm) despite the removal of carriers in its gate region during the nanowire etching.

The slanted tri-gate devices were benchmarked against state-of-the-art GaN (MOS)HEMTs on silicon substrates (Fig. 6). The high V_{BR} of 1350 V at 1 μA/mm presented in this work is comparable to the best-reported value of V_{BR} (1460 V) [15] but with a 14-μm-smaller L_{GD}, resulting in a 3.6x-smaller $R_{ON,SP}$. The high-power FOM of the slanted tri-gate transistors was up to 1.2 GW/cm^2, which is a record value to the best of our knowledge and reveals the significant potential of the slanted tri-gate for the enhancement of V_{BR} in GaN power devices while maintaining small L_{GD} and R_{ON}.

V. Conclusion

In this work we demonstrated a novel slanted tri-gate architecture to enhance the voltage-blocking performance in lateral GaN devices, whose V_p can be tailored laterally by varying w with lithography. This provides a new degree of freedom for engineering the distribution of electric field and opens enormous opportunities for nanostructured GaN devices in future power/RF applications.

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