Total Ionizing Dose Effects on Analog Performance of 28 nm Bulk MOSFETs

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***Abstract*—This paper uses the simplified charge-based EKV MOSFET model for studying the effects of total ionizing dose (TID) on analog parameters and figures-of-merit (FoMs) of 28 nm bulk MOSFETs. These effects are demonstrated to be fully captured by the five key parameters of the simplified EKV model. The latter are extracted from the measured transfer characteristics at each TID. Despite the very few parameters, both the simplified large- and small-signal models present an excellent match with measurements at all levels of TID. The impacts of TID on essential parameters, including the drain leakage current, the threshold voltage, the slope factor, and the specific current, are then evaluated. Finally, TID effects on the transconductance G_m, the output conductance G_{ds}, the intrinsic gain G_m/G_{ds} and the transconductance efficiency G_m/I_D are investigated.**

***Index Terms*—analog parameters, transconductance efficiency, EKV, intrinsic gain, inversion coefficient, TID, 28 nm bulk MOSFETs**

I. Introduction

The forthcoming high-luminosity Large Hadron Collider (HL-LHC) at CERN is expected to experience an unprecedented radiation level up to 1 Grad of total ionizing dose (TID) over ten years of operation. This will be a challenge for the electronic components of the innermost detectors, including analog amplifiers, filters, analog-to-digital converters and application-specific integrated circuits. For a long-term reliable operation, highly upgraded detecting systems are needed with a higher bandwidth and more radiation-tolerant front-end electronics. Aggressively downscaled CMOS technologies bring a high operation speed and demonstrate the capability of mitigating TID effects [1], [2]. Therefore, we have started investigating the radiation tolerance of a commercial 28 nm bulk CMOS process up to 1 Grad with the perspective of using it for the future radiation-tolerant detectors [3], [4].

Our previous studies have shown that the dominant TID effects on 28 nm bulk MOSFETs include a significant drain leakage current increase, a subthreshold swing degradation, a substantial drive current loss, a threshold voltage shift, and a mobility reduction. Prior investigations have attributed these parameter variations to radiation-induced charge generation and trapping related to dielectrics [5]. Although significant progress has been made in understanding the underlying physics of TID effects, not much work has been undertaken about the effects on analog parameters and figures-of-merit (FoMs). As a first step towards the characterization of these effects, this work proposes to use the simplified charge-based EKV MOSFET model which requires only five parameters to fully describe the large- and small-signal characteristics over a wide range of bias from weak to strong inversion and even for advanced technology nodes [6], [7]. Additionally, the inversion coefficient offers an efficient way to normalize the MOSFET characteristics and to evaluate the transconductance efficiency G_m/I_D over a wide range of operating points.

This paper first describes the simplified EKV model, the parameter extraction methodology and the model validation with measurements in Section II. TID effects on extracted model parameters are discussed in Section III, while the impacts of TID on the intrinsic gain and the transconductance efficiency are illustrated in Section IV and Section V. The paper ends up with a brief conclusion.

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II. The Simplified EKV Model and the Related Parameters

A. Model Description

The simplified charge-based EKV MOSFET model introduces *inversion coefficient* IC to replace the overdrive voltage $V_G - V_{T0}$ as an essential design parameter that spans the entire range of operating points from weak via moderate to strong inversion. IC identifies the channel inversion level of a MOSFET and is defined as the normalized drain current [8]:

$$IC \triangleq I_D|_{saturation}/I_{spec}, \tag{1}$$

where I_{spec} is the *specific current* defined as [8]

$$I_{spec} = I_{spec\square} \cdot W/L \quad \text{with} \quad I_{spec\square} \triangleq 2n \cdot \mu_0 \cdot C_{ox} \cdot U_T^2, \tag{2}$$

where $I_{spec\square}$ is the *specific current per square*, n is the *slope factor*, μ_0 is the *low-field channel mobility*, C_{ox} is the *gate oxide capacitance per unit area*, and $U_T \triangleq kT/q$ is the *thermal voltage*. Based on IC, operation regions of a MOSFET can be classified as *weak inversion* (WI) for $IC \leqslant 0.1$, *moderate inversion* (MI) for $0.1 < IC \leqslant 10$, and *strong inversion* (SI) for $IC > 10$.

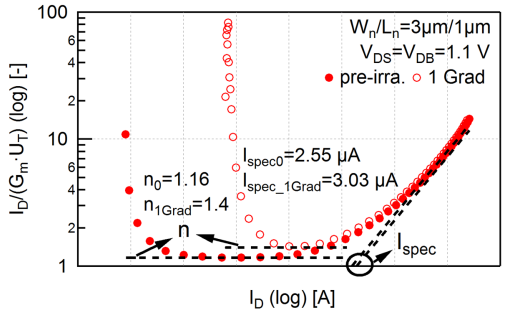

Fig. 1. Extraction of the slope factor n and the specific current I_{spec} with an example of a wide/long-channel nMOSFET.

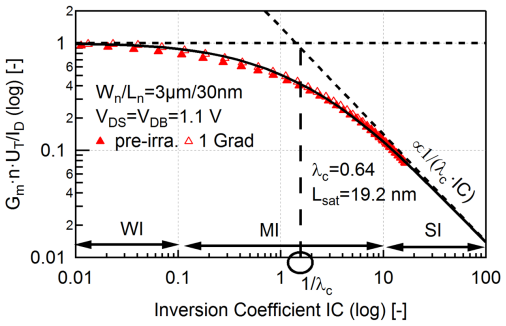

Fig. 2. Extraction of the velocity saturation parameter λ_c with an example of a wide/short-channel MOSFET.

To model the impact of *velocity saturation* (VS) on short-channel devices, the parameter λ_c is introduced as [6]

$$\lambda_c = L_{sat}/L, \tag{3}$$

with L_{sat} being the portion of the channel over which the carrier drift velocity saturates. Including the effect of VS, the normalized saturation voltage is then expressed as

$$\begin{aligned}(V_P - V_S)/U_T &= (V_G - V_{T0} - n\cdot V_S)/(n\cdot U_T)\\ &= \ln\left[f(IC)/2\right] + f(IC),\\ f(IC) &= \sqrt{(\lambda_c\cdot IC+1)^2 + 4\cdot IC} - 1,\end{aligned} \tag{4}$$

where V_{T0} is the *threshold voltage*.

Since TID has a strong impact on the *drain leakage current*, the latter is approximated by a constant current adding to the drain current. It constitutes an additional parameter I_{leak} to the simplified EKV model which is straightforward to extract.

Note that the above normalization makes the simplified EKV model independent of technology, which is entirely captured by five parameters (V_{T0}, n, I_{spec}, L_{sat} and I_{leak}). This is the main reason for which we use it to investigate the effects of TID on MOSFET characteristics.

B. Parameter Extraction

The parameter extraction starts with extracting the *slope factor* n from the plateau of $I_D/(G_m\cdot U_T)$ versus I_D curve in WI for a long-channel device, as illustrated in Fig. 1 for measurements with respect to pre-irradiation and a high TID. It is followed by the extraction of the *specific current* I_{spec}

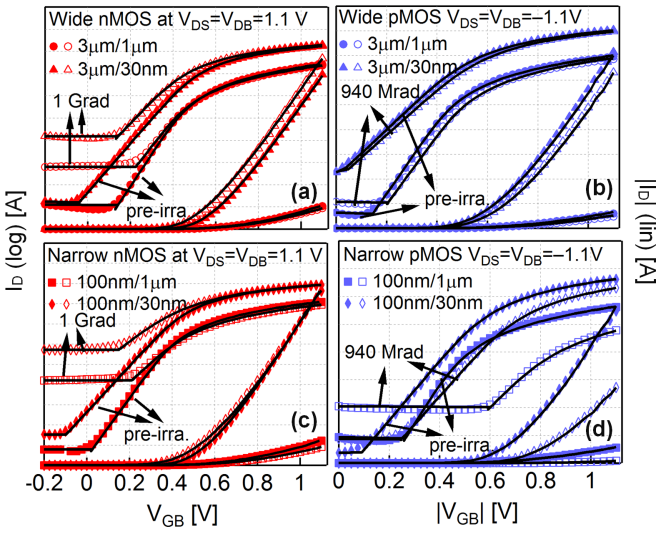

Fig. 3. Modeled and measured transfer characteristics of n (a,c) and p (b,d) types of MOSFETs with respect to pre-irradiation (solid markers) and a high TID (open markers).

from the same plot as the current at the intersection of the SI asymptote and the unity horizontal line. Having n and I_{spec}, and therefore $I_{spec\square}$, we can then plot the normalized transconductance efficiency $G_m\cdot n\cdot U_T/I_D$ versus IC for a short-channel device, as shown in Fig. 2. $1/\lambda_c$ is extracted at the intersection of the SI asymptote $1/(\lambda_c\cdot IC)$ and the unity horizontal line. Having now extracted n, I_{spec}, and λ_c, we can use (4) to calculate the overdrive voltage. The *threshold voltage* V_{T0} is then extracted to fit the model with the measured I_D versus V_{GB} curve. The last parameter is the *drain leakage current* I_{leak} that is easily extracted from the plateau of the I_D versus V_{GB} curve in WI, when available.

C. Large-signal Transfer Characteristics Validation

Fig. 3 compares the model to the measured transfer characteristics for all investigated devices with respect to pre-irradiation and a high TID. The simplified model matches pre-irradiation measurements very well in all regions of operation, demonstrating the capability of fully capturing the technology with only five parameters. This excellent agreement extends to all levels of TID, as plotted for the highest one in Fig. 3, which confirms the promising use of this simplified model in radiation-tolerant circuit design in nanoscale CMOS processes.

The comparison of measurements at pre-irradiation and a high TID indicates a significant *drain leakage current* increase for nMOSFETs (Fig. 3ac) and a substantial drive current loss for pMOSFETs (Fig. 3bd) as well as a *threshold voltage* shift and a *slope factor* degradation. Relevant parameters extracted with the simplified model are discussed in Section III.

III. TID Effects on Analog Parameters

The five model parameters are extracted for each TID by following the procedures in Section II. Fig. 4 presents the evolution of extracted parameters with TID. Fig. 4a illustrates the significant *drain leakage current* increase for nMOSFETs,

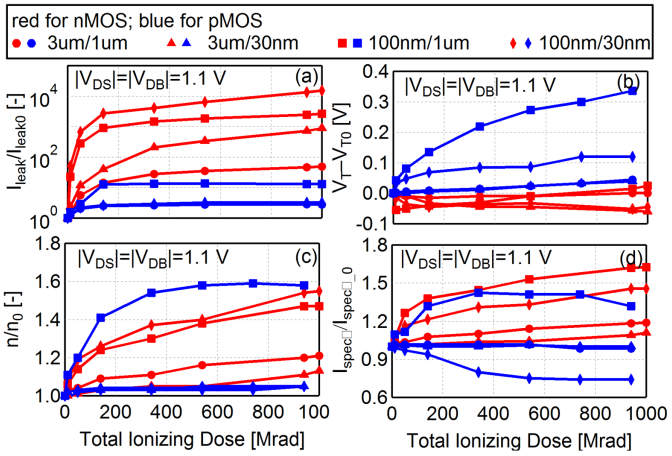

Fig. 4. TID effects on the drain leakage current (a), the threshold voltage (b), the slope factor (c), and the specific current per square (d) of *n*- and *p*MOSFETs.

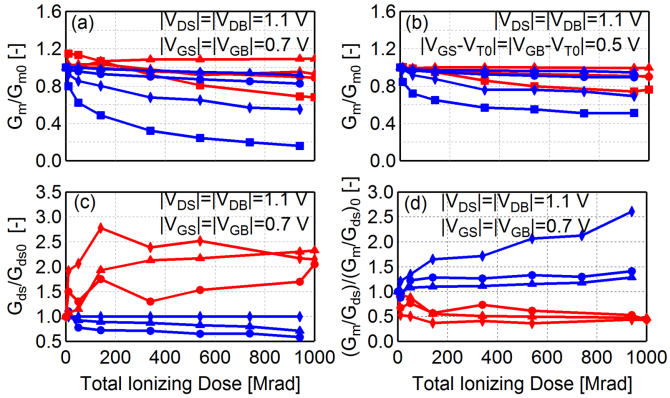

Fig. 5. TID effects on the transconductance (ab), the output conductance (c), and the intrinsic gain (d) of *n*- and *p*MOSFETs. This plot shares the legend with Fig. 4.

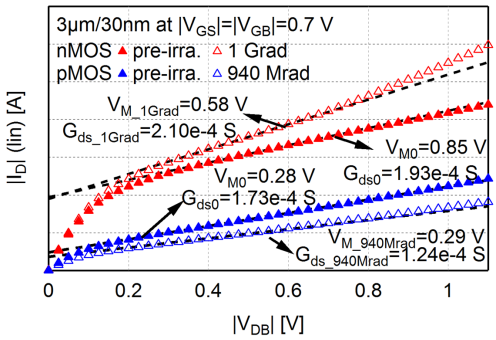

Fig. 6. Output characteristics of wide/short-channel (3 µm/30 nm) *n*- and *p*MOSFETs.

as also seen in Fig. 3ac. This increase is closely related to the radiation-induced parasitic leakage current along the sidewalls of the shallow-trench isolation (STI) [9].

Short-channel *n*MOSFETs present a slight *threshold voltage* decrease in Fig. 4b. Due to the counterbalance of interface over oxide charged traps, the *threshold voltage* of long-channel *n*MOSFETs first decreases and then increases [10]. In contrast, the superposed effects of oxide and interface charged traps result in a *threshold voltage* increment for all *p*MOSFETs. The increase reaches almost 350 mV for the narrow/long-channel *p*MOSFET, which corresponds to the significant drive current loss observed in Fig. 3d.

Except the narrow/long-channel *p*MOSFET, all other *p*MOSFETs show a negligible *slope factor* increase in Fig. 4c. The *slope factor* of *n*MOSFETs, especially two narrow-channel devices, is more sensitive to TID. The *slope factor* increase in narrow-channel MOSFETs is mostly due to the charge trapping at STI-related border traps or interface traps.

For most of MOSFETs, the *specific current* (Fig. 4d) follows the trend of the *slope factor* (Fig. 4c). However, the *specific current* of *p*MOSFETs, particularly two narrow-channel devices, starts to decrease at a certain TID. This demonstrates the radiation-induced mobility reduction, as predicted by (2).

As a first conclusion, the model and measurements demonstrate the high radiation tolerance of most of studied MOSFETs except some narrow-channel devices. Designers should therefore be careful when using narrow-channel MOSFETs for radiation-tolerant circuit design. Note that the *velocity saturation* parameter λ_c remains almost constant with TID, which is not shown here.

IV. TID Effects on the Intrinsic Gain

The correct operation of many analog circuits relies on a sufficient *intrinsic gain* of the transistors. Therefore, it is crucial to investigate TID effects on this FoM. Fig. 5acd show the *transconductance* G_m, the *output conductance* G_{ds} and the *intrinsic gain* G_m/G_{ds} evaluated at the same operating point $|V_{DB}| = 1.1\,\mathrm{V}$ and $|V_{GB}| = 0.7\,\mathrm{V}$ as a function of TID. The *transconductance* plotted in Fig. 5a includes the effects of both *threshold voltage* shift and *mobility reduction*. It is basically following the *threshold voltage* shift shown in Fig. 4b. The *transconductance* of long-channel and narrow/short-channel *n*MOSFETs first increases and then decreases, while that of the narrow/short-channel device continuously increases until the highest TID. Due to the significant *threshold voltage* increment, *p*MOSFETs present a substantial *transconductance* loss that is higher than the same size of *n*MOSFETs. To eliminate the effect of *threshold voltage* shift, the *transconductance* at a constant overdrive voltage ($|V_{GB} - V_{T0}| = 0.5\,\mathrm{V}$) is shown in Fig. 5b. All studied MOSFETs are still having a *transconductance* loss but less compared with Fig. 5a. The remaining loss in Fig. 5b is from the radiation-induced *mobility reduction*. Two narrow-channel *p*MOSFETs present the most serious *mobility reduction* that is consistent with their $I_{spec\square}$ decrease shown in Fig. 4d.

Fig. 5c presents the evolution of *output conductance* with TID. It increases for *n*MOSFETs and decreases for *p*MOSFETs. This behavior can be clearly seen from the output characteristics of wide/short-channel (3 µm/30 nm) *n*- and *p*MOSFETs plotted in Fig. 6. After a high TID, the wide/short-channel *n*MOSFET shows a lower Early voltage and hence

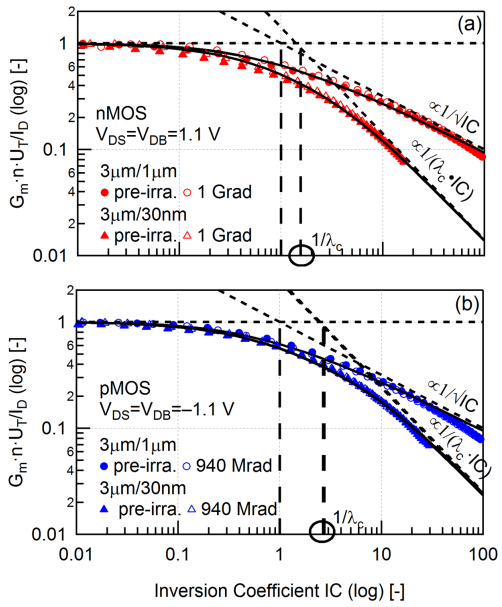

Fig. 7. Normalized transconductance efficiency of *n* (a) and *p* (b) types of wide/long- and wide/short-channel MOSFETs with respect to pre-irradiation and a high level of TID.

a higher *output conductance*, whereas the wide/short-channel *p*MOSFET presents a higher Early voltage and a lower *output conductance*. The observed modification in *output conductance* demonstrates the radiation-enhanced drain-induced barrier lowering (DIBL) for *n*MOSFETs and the radiation-suppressed DIBL for *p*MOSFETs. The *transconductance* loss and the *output conductance* increase result in a degraded *intrinsic gain* for *n*MOSFETs, as shown in Fig. 5d. Owning to a lower *output conductance* after irradiation, *p*MOSFETs obtain a slightly improved *intrinsic gain*.

V. TID Effects on the Transconductance Efficiency

The *transconductance efficiency* G_m/I_D is an important analog FoM for low-power analog circuit design. The normalized *transconductance efficiency* of wide/long- and wide/short-channel MOSFETs is illustrated in Fig. 7 which highlights the VS-induced degradation at a high IC. Moreover, after a proper normalization with extracted parameters, all the measured points with respect to pre-irradiation and a high TID are seen to nicely fall on the curves of the simplified EKV model. This demonstrates the negligible effects of TID on the *normalized* G_m/I_D. Although the ionizing radiation affects the analog parameters, the normalization strips off the TID effects from the normalized *transconductance efficiency*. This inversion coefficient based simplified model can therefore be promising for radiation-tolerant low-power analog circuit design.

VI. Conclusion

The effects of high total ionizing dose on analog performance of a 28 nm bulk CMOS process are investigated using the simplified charge-based EKV MOSFET model that requires only five parameters to fully describe the dc behavior of MOSFETs. The parameters are first extracted for non-irradiated *n*- and *p*MOSFETs of various sizes, hence validating the model. The same parameters are then extracted at each TID up to 1 Grad. The *drain leakage current* is the most seriously affected parameter, particularly for narrow-channel *n*MOSFETs. The *threshold voltage* demonstrates a slight change for *n*MOSFETs and a large increase for narrow-channel *p*MOSFETs. The impact of TID on the *intrinsic gain* is also investigated. It shows a reduction by half for *n*MOSFETs, whereas it increases by up to 2.5x for *p*MOSFETs. Finally, TID effects on the *transconductance efficiency* G_m/I_d is evaluated. After the proper parameter extraction and normalization, TID shows a negligible influence on the normalized *transconductance efficiency*. This study shows that overall, the 28 nm bulk CMOS process is rather radiation tolerant except for narrow/long-channel MOSFETs. It also highlights the advantage of using the simplified charge-based EKV MOSFET model for analyzing TID effects on analog performance.

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