

# Novel Insight into the Output Current Ripple for Multilevel and Multiphase Converter Topologies

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**Abstract**—When it comes to the computation / estimation of the switching losses in a multilevel converter, it is crucial to know the instantaneous value of the output current. If the average output current value is used instead, there is a non negligible error when the quality of the output current waveform is low. This paper addresses this issue with a generic and versatile fast numerical method for phase-disposition PWM that produces the exact switching pattern, hence the exact inductor flux, without having to run time-domain switched simulation(s), as the calculations are performed for the minimal set of points required to fully determine the inductor flux ripple at the switching instants.

## I. INTRODUCTION

A semi-numerical method has been proposed in [1] for the fast estimation of submodule losses for a DC/AC modular multilevel converter (MMC) using the concept of virtual submodule (VSM). In that work, the need for detailed and time consuming switched model simulations is avoided by adopting an analytical average model that captures the low order harmonics in the branch capacitor voltage, branch current and branch modulation index. Two main hypotheses were necessary: (i) the branch current ripple is neglected and (ii) the capacitor voltage spread within a branch is replaced with its average. Such a model is sufficient to estimate the average semiconductor losses in the case of an MMC, where conduction losses are predominant, due to the low submodule switching frequency. The reported time gain was considerable, allowing for the comparison of multiple control methods and power semiconductor devices in a very short time. In contrast to an MMC, conventional multi-level and -phase topologies have much smaller capacitor voltage ripples, if we assume a tight control of the intermediate capacitor voltages. This means the sensitivity to voltage variations is reduced. In this paper, the VSM concept is adapted to conventional multilevel converters and augmented with a fast and versatile numerical method for modeling the instantaneous output current ripple at the switching instants. The improvement offered by the proposed method is shown in Fig. 1. The original VSM method was considering the average fundamental flux / current (× marks), while the proposed method reconstructs the instantaneous output flux / current (○ marks). Depending on the converter’s switching frequency and its output inductor value, there could be a significant difference between these two sets of values, which would translate into notable discrepancies in the semiconductor switching losses estimation.

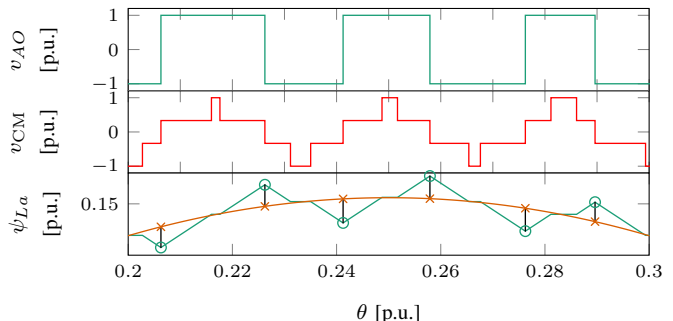


Figure 1: Fraction of a fundamental period for  $N_{Iv1} = 2$ ,  $p = 30$ ,  $M = 0.95$  and  $n_{ph} = 3$ . In the bottom plot, × marks indicate the switched output flux taken from the average for the VSM method, while ○ marks indicate the exact switched output flux with the proposed method.

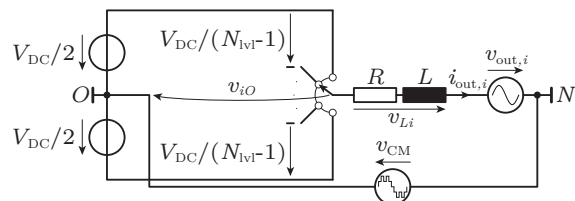


Figure 2: Multi-level and -phase generalization of the problem for the phase  $i$ .  $L$  represents either the output inductor or the leakage inductance of the output transformer. The common mode voltage is defined as  $v_{CM} = v_{NO} = \sum_i v_{iO} / n_{ph}$  (containing high order harmonics and eventually some low order harmonics, in case the DC bus utilization is extended).

Several works have been published on the peak-to-peak and envelope of the output current ripple for three-phase [2], [3] and multi-phase converters [4]. Except for the mathematical exercise, it is unclear how this information can be useful in the converter design phase. The peak output current coincides with all switching events only for the case of multilevel single-phase converters. This can be observed in Fig. 1, as the output flux / current changes its slope with switching events in any phase. For multiphase converters, no closed-form analytical solution has been reported, so a numerical method that accurately determines the ripple current value at the phase switching instants is proposed. Phase-disposition PWM (PD-PWM) is considered throughout the paper, even though other level-shifted modulation methods could be accounted for as well, at the expense of small adaptations. The generalized representation for one phase of a multi-level and -phase

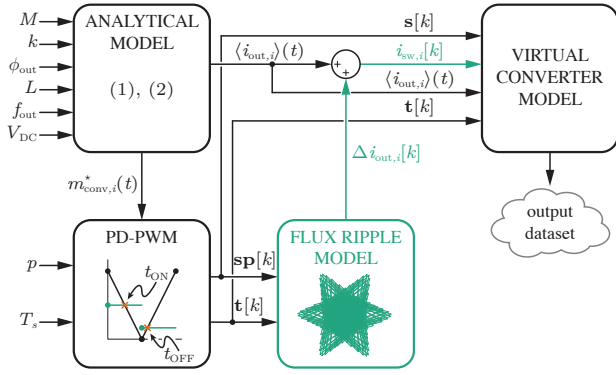


Figure 3: Extended VSM concept to multilevel converters with addition of an output flux / current ripple model. The model is composed by four logical blocks: (i) an analytical model that determines the reference modulation index and fundamental output current, (ii) a modulation block based on the single-carrier PD-PWM, (iii) an output flux ripple model and (iv) a virtual converter model.

converter is shown in Fig. 2. This model is used for the theoretical developments in the paper. The influence of the other phases is entirely captured through the common mode voltage  $v_{CM}$ , which plays a crucial role. Note that under the assumption of constant intermediate voltages the output flux / current is independent from the converter's topology, for identical number of phases, levels and output switching frequency.

## II. EXTENDED VSM METHOD FOR MULTILEVEL CONVERTERS

The extended VSM method for conventional multilevel converters, with addition of an output flux / current ripple model, is shown in Fig. 3.

### A. Reference calculation

The converter reference signal is defined as:

$$m_{conv,i}^*(t) = \underbrace{M \cos\left(\omega_{out}t + \frac{(i-1)2\pi}{n_{ph}}\right)}_{m_{conv,fund,i}^*} + m_{CM}(t), \quad (1)$$

where  $M = 2\hat{v}_{conv}/V_{DC}$ ,  $\omega_{out} = 2\pi f_{out}$  and  $i \in \{1, \dots, n_{ph}\}$ .  $M \in [0, 1]$  without extended DC bus utilization, or  $M \in [0, 1/\cos(\pi/2n_{ph})]$  when the common mode signal  $m_{CM}(t)$  is used to extend the linear modulation range [5]. The common mode signal is generated either by (i)  $n_{ph}$ -th harmonic injection, (ii) min/max or (iii) generalized flat-topped modulation (extension for multi-phase systems of the proposal in [6]). Details about this are presented in Appendix A.

A reference change is performed to constrain  $m_{conv,i}^*$  in  $[0, 1]$ :  $m_{conv}^{*'} = (1 + m_{conv}^*)/2$ . The average fundamental (noted as  $\langle \cdot \rangle$ ) output current is determined by complex calculation (the resistance  $R$  is ignored in the paper):

$$\langle i_{out} \rangle = \frac{\langle v_{conv} \rangle - v_{out}}{\omega_{out}L}, \quad (2)$$

where

$$\langle v_{conv} \rangle = M \frac{V_{DC}}{2} e^{j\omega_{out}t}, \quad v_{out} = k \frac{V_{DC}}{2} e^{j(\omega_{out}t + \phi_{out})}. \quad (3)$$

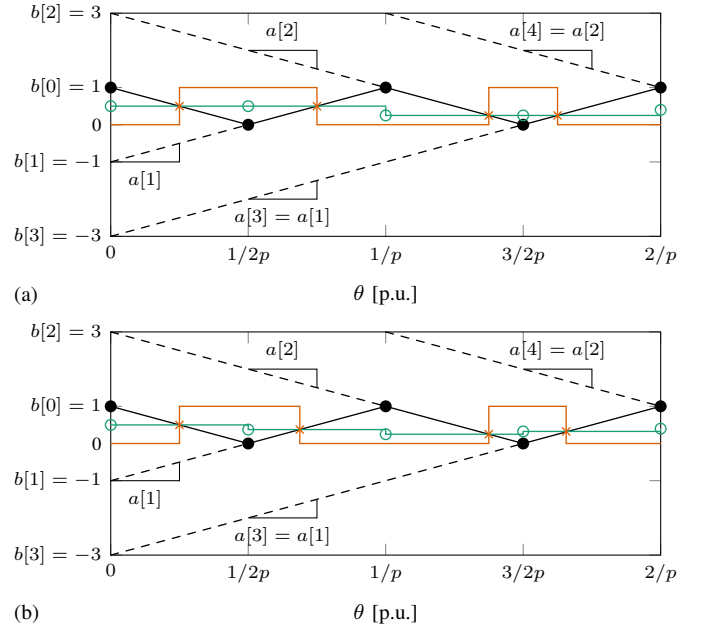


Figure 4: Reference / carrier intersection process for (a) symmetrical sampling with modulation index resampling at  $T_{sw}/2$  and (b) asymmetrical sampling.  $\bullet$  is the carrier signal,  $\circ$  the sampled single-carrier modulation index  $m_{conv,i}^{*'}[k]$ ,  $\times$  the computed reference / carrier intersection and  $\text{—}$  the resulting phase switching pattern. The circles / marks indicate the respective times and values of the various signals that are stored for further computations.

The magnitude and phase of the output current are extracted from (2).

### B. PD-PWM model

The reference signals are sampled at  $t[k] = kT_s$ , with  $T_s = T_{sw} = 1/pf_{out}$  for symmetrical sampling or  $T_s = T_{sw}/2$  for asymmetrical sampling. The phase correction of  $T_s/2$  is implemented [7]. Note that this is an approximation that assumes a linear evolution of  $m_{conv,i}^{*'}(t)$  over a sampling interval  $[kT_s, (k+1)T_s]$ . However, the lower the switching frequency the less valid this approximation is. Some adaptations have to be introduced in order to compensate for these imprecisions. More details are presented in Appendix B. In case of symmetrical sampling, the reference has to be resampled with  $T_s/2$  by duplicating the values, as shown in Fig. 4(a), in order to determine the switching time (or angle) every half carrier period, that corresponds to either a switch-on or a switch-off. This means there is no real complexity increase for asymmetrical over symmetrical sampling. For each half carrier period, the switching time (or angle) is obtained by solving an affine problem in each phase:

$$m_{conv,i}^{*'}[k] = a[k]\theta_i + b[k] \quad (4)$$

for  $\theta_i$ , where the slope and the offset of the carrier signal are given by:

$$a[k] = \frac{(-1)^{k+1}}{2pf_{out}}, \quad b[k] = \frac{(-1)^k(2k+1)+1}{2}. \quad (5)$$

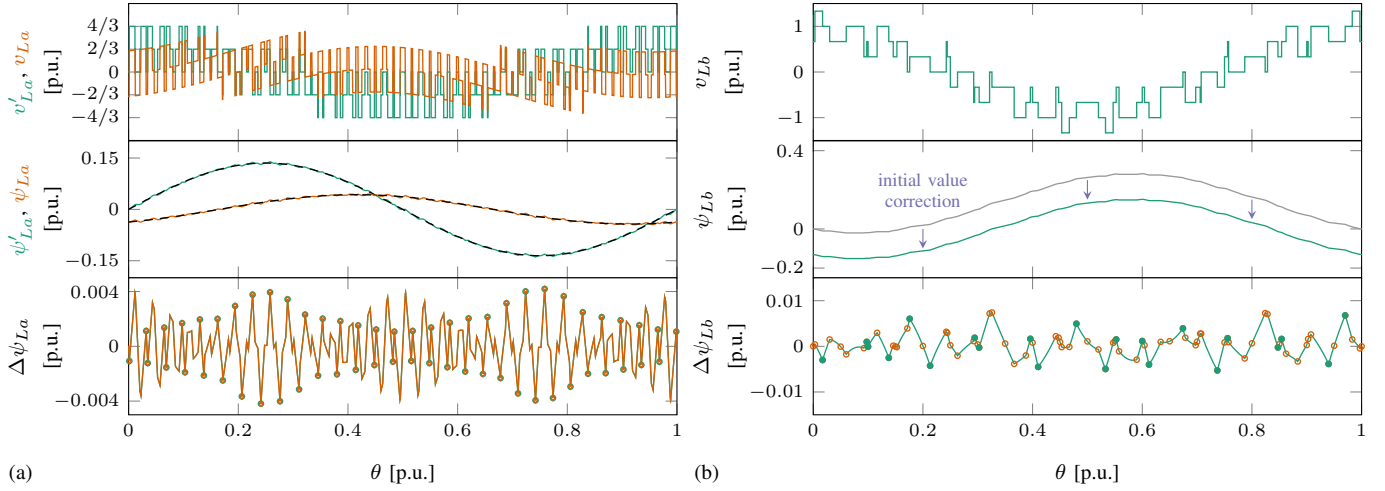


Figure 5: Flux ripple model illustration. (a)  $N_{lv1} = 2$ ,  $p = 30$ ,  $M = 0.85$ ,  $k = 0.75$ ,  $\phi = \pi/10$ ,  $n_{ph} = 3$  and asymmetrical sampling, in the phase  $a$ , without grid (—) and with grid (—). The output flux ripple values are perfectly matching at the switching instants (○ vs. ◇ marks), confirming the output flux ripple is only determined by  $m_{conv}^*$ . (b)  $N_{lv1} = 3$ ,  $p = 10$ ,  $M = 0.95$  and asymmetrical sampling, in the phase  $b$  with ○ marks for switching events in  $v_{CM}$  and ● marks for switching events in the phase  $b$ . The initial value correction is derived from the sine curve fitting (the parameter  $C$ ), as explained in Appendix B. Observe that the output flux ripple envelope doesn't capture the complete set of phase switching instants.

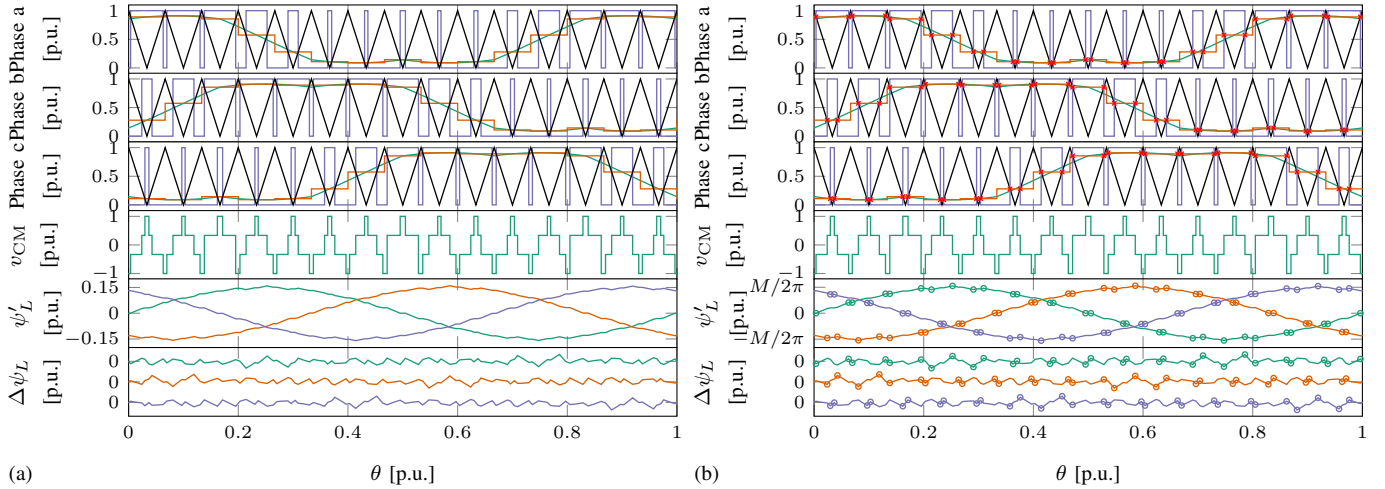


Figure 6: Results for  $N_{lv1} = 2$ ,  $p = 15$ ,  $M = 0.95$ ,  $n_{ph} = 3$ , asymmetrical sampling and min/max common mode injection: (a) PLECS model and (b) proposed method. × marks indicate the reference / carrier intersections, while ○ marks correspond to the instants where the respective phase is switching.

In order to account for multilevel waveforms, the single-carrier PWM presented in [8], implying the sampling of:

$$m_{conv,mod,i}^*[k] = (N_{lv1} - 1) \left( m_{conv,i}^*[k] - \frac{\text{floor}(m_{conv,i}^*[k](N_{lv1} - 1))}{N_{lv1} - 1} \right), \quad (6)$$

rather than  $m_{conv,i}^*[k]$ , is combined with a function  $cbc$  that retrieves the carrier band changes:

$$cbc_i[k] = \frac{\text{floor}(m_{conv,i}^*[k](N_{lv1} - 1))}{N_{lv1} - 1}, \quad (7)$$

enabling multiple consecutive switch-on or switch-off by summation with the two-level switching waveform. This means the reference / carrier intersection complexity is independent from the number of levels. This block provides two (vector) outputs: (i) the switching times  $\mathbf{t}$  and (ii) the switch position  $\mathbf{sp}$ .

### C. Flux ripple model

The inductor flux is the image of the output current ( $\psi_{L,i} = Li_{out,i}$ ). It corresponds to the time integral of the inductor voltage  $v_{L,i} = v_{conv,i} - (v_{out,i} + v_{CM})$ . However, as the primary interest is to obtain an inductor flux ripple model, it is enough to integrate only  $v'_{L,i} = v_{conv,i} - v_{CM}$ . As  $v'_L$  is piecewise constant, this task is trivial and computationally inexpensive. The time step is not constant, but is defined by the difference between two consecutive switching times. A fundamental component different from  $\langle i_{out,i} \rangle$  has to be subtracted to the integral, but the ripple content is preserved. This means the ripple waveform, hence the switched current, only depends on  $m_{conv,mod,i}^*$  and not on the output voltage (cf. Fig. 5(a)). For all subsequent results, unless specified,  $k = 0$ . It could be foreseen to compute and store the

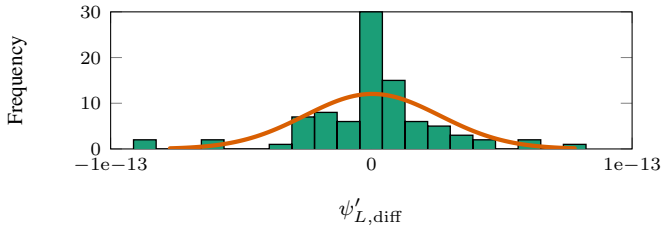


Figure 7: Normal distribution of the output flux difference at the phase switching instants.  $\psi'_{L,diff} = \psi'_{L,MATLAB} - \psi'_{L,PLECS}$ ,  $\mu = 3.6608e-16$  and  $\sigma = 2.5876e-14$ .

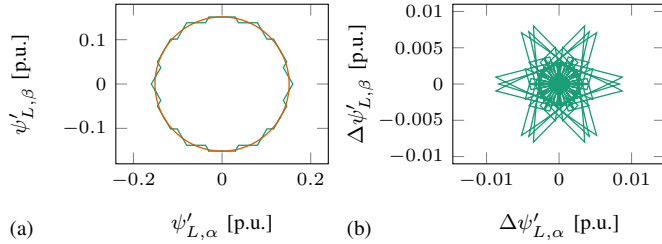


Figure 8: Results in  $\alpha\beta$  plane for  $N_{lvl} = 2$ ,  $p = 15$ ,  $M = 0.95$ ,  $n_{ph} = 3$ , asymmetrical sampling and min/max common mode voltage injection: (a) output flux (with  $\langle\psi'_{L,\alpha\beta}\rangle$  in —) and (b) output flux ripple trajectory.

values of  $\Delta\psi_{L,i}$  for a set of  $M$  values and use that lookup table during analysis. Notably, while  $v_{conv,i}$  is a piecewise constant waveform, implying  $\psi_{conv,i}$  to be piecewise linear, the instantaneous value of  $\Delta\psi_{L,i}$  will not be piecewise linear, as  $\langle\psi_{conv,i}\rangle$  is a sinusoid. The process is illustrated in Fig. 5(b). In addition, it is manifest from Fig. 5(a) that the envelope fails at capturing the switched current.

### III. SIMULATION RESULTS

The extended VSM method will be demonstrated in three steps: (i) benchmarking of the method against a PLECS switched model for a two-level three-phase converter in order to demonstrate the accuracy of the output flux obtained with the flux ripple model, (ii) demonstration of the method for one multi-level and -phase case and (iii) comparison of the semiconductor losses obtained with the extended VSM against both the original VSM proposal [1] and a detailed PLECS switched model.

#### A. Two-level three-phase case

First the simple two-level three-phase case is discussed. In Fig. 6, the result of the PD-PWM block is presented and compared with a PLECS model<sup>1</sup> with exactly the same parameters. The statistical distribution of the difference in the switched output flux in all phases between the proposed method and PLECS is shown in Fig. 7. A similar result is obtained when comparing the switching times in the common mode voltage. The accuracy of the proposed method is demonstrated. The flux and flux ripple trajectories in  $\alpha\beta$  plane are shown in Fig. 8. Note that, as  $k = 0$ , the converter and inductor flux

<sup>1</sup>PLECS solver configuration: variable time-step, DOPRI, maximum time step 0.01 s and relative tolerance  $1e-8$ .

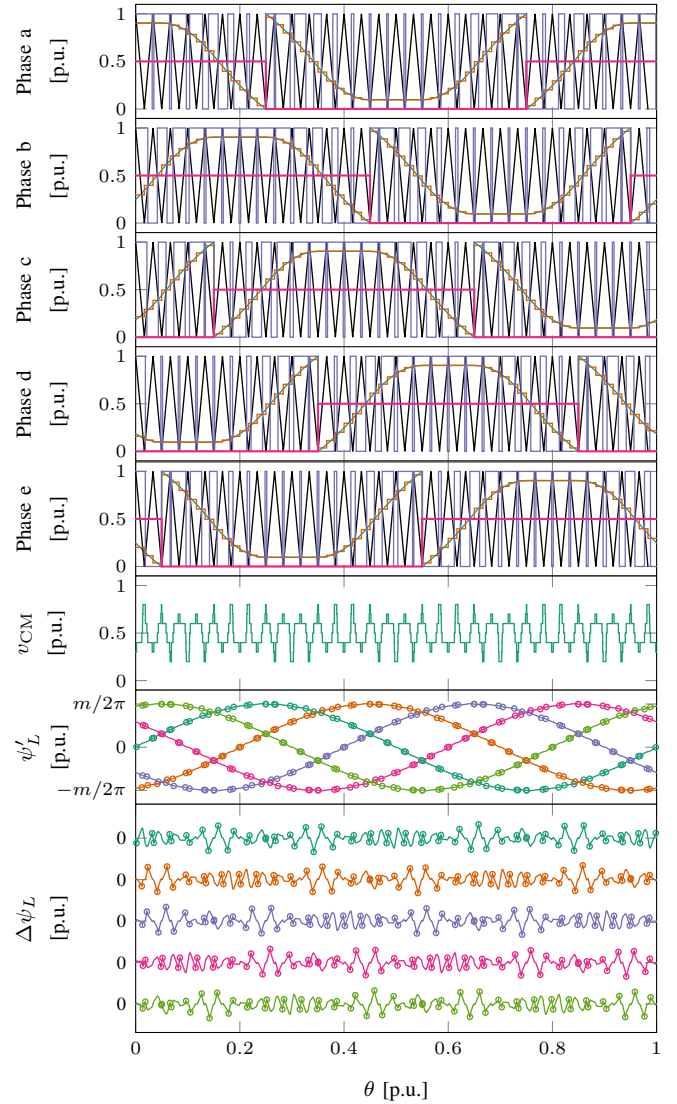


Figure 9: Results for  $N_{lvl} = 3$ ,  $p = 30$ ,  $M = 0.95$ ,  $n_{ph} = 5$ , asymmetrical sampling and flat-top common mode injection. In the phase carrier / reference intersection plots, — is cbc. O marks correspond to the instants where the respective phase is switching.

are identical ( $\psi'_{L,\alpha\beta} = \psi_{conv,\alpha\beta}$ ), with the common mode component normal to the  $\alpha\beta$  plane (not shown).

#### B. Three-level five-phase case

A three-level five-phase converter with flat-top common mode injection is taken to demonstrate the flux ripple method for multi-level and -phase applications. The results are summarized in Fig. 9. To capture the multilevel switching pattern, the single-phase carrier in combination with the carrier band change is used. The reference signal  $m_{conv,i}^*$  is replaced with the previously defined  $m_{conv,mod,i}^*$ . As  $N_{lvl} = 3$ , there will be one “folding” of the modulation index waveforms and only two transitions per period in the carrier band change waveforms  $cbc_i$ . The final multilevel switching pattern is reconstructed in each phase by the summation of the two-

TABLE I: Five-level diode clamped converter parameters

Variable	$V_{dc}$	$V_{l-l}$	$f_{out}$	$p$	$L_{out}$	$\angle i_{out}$
Value	10 kV	6.6 kV	20 Hz	30	10 mH	$\pi/2$

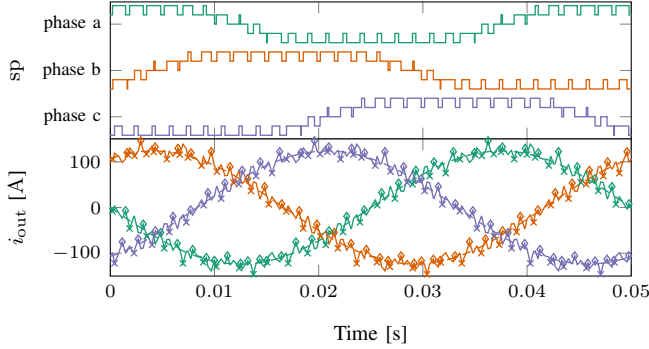


Figure 10: Waveforms obtained from the extended VSM method for a three-phase five-level diode clamped converter with the parameters of Table I and third harmonic common-mode injection.  $\times$  marks indicate turn-ON events, while  $\diamond$  marks indicate turn-OFF events. As an indication, the output current THD is 8.42%.

level switching pattern with the single-carrier and the carrier band change signal.

### C. Semiconductor losses for a five-level three-phase diode clamped converter

The losses obtained with the extended VSM method are compared against both the original VSM method and a switched PLECS model.

First of all, the switching pattern and output current waveforms are obtained for the parameters in Table I. They are shown in Fig. 10. The output current magnitude / output inductance value / pulse number are intentionally low in order to emphasize the output current ripple. While this step is common for all converter topologies that share the same number of phases, levels and output switching frequency, the following required step towards semiconductor loss calculation is topology specific, as the device waveforms (both current and voltage) have to be reconstructed from the switching pattern and output current waveforms.

A three-phase five-level diode clamped converter has been selected as example (cf. Fig. 11). Depending on the switch position  $sp$  and the output current polarity, the devices in conduction can be identified for the topology. This is summarized in Table II. The result of the application of Table II to the waveforms of Fig. 10 is shown in Fig. 12. Note that the device voltage waveforms are relevant in order to determine the zero voltage switching conditions for the diodes. This completely defines the set of data for the calculation of the conduction losses. Regarding the switching losses, a state transition diagram is established in Fig. 13. As there is no redundant switching combination, no additional decision algorithm is required. The semiconductor device is ABB SNG0150P45030 [10], with a junction temperature of 125 °C. The clamping diodes ( $D_{9..14}$ ) have the same characteristics as the anti-parallel diodes in the half-bridge IGBT module.

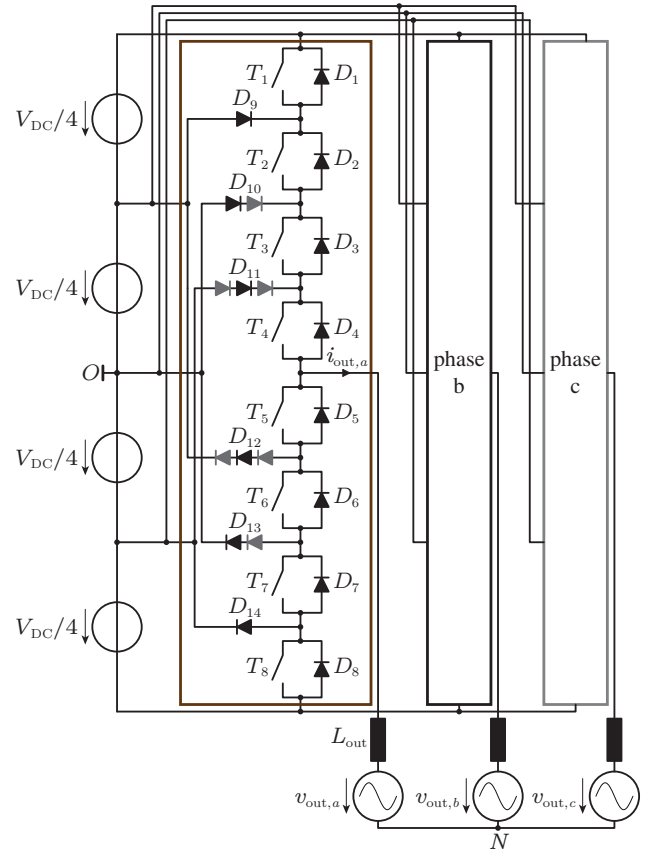


Figure 11: Three-phase five-level diode clamped converter. In reality, if similar semiconductor blocking voltages are used,  $D_{12}$  and  $D_{11}$  are made with three series-connected diodes, while  $D_{10}$  and  $D_{13}$  with two. Each voltage level is assumed to be maintained close to the ideal  $V_{DC}/4$  thanks to some balancing circuit [9]. Necessary static and dynamic snubbers for series-connected diodes are not discussed and outside the scope of the paper.

TABLE II: Switch combinations & active devices for one phase-leg of a five-level three-phase diode clamped converter. The switch position is defined as  $sp_i = \sum_j s_{j,i} - (N_{lv1} - 1)/2$  for odd  $N_{lv1}$ .

Switch position					Active devices	
$s_{1,i}$	$s_{2,i}$	$s_{3,i}$	$s_{4,i}$	$sp_i$	$i_{out,i} \geq 0$	$i_{out,i} < 0$
1	1	1	1	2	$T_{1..4}$	$D_{1..4}$
0	1	1	1	1	$D_9, T_{2..4}$	$D_{12}, T_5$
0	0	1	1	0	$D_{10}, T_{3..4}$	$D_{13}, T_{5..6}$
0	0	0	1	-1	$D_{11}, T_4$	$D_{14}, T_{5..7}$
0	0	0	0	-2	$D_{5..8}$	$T_{5..8}$

As the pulse number is an even multiple of 3, the switching pattern is phase-shifted by  $\pm 2\pi/3$  from phase  $a$  to the phases  $b$  and  $c$ . Hence, the semiconductor losses share the same distribution in all three phases. For this reason, only the semiconductor losses in phase  $a$  will be presented as results. The semiconductor losses for the original VSM method and the extended VSM are reported in Figs. 14 and 15, respectively. The relative error is defined with losses from PLECS as reference:

$$\varepsilon = \frac{x - x_{PLECS}}{x_{PLECS}} \cdot 100 [\%] \quad (8)$$

In the first comparison (Fig. 16), as the original VSM method



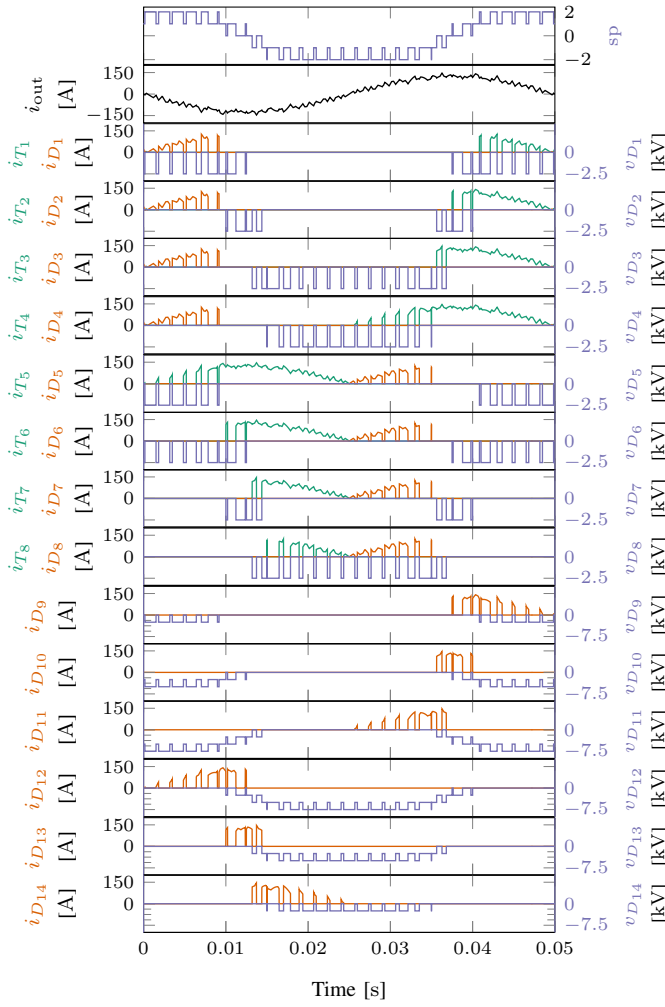


Figure 12: Devices current and voltage reconstruction in phase  $a$ , following Table II. Switchings only occur when the reference is within the carrier band that correspond to a given pair of switches, as there is no redundant switching combination.

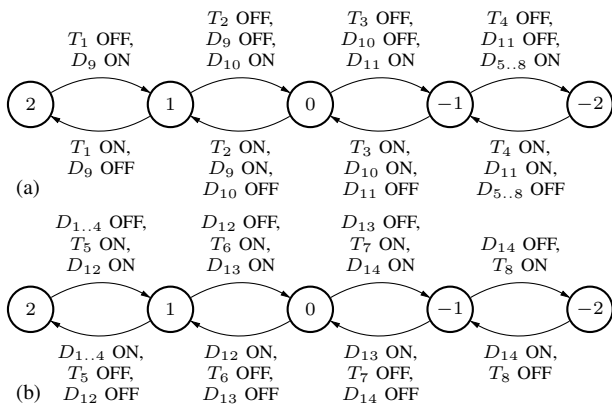


Figure 13: State transitions for one phase-leg of a five-level diode clamped converter: (a)  $i_{out} \geq 0$  and (b)  $i_{out} < 0$ . As there is no state redundancy, the switching combination  $[s_1, s_2, s_3, s_4]$  can be replaced by the switch position  $sp$  without loss of information.

only considers a purely sinusoidal output current at fundamental frequency, large errors are observed. This confirms that the

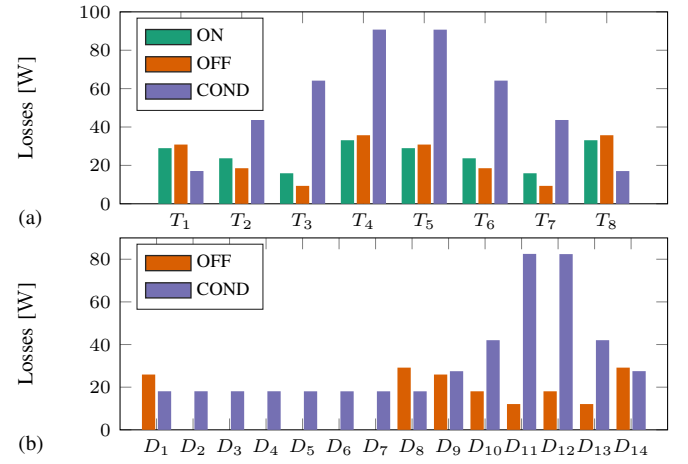


Figure 14: Semiconductor losses in phase  $a$  obtained with the original VSM method for: (a) IGBTs and (b) diodes.

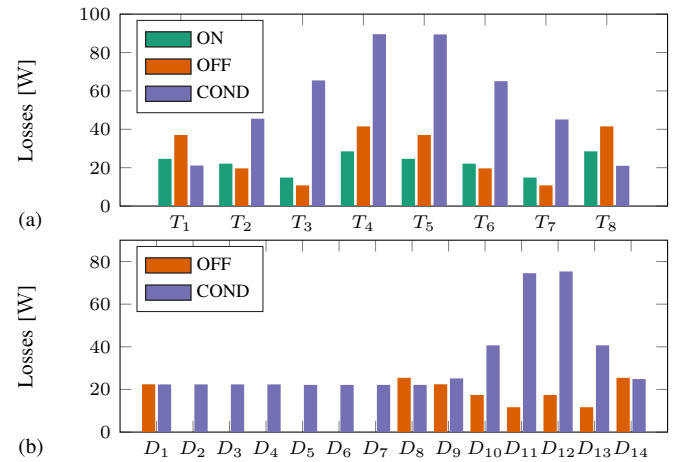


Figure 15: Semiconductor losses in phase  $a$  obtained with the extended VSM method for: (a) IGBTs and (b) diodes.

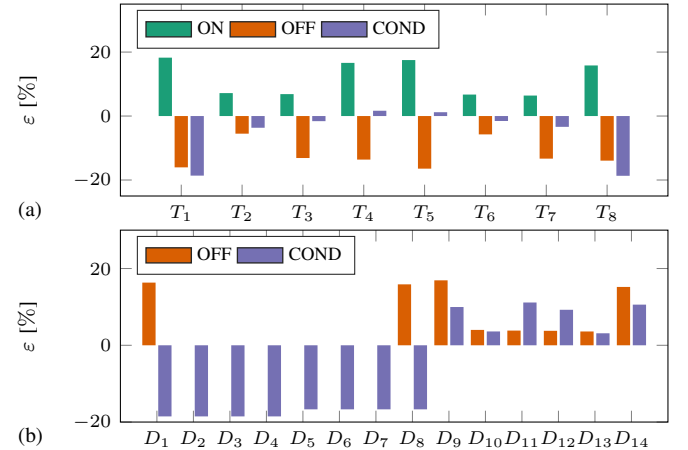


Figure 16: Semiconductor losses relative errors between the original VSM method applied to conventional multi-level converters and the PLECS switched model in phase  $a$  for: (a) IGBTs and (b) diodes.

original VSM method is not suited for conventional multi-level converters operated at low switching frequencies. In the second

$$m_{CM,mm}(t) = -M \frac{\cos\left(\text{mod}\left(2\pi f_{\text{out}}t - \frac{\pi}{n_{\text{ph}}}, \frac{2\pi}{n_{\text{ph}}}\right) - \frac{\pi}{n_{\text{ph}}}\right) + \cos\left(\text{mod}\left(2\pi f_{\text{out}}t, \frac{2\pi}{n_{\text{ph}}}\right) + \frac{(n_{\text{ph}}-1)\pi}{n_{\text{ph}}}\right)}{2} \quad (10a)$$

$$m_{CM,ft}(t) = -M \text{sgn}\left(\text{mod}\left(2\pi f_{\text{out}}t - \frac{\pi}{2n_{\text{ph}}}, \frac{2\pi}{n_{\text{ph}}}\right) - \frac{\pi}{n_{\text{ph}}}\right) \left[ \cos\left(\text{mod}\left(2\pi f_{\text{out}}t - \frac{\pi}{2n_{\text{ph}}}, \frac{\pi}{n_{\text{ph}}}\right) - \frac{\pi}{2n_{\text{ph}}}\right) - \cos\left(\frac{\pi}{2n_{\text{ph}}}\right) \right] \quad (10b)$$

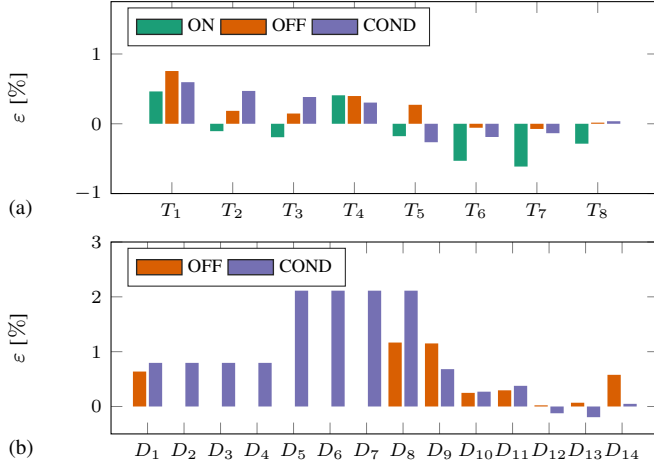


Figure 17: Semiconductor losses relative errors for the extended VSM method and the PLECS switched model in phase  $a$  for: (a) IGBTs and (b) diodes.

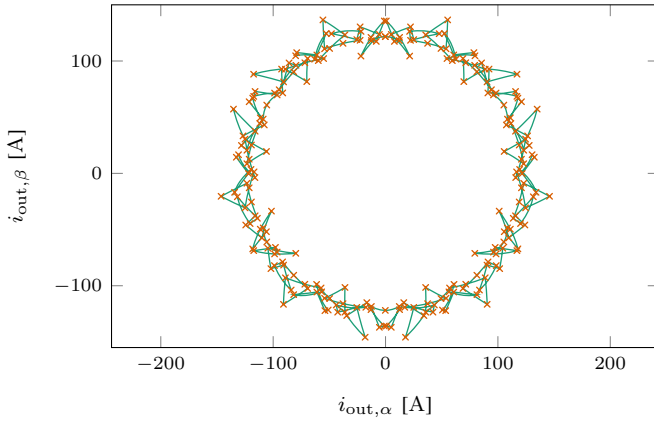


Figure 18: Output current trajectory in  $\alpha\beta$  plane, with — the trajectory from the PLECS switched model and  $\times$  marks from the extended VSM method at the switching instants.

comparison (Fig. 17), the relative errors come from different loss scalings and interpolation methods, as the output current difference is smaller than 1 mA (cf. Fig. 18). This definitively confirms the relevance and accuracy of the extended VSM method.

#### IV. CONCLUSION

The VSM method extended with an output flux ripple model has been successfully applied to conventional multi-level and -phase converters with low output current waveform quality. In particular, the key role of the common mode voltage has been stressed. This is what makes the multi-phase analysis more

complicated than the single-phase one. In multiphase systems, the switching events occurring in any phase affect the output current in every phase. Unlike the output current envelope expressions, the extended VSM method is able to capture the exact switched output current. This is of high relevance in the converter design phase for semiconductor loss calculation, as it has been shown through detailed loss comparisons. The generalization to multilevel converters is of low complexity thanks to the single-carrier method, while the extension to multiphase ones is straightforward. The very good matching with the PLECS switched models has validated the proposed method at a conceptual level. Finally, the comparison with the original VSM, where the output current quality assumption was far from being verified, has backed the improvement offered by the extended VSM method with the capture of the exact output flux / current ripple.

#### ACKNOWLEDGMENTS

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#### APPENDIX A

##### COMMON MODE INJECTION EXPRESSIONS FOR MULTI-PHASE SYSTEMS

The expressions for each common mode injection method are, respectively:

$$m_{CM,n_{\text{ph}}-th} = -M \frac{\sin(\pi/(2n_{\text{ph}}))}{n_{\text{ph}}} \cos(2\pi n_{\text{ph}} f_{\text{out}} t) \quad (9a)$$

$$m_{CM,mm} = -\frac{\min\{\mathbf{m}_{\text{conv fund}}^*\} + \max\{\mathbf{m}_{\text{conv fund}}^*\}}{2} \quad (9b)$$

$$m_{CM,ft} = -\sum_{i=1}^{n_{\text{ph}}} \max \left\{ \min \left\{ m_{\text{conv fund},i}^*, \right. \right. \\ \left. \left. M \cos(\pi/(2n_{\text{ph}})) \right\}, -M \cos(\pi/(2n_{\text{ph}})) \right\} \quad (9c)$$

where  $\mathbf{m}_{\text{conv fund}}^* = [m_{\text{conv fund},1}^*, \dots, m_{\text{conv fund},n_{\text{ph}}}^*]$ . In any case, only odd harmonics multiple of  $n_{\text{ph}}$  are used. While the expressions for the min/max and flat-top common mode injection methods are suitable for real-time implementation, they are not for analytical studies, as it is the case in this paper for the definition of  $m_{\text{conv},i}^*(t)$  (cf. Fig. 3). This is the reason why replacement expressions that avoid  $\min\{\cdot\}$  and  $\max\{\cdot\}$

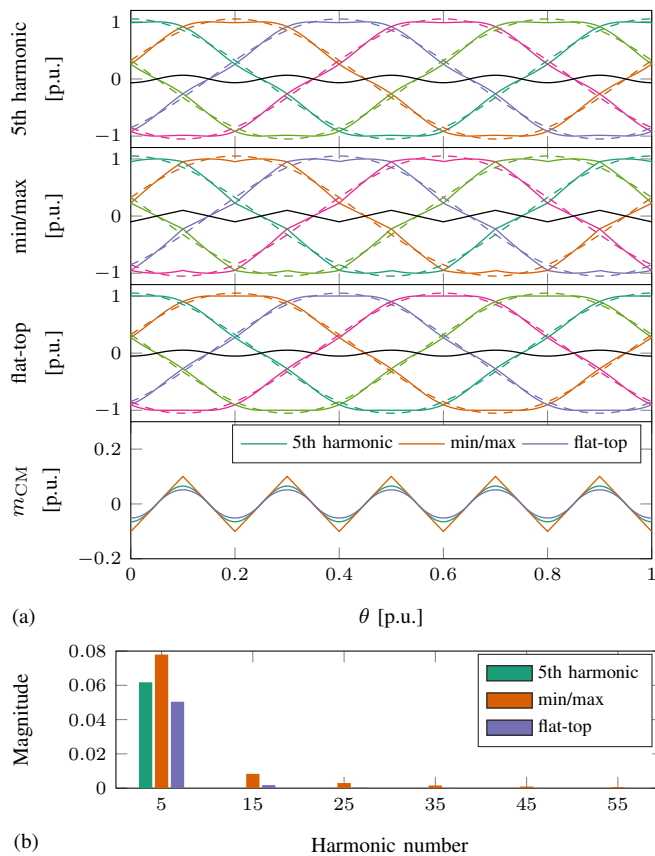


Figure 19: Common mode injection methods illustrated for  $n_{ph} = 5$  and  $M = 1/\cos(\pi/10)$ : (a) phase reference signals for each common mode injection method with the common mode signal in black and the fundamental in dashed lines and (b) relative harmonic distributions of  $m_{CM}(t)$  (scaled by  $M$ ).

are presented in (10). An example of the resulting waveforms and harmonic distributions for  $n_{ph} = 5$  is presented in Fig. 19. The flat-top common mode injection method has the advantage of featuring the lowest peak common mode signal amplitude.

#### APPENDIX B HALF SAMPLING TIME PHASE-SHIFT ASSUMPTION CORRECTION

As mentioned, the phase-shifting of the reference signal by  $T_s/2$  before sampling is an approximation, valid only if  $m_{conv,i}^*$  is linear over a sampling interval  $[kT_s, (k+1)T_s]$ . As a result, the obtained fundamental magnitude component differs slightly from the analytical one expected. This means the flux ripple will not be equal to zero at the reference sampling instants, if the ideal analytical one is subtracted from it. This is particularly visible for the flux ripple trajectory in  $\alpha\beta$  plane. Fig. 20 compares the obtained flux ripple trajectories without and with compensation. In Matlab, a sine curve fitting (of the form  $A \sin(2\pi f_{out}t + B) + C$ ) at the sampling instants (i.e. when the flux ripple has to be zero by construction) on  $n_{ph} - 1$

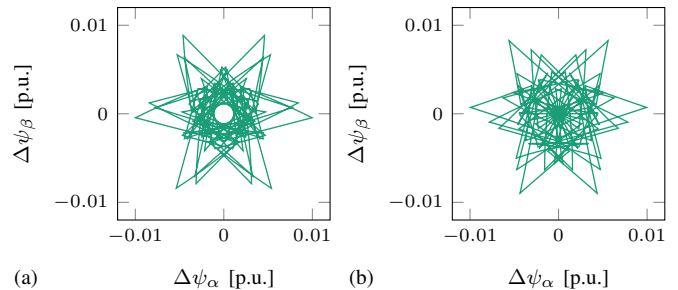


Figure 20: Sampling correction for  $N_{lvl} = 2$ ,  $p = 15$ ,  $M = 0.95$ ,  $n_{ph} = 3$ , symmetrical sampling and min/max common mode voltage injection: (a) without correction and (b) with correction factor ( $A/M = 0.9853$ ).

phases is performed, so that the (small) amplitude difference can be compensated and the initial value properly corrected. In the PLECS switched model simulations, the inductor currents are initialized to the values used for the initial correction in the extended VSM method, i.e. the parameter  $C$ .

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